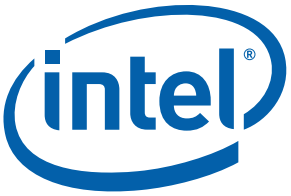


Intel® Atom™ Processor S1200 Product Family for Microserver

Datasheet, Volume 1 of 2

December 2012

Document Number: 328194-001

Revision History

Date	Revision	Description
November 2012	1.0	Initial release.

Contents

Figures

Tables

§ §

1 Overview

1.1 Introduction

The Intel® Atom™ Processor S1200 Product Family for Microserver is the new generation of System-On-Chip (SoC) 64-bit processors built using Intel 32-nanometer process technology. Throughout this document, the Intel® Atom™ Processor S1200 Product Family for Microserver is also referred to as the processor, SoC, or S12x0.

This document relates to the following product SKUs:

Table 1. Intel® Atom™ Processor S1200 Product Family

SKU Name	TDP
Intel® Atom™ Processor S1260	8.5 W
Intel® Atom™ Processor S1240	6.3 W
Intel® Atom™ Processor S1220	8.1 W

The SoC is targeted for segments focusing on highly dense, low power server configurations (i.e., Microserver) as shown in Figure 1-1 and the traditional Small and Medium Business (SMB) server segment as shown in Figure 1-2.

Figure 1-1. Multi-Node Microserver Configuration

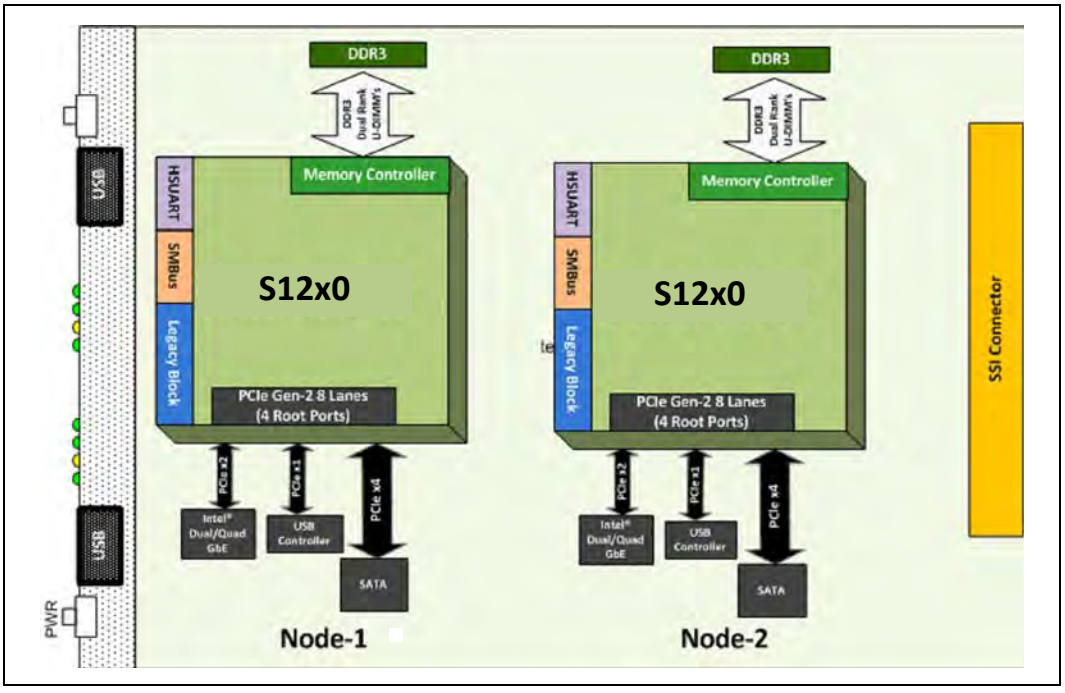
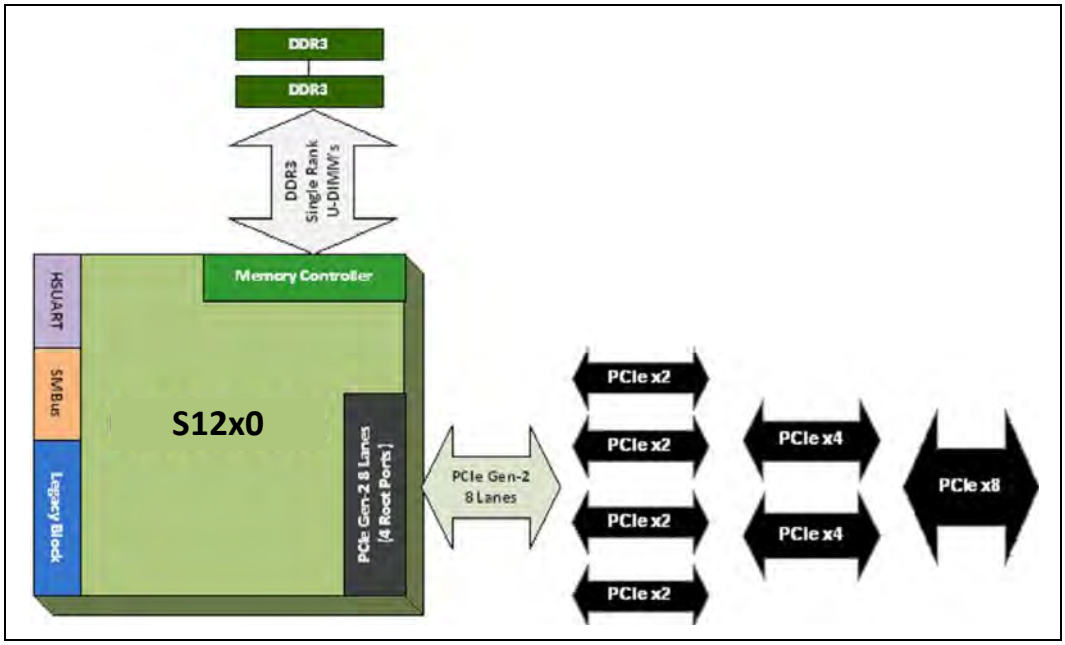


Figure 1-2. SMB Server Configuration

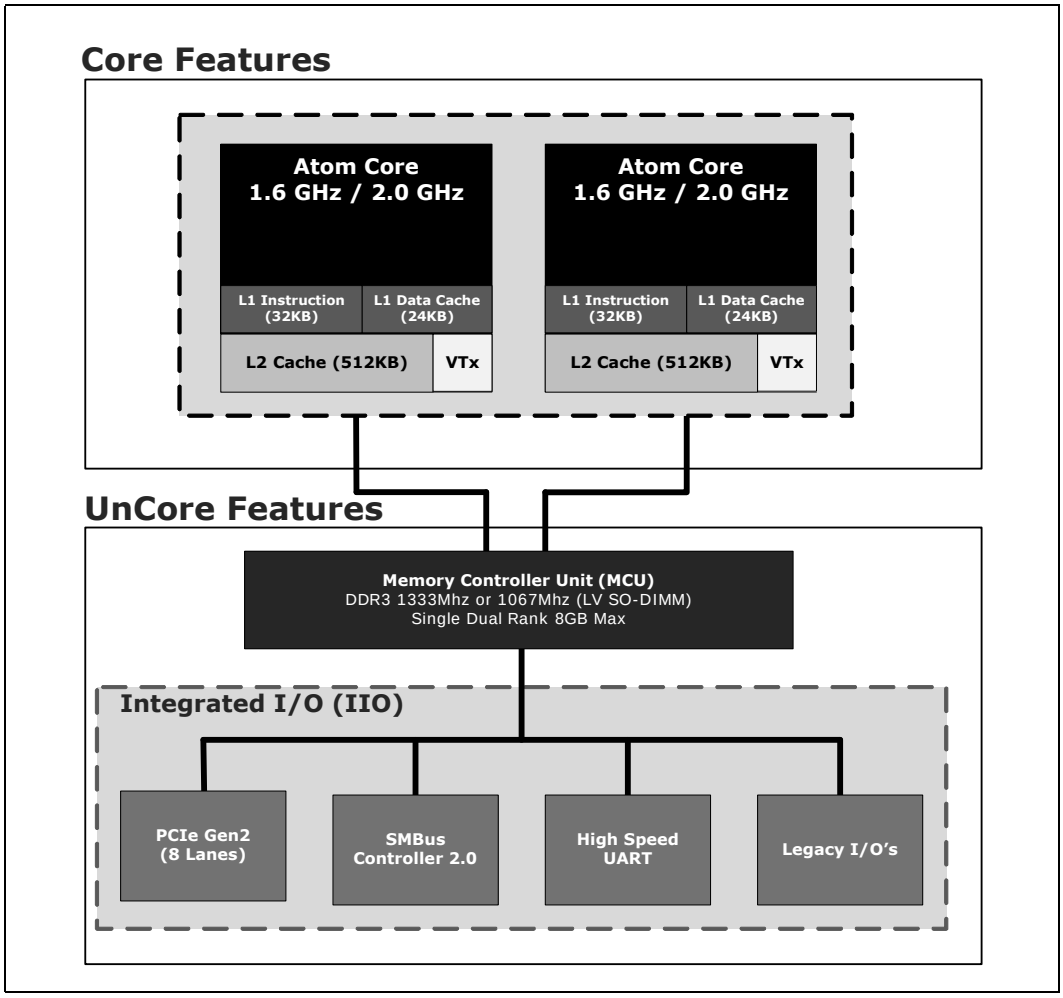


1.2 Key Features of the Processor

- Number of cores: Dual core with two threads per core
- Operating Frequency: 1.6GHz/2.0GHz depending on the SKU
- Cache/Core Includes:
  - 32KB, 4-way L1 instruction cache
  - 24KB, 6-way L1 data cache
  - 512KB, 8-way L2 Cache per Core (Total of 1024KB)
- Supports 36-bit physical addressing
- Target TDP (Thermal Design Power) Consumption:
  - 8.5W (Intel® Atom™ Processor S1260)
  - 6.3W (Intel® Atom™ Processor S1240)
  - 8.1W (Intel® Atom™ Processor S1220)
- Supports C1, C2, C4 and C6 CPU states
- Supports single channel DDR3 with ECC support:
  - 72-bits data bus (64bit data + 8 bit ECC)
  - 1067MT/s and 1333MT/s data rate with U-DIMM and SO-DIMM support
  - Supports single, dual, or two single-rank DIMM
  - Supported memory size from 512MB to 8GB with x8/x16 DRAM devices (x16 device with non-ECC only)
  - Supported DRAM densities 1Gb, 2Gb and 4Gb device technology
  - Low Voltage (LV) SO-DIMM is supported at 1066MT
- Supporting up to 8 lanes with up to four PCIe* Gen 2 ports (controllers). These can be configured as:
  - One PCIe x8 ports OR
  - Two PCIe x4 ports OR
  - Four PCIe x2 ports OR
  - One PCIe x4 and Two PCIe x2ports
- Memory RAS Features Includes:
  - Hardware based Memory Scrubbing (Demand and Patrol Scrubs)
  - Data and Address Parity Protection (SEC-DED-ECC)
  - Error Injection
  - Data Scrambling
  - Memory Region Isolation
- Supports Intel® 64-bits with CPU virtualization VT*x*
- Integrated Legacy Interfaces includes:
  - SMBus
  - GPIO
  - High Speed UART
  - LPC Bus

This section describes the key S12x0 architecture features of the Core and UnCore modules of the S12x0 family.

Figure 1-3. Intel® Atom™ Processor S1200 Product Family for Microserver High-Level Block Diagram



1.2.1 Intel® Atom™ Core Features and Caching Hierarchy

- 1.6GHz/2.0GHz Intel® Atom™ Core, Two Cores support.
- Features per core:
  - — Two thread per Core.
  - — Support for Intel® 64 Bits, VT*x* Compatible.
  - — 36 bits physical address.
- Caching Hierarchy - two levels:
  - — 32KB, 4-way L1 Instruction Cache (ICU).
  - — 24KB, 6-way L1 Data Cache (DCU).
  - — 512KB, 8-way L2 cache.
- Addressing Space:
  - — 36 bits physical address.
  - — 48 bits virtual address space.

1.2.1.1 Processor Core Technologies

The S12x0 core offers several technologies. Table 1-2 describes these technologies implemented by the S12x0 core.

Table 1-2. Technologies in Processor Core

Name	Short Description
VT*x*	VT eXtension supports virtualization of processor hardware for a multiple software environment.
Execute Disable Bit	Execute Disable Bit: The Intel Execute Disable Bit functionality can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system.
Hyper-Threading Technology	Intel® Hyper-Threading Technology: Allows each Intel Atom execution core to function as two logical processors.
Enhanced Intel SpeedStep® Technology	Enhanced Intel SpeedStep® Technology: Enables very high performance while meeting the power-conservation needs of the platform.
Intel® Thermal Monitor and Thermal Monitor 2	Briarwood core processor supports a digital thermal sensor that will provide per thread temperatures.
SSE 3.0	Streaming SIMD Extensions 3.0

1.2.2 UnCore Features

This section describes key features supported by each of the UnCore modules designed specifically for the microserver processor segment. Detailed descriptions of these key modules is provided in subsequent chapters.

1.2.2.1 Integrated Memory Controller (iMC)

The S12x0 contains an integrated 72-bit single channel memory controller that supports discrete DDR3 DRAM devices, a single dual-rank DIMM, or two single-rank DIMMs. The data bus width of 72 bits supports 64-bit data and an 8-bit ECC.

Key features are as follows:

- Single channel DDR3 memory controller:
  - — One or Two rank UDIMMs and VLP DIMMs support
  - — DIMMs supports include 1.5V Only
  - — SO-DIMMs supports include both 1.5V and Low Voltage (*LV*) 1.35V SO-DIMMs
- Supports 1066 MT/s (*Max speed supported with Low Voltage SO-DIMM*) and 1333MT/s DDR3 frequencies
- Supports total memory size of 512MB up to 8GB:
  - — Supports x8 and x16 (x16 device with non-ECC only) DRAM device widths
  - — Supports 1Gb, 2Gb and 4Gb DRAM device densities
  - — Supports 1 or 2 ranks (*2 chip selects*), dual ranks must be identical
- 72-bit data bus (*64-bit data and 8-bit SEC-DED-ECC*):
- Supported data reliability features
  - — Demand and Patrol memory scrub
  - — Error injection on write/read data paths including address matching
  - — DDR Data Scrambler to reduce power supply noise, improve signal integrity and to encrypt/protect the contents of memory
- Supports different physical address mappings to optimize for performance
- Aggressive power management to reduce power consumption
- Supports 1N/2N/3N mode for DRAM command
- Out-of-order request service for increased performance
- Opportunistic and per-rank refresh for reduced performance impact

1.2.2.2 Integrated I/O (IIO)

The S12x0 provides an integrated I/O module, which consists of high-speed and legacy I/O interfaces.

Features included are:

- PCI Express* Version 2.1 Root Port interfaces - Up to eight lanes of PCIe
- Supports up to eight lanes with up to four PCIe gen2 root ports (controllers).
- System Management bus (SMBus 2.0) Controller
- Legacy I/O

1.2.2.2.1 PCI Express Interface (PCIe)

S12x0 provides a number of integrated PCI Express Gen2 Root Ports for flexible I/O connectivity. The following are key attributes of the PCI Express interface:

— Gen2 speeds at 5GT/s (backward compatible to PCIe Gen1 2.5GT/s)

— x8 interface bifurcated down to one x8 or two x4 or four x2

1.2.2.2.2 System Management Bus (SMBus) 2.0 Controller

The S12x0 provides two System Management Bus (SMBus) 2.0 host controllers.

An SMBus controller is a two-wire bus that support multiple devices both as Masters and Slaves. Generally, a bus Master device:

- initiates a bus transfer between it and a single SMBus Slave.
- provides the clock signals.

The SMBus 2.0 Controller is based on the *System Management Bus (SMBus) Specification*, Version 2.0 and was introduced as an alternative higher-power set of electrical characteristics versus the earlier version 1.0 and 1.1. This higher-drive capability is required when implementing PCI Express throughout the system.These host controllers are part of the S12x0 System Management Transport and are treated as integrated PCI endpoint devices. It also enabled Plug and Play support.

1.2.3 Legacy I/O Features

The Legacy Block consists of legacy modules some of which are required for Windows and other PC OS hardware compatibility.

The Legacy Block consists of modules like Real Time Clock, Timers, Interrupt Controllers, General Purpose I/O, LPC Interface, etc.

- Timers:
  - 8254 Programmable interval Timers (PIT).
  - Real-Time Clock (RTC).
  - High-Precision Event Timer (HPET).
- Interrupt Controller:
  - 8259 Programmable Interrupt Controllers (PIC).
  - I/O Advanced Programmable Interrupt Controller (IOAPIC) 1.1.
- Interfaces:
  - High-Speed UART.
  - Low Pin Count (LPC) 1.1.
  - General-Purpose I/O (GPIO).
  - Serial Peripheral Interface (SPI).
  - SMBus 1.0 Controller.
- Miscellaneous:
  - Interrupt Routing.
  - GPIO Functional MUXing.

1.3 Power Management Support

1.3.1 Power Management Features

Below are the S12x0 power management features:

- ACPI Platform Sleep State support: S0, S3, S4, S5
- ACPI Processor (CPU) C States: C0, C1, C2, C4, C6
- ACPI Device States: D0, D3
- PCI Express: L0, L0s, L1, L2, L3
- Enhanced Intel SpeedStep® Technology
- Hardware throttling
- Clock Gating
- Thermal throttling
- Dynamic I/O power reductions (disabling sense amps on input buffers, tri-stating output buffers)
- Reprogrammable Power Management Unit (PMU)
- Reprogrammable thermal management algorithms performed by PMU
- DDR3 SDRAM memory controller and PHY:
  - Dynamic Rank Power Down
  - Dynamic power down is employed during normal operation. If all the pages have been closed at the time of CKE pin de-assertion, the SDRAM devices enter the precharge power-down state. Otherwise the devices enter the active power-down state.
  - Conditional Memory Self-Refresh
  - DLL master/slave shutdown based on CPU state
  - Address and command signal tri-state when all memory is in power-down, self-refresh, or when not in use (no chip select asserted)
  - Chip-select tri-state for a powered-down row
  - Clock tri-stating for unpopulated DIMMs
  - CKE/CS tri-stating for unpopulated rows
  - Conditional Memory Self-Refresh during C2-C4-C6
  - Conditional and software directed Memory Self-Refresh
    Supports conditional self-refresh entry in the C2-C6 states, based on memory request traffic from host interface agents
- Debug and Testability hooks

1.4 Thermal Management Support

The S12x0 implements configurable forms of Thermal Management for itself, the DDR3 SDRAM, and system-level thermal limits. It supports both thermal-sensor-based and event-counter-based thermal management. It has several forms of threshold evaluation called trip mechanisms. It also has one configurable form of threshold enforcement called throttling with four unique limits.

The S12x0 contains many techniques to help better manage thermal attributes of the processor:

- Intel® Thermal Monitor and Intel® Thermal Monitor 2:
  - — Provides thermal management.
- Enhanced Digital Thermal Sensor (DTS):
  - — One Digital Thermal Sensor per core of the dual-core S12x0.
  - — Provides per-thread temperature sensing.

For additional information about implementing the thermal-management features in this document, refer to the Thermal/Mechanical Design Guide (TMDG) document for the S12x0.

1.5 Package Summary

The S12x0 is manufactured in a 34mm x 28mm Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with 1283 solder balls on the bottom side.

1.6 Terminology

A '_N', '#', '_B', or 'B' symbol after a signal name refers to an active low signal indicating a signal is in the active state when driven to a low level. When RESETB, for example, is low, a reset has been requested.

Table 1-3. Processor Terminology (Sheet 1 of 2)

Term	Description
DDR3	Third generation Double Data Rate SDRAM memory technology that is the successor to DDR2 SDRAM
DMA	Direct Memory Access
ECC	Error Correction Code
Enhanced Intel SpeedStep® Technology	Allows the operating system to reduce power consumption when performance is not needed.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
IIO	The Integrated I/O Controller. An I/O controller that is integrated in the processor die.
iMC	The Integrated Memory Controller. A Memory Controller that is integrated in the processor die.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture. Further details on Intel 64 architecture and programming model can be found at http://developer.intel.com/technology/intel64/.
Intel® Virtualization Technology (Intel® VT)	Processor Virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
Integrated Heat Spreader (IHS)	A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
Jitter	Any timing variation of a transition edge or edges from the defined Unit Interval (UI).
LLC	Last Level Cache
LRU	Least Recently Used. A term used in conjunction with cache hierarchy.
MLC	Mid Level Cache
PCODE	Power Management Unit (PMU) micro-code.
PMU	Power Management Unit.
PCI Express	PCI Express Generation 2.0
Processor	The 64-bit, single-core or multi-core component (package)
Processor Core	The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache.
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DDR3 DIMM.
SSE	Intel® Streaming SIMD Extensions (Intel® SSE)
So-DIMM	Small outline Dual In-line Memory Module

Table 1-3. Processor Terminology (Sheet 2 of 2)

Term	Description
SMBus	System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system. It is based on the principals of the operation of the I2C* two-wire serial bus from Philips Semiconductor.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power
TSOD	Temperature Sensor On DIMM
UDIMM	Unbuffered Dual In-line Memory Module
Unit Interval	Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,…., t_k then the UI at instance “n” is defined as: $UI_n = t_n - t_{n-1}$
V_{CC}	Processor core power supply
V_{SS}	Processor ground
x1	Refers to a Link or Port with one Physical Lane
x4	Refers to a Link or Port with four Physical Lanes
x8	Refers to a Link or Port with eight Physical Lanes

1.7 Related Documents

Refer to the following documents for additional information.

Table 1-4. Related Documents

Document†	Document Number/Location
Processor Documents	
Intel® Atom™ Processor S1200 Product Family for Microserver Datasheet, Volume 2 of 2	328195
Intel® Atom™ Processor S1200 Product Family for Microserver Thermal/Mechanical Design Guide (TMDG)	328196
Intel® Atom™ Processor S1200 Product Family for Microserver Boundary Scan Description Language (BSDL) File	328197
Intel® Atom™ Processor S1200 Product Family for Microserver Specification Update	328198
Public Specifications	
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info
PCI Local Bus Specification, Revision 3.0 (February 3, 2004) *PCI Local Bus Specification*, Revision 2.1 (November 18, 2010; plus Errata)	http://www.pcisig.com/specifications
PCI Express Base Specification, Revision 3.0 (November 10, 2010)	
PCI-to-PCI Bridge Architecture Specification, Revision 1.2 (June 9, 2003)	
PCI Bus Power Management Interface Specification, Revision 1.2 (March 3, 2004)	
DDR3 SDRAM Specification	http://www.jedec.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide Volume 3B: System Programming Guide Intel® 64 and IA-32 Architectures Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm

1.8 State of Data

The data contained within this document is the most accurate information available by the publication date of this document.

2 Interfaces

2.1 Integrated Memory Controller

2.1.1 Introduction

The S12x0 contains an integrated 72-bit, single channel Memory Controller (iMC) that supports discrete DDR3 DRAM devices, a single dual-rank DDR3 UDIMM/SO-DIMM, or two single-rank DDR3 UDIMMs/SO-DIMMs.

The data bus width of 72 bits supports 64-bit data and an 8-bit ECC. The memory controller supports data rates from 800MT/s to 1333MT/s. The supported DRAM device densities are 1Gb, 2Gb and 4Gb. The SDRAM device data width is either x8 or x16 and the memory controller supports either 1 or 2 ranks. Note that x16 devices are only supported in non-ECC configurations. Currently, there has been no post-Silicon validation of any ECC enabled x16 device configurations. ECC DIMMs do not use x16 devices.

2.1.2 Supported Features

The key features of the DDR3 memory interface are summarized in the following list.

- Single channel DDR3 memory controller:
  - — One- or two- rank Unbuffered DIMMs (UDIMMs) and Small-Outline DIMMS (SO-DIMMs) supported.
  - — UDIMM support is for 1.5V devices only.
  - — SO-DIMM support for both 1.5V and Low Voltage (LV) 1.35V SO-DIMMs.
- DRAM speeds supported: 800, 1067 (*the maximum speed supported for Low-Voltage SO-DIMM*), and 1333 MT/s.
- Supports total memory size of 512MB up to 8GB:
  - — Supports x8 DRAM device widths (ECC and non-ECC configurations).
  - — Supports x16 DRAM device width only with non-ECC configurations
  - — Supports 1Gb, 2Gb and 4Gb DRAM device densities.
  - — Supports 1 or 2 ranks (*2 chip selects*), dual ranks must be identical.
- 72-bit data bus (*64-bit data and 8-bit SEC-DED-ECC*).
- Supported data reliability features:
  - — Demand and Patrol memory scrub.
  - — Error injection on write/read data paths including address matching.
  - — DDR Data Scrambler to reduce power supply noise, improve signal integrity and to encrypt/protect the contents of memory.
- Supports different physical address mappings to optimize for performance.
- Aggressive power management to reduce power consumption.
- Supports 1N/2N/3N mode for DRAM command.
- Out-of-order request service for increased performance.
- Opportunistic and per-rank refresh for reduced performance impact.

2.1.3 Functional Description

The DDR3 Memory Controller supports three DDR3 transfer rates:

- 800MT/s (6.4GB/s).
- 1067MT/s (8.5GB/s).
- 1333MT/s (10.7GB/s).

Serial Presence Detect (SPD) discovery is used by BIOS to determine the number of DIMMs populated, the number of ranks per DIMM, the device width, density and the speed.

2.1.3.1 DRAM Requests and Data Ordering

The memory controller supports four unique command requests from the root complex:

- 32 byte write, 32 byte aligned (address [4:0] = 0).
- 64 byte write, 64 byte aligned (address [5:0] = 0).
- 32 byte read, 32 byte aligned (address [4:0] = 0).
- 64 byte read, 32 byte aligned (address [4:0] = 0).

The memory controller does not support partial writes because of the ECC protection and because the DDR3 I/O signals do not support data masks. The root complex is configured to disable partial writes by performing an underfill read, followed later by a full 32 or 64 byte write.

The memory controller can reorder the root complex requests ito optimize the memory bandwidth. It operates, however, under the following restrictions:

- Requests that address the same cache line (address[35:6]) are performed in the same order as received from the root complex
- Requests are performed in order if this feature is disabled (DSCH[8]=1) or if a request has reached the out-of-order aging threshold (DSCH[4:0]).

2.1.3.2 DRAM Out of Bound Access

The iMC sends an out-of-bound write access to DDR3 memory without any chip selects asserted low. This prevents the corruption of the memory. Out-of-bound read accesses are sent to DDR3 memory but the memory controller returns 0xFF data to the internal memory arbitration unit of the S12x0. This is done to prevent data from secured addresses returning by wrapped around addresses.

Note: In a correctly configured system, the memory controller should never receive an out of bounds access from the SoC Root Complex.

2.1.3.3 DRAM Power Management

Power Management involves managing and reducing the power consumed by both the memory controller and the DRAM devices. The DRAM devices provide two ways to reduce power consumption: Power Down mode and Self Refresh. The memory controller manages these two power saving modes, and in addition, controls a number of its own components to further reduce power consumption. The memory controller supports memory power management in the following conditions:

- **Active Power Down** - No commands are visible for the rank, the rank power down idle timer has expired and one or more pages are open
- **Pre-charge Power Down** - No commands are visible for the rank, the rank power down idle timer has expired and all pages are closed
- **Dynamic Self Refresh** - Dynamic self-refresh is enabled, all pages in all ranks are closed, no commands in the command queue or being received from the north cluster, the status priority level from the root is below 2, and the self-refresh idle timer has expired
- **Self Refresh** - If enabled, entered when the system transitions to suspend mode.

2.1.3.3.1 Power Down Modes

When DRAM is in Power-Down mode, all input and output buffers are deactivated, excluding CK, CK#, ODT, CKE and RESET#, and the DRAM internal clock is disabled. Power- Down is applied per rank whenever a rank is inactive. DDR3 supports 3 types of Power-Down modes: **Active Power-Down** (*at least one bank in the PD rank is open*), **Precharge Power-Down** (*all banks in the PD rank are closed*) and **DLLoff mode**. The DLLoff mode is only supported as long as the ranks are self terminating. This means that the DODT register is configured to drive only the same rank ODT signal as the rank targeted with the read/write command.

The memory controller supports a programmable power management command that is sent to the DDRIO physical layer to enter a low power mode. The selection of low power mode is entered is based upon power savings versus self-refresh exit latency. In general, the higher power saving states require larger self-refresh exit latencies because it takes longer to power on all of the features.

2.1.3.3.2 Dynamic Self Refresh Mode

The memory controller also supports Dynamic Self Refresh during normal operation to support the maximum power savings mode. It wakes the memory from Self Refresh whenever a memory request is received, then re-enters Self Refresh mode when the memory controller is idle and the self-refresh timer expires.

2.1.3.3.3 Page Management

The memory controller is capable of closing pages after the page has been idle for a configurable period of time. This benefits the system for both power and performance. From a performance standpoint, it helps since it can reduce the number of page misses encountered. From a power perspective, it allows the memory devices to reach the precharge power management state (*power down when all banks are closed*), which has better power saving characteristics on most memory devices than when the pages are left open and the device is in Active Power-Down mode.

2.1.3.3.4 Self Refresh Modes

Self Refresh can be used to retain data in the DRAM devices even if the rest of the system is powered down. When the memory is in Self Refresh, the memory controller disables all output signals except the CKE and RESET# signals. Self-Refresh has 2 main usage modes:

- Power-saving during S0 idle periods.
- Sustaining DRAM content when the system moves to S3 power state.

There are two modes for system triggered Self-Refresh Entry/Exit: dynamically and via IOSF-SB messages. Additionally, DDRIO may initiate a short SR Exit/Entry cycle for periodic RCOMP updates.

2.1.3.3.5 Refresh Mode

In general, a Refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be postponed during operation of the DDR3 SDRAM. This means that at no point in time more than a total of eight Refresh commands can be postponed.

In case eight Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9×tREFI. A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”) with each one reducing the number of regular Refresh commands required later by one.

2.2 PCI Express Interface

2.2.1 PCI Express Root Port Features and Functions

- The S12x0 provides eight PCI Express* lanes that comply with the *PCI Express Base Specification - Revision 2.1*. These eight lanes are contained in one Root Port Unit.

The unit can be configured as one of the following:

- One x8 Root Port.
- Two x4 Root Ports.
- Four x2 Root Ports.
- One x4 Root Port and two x2 Root Ports.

All 8 lanes support PCIe data-rate modes:

2.5 GT/s (PCIe Generation 1).

5.0 GT/s (PCIe Generation 2)

Each Root Port (RP) is internally connected to the S12x0 PCI Root Complex and each is a standard PCI-to-PCIe Bridge device on PCI Bus 0. In other words, each is a Root Complex integrated Root Port (RCiRP). During PCI configuration (Configuration Read, Configuration Write) they respond to Type 0 Configuration Transactions. In that they forward Type 1 Configuration Transactions to its downstream agents, the Root Ports are “transparent” bridges:

- If only one integrated Root Port is configured, it assigned PCI Device number 1, Function number 0.
- If a second integrated Root Port is configured, it is assigned PCI Device 2, Function 0.
- If a third and fourth integrated Root Port are configured, they are assigned PCI Device 3, Function 0 and Device 4, Function 0 respectively.

The S12x0 PCIe Root Ports do not support PCI Express Address Translation Services (ATS) which is a separate PCI document, *Address Translation Services*, Revision 1.1.

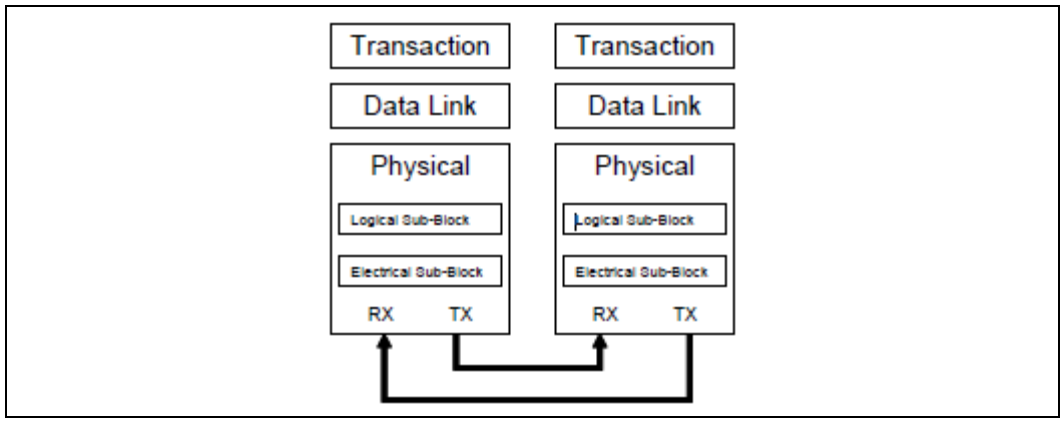
Note: The S12x0 complies with the *PCI Express Base Specification - Revision 2.1* for Root Port PCIe link data transfer speeds. But it also supports the *PCI Express Base Specification,* Revision 3.0 for some of the new capabilities introduced in Revision 3.0 of the specification.

2.2.2 PCI Express Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCIe Plug-and-Play specification.

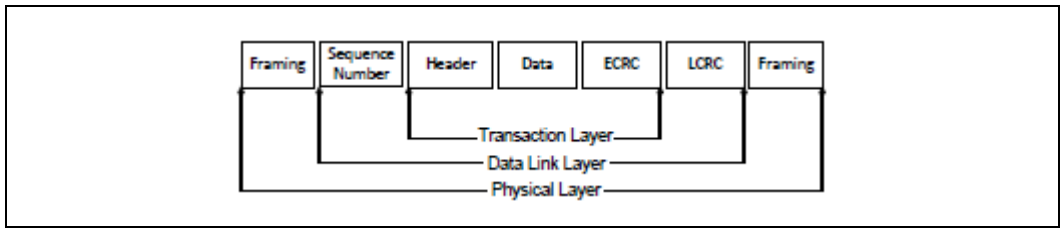
The PCI Express architecture is specified in three layers: Transaction Layer, Data Link Layer, and Physical Layer. The partitioning in the component is not necessarily along these same boundaries. Refer to Figure 2-1 for the PCI Express Layering Diagram.

Figure 2-1. PCI Express Layering Diagram



PCI Express uses packets to communicate information between components. Packets are formed in the Transaction and Data Link Layers to carry the information from the transmitting component to the receiving component. As the transmitted packets flow through the other layers, they are extended with additional information necessary to handle packets at those layers. At the receiving side, the reverse process occurs and packets get transformed from their Physical Layer representation to the Data Link Layer representation and finally (for Transaction Layer Packets) to the form that can be processed by the Transaction Layer of the receiving device.

Figure 2-2. Packet Flow through the Layers



2.2.2.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

2.2.2.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

The transmission side of the Data Link Layer accepts TLPs assembled by the Transaction Layer, calculates and applies data protection code and TLP sequence number, and submits them to Physical Layer for transmission across the Link. The receiving Data Link Layer is responsible for checking the integrity of received TLPs and for submitting them to the Transaction Layer for further processing. On detection of TLP error(s), this layer is responsible for requesting retransmission of TLPs until information is correctly received, or the Link is determined to have failed. The Data Link Layer also generates and consumes packets which are used for Link management functions.

2.2.2.3 Physical Layer

The Physical Layer includes all circuitry for interface operation including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry. It also includes logical functions related to interface initialization and maintenance. The Physical Layer exchanges data with the Data Link Layer in an implementation-specific format and is responsible for converting this to an appropriate serialized format and transmitting it across the PCI Express Link at a frequency and width compatible with the remote device.

2.2.3 PCI Express Configuration Mechanism

The PCI Express link is mapped through a PCI-to-PCI bridge structure.

PCI Express extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the Conventional PCI Specification. PCI Express configuration space is divided into a PCI-compatible region (which consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express region (which consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express configuration access mechanism described in the PCI Express Enhanced Configuration Mechanism section.

The PCI Express Host Bridge is required to translate the memory-mapped PCI Express configuration space accesses from the host processor to PCI Express configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only.

See the PCI Express Base Specification for details of both the PCI-compatible and PCI Express Enhanced configuration mechanisms and transaction rules.

2.3 SMBus

2.3.1 System Management

SMBus is a two-wire bus. Multiple devices, both bus Masters and bus Slaves, may be connected to a SMBus segment. Generally, a bus Master device:

- initiates a bus transfer between it and a single SMBus Slave
- provides the clock signals.

The one exception to this rule is during initial bus setup when a single Master may initiate transactions with multiple Slaves simultaneously. A bus Slave device can receive data provided by the Master or it can provide data to the Master. Only one SMBus device may master the bus at any time. Since more than one device may attempt to take control of the bus as a Master, SMBus provides an arbitration mechanism that relies on the wired-AND connection of all SMBus device interfaces to the SMBus.

When introduced, the *System Management Bus (SMBus) Specification, Version 2.0* introduced an alternative higher-power set of electrical characteristics versus the earlier version 1.0 and 1.1. This higher-drive capability is required when implementing PCI Express throughout the system. It also enabled Plug and Play support. The SMBus remains active even during power management states when the PCIe devices are turned off, allowing communication during sleep states without waking up the PCIe bus.

Its clock frequency range is 10KHz to 100kHz.

2.4 Integrated Legacy I/O Overview

The Low Pin Count (LPC) and other legacy controllers are configured through the PCI-to-ISA Bridge registers. The list of PCI configuration registers is in Table 2-1. These registers are described in detail in Volume 2 of this Datasheet.

This is followed by the HSUART functional description, Section 2.4.1, “High-Speed UART (HSUART)” , which is not part of the bridge.

The remaining sub-chapters describe the functional characteristics of the legacy controllers on the PCI-to-ISA Bridge.

The Low Pin Count (LPC) and other legacy controllers are configured through the PCI-to_ISA Bridge registers. The list of PCI configuration registers is in Table 2-1. These registers are described in detail in Volume 2 of the EDS.

Note: The PCI-to-ISA Bridge refers to functionality internal to the SoC configured through registers.

Table 2-1. PCI Configuration Registers for LPC Bridge - Bus 0, Device 31, Function 0

Start	End	Symbol	Register Name
00	03	ID	Identifiers
04	05	CMD	Command
06	07	STS	Device Status
08	08	RID	Revision ID
09	0B	CC	Class Code
0E	0E	HTYPE	Header Type
2C	2F	SS	Subsystem Identifiers
40	43	SMBA	SM Bus Base Address
44	47	GBA	GPIO Base Address
48	4B	PM1BLK	PM1_BLK Base Address
4C	4F	GPE0BLK	GPE0_BLK Base Address
58	5B	ACTL	ACPI Control
5C	5F	MC	Miscellaneous Control
60	67	PxRC	PIRQx Routing Control where x is [A-H]
68	6B	SCNT	Serial IRQ Control
84	87	WDTBA	Watch Dog timer Base Address
90	93	CMOSDS	CMOS IO Drive Strength control
94	97	CMOSSUSDS	CMOS SUS IO Drive Strength control
98	9B	LPCDS	LPC IO Drive Strength Control
9C	9F	LPCCLK0DS	LPC CLK0 IO Drive Strength Control
A0	A3	LPCCLK1DS	LPC CLK1 IO Drive Strength Control
A4	A7	VISACTRLCR	VISA Control CR
A8	AB	VISALANE0CR	VISA LANE0 CR
AC	AF	VISALANE1CR	VISA LANE1 CR
D0	D3	FS	FWH ID Select
D4	D7	BDE	BIOS Decode Enable
D8	DB	BC	BIOS Control
F0	F3	RCBA	Root Complex Base Address

2.4.1 High-Speed UART (HSUART)

This Chapter is the functional description of the S12x0 High-Speed Universal Asynchronous Receiver/Transmitter (HSUART). It is an integrated, high-speed UART for serial data communication. The HSUART provides one UART controller. Its main features include:

- Characteristics of 16550-compatible UART devices.
- 64-byte First-In First-Out (FIFO) character buffer for the receiver.
- 64-byte FIFO character buffer for the transmitter.
- Programmable interrupt trigger levels for the FIFO buffers.
- Symbols (raw bits) per second (baud rate) based on programmable multiplier and divisor.
- Programmable baud rates from 300 bps to 3.6864Mbps.
- Auto baud-rate detection capability.
- Flow control by hardware or by software.
- Configurable data-frame format:
  - Data bits: 5, 6, 7 or 8 bits.
  - Parity: Even, odd, or no parity generation.
  - Stop bits: 1, 1.5, or 2 stop bits.
- False start-bit detection.
- Line break generation/detection.
- Prioritized interrupt.
- Complete status report capabilities.
- Ability to be disabled by software which also disables the portion of the system clock driving the HSUART controller.

2.4.2 Low Pin Count (LPC) Interface

The S12x0 implements the Low Pin Count (LPC) interface as described in the *Low Pin Count (LPC) Interface Specification, Revision 1.1* (LPC 1.1). The specification describes Memory, I/O and DMA transactions. Unlike the legacy Industry Standard Architecture (ISA) bus, which runs at 8MHz, the LPC interface uses the PCI 33-MHz. Some designs also benefit from the reduced pin count because it uses less space and power and is more thermal-efficient.

2.4.3 Internal CPU Interface Signals

Some of the legacy signals sent internally to the CPU are generated in the legacy block.

2.4.3.1 CPU Interface Signal - INIT#

The S12x0 runtime use of INIT# as a reset is not supported (sometimes called “Soft” reset on past chipsets). CPU Built-In Self Test (BIST) is initiated internally.

To enter CPU BIST, software first sets the CPU BIST Enable (CBE) bit in the Power Management Configuration Suspend/Resume Well (PMSW) I/O register, and then initiates a warm reset by writing the Warm Reset bit of the Reset Control Register (RSTC) described in this chapter.

The PMSW register is located in the variable I/O registers, Base: GPE0BLK Offset: 2Ch.

2.4.3.2 CPU Interface Signal - NMI

Internal Non-Maskable Interrupts (NMIs) can be generated by PCI Express ports and internally from the internal IOCHK# signal from the Low Pin Count interface signal LPC_SERIRQ.

2.4.3.3 CPU Interface Signal - INTR

This internal signal is generated by the 8259 interrupt controllers when 8259s are used for interrupts.

2.4.3.4 CPU Interface Signal - SMI#

This signal is generated by the internal power management controller.

2.4.4 I/O Advanced Programmable Interrupt Controller (IOxAPIC)

The IOAPIC is a 32-bit device with an 8-bit interface. Originally, when first available, an IOAPIC device was attached to a system’s ISA eight-bit bus. In the S12x0, the IOAPIC is part of the Integrated Legacy Block (ILB) of I/O devices. It has some of the same functions of the legacy IOAPIC, but it requires 32-bit data (Double Word) transfers and not 8-bit transfers.

2.4.5 General-Purpose I/O (GPIO)

The S12x0 provides 30 General Purpose I/O (GPIO) registers with signal pins.

Twenty-one of these GPIOs are powered by the Core power well and are turned off during sleep mode (S3 and higher). The other nine GPIOs are powered by the Suspend (SUS) power well (also known as the Resume power well) and remain active during S3. All the GPIOs in the SUS power well can be used to wake the system from the Suspend-to-RAM state, if the OS does not clear the General Purpose Event 0 Enable (GPE0E) register before entering the S3 state.

The GPIO signal pins are not 5-Volt tolerant.

Brief descriptions, electrical parameters, and other platform board information for these GPIO signals are specified in Chapter 7, “Electrical Specifications” on page 107.

The software control and access to the GPIO registers and signals are handled through a 128-byte block of I/O-mapped registers. The starting I/O address of this block is defined by the 32-bit GPIO Base Address (GBA) register located in the legacy-device block’s PCI Configuration Space at Bus 0, Device 31 (decimal), Function 0, offset 048h. Details of the GBA register and the 128-byte I/O block are in Volume 2 of this Datasheet. The registers used in the 128-byte block are also summarized below.

2.4.6 Serial Peripheral Interface (SPI)

The S12x0 Serial Peripheral Interface (SPI) is a four-pin interface that provides a potentially lower-cost alternative for system flash versus the Firmware Hub (FWH) interface that is available through the Low Pin Count (LPC) bus pins.

The S12x0 SPI:

- Provides two SPI-Slave Chip-Select output pins.
- Provides support for SPI Flash components from multiple vendors.
- Provides simple hardware:
  - Equivalent to LPC-based Firmware Hubs.
  - Provides a Write-Protection scheme.
  - Equivalent LPC-based performance (duration of Boot and Resume times).
  - Top Swap functionality.
  - Support for ISA legacy E0000 and F0000 memory segments below 1 MB.
  - 64-Kb granular protection.
  - Maximum SPI Flash memory size addressable by the S12x0 is 16 MB.
  - Data throughput of the SPI bus is 20 Mbps.

Note that the SPI does not provide support for very large BIOS sizes as easily as the FWH interface. The S12x0 SPI interface provides two SPI Chip Select pins.

Additional electrical information is in Chapter 7, “Electrical Specifications” on page 107. Register details are in Volume 2 of this Datasheet.

2.4.7 Real Time Clock

The S12x0 Real Time Clock (RTC) module provides a battery backed date and time keeping device. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 µs to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola MS146818B. The timekeeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second.

The lower 14 bytes on the lower RAM block have very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions. A host-initiated write takes precedence over a hardware update in the event of a collision.

2.4.8 8254 Programmable Interval Timer (PIT)

The S12x0 integrated 8254 Programmable Interval Timer (PIT) contains three counters which have pre-defined, fixed uses. The 8254 PIT and its control registers are in the Core power well and are clocked by a 14.31818MHz clock. The clock source is the HPET_CLK14IN input signal pin.

2.4.8.1 Counter 0, System Timer

Counter 0 functions as the System Timer by controlling the state of an interrupt signal. It is often used to create a system real-time clock.

The Counter 0 control word must be configured so that the Counter 0 OUT signal is a square wave (Mode 3, Square Wave Rate Generator). This signal is connected internally to the S12x0 integrated 8259 Programmed Interrupt Controller (PIC) as IRQ0, the highest-priority hardware interrupt. This signal is also connected internally to IRQ2 of the integrated I/O APIC.

While not shared, this interrupt signal can be blocked from the two interrupt controllers by software. Here the S12x0 High-Precision Event Timer (HPET) Timer 0 output signal is mapped to IRQ0 of the PIC, and to IRQ2 of the I/O APIC.

The Counter 0 produces a square wave that has a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter-period after software writes the count value to the counter I/O address. Counter 0 initially asserts its OUT (interrupt) signal and decrements the count value by two each counter period. The counter negates its OUT signal when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts OUT (the interrupt) when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating its OUT signal.

2.4.8.2 Counter 1, Refresh-Cycle Toggle Status

The control word must be configured so that Counter 1 is a Rate Generator (Mode 2), also known as a “divide-by-N counter.”

The output signal of Counter 1 provides the read-only Refresh-Cycle Toggle Status, available as bit 4 of the NMI Status and Control (NSC) Register. It is used to generate memory refresh request cycles.

Programming Counter 1 to anything other than Mode 2 results in undefined behavior.

2.4.8.3 Counter 2, Speaker Tone

The control word must be configured so that Counter 2 is a Square Wave Rate Generator (Mode 3). The output signal of Counter 2 provides the tone for the internal circuitry that produces the S12x0 audio-speaker output signal, SPKR. The speaker is described in Section 2.4.12, “System Audio Speaker” on page 41.

2.4.8.4 Timer I/O Registers

The registers associated with the 8254 have fixed addresses and are in I/O address space.

Table 2-2. Timer I/O Registers

I/O Port Address	Register Name/Function		Default Value	Type
40h/50h	Counter 0 Interval Time Status Byte Format	ISTST[0]	0XXXXXXXb	Read Only
	Counter 0 Counter Access Port Register	CAP[0]	Undefined	Read/Write
41h/51h	Counter 1 Interval Time Status Byte Format	ISTST[1]	0XXXXXXXb	Read Only
	Counter 1 Counter Access Port Register	CAP[1]	Undefined	Read/Write
42h/52h	Counter 2 Interval Time Status Byte Format	ISTST[2]	0XXXXXXXb	Read Only
	Counter 2 Counter Access Port Register	CAP[w]	Undefined	Read/Write
43h/53h	Timer Control Word Register	TCW	Undefined	Write Only
	Read Back Command	RBC	XXXXXXX0b	Write Only
	Counter Latch Command	CLC	X0h	Write Only

The descriptions and details of these registers are in Chapter 7, “Electrical Specifications” on page 107.

2.4.9 8259 Interrupt Controllers (PIC)

The S12x0 contains two integrated 8259 Programmable Interrupt Controllers (PIC). They are implemented as a Master and Slave 8529 as they are in legacy ISA systems. The following table shows how the Master and Slave are connected.

Table 2-3. Interrupt Controller Core Connections

8259 PIC	8259 Input	Typical Legacy Interrupt Source	Internal Connection / Function
Master	0	Internal Timer	Timer (8254 PIT Counter 0 output) / HPET Timer 0 interrupt.
	1	External Keyboard	IRQ1 via the Low Pin Count (LPC) bus serial interrupt request pin LPC_SERIRQ.
	2	Internal 8259 PIC	Slave 8529 PIC controller INTR output.
	3	External Serial Port A	IRQ3 via LPC bus pin LPC_SERIRQ, inverted PIRQx#.
	4	External Serial Port B	IRQ4 via LPC bus pin LPC_SERIRQ, inverted PIRQx#.
	5	External Parallel Port / Generic	IRQ5 via LPC bus pin LPC_SERIRQ, inverted PIRQx#.
	6	External Floppy Disk	IRQ6 via LPC bus pin LPC_SERIRQ, inverted PIRQx#.
	7	External Parallel Port / Generic	IRQ7 via LPC bus pin LPC_SERIRQ, inverted PIRQx#.
Slave	0	Internal Real Time Clock	Inverted IRQ8# from RTC / HPET Timer 1 interrupt.
	1	Generic	IRQ9 via LPC bus pin LPC_SERIRQ, SCI, or inverted PIRQx#.
	2	Generic	IRQ10 via SERIRQ, SCI, or inverted PIRQx#.
	3	Generic	IRQ11 via SERIRQ, SCI, or inverted PIRQx#, or HPET Timer 2 interrupt.
	4	External PS/2 Mouse	IRQ12 via SERIRQ, or inverted PIRQx#.
	5	Internal	Inverted PIRQx#.
	6	External Primary SATA Device	IRQ14 via LPC bus pin LPC_SERIRQ, inverted PIRQx#.
	7	External Secondary SATA Device	Inverted PIRQx#.

The S12x0 does not provide special IRQ14 or IRQ15 signal pins to support SATA devices. The only external access to these interrupts is to IRQ14 via the Low Pin Count bus serial interrupt pin LPC_SERIRQ.

The 8259 PIC Slave controller is cascaded onto the 8254 PIC Master controller through Master controller interrupt input 2. Interrupts can be individually programmed to function in either edge mode (default) or level mode, except for IRQ0, IRQ2, IRQ8#. These three interrupts only operate in edge mode and cannot be programmed to operate in level mode.

Note: Active-low interrupt sources, IRQ8# of the RTC and the PIRQx# interrupts, are inverted internal to the S12x0 before their connection to the integrated 8259 PIC Master and Slave. In the following descriptions of the integrated 8259 PIC's, the interrupt levels are in reference to the signals at the internal interface of the 8259 PIC's, after the required inversions have occurred. Therefore, the term "high" indicates "active", which means "low" on an originating RTC-IRQ8# or PIRQ# interrupts.

2.4.9.1 I/O Registers

The interrupt controller registers are located in I/O address space at the fixed I/O addresses of 20h and 21h for the master controller (IRQ0 - 7), and at A0h and A1h for the slave controller (IRQ8 - 13). These registers have multiple functions depending upon the data written to them. Below is a description of the different register possibilities for each address.

Table 2-4. Register Table

Port	Aliases	Register Name/Function
20h	24h, 28h, 2Ch, 30h, 34h, 38h, 3Ch	Master 8259 ICW1 Init. Cmd Word 1 Register
		Master 8259 OCW2 Op Ctrl Word 2 Register
		Master 8259 OCW3 Op Ctrl Word 3 Register
21h	25h, 29h, 2Dh, 31h, 35h, 39h, 3Dh	Master 8259 ICW2 Init. Cmd Word 2 Register
		Master 8259 ICW3 Init. Cmd Word 3 Register
		Master 8259 ICW4 Init. Cmd Word 4 Register
		Master 8259 OCW1 Op Ctrl Word 1 Register
A0h	A4h, A8h, ACh, B0h, B4h, B8h, BCh	Slave 8259 ICW1 Init. Cmd Word 1 Register
		Slave 8259 OCW2 Op Ctrl Word 2 Register
		Slave 8259 OCW3 Op Ctrl Word 3 Register
A1h	A5h, A9h, ADh, B1h, B5h, B9h, BDh	Slave 8259 ICW2 Init. Cmd Word 2 Register
		Slave 8259 ICW3 Init. Cmd Word 3 Register
		Slave 8259 ICW4 Init. Cmd Word 4 Register
		Slave 8259 OCW1 Op Ctrl Word 1 Register
4D0h	-	Master 8259 Edge/Level Triggered Register
4D1h	-	Slave 8259 Edge/Level Triggered Register

The register details are in Volume 2 of this Datasheet.

2.4.10 High-Precision Event Timer (HPET)

The S12x0 High-Precision Event Timer (HPET) provides a set of timers that can be used by the operating system for timing various events. One HPET is implemented containing one Counter and three Timers:

- Counter - 64 bits wide
- Timer 0 - 64 bits wide
- Timer 1 - 32 bits wide
- Timer 2 - 32 bits wide

The 14.31838-MHz clock source of the timer is provided by the platform board through the S12x0 input pin HPET_CLK14IN.

2.4.10.1 HPET MMIO Registers

The HPET registers Memory-Mapped I/O (MMIO). They have been assigned fixed addresses in memory address space. The HPET MMIO is a 1-KB block starting at address FED0_0000h. All HPET registers are in the Core power well and are reset by the RESETB input signal pin. Register accesses that cross register boundaries result in undefined behavior. The table below summarizes the registers information and shows the memory-address offset from FED0_0000h.

Table 2-5. HPET MMIO Registers

Start	End	Bits	Symbol	Register Name
000	007	64	GCID	General Capabilities and ID
010	017	64	GC	General Configuration
020	027	64	GIS	General Interrupt Status
0F0	0F7	64	MCV	Main Counter Value
100	107	64	T0C	Timer 0 Configuration and Capability
108	10F	64	T0CV	Timer 0 Comparator Value
120	127	64	T1C	Timer 1 Configuration and Capability
128	12F	64	T1CV	Timer 1 Comparator Value
140	147	64	T2C	Timer 2 Configuration and Capability
148	14F	64	T2CV	Timer 2 Comparator Value

Details of these registers are Volume 2 of this Datasheet.

2.4.11 SMBus 1.0 Controller

The S12x0 provides an SMBus 1.0-compliant host controller. It conforms to the System Management Bus Specification, Version 1.0 (SMBus). This host controller provides a mechanism for the CPU to initiate communications with SMBus peripherals (slaves).

The S12x0 also has two integrated SMBus 2.0 controllers. They are described in. They are configured through PCI Bus 0, Device 19, Function 0 and Function 1:

- Function 0 - SMBus Controller 0 - Hard-Drive management.
- Function 1 - SMBus Controller 1 - System Container management.

The SMBus 1.0 controller described in this chapter is used by the BIOS to implement Serial Presence Detect (SPD) access to the system-memory SDRAM components.

2.4.12 System Audio Speaker

The S12x0 provides registers and circuitry for a system audio speaker. The platform can use the S12x0 signal pin, SPKR, for this purpose. The circuitry for SPKR is located in the S12x0 Core power well.

The internal circuitry uses the following S12x0 components:

- Integrated 8254 Programmable Interval Timer (PIT), Counter 2 output.
  - — provides the square-wave tone signal that can be gated.
- Software-accessible register bits of the NMI Status and Control Register (NSC)
  - — Bit 1: Speaker Data Enable: (default is = 0), When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the 8254 PIT Counter 2 OUT signal value.
  - — Bit 2: Timer Counter 2 Enable: (default is = 0), When cleared, 8254 PIT Counter 2 counting is disabled. When set, counting is enabled.
  - — Bit 5: (read-only) Timer Counter 2 Status: (default is = 0), Reflects the current state of the 8254 PIT Counter 2 output. Counter 2 must be programmed for this bit to have a determinate value.

Details of the S12x0 integrated 8254 PIT Counters are in Section 2.4.8, “8254 Programmable Interval Timer (PIT)” on page 36.

2.4.13 Watchdog Timer (WDT)

The S12x0 supports a user-configurable watchdog timer. It contains selectable prescalar providing a resolution that ranges from 1 microsecond to approximately 16 minutes. The timer uses a 35-bit down-counter. When the WDT triggers, the output signal OWDTOUT pin is asserted.

The WDT counter is loaded with the value from the 1st Preload register. The timer is then enabled and it starts counting down. The time at which the WDT first starts counting down is called the first stage. If the host fails to reload the WDT before the 35-bit down counter reaches zero, the WDT generates an internal interrupt.

After this internal interrupt is generated, the WDT loads the value from the 2nd Preload register into the WDTs 35-bit Down-Counter and starts counting down. The WDT is now in the second stage. If the host still fails to reload the WDT before the second time-out, the WDT drives the output signal OWDTOUT pin high and sets the time-out bit (WDT_TIMEOUT). This bit indicates that the System has become unstable. The output signal OWDTOUT pin is held high until the system is Reset or the WDT times-out again. This depends on the state of the WDT Time-out Configuration bit of the WDT Lock Register (WDTLR). The process of reloading the WDT involves the following sequence of writes:

1. Write “80” to offset WDTBA + 0Ch.
2. Write “86” to offset WDTBA + 0Ch.
3. Write ‘1’ to WDT_RELOAD in Reload Register.

The same process is used for setting the values in the preload registers. The only difference exists in step 3. Instead of writing a ‘1’ to the WDT_RELOAD, write the desired preload value into the corresponding Preload register. This value is not loaded into the 35-bit down counter until the next time the WDT reenters the stage. For example, if Preload Value 2 is changed, it is not loaded into the 35-bit down counter until the next time the WDT enters the second stage.

2.4.13.1 Features

Selectable Prescalar – approximately 1 MHz (1 microsecond to 1 second) and approximately 1 KHz (1 ms to approximately 16 minutes)

- 33-MHz Clock (30-ns clock ticks).
- WDT Mode:
  - — Second stage drives WDT output (WDT_TIMEOUT) high or inverts the previous value. Used only after first time-out occurs.
  - — WDT_TIMEOUT status bit preserved in RTC power well for possible error detection and correction.
  - — Drives output signal OWDTOUT if output is enabled. The enable is register bit 5 of the WDT Configuration Register (WDTCR).
- Timer can be Disabled (default state) or Locked (Hard Reset required to disable WDT).

WDT Automatic Reload of Preload value when WDT Reload Sequence is performed.

3 Technologies

3.1 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems. The multiple, independent operating systems run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

- Intel® Virtualization Technology (Intel® VT) for Intel® 64 and IA-32 Intel® Architecture (Intel® VT-x) adds hardware support in the processor to improve the virtualization performance and robustness. Intel VT-x specifications and functional descriptions are included in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B and is available at http://www.intel.com/products/processor/manuals/index.htm

3.1.1 Intel VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- Robust: VMMs no longer need to use para-virtualization or binary translation. This means that they are able to run off-the-shelf OS's and applications without any special steps.
- Enhanced: Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- More reliable: Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- More secure: The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

3.1.2 Intel VT-x Features

The processor core supports the following Intel VT-x features:

- Extended Page Tables (EPT)
  - hardware assisted page table virtualization maintenance
- Virtual Processor IDs (VPID)
  - Ability to assign a VM ID to tag processor core hardware structures (for example, TLBs)
  - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
  - Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
  - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees
- Descriptor-Table Exiting
  - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
  - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.
- Pause Loop Exiting (PLE)
  - PLE aims to improve virtualization performance and enhance the scaling of virtual machines with multiple virtual processors
  - PLE attempts to detect lock-holder preemption in a VM and helps the VMM to make better scheduling decisions

3.2 Security Technologies

3.2.1 Execute Disable Bit

Intel's Execute Disable Bit functionality can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system.

- Allows the processor to classify areas in memory by where application code can execute and where it cannot.
- When a malicious worm attempts to insert code in the buffer, the processor disables code execution, preventing damage and worm propagation.

3.3 Intel® Hyper-Threading Technology

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology), which allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled via the BIOS and requires operating system support. For more information on Intel Hyper-Threading Technology, see http://www.intel.com/products/ht/hyperthreading_more.htm.

3.4 Enhanced Intel SpeedStep® Technology

The processor supports Enhanced Intel SpeedStep® Technology as an advanced means of enabling very high performance while also meeting the power-conservation needs of the platform.

Enhanced Intel SpeedStep Technology builds upon that architecture using design strategies that include the following:

- Separation between Voltage and Frequency Changes. By stepping voltage up and down in small increments separately from frequency changes, the processor is able to reduce periods of system unavailability (which occur during frequency change). Thus, the system is able to transition between voltage and frequency states more often, providing improved power/performance balance.
- Clock Partitioning and Recovery. The bus clock continues running during state transition, even when the core clock and Phase-Locked Loop are stopped, which allows logic to remain active. The core clock is also able to restart more quickly under Enhanced Intel SpeedStep® Technology.

§ §

4 Power Management

4.1 Overview

Power Management events internal to the Intel® Atom™ Processor S1200 Product Family for MicroserverIntel® Atom™ Processor S1200 Product Family for Storage (S12x0 are controlled by the internal Power Management Unit (PMU). The PMU function is distributed on the component. It is main parts are called the P-Unit (an internal, dedicated microcontroller that runs custom firmware) and a power management block that is part of the Intel Legacy Block that contains the Low Pin Count (LPC) interface and other integrated legacy devices. This chapter simply refers to this distributed function as the PMU.

An external, board-level System Management Controller (SMC), or some other external circuitry, is required to manage the platform power planes, power on, sleep states and reset signaling. This chapter simply refers to the SMC or external circuitry as External Circuitry (EC). The EC interfaces with the PMU of the S12x0 to perform its management functions.

The PMU is responsible for the following tasks:

- Manage the voltages of the internal power wells
- Communication with the External Circuitry (EC)
- Reset request sequences
- Managing S12x0 C-states
- Sleep State entry sequences
- DDR3 power management and RComp Routines
- Low Pin Count (LPC) interface clock control.
- Thermal Management of the S12x0
- Interface with BIOS and the Operating System Software.

4.1.1 Acronyms

Table 4-1. Power Management Acronyms

Acronym	Description
ACPI	Advanced Configuration and Power Interface
PMU	Power Management Unit - Device internal to the S12x0 that handles power management events.
PMC	Power Management Microcode
EC	External Circuitry - The System Management Controller, or other board-level controller, that handles power management events.
CPU	Central Processing Unit - Refers to the processing core.
DLL	Delay-Locked Loop
OSPM	Operating System Power Management
RTC	Real Time Clock unit
DDR3	Double Data Rate, Third Specification - Refers a JEDEC memory architecture.
MSI	Message Signaled Interrupt.
SCI	System Control Interrupt. An OS-visible system interrupt used by hardware to notify the OS of ACPI events.
SMI	System Management Interrupt. An OS-transparent interrupt generated by interrupt events on legacy systems. By contrast, on ACPI systems, interrupt events generate an OS-visible interrupt that is shareable (edge-style interrupts will not work). The S12x0 supports both legacy operating systems and ACPI systems. It has a mechanism to re-map the interrupt events between SMIs and SCIs when switching between ACPI and legacy models.

4.1.2 Power Management Features

Below are S12x0 power management features:

- ACPI Platform Sleep State support: S0, S3, S4, S5
- ACPI Processor (CPU) C States: C0, C1, C2, C4, C6
- ACPI Device States: D0, D3
- PCI Express*: L0, L1, L2, L3
- Enhanced Geyserville (eGVL) CPU local bus
- Enhanced Intel SpeedStep® Technology
- Hardware throttling
- Clock Gating
- Thermal throttling
- Dynamic I/O power reductions (disabling sense amps on input buffers, tri-stating output buffers)
- Reprogrammable Power Management Unit (PMU)
- Reprogrammable thermal management algorithms performed by PMU
- DDR3 SDRAM memory controller and PHY:
  - — Dynamic Rank Power Down
  - — Dynamic power down is employed during normal operation. If all the pages have all been closed at the time of CKE pin de-assertion, the SDRAM devices will enter the precharge power-down state. Otherwise the devices enter the active power-down state.
  - — Conditional Memory Self-Refresh
  - — DLL master/slave shutdown based on CPU state.
  - — Address and command signal tri-state when all memory is in powerdown or self-refresh, or when not in use (no chip select asserted)
  - — Chip-select tri-state for a powered-down row
  - — Clock tri-stating for unpopulated DIMMs
  - — CKE/CS tri-stating for unpopulated rows
  - — Conditional Memory Self-Refresh during C2-C4-C6
  - — Conditional and software directed Memory Self-Refresh
    Supports conditional self-refresh entry in the C2-C6 states, based on memory request traffic from host interface agents.
- Debug and Testability hooks.

4.2 Communication with the External Circuitry

The External Circuitry (EC) on the platform board controls the voltages of the system power rails. The S12x0 Power Management Unit (PMU) communicates with the EC through the signal pins briefly described in Table 4-2.

Table 4-2. Power Management Signal Pins (Sheet 1 of 2)

Pin Name	Direction	Power Well	Description
Reset and Power Sequencing			
RESETB	I	SUS	**Processor Reset#**: When asserted, the S12x0 is put in reset until RESETB is de-asserted. When de-asserted, it releases core reset.
PWROK	I	RTC	**Power OK**: When asserted, PWROK is an indication that all platform power rails have been stable. PWROK can be driven asynchronously. ***Note:*** It is required that the power associated with PCI and PCI Express* have been valid for 99ms prior to PWROK assertion in order to comply with the 100ms PCI and PCI Express specifications concerning deassertion of RESETB.
RSMRSTB	I	RTC	**Resume Well Reset**: This signal, when asserted as '0', is used for resetting the SUS power well. An external RC circuit is required to ensure that the SUS well power is valid prior to RSMRSTB going high.
RTCRESETB	I	RTC	**RTC Well Reset**: Normally held high (to VCCRTC), but can be driven low on the tester or board to test RTC power-well circuitry. Can also be driven with an RC circuit so that the S12x0 can detect that a new battery has been installed.
SUSCLK	O	SUS	Essentially same as the Real Time Clock RTCCLK signal. Output of the RTC generator circuit (32.768 kHz).
SLPMODE	O	SUS	Indicates the type of sleep that needs to be entered when qualified with the SLPRDYB signal. (1=S3, 0=S4/5)
SLPRDYB	O	SUS	When asserted low, this indicates that system is ready to enter the sleep state indicated by SLPMODE signal. Deassertion of this signal indicates that a wake is being requested from a system device.
RSTWARN	I	SUS	Indicates that a reset is needed, and will be issued once the S12x0 responds with a RSTRDYB assertion. Asserting the RSTWARN signal tells the S12x0 to enter a sleep state or begin to power down. The External Circuitry (EC) might do so after an external event, such as pressing of the Power Button or occurrence of a Thermal Event.
RSTRDYB	O	SUS	Indicates that the S12x0 has finished clean-up and ready for RESETB assertion
WAKE_B	I	SUS	**PCI-Express Wake Event**: Indicates a PCI-Express port wants to wake the system. PCIe device sending to SOC to request power and clock.
PUNIT_ST_ADDR[1:0]	I		**P-Unit Start Address:** A strap used to define the starting address of the internal Power Management Unit (PMU) firmware stored in the SPI Flash memory. 00: 0xFFFB_0000 01: 0xFFFC_0000 10: 0xFFFE_0000 11: 0xFFFD_0000

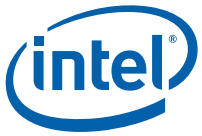


Table 4-2. Power Management Signal Pins (Sheet 2 of 2)

Pin Name	Direction	Power Well	Description
Thermal Management			
CPU_PROCHOTB	I/O		This signal is bi-directional. It either indicates that the S12x0 has reached its maximum operating temperature or can be driven from an external source to activate the TCC. The ability to activate the TCC via CPU_PROCHOTB can provide a means for thermal protection of system components.
THRMTRIPB	O		The S12x0 protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor stops all execution when the junction temperature exceeds approximately 125 °C. This condition is signaled to the system by the THERMTRIPB (Thermal Trip) pin.
THRMB	I	SUS	**Thermal Alarm:** Generated by external hardware to generate SMI#/SCI. The receiver is located in the SUS power well.
Error Status			
ERR[2:0]	O		Three open-drain signals for the purpose of error reporting error classes. ERR[0]- Correctable Error: A Correctable Error is reported to the CPU as an SMI (default) or NMI. ERR[1]- Non-Fatal Error: A Non-Fatal Error is reported to the CPU as an NMI (default) or SMI. ERR[2]- Fatal Error: A Fatal Error is reported to the CPU as an NMI (default) or SMI.

4.3 Power Planes and Voltage Rails

The S12x0 internal circuits have several required voltages that must be supplied from the system platform board. Each supplied voltage serves one or more de-coupled Voltage Rails within the die. The voltage rails provide the power to the die circuit power wells. Additionally, these internal Voltage Rails are grouped by when they must be switched on or off by the External Circuitry (EC) voltage controller for the various ACPI-defined Global States (G-States) and System States (S-States).

There are three such groups. They are defined in the following sections.

4.3.1 Power Group Definitions

This External Design Specification is not consistent when identifying the power/voltage groups. The various terms used are explained below.

4.3.1.1 Core Power Well

The terms used are as follows and refer to the same power group:

- Core Power Well
- VCC_S0 Group (Core)
- S0 Voltage Rail Group
- Core power
- Vcc_Core (in some waveform figures)

This power group includes all internal voltage rails and associated power wells that are on when the system is in the System Sleep S0 State (system is fully powered-on). These voltage rails are turned off when the system transitions to the one of the other System Sleep States which are the low-power sleep states.

There are 20 General-Purpose I/O (GPIO) registers in the Core power well. This includes the GPIO[0] which is used to provide signal pin BOOTDEVSEL.

Included in this voltage group are:

- VCC - The core processor voltage.
- VNN - The S12x0 main internal voltage.

4.3.1.2 SUS Power Well

The terms used are as follows and refer to the same power group:

- SUS Power Well
- Suspend Power Well
- Resume Power Well
- Suspend/Resume Power Well
- VCC_S3 Group (Suspend/Resume)
- S3 Voltage Rail Group
- Vcc_RSM (in some waveform figures)

This power group includes internal voltage rails and associated power wells that are on when the system is in the S0 and S3 states. These voltage rails are turned off when the system sleep state transitions from the S3 sleep state to the S5 sleep states.

There are nine General-Purpose I/O (GPIO) registers in the SUS power well. The power management signal pins THRMB, SLPRDYB, SLPMODE, RSTRDYB, SUSCLK, RSTWARN, WAKE_B, and RESETB have their drivers/receivers in the SUS power well.

Additionally, the DDR3 SDRAM I/Os provided by the integrated memory controller are powered from VCCSUS1P5 which is part of the SUS power group. This is required to keep DDR3 SDRAM components in Self-Refresh mode while in S3, to preserve its contents.

4.3.1.3 RTC Power Well

The terms used are as follows and refer to the same power group:

- RTC Power Well
- Real-Time Clock power well
- VCC_S5 Group (RTC)
- S5 Voltage Rail Group
- RTC power

This power group includes all internal voltage rails and associated power wells that are on when the system is in the System Sleep S5 State. This group is supplied its 3.3V from the SUS power supply or from an external battery source, typically a 3.3V, lithium-type coin cell.

If there is a complete power failure (no AC power and no battery back-up supply) this voltage rail does not provide any power if there is no functioning coin-cell battery providing its power.

Registers located in this power well are indicated by “RTC Power Well” in the register description.

The RTC_X1PAD and RTC_X2PAD for the external crystal and internal RTC oscillator are in the RTC power well. Also in this power well are some RTC logic circuits and a small portion of the Power Management Unit (PMU).

If the platform design does not need the RTC power well, the well can be tied to the SUS power well voltage supply as long as the Reset Sequence function is maintained.

4.3.2 Power Plane vs. Supported System Sleep States

Table 4-3. Power Planes and Supported System Sleep States

Power Group	Platform Power Rail	Default (Volts)	Range (Volts)	S0 (C6)	S3	S5	Description
Core	SVID	1.05	0.75 - 1.10	On	Off	Off	CPU Core. On-die power-gated during C0 (S6)
	V1P05 (VNN)	1.05	-	On	Off	Off	• Uncore circuits • Internal VNN common rail • Core GPIO • DDR3/PCIe digital • Internal fuses • Visa circuits
	V1P5	1.5	-	On	Off	Off	• PCI Express analog • PLLs • CPU Thermal Sensor • SoC Thermal Sensor
	V1P8	1.8	-	On	Off	Off	• High Voltage GPIO biasing • Medium Voltage GPIO biasing • SMBus • CPU-SoC Thermal Sensor
	V3P3	3.3	-	On	Off	Off	• Core GPIO 3.3V • SMBus
SUS	V1P05_S	1.05	-	On	On	Off	SUS GPIO
	V1P5_S	1.5	-	On	On	Off	DDR3 PHY
	V1P8_S	1.8	-	On	On	Off	SUS GPIO biasing
	V3P3_S	3.3	-	On	On	Off	• RTC-SUS Power Well • SUS GPIO 3.3V
RTC	V3P3_RTC	3.3	-	On	On	On	RTC Power Well

4.3.3 Voltage Sequencing Requirements

The platform External Circuitry (EC) is responsible for sequencing the various voltages for the S12x0. The following requirements must be met.

- RTC power group comes up first.
- SUS power group comes up next, in the following order: 3.3V, 1.8V, 1.5V, and 1.05V.
- Core power group comes up last. Sequencing requirements here are: 3.3V, 1.8V, 1.5V, 1.05V (VNN) and VCC.

The sequence of turning off the voltages will be in the reverse order, based on the power states. In some power states, some voltage rails are on ON and some rails are OFF. Based on platform requirements and optimization, the different power planes can be tied together to optimize platform Voltage Regulators.

4.3.4 Voltage Rail Ramp Rate

There is a balance that must be achieved on voltage rail ramp rates:

- Faster: For rails that are turning on from S3/5, faster ramp rates decrease transition time. This makes these lower power states more efficient and decreases interrupt response latency.
- Slower: the faster the ramp rate, the more the sudden voltage jump acts like Electrostatic Discharge (ESD). ESD circuits are used on the S12x0 to protect rest of the die. The ESD clamps for ESD protection on the S12x0 internal voltage planes can only protect voltage-rail ramping rates slower than 100mV/us during power-up. Protection is not provided for faster voltage-rail ramp rates.

4.3.5 SerialVID (SVID) Overview

In operation, the S12x0 CPU core voltage is variable, and changing dynamically, if variable-voltage regulators are used on the platform. To do this, the S12x0 provides the 3-pin SerialVID interface which conforms to controllers complying with IMVP7. Refer to the Intel *VR12/IMVP7 Pulse Width Modulation (PWM) Specification* and the Intel *VR12/IMVP7 SVID ProtocolVR12/IMVP7 SVID Protocol* documents for details.

Serial Voltage Identification (SerialVID) is a three-wire (clock, data, alert) serial synchronous interface used to transfer power management information between a master (the S12x0 in this case) and a slave (typically a voltage-regulator controller).

One SerialVID interface can bus-link multiple slave devices, usually, multiple voltage-regulator (VR) controllers, to the S12x0. The clock is source-synchronous provided by the S12x0 and there is a four-bit addressing scheme for selecting the slave devices. The following are the SerialVID interface pins provided by the S12x0:

- SVID_ALERT_B - Active-low input signal pin, low-voltage receiver.
  Synchronous to the clock, this signal notifies the S12x0 that critical VR status has changed. Referred to as Alert# in the specification.
- SVID_DATA - Input/Output signal pin, low-voltage receiver and open-drain driver.
  Synchronous to the clock, used by the S12x0 and slave to send information to each other. Referred to as VDIO in the specification.
- SVID_CLK - Output signal pin, low-voltage open-drain driver.
  The S12x0 may shut-down the clock signal to save power when no data transfer is needed. Referred to as VCLK in the specification.

To adjust the voltage output of the VR providing the CPU core voltage, the S12x0 issues SerialVID commands to the controller. It provides the controller a target Voltage Identification (VID) to meet, and the VR steps the voltage change in order to achieve the target voltage value.

Table 4-4. Dynamic VID Slew Rate

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Dynamic VID Slew Rate	SR_{DVID}	SetVID Slow	2.5	3.125	3.75	mV/µsec
		SetVID Fast	10	12.5	15	mV/µsec

4.4 ACPI State Descriptions

Table 4-5 below shows the ACPI power states defined for the S12x0 platforms.

Table 4-5. General Power States

State/Substates	Supported	Legacy Name / Description
G0/S0/C0	Yes	**Full On**: CPU operating. Individual devices may be shut to save power. The different CPU operating levels are defined by Cx states.
GO/S0/Cx	Yes	**Cx State:** C0/C1/C2/C4/C6. When C3/C5 is requested from the operating system, it's internally mapped to C4 by the CPU.
G1/S1	Not Supported	
G1/S3	Yes	**Suspend-To-RAM (STR)**: The system context is maintained in system DRAM, but power is shut to non-critical circuits. Memory is retained, and refreshes continue. All external clocks shut off, but the RTC clock and internal ring oscillator clocks are still toggling.
G1/S4	Yes	**Suspend-To-Disk (STD)**: The context of the system is maintained on the disk. All power is then shut to the system except for the logic required to resume. S12x0 hardware treats S4 and S5 requests exactly the same way.
G2/S5	Yes	**Soft OFF**: System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.
G3	Yes	**Mechanical OFF:** System context is not maintained. All power shut off except for the RTC. No "Wake" events are possible, because the system does not have any power. This state occurs if the user removes the coin cell batteries or turns off a mechanical switch.

Note: The above table is for informational purposes only.

Note: Table 4-6 below shows transitions rules among the various states. Note that transitions among the various states may appear to temporarily transition through intermediate states. These intermediate transitions and states are not listed in the table.

Table 4-6. ACPI Power Management State Transitions

Present State	Transition Trigger	Next State
G0/S0/C0	IA Code MWAIT or LVL Rd	G0/S0/Cx
	SLP_EN bit set	S3/S4/S5 state (specified by SLP_TYP)
	Mechanical Off	G3
G0/S0/Cx	Cx break events which include: CPU snoop, MSI, Legacy Interrupt	G0/S0/C0
G1/G3	RTC Alarm (Set RTC_EN bit in PM1_EN Register)	G0/S0/C0
	WAKE_B (pin from PCI Express* ports)	Not supported.
	SMBus ALERT# signal.	Not supported.
G2/S5	Any Enabled Wake Event	G0/S0/C0
	Power Failure	G3
	Power Button Override	G0/S0/C0
G3	Power Returns	Option to go to S0/C0 (reboot) or G2/S5 (stay off until power button pressed or other enabled wake event). Some wake events are preserved through a power failure.
	Coin-Cell Battery plugged-in	G2/S5

Note: **Snooping** is a technique used in distributed shared memory systems and multiprocessors to achieve cache coherency. Although there is one main memory, there are several caches (one per processor), and unless preventative steps are taken, the same memory location may be loaded into two caches, and given two different values. To prevent this, every cache controller monitors the bus, listening for broadcasts which may cause it to invalidate its cache line.

4.5 Performance States (P-States) and Throttling

When the S12x0 is in the fully-powered and operational state (S0 State), the Operating System (OS) software can enable various performance and throttling-based power-saving measures.

4.5.1 Enhanced Intel SpeedStep® Technology

The S12x0 supports the Enhanced Intel SpeedStep® Technology, which allows the operating system to reduce power consumption when performance is not needed.

Enhanced Intel SpeedStep® Technology centralizes the control mechanism in the S12xx, eliminating the need for any coordination during the frequency/voltage transition.

- Since voltage switching constitutes the bulk of the transition time, Enhanced Intel SpeedStep® Technology voltage transitions are performed while the S12x0 is executing instructions and servicing bus master transactions. Instruction execution is halted only for the short duration of the frequency change.
- Since a higher voltage is required to operate the S12x0 at a higher frequency, the order in which voltage and frequency transitions occur depends on the type of transition.
  - — When transitioning from a lower to higher performance state, the voltage transition must occur first. Once the voltage has stabilized at the required level, the frequency transition occurs.
  - — When transitioning from a higher to lower performance state, the frequency transition occurs first, and the voltage transition follows.
- For low to high transitions, however, this means that there may be a substantial latency before the final performance state is reached, although instructions are still executed for the majority of the total transition time period.
- The move of all the controls to the S12x0 significantly reduces the hardware and software overhead for transitions to the order of ~5-10µs effectively allowing for a much higher frequency of transitions.
- Furthermore, the controls for initiating the transitions are moved to Model Specific Registers (MSRs), effectively completing the transition of controls into the S12x0.

The Enhanced Intel SpeedStep® Technology offers the capability to support a multitude of S12x0 performance states, also known as P-states.

4.5.2 Dynamic Power Management on I/O

The S12x0 provides several features to reduce I/O power dynamically.

- PCI Express Interface
  - — Active power management support using L0, L1 states.
  - — All inputs and outputs disabled in L2/L3 Ready state.
  - — Reduced transmitter current on PCI Express ports.
- LPC
  - — LPC_CLKOUT[2:0] are not driven externally when using SERIRQ mode.

4.5.2.1 LPC Clock Control

When there are no pending Low Pin Count (LPC) cycles, and Serial Interrupt signal pin (LPC_SERIRQ) is in quiet mode, the internal Power Management Unit (PMU) shuts-down the LPC clock output signal (LPC_CLKOUT[1:0]). LPC devices on the bus that need to request that the LPC clock continue running, and sense the LPC_CLKRUN_B in the high state, can drive LPC_CLKRUN_B low within 4 clocks periods. If no device drives LPC_CLKRUN_B low once it has been high for 4 clock periods, the PMU stops the LPC clock. If an LPC peripheral asserts LPC_CLKRUN_B (low), the PMU drives the LPC clock, and starts driving the LPC_CLKRUN_B signal.

4.6 Processor Core States (C-State)

The S12x0 provides support for C1, C2, C4, and C6. As added features, the S12x0 also supports three extended C-States and the ability to enable C4 in the presence of high bandwidth bus-mastering devices using C2 popup feature.

The Operating System Power Management (OSPM) has primary control for dynamically changing S12x0 C-states, while the internal Power Management Unit (PMU) brings the package to the requested C state. The C-states are described in the table below.

Table 4-7. Processor C States

Global State	Sleep State	CPU C State	CPU Caches	CPU Clocks	DDR3 SDRAM	Description
G0	S0	C0	In use	ON	On	Full On. Operating System selectable P-States (perf/pwr operating points).
G0	S0	C1	Valid. Snoopable	ON	On	Auto-Halt.
G0	S0	C2	Valid. Snoopable	GCLK off	Conditional self-refresh	Stop Grant or Quick Start.
G0	S0	C3	-	-	-	C3 State is not supported. All C3 requests are mapped to C4.
G0	S0	C4	Valid. C2pop to Snoop	CPLL off	Conditional self-refresh	Deeper Sleep, CPU caches valid and must be snooped (C2-popup), CPU Voltage lowered.
G0	S0	C5	-	-	-	C5 State is not supported. All C5 requests are mapped to C4.
G0	S0	C6	Flushed. No snoops	CPLL off	Conditional self-refresh	VCC below retention (state saved in SRAM)
G1	S3	Pwr off	Off	Pwr Off	Self-refresh	Care powered off. Suspend to RAM
G1	S4	Pwr off	Off	Pwr Off	Pwr Off	System Clocks off except RTC, Suspend to disk.
G2	S5	Pwr off	Off	Pwr Off	Pwr Off	System Clocks off except RTC, Soft Off.
G3	NA	Pwr Off	Off	Pwr Off	Pwr Off	System Clocks Off, Hard Off.

4.6.1 C-State Variations

The S12x0 processing core is divided into three distinct blocks:

- two logical processors
- a shared area

The S12x0 processing core can support C-States at the logical processor level and package level. The two logical processors can enter a low-power C-State independently. One logical processor can enter Thread-C1 (TC1), Thread-C2 (TC2), Thread-C4 (TC4), or Thread-C6 (TC6) while the other logical processor executes code in C0. Since both execution logical processors share the same voltage plane, the package C4 voltage transitions only occur when both logical processors enter C4. This logic applies to C6 state as well. While any logical processor can enter the TC6 state, the package will enter the C6 only when both the logical processors are in TC6 and the L2 cache has been fully flushed.

When both logical processors enter a C-State, the package can enter a given C-State. The shared area will always reside in the higher power C-State of the two logical processors (for example if logical processor 0 is in TC4 and logical processor 1 is in TC2, the shared area and package will reside in C2).

When the package is in C4, both L1 and L2 are still valid and snoops must be serviced. When L2 size is reduced to zero, L1 cache is also invalidated and snoops are directed to the memory.

The C-state coordination support expands up to four logical processors with the dual-core S12x0. Each core manages two logical processors as described above. An additional level of coordination is added using a Power Management Link to dynamically update power state status and requests between the two cores to enable hardware-based coordination of the operating point changes among CPUs.

4.6.2 C-State Definition

This section provides the overview of various C states supported by the S12x0. It also covers the characteristic of the Power Management Unit (PMU) at these C states.

4.6.2.1 C0 State – Full On

The characteristics of C0 state are:

- This is the only state that runs software.
- All clocks are running
- STPCLK is de-asserted and the processor core is active.
- The S12x0 services snoops and maintains cache coherency in this state.
- All power management for interfaces, clock gating, etc., controlled at the unit level.

4.6.2.2 C1 State – Auto-Halt

The characteristics of C1 state are:

- The first level of power reduction occurs when the S12x0 executes an Auto-Halt instruction. This stops the execution of the instruction stream and greatly reduces the S12x0 power consumption.
- The S12x0 can service snoops and maintain cache coherency in this state.
- The PMU does not distinguish C1 from C0 explicitly.

4.6.2.3 C2 State – Stop Grant

The next level of power reduction occurs when the S12x0 is placed into the Stop Grant state by the assertion of STPCLK. The characteristics of C2 state are:

- The S12x0 can service snoops and maintain cache coherency in this state.
- The PMU only supports receiving a single Stop Grant.
- Entry into the C2 state occurs after the S12x0 performs a Level 2 read. The C2 state will be exited, entering the C0 state, when break event is detected. The S12x0 must ensure the DLLs are awake and the memory will be out of self-refresh at this point.
- Master & Slave portions of the DLLs may be disabled when no read access is pending, the internal graphics controller is completely idle, and the display requirements are within a predefined limit (no graphics).
- Memory is put into conditional self-refresh mode when no further access is pending.
- Entry into the package C2 state will occur after the CPU (or, in a Intel® Hyper-Threading Technology-enabled system, both threads) requests C2 (or deeper). Upon STPCLK assertion, the CPU is not guaranteed to recognize transitions or take the proper behavior on special control and interrupt pins. Therefore, the PMU will freeze the state of these pins while STPCLK is asserted, and not change the values until the CPU has returned to C0.

C2 is entered when the CPU reads the LVL2 register, and from C4 if bus masters require snoops.

4.6.2.4 C4 State – Deeper Sleep

In this state, the core processor shuts down its PLL and cannot handle snoop requests. The core processor voltage regulator is also told to reduce the processor voltage. During the C4 state, the S12x0 will continue to handle traffic to memory so long as this traffic does not require a snoop (i.e., no coherent traffic requests are serviced).

The C4 state is entered by receiving a C4 request from the core processor/OS. The exit from C4 occurs when the S12x0 detects a snoopable event or a break event, which would cause it to wake up the core processor and initiate the C0 sequence.

C4 is entered when the CPU reads the LVL4 register, and after a return to C2 from a prior C4 state.

4.6.2.4.1 Cache Shrink and LVL5 Read

The processor can be triggered to issue a LVL5 read, when the L2 cache is shrunk to zero size upon successive C4 entries. Since the L2 cache is shut down, snoops are not required to be serviced by the processor and this is indicated to the North Complex by the LVL5 read. The snoops are replied as misses by the chipset such that they are directed to the memory and not to the cache.

The BIOS must follow a specific sequence of steps to enable this feature. Intel recommends the BIOS enable this feature before enabling any Power Management feature (C-States in particular) such that the L2 Cache is at a known state and is not shrunken.

Expansion to the full size will happen as execution continues based on increase in load (up-shift in performance state) or a continuous residency in C0 over a predefined time period. Exit from C4 can happen due to reasons like either thread requesting C-States other than C4, or either thread requesting a different P State than the lowest operating point.

4.6.2.5 C6 - Deep Power Down Technology

Prior to entering the C6 state, the core processor will flush its cache and save its core context to a dedicated on-die SRAM on a different power plane. Once the C6 entry sequence has completed, the core processor voltage can be completely shut off.

The key difference between the C4 state and the C6 state is that since the core processor cache is empty, there is no need to perform snoops on the host bus. This means that bus master events (which would cause popup from the C4 state to the C2 state) can be allowed to flow unimpeded during the C6 state. However, the CPU must still be returned to C0 in order to service interrupts (pin or MSI).

Note: A residency counter, C6C, in the PMU is read by the CPU to enable an intelligent promotion/demotion based on energy awareness of transitions and history of residencies/transitions.

C6 can be entered by means of MWAIT (C6) or I/O Level 6 read. The I/O Level 6 read mechanism is needed to support the processor under OSPM. Note that C4E, Hard C4E, and GV3 should all be enabled for C6 to function correctly.

4.6.2.5.1 Thread C6 (TC6) State

The two threads of a processor core will enter TC6 state independent of each other. Each thread will save its state into a dedicated on-die SRAM. The last thread to enter TC6 will shrink the L2 cache.

4.6.2.5.2 Package C6 State

When both processor-core threads enter TC6, the L2 cache can have non-zero ways. Until the cache is shrunk to zero ways, the package will enter only C4 state. The L2 shrink to zero can take multiple TC6/C4 entries. Only after all the ways are shrunk to 0, the package will enter C6.

It should be noted that the C6 entry will always do an entry to LFM frequency and will also start a transition to the LFM VID before entering package C6. At exit from C6, the processor will lock at LFM VID and frequency. When the microcode restore of the P state control register is done, the transition to the original operating point will start. The entry to LFM when exiting C6 will be enforced even if Hard C4E is enabled.

Both S12x0 cores enter and exit the C6 power state in unison. There is no support for one of two cores entering the C6 power state independently.

4.6.2.6 C6 Demotion Policy

Deeper C-States such as C6 have a high energy cost for the transitions. This cost becomes more significant as the frequency of C-State entry/exit increases.

Incorrect usage of Deeper C-States will result in additional power consumption rather than reduction. The processor implements a hardware based C6 Demotion policy. This C-State policy depends on a C-State residency timer.

The existence of such timers on the platform will be indicated by the BIOS to the CPU by setting bit 25 in the PMG_CST_CONFIG_CONTROL MSR. Refer to the *Intel® Atom™ Processor S1200 Product Family for Microserver BIOS Writer's Guide*.

4.6.3 Extended Low Power States

When idle, there should be no demand for processor performance (otherwise, the processor would not be idle). Extended C-States optimize for power by forcibly reducing the performance state of the thread when it is idle and enters a C-State. Instead of directly transitioning into the C-State, the enhanced version of the C-States first reduce the performance state of the processor by performing an Enhanced Intel SpeedStep® Technology transition to the lowest operating point before entering a C-State. Upon receiving a break event from the C-State, control will be returned to software while an Enhanced Intel SpeedStep® Technology upwards transition to the initial operating point occurs.

The advantage of this feature is that it significantly reduces leakage while in C1 and C2 and reduces the exit latency from C4 and C6.

Extended C-State entry may occur by means of multiple methods. Software can forcibly cause the processor to enter an extended C-State by means of an MWAIT hint (see *RS - Intel® Atom™ Processor S1200 Family BIOS Writer's Guide*). The other method is IA-32 firmware based. IA-32 firmware may also override C4 with C4E during POST which will cause any C4 requests to trigger a C4E sequence.

Extended C-States are expected to be highly transparent to software however, software should be aware that immediately after breaking out of a C-State, the performance state of the processor may be briefly reduced as it returns to the original operating point. This temporary reduction in performance is visible by means of the IA32_PERF_STS register, which will return an Enhanced Intel SpeedStep® Technology operating point different than the last requested one from the operating system. It should also be noted that in an Intel® Hyper-Threading Technology processor, all logical processors in the processor physical package must be idle before the C-State transition may occur.

The S12x0 currently supports C1E, C2E and C4E.

Note: Direct reads (without enabling the I/O MWAIT Redirection) to the LV2 and LV4 registers in the chipset will not result in the processor entering extended C-States. The processor will only automatically enter extended C-States when I/O MWAIT redirection is enabled and the appropriate bits in IA32_DEBUGCTL (bit[26] for C2E, bit[32] for C4E, are set or a MWAIT with the appropriate MWAIT Hint is executed. However, C4E is an exception if iDPRSTP_B is enabled and Hard C4E is enabled (bit[33] in the IA32_DEBUGCTL MSR).

Note: Direct read to the LVL6 register should also be avoided for the proper working of the C6 state.

4.6.4 C2 Popup/Popdown

While in C4, processor caches are not snoopable since processor clocks that power snoop logic are not active. As a result, bus mastering devices that require short latency snoop responses often cause C4 to be disabled in systems.

The core processor and supporting chipsets may support a feature called C2 popup/popdown that will allow the processor to reside in an unsnoopable state such as C4 until the processor is snooped. When snooped, the S12x0 will wake (popup) the core processor into the lowest power snoopable state (C2), at which time the snoop can be serviced.

After servicing the snoop and not receiving further snoops in a time-out window, the S12x0 may put the core processor back into a lower power, unsnoopable, state (popdown). In order to allow chipset Popup feature to operate efficiently, the HardC4E should be activated.

The Hard C4E can be enabled through the bit[33] in the IA32_DEBUGCTL MSR. Once the Hard C4E is enabled, the exit latency from C4 to C2 will be shortened. Although this feature is enabled and setup by system BIOS, software should be aware of this behavior since it could lead to inaccurate C4 residency calculations caused by time spent in C2 servicing snoops instead of the software selected state of C4.

4.6.5 Recommended C-State Configurations

Following are recommended C-State configurations for Operating Systems that support MWAIT instructions:

- Expose MWAIT(C1) as ACPI C1 and MWAIT(C2) as ACPI C2 to the Operating System in AC mode
- Expose MWAIT(C6) as ACPI C3 to the Operating System in Battery mode.

Note: Some Operating Systems provide support for all available S12x0 C-states to be reported through ACPI

- If the system includes a bus master device that cannot tolerate long bus master latency, MWAIT(C4) and MWAIT(C6) should be reported with BM_STS avoidance bit set.

For Operating Systems that do not support MWAIT instructions, the recommended C-states should be exposed using the HLT instruction for ACPI C1 and LVLx register reads for ACPI C2 and ACPI C3.

4.6.6 Hardware Coordination of C-States

Table 4-8 depicts how the hardware coordination logic will resolve thread C-State mismatches to determine the shared area and package state per core.

Table 4-8. Thread Coordination Logic for C-States (Per Core)

Thread 0 State	Thread 1 State	Shared Area/Package State
TC0	TC0	C0
TC0	TC1, TC2, TC4	C0
TC1	TC0	C0
TC1	TC1, TC2, TC4	C1 or C1E
TC2	TC0	C0
TC2	TC1	C1 or C1E
TC2	TC2, TC4	C2 or C2E
TC4	TC0	C0
TC4	TC1	C1 or C1E
TC4	TC2	C2 or C2E
TC4	TC4	C4 or C4E
TC4 with Dynamic L2 On	TC1	C1 or C1E
TC4 with Dynamic L2 On	TC2	C2 or C2E
TC4 with Dynamic L2 On	TC4	C4 or C4E
TC4 with Dynamic L2 On	TC4 with Dynamic L2 On	C4 or C4E until L2 is zero in size LVL5 read issued after L2 is zero in size
TC6	TC0	C0
TC6	TC1	C1 or C1E
TC6	TC2	C2 or C2E
TC6	TC4	C4 or C4E
TC6	TC6	C4 or C4E until L2 is zero in size C6 after L2 is zero in size

The C-State hardware coordination logic at minimum requires operating system software to be able to support independent C-States (more than C1) per logical processor.

4.6.7 I/O Based C-State Hardware Coordination

Support for the MWait extensions and hints which enable native C-State instructions allows for optimal use of C-States in a Intel® Hyper-Threading Technology environment since it does not involve the North Complex. This is achieved by allowing individual threads to be placed at a low power C-State by using these instructions and without North Complex involvement. However, additional flexibility has been added to the S12x0 to allow for short term integration into operating systems, by providing an alternative to Monitor/MWait by means of I/O based C-States.

I/O based C-States will use the same hardware coordination logic as native MWait C-States but utilize a different interface. I/O based C-States can be enabled by BIOS.

4.6.8 C-States from I/O Instruction Decoded to MWAIT

If executing a MONITOR/MWAIT pair, software must ensure that no I/Os that are decoded to an MWAIT occur between the MONITOR and MWAIT instruction pair. The I/O redirected instruction will be internally translated to an MWAIT by the processor which will clear the monitor, and as a result the subsequent MWAIT will not result in the processor entering any optimized state and the execution will continue from the instruction following MWAIT.

4.6.9 C1 BIOS Coordination

In the event that the operating system does not support C-States in an MP environment, a mechanism exists in the S12x0 processor to generate SMIs when both execution threads enter C1. This mechanism will prove valuable to mobile systems since it allows a processor to enter C2, C4 and C6 despite operating systems limitations that only allow for C1. C1 BIOS Coordination is enabled by BIOS.

4.6.10 CPU C-State Triggering

Operating System can trigger a C-State request only if starting from C0 (remember, that is the only state Intel® architecture code can execute in). It can either:

- Issue an I/O PORT Read (when used for C-state changes, it is called a “level read”) to a location in the ACPI Processor Block (PMBA). See the register definition.
- Use a MONITOR – MWAIT IA instructions (recommended). This also gives additional C-State / Part specific hints for enter each C-State. This results in the core processor eventually performing the level read to the S12x0 North Complex.
- C1 is entered with execution of a HLT (HALT) Intel® architecture instruction.
- C2 can be entered from C4 to handle snoops (C2-popup).

Table 4-9. FTH MWAIT Parameters

CX	ECX		EAX				Description
	RSVD	UBNOINT	RSVD	State	Sub-state		
	31:1	0	31:8	7:4	3	2:0	
C0	0	0	0	1111	x	000 = Cx 001 = CxE Others = rsvd	Skip Mwait
C1	0	0/1	0	0000	0	000 = Cx 001 = CxE Others = rsvd	Subs[2:0]: C1 / C1E
C2	0	0/1	0	0001	x	000 = Cx 001 = CxE Others = rsvd	Subs[2:0]: C2 / C2E
c3	0	0/1	0	0010	x	000 = Cx 001 = CxE Others = rsvd	C3 ===> C4 Subs[2:0]: C4 / C4E
c4	0	0/1	0	0011	0= Shrink 1= NoShrink	000 = Cx 001 = CxE Others = rsvd	Subs[2:0]: C4 / C4E Sub[3]: No Shrink Flavor
C5	0	0/1	0	0100	x	000 = Cx 001 = CxE Others = rsvd	C5 ===> C4 Subs[2:0]: C4 / C4E
C6	0	0/1	0	0101	0= Shrink 1= NoShrink	000 = C6 001 = C6E 010 = C6S Others = rsvd	Subs[2:0]: C6 / C6E (both exit to LFM) C6S – shrink full cache in one step Sub[3]: No Shrink Flavor

Details on Entry Modes to various C-States (as seen by the S12x0 North Complex):

- C1 is transparent to the North Complex.
- C2 is entered when the CPU reads the LVL2 register, and from C3/C4 if bus masters require snoops.
- C3 is entered when the CPU reads the LVL3 register, and after a return to C2 from a prior C3 state.
- C4 is entered when the CPU reads the LVL4 register, and after a return to C2 from a prior C4 state.
- C5/C6 is entered when the CPU reads the LVL5/6 register.

4.7 Transition Rules Among C States and S States

The following priority rules and assumptions apply among the various S0/Cx and throttling states:

- Entry to any S0/Cx state is mutually exclusive with entry to an Sx state. Sleep states have higher priority.
- When PM1C.SLPEN is set (system going to S3, S4, or S5), throttling is disabled.
- If a LVL2/3/4/5/6 read occurs during throttling (PCNT.TEN or PCNT.TFORCE set), the system transitions to the Cx state. This has higher priority than software throttling.
- After an exit from a Cx state (due to a break event), if PCNT.TEN or PCNT.TFORCE is set, the system continues throttling.

Before entering an S state, the OS masks all interrupts and disables all bus masters.

4.8 System Sleep State Control (S States)

The S12x0 supports the S3, S4, and S5 sleep states. S4 and S5 states are identical from a hardware perspective.

The processor platform architecture assumes the usage of External Circuitry (EC) for Sleep State control. Some flows in this section refer to the EC for support of the S states transitions.

The processor is returned to the S0 state from S3, S4 and S5 by wake events. The wake events can be initiated by:

- Internal and external events to the processor, therefore, the processor requires the Suspend (SUS) Well power to stay on when it is in S3 state.
- The EC, since the processor cannot initiate an exit from S4 or S5 on its own. Therefore the SUS Well power is disabled in S4/S5 state. Only the RTC Well power stays on in S4/S5 state.

4.8.1 S-State Definition

4.8.1.1 S0 - Full On

This is the normal operating state of the processor. In S0, the core processor will transition in and out of the various processor C-States and P-States.

4.8.1.2 S3 - Suspend to RAM (Standby)

S3 is a suspend state where the Core Well power planes of the S12x0 are turned off and the SUS Well power remains powered.

- All power wells are disabled, except for the SUS and RTC power wells.
- The core processor macro-state is saved in memory.
- Memory is held in self-refresh and the memory interface is disabled, except the CKE pin as it is powered from the SUS voltage rail. CKE is driven low.

4.8.1.3 S4 - Suspend to Disk (Hibernate)

S4 is a suspend state where all power planes of the S12x0 are turned off, except for the RTC well. In this ACPI state, system context is saved to the hard disk.

Key features:

- No activity is allowed.
- All power wells are disabled, except for the RTC well.
- A full system reset is required to resume from S4.

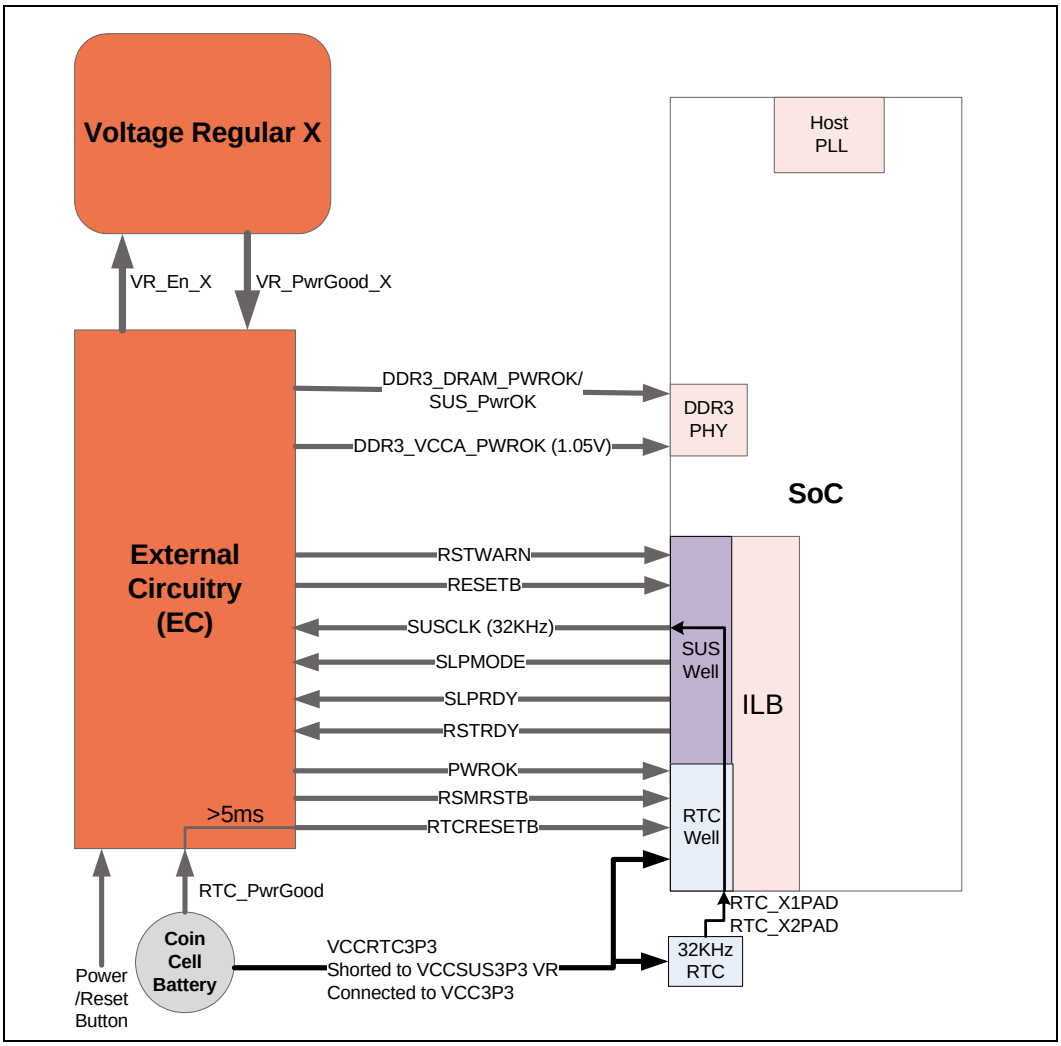
4.8.1.4 S5 - Soft Off

From a hardware perspective the S5 state is identical to the S4 state. The difference is purely software, in that, software does not write system context to hard disk when entering S5.

4.8.2 Power Well Transition Sequence

Figure 4-1 shows a simplified platform power management control. The purpose is to show the key connectivity related to power-on and S-State transitions between the S12x0 and related board components.

Figure 4-1. Power Management System Connectivity



4.8.2.1 RTC Power Well Transition (G5 -> G3)

This sequence occurs when the RTC battery is first inserted. When power is re-applied, the following occurs:

1. VCCRTC ramps.
2. RTCRESETB should be held low.
3. RTCCLK (32KHz from external crystal) starts automatically with VCCRTC. See later steps for when it becomes stable.
4. After VCCRTC ramps, EC de-asserts RTCRESETB. The system is now G3:
   a. VCCRTC ON; RTCRESETB de-asserted; RTC Oscillator stable (in RTC power well).
   b. VCCSUS OFF; RSMRSTB remain asserted.
   c. SUSCLK not available.
   d. VCCORE OFF; PWROK low; all internal PLLs off.

4.8.2.2 Transition without G3/G2

This sequence must be adhered to in cases where one of the following conditions apply:

1. The system does not implement an RTC battery (coin cell) or a main battery.
2. The coin cell is drained with no main or a dead main battery.
3. No coin cell implemented or dead coin cell and main battery is being swapped.

AND one of the following conditions also applies:

1. The platform does not implement a power button to initiate a sequence to S0, and battery or AC power become available.
2. The platform does use a power button, but the default first sequence when power is available is entry into S0.

In these cases, the relation between RTC and SUS power wells becomes important.

1. VCCRTC ramps.
2. RTCRESETB should be held low.
3. RTCCLK (32KHz from external crystal) starts automatically with VCCRTC. See later steps for when it becomes stable.
4. After VCCSUS ramps, EC de-asserts RTCRESETB.
   a. VCCRTC ON; RTCRESETB de-asserted; RTC Oscillator stable (in RTC power well).
   b. VCCSUS ON; RSMRSTB de-asserted.
   c. SUSCLK available.
   d. VCCORE ON; PWROK high; all internal PLLs on.

4.8.2.3 SUS Power Well Transition

This section describes how the SUS well powers-up and comes out of reset. This section covers several different scenarios (there are many commonalities):

- G3 exit.
- Global reset exit.

The following table describes the G3 to S5 portion flow, used for Cold Boot.

Note: In cases where a coin battery is present, the system will already be in the G3 state (VCCRTC and RTCCLK will already be stable and RTCRESETB high). Otherwise, VCCRTC ramps with VCCSUS:

1. Board event such as AC power or power button press.
2. VCCSUS (SUS well rails) ramp in the order mentioned in Section 4.3.3, “Voltage Sequencing Requirements” .
3. After VCCSUS stable, RSMRST_B can be de-asserted. DDR3_DRAM_PWROK (to DDR3 PHY 1.5 power well) can be asserted by EC; this is used by DDR3 PHY firewall control to keep DRAM in self refresh.
4. RSMRSTB high causes SUS power well pins traps to latch.
5. After RSMRSTB is high, RTCCLK stabilization counter expires and RTCCLK is considered stable.
   SUSCLK output (32 KHz) will begin toggling. This is a feed through from the RTC crystal clock input (from RTC power well to SUS power internally).
   — Internally, in the case that RTC oscillator clock has not stabilized, the propagation of RSMRSTB should be delayed until stabilization of RTC oscillator clock occurs (which gets sent out as SUSCLK).
6. SUSCLK (32 KHz) is driven to the board.

System is now in S4/S5:

- VCCRTC ON; RTCRESETB de-asserted; RTCCLK stable.
- VSSSUS ON; RSMRSTB de-asserted; DDR3_DRAM_PWROK asserted.
- SUSCLK Available (assume coin cell battery is available).
- VCCCORE OFF; PWROK low; all internal PLLs off.

4.8.3 Sleep State Transitions

To enter an S-State the OS will send a message to all drivers that a sleep event is occurring. When the drivers have finished handling their devices and completed all outstanding transactions, they each respond back to the OS. When all drivers have completed their sleep routines, the OS will write the Sleep Type and Sleep Enable bits in the internal Power Management Unit (PMU), using I/O write cycles. Since the sleep routine in the OS was a call, the CPU returns to the calling code and waits in a loop polling on the wake status bit.

The S-State and C-State flows are separate flows in the OS, and the S12x0 will hang if any code were to write to Sleep Enable and then do an MWAIT to put the package into a C-State.

Note: The S12x0 hardware does not check for this condition and depends on software to never create the case where there are simultaneous C-State and S-State requests outstanding.

4.8.3.1 Initiating Sleep States

It is assumed that the OS has stopped all threads before issuing the IOWr from one of the threads.

Entry to Sleep states (S3, S4, S5) are initiated by any of the following methods:

- OS performing IOWrite setting the desired type in PM1C.SLPTYP and setting PM1C.SLPEN.
- Assertion of THERMTRIPB which causes a transition to S5. This may occur when the system is in S0.
- Detection of a catastrophic temperature event causes a transition straight to S5, if enabled. This can occur in any state that the main power well is on.
- Internal watchdog timer expires, and watchdog timer is enabled for shutdown in WDTC register.

4.8.3.2 S3-to-S0 Sleep Exit Sequence and Timing

Exit from the S3 Sleep state can be triggered by a Wake Event that is either internal to the SoC or external to the SoC.

4.8.3.2.1 Internally-Triggered Wake Event

Exit from the S3 Sleep state can be triggered by these internal events:

- An alert from the Real-Time Clock Alarm
- An indication from an enabled GPIOSUS signal pin to exit S3 and resume.
- The active-low WAKE_B input signal pin is asserted. WAKE_B is provided for the external PCI Express* devices to wake the system.

Once triggered, the following sequence follows:

1. The SoC de-asserts the active-low SLPRDYB output signal pin to indicate to the external circuitry (EC) that the SoC needs to wake up.
2. The EC enables all power supplies, including the core rail, in preparation for full power-on (S0 state) operation. At this point the SoC input signal PWROK, driven by the EC, remains low.
3. At this point, the sequence continues as stated in "S4/5-S0 Sleep Exit Sequence and Timing" on page 78, steps 5 through 10 with the current signal states:
   — active-low SLPRDYB output signal pin is high
   — active-low RSTRDYB output signal pin is low
   — active-high SLPMODE output signal pin is high

4.8.3.2.2 Externally-Triggered Wake Event

Exit from the S3 Sleep state can be triggered various events detected by the external circuitry (EC). When detected by the EC, the sequence is as follows:

1. The EC enables all power supplies, including the core rail, in preparation for full power-on (S0 state) operation. At this point the SoC input signal PWROK, driven by the EC, remains low.
2. At this point, the sequence continues as stated in "S4/5-S0 Sleep Exit Sequence and Timing" on page 78, steps 5 through 10 with the current signal states:
   — active-low SLPRDYB output signal pin is low
   — active-low RSTRDYB output signal pin is low
   — active-high SLPMODE output signal pin is high

4.8.3.3 S4/5-S0 Sleep Exit Sequence and Timing

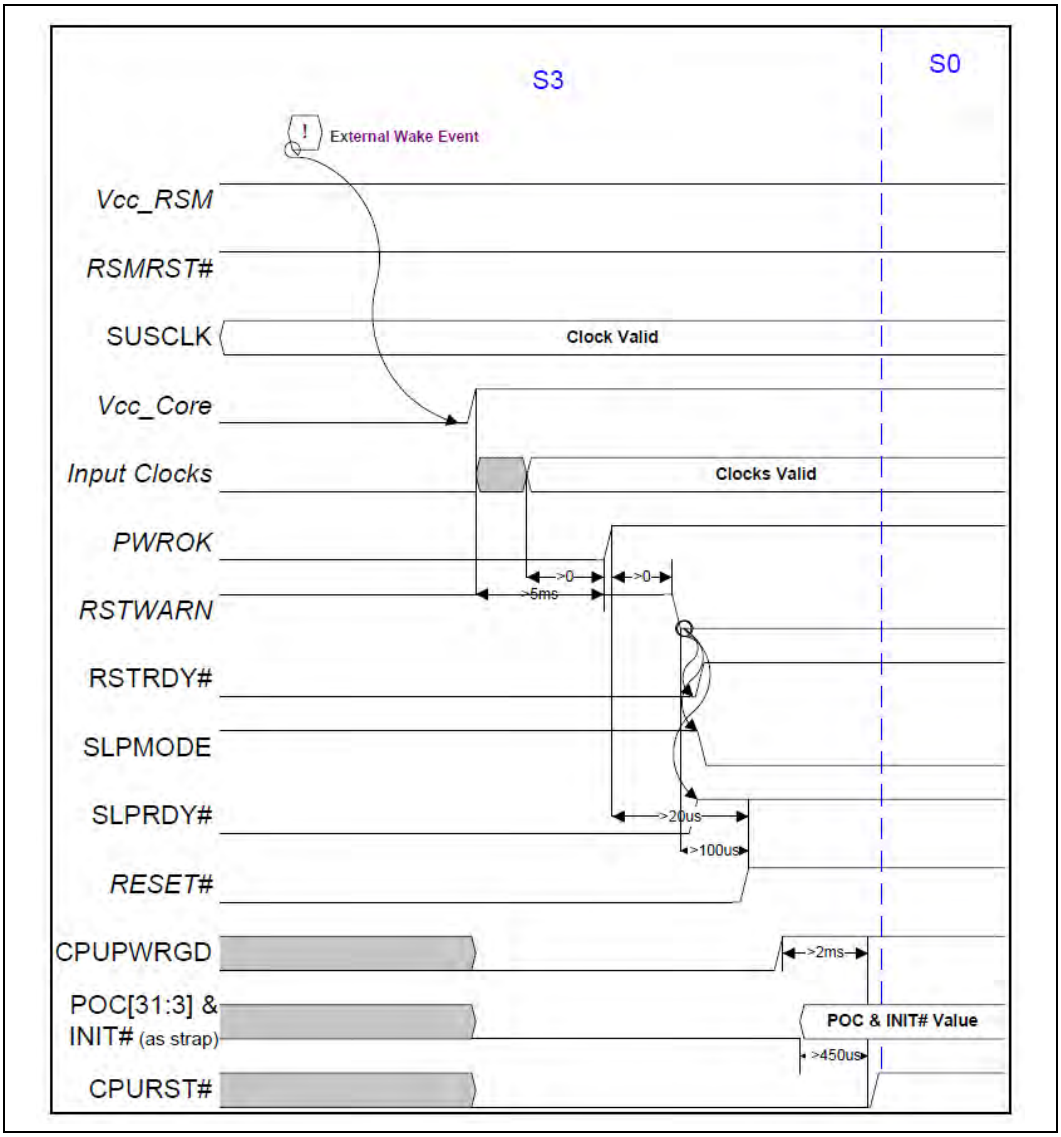
The SoC relies on the external circuitry (EC) to start the SoC transition from the hibernate (S4) or soft-off (S5) Sleep state to the full-on S0 state. Once the S0 state is achieved, the SoC sets the Wake Status bit of the Power Management 1 Status (PM1S.WAKE) register. The general S4/S5-to-S0 sequence is as follows.

1. Initially these SoC signal pins are driven by the EC:
   - active-low RSMRSTB input signal pin is low
   - active-low RESETB input signal pin is low
   - active-high PWROK input signal pin is low
2. The EC detects an event such as the system power-on button made active.
3. The EC brings up the SUS supply voltages in the following order: 3.3V, 1.8V, 1.5V, and 1.05V.
4. Once the SUS voltages are up and stable, the EC drives the active-low RSMRSTB input signal pin high. The SoC internal 32-kHz clock becomes active.

Step 5 is the entry point from the S3-to-S0 sequences shown in Section 4.8.3.2.1, “Internally-Triggered Wake Event” on page 77 and Section 4.8.3.2.2, “Externally-Triggered Wake Event” on page 77.

5. After a period of time, the EC brings up the CORE supply voltages in the following order: 3.3V, 1.8V, 1.5V, 1.05V (VNN) and VCC.
6. When the CORE voltages become stable, the SoC enables its internal clocks.
7. After a period of time, the EC asserts the PWROK input signal pin.
8. If not already de-asserted, the EC de-asserts the RSTWARN input signal pin.
9. After some delay period, the active-high SoC output signal SLPMODE is driven low and the active-low SoC output signals SLPRDYB and RSTRDYB are driven high.
10. After sufficient delay from it de-asserting RSTWARN and asserting PWROK, the EC de-asserts the RESETB input signal pin.

Figure 4-2. S3-to-S0 Transitions



4.9 Main Memory Power Management

The S12x0 manages the power consumed by both the memory controller and the DRAM devices. The DDR3 SDRAM devices provide two ways to reduce power consumption: Power-Down state and Self-Refresh state. The memory controller manages these two power-saving DDR SDRAM states and, in addition, controls a number of its own components to further reduce power consumption.

Additional details of DDR3 SDRAM memory component operation can be found in the JEDEC Association Standard No. JESD79-3E, *DDR3 SDRAM Specification*.

The memory controller supports memory power management in the following conditions:

- Active Power Down - When no commands are visible for the rank, the rank power down idle timer has expired, and one or more pages are open.
- Pre-charge Power Down - When no commands are visible for the rank, the rank power down idle timer has expired, and all pages are closed.
- Dynamic Self Refresh - When Dynamic Self-Refresh is enabled, all pages in all ranks are closed, no commands in the command queue or being received from the north cluster, the status priority level from the north cluster is below 2, and the self-refresh idle timer has expired.
- Self Refresh - Entered when the suspend message is received from internal circuit blocks.

4.9.1 During Power-Up

During power-up, the S12x0 integrated memory controller output signals, DDR3 Clock Enables (DDR3_CKE[1:0]), are recognized by the DDR3 SDRAM components. At power-up, besides their clock enable (CKE) input pins, the DDR3 SDRAM components only recognize their RESET# input pins (driven by DDR3_DRAMRSTB). During power-up, the integrated memory controller drives DDR3_CKE[1:0] low to ensure that the SDRAM components float their data (DQ) and data strobe (DQS) signals during power-up and continue to do so until the BIOS is ready to release the CKE from the low state.

4.9.2 During System Operation

The main memory is power-managed during normal operation (C0 C-State), and when the CPU is in the low-power ACPI C-States. Most of memory power management is managed by the S12x0 integrated memory controller.

The memory controller supports the memory-device power management modes (also called states) when the following conditions occur:

- Active Power-Down Mode - The S12x0 commands the DDR3 SDRAM to enter this mode when there are no memory commands apparent for the memory Rank (memory devices connected to the same chip select), the S12x0 Rank power-down idle timer has expired, and one or more memory-device Banks are open (Active).
- Precharge Power Down Mode - This is entered when no memory commands are apparent for the memory Rank, the S12x0 Rank power-down idle timer has expired, and all memory-device Banks are closed (Idle).
- Dynamic Self-Refresh Mode - If the S12x0 Dynamic Self-Refresh is enabled, this mode is entered when all Banks in all Ranks are closed (Idle), no memory commands are in the command queue or being received by the integrated memory controller, and the S12x0 self-refresh idle timer has expired.
- Self-Refresh Mode - This is entered when the S12x0 commands the DDR3 SDRAM to enter this mode when the integrated Power Management Unit (PMU) sends a suspend message to the integrated memory controller.
- Page Management - Power is saved by closing memory pages.
- Refresh Mode Power Savings - The S12x0 reduces the number of regular Refresh (REF) commands.
- Conditional Self-Refresh - The DDR3 memory is placed into Self-Refresh mode while remaining in a low-power state.
- Other Power Saving Features.

4.9.2.1 DDR3 Power-Down Modes

When DDR3 SDRAM devices are these modes, a number of their input and output buffers are deactivated and the SDRAM internal clock is disabled. DDR3 SDRAM Power-Down is applied per Rank whenever a Rank is inactive. This is called Dynamic Rank Power-Down. If all the memory device Banks have all been closed (idle) at the time of DDR3 clock enable (CKE) DDR3_CKE[1:0] pin de-assertion, the DRAM devices enter the Precharge Power-Down state. Otherwise the devices enter the Active Power-Down state.

4.9.2.2 DDR3 Self-Refresh Mode

Self Refresh mode is used to retain data in the DDR3 SDRAM devices, even if the rest of the system is powered down. When the memory is in Self-Refresh mode, the S12x0 integrated memory controller disables all of its output signals except the CKE clock enables (DDR3_CKE[1:0]) and RESET# (DDR3_DRAMRSTB) signals.

Self-Refresh mode has two main usage modes:

- Power-saving during normal operation during idle periods.
- Sustaining DDR3 SDRAM content when the system moves to S3 power state.

There are two modes for system-triggered Self-Refresh Entry/Exit - Dynamically and from internal messages from the internal Power Management unit (PMU). Additionally, the integrated memory controller may initiate a short Self-Refresh Exit/Entry cycle for periodic RCOMP updates.

The S12x0 integrated memory controller uses what is called dynamic Self-Refresh during normal operation in order to support the maximum power savings mode. It wakes the memory from Self-Refresh mode whenever a memory request is received, then re-enters Self-Refresh mode when the memory controller is idle and the self-refresh timer expires.

The integrated memory controller supports an internal programmable power-management command that is sent to the physical layer circuitry into order enter a low power mode. The selection of which low power mode is selected based upon power savings versus self-refresh exit latency. In general, the higher power saving states require larger self-refresh exit latencies because it takes longer to power on all of the features.

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5 Thermal Management

The Intel® Atom™ Processor S1200 Product Family for Microserver (S12x0) is the new generation of System-On-Chip (SoC) 64-bit processor; dual-core processors built on 32-nanometer process technology.

The S12x0 implements configurable forms of Thermal Management for itself, the DDR3 SDRAM, and system-level thermal limits. It supports both thermal-sensor-based and event-counter-based thermal management It has several forms of threshold evaluation called trip mechanisms. It also has one configurable form of threshold enforcement called throttling with four unique limits.

The S12x0 contains many techniques to help better manage thermal attributes of the processor:

Intel® Thermal Monitor and Intel® Thermal Monitor 2:

- Provides thermal management.

Enhanced Digital Thermal Sensor (DTS):

- One Digital Thermal Sensor per core of the dual-core S12x0.
- Provides per-thread temperature sensing.

Details of the registers for thermal management are listed in Volume 2 of this Datasheet.

For additional information about implementing the thermal-management features in this document, refer to the Thermal/Mechanical Design Guide (TMDG) document for the S12x0.

For BIOS developers, refer to the BIOS Writer's Guide for the S12x0.

5.1 Intel® Thermal Monitor

Intel® Thermal Monitor (TM) is a feature of the processor. It provides thermal-based clock throttling.

When TM is enabled and active due to the die temperature reaching the pre-determined TM-activation temperature, the Thermal Control Circuit (TCC) of the processor attempts to cool the processor by alternating these processes:

1. stopping the processor clocks for a period of time.
2. run the processor clocks full-speed for a period of time:
   — performed at a duty cycle ~30% – 50%.

This alternation is performed by the TCC until the processor temperature drops below the activation temperature.

The temperature that triggers the TM is set during the fabrication of the S12x0 and is visible to software.

5.2 Intel® Thermal Monitor 2

Intel® Thermal Monitor 2 (TM2) is a feature of the processor. It provides thermal-based Enhanced Intel SpeedStep® Technology transitions. When TM2 is enabled and active due to the die temperature reaching the pre-determined TM2-activation temperature, the Enhanced Thermal Control Circuit (TCC) of the processor attempts to cool the processor by performing the following 2-step process:

1. Reduce the core activity to about one-half the bus-to-core ratio that it was at power-on.
2. Step-down the core VCC voltage.

The temperature that triggers the TM2 is set during the fabrication of the S12x0 and is visible to software.

5.3 Processor-Hot Signal Pin

The S12x0 provides a pin (CPU_PROCHOTB) for the output signal, Processor Hot. It is an active-low signal and is asserted when the processor die temperature has reached its maximum operating temperature. The processor can be programmed to generate an interrupt upon the assertion or de-assertion of Processor Hot.

The CPU_PROCHOTB pin is default-configured as an output-only signal, but it can be programmed to be a bi-directional signal and driven from an external source. In this mode, when CPU_PROCHOTB is asserted (the pin is asserted as a low) it triggers either the TCC or Enhanced TCC circuitry, discussed above, as programmed by an enable bit for TM1 or an enable bit for TM2, respectively. It is required that either TM1 or TM2 is enabled.

For dual-core product SKUs of the S12x0, if one core indicates Processor Hot, it activates the TM1 or TM2 activity on both cores. In a sense, the hot core acts as an external agent to the other core.

5.4 On-Demand Mode

Besides the automatic activation of the Thermal Control Circuit (TCC) discussed above, the portion of the Thermal Control Circuit that enables processor clock modulation can be enabled and disabled by software. This is the On-Demand feature. On Demand sets its own clock-modulation duty-cycle. This is done through the 64-bit register, A32_CLOCK_MODULATION of the Model Specific Register (MSR). This register is replicated per thread and the hardware resolves different, programmed duty-cycles by picking the one with highest performance.

If both the On-Demand Thermal portion of the TCC is enabled by software and the automatically-activated TCC is enabled, the automatic TCC and its modulation values take precedence.

5.5 Thermal Diode

For each core, the S12x0 incorporates an on-die PNP transistor. Its base-to-emitter junction is used as a thermal diode. Its collector is shorted to ground. The anode and cathode of the thermal diode for each core are attached to the component pins:

Thermal Diode for CPU0:

- Anode: CPU0_THERMDA (input pin).
- Cathode: CPU0_THERMDC (output pin).

Thermal Diode for CPU1:

- Anode: CPU1_THERMDA (input pin).
- Cathode: CPU1_THERMDC (output pin).

Note: The on-die thermal diodes are available but not supported on the Intel® Atom™ Processor S1200 Product Family. The on-die Digital Thermal Sensor (DTS) is available for die temperature monitoringS12x0.

5.6 On-Die Digital Thermal Sensor (DTS)

Each S12x0 core processor also contains a ring-oscillator based, on-die Digital Thermal Sensor (DTS) that can be read by means of a Model-Specific Register (MSR). There is no other I/O interface. In a Hyper-Threading (HT) implementation of the S12x0 processor, each thread has a unique digital sensor whose temperature is accessible by means of MSR.

The digital sensor is the preferred method of reading the CPU die temperature since they are located much closer to the hottest portions of the die. They can track the die temperature more accurately and activate CPU throttling by means of the Intel® Thermal Monitor.

The thermal sensors can be programmed to trigger hardware throttling and/or software interrupts. Hardware throttling affects a number of internal blocks. Resulting interrupt types include Message Signaled Interrupts (MSI), System Management Interrupts (SMI), and System Control Interrupts (SCI). It is expected that SCI is the most likely interrupt type to be used, while SMI is provided for flexibility and for potential anomaly work-arounds.

The S12x0 is capable of producing enough heat to damage the part if the ambient temperature is high enough, especially in passively-cooled systems. For example, the Thermal Design Power (TDP) budgets do not take into account maximum I/O traffic that the part is capable of supporting, but rather a practical maximum. Reducing the data traffic or clock frequency based on monitoring activity to guarantee that it can never go over the maximum temperature in any environment can cause performance to suffer even in good thermal environments where the temperature of the part is never really in danger. The S12x0 temperature varies due to:

External conditions:

- Ambient temperature due to location of the system.
- System fan vents are blocked.
- Heat produced by other components of the platform.

Internal conditions:

- Light versus heavy integrated peripheral workload.
- Idle versus intensive memory workloads.
- Lightly-connected system versus a highly-connected system.

Counter-based throttling cannot detect situations such as fan failure and heatsink detachment. In some cases, it is advisable that the S12x0 be configured to trigger an interrupt to ACPI to allow fan control. If throttling is not sufficient to keep temperatures from rising, then the a trip point can be used to lower platform power by the S12x0 assertion of the active low, open-drain, CPU_PROCHOTB signal. This signal is bi-directional and can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via CPU_PROCHOTB can provide a means for thermal protection of system components.

For additional information about implementing the DTS, refer to the Thermal/Mechanical Design Guide (TMDG) for the S12x0. For BIOS programming details, refer to the BIOS Writer's Guide for the S12x0.

5.7 SoC Thermal Sensor

Four signal pins are provided:

Thermal Diode for CPU0:

- Anode: SOC_THERMDA (input pin).
- Cathode: SOC_THERMDC (output pin).

For Design For Testability purposes:

- SOC_THERMREFNPAD = This pin must be connected to ground with an external 8 KΩ resister on the platform board
- SOC_THERMANATP[1:0] = Analog Test Ports.

5.8 Catastrophic Overheating Thermal Sensor

Pin: THRMTRIPB (Open Drain)

The S12x0 protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor stops all execution when the junction temperature exceeds approximately 125 °C. This condition is signaled to the system by the active-low, open-drain THERMTRIPB (Thermal Trip) signal pin.

Assertion of THERMTRIPB causes an immediate transition to the Soft-Off, S5 Sleep State. This assertion may occur when the system is in the System On, S0 state.

5.9 Thermal Throttling of DRAM Transactions

The S12x0 has the capability to independently throttle read and write transactions sent to a given rank of memory in order to assist the system in throttling DRAM bandwidth for thermal reasons.

5.10 Thermal Alarm

Pin: THERMB (input)

The Thermal Alarm is an active-low signal is generated by external hardware. When it is asserted, a System Management Interrupt (SMI#) or System Control Interrupt (SCI) is generated depending on how the interrupts are routed internally and whether these interrupts are enabled. The circuitry for the pin is in the Suspend (SUS) power well of the S12x0.

5.11 Thermal Control and Status Registers

This is a summary of registers that pertain to thermal management. Details of the registers for thermal management are listed in Volume of this .

5.11.1 Thermal Diode Offset Register

Read-only 64-bit register that conveys the delta between the temperature reported by the thermal diode and the die temperature. The value in this register must be subtracted from the diode reading in order to obtain the true die temperature. The delta should also be applied to any threshold values used. The BIOS must apply this offset to the thermal diode reading to obtain the true die temperature.

5.11.2 Performance Status Register

64-bit register allows the system BIOS or OS to determine the current processor performance state, and also determine maximum and minimum operating points of the processor.

5.11.3 Root Fabric (RTF) Thermal Throttle Register

Thermal-throttle period values for RTF arbiter grants.

5.11.4 ACPI Intel® Thermal Monitor Control Register - Clock Modulation

64-bit register accessed only when referenced as a Qword through a Read MSR (RDMSR) or Write MSR (WRMSR) instruction. This register is used to read and write the duty cycle bits, and to enable the on-demand clock modulation feature of the Intel® Thermal Monitor:

- Allows the BIOS to activate or deactivate the On-Demand Thermal Control Circuit (TCC) portion of the Intel® Thermal Monitor feature.
- Provides the On-demand clock modulation duty cycle.

5.11.5 ACPI Intel® Thermal Monitor Interrupt Control Register - Thermal Interrupt

64-bit register accessed only when referenced as a Qword through a Read MSR (RDMSR) or Write MSR (WRMSR) instruction. This register is used to program the interrupt capabilities for the Intel® Thermal Monitor:

- Various temperature-related interrupt enables and threshold value conditions.

5.11.6 ACPI Intel® Thermal Monitor Status Register - Thermal Sensor

64-bit register accessed only when referenced as a Qword through a Read MSR (RDMSR) or Write MSR (WRMSR) instruction. This register is used to read the status for the integrated thermal sensor:

- Digital readout and thermal threshold information.

5.11.7 ACPI Intel® Thermal Monitor Control Register - Thermal Control

64-bit register accessed only when referenced as a Qword through a Read MSR (RDMSR) or Write MSR (WRMSR) instruction. This register is used to configure and enable the Intel® Thermal Monitor feature:

- Provides the frequency (bus ratio) and the voltage to use for the throttled performance state that will be initiated when the on-die sensor goes from not hot to hot.

5.11.8 ACPI Intel® Thermal Monitor Control Register - Thermal Status

64-bit register accessed only when referenced as a Qword through a Read MSR (RDMSR) or Write MSR (WRMSR) instruction. This register is used to read the status for the integrated thermal sensor:

- Various temperature-related logs and status.

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6 Signal Descriptions

This chapter provides a detailed description of the signals and boot strap definitions for the S12x0. The signals are arranged in functional groups according to their associated interface.

Each signal description table has the following headings:

- **Signal**: The name of the signal ball/pin.
- **Direction and Type**: The buffer direction and type. Buffer direction can be input, output, or I/O (bidirectional). See Table 6-1 for definitions of the different buffer types.
- **Power Well**: The power plane used to supply power to that signal. There are three power wells: Core; SUS (Suspend/Resume); RTC.
- **Description**: A brief explanation of the signal function.

Table 6-1. Buffer Types

Buffer Type	Buffer Description
CMOS1.05 CMOS1.05_OD	1.05V CMOS buffer, or CMOS Open Drain.
CMOS1.5	1.5V CMOS buffer.
CMOS1.8	1.8V CMOS buffer.
CMOS3.3 CMOS3.3_OD	3.3V CMOS buffer, or CMOS 3.3V Open Drain.
PCIe* Gen 2	PCI Express* interface signals. These signals are compatible with *PCI Express Base Specification - Revision 2.1*. Section 4.3 Electrical Sub-block. Each lane of a PCI Express link is AC coupled. The buffers are not 3.3V tolerant.
Analog	Analog reference voltage, input/output signal, or connection to an external or internal passive component.
Analog1.8	Analog input/output signal using circuitry powered by the 1.8V supply.

6.1 System DDR3 Memory Signals

Table 6-2. System Memory Signals (Sheet 1 of 3)

Signal	Direction/ Type	Power Well	Description
DDR3_ODT[1:0]	I/O CMOS1.5	Core	**DDR3 On-Die Termination Enable:** (active high) One pin per rank, 2 ranks supported. Enables SDRAM On-Die Termination during Data Write or Data Read transactions.
DDR3_CK[1:0] DDR3_CKB[1:0]	I/O CMOS1.5	Core	**Differential DDR3 Clock:** DDR3 Differential Clock output to DDR3 DIMMs and SDRAM. All command and control signals are valid on the rising edge of DDR3_CK. Each pair corresponds to each rank on DRAM side.
DDR3_CKE[1:0]	I/O CMOS1.5	SUS	**DDR3 Clock Enable:** (active high) Output used for power up /power down and self refresh of the SDRAM devices. There is one DDR3_CKE per rank. Enables/Disables SDRAM internal clock signals and device input buffers and output drivers.
DDR3_CSB[1:0]	I/O CMOS1.5	Core	**DDR3 Chip Select:** (active low) One pin per rank, 2 ranks supported. Used to qualify the command on the command bus for a particular rank. Selects one rank as the target of the Command and Address and is considered part of the Command Code.
DDR3_RASB	I/O CMOS1.5	Core	**DDR3 Row Address Strobe:** (active low) This signal is used with DDR3_CASB, DDR3_WEB, and DDR3_CSB to define the Command Code.
DDR3_CASB	I/O CMOS1.5	Core	**DDR3 Column Address Strobe:** (active low) This signal is used with DDR3_RASB, DDR3_WEB, and DDR3_CSB to define the Command Code.
DDR3_WEB	I/O CMOS1.5	Core	**DDR3 Write Enable:** (active low) This signal is used with DDR3_CASB, DDR3_RASB, and DDR3_CSB to define the Command Code.
DDR3_BS[2:0]	I/O CMOS1.5	Core	**DDR3 Bank Select:** (active high) Also known as the **Bank Address**, defines which banks are being addressed within each rank. Also, determines which Mode Register is to be accessed during a Mode Register Set cycle.
DDR3_MA[15:0]	I/O CMOS1.5	Core	**DDR3 Memory Address:** Output, multiplexed: Row Address for Active commands; Column Address for Read and Write commands. Selects one location out of the memory array in the respective bank. Also, provides the Op-Code during Mode Register Set commands. These signals follow common clock protocol w.r.t. CK/CKB pairs
DDR3_DQ[63:0]	I/O CMOS1.5	SUS	**DDR3 Data Bus:** Memory Read and Write Data. Data signal interface to the SDRAM data bus. These 64 bits signals have 8 Byte Lanes, and each Byte lanes have corresponding strobe pair.
DDR3_ECC[7:0]	I/O CMOS1.5	SUS	**DDR3 ECC Bus:** Memory Error Correction Code driven along with Read and Write Data.
DDR3_DQSECC DDR3_DQSECCB	I/O CMOS1.5	Core	DDR3 ECC Strobe: Differential-pair output with read-data ECC, Differential-pair input with write-data ECC. Edge-aligned with read-data ECC, centered in write-data ECC.
DDR3_DQS[7:0] DDR3_DQSB[7:0]	I/O CMOS1.5	Core	DDR3 Data Strobes: Differential-pair outputs with read data, Differential-pair inputs with write data. Edge-aligned with read data, centered in write data. Different numbers of strobes are used depending on whether the connected DRAMs are x4, or x8.
DDR3_CLKREFP DDR3_CLKREFN	I CMOS1.5	Core	**DDR3 Clock Reference:** Differential-pair input. Used to provide clocking to the DDR PLL and PHY portion of the integrated Memory Controller. 100MHz.

Table 6-2. System Memory Signals (Sheet 2 of 3)

Signal	Direction/ Type	Power Well	Description
DDR3_DRAMRSTB	I/O CMOS1.5	SUS	**DDR3 DRAM Reset:** (active low) Asynchronous output Reset signal to DIMM and SDRAM devices.It is common to all ranks.
DDR3_DRAM_PWROK	I CMOS 1.5	SUS	**DDR3 DRAM Power OK:** (active high) Input driven by the platform board and used by the integrated Memory Controller PHY circuitry firewall to keep the SDRAM in Self-Refresh Mode. This signal indicates the status of VCC_DDR3_1P5 power supply.
DDR3_SYSPWRGOOD	I CMOS 1.5	SUS	**DDR3 System Power Good:** (active high) Input driven by the platform board and used by the integrated Memory Controller to qualify that the VCC 1.05V power source is valid. Used for S3 Sleep-State isolation inside the integrated Memory Controller PHY circuitry.
DDR3_VREF	I (see description)		**DDR3 Voltage Reference:** External voltage reference from a resistor-divider on the platform board. • 0.75 V for 1.5-Volt DDR3 SDRAMs • 0.675 for 1.35-Volt DDR3L SDRAMs
DDR3_DQPU	I/O Analog		**DDR3 Data Pull-Up Resistor:** Compensation PAD. This signal needs to be terminated to VSS on board using the RES of 30.1 ohms. This external resistor termination scheme is used for Resistor compensation of DQ buffers.
DDR3_CMDPU	I/O Analog		**DDR3 Command Pull-Up Resistor:** Compensation PAD. This signal needs to be terminated to VSS on board using the RES of 27.4 ohms. This external resistor termination scheme is used for Resistor compensation of CMD buffers.
DDR3_ODTPU	I/O Analog		**DDR3 On-Die Termination Pull-Up Resistor:** Compensation PAD. This signal needs to be terminated to VSS on board using the RES of 274 ohms. This external resistor termination scheme is used for Resistor compensation of DDR ODT strength.
SPD_ENB	I CMOS1.05	CORE	**SPD Enable:** (active low) Input function-strapping signal. DIMM SPD discovery and usage of the SMBus 1.0 for SPD: 0 = Asserted. Enabled; SPD is expected. 1 = Not Asserted. Disabled; no SPD, i.e., soldered SDRAM.
MEM_SPEED[1:0]	I CMOS1.05	CORE	**DDR3 Memory Speed:** (active high) Input function-strapping signals decoded to set the DDR3 SDRAM speed when SPD is not used or required: 00: DDR3-1066 01: DDR3-1333 10: Reserved 11: Reserved
GPIOSUS[0]	I/O CMOS3.3	SUS	**DDR3 Memory Device Data Width:** When DDR3 SDRAM components are soldered directly to the platform board, this input function-strapping signal must indicate the data width of the DDR3 SDRAM components used: 0 = x16 DDR3 SDRAM components 1 = x8 DDR3 SDRAM components ***Note:*** Not used if DIMMs are used for DDR3 memory.
GPIOSUS[6:5]	I/O CMOS3.3	SUS	**DDR3 Memory Device Bit Density:** When DDR3 SDRAM components are soldered directly to the platform board, this input function-strapping signal must indicate the bit density of the DDR3 SDRAM components used: [6:5] 11: Reserved 10: 4Gbit DDR3 SDRAM components 01: 2Gbit DDR3 SDRAM components 00: 1Gbit DDR3 SDRAM components ***Note:*** Not used if DIMMs are used for DDR3 memory.

Table 6-2. System Memory Signals (Sheet 3 of 3)

Signal	Direction/ Type	Power Well	Description
GPIOSUS[8]	I/O CMOS3.3	SUS	**DDR3 Memory Device Number of Ranks:** When DDR3 SDRAM components are soldered directly to the platform board, this input function-strapping signal must indicate the number of ranks of the DDR3 SDRAM components used: 0 = Two ranks 1 = One rank ***Note:*** Not used if DIMMs are used for DDR3 memory.
SMBH_CLK	I/O CMOS3.3_ OD	CORE	**SMBus 1.0 Clock:** Open Drain. Clock for the dedicated SMBus 1.0 interface to the Serial Presence Detect (SPD) and Thermal Sensors on the DIMMs.
SMBH_DATA	I/O CMOS3.3_ OD	CORE	**SMBus 1.0 Data:** Open Drain. Data for the dedicated SMBus 1.0 interface to the Serial Presence Detect (SPD) and Thermal Sensors on the DIMMs.

6.2 PCI Express Root Port Signals

Table 6-3. PCI Express Root Port Unit 0 Signals

Signal	Direction/ Type	Power Well	Description
RP0_PETP[7:0] RP0_PETN[7:0]	I/O PCIe Gen 2		**PCI Express Transmit:** Differential-pair output. 2.5GT/s and 5.0 GT/s data rates supported.
RP0_PERP[7:0] RP0_PERN[7:0]	I/O PCIe Gen 2		**PCI Express Receive:** Differential-pair input. 2.5GT/s and 5.0GT/s data rates supported.
RP0_RCOMP	I PCIE Gen 2		**R-Comp:** Input driven by the platform board by a precision resistor tied to the analog voltage supply (VCCARP0_1P5). This input is used as the voltage-sampling path between output resistors and internal comparators. This resistor cannot be shared with or connected to any other PCI Express interface unit. Recommended resistor value: • 10.5KΩs for 1.8V analog supply. • 7.5KΩs for a 1.5V analog supply.
RP0_CLKINP RP0_CLKINN	I PCIE Gen 2		**PCI Express Reference Clock:** Differential-pair input. 100MHz.
TESTHI_1P05	I CMOS1.05		**Reserved:** Pull-up to 1.05V via a 10K-ohm resistor.

6.3 Low Pin Count (LPC) Signals

Table 6-4. LPC Interface Signals

Signal Name	Direction/ Type	Power Well	Description
LPC_AD[3:0]	I/O CMOS3.3	CORE	**LPC Address/Data:** Multiplexed Command, Address, Data.
LPC_FRAME_B	O CMOS3.3	CORE	**LPC Frame:** (active low) Output signal that indicates the start of an LPC cycle or an abort. ***Note:*** The LPC controller does not implement DMA or bus mastering cycles.
LPC_SERIRQ	I/O CMOS3.3	CORE	**Serial Interrupt Request:** Bi-directional signal that conveys the serial interrupt protocol.
LPC_CLKRUN_B	I/O CMOS3.3	CORE	**Clock Run:** (active low) Bi-directional signal that gates the operation of the LPC_CLKOUTx. Once an interrupt sequence has started, LPC_CLKRUN_B should remain asserted to allow the LPC_CLKOUTx to run.
LPC_CLKOUT[1:0]	O CMOS3.3	CORE	**LPC Clock:** These signals are the clocks driven by the processor to LPC devices. Each clock can support up to two loads. ***Note:*** If the primary boot device is connected via the LPC interface, it should use LPC_CLKOUT[0]. ***Note:*** Using the LPC interface for the boot device is not supported at this time and may not ever be supported by this Intel product. Only use the SPI interface for boot device connection.
LPCCLK0_DS	I	RTC	**LPC Clock 0 Drive Strength:** (active high) Input function-strapping signal. LPC clock 0 drive strength is defined by two 10-bit fields (PSTR and NSTR) in the LPC CLK0 IO Drive Strength Control register (LPCCLK0DS). This bit modifies the default drive-strength values for higher or lower LPC Clock 0 (LPC_CLKOUT0) drive strength. The PSTR field controls the drive high strength and the NSTR controls the drive low strength. The 10-bit default values are assigned as follows: 0 = Low drive strength, one clock load. PSTR = 1Fh and NSTR = 0Fh. 1 = High drive strength, two clock loads. PSTR = 3Fh and NSTR = 1Fh.

Note: The optional LPC interface signal named LSMI# is not provided and is only needed if a peripheral wants to cause an SMI# on an I/O instruction for retry. Alternately, the peripheral can use SMI# via the LPC_SERIRQ interface. The LSMI# can also be implemented by connecting it to any of the SMI-capable GPIO input signals.

6.4 SMBus 2.0 Signals

Table 6-5. SMBus Interface Signals

Signal Name	Direction/ Type	Power Well	Description
SMBD_CLK	I/O CMOS3.3_ OD	CORE	**SMBus 2.0 Clock:** Open Drain. Clock for the SMBus 2.0 interface for system management of the mass-storage drives.
SMBD_DATA	I/O CMOS3.3_ OD	CORE	**SMBus 2.0 Data:** Open Drain. Data for the SMBus 2.0 interface for system management of the mass-storage drives.
SMBM_CLK	I/O CMOS3.3_ OD	CORE	**SMBus 2.0 Clock:** Open Drain. Clock for the SMBus 2.0 interface for system management of the system enclosure.
SMBM_DATA	I/O CMOS3.3_ OD	CORE	**SMBus 2.0 Data:** Open Drain. Data for the SMBus 2.0 interface for system management of the system enclosure.

6.5 SPI and Flash Memory Signals

Serial Peripheral Interface (SPI). Used to interface with SPI Serial Flash memory devices.

Table 6-6. SPI Interface Signals

Signal Name	Direction/ Type	Power Well	Description
BOOTDEVSEL	I/O CMOS3.3	CORE	**Boot Device Select:** Input function-strapping signal. 0 = Boot from SPI Serial Flash Memory Component. 1 = Boot from Low Pin Count (LPC) interface. ***Note:*** This function-strapping signal is actually the GPIOCORE[0] signal pin.
SPI_MOSI	O CMOS3.3	CORE	**SPI Data Output:** Master Output (Slave Input) data for the SPI. Used to interface with SPI Serial Flash memory devices.
SPI_MISO	I CMOS3.3	CORE	**SPI Data Input:** Master Input (Slave Output) data for the SPI. Used to interface with SPI Serial Flash memory devices.
SPI_CSB[1:0]	O CMOS3.3	CORE	**SPI Chip Select Signal:** (active low) Bidirectional. When asserted, the slave SPI peripheral is selected.
SPI_SCLK	O CMOS3.3	CORE	**SPI Clock Output:** SPI clock accompanying data.

6.6 Reset, RTC and Power Management Signals

Table 6-7. Reset, RTC and Power Management Interface Signals (Sheet 1 of 2)

Signal Name	Direction/ Type	Power Well	Description
RESETB	I CMOS3.3	SUS	**System Reset:** (active low) The Hard Reset input driven by the External Circuitry. When asserted, the processor immediately initializes and returns to its default state. Once de-asserted, the core is released from reset.
PWROK	I CMOS3.3	RTC	**Power OK:** (active high) Input asserted by the External Circuitry (EC) to indicate on that the power supplied to the core is stable. PWROK can be driven asynchronously.The EC typically uses PWROK to produce the PERST# signal on the PCI Express interfaces. ***Note:*** The power associated with the PCI Express circuitry needs to be valid for at least 99 ms prior to PWROK assertion in order to comply with the PCI Express 100-ms requirement for RESETB de-assertion.
EPWRGOOD	I CMOS1.05	CORE	**Early Power Good:** (active high) Input. Reserved. Must be terminated with a 1.0KΩ 5% pull-down resistor tied to VSS on the platform board.
RSMRSTB	I CMOS3.3	RTC	**Resume Well Reset:** (active low) Input asserted by the External Circuitry (EC) to reset the registers and components in the SUS power well. An external RC circuit is required to ensure that the SUS power well voltage is valid prior to the de-assertion of the RSMRSTB signal.
RTCRESETB	I CMOS3.3	RTC	**RTC Well Reset:** (active low) Input normally pulled high on the platform board to the RTC 3.3V power source VCCRTC3P3. Can be driven low with external circuitry to test the RTC power well and reset certain register bits its in the RTC power-well registers that are not reset by the Resume Well Reset signal RSMRSTB. Unless entering a test mode, the RSMRSTB input must always be inactive (high) when all other non-RTC power planes are on. In order for the processor to detect when a new coin-battery has been installed, an external RC circuit can be connected to the RTCRESETB input signal. The RC circuit must be designed to create a time delay long enough so that RTCRESETB de-asserts (goes high) after the coin-battery voltage is valid. ***Note:*** The RC time delay needs to be in the 10- to 20-ms range to allow the processor to detect this condition.
RTC_EXTPAD	I/O Analog	RTC	**Real Time Clock External Pad:** Requires connection to 0.1µF capacitor connected to VSS on platform board.
RTC_X1PAD RTC_X2PAD	I/O Analog	RTC	**Real Time Clock Crystal:** Connections for an external 32.768kHz crystal and associated circuitry.
RTC_INTVRMEN	I CMOS3.3	RTC	**RTC Internal VRM Enable:** (active high) Enables the internal 1.05V and 1.5V regulators of the RTC. Must be pulled-up to VCCRTC3P3 with an external 4.7k resistor.
RTC_SRTCRSTB	I CMOS3.3	RTC	**RTC Well Secondary Reset:** Unused, active-low input pin. The platform board must tie this pin high with a 4.7 KΩ pull-up resistor to P3V3_RTC.
SUSCLK	O CMOS3.3	SUS	**Suspend Clock:** Output signal of the integrated Real-Time Clock oscillator (32.768kHz). The SUSCLK output signal has a duty cycle ranging from 30% to 70%.

Table 6-7. Reset, RTC and Power Management Interface Signals (Sheet 2 of 2)

Signal Name	Direction/ Type	Power Well	Description
WAKE_B	I CMOS3.3_ OD	SUS	**PCI Express* Wake-up Event:** (active low) Open-Drain input signal that is asserted by a PCI Express* port indicating it wants to wake-up the system. This is a single signal, named WAKE# by the PCI Express specification, that can be driven by any of the PCI Express devices implemented on the platform board. The device indicating the wake-up drives this signal low.
RSTWARN	I CMOS3.3	SUS	**Reset Warning:** (active high) Input asserted by the External Circuitry (EC) to indicate that a reset is needed and causes the processor to quiescent activity in preparation for a reset or entering a sleep state. A system management controller might do so after an external event, such as pressing of the power button or occurrence of a thermal event.
SLPMODE	O CMOS3.3	SUS	**Sleep Mode:** (active high) Output signal sent to the External Circuitry indicating the sleep state that needs to be entered. It is qualified with the active-low SLPRDYB output signal. When SLPMODE is high, entry into the S3 Sleep State is indicated. When SLPMODE is low, entry into the S4/S5 Sleep State is indicated.
SLPRDYB	O CMOS3.3	SUS	**Sleep Ready:** (active low) Output signal asserted to the External Circuitry indicating the system is ready to enter the sleep state indicated by the SLPMODE signal. De-assertion (the transition to the high state) of this output signal indicates that a wake-up has been requested by a system device.
RSTRDYB	O CMOS3.3	SUS	**Reset Ready:** (active low) Output signal asserted to the External Circuitry (EC) indicating the system is ready to be reset by the EC-driven RESETB input signal.
PUNIT_ST_ADDR[1:0]	I CMOS1.05	CORE	**P-Unit Firmware Starting Address Strap:** Input strapping identifying the 32-bit starting address of the 2KB block of the integrated Power Management Unit (P-Unit) controller firmware located in the SPI Flash Memory device.For using reference BIOS the pins can just be strapped to '00'. [1:0] 00 = FFFB_0000 01 = FFFC_0000 10 = FFFE_0000 11 = FFFD_0000
SVID_CLK	O CMOS1.05_ OD	CORE	**Serial Voltage Identification (sVID) Clock:** Source-synchronous output, used by the External Circuitry (EC) to qualify SVID_DATA. Has 20KΩ internal pull-up resistor. Requires external 55Ω resistor tied to 1.05V.
SVID_DATA	I/O CMOS1.05_ OD	CORE	**sVID Data:** Bi-Directional signal. Used by the processor and the EC to transmit serial data to each other. Has 20KΩ internal pull-up resistor. Requires external 55Ω resistor tied to 1.05V.
SVID_ALERT_B	I CMOS1.05	CORE	**sVID Alert:** (active low) Input signal driven asynchronously by the EC to indicate to the processor that the VR status register needs to be read.Has 20KΩ internal pull-up resistor. Requires external 55Ω resistor tied to 1.05V.

6.7 JTAG and Debug Signals

The JTAG interface is accessible only after the active-high PWROK input signal is asserted.

Table 6-8. JTAG and Debug Interface Signals (Sheet 1 of 2)

Signal Name	Direction/ Type	Power Well	Description
PSMI_VISA[29:0]	I/O CMOS1.05	Core	Reserved
DFX_GPIO_GRP0[7:0]	I/O CMOS1.8	Core	**DFx Group 0:** Design-For-Debug (also Test, Manufacture, and Validation) group of general-purpose I/O pins shared across various modes.
DFX_GPIO_GRP1[7:0]	I/O CMOS1.8 CMOS, bit[6] is OD	Core	**DFx Group 1:** Design-For-Debug (also Test, Manufacture, and Validation) group of general-purpose I/O pins shared across various modes. DFX_GPIO_GRP1[6] is CMOS OD.
HVMGEAR_SEL	I CMOS1.05	CORE	**High-Volume Manufacturing (HVM) Gear Select:** (active high) Must be pulled-down to a logic low on the platform board.
CPU_PREQB	I CMOS1.05	CORE	**CPU Probe Mode Request:** (active low) Input signal to request the CPU to enter Probe Mode. Platform board must connect to a 56Ω resistor tied to VCC.
CPU_PRDYB	O CMOS1.05_ OD	CORE	**CPU Probe Mode Ready:** (active low) Open-drain output signal indicating that the CPU is in Probe Mode as a response to a CPU Probe Mode Request.
CPU0_HFPLL	O CMOS1.05	CORE	**CPU 0 High Frequency Debug:** Output. For debug purposes. Can be routed to debug pad on platform board.
CPU1_HFPLL	O CMOS1.05	CORE	**CPU 1 High Frequency Debug:** Output. For debug purposes. Can be routed to debug pad on platform board.
CPU0_SFRANAD	O Analog1.8	CORE	**CPU 0 Super Filter Regulator (SFR):** Analog output. For debug purposes. Can be routed to debug pad on platform board.
CPU1_SFRANAD	O Analog1.8	CORE	**CPU 1 Super Filter Regulator (SFR):** Analog output. For debug purposes. Can be routed to debug pad on platform board.
HPLL_MONP HPLL_MONN	I/O CMOS		**Host PLL Monitor:** Differential-pair output. For debug and test purposes.
DDR3_MON1P DDR3_MON1N	O CMOS		**DDR3 Memory PLL Monitor 1:** Differential-pair output. For debug and test purposes.
DDR3_MON2P DDR3_MON2N	O CMOS		**DDR3 Memory PLL Monitor 2:** Differential-pair output. For debug and test purposes.
RP0_PLLMON0	I/O PCIE Gen 2		**PCI Express* Root Port Unit 0 PLL Monitor 0:** Bidirectional. For debug and test purposes.
RP0_PLLMON1	I/O PCIE Gen 2		**PCI Express Root Port Unit 0 PLL Monitor 1:** Bidirectional. For debug and test purposes
CPU_EXTBGREF	I Analog 1.8V	Core	**CPU External Bandgap Reference:** Analog input signal used as a reference voltage for debugging the host DLL and thermal sensors.
SOC_THERMANATP[1:0]	I/O Analog1.5		**SoC Thermal Management Tap:** Two bi-directional analog signals. Used as a 2-bit test port.
EDM			**Edge Die Monitor:** Reserved for Intel Use. Make no platform-board connection to this signal pin.
RSVD_MVT[1:0]	I/O CMOS1.8	Core	**Reserved for Future Use.** Make no platform-board connections to these signal pins.

Table 6-8. JTAG and Debug Interface Signals (Sheet 2 of 2)

Signal Name	Direction/ Type	Power Well	Description
JTA_POWEROK	I CMOS1.05	Core	**JTAG Power OK:** input signal that initializes the JTAG functions and circuitry.
SOC_TDI	I CMOS1.05	Core	**JTAG Test Data In (TDI):** Input serial data conforming to the JTAG specification.
SOC_TDO	I/O CMOS1.05_ OD	Core	**JTAG Test Data Out (TDO):** Open-drain. Output serial data conforming to the JTAG specification.
SOC_TMS	I CMOS1.05	Core	**JTAG Test Mode Select (TMS):** (active high) Input used to select the JTAG mode conforming to the JTAG specification.
SOC_TCK	I CMOS1.05	Core	**JTAG Test Clock (TCK):** Input used as the data/mode clock conforming to the JTAG specification.
SOC_TRSTB	I CMOS1.05	Core	**JTAG Test Reset:** (active low) Input that asynchronously resets the Test Access Port (TAP) logic. It must be asserted (driven low) by the platform board during Power-On Reset.

6.8 Thermal Management Signals

Table 6-9. Thermal Management Signals

Signal Name	Direction/ Type	Power Well	Description
CPU_PROCHOTB	I/O CMOS1.05_ OD	Core	**Processor Hot:** (active low) Bi-directional signal. Driven by the processor when it has reached its maximum operating temperature. Driven by the External Circuitry or external source to activate the processor's Thermal Control Circuitry (TCC). Doing this is a way to use the TCC to provide thermal protection for other system components.
CPU0_THERMDA CPU1_THERMDA	I Analog	Core	**CPU[1:0] Thermal Diode Anode:** The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal "diode", with its collector shorted to ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a standalone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached.
CPU0_THERMDC CPU1_THERMDC	O Analog		**CPU[1:0] Thermal Diode Cathode:** The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal "diode", with its collector shorted to ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached.
SOC_THERMDA SOC_THERMDC	I/O Analog 1.5V		**Thermal Diode:** The anode (SOC_THERMDA) and cathode SOC_THERMDC) of the component's thermal diode.
SOC_THERMREFNPAD	I/O Analog 1.5V	Core	**SOC Thermal Reference Pad:** Platform board must connect this pin to an 8KΩ resistor to ground.
THRMB	I CMOS3.3	Core	**Thermal Alarm:** (active low) Input signal driven by the External Circuitry to generate a thermal-related SMI or SCI.
THRMTRIPB	O CMOS1.05_ OD	CORE	**Thermal Trip:** (active low) Output signal indicating that a catastrophic overheating condition has been sensed by the internal thermal sensor. To prevent false trips, this sensor is set well above the normal operating temperature. The processor stops all execution when the junction temperature exceeds approximately 125°C.

6.9 High-Speed UART Signals

Table 6-10. High-Speed UART Signals

Signal Name	Direction/ Type	Power Well	Description
UART_CTS_N	I CMOS3.3	CORE	**UART Clear to Send:** (active low) Input.
UART_DCD_N	I CMOS3.3	CORE	**UART Data Carrier Detect:** (active low) Input.
UART_DSR_N	I CMOS3.3	CORE	**UART Data Set Ready:** (active low) Input.
UART_DTR_N	O CMOS3.3	CORE	**UART Data Terminal Ready:** (active low) Output.
UART_RI_N	I CMOS3.3	CORE	**UART Ring Indicator:** (active low) Input.
UART_RTS_N	O CMOS3.3	CORE	**UART Request to Send:** (active low) Output.
UART_RXD	I CMOS3.3	CORE	**UART Receive Data:** Input.
UART_TXD	O CMOS3.3	CORE	**UART Transmit:** Output.

6.10 General-Purpose I/O Signals

Table 6-11. General-Purpose I/O Signals

Signal Name	Direction/ Type	Power Well	Description
GPIOCORE[4:1]	I/O CMOS3.3	Core	**General-Purpose I/O Ports:** Available for platform board design.
GPIOCORE[20:5]	I/O CMOS3.3	Core	For Software and Platform Board Design GPIO usage.
GPIOSUS[4:1]	I/O CMOS3.3	SUS	**General-Purpose I/O Ports:** Available for platform board design.
GPIOSUS[7]	I/O CMOS3.3	SUS	**General-Purpose I/O Ports:** Available for platform board design.
GPIOSUS[8, 6, 5, 0]	I/O CMOS3.3	SUS	**General-Purpose I/O Ports:** See note below.

6.11 Speaker, WDT and HPET Signals

Table 6-12. Speaker, WDT and HPET Signals

Signal Name	Direction/ Type	Power Well	Description
SPKR	O CMOS3.3	CORE	**Speaker:** Output signal for implementing a PC-compatible speaker on the platform board. If enabled by software, the SPKR output is equivalent to the Counter 2 OUT signal value of the integrated 8254 Programmable Interval Timer (PIT).
OWDTOUT	I/O CMOS1.05	CORE	**Watch Dog Timer (WDT) Output:** (active high) Output signal indicating that the integrated Watch Dog Timer has timed out. If enabled by software, this signal, when asserted, indicates that the system has possibly become unstable.
HPET_CLK14IN	I CMOS3.3	CORE	**High-Precision Event Timer (HPET) Clock:** Input clock provided by the External Circuitry. 14.31838MHz, single ended, non-spread spectrum.

6.12 Processor Clock and Error Signals

Table 6-13. Processor Clock and Error Signals

Signal Name	Direction/ Type	Power Well	Description
HPLL_CLKREFP HPLL_CLKREFN	I CMOS1.5	CORE	**Host Clock Reference:** Differential-pair input. Used to provide clocking to the CPUs, integrated Memory Controller, and most of the integrated Legacy Devices. 100MHz.
CPU_IERR	I/O CMOS1.05	CORE	**CPU Internal Error:**
ERR[2:0]	O CMOS3.3	CORE	**Error Class:** (active high) Open-drain output signals provided for the External Circuitry. Reports the following Error Classes: ERR[2] - Fatal Errors ERR[1] - Non-Fatal Errors ERR[0] - Correctable Errors

6.13 Buffer Compensation Control Signals

Table 6-14. Buffer Compensation Control Signals

Signal Name	Direction/ Type	Power Well	Description
HV_GPIO_RCOMP	I/O		Attach to 50 ohm resistor.
MV_GPIO_RCOMP	I/O		Attach to 50 ohm resistor.
LV_GPIO_RCOMP	I/O		Attach to 50 ohm resistor.

6.14 Power and Ground Signals

Table 6-15. Power and Ground Signals (Sheet 1 of 2)

Signal Name	Voltage (Volts)	Power Well	Description
NC	n/a	n/a	**No Connect:** Platform board must make no connection to these balls/pins.
VSS	0	All	**Power supply voltage return:** Connect to ground.
VSS_NCTF	0	All	**VSS Non-Critical to Function (NCTF):** Connect to VSS on platform board design. ***Note:*** NCTF locations are typically redundant ground or noncritical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
VCC	1.05	Core	**Core 1.05V Supply**: For CPU 0, CPU 1, and associated circuitry.
VCCA_DDR3_1P05	1.05		DDR3 Clock quiet digital power supply
VCCACLK_DDR3_1P05	1.05		DDR3 digital power supply
VCCADLL_DDR3_1P05	1.05		DDR3 DLL quiet digital supply
VCCCPU0VIDSI01P05	1.05		
VCCFHVCPU0SI01P05	1.05		**Reserved for Intel Use:** This pin must be connected to 1.05V on the platform board.
VCCFHVCPU1SI01P05	1.05		**Reserved for Intel Use:** This pin must be connected to 1.05V on the platform board.
VCCDHPLL1P05	1.05		Host Digital Clock 1.05V Supply:
VCCFHVSOC1P05	1.05		**Reserved for Intel Use:** This pin must be connected to 1.05V on the platform board.
VCCPLL_DDR3_1P05	1.05		
VCCPLLCPU0SI01P05	1.05		
VCCPLLCPU1SI01P05	1.05		Keep separate from CPU0 for independent LC filter on board.
VCCRAMCPU0XSI01P05	1.05		
VCCSUS1P05	1.05	SUS	Suspend (SUS) Power Well 1.05V supply:
VCC_DDR3_1P5	1.5		DDR3 I/O power supply
VCCARP0_1P5	1.5		PCI Express Port - 1.8V/1.5V analog power supply.
VCCATS1P5	1.5		Separate high voltage power supply.
VCCCLK_DDR3_1P5	1.5		DDR3 Clock quiet I/O power supply
VCCREFRP0_1P5	1.5		PCI Express Port - Connect externally to the 1.5V supply. Needed to create voltage references.
VCCSFRPLL_DDR3_1P5	1.5		**SFRANAD:** SFR (Super Filter Regulator) analog output for debugging.
VCCABGTS1P8	1.8		Bandgap supply.
VCCAGPIO1P8	1.8		General Purpose I/O (GPIO) 1.8V supply:
VCCASFRHPLL1P8	1.8		**SFR:** Super Filter Regulator analog output for debugging.
VCCSUS1P8	1.8	SUS	Suspend (SUS) Power Well 1.8V supply:
VCCAGPIO3P3	3.3		General Purpose I/O (GPIO) 3.3V supply:
VCCRTC3P3	3.3	RTC	**Real-Time Clock (RTC) Power Well 3.3V supply:** Battery voltage input.

Table 6-15. Power and Ground Signals (Sheet 2 of 2)

Signal Name	Voltage (Volts)	Power Well	Description
VCCSUS3P3	3.3	SUS	Suspend (SUS) Power Well 3.3V supply:
VCCCPU0SENSE VSSCPU0SENSE	O CMOS1.05		**CPU 0 and CPU 1 Vcc Sense:** Differential-pair output. Used by the External Circuitry (EC) to sense the 1.05V power of the core CPU circuitry.
VCCCPU0VIDSI0GT1P05	Output		Output pins MUST NOT connect to 1.05V supply on platform. Route to a test point.
VCCCPU1VIDSI0GT1P05	Output		Output pins MUST NOT connect to 1.05V supply on platform. Route to a test point.
TESTHI_1P5_00	1.5		Connect externally to the 1.5V supply. Needed to create voltage references.
TESTHI_1P5_01	1.5		Connect externally to the 1.5V supply. Needed to create voltage references.
TESTHI_1P5_02	1.5		Connect externally to the 1.5V supply. Needed to create voltage references.
TESTHI_1P5_03	1.5		Connect externally to the 1.5V supply. Needed to create voltage references.
TESTHI_1P5_04	1.5		Connect externally to the 1.5V supply. Needed to create voltage references.
TESTHI_1P5_05	1.5		Connect externally to the 1.5V supply. Needed to create voltage references.
TESTHI_1P05	1.05		Connect to 1.05V supply.
TESTLO_00	GND		Pull down to ground.
TESTLO_01	GND		Pull down to ground.
TESTLO_02	GND		Pull down to ground.
TESTLO_03	GND		Pull down to ground.
TESTLO_04	GND		Pull down to ground.
TESTLO_05	GND		Pull down to ground.
TESTLO_06	GND		Pull down to ground.
TESTLO_07	GND		Pull down to ground.
TESTLO_08	GND		Pull down to ground.
TESTLO_09	GND		Pull down to ground.
TESTLO_10	GND		Pull down to ground.
TESTLO_11	GND		Pull down to ground.
TESTLO_12	GND		Pull down to ground.
TESTLO_13	GND		Pull down to ground.
TESTLO_14	GND		Pull down to ground.
TESTLO_15	GND		Pull down to ground.
TESTLO_16	GND		Pull down to ground.
TESTLO_17	GND		Pull down to ground.

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7 Electrical Specifications

7.1 Supply Operational Voltage Requirements

The operational voltage requirements in Table 7-1.

At conditions outside the operational condition limits, but within absolute maximum and minimum ratings, neither correct function nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but its lifetime may be degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither proper operation nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, it will either not function or its reliability will be severely degraded when returned to conditions within the functional operating condition limits.

Even though the component contains protective circuitry to resist damage from Electrostatic Discharge (ESD), precautions should always be taken to avoid high static voltages and high electric fields.

Table 7-1. Voltage Source Operational Requirements (Sheet 1 of 2)

Voltage-Supply Ball Name	Parameter	Min.	Typical	Max.	Units	Notes
1.05V Processor VID Rail (Min/Max: +/- 5%)						
VCCCPU0VIDSI01P05	1.05	0.997	1.05	1.102	V	
1.05V Power Sources (Min/Max: +/- 5%)						
VCC	SoC Power Voltage Range	0.997	1.05	1.102	V	
VCCSUS1P05	1.05V SUS Power Well Voltage Range	0.997	1.05	1.102	V	
VCCDHPLL1P05	Host Digital Clock Supply Voltage Range	0.997	1.05	1.102	V	
VCCPLL_DDR3_1P05	1.05	0.997	1.05	1.102	V	
VCCRAMCPU0XSI01P05	1.05	0.997	1.05	1.102	V	
VCCPLLCPU0SI01P05	1.05	0.997	1.05	1.102	V	
VCCPLLCPU1SI01P05	1.05	0.997	1.05	1.102	V	
VCCCPU0VIDSI01P05	1.05	0.997	1.05	1.102	V	
VCCFHVCPU0SI01P05 VCCFHVCPU1SI01P05	Reserved for Intel Use Supply Voltage Range	0.997	1.05	1.102	V	
VCCA_DDR3_1P05	1.05	0.997	1.05	1.102	V	
VCCACLK_DDR3_1P05	1.05	0.997	1.05	1.102	V	
VCCADLL_DDR3_1P05	1.05	0.997	1.05	1.102	V	
VCCFHVSOC1P05	1.05	0.997	1.05	1.102	V	
VCCANTB_1P05	PCI Express 1.05V Analog Power	0.997	1.05	1.102	V	

Table 7-1. Voltage Source Operational Requirements (Sheet 2 of 2)

Voltage-Supply Ball Name	Parameter	Min.	Typical	Max.	Units	Notes
TESTHI_1P05	1.05V Analog Supply Voltage Range	0.997	1.05	1.102	V	
1.5V Power Sources (Min/Max: +/- 5% OR +/- 4.5%)						
VCCATS1P5	1.5	1.425	1.5	1.575	V	
PCI Express* Analog[1]	1.5V Analog Supply Voltage Range	1.425	1.5	1.575	V	
PCI Express Reference[2]	1.5V Reference Voltage Range	1.432	1.5	1.567	V	
VCC_DDR3_1P5	1.5	1.425	1.5	1.575	V	
VCC_DDR3_1P5 (DDR3-L)	1.5	1.432	1.5	1.567	V	
VCC_DDR3_1P5	DDR IO Power Supply (1.5V)	1.425	1.5	1.575	V	
VCC_DDR3_1P5 (DDR3-L)	DDR IO Power Supply (1.35V)	1.432	1.5	1.567	V	
VCCSFRPLL_DDR3_1P5	1.5	1.425	1.5	1.575	V	
1.8V Power Sources (Min/Max: +/- 5%)						
VCCAGPIO1P8	1.8V Voltage Range	1.710	1.8	1.890	V	
VCCSUS1P8	1.8V SUS Power Well Voltage Range	1.710	1.8	1.890	V	
VCCASFRHPLL1P8	1.5V Analog SFR Voltage Range	1.710	1.8	1.890	V	
VCCABGTS1P8	Bandgap Supply Voltage Range	1.710	1.8	1.890	V	
3.3V Power Sources						
VCCAGPIO3P3	3.3V Voltage Range	3.135	3.3	3.465	V	
VCCSUS3P3	3.3V SUS Power Well Voltage Range	3.135	3.3	3.465	V	
VCCRTC3P3	3.3V RTC Power Well Voltage Range		3.0		V	

Notes:
1. Includes power source pins VCCAxxx_1P5 used for PCI Express analog interface power.
2. Includes voltage reference pins VCCREFxxx_1P5.

7.2 DC Power Characteristics

The values in Table 7-2 are all measurements from parameter characterization of the silicon.

Table 7-2. Power Well Information

Power Well	Voltage Rail
CORE	VCCCPU0VIDSI01P05, VCC,VCCDHPLL1P05, VCCPLL_DDR3_1P05, VCCRAMCPU0XSI01P05, VCCPLLCPU0SI01P05, VCCPLLCPU1SI01P05, VCCFHVCPU0SI01P05, VCCFHVCPU1SI01P05, VCCA_DDR3_1P05, VCCACLK_DDR3_1P05, VCCADLL_DDR3_1P05, VCCFHVSOC1P05, VCCANTB_1P05, TESTHI_1P05, VCCATS1P5, PCI Express* Analog[1], PCI Express Reference[2], VCCAGPIO1P8, VCCASFRHPLL1P8, VCCABGTS1P8, VCCAGPIO3P3,
SUS	VCCSUS1P05, VCC_DDR3_1P5, VCCCLK_DDR3_1P5, VCCSFRPLL_DDR3_1P5, VCCSUS1P8, VCCSUS3P3
RTC	VCCRTC3P3

Table 7-3. Intel® Atom™ Processor S1240 SKU (1.5V DDR3): Voltage Source DC Characteristics (TDP@Tj=102C and MAX@Tj=102C)

Voltage Rail	Voltage	I_{TDP} (mA)	P_{TDP} (mW)	V_{MAX}(V)	I_{MAX} (mA)	P_{MAX} (mW)
1.05V Processor VID Rail						
VCCCPU0VIDSI01P05	1.01	1942.55	1958.23	1.15	3390.33	3898.87
1.05V Power Sources						
VCC	1.05	1550.09	1627.59	1.15	1786.99	2055.04
VCCSUS1P05	1.05	0.34	0.36	1.15	0.37	0.43
VCCDHPLL1P05	1.05	2.03	2.13	1.15	2.22	2.56
VCCPLL_DDR3_1P05	1.05	9.94	10.43	1.15	10.88	12.51
VCCRAMCPU0XSI01P05	1.05	75.13	78.89	1.15	82.29	94.63
VCCRAMCPU1XSI01P05	1.05	75.13	78.89	1.15	82.29	94.63
VCCPLLCPU0SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCPLLCPU1SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCFHVCPU0SI01P05	1.05	0	0	1.15	0	0
VCCFHVCPU1SI01P05	1.05	0	0	1.15	0	0
VCCA_DDR3_1P05	1.05	353.19	370.85	1.15	390.68	449.29
VCCACLK_DDR3_1P05	1.05	9.94	10.43	1.15	10.88	12.51
VCCADLL_DDR3_1P05	1.05	113.36	119.03	1.15	115.87	133.25
VCCFHVSOC1P05	1.05	16.13	16.94	1.15	17.67	20.32
VCCANTB_1P05	1.05	861.34	904.4	1.15	990.54	1139.12
TESTHI_1P05	1.05	0	0	1.15	0	0
1.5V Power Sources						
VCCATS1P5	1.5	2.27	3.4	1.575	2.38	3.75
PCI Express* Analog[1]	1.5	20.98	31.47	1.575	22.04	34.71
PCI Express Reference[2]	1.5	0.12	0.19	1.575	0.14	0.22
VCC_DDR3_1P5	1.5	513.18	769.77	1.575	777.47	1224.52
VCCCLK_DDR3_1P5	1.5	60.51	90.76	1.575	69.02	108.71
VCCSFRPLL_DDR3_1P5	1.5	26.43	39.64	1.575	30.15	47.49
TESTHI_1P5	1.5	1.56	2.34	1.575	1.71	2.69
1.8V Power Sources						
VCCAGPIO1P8	1.8	2.86	5.15	1.89	3	5.67
VCCSUS1P8	1.8	0.65	1.17	1.89	0.68	1.29
VCCASFRHPLL1P8	1.8	17.4	31.32	1.89	18.27	34.53
VCCABGTS1P8	1.8	18.9	34.02	1.89	19.85	37.52
3.3V Power Sources						
VCCAGPIO3P3	3.3	25.03	82.59	3.465	26.28	91.05
VCCSUS3P3	3.3	4.03	13.3	3.465	4.23	14.66
VCCRTC3P3	3.3	0.1	0.33	3.465	0.11	0.36

Notes:

1. Includes power source pins VCCAxxx_1P5 used for PCI Express analog interface power. Includes voltage reference pins VCCREFxxx_1P5.

Table 7-4. Intel® Atom™ Processor S1240 SKU (1.35V DDR3-L): Voltage Source DC Characteristics (TDP@Tj=102C and MAX@Tj=102C)

Voltage Rail	Voltage	ITDP (mA)	PTDP (mW)	VMAX(V)	IMAX (mA)	PMAX (mW)
1.05V Processor VID Rail						
VCCCPU0VIDSI01P05	1.01	1942.57	1958.25	1.15	3390.33	3898.87
1.05V Power Sources						
VCC	1.05	1550.09	1627.59	1.15	1786.99	2055.04
VCCSUS1P05	1.05	0.34	0.36	1.15	0.37	0.43
VCCDHPLL1P05	1.05	2.03	2.13	1.15	2.22	2.56
VCCPLL_DDR3_1P05	1.05	8.74	9.18	1.15	9.58	11.01
VCCRAMCPU0XSI01P05	1.05	75.13	78.89	1.15	82.29	94.63
VCCRAMCPU1XSI01P05	1.05	75.13	78.89	1.15	82.29	94.63
VCCPLLCPU0SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCPLLCPU1SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCFHVCPU0SI01P05	1.05	0	0	1.15	0	0
VCCFHVCPU1SI01P05	1.05	0	0	1.15	0	0
VCCA_DDR3_1P05	1.05	310.81	326.35	1.15	390.68	449.29
VCCACLK_DDR3_1P05	1.05	8.74	9.18	1.15	9.58	11.01
VCCADLL_DDR3_1P05	1.05	99.76	104.74	1.15	115.87	133.25
VCCFHVSOC1P05	1.05	16.13	16.94	1.15	17.67	20.32
VCCANTB_1P05	1.05	861.34	904.4	1.15	990.54	1139.12
TESTHI_1P05	1.05	0	0	1.15	0	0
1.5V Power Sources						
VCCATS1P5	1.5	2.27	3.4	1.575	2.38	3.75
PCI Express* Analog[1]	1.5	20.98	31.47	1.575	22.03	34.7
PCI Express Reference[2]	1.5	0.12	0.19	1.575	0.13	0.2
VCC_DDR3_1P5	1.35	501.78	677.40	1.42	699.73	991.86
VCCCLK_DDR3_1P5	1.35	59.16	79.87	1.42	62.12	88.05
VCCSFRPLL_DDR3_1P5	1.5	23.06	34.59	1.575	26.31	41.43
TESTHI_1P5	1.5	1.56	2.34	1.575	1.64	2.58
1.8V Power Sources						
VCCAGPIO1P8	1.8	1.67	3.00	1.89	1.75	3.31
VCCSUS1P8	1.8	0.65	1.17	1.89	0.68	1.29
VCCASFRHPLL1P8	1.8	17.4	31.32	1.89	19.85	37.51
VCCABGTS1P8	1.8	18.9	34.02	1.89	19.85	37.51
3.3V Power Sources						
VCCAGPIO3P3	3.3	25.03	82.59	3.465	26.28	91.05
VCCSUS3P3	3.3	4.03	13.3	3.465	4.23	14.66
VCCRTC3P3	3.3	0.1	0.33	3.465	0.11	0.36

Notes:
1. Includes power source pins VCCAxxx_1P5 used for PCI Express analog interface power. Includes voltage reference pins VCCREFxxx_1P5.

Table 7-5. Intel® Atom™ Processor S1220 SKU (1.5V DDR3): Voltage Source DC Characteristics (TDP@Tj=95C and MAX@Tj=95C)

Voltage Rail	Voltage	I_{TDP} (mA)	P_{TDP} (mW)	V_{MAX}(V)	I_{MAX} (mA)	P_{MAX} (mW)
1.05V Processor VID Rail						
VCCCPU0VIDSI01P05	1.13	2012.27	2288.96	1.15	3118.62	3586.40
1.05V Power Sources						
VCC	1.05	2390.26	2509.78	1.15	2707.11	3113.17
VCCSUS1P05	1.05	0.34	0.36	1.15	0.37	0.43
VCCDHPLL1P05	1.05	2.03	2.13	1.15	2.22	2.56
VCCPLL_DDR3_1P05	1.05	16.92	17.76	1.15	18.53	21.31
VCCRAMCPU0XSI01P05	1.05	62.23	65.34	1.15	68.15	78.38
VCCRAMCPU1XSI01P05	1.05	62.23	65.34	1.15	68.15	78.38
VCCPLLCPU0SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCPLLCPU1SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCFHVCPU0SI01P05	1.05	0	0	1.15	0	0
VCCFHVCPU1SI01P05	1.05	0	0	1.15	0	0
VCCA_DDR3_1P05	1.05	402.36	422.48	1.15	448.81	516.13
VCCACLK_DDR3_1P05	1.05	12.47	13.09	1.15	13.65	15.7
VCCADLL_DDR3_1P05	1.05	131.69	138.27	1.15	133.87	153.95
VCCFHVSOC1P05	1.05	16.13	16.94	1.15	17.67	20.32
VCCANTB_1P05	1.05	1341.41	1408.48	1.15	1541.53	1772.76
TESTHI_1P05	1.05	0	0	1.15	0	0
1.5V Power Sources						
VCCATS1P5	1.5	2.27	3.4	1.575	2.38	3.75
PCI Express* Analog[1]	1.5	24.44	36.65	1.575	25.68	48.54
PCI Express Reference[2]	1.5	0.14	0.2	1.575	0.16	0.3
VCC_DDR3_1P5	1.5	536.69	805.03	1.575	817.62	1287.76
VCCCLK_DDR3_1P5	1.5	59.83	89.75	1.575	68.25	107.5
VCCSFRPLL_DDR3_1P5	1.5	26.43	39.64	1.575	30.15	47.49
TESTHI_1P5	1.5	3.18	4.77	1.575	3.47	6.57
1.8V Power Sources						
VCCAGPIO1P8	1.8	2.86	5.15	1.89	3	5.68
VCCSUS1P8	1.8	0.65	1.17	1.89	0.68	1.29
VCCASFRHPLL1P8	1.8	17.4	31.32	1.89	18.27	34.53
VCCABGTS1P8	1.8	18.9	34.02	1.89	19.85	37.51
3.3V Power Sources						
VCCAGPIO3P3	3.3	25.03	82.59	3.465	26.28	91.05
VCCSUS3P3	3.3	4.03	13.3	3.465	4.23	14.66
VCCRTC3P3	3.3	0.1	0.33	3.465	0.11	0.36

Notes:

1. Includes power source pins VCCAxxx_1P5 used for PCI Express analog interface power. Includes voltage reference pins VCCREFxxx_1P5.

Table 7-6. Intel® Atom™ Processor S1220 SKU (1.35V DDR3-L): Voltage Source DC Characteristics (TDP@Tj=95C and MAX@Tj=95C)

Voltage Rail	Voltage	ITDP (mA)	PTDP (mW)	VMAX(V)	IMAX (mA)	PMAX (mW)
1.05V Processor VID Rail						
VCCCPU0VIDSI01P05	1.13	2012.27	2288.96	1.15	3118.62	3586.40
1.05V Power Sources						
VCC	1.05	2390.26	2509.78	1.15	2707.11	3113.17
VCCSUS1P05	1.05	0.34	0.36	1.15	0.37	0.43
VCCDHPLL1P05	1.05	2.03	2.13	1.15	2.22	2.56
VCCPLL_DDR3_1P05	1.05	14.89	15.63	1.15	16.3	18.75
VCCRAMCPU0XSI01P05	1.05	62.23	65.34	1.15	68.15	78.38
VCCRAMCPU1XSI01P05	1.05	62.23	65.34	1.15	68.15	78.38
VCCPLLCPU0SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCPLLCPU1SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCFHVCPU0SI01P05	1.05	0	0	1.15	0	0
VCCFHVCPU1SI01P05	1.05	0	0	1.15	0	0
VCCA_DDR3_1P05	1.05	354.08	371.78	1.15	448.81	516.13
VCCACLK_DDR3_1P05	1.05	10.97	11.52	1.15	12.01	13.82
VCCADLL_DDR3_1P05	1.05	115.88	121.68	1.15	133.87	153.95
VCCFHVSOC1P05	1.05	16.13	16.94	1.15	17.67	20.32
VCCANTB_1P05	1.05	1341.41	1408.48	1.15	1541.53	1772.76
TESTHI_1P05	1.05	0	0	1.15	0	0
1.5V Power Sources						
VCCATS1P5	1.5	2.27	3.4	1.575	2.38	3.75
PCI Express* Analog[1]	1.5	24.44	36.65	1.575	25.68	40.45
PCI Express Reference[2]	1.5	0.14	0.2	1.575	0.16	0.25
VCC_DDR3_1P5	1.35	524.76	708.43	1.42	735.86	1043.08
VCCCLK_DDR3_1P5	1.35	58.50	78.98	1.42	61.43	87.07
VCCSFRPLL_DDR3_1P5	1.5	23.06	34.59	1.575	26.31	41.43
TESTHI_1P5	1.5	3.18	4.77	1.575	3.47	5.47
1.8V Power Sources						
VCCAGPIO1P8	1.8	1.67	3.0	1.89	1.75	3.31
VCCSUS1P8	1.8	0.65	1.17	1.89	0.68	1.29
VCCASFRHPLL1P8	1.8	17.4	31.32	1.89	18.27	34.53
VCCABGTS1P8	1.8	18.9	34.02	1.89	19.85	37.51
3.3V Power Sources						
VCCAGPIO3P3	3.3	25.03	82.59	3.465	26.28	91.05
VCCSUS3P3	3.3	4.03	13.3	3.465	4.23	14.66
VCCRTC3P3	3.3	0.1	0.33	3.465	0.11	0.36

Notes:
1. Includes power source pins VCCAxxx_1P5 used for PCI Express analog interface power. Includes voltage reference pins VCCREFxxx_1P5.

Table 7-7. Intel® Atom™ Processor S1260 SKU (1.5V DDR3) Voltage Source DC Characteristics (TDP@Tj=95C and MAX@Tj=95C)

Voltage Rail	Voltage	I_{TDP} (mA)	P_{TDP} (mW)	V_{MAX}(V)	I_{MAX} (mA)	P_{MAX} (mW)
1.05V Processor VID Rail						
VCCCPU0VIDSI01P05	1.13	3161.81	3463.41	1.15	4052.26	4660.10
1.05V Power Sources						
VCC	1.05	2031.99	2133.59	1.15	2375.51	2709.34
VCCSUS1P05	1.05	0.34	0.36	1.15	0.37	0.43
VCCDHPLL1P05	1.05	7.74	8.13	1.15	8.48	9.75
VCCPLL_DDR3_1P05	1.05	9.88	10.37	1.15	10.82	12.44
VCCRAMCPU0XSI01P05	1.05	65.02	68.28	1.15	71.22	81.90
VCCRAMCPU1XSI01P05	1.05	65.02	68.28	1.15	71.22	81.90
VCCPLLCPU0SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCPLLCPU1SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCFHVCPU0SI01P05	1.05	0	0	1.15	0	0
VCCFHVCPU1SI01P05	1.05	0	0	1.15	0	0
VCCA_DDR3_1P05	1.05	351.19	368.75	1.15	446.45	513.42
VCCACLK_DDR3_1P05	1.05	9.88	10.37	1.15	10.82	12.44
VCCADLL_DDR3_1P05	1.05	112.72	118.35	1.15	123.45	141.97
VCCFHVSOC1P05	1.05	21.85	22.94	1.15	23.93	27.52
VCCANTB_1P05	1.05	937.53	984.40	1.15	1043.28	1199.77
TESTHI_1P05	1.05	0	0	1.15	0	0
1.5V Power Sources						
VCCATS1P5	1.5	6.27	9.40	1.575	6.58	10.36
PCI Express* Analog[1]	1.5	27.65	41.47	1.575	29.03	45.72
PCI Express Reference[2]	1.5	6.79	10.19	1.575	7.13	11.23
VCC_DDR3_1P5	1.5	520.27	780.40	1.575	693.55	1092.34
VCCCLK_DDR3_1P5	1.5	70.16	105.24	1.575	73.67	116.03
VCCSFRPLL_DDR3_1P5	1.5	26.28	39.42	1.575	27.59	39.11
TESTHI_1P5	1.5	41.56	62.34	1.575	43.64	68.73
1.8V Power Sources						
VCCAGPIO1P8	1.8	2.68	5.15	1.89	3.00	5.68
VCCSUS1P8	1.8	0.65	1.17	1.89	0.68	1.29
VCCASFRHPLL1P8	1.8	20.73	37.32	1.89	21.77	41.15
VCCABGTS1P8	1.8	22.23	40.02	1.89	23.35	44.12
3.3V Power Sources						
VCCAGPIO3P3	3.3	25.03	82.59	3.465	26.28	91.05
VCCSUS3P3	3.3	4.03	13.3	3.465	4.23	14.66
VCCRTC3P3	3.3	0.10	0.33	3.465	0.11	0.36

Notes:
Note: Includes power source pins VCCAxxx_1P5 used for PCI Express analog interface power. Includes voltage reference pins VCCREFxxx_1P5.

Table 7-8. Intel® Atom™ Processor S1260 SKU (1.35V DDR3-L) Voltage Source DC Characteristics (TDP@Tj=95C and MAX@Tj=95C)

Voltage Rail	Voltage	ITDP (mA)	PTDP (mW)	VMAX(V)	IMAX (mA)	PMAX (mW)
1.05V Processor VID Rail						
VCCCPU0VIDSI01P05	1.13	3161.81	3463.41	1.15	4052.26	4660.10
1.05V Power Sources						
VCC	1.05	2031.99	2133.59	1.15	2375.51	2709.34
VCCSUS1P05	1.05	0.34	0.36	1.15	0.37	0.43
VCCDHPLL1P05	1.05	7.74	8.13	1.15	8.48	9.75
VCCPLL_DDR3_1P05	1.05	8.69	9.13	1.15	9.52	10.95
VCCRAMCPU0XSI01P05	1.05	65.02	68.28	1.15	71.22	81.90
VCCRAMCPU1XSI01P05	1.05	65.02	68.28	1.15	71.22	81.90
VCCPLLCPU0SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCPLLCPU1SI01P05	1.05	0.02	0.02	1.15	0.02	0.02
VCCFHVCPU0SI01P05	1.05	0	0	1.15	0	0
VCCFHVCPU1SI01P05	1.05	0	0	1.15	0	0
VCCA_DDR3_1P05	1.05	309.05	324.50	1.15	446.45	513.42
VCCACLK_DDR3_1P05	1.05	8.69	9.13	1.15	9.52	10.95
VCCADLL_DDR3_1P05	1.05	99.19	104.15	1.15	123.45	141.97
VCCFHVSOC1P05	1.05	21.85	22.94	1.15	23.93	27.52
VCCANTB_1P05	1.05	937.53	984.40	1.15	1043.28	1199.77
TESTHI_1P05	1.05	0	0	1.15	0	0
1.5V Power Sources						
VCCATS1P5	1.5	6.27	9.40	1.575	6.58	10.36
PCI Express* Analog[1]	1.5	27.65	41.47	1.575	29.03	45.72
PCI Express Reference[2]	1.5	6.79	10.19	1.575	7.13	11.23
VCC_DDR3_1P5	1.35	508.71	686.75	1.42	624.20	884.80
VCCCLK_DDR3_1P5	1.35	68.60	92.61	1.42	66.30	93.99
VCCSFRPLL_DDR3_1P5	1.5	22.93	34.39	1.575	24.07	34.12
TESTHI_1P5	1.5	41.56	62.34	1.575	43.64	68.73
1.8V Power Sources						
VCCAGPIO1P8	1.8	2.86	5.15	1.89	3.00	5.68
VCCSUS1P8	1.8	0.65	1.17	1.89	0.68	1.29
VCCASFRHPLL1P8	1.8	20.73	37.32	1.89	21.77	41.15
VCCABGTS1P8	1.8	22.23	40.02	1.89	23.35	44.12
3.3V Power Sources						
VCCAGPIO3P3	3.3	25.03	82.59	3.465	26.28	91.05
VCCSUS3P3	3.3	4.03	13.3	3.465	4.23	14.66
VCCRTC3P3	3.3	0.10	0.33	3.465	0.11	0.36

Notes:
1. Includes power source pins VCCAxxx_1P5 used for PCI Express analog interface power. Includes voltage reference pins VCCREFxxx_1P5.

7.3 Signal Input and Output Operational DC Characteristics

The operational DC characteristics are shown by Buffer Type in Table 7-9 below. Refer to Chapter 6, "Signal Descriptions" of this document, to match the external signal pins with the Buffer Type classifications.

Table 7-9. Signal DC Operational Characteristics (Sheet 1 of 3)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
CMOS1.05 Buffers						
V_{IL}	Input Low Voltage			0.284	V	
V_{IH}	Input High Voltage	0.624			V	
V_{OL}	Output Low Voltage			0.105	V	
V_{OH}	Output High Voltage	0.945			V	
I_{OL}	Output Low Current	-1.5			mA	
I_{OH}	Output High Current			500	µA	
I_{IL}	Input Leakage Current			10	µA	
C_{pad}	Pad Capacitance	2		25	pF	
$I_{IL(2)}$	Input Leakage Current			60	µA	Read Note 1
$C_{pad(2)}$	Pad Capacitance	2		5	pF	Read Note 1
Note: (1) $I_{IL(2)}$ & $C_{pad(2)}$ are for following signals: CPU0HFPLL, CPU1HFPLL, PSMI_VISA[29:0], OWDTOUT, CPU_IERR						
CMOS1.05_OD Open-Drain Buffers						
V_{OL}	Output Low Voltage			0.105	V	
V_{OH}	Output High Voltage	0.997	1.05	1.102	V	200 ohm pull-up
I_{OL}	Output Low Current	-1.5			mA	
I_{OH}	Output High Current			500	µA	
C_{pad}	**Pad Capacitance**	2		25	pF	
Vccx	Supply Voltage		1.05		V	
CMOS1.5 Buffers (DDR3)						
V_{IL}	Input Low Voltage			0.598	V	
V_{IH}	Input High Voltage	0.85			V	
V_{OL}	Output Low Voltage		0.3		V	
V_{OH}	Output High Voltage		1.2		V	
I_{OL}	Output Low Current		11.5		mA	
I_{OH}	Output High Current		-46		mA	
I_{IL}	Input Leakage Current			40	µA	
R_{ON}	DDR3 Clock Buffer Strength		26		ohm	
C_{pad}	Pad Capacitance		2.6		pF	

Table 7-9. Signal DC Operational Characteristics (Sheet 2 of 3)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
CMOS1.8 Buffers						
V_{IL}	Input Low Voltage			0.63	V	
V_{IH}	Input High Voltage	1.08			V	
V_{OL}	Output Low Voltage			0.18	V	For Open Drain 200 ohm pull-up resistor
V_{OH}	Output High Voltage	1.62			V	
I_{OL}	Output Low Current	-1.5			mA	
I_{OH}	Output High Current	0.5			mA	
I_{IL}	Input Leakage Current		10		µA	
C_{pad}	Pad Capacitance	2		75	pF	
CMOS3.3 Buffers						
V_{IL}	Input Low Voltage			0.99	V	
V_{IH}	Input High Voltage	1.65			V	
V_{OL}	Output Low Voltage			0.33	V	
V_{OH}	Output High Voltage	2.97			V	
I_{LEAK}	Input Leakage Current		35		µA	
C_{PAD}	Input Capacitance	2		25	pF	
Vccx	Supply Voltage	-0.25	3.3	3.96	V	
$I_{LEAK(2)}$	Input Leakage Current		100		µA	Read Note 2
$C_{PAD(2)}$	Input Capacitance	2		15	pF	Read Note 2
Note: (2) $I_{LEAK(2)}$ & $C_{PAD(2)}$ are for LPC signals.						
CMOS3.3_OD Open-Drain Buffers						
V_{IL}	Input Low Voltage			0.99	V	
V_{IH}	Input High Voltage	1.65			V	
V_{OL}	Output Low Voltage			0.33	V	
V_{OH}	Output High Voltage	2.97			V	
I_{LEAK}	Input Leakage Current		35		µA	
C_{PAD}	Input Capacitance	2		25	pF	
Vccx	Supply Voltage	-0.25	3.3	3.96	V	

Table 7-9. Signal DC Operational Characteristics (Sheet 3 of 3)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
PCI Express* Transmit and Receive						
$V_{TX-DIFF\ P-P}$	Differential Peak to Peak Output Voltage	0.8	1.0	1.2	V	
V_{TX_CM-ACp}	AC Peak Common Mode Output Voltage			60	mV	
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	
$V_{RX-DIFF\ p-p}$	Differential Input Peak to Peak Voltage	0.175		1.2	V	
V_{RX_CM-ACp}	AC peak Common Mode Input Voltage			75@2.5GHz 300@100MHz	mV	
Reference-Clock Input - Host, Memory, PCI Express Port, and HPET						
V_{SWING}	Input swing	300			mV	
V_{CROSS}	Crossing point	300		550	mV	
V_{CROSS_VAR}	V_{CROSS} Variance			140	mV	
V_{IH}	Maximum input voltage			1.5	V	
V_{IL}	Minimum input voltage	-0.3			V	
RTCRESETB, PWROK, RSMRSTB, RTC_INTVRMEN						
V_{IH}	Input high voltage	2.17		VCCRTC3P3 +0.5	V	
V_{IL}	Input low voltage	-0.5		0.68	V	
RTC Crystal Pads						
CL	RTC_X1PAD, RTC_X2PAD Capacitance (typical)	18			pF	Typical values for external capacitors are 18pF, based on crystal load of 12.5pF.

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8 Component Ball-Out Listing

This chapter provides the ball-out (also called solder balls, pins, bumps) assignments for the S12x0 processor.

Warning: The balls with the signal name “NC” are “No-Connect” balls. The platform board must not make any connections to these balls.

The ball-out assignments are first shown in alphabetical order according to the signal name, Section 8.1, “Sorted by Signal Name” , and then according to the ball-grid number assignment, Section 8.3, “Ball Map” shows the ball map and the physical locations of the signals on the ball grid.

8.1 Sorted by Signal Name

See Table 8-1, “Ball-out Sorted by Signal Name” on page 121, starting on following page.

Table 8-1. Ball-out Sorted by Signal Name (Sheet 1 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
BOOTDEVSEL	E52	DDR3_DQ[19]	BB26
CPU_EXTBGREF	E36	DDR3_DQ[2]	BG15
CPU_IERR	AG54	DDR3_DQ[20]	BH26
CPU_PRDYB	AC52	DDR3_DQ[21]	BB25
CPU_PREQB	AE62	DDR3_DQ[22]	BA29
CPU_PROCHOTB	AC56	DDR3_DQ[23]	BG29
CPU0_HFPLL	AH50	DDR3_DQ[24]	BM22
CPU0_SFRANAD	C36	DDR3_DQ[25]	BN28
CPU0_THERMDA	AD39	DDR3_DQ[26]	BN23
CPU0_THERMDC	AC38	DDR3_DQ[27]	BM27
CPU1_HFPLL	AG50	DDR3_DQ[28]	BP22
CPU1_SFRANAD	D35	DDR3_DQ[29]	BL28
CPU1_THERMDA	AG39	DDR3_DQ[3]	BH19
CPU1_THERMDC	AF38	DDR3_DQ[30]	BL23
DDR3_BS[0]	BL43	DDR3_DQ[31]	BL26
DDR3_BS[1]	BL41	DDR3_DQ[32]	BM52
DDR3_BS[2]	BN32	DDR3_DQ[33]	BM58
DDR3_CASB	BN46	DDR3_DQ[34]	BN53
DDR3_CK[0]	BD41	DDR3_DQ[35]	BN57
DDR3_CK[1]	BG41	DDR3_DQ[36]	BL57
DDR3_CKB[0]	BD42	DDR3_DQ[37]	BL59
DDR3_CKB[1]	BG42	DDR3_DQ[38]	BL53
DDR3_CKE[0]	BL46	DDR3_DQ[39]	BM54
DDR3_CKE[1]	BK45	DDR3_DQ[4]	BG19
DDR3_CLKREFN	BF45	DDR3_DQ[40]	BH58
DDR3_CLKREFP	BG45	DDR3_DQ[41]	BB59
DDR3_CMDPU	BH34	DDR3_DQ[42]	BG58
DDR3_CSB[0]	BN44	DDR3_DQ[43]	BD60
DDR3_CSB[1]	BP46	DDR3_DQ[44]	BB57
DDR3_DQ[0]	BG13	DDR3_DQ[45]	BB60
DDR3_DQ[1]	BF21	DDR3_DQ[46]	BH57
DDR3_DQ[10]	BN14	DDR3_DQ[47]	BE57
DDR3_DQ[11]	BM18	DDR3_DQ[48]	BD65
DDR3_DQ[12]	BP13	DDR3_DQ[49]	AY65
DDR3_DQ[13]	BN19	DDR3_DQ[5]	BG21
DDR3_DQ[14]	BL14	DDR3_DQ[50]	BE64
DDR3_DQ[15]	BL17	DDR3_DQ[51]	AW62
DDR3_DQ[16]	BH25	DDR3_DQ[52]	AY63
DDR3_DQ[17]	BA25	DDR3_DQ[53]	AW64
DDR3_DQ[18]	BG25	DDR3_DQ[54]	BD63

Table 8-1. Ball-out Sorted by Signal Name (Sheet 2 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
DDR3_DQ[55]	BC64	DDR3_ECC[6]	BH49
DDR3_DQ[56]	AT63	DDR3_ECC[7]	BK49
DDR3_DQ[57]	AT64	DDR3_MA[0]	BK40
DDR3_DQ[58]	AR65	DDR3_MA[1]	BL39
DDR3_DQ[59]	AN65	DDR3_MA[10]	BN41
DDR3_DQ[6]	BD13	DDR3_MA[11]	BL34
DDR3_DQ[60]	AL63	DDR3_MA[12]	BL32
DDR3_DQ[61]	AR63	DDR3_MA[13]	BN48
DDR3_DQ[62]	AL62	DDR3_MA[14]	BM31
DDR3_DQ[63]	AL65	DDR3_MA[15]	BP31
DDR3_DQ[7]	BF13	DDR3_MA[2]	BP40
DDR3_DQ[8]	BM13	DDR3_MA[3]	BL37
DDR3_DQ[9]	BL19	DDR3_MA[4]	BN39
DDR3_DQPU	BG34	DDR3_MA[5]	BN37
DDR3_DQS[0]	BG17	DDR3_MA[6]	BP37
DDR3_DQS[1]	BN17	DDR3_MA[7]	BL35
DDR3_DQS[2]	BE26	DDR3_MA[8]	BN35
DDR3_DQS[3]	BN26	DDR3_MA[9]	BM34
DDR3_DQS[4]	BL55	DDR3_MON1N	BG38
DDR3_DQS[5]	BH62	DDR3_MON1P	BG37
DDR3_DQS[6]	BB63	DDR3_MON2N	BF38
DDR3_DQS[7]	AN63	DDR3_MON2P	BF37
DDR3_DQSB[0]	BH17	DDR3_ODT[0]	BL48
DDR3_DQSB[1]	BM16	DDR3_ODT[1]	BP49
DDR3_DQSB[2]	BD26	DDR3_ODTPU	BH32
DDR3_DQSB[3]	BM25	DDR3_RASB	BP43
DDR3_DQSB[4]	BN55	DDR3_SYSPWRGOOD	BG32
DDR3_DQSB[5]	BF62	DDR3_VREF	BH41
DDR3_DQSB[6]	BB65	DDR3_WEB	BL44
DDR3_DQSB[7]	AP64	DFX_GPIO_GRP0[0]	D30
DDR3_DQSECC	BE49	DFX_GPIO_GRP0[1]	D28
DDR3_DQSECCB	BG49	DFX_GPIO_GRP0[2]	B28
DDR3_DRAM_PWROK	BH42	DFX_GPIO_GRP0[3]	B30
DDR3_DRAMRSTB	BC38	DFX_GPIO_GRP0[4]	H32
DDR3_ECC[0]	BG50	DFX_GPIO_GRP0[5]	H30
DDR3_ECC[1]	BB49	DFX_GPIO_GRP0[6]	E28
DDR3_ECC[2]	BK51	DFX_GPIO_GRP0[7]	J30
DDR3_ECC[3]	BD50	DFX_GPIO_GRP1[0]	C33
DDR3_ECC[4]	BD49	DFX_GPIO_GRP1[1]	D33
DDR3_ECC[5]	BA50	DFX_GPIO_GRP1[2]	G34

Table 8-1. Ball-out Sorted by Signal Name (Sheet 3 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
DFX_GPIO_GRP1[3]	H34	HPLL_CLKREFN	V20
DFX_GPIO_GRP1[4]	B35	HPLL_CLKREFP	V21
DFX_GPIO_GRP1[5]	E31	HPLL_MONN	H1
DFX_GPIO_GRP1[6]	C31	HPLL_MONP	F1
DFX_GPIO_GRP1[7]	G32	HV_GPIO_RCOMP	M38
EDM	AG57	HVMGEAR_SEL	AD52
EPWRGOOD	AD58	JTA_POWEROK	AC53
ERR[0]	H48	LPC_AD[0]	G42
ERR[1]	D51	LPC_AD[1]	G41
ERR[2]	C51	LPC_AD[2]	H42
GPIOCORE[1]	K50	LPC_AD[3]	H41
GPIOCORE[10]	D57	LPC_CLKOUT[0]	B44
GPIOCORE[11]	B55	LPC_CLKOUT[1]	C45
GPIOCORE[12]	G62	LPC_CLKRUN_B	C42
GPIOCORE[13]	E57	LPC_FRAME_B	D44
GPIOCORE[14]	E59	LPC_SERIRQ	J46
GPIOCORE[15]	G64	LPCCLK0_DS	R63
GPIOCORE[16]	H56	LV_GPIO_RCOMP	AC47
GPIOCORE[17]	L54	MEM_SPEED[0]	AD56
GPIOCORE[18]	H59	MEM_SPEED[1]	AD53
GPIOCORE[19]	L52	MV_GPIO_RCOMP	P34
GPIOCORE[2]	K48	NC	B53
GPIOCORE[20]	N48	NC	G17
GPIOCORE[3]	D53	NC	G18
GPIOCORE[4]	H52	NC	G25
GPIOCORE[5]	H54	NC	G26
GPIOCORE[6]	E55	NC	H13
GPIOCORE[7]	D55	NC	H17
GPIOCORE[8]	B57	NC	H18
GPIOCORE[9]	M46	NC	H25
GPIOSUS[0]	M52	NC	H26
GPIOSUS[1]	L59	NC	J13
GPIOSUS[2]	M56	NC	J21
GPIOSUS[3]	P50	NC	J22
GPIOSUS[4]	M59	NC	L17
GPIOSUS[5]	M60	NC	L18
GPIOSUS[6]	K62	NC	L21
GPIOSUS[7]	L60	NC	L22
GPIOSUS[8]	N50	NC	L25
HPET_CLK14IN	P46	NC	L26

Table 8-1. Ball-out Sorted by Signal Name (Sheet 4 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
NC	N8	NC	AM9
NC	N10	NC	AM11
NC	N13	NC	AM14
NC	N14	NC	AM15
NC	N17	NC	AR8
NC	N18	NC	AR10
NC	N25	NC	AR14
NC	N26	NC	AR16
NC	R9	NC	AT8
NC	R11	NC	AT10
NC	R14	NC	AT13
NC	R15	NC	AT14
NC	U9	NC	AW14
NC	U11	NC	AW15
NC	U14	OWDTOUT	AH53
NC	U15	PSMI_VISA[0]	AT53
NC	W8	PSMI_VISA[1]	AR53
NC	Y8	PSMI_VISA[10]	AM52
NC	AC9	PSMI_VISA[11]	AR59
NC	AC11	PSMI_VISA[12]	AM58
NC	AC14	PSMI_VISA[13]	AM56
NC	AC15	PSMI_VISA[14]	AW56
NC	AD9	PSMI_VISA[15]	AL53
NC	AD11	PSMI_VISA[16]	AL52
NC	AD14	PSMI_VISA[17]	AW58
NC	AD15	PSMI_VISA[18]	AH57
NC	AG8	PSMI_VISA[19]	AH59
NC	AG10	PSMI_VISA[2]	AT59
NC	AG13	PSMI_VISA[20]	AL56
NC	AG14	PSMI_VISA[21]	AH62
NC	AG53	PSMI_VISA[22]	AJ63
NC	AH8	PSMI_VISA[23]	AL58
NC	AH10	PSMI_VISA[24]	AJ65
NC	AH13	PSMI_VISA[25]	AG66
NC	AH14	PSMI_VISA[26]	AG60
NC	AH54	PSMI_VISA[27]	AG64
NC	AL9	PSMI_VISA[28]	AG63
NC	AL11	PSMI_VISA[29]	AF63
NC	AL14	PSMI_VISA[3]	AT54
NC	AL15	PSMI_VISA[4]	AR54

Table 8-1. Ball-out Sorted by Signal Name (Sheet 5 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
PSMI_VISA[5]	AT60	RP0_PETP[5]	BC8
PSMI_VISA[6]	AT57	RP0_PETP[6]	AY11
PSMI_VISA[7]	AR57	RP0_PETP[7]	AW9
PSMI_VISA[8]	AR60	RP0_PLLMON0	BM5
PSMI_VISA[9]	AM53	RP0_PLLMON1	BM3
PUNIT_ST_ADDR[0]	AG48	RP0_RCOMP	AT23
PUNIT_ST_ADDR[1]	AH48	RSMRSTB	L63
PWROK	J63	RSTRDYB	M54
RESETB	T58	RSTWARN	T53
RP0_CLKINN	BF4	RSVD_MVT[0]	B39
RP0_CLKINP	BE5	RSVD_MVT[1]	H37
RP0_PERN[0]	BM9	RTC_EXTPAD	L65
RP0_PERN[1]	BM7	RTC_INTVRMEN	J64
RP0_PERN[2]	BJ4	RTC_SRTCRSTB	N62
RP0_PERN[3]	BF1	RTC_X1PAD	R65
RP0_PERN[4]	BD4	RTC_X2PAD	N65
RP0_PERN[5]	BB2	RTCRESETB	R62
RP0_PERN[6]	AY5	SLPMODE	R56
RP0_PERN[7]	AY4	SLPRDYB	R58
RP0_PERP[0]	BN10	SMBD_CLK	W11
RP0_PERP[1]	BL7	SMBD_DATA	W17
RP0_PERP[2]	BH3	SMBH_CLK	Y11
RP0_PERP[3]	BF3	SMBH_DATA	W13
RP0_PERP[4]	BD2	SMBM_CLK	Y13
RP0_PERP[5]	BB4	SMBM_DATA	W16
RP0_PERP[6]	BB5	SOC_TCK	AD62
RP0_PERP[7]	AY2	SOC_TDI	AA66
RP0_PETN[0]	BB19	SOC_TDO	AA64
RP0_PETN[1]	BB17	SOC_THERMANATP[0]	T18
RP0_PETN[2]	BK9	SOC_THERMANATP[1]	P22
RP0_PETN[3]	BG9	SOC_THERMDA	R21
RP0_PETN[4]	BD8	SOC_THERMDC	P21
RP0_PETN[5]	BC10	SOC_THERMREFNPAD	R22
RP0_PETN[6]	AY9	SOC_TMS	AD63
RP0_PETN[7]	AW11	SOC_TRSTB	AA62
RP0_PETP[0]	BD19	SPD_ENB	AD49
RP0_PETP[1]	BD17	SPI_CSB[0]	C40
RP0_PETP[2]	BH8	SPI_CSB[1]	E39
RP0_PETP[3]	BG8	SPI_MISO	E40
RP0_PETP[4]	BD10	SPI_MOSI	D42

Table 8-1. Ball-out Sorted by Signal Name (Sheet 6 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
SPI_SCLK	J38	TESTLO_08	AN2
SPKR	H38	TESTLO_08	AR2
SUSCLK	T52	TESTLO_08	AT5
SVID_ALERT_B	AB63	TESTLO_08	AU1
SVID_CLK	AB62	TESTLO_09	W1
SVID_DATA	AC58	TESTLO_10	Y2
TESTHI_1P05	AE64	TESTLO_11	AJ23
TESTHI_1P5_00	AA21	TESTLO_12	N2
TESTHI_1P5_01	AA28	TESTLO_12	R2
TESTHI_1P5_02	AM21	TESTLO_12	R5
TESTHI_1P5_03	AM28	TESTLO_12	U2
TESTHI_1P5_04	AJ21	TESTLO_12	W4
TESTHI_1P5_05	AJ28	TESTLO_12	AB4
TESTLO_00	B41	TESTLO_12	AD4
TESTLO_01	H14	TESTLO_12	AD5
TESTLO_02	J14	TESTLO_13	E49
TESTLO_03	AA23	TESTLO_14	A51
TESTLO_04	B12	TESTLO_15	B10
TESTLO_04	B19	TESTLO_15	B17
TESTLO_04	B21	TESTLO_15	C15
TESTLO_04	B26	TESTLO_15	C24
TESTLO_04	D10	TESTLO_15	D19
TESTLO_04	D12	TESTLO_15	D21
TESTLO_04	D15	TESTLO_15	D23
TESTLO_04	D17	TESTLO_15	D24
TESTLO_04	D26	TESTLO_15	E10
TESTLO_04	E21	TESTLO_15	E12
TESTLO_04	E23	TESTLO_15	E19
TESTLO_04	F5	TESTLO_15	G5
TESTLO_04	G9	TESTLO_15	H9
TESTLO_04	H10	TESTLO_15	K4
TESTLO_04	K3	TESTLO_15	K10
TESTLO_04	L2	TESTLO_15	L4
TESTLO_05	AL5	TESTLO_16	AF4
TESTLO_06	AN5	TESTLO_16	AG5
TESTLO_07	AM23	TESTLO_16	AH3
TESTLO_08	AF2	TESTLO_16	AL2
TESTLO_08	AH1	TESTLO_16	AN4
TESTLO_08	AH4	TESTLO_16	AR4
TESTLO_08	AL4	TESTLO_16	AU3

Table 8-1. Ball-out Sorted by Signal Name (Sheet 7 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
TESTLO_16	AV2	VCC	AL32
TESTLO_17	N4	VCC	AL36
TESTLO_17	N5	VCC	AL39
TESTLO_17	R4	VCC	AL42
TESTLO_17	U4	VCC	AM31
TESTLO_17	V5	VCC	AM34
TESTLO_17	AB2	VCC	AM38
TESTLO_17	AB5	VCC	AM41
TESTLO_17	AD2	VCC	AP29
THRMB	J37	VCC	AP32
THRMTRIPB	AG59	VCC	AT31
UART_CTS_N	C49	VCC	AT34
UART_DCD_N	H46	VCC	AU29
UART_DSR_N	J44	VCC	AU32
UART_DTR_N	A48	VCC_DDR3_1P5	BD37
UART_RI_N	B48	VCC_DDR3_1P5	BD38
UART_RTS_N	H50	VCC_DDR3_1P5	BD45
UART_RXD	D48	VCC_DDR3_1P5	BE32
UART_TXD	E48	VCC_DDR3_1P5	BE34
VCC	W32	VCC_DDR3_1P5	BE41
VCC	W36	VCC_DDR3_1P5	BE42
VCC	W39	VCC_DDR3_1P5	BK32
VCC	W42	VCC_DDR3_1P5	BK35
VCC	AA31	VCC_DDR3_1P5	BK37
VCC	AA34	VCC_DDR3_1P5	BK39
VCC	AA38	VCC_DDR3_1P5	BK44
VCC	AA41	VCC_DDR3_1P5	BK46
VCC	AC31	VCC_DDR3_1P5	BM36
VCC	AD29	VCC_DDR3_1P5	BM40
VCC	AD32	VCC_DDR3_1P5	BM43
VCC	AF31	VCC_DDR3_1P5	BM45
VCC	AG29	VCC_DDR3_1P5	BM49
VCC	AG32	VCC_DDR3_1P5	BP34
VCC	AG36	VCCA_DDR3_1P05	AP36
VCC	AJ31	VCCA_DDR3_1P05	AP38
VCC	AJ34	VCCA_DDR3_1P05	AP39
VCC	AJ38	VCCA_DDR3_1P05	AP41
VCC	AJ41	VCCA_DDR3_1P05	AP42
VCC	AJ44	VCCA_DDR3_1P05	AP44
VCC	AL29	VCCA_DDR3_1P05	AP46

Table 8-1. Ball-out Sorted by Signal Name (Sheet 8 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
VCCA_DDR3_1P05	AR48	VCCANTB_1P05	AL26
VCCA_DDR3_1P05	AR50	VCCANTB_1P05	AL28
VCCABGTS1P8	AG23	VCCANTB_1P05	AP20
VCCACLK_DDR3_1P05	AW32	VCCANTB_1P05	AP21
VCCACLK_DDR3_1P05	BA32	VCCANTB_1P05	AP23
VCCADLL_DDR3_1P05	AU36	VCCANTB_1P05	AP25
VCCADLL_DDR3_1P05	AU38	VCCANTB_1P05	AP26
VCCADLL_DDR3_1P05	AU39	VCCANTB_1P05	AP28
VCCADLL_DDR3_1P05	AU41	VCCANTB_1P05	AR19
VCCADLL_DDR3_1P05	AU42	VCCANTB_1P05	AU23
VCCADLL_DDR3_1P05	AU44	VCCANTB_1P05	AU25
VCCADLL_DDR3_1P05	AU46	VCCANTB_1P05	AU26
VCCADLL_DDR3_1P05	AU47	VCCANTB_1P05	AU28
VCCADLL_DDR3_1P05	AW46	VCCANTB_1P05	AW21
VCCADLL_DDR3_1P05	AW47	VCCANTB_1P05	AW23
VCCAGPIO1P8	L32	VCCANTB_1P05	AY21
VCCAGPIO1P8	N32	VCCANTB_1P05	AY23
VCCAGPIO1P8	P32	VCCARP0_1P5	AT21
VCCAGPIO1P8	T32	VCCASFRHPLL1P8	AD23
VCCAGPIO1P8	V32	VCCASFRHPLL1P8	AD25
VCCAGPIO1P8	AG28	VCCATS1P5	AF28
VCCAGPIO3P3	M37	VCCCLK_DDR3_1P5	BA41
VCCAGPIO3P3	P37	VCCCLK_DDR3_1P5	BB41
VCCAGPIO3P3	R37	VCCCPU0SENSE	AD41
VCCAGPIO3P3	T36	VCCCPU0VIDSI01P05	U62
VCCAGPIO3P3	V36	VCCCPU0VIDSI01P05	U63
VCCAGPIO3P3	AF23	VCCCPU0VIDSI01P05	U65
VCCANTB_1P05	AC18	VCCCPU0VIDSI01P05	V63
VCCANTB_1P05	AC20	VCCCPU0VIDSI01P05	V64
VCCANTB_1P05	AC21	VCCCPU0VIDSI01P05	V66
VCCANTB_1P05	AC23	VCCCPU0VIDSI01P05	W44
VCCANTB_1P05	AC25	VCCCPU0VIDSI01P05	W46
VCCANTB_1P05	AC26	VCCCPU0VIDSI01P05	W48
VCCANTB_1P05	AD18	VCCCPU0VIDSI01P05	W50
VCCANTB_1P05	AD20	VCCCPU0VIDSI01P05	W53
VCCANTB_1P05	AL18	VCCCPU0VIDSI01P05	W54
VCCANTB_1P05	AL20	VCCCPU0VIDSI01P05	W57
VCCANTB_1P05	AL21	VCCCPU0VIDSI01P05	W59
VCCANTB_1P05	AL23	VCCCPU0VIDSI01P05	Y48
VCCANTB_1P05	AL25	VCCCPU0VIDSI01P05	Y50

Table 8-1. Ball-out Sorted by Signal Name (Sheet 9 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
VCCCPU0VIDSI01P05	Y53	VSS	A18
VCCCPU0VIDSI01P05	Y54	VSS	A21
VCCCPU0VIDSI01P05	Y57	VSS	A24
VCCCPU0VIDSI01P05	Y59	VSS	A27
VCCCPU0VIDSI01P05	AA44	VSS	A30
VCCCPU0VIDSI01P05	AA46	VSS	A33
VCCCPU0VIDSI01P05	AC44	VSS	A36
VCCCPU0VIDSI0GT1P05	AC41	VSS	A39
VCCCPU0VIDSI0GT1P05	AC42	VSS	A42
VCCCPU1VIDSI0GT1P05	AG41	VSS	A45
VCCCPU1VIDSI0GT1P05	AG42	VSS	A54
VCCDHPLL1P05	AD28	VSS	A57
VCCFHVCPU0SI01P05	AC36	VSS	B14
VCCFHVCPU1SI01P05	AF36	VSS	B23
VCCFHVSOC1P05	AL47	VSS	B32
VCCFHVSOC1P05	AL49	VSS	B37
VCCPLL_DDR3_1P05	AY38	VSS	B46
VCCPLL_DDR3_1P05	BA38	VSS	B50
VCCPLLCPU0SI01P05	AC49	VSS	C6
VCCPLLCPU1SI01P05	AD47	VSS	C9
VCCRAMCPU0XSI01P05	AC34	VSS	C13
VCCRAMCPU0XSI01P05	AG34	VSS	C18
VCCREFRP0_1P5	AT28	VSS	C22
VCCRTC3P3	M44	VSS	C27
VCCRTC3P3	P44	VSS	C54
VCCRTC3P3	R44	VSS	C58
VCCRTC3P3	T44	VSS	C60
VCCSFRPLL_DDR3_1P5	BA34	VSS	D6
VCCSFRPLL_DDR3_1P5	BB34	VSS	D8
VCCSUS1P05	P48	VSS	D14
VCCSUS1P05	T47	VSS	D32
VCCSUS1P05	T48	VSS	D37
VCCSUS1P8	L41	VSS	D39
VCCSUS1P8	N41	VSS	D41
VCCSUS1P8	P41	VSS	D46
VCCSUS3P3	L42	VSS	D50
VCCSUS3P3	N42	VSS	D59
VCCSUS3P3	P42	VSS	D60
VCCSUS3P3	T42	VSS	E7
VSS	A15	VSS	E9

Table 8-1. Ball-out Sorted by Signal Name (Sheet 10 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
VSS	E13	VSS	J66
VSS	E14	VSS	K17
VSS	E16	VSS	K18
VSS	E18	VSS	K25
VSS	E22	VSS	K26
VSS	E25	VSS	K32
VSS	E27	VSS	K34
VSS	E30	VSS	K41
VSS	E32	VSS	K42
VSS	E34	VSS	L5
VSS	E37	VSS	L7
VSS	E41	VSS	L8
VSS	E43	VSS	L13
VSS	E45	VSS	L14
VSS	E46	VSS	L29
VSS	E50	VSS	L30
VSS	E54	VSS	L34
VSS	E58	VSS	L37
VSS	E61	VSS	L38
VSS	F4	VSS	L44
VSS	F63	VSS	L46
VSS	G3	VSS	L48
VSS	G7	VSS	L50
VSS	G10	VSS	L57
VSS	G48	VSS	M3
VSS	G50	VSS	M5
VSS	G56	VSS	M21
VSS	G59	VSS	M22
VSS	H4	VSS	M29
VSS	H21	VSS	M30
VSS	H22	VSS	M57
VSS	H29	VSS	M62
VSS	H44	VSS	M64
VSS	H58	VSS	M66
VSS	H62	VSS	N7
VSS	H63	VSS	N11
VSS	J5	VSS	N34
VSS	J29	VSS	N63
VSS	J52	VSS	P17
VSS	J54	VSS	P18

Table 8-1. Ball-out Sorted by Signal Name (Sheet 11 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
VSS	P25	VSS	V23
VSS	P26	VSS	V25
VSS	P29	VSS	V26
VSS	P30	VSS	V28
VSS	P38	VSS	V29
VSS	R8	VSS	V31
VSS	R12	VSS	V34
VSS	R29	VSS	V38
VSS	R30	VSS	V39
VSS	R38	VSS	V41
VSS	R46	VSS	V42
VSS	R52	VSS	V44
VSS	R53	VSS	V46
VSS	R55	VSS	W3
VSS	R59	VSS	W7
VSS	R66	VSS	W10
VSS	T1	VSS	W14
VSS	T3	VSS	W19
VSS	T5	VSS	W21
VSS	T17	VSS	W23
VSS	T20	VSS	W25
VSS	T21	VSS	W26
VSS	T23	VSS	W28
VSS	T25	VSS	W29
VSS	T26	VSS	W31
VSS	T28	VSS	W34
VSS	T29	VSS	W38
VSS	T31	VSS	W41
VSS	T34	VSS	W51
VSS	T37	VSS	W56
VSS	T39	VSS	W60
VSS	T41	VSS	W62
VSS	T45	VSS	Y4
VSS	T50	VSS	Y5
VSS	T55	VSS	Y7
VSS	T59	VSS	Y10
VSS	T62	VSS	Y14
VSS	T64	VSS	Y16
VSS	U8	VSS	Y17
VSS	U12	VSS	Y19

Table 8-1. Ball-out Sorted by Signal Name (Sheet 12 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
VSS	Y51	VSS	AD46
VSS	Y56	VSS	AD50
VSS	Y60	VSS	AD55
VSS	Y63	VSS	AD59
VSS	Y65	VSS	AD65
VSS	AA3	VSS	AD66
VSS	AA5	VSS	AE1
VSS	AA25	VSS	AE3
VSS	AA26	VSS	AE5
VSS	AA29	VSS	AE47
VSS	AA32	VSS	AF20
VSS	AA36	VSS	AF21
VSS	AA39	VSS	AF25
VSS	AA42	VSS	AF26
VSS	AA47	VSS	AF29
VSS	AB1	VSS	AF32
VSS	AB20	VSS	AF34
VSS	AB65	VSS	AF39
VSS	AC8	VSS	AF42
VSS	AC12	VSS	AF44
VSS	AC17	VSS	AF46
VSS	AC28	VSS	AF62
VSS	AC29	VSS	AF65
VSS	AC32	VSS	AG7
VSS	AC39	VSS	AG11
VSS	AC46	VSS	AG16
VSS	AC50	VSS	AG17
VSS	AC55	VSS	AG19
VSS	AC59	VSS	AG21
VSS	AD8	VSS	AG25
VSS	AD12	VSS	AG26
VSS	AD17	VSS	AG31
VSS	AD21	VSS	AG38
VSS	AD26	VSS	AG44
VSS	AD31	VSS	AG46
VSS	AD34	VSS	AG51
VSS	AD36	VSS	AG56
VSS	AD38	VSS	AH7
VSS	AD42	VSS	AH11
VSS	AD44	VSS	AH16

Table 8-1. Ball-out Sorted by Signal Name (Sheet 13 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
VSS	AH17	VSS	AM20
VSS	AH19	VSS	AM25
VSS	AH51	VSS	AM26
VSS	AH56	VSS	AM29
VSS	AH60	VSS	AM32
VSS	AJ2	VSS	AM36
VSS	AJ4	VSS	AM39
VSS	AJ5	VSS	AM42
VSS	AJ25	VSS	AM44
VSS	AJ26	VSS	AM46
VSS	AJ29	VSS	AM47
VSS	AJ32	VSS	AM49
VSS	AJ36	VSS	AM50
VSS	AJ39	VSS	AM55
VSS	AJ42	VSS	AM59
VSS	AJ46	VSS	AN47
VSS	AJ47	VSS	AN62
VSS	AK3	VSS	AN66
VSS	AK5	VSS	AP1
VSS	AK20	VSS	AP3
VSS	AK62	VSS	AP5
VSS	AK64	VSS	AP31
VSS	AK66	VSS	AP34
VSS	AL1	VSS	AP62
VSS	AL8	VSS	AR7
VSS	AL12	VSS	AR11
VSS	AL17	VSS	AR13
VSS	AL31	VSS	AR17
VSS	AL34	VSS	AR51
VSS	AL38	VSS	AR56
VSS	AL41	VSS	AR62
VSS	AL44	VSS	AT7
VSS	AL46	VSS	AT11
VSS	AL50	VSS	AT16
VSS	AL55	VSS	AT17
VSS	AL59	VSS	AT19
VSS	AM8	VSS	AT25
VSS	AM12	VSS	AT26
VSS	AM17	VSS	AT29
VSS	AM18	VSS	AT32

Table 8-1. Ball-out Sorted by Signal Name (Sheet 14 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
VSS	AT36	VSS	AW49
VSS	AT38	VSS	AW50
VSS	AT39	VSS	AW52
VSS	AT41	VSS	AW53
VSS	AT42	VSS	AW55
VSS	AT44	VSS	AW59
VSS	AT46	VSS	AW66
VSS	AT48	VSS	AY1
VSS	AT50	VSS	AY8
VSS	AT51	VSS	AY12
VSS	AT56	VSS	AY14
VSS	AT66	VSS	AY15
VSS	AU4	VSS	AY19
VSS	AU21	VSS	AY29
VSS	AU31	VSS	AY30
VSS	AU34	VSS	AY37
VSS	AU62	VSS	AY45
VSS	AV4	VSS	AY46
VSS	AV5	VSS	AY52
VSS	AV63	VSS	AY53
VSS	AV65	VSS	AY55
VSS	AW3	VSS	AY56
VSS	AW5	VSS	AY58
VSS	AW8	VSS	AY59
VSS	AW12	VSS	AY62
VSS	AW17	VSS	BA17
VSS	AW19	VSS	BA21
VSS	AW20	VSS	BA23
VSS	AW25	VSS	BA26
VSS	AW26	VSS	BA30
VSS	AW28	VSS	BA37
VSS	AW30	VSS	BA42
VSS	AW31	VSS	BA45
VSS	AW34	VSS	BA46
VSS	AW36	VSS	BA49
VSS	AW38	VSS	BB32
VSS	AW39	VSS	BB42
VSS	AW41	VSS	BB50
VSS	AW42	VSS	BB53
VSS	AW44	VSS	BB54

Table 8-1. Ball-out Sorted by Signal Name (Sheet 15 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
VSS	BB56	VSS	BF29
VSS	BB62	VSS	BF30
VSS	BB66	VSS	BF46
VSS	BC1	VSS	BF53
VSS	BC3	VSS	BF54
VSS	BC5	VSS	BG4
VSS	BC7	VSS	BG5
VSS	BC11	VSS	BG11
VSS	BC13	VSS	BG23
VSS	BC15	VSS	BG26
VSS	BC21	VSS	BG30
VSS	BC23	VSS	BG46
VSS	BC29	VSS	BG53
VSS	BC30	VSS	BG54
VSS	BC37	VSS	BG57
VSS	BC45	VSS	BG63
VSS	BC46	VSS	BH5
VSS	BC62	VSS	BH11
VSS	BD7	VSS	BH50
VSS	BD15	VSS	BH60
VSS	BD21	VSS	BH64
VSS	BD23	VSS	BJ62
VSS	BD25	VSS	BJ63
VSS	BD29	VSS	BK6
VSS	BD30	VSS	BK8
VSS	BD32	VSS	BK10
VSS	BD34	VSS	BK12
VSS	BD46	VSS	BK13
VSS	BD53	VSS	BK15
VSS	BD54	VSS	BK17
VSS	BD59	VSS	BK18
VSS	BD62	VSS	BK19
VSS	BE17	VSS	BK21
VSS	BE19	VSS	BK22
VSS	BE25	VSS	BK24
VSS	BE50	VSS	BK26
VSS	BE63	VSS	BK27
VSS	BE66	VSS	BK28
VSS	BF15	VSS	BK30
VSS	BF23	VSS	BK31

Table 8-1. Ball-out Sorted by Signal Name (Sheet 16 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
VSS	BK36	VSS_NCTF	A64
VSS	BK42	VSS_NCTF	A66
VSS	BK48	VSS_NCTF	C3
VSS	BK53	VSS_NCTF	C5
VSS	BK54	VSS_NCTF	C62
VSS	BK56	VSS_NCTF	C64
VSS	BK57	VSS_NCTF	C66
VSS	BK58	VSS_NCTF	E1
VSS	BK60	VSS_NCTF	E3
VSS	BL8	VSS_NCTF	E5
VSS	BL10	VSS_NCTF	E62
VSS	BL12	VSS_NCTF	E64
VSS	BL16	VSS_NCTF	E66
VSS	BL21	VSS_NCTF	F66
VSS	BL25	VSS_NCTF	H66
VSS	BL30	VSS_NCTF	K1
VSS	BL50	VSS_NCTF	N1
VSS	BL52	VSS_NCTF	BG1
VSS	BL61	VSS_NCTF	BG66
VSS	BM61	VSS_NCTF	BJ1
VSS	BN12	VSS_NCTF	BJ66
VSS	BN21	VSS_NCTF	BK1
VSS	BN30	VSS_NCTF	BK3
VSS	BN50	VSS_NCTF	BK5
VSS	BP10	VSS_NCTF	BK62
VSS	BP16	VSS_NCTF	BK64
VSS	BP19	VSS_NCTF	BK66
VSS	BP25	VSS_NCTF	BM1
VSS	BP28	VSS_NCTF	BM62
VSS	BP52	VSS_NCTF	BM64
VSS	BP55	VSS_NCTF	BM66
VSS	BP58	VSS_NCTF	BP1
VSS_NCTF	A5	VSS_NCTF	BP3
VSS_NCTF	A6	VSS_NCTF	BP5
VSS_NCTF	A8	VSS_NCTF	BP6
VSS_NCTF	A9	VSS_NCTF	BP8
VSS_NCTF	A12	VSS_NCTF	BP59
VSS_NCTF	A59	VSS_NCTF	BP61
VSS_NCTF	A61	VSS_NCTF	BP62
VSS_NCTF	A62	VSS_NCTF	BP64

Table 8-1. Ball-out Sorted by Signal Name (Sheet 17 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
VSS_NCTF	BP66	WAKE_B	T56
VSSCPU0SENSE	AF41		

8.2 Sorted by Ball Number

See Table 8-2, “Ball-out Sorted by Ball Number” on page 139, starting on following page.

Table 8-2. Ball-out Sorted by Ball Number (Sheet 1 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
A5	VSS_NCTF	AA42	VSS
A6	VSS_NCTF	AA44	VCCCPU0VIDSI01P05
A8	VSS_NCTF	AA46	VCCCPU0VIDSI01P05
A9	VSS_NCTF	AA47	VSS
A12	VSS_NCTF	AA62	SOC_TRSTB
A15	VSS	AA64	SOC_TDO
A18	VSS	AA66	SOC_TDI
A21	VSS	AB1	VSS
A24	VSS	AB2	TESTLO_17
A27	VSS	AB4	TESTLO_12
A30	VSS	AB5	TESTLO_17
A33	VSS	AB20	VSS
A36	VSS	AB62	SVID_CLK
A39	VSS	AB63	SVID_ALERT_B
A42	VSS	AB65	VSS
A45	VSS	AC8	VSS
A48	UART_DTR_N	AC9	NC
A51	TESTLO_14	AC11	NC
A54	VSS	AC12	VSS
A57	VSS	AC14	NC
A59	VSS_NCTF	AC15	NC
A61	VSS_NCTF	AC17	VSS
A62	VSS_NCTF	AC18	VCCANTB_1P05
A64	VSS_NCTF	AC20	VCCANTB_1P05
A66	VSS_NCTF	AC21	VCCANTB_1P05
AA3	VSS	AC23	VCCANTB_1P05
AA5	VSS	AC25	VCCANTB_1P05
AA21	TESTHI_1P5_00	AC26	VCCANTB_1P05
AA23	TESTLO_03	AC28	VSS
AA25	VSS	AC29	VSS
AA26	VSS	AC31	VCC
AA28	TESTHI_1P5_01	AC32	VSS
AA29	VSS	AC34	VCCRAMCPU0XSI01P05
AA31	VCC	AC36	VCCFHVCPU0SI01P05
AA32	VSS	AC38	CPU0_THERMDC
AA34	VCC	AC39	VSS
AA36	VSS	AC41	VCCCPU0VIDSI0GT1P05
AA38	VCC	AC42	VCCCPU0VIDSI0GT1P05
AA39	VSS	AC44	VCCCPU0VIDSI01P05
AA41	VCC	AC46	VSS

Table 8-2. Ball-out Sorted by Ball Number (Sheet 2 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
AC47	LV_GPIO_RCOMP	AD52	HVMGEAR_SEL
AC49	VCCPLLCPU0SI01P05	AD53	MEM_SPEED[1]
AC50	VSS	AD55	VSS
AC52	CPU_PRDYB	AD56	MEM_SPEED[0]
AC53	JTA_POWEROK	AD58	EPWRGOOD
AC55	VSS	AD59	VSS
AC56	CPU_PROCHOTB	AD62	SOC_TCK
AC58	SVID_DATA	AD63	SOC_TMS
AC59	VSS	AD65	VSS
AD2	TESTLO_17	AD66	VSS
AD4	TESTLO_12	AE1	VSS
AD5	TESTLO_12	AE3	VSS
AD8	VSS	AE5	VSS
AD9	NC	AE47	VSS
AD11	NC	AE62	CPU_PREQB
AD12	VSS	AE64	TESTHI_1P05
AD14	NC	AF2	TESTLO_08
AD15	NC	AF4	TESTLO_16
AD17	VSS	AF20	VSS
AD18	VCCANTB_1P05	AF21	VSS
AD20	VCCANTB_1P05	AF23	VCCAGPIO3P3
AD21	VSS	AF25	VSS
AD23	VCCASFRHPLL1P8	AF26	VSS
AD25	VCCASFRHPLL1P8	AF28	VCCATS1P5
AD26	VSS	AF29	VSS
AD28	VCCDHPLL1P05	AF31	VCC
AD29	VCC	AF32	VSS
AD31	VSS	AF34	VSS
AD32	VCC	AF36	VCCFHVCPU1SI01P05
AD34	VSS	AF38	CPU1_THERMDC
AD36	VSS	AF39	VSS
AD38	VSS	AF41	VSSCPU0SENSE
AD39	CPU0_THERMDA	AF42	VSS
AD41	VCCCPU0SENSE	AF44	VSS
AD42	VSS	AF46	VSS
AD44	VSS	AF62	VSS
AD46	VSS	AF63	PSMI_VISA[29]
AD47	VCCPLLCPU1SI01P05	AF65	VSS
AD49	SPD_ENB	AG5	TESTLO_16
AD50	VSS	AG7	VSS

Table 8-2. Ball-out Sorted by Ball Number (Sheet 3 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
AG8	NC	AH8	NC
AG10	NC	AH10	NC
AG11	VSS	AH11	VSS
AG13	NC	AH13	NC
AG14	NC	AH14	NC
AG16	VSS	AH16	VSS
AG17	VSS	AH17	VSS
AG19	VSS	AH19	VSS
AG21	VSS	AH48	PUNIT_ST_ADDR[1]
AG23	VCCABGTS1P8	AH50	CPU0_HFPLL
AG25	VSS	AH51	VSS
AG26	VSS	AH53	OWDTOUT
AG28	VCCAGPIO1P8	AH54	NC
AG29	VCC	AH56	VSS
AG31	VSS	AH57	PSMI_VISA[18]
AG32	VCC	AH59	PSMI_VISA[19]
AG34	VCCRAMCPU0XSI01P05	AH60	VSS
AG36	VCC	AH62	PSMI_VISA[21]
AG38	VSS	AJ2	VSS
AG39	CPU1_THERMDA	AJ4	VSS
AG41	VCCCPU1VIDSI0GT1P05	AJ5	VSS
AG42	VCCCPU1VIDSI0GT1P05	AJ21	TESTHI_1P5_04
AG44	VSS	AJ23	TESTLO_11
AG46	VSS	AJ25	VSS
AG48	PUNIT_ST_ADDR[0]	AJ26	VSS
AG50	CPU1_HFPLL	AJ28	TESTHI_1P5_05
AG51	VSS	AJ29	VSS
AG53	NC	AJ31	VCC
AG54	CPU_IERR	AJ32	VSS
AG56	VSS	AJ34	VCC
AG57	EDM	AJ36	VSS
AG59	THRMTRIPB	AJ38	VCC
AG60	PSMI_VISA[26]	AJ39	VSS
AG63	PSMI_VISA[28]	AJ41	VCC
AG64	PSMI_VISA[27]	AJ42	VSS
AG66	PSMI_VISA[25]	AJ44	VCC
AH1	TESTLO_08	AJ46	VSS
AH3	TESTLO_16	AJ47	VSS
AH4	TESTLO_08	AJ63	PSMI_VISA[22]
AH7	VSS	AJ65	PSMI_VISA[24]

Table 8-2. Ball-out Sorted by Ball Number (Sheet 4 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
AK3	VSS	AL55	VSS
AK5	VSS	AL56	PSMI_VISA[20]
AK20	VSS	AL58	PSMI_VISA[23]
AK62	VSS	AL59	VSS
AK64	VSS	AL62	DDR3_DQ[62]
AK66	VSS	AL63	DDR3_DQ[60]
AL1	VSS	AL65	DDR3_DQ[63]
AL2	TESTLO_16	AM8	VSS
AL4	TESTLO_08	AM9	NC
AL5	TESTLO_05	AM11	NC
AL8	VSS	AM12	VSS
AL9	NC	AM14	NC
AL11	NC	AM15	NC
AL12	VSS	AM17	VSS
AL14	NC	AM18	VSS
AL15	NC	AM20	VSS
AL17	VSS	AM21	TESTHI_1P5_02
AL18	VCCANTB_1P05	AM23	TESTLO_07
AL20	VCCANTB_1P05	AM25	VSS
AL21	VCCANTB_1P05	AM26	VSS
AL23	VCCANTB_1P05	AM28	TESTHI_1P5_03
AL25	VCCANTB_1P05	AM29	VSS
AL26	VCCANTB_1P05	AM31	VCC
AL28	VCCANTB_1P05	AM32	VSS
AL29	VCC	AM34	VCC
AL31	VSS	AM36	VSS
AL32	VCC	AM38	VCC
AL34	VSS	AM39	VSS
AL36	VCC	AM41	VCC
AL38	VSS	AM42	VSS
AL39	VCC	AM44	VSS
AL41	VSS	AM46	VSS
AL42	VCC	AM47	VSS
AL44	VSS	AM49	VSS
AL46	VSS	AM50	VSS
AL47	VCCFHVSOC1P05	AM52	PSMI_VISA[10]
AL49	VCCFHVSOC1P05	AM53	PSMI_VISA[9]
AL50	VSS	AM55	VSS
AL52	PSMI_VISA[16]	AM56	PSMI_VISA[13]
AL53	PSMI_VISA[15]	AM58	PSMI_VISA[12]

Table 8-2. Ball-out Sorted by Ball Number (Sheet 5 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
AM59	VSS	AR17	VSS
AN2	TESTLO_08	AR19	VCCANTB_1P05
AN4	TESTLO_16	AR48	VCCA_DDR3_1P05
AN5	TESTLO_06	AR50	VCCA_DDR3_1P05
AN47	VSS	AR51	VSS
AN62	VSS	AR53	PSMI_VISA[1]
AN63	DDR3_DQS[7]	AR54	PSMI_VISA[4]
AN65	DDR3_DQ[59]	AR56	VSS
AN66	VSS	AR57	PSMI_VISA[7]
AP1	VSS	AR59	PSMI_VISA[11]
AP3	VSS	AR60	PSMI_VISA[8]
AP5	VSS	AR62	VSS
AP20	VCCANTB_1P05	AR63	DDR3_DQ[61]
AP21	VCCANTB_1P05	AR65	DDR3_DQ[58]
AP23	VCCANTB_1P05	AT5	TESTLO_08
AP25	VCCANTB_1P05	AT7	VSS
AP26	VCCANTB_1P05	AT8	NC
AP28	VCCANTB_1P05	AT10	NC
AP29	VCC	AT11	VSS
AP31	VSS	AT13	NC
AP32	VCC	AT14	NC
AP34	VSS	AT16	VSS
AP36	VCCA_DDR3_1P05	AT17	VSS
AP38	VCCA_DDR3_1P05	AT19	VSS
AP39	VCCA_DDR3_1P05	AT21	VCCARP0_1P5
AP41	VCCA_DDR3_1P05	AT23	RP0_RCOMP
AP42	VCCA_DDR3_1P05	AT25	VSS
AP44	VCCA_DDR3_1P05	AT26	VSS
AP46	VCCA_DDR3_1P05	AT28	VCCREFRP0_1P5
AP62	VSS	AT29	VSS
AP64	DDR3_DQSB[7]	AT31	VCC
AR2	TESTLO_08	AT32	VSS
AR4	TESTLO_16	AT34	VCC
AR7	VSS	AT36	VSS
AR8	NC	AT38	VSS
AR10	NC	AT39	VSS
AR11	VSS	AT41	VSS
AR13	VSS	AT42	VSS
AR14	NC	AT44	VSS
AR16	NC	AT46	VSS

Table 8-2. Ball-out Sorted by Ball Number (Sheet 6 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
AT48	VSS	AW8	VSS
AT50	VSS	AW9	RP0_PETP[7]
AT51	VSS	AW11	RP0_PETN[7]
AT53	PSMI_VISA[0]	AW12	VSS
AT54	PSMI_VISA[3]	AW14	NC
AT56	VSS	AW15	NC
AT57	PSMI_VISA[6]	AW17	VSS
AT59	PSMI_VISA[2]	AW19	VSS
AT60	PSMI_VISA[5]	AW20	VSS
AT63	DDR3_DQ[56]	AW21	VCCANTB_1P05
AT64	DDR3_DQ[57]	AW23	VCCANTB_1P05
AT66	VSS	AW25	VSS
AU1	TESTLO_08	AW26	VSS
AU3	TESTLO_16	AW28	VSS
AU4	VSS	AW30	VSS
AU21	VSS	AW31	VSS
AU23	VCCANTB_1P05	AW32	VCCACLK_DDR3_1P05
AU25	VCCANTB_1P05	AW34	VSS
AU26	VCCANTB_1P05	AW36	VSS
AU28	VCCANTB_1P05	AW38	VSS
AU29	VCC	AW39	VSS
AU31	VSS	AW41	VSS
AU32	VCC	AW42	VSS
AU34	VSS	AW44	VSS
AU36	VCCADLL_DDR3_1P05	AW46	VCCADLL_DDR3_1P05
AU38	VCCADLL_DDR3_1P05	AW47	VCCADLL_DDR3_1P05
AU39	VCCADLL_DDR3_1P05	AW49	VSS
AU41	VCCADLL_DDR3_1P05	AW50	VSS
AU42	VCCADLL_DDR3_1P05	AW52	VSS
AU44	VCCADLL_DDR3_1P05	AW53	VSS
AU46	VCCADLL_DDR3_1P05	AW55	VSS
AU47	VCCADLL_DDR3_1P05	AW56	PSMI_VISA[14]
AU62	VSS	AW58	PSMI_VISA[17]
AV2	TESTLO_16	AW59	VSS
AV4	VSS	AW62	DDR3_DQ[51]
AV5	VSS	AW64	DDR3_DQ[53]
AV63	VSS	AW66	VSS
AV65	VSS	AY1	VSS
AW3	VSS	AY2	RP0_PERP[7]
AW5	VSS	AY4	RP0_PERN[7]

Table 8-2. Ball-out Sorted by Ball Number (Sheet 7 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
AY5	RP0_PERN[6]	B44	LPC_CLKOUT[0]
AY8	VSS	B46	VSS
AY9	RP0_PETN[6]	B48	UART_RI_N
AY11	RP0_PETP[6]	B50	VSS
AY12	VSS	B53	NC
AY14	VSS	B55	GPIOCORE[11]
AY15	VSS	B57	GPIOCORE[8]
AY19	VSS	BA17	VSS
AY21	VCCANTB_1P05	BA21	VSS
AY23	VCCANTB_1P05	BA23	VSS
AY29	VSS	BA25	DDR3_DQ[17]
AY30	VSS	BA26	VSS
AY37	VSS	BA29	DDR3_DQ[22]
AY38	VCCPLL_DDR3_1P05	BA30	VSS
AY45	VSS	BA32	VCCACLK_DDR3_1P05
AY46	VSS	BA34	VCCSFRPLL_DDR3_1P5
AY52	VSS	BA37	VSS
AY53	VSS	BA38	VCCPLL_DDR3_1P05
AY55	VSS	BA41	VCCCLK_DDR3_1P5
AY56	VSS	BA42	VSS
AY58	VSS	BA45	VSS
AY59	VSS	BA46	VSS
AY62	VSS	BA49	VSS
AY63	DDR3_DQ[52]	BA50	DDR3_ECC[5]
AY65	DDR3_DQ[49]	BB2	RP0_PERN[5]
B10	TESTLO_15	BB4	RP0_PERP[5]
B12	TESTLO_04	BB5	RP0_PERP[6]
B14	VSS	BB17	RP0_PETN[1]
B17	TESTLO_15	BB19	RP0_PETN[0]
B19	TESTLO_04	BB25	DDR3_DQ[21]
B21	TESTLO_04	BB26	DDR3_DQ[19]
B23	VSS	BB32	VSS
B26	TESTLO_04	BB34	VCCSFRPLL_DDR3_1P5
B28	DFX_GPIO_GRP0[2]	BB41	VCCCLK_DDR3_1P5
B30	DFX_GPIO_GRP0[3]	BB42	VSS
B32	VSS	BB49	DDR3_ECC[1]
B35	DFX_GPIO_GRP1[4]	BB50	VSS
B37	VSS	BB53	VSS
B39	RSVD_MVT[0]	BB54	VSS
B41	TESTLO_00	BB56	VSS

Table 8-2. Ball-out Sorted by Ball Number (Sheet 8 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
BB57	DDR3_DQ[44]	BD30	VSS
BB59	DDR3_DQ[41]	BD32	VSS
BB60	DDR3_DQ[45]	BD34	VSS
BB62	VSS	BD37	VCC_DDR3_1P5
BB63	DDR3_DQS[6]	BD38	VCC_DDR3_1P5
BB65	DDR3_DQSB[6]	BD41	DDR3_CK[0]
BB66	VSS	BD42	DDR3_CKB[0]
BC1	VSS	BD45	VCC_DDR3_1P5
BC3	VSS	BD46	VSS
BC5	VSS	BD49	DDR3_ECC[4]
BC7	VSS	BD50	DDR3_ECC[3]
BC8	RP0_PETP[5]	BD53	VSS
BC10	RP0_PETN[5]	BD54	VSS
BC11	VSS	BD59	VSS
BC13	VSS	BD60	DDR3_DQ[43]
BC15	VSS	BD62	VSS
BC21	VSS	BD63	DDR3_DQ[54]
BC23	VSS	BD65	DDR3_DQ[48]
BC29	VSS	BE5	RP0_CLKINP
BC30	VSS	BE17	VSS
BC37	VSS	BE19	VSS
BC38	DDR3_DRAMRSTB	BE25	VSS
BC45	VSS	BE26	DDR3_DQS[2]
BC46	VSS	BE32	VCC_DDR3_1P5
BC62	VSS	BE34	VCC_DDR3_1P5
BC64	DDR3_DQ[55]	BE41	VCC_DDR3_1P5
BD2	RP0_PERP[4]	BE42	VCC_DDR3_1P5
BD4	RP0_PERN[4]	BE49	DDR3_DQSECC
BD7	VSS	BE50	VSS
BD8	RP0_PETN[4]	BE57	DDR3_DQ[47]
BD10	RP0_PETP[4]	BE63	VSS
BD13	DDR3_DQ[6]	BE64	DDR3_DQ[50]
BD15	VSS	BE66	VSS
BD17	RP0_PETP[1]	BF1	RP0_PERN[3]
BD19	RP0_PETP[0]	BF3	RP0_PERP[3]
BD21	VSS	BF4	RP0_CLKINN
BD23	VSS	BF13	DDR3_DQ[7]
BD25	VSS	BF15	VSS
BD26	DDR3_DQSB[2]	BF21	DDR3_DQ[1]
BD29	VSS	BF23	VSS

Table 8-2. Ball-out Sorted by Ball Number (Sheet 9 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
BF29	VSS	BG66	VSS_NCTF
BF30	VSS	BH3	RP0_PERP[2]
BF37	DDR3_MON2P	BH5	VSS
BF38	DDR3_MON2N	BH8	RP0_PETP[2]
BF45	DDR3_CLKREFN	BH11	VSS
BF46	VSS	BH17	DDR3_DQSB[0]
BF53	VSS	BH19	DDR3_DQ[3]
BF54	VSS	BH25	DDR3_DQ[16]
BF62	DDR3_DQSB[5]	BH26	DDR3_DQ[20]
BG1	VSS_NCTF	BH32	DDR3_ODTPU
BG4	VSS	BH34	DDR3_CMDPU
BG5	VSS	BH41	DDR3_VREF
BG8	RP0_PETP[3]	BH42	DDR3_DRAM_PWROK
BG9	RP0_PETN[3]	BH49	DDR3_ECC[6]
BG11	VSS	BH50	VSS
BG13	DDR3_DQ[0]	BH57	DDR3_DQ[46]
BG15	DDR3_DQ[2]	BH58	DDR3_DQ[40]
BG17	DDR3_DQS[0]	BH60	VSS
BG19	DDR3_DQ[4]	BH62	DDR3_DQS[5]
BG21	DDR3_DQ[5]	BH64	VSS
BG23	VSS	BJ1	VSS_NCTF
BG25	DDR3_DQ[18]	BJ4	RP0_PERN[2]
BG26	VSS	BJ62	VSS
BG29	DDR3_DQ[23]	BJ63	VSS
BG30	VSS	BJ66	VSS_NCTF
BG32	DDR3_SYSPWRGOOD	BK1	VSS_NCTF
BG34	DDR3_DQPU	BK3	VSS_NCTF
BG37	DDR3_MON1P	BK5	VSS_NCTF
BG38	DDR3_MON1N	BK6	VSS
BG41	DDR3_CK[1]	BK8	VSS
BG42	DDR3_CKB[1]	BK9	RP0_PETN[2]
BG45	DDR3_CLKREFP	BK10	VSS
BG46	VSS	BK12	VSS
BG49	DDR3_DQSECCB	BK13	VSS
BG50	DDR3_ECC[0]	BK15	VSS
BG53	VSS	BK17	VSS
BG54	VSS	BK18	VSS
BG57	VSS	BK19	VSS
BG58	DDR3_DQ[42]	BK21	VSS
BG63	VSS	BK22	VSS

Table 8-2. Ball-out Sorted by Ball Number (Sheet 10 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
BK24	VSS	BL28	DDR3_DQ[29]
BK26	VSS	BL30	VSS
BK27	VSS	BL32	DDR3_MA[12]
BK28	VSS	BL34	DDR3_MA[11]
BK30	VSS	BL35	DDR3_MA[7]
BK31	VSS	BL37	DDR3_MA[3]
BK32	VCC_DDR3_1P5	BL39	DDR3_MA[1]
BK35	VCC_DDR3_1P5	BL41	DDR3_BS[1]
BK36	VSS	BL43	DDR3_BS[0]
BK37	VCC_DDR3_1P5	BL44	DDR3_WEB
BK39	VCC_DDR3_1P5	BL46	DDR3_CKE[0]
BK40	DDR3_MA[0]	BL48	DDR3_ODT[0]
BK42	VSS	BL50	VSS
BK44	VCC_DDR3_1P5	BL52	VSS
BK45	DDR3_CKE[1]	BL53	DDR3_DQ[38]
BK46	VCC_DDR3_1P5	BL55	DDR3_DQS[4]
BK48	VSS	BL57	DDR3_DQ[36]
BK49	DDR3_ECC[7]	BL59	DDR3_DQ[37]
BK51	DDR3_ECC[2]	BL61	VSS
BK53	VSS	BM1	VSS_NCTF
BK54	VSS	BM3	RP0_PLLMON1
BK56	VSS	BM5	RP0_PLLMON0
BK57	VSS	BM7	RP0_PERN[1]
BK58	VSS	BM9	RP0_PERN[0]
BK60	VSS	BM13	DDR3_DQ[8]
BK62	VSS_NCTF	BM16	DDR3_DQSB[1]
BK64	VSS_NCTF	BM18	DDR3_DQ[11]
BK66	VSS_NCTF	BM22	DDR3_DQ[24]
BL7	RP0_PERP[1]	BM25	DDR3_DQSB[3]
BL8	VSS	BM27	DDR3_DQ[27]
BL10	VSS	BM31	DDR3_MA[14]
BL12	VSS	BM34	DDR3_MA[9]
BL14	DDR3_DQ[14]	BM36	VCC_DDR3_1P5
BL16	VSS	BM40	VCC_DDR3_1P5
BL17	DDR3_DQ[15]	BM43	VCC_DDR3_1P5
BL19	DDR3_DQ[9]	BM45	VCC_DDR3_1P5
BL21	VSS	BM49	VCC_DDR3_1P5
BL23	DDR3_DQ[30]	BM52	DDR3_DQ[32]
BL25	VSS	BM54	DDR3_DQ[39]
BL26	DDR3_DQ[31]	BM58	DDR3_DQ[33]

Table 8-2. Ball-out Sorted by Ball Number (Sheet 11 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
BM61	VSS	BP37	DDR3_MA[6]
BM62	VSS_NCTF	BP40	DDR3_MA[2]
BM64	VSS_NCTF	BP43	DDR3_RASB
BM66	VSS_NCTF	BP46	DDR3_CSB[1]
BN10	RP0_PERP[0]	BP49	DDR3_ODT[1]
BN12	VSS	BP52	VSS
BN14	DDR3_DQ[10]	BP55	VSS
BN17	DDR3_DQS[1]	BP58	VSS
BN19	DDR3_DQ[13]	BP59	VSS_NCTF
BN21	VSS	BP61	VSS_NCTF
BN23	DDR3_DQ[26]	BP62	VSS_NCTF
BN26	DDR3_DQS[3]	BP64	VSS_NCTF
BN28	DDR3_DQ[25]	BP66	VSS_NCTF
BN30	VSS	C3	VSS_NCTF
BN32	DDR3_BS[2]	C5	VSS_NCTF
BN35	DDR3_MA[8]	C6	VSS
BN37	DDR3_MA[5]	C9	VSS
BN39	DDR3_MA[4]	C13	VSS
BN41	DDR3_MA[10]	C15	TESTLO_15
BN44	DDR3_CSB[0]	C18	VSS
BN46	DDR3_CASB	C22	VSS
BN48	DDR3_MA[13]	C24	TESTLO_15
BN50	VSS	C27	VSS
BN53	DDR3_DQ[34]	C31	DFX_GPIO_GRP1[6]
BN55	DDR3_DQSB[4]	C33	DFX_GPIO_GRP1[0]
BN57	DDR3_DQ[35]	C36	CPU0_SFRANAD
BP1	VSS_NCTF	C40	SPI_CSB[0]
BP3	VSS_NCTF	C42	LPC_CLKRUN_B
BP5	VSS_NCTF	C45	LPC_CLKOUT[1]
BP6	VSS_NCTF	C49	UART_CTS_N
BP8	VSS_NCTF	C51	ERR[2]
BP10	VSS	C54	VSS
BP13	DDR3_DQ[12]	C58	VSS
BP16	VSS	C60	VSS
BP19	VSS	C62	VSS_NCTF
BP22	DDR3_DQ[28]	C64	VSS_NCTF
BP25	VSS	C66	VSS_NCTF
BP28	VSS	D6	VSS
BP31	DDR3_MA[15]	D8	VSS
BP34	VCC_DDR3_1P5	D10	TESTLO_04

Table 8-2. Ball-out Sorted by Ball Number (Sheet 12 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
D12	TESTLO_04	E21	TESTLO_04
D14	VSS	E22	VSS
D15	TESTLO_04	E23	TESTLO_04
D17	TESTLO_04	E25	VSS
D19	TESTLO_15	E27	VSS
D21	TESTLO_15	E28	DFX_GPIO_GRP0[6]
D23	TESTLO_15	E30	VSS
D24	TESTLO_15	E31	DFX_GPIO_GRP1[5]
D26	TESTLO_04	E32	VSS
D28	DFX_GPIO_GRP0[1]	E34	VSS
D30	DFX_GPIO_GRP0[0]	E36	CPU_EXTBGREF
D32	VSS	E37	VSS
D33	DFX_GPIO_GRP1[1]	E39	SPI_CSB[1]
D35	CPU1_SFRANAD	E40	SPI_MISO
D37	VSS	E41	VSS
D39	VSS	E43	VSS
D41	VSS	E45	VSS
D42	SPI_MOSI	E46	VSS
D44	LPC_FRAME_B	E48	UART_TXD
D46	VSS	E49	TESTLO_13
D48	UART_RXD	E50	VSS
D50	VSS	E52	BOOTDEVSEL
D51	ERR[1]	E54	VSS
D53	GPIOCORE[3]	E55	GPIOCORE[6]
D55	GPIOCORE[7]	E57	GPIOCORE[13]
D57	GPIOCORE[10]	E58	VSS
D59	VSS	E59	GPIOCORE[14]
D60	VSS	E61	VSS
E1	VSS_NCTF	E62	VSS_NCTF
E3	VSS_NCTF	E64	VSS_NCTF
E5	VSS_NCTF	E66	VSS_NCTF
E7	VSS	F1	HPLL_MONP
E9	VSS	F4	VSS
E10	TESTLO_15	F5	TESTLO_04
E12	TESTLO_15	F63	VSS
E13	VSS	F66	VSS_NCTF
E14	VSS	G3	VSS
E16	VSS	G5	TESTLO_15
E18	VSS	G7	VSS
E19	TESTLO_15	G9	TESTLO_04

Table 8-2. Ball-out Sorted by Ball Number (Sheet 13 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
G10	VSS	H54	GPIOCORE[5]
G17	NC	H56	GPIOCORE[16]
G18	NC	H58	VSS
G25	NC	H59	GPIOCORE[18]
G26	NC	H62	VSS
G32	DFX_GPIO_GRP1[7]	H63	VSS
G34	DFX_GPIO_GRP1[2]	H66	VSS_NCTF
G41	LPC_AD[1]	J5	VSS
G42	LPC_AD[0]	J13	NC
G48	VSS	J14	TESTLO_02
G50	VSS	J21	NC
G56	VSS	J22	NC
G59	VSS	J29	VSS
G62	GPIOCORE[12]	J30	DFX_GPIO_GRP0[7]
G64	GPIOCORE[15]	J37	THRMB
H1	HPLL_MONN	J38	SPI_SCLK
H4	VSS	J44	UART_DSR_N
H9	TESTLO_15	J46	LPC_SERIRQ
H10	TESTLO_04	J52	VSS
H13	NC	J54	VSS
H14	TESTLO_01	J63	PWROK
H17	NC	J64	RTC_INTVRMEN
H18	NC	J66	VSS
H21	VSS	K1	VSS_NCTF
H22	VSS	K3	TESTLO_04
H25	NC	K4	TESTLO_15
H26	NC	K10	TESTLO_15
H29	VSS	K17	VSS
H30	DFX_GPIO_GRP0[5]	K18	VSS
H32	DFX_GPIO_GRP0[4]	K25	VSS
H34	DFX_GPIO_GRP1[3]	K26	VSS
H37	RSVD_MVT[1]	K32	VSS
H38	SPKR	K34	VSS
H41	LPC_AD[3]	K41	VSS
H42	LPC_AD[2]	K42	VSS
H44	VSS	K48	GPIOCORE[2]
H46	UART_DCD_N	K50	GPIOCORE[1]
H48	ERR[0]	K62	GPIOSUS[6]
H50	UART_RTS_N	L2	TESTLO_04
H52	GPIOCORE[4]	L4	TESTLO_15

Table 8-2. Ball-out Sorted by Ball Number (Sheet 14 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
L5	VSS	M52	GPIOSUS[0]
L7	VSS	M54	RSTRDYB
L8	VSS	M56	GPIOSUS[2]
L13	VSS	M57	VSS
L14	VSS	M59	GPIOSUS[4]
L17	NC	M60	GPIOSUS[5]
L18	NC	M62	VSS
L21	NC	M64	VSS
L22	NC	M66	VSS
L25	NC	N1	VSS_NCTF
L26	NC	N2	TESTLO_12
L29	VSS	N4	TESTLO_17
L30	VSS	N5	TESTLO_17
L32	VCCAGPIO1P8	N7	VSS
L34	VSS	N8	NC
L37	VSS	N10	NC
L38	VSS	N11	VSS
L41	VCCSUS1P8	N13	NC
L42	VCCSUS3P3	N14	NC
L44	VSS	N17	NC
L46	VSS	N18	NC
L48	VSS	N25	NC
L50	VSS	N26	NC
L52	GPIOCORE[19]	N32	VCCAGPIO1P8
L54	GPIOCORE[17]	N34	VSS
L57	VSS	N41	VCCSUS1P8
L59	GPIOSUS[1]	N42	VCCSUS3P3
L60	GPIOSUS[7]	N48	GPIOCORE[20]
L63	RSMRSTB	N50	GPIOSUS[8]
L65	RTC_EXTPAD	N62	RTC_SRTCRSTB
M3	VSS	N63	VSS
M5	VSS	N65	RTC_X2PAD
M21	VSS	P17	VSS
M22	VSS	P18	VSS
M29	VSS	P21	SOC_THERMDC
M30	VSS	P22	SOC_THERMANATP[1]
M37	VCCAGPIO3P3	P25	VSS
M38	HV_GPIO_RCOMP	P26	VSS
M44	VCCRTC3P3	P29	VSS
M46	GPIOCORE[9]	P30	VSS

Table 8-2. Ball-out Sorted by Ball Number (Sheet 15 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
P32	VCCAGPIO1P8	T17	VSS
P34	MV_GPIO_RCOMP	T18	SOC_THERMANATP[0]
P37	VCCAGPIO3P3	T20	VSS
P38	VSS	T21	VSS
P41	VCCSUS1P8	T23	VSS
P42	VCCSUS3P3	T25	VSS
P44	VCCRTC3P3	T26	VSS
P46	HPET_CLK14IN	T28	VSS
P48	VCCSUS1P05	T29	VSS
P50	GPIOSUS[3]	T31	VSS
R2	TESTLO_12	T32	VCCAGPIO1P8
R4	TESTLO_17	T34	VSS
R5	TESTLO_12	T36	VCCAGPIO3P3
R8	VSS	T37	VSS
R9	NC	T39	VSS
R11	NC	T41	VSS
R12	VSS	T42	VCCSUS3P3
R14	NC	T44	VCCRTC3P3
R15	NC	T45	VSS
R21	SOC_THERMDA	T47	VCCSUS1P05
R22	SOC_THERMREFNPAD	T48	VCCSUS1P05
R29	VSS	T50	VSS
R30	VSS	T52	SUSCLK
R37	VCCAGPIO3P3	T53	RSTWARN
R38	VSS	T55	VSS
R44	VCCRTC3P3	T56	WAKE_B
R46	VSS	T58	RESETB
R52	VSS	T59	VSS
R53	VSS	T62	VSS
R55	VSS	T64	VSS
R56	SLPMODE	U2	TESTLO_12
R58	SLPRDYB	U4	TESTLO_17
R59	VSS	U8	VSS
R62	RTCRESETB	U9	NC
R63	LPCCLK0_DS	U11	NC
R65	RTC_X1PAD	U12	VSS
R66	VSS	U14	NC
T1	VSS	U15	NC
T3	VSS	U62	VCCCPU0VIDSI01P05
T5	VSS	U63	VCCCPU0VIDSI01P05

Table 8-2. Ball-out Sorted by Ball Number (Sheet 16 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
U65	VCCCPU0VIDSI01P05	W31	VSS
V5	TESTLO_17	W32	VCC
V20	HPLL_CLKREFN	W34	VSS
V21	HPLL_CLKREFP	W36	VCC
V23	VSS	W38	VSS
V25	VSS	W39	VCC
V26	VSS	W41	VSS
V28	VSS	W42	VCC
V29	VSS	W44	VCCCPU0VIDSI01P05
V31	VSS	W46	VCCCPU0VIDSI01P05
V32	VCCAGPIO1P8	W48	VCCCPU0VIDSI01P05
V34	VSS	W50	VCCCPU0VIDSI01P05
V36	VCCAGPIO3P3	W51	VSS
V38	VSS	W53	VCCCPU0VIDSI01P05
V39	VSS	W54	VCCCPU0VIDSI01P05
V41	VSS	W56	VSS
V42	VSS	W57	VCCCPU0VIDSI01P05
V44	VSS	W59	VCCCPU0VIDSI01P05
V46	VSS	W60	VSS
V63	VCCCPU0VIDSI01P05	W62	VSS
V64	VCCCPU0VIDSI01P05	Y2	TESTLO_10
V66	VCCCPU0VIDSI01P05	Y4	VSS
W1	TESTLO_09	Y5	VSS
W3	VSS	Y7	VSS
W4	TESTLO_12	Y8	NC
W7	VSS	Y10	VSS
W8	NC	Y11	SMBH_CLK
W10	VSS	Y13	SMBM_CLK
W11	SMBD_CLK	Y14	VSS
W13	SMBH_DATA	Y16	VSS
W14	VSS	Y17	VSS
W16	SMBM_DATA	Y19	VSS
W17	SMBD_DATA	Y48	VCCCPU0VIDSI01P05
W19	VSS	Y50	VCCCPU0VIDSI01P05
W21	VSS	Y51	VSS
W23	VSS	Y53	VCCCPU0VIDSI01P05
W25	VSS	Y54	VCCCPU0VIDSI01P05
W26	VSS	Y56	VSS
W28	VSS	Y57	VCCCPU0VIDSI01P05
W29	VSS	Y59	VCCCPU0VIDSI01P05

Table 8-2. Ball-out Sorted by Ball Number (Sheet 17 of 17)

Signal Name	Ball Number	Signal Name	Ball Number
Y60	VSS	Y65	VSS
Y63	VSS		

8.3 Ball Map

The ball map is divided into eight sections. The sections are defined in Figure 8-1 below. The eight sections are show as eight separate figures, from Figure 8-2, “Ball Map - Part 1 of 8” through Figure 8-9, “Ball Map - Part 8 of 8”.

Figure 8-1. Ball Map

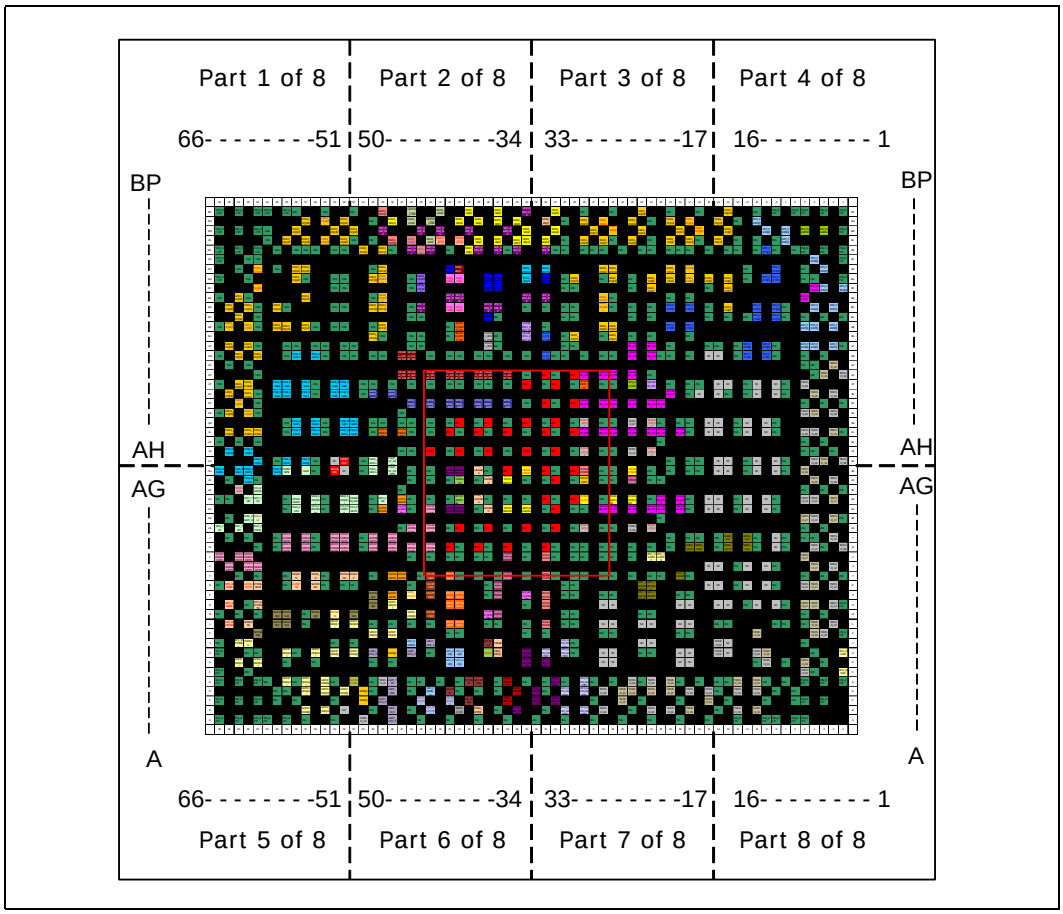


Figure 8-2. Ball Map - Part 1 of 8

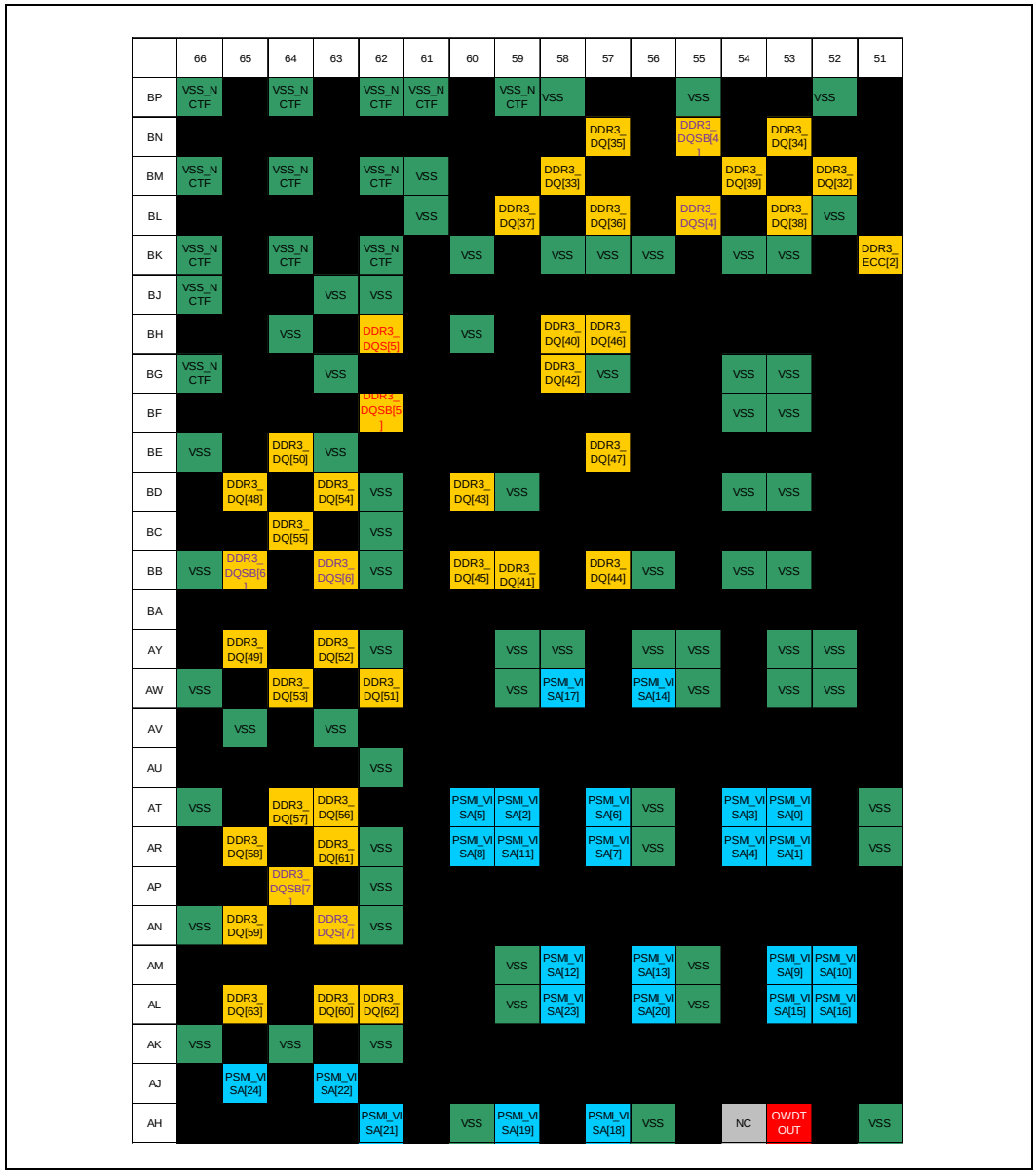


Figure 8-3. Ball Map - Part 2 of 8

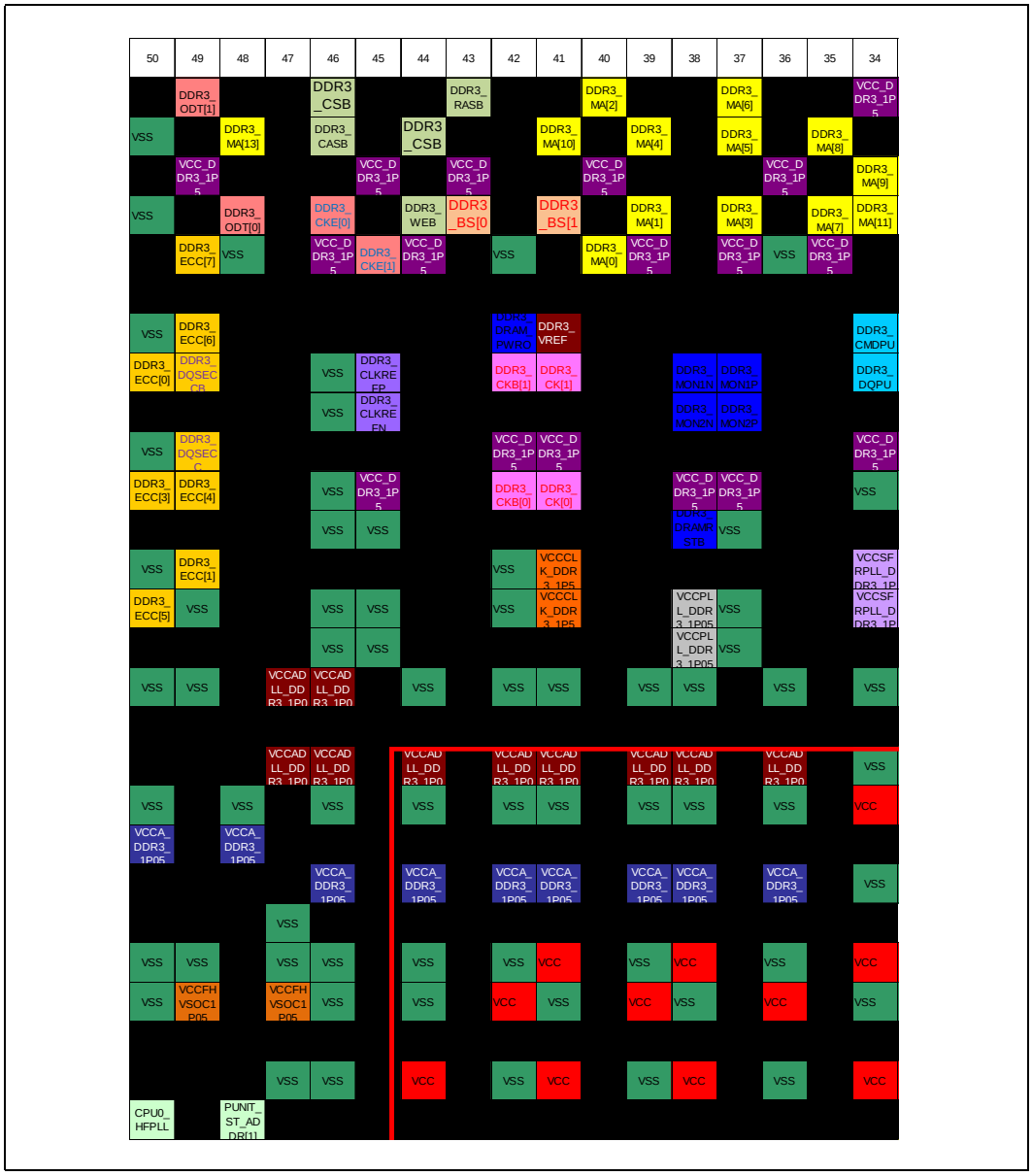


Figure 8-4. Ball Map - Part 3 of 8

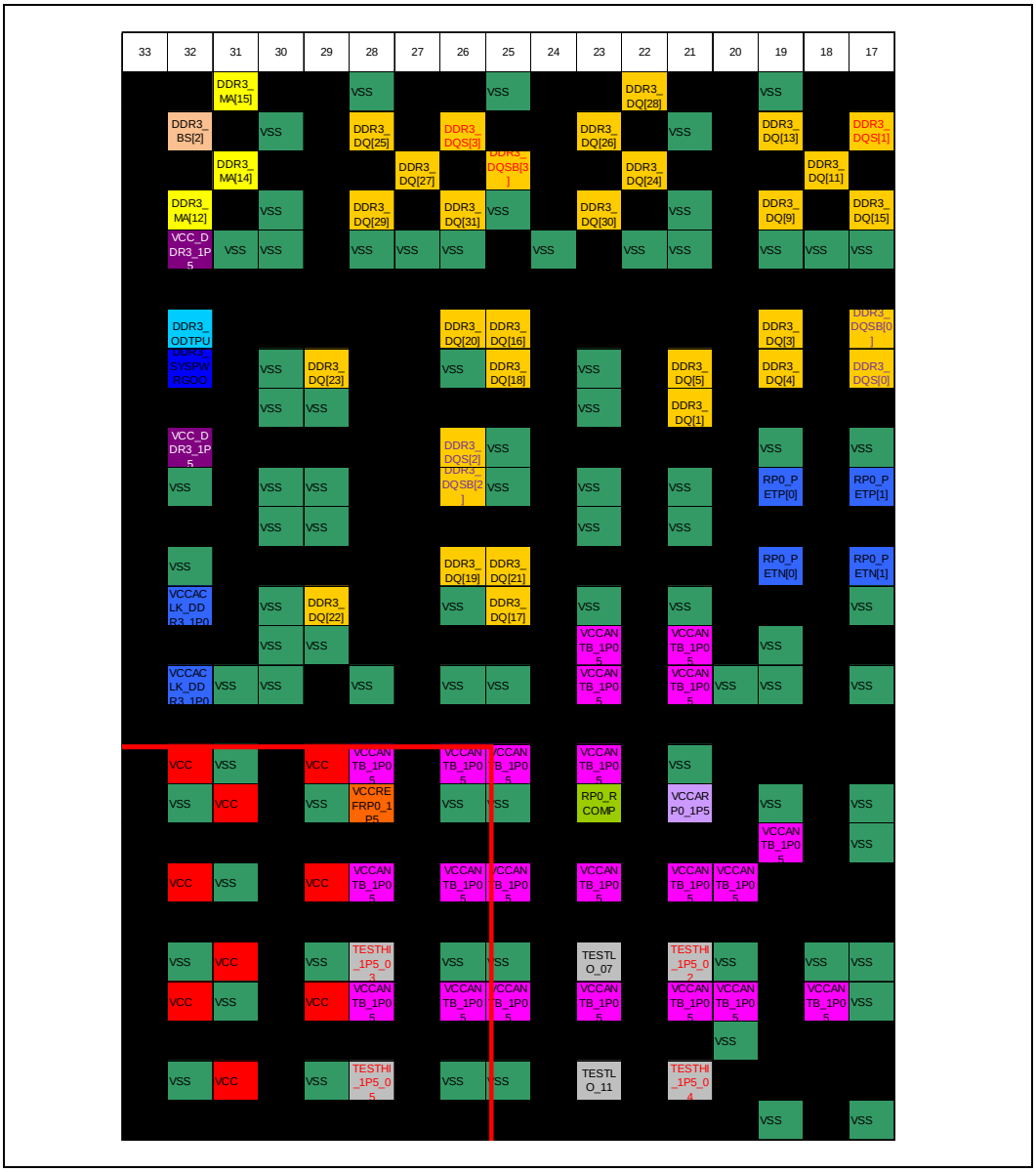
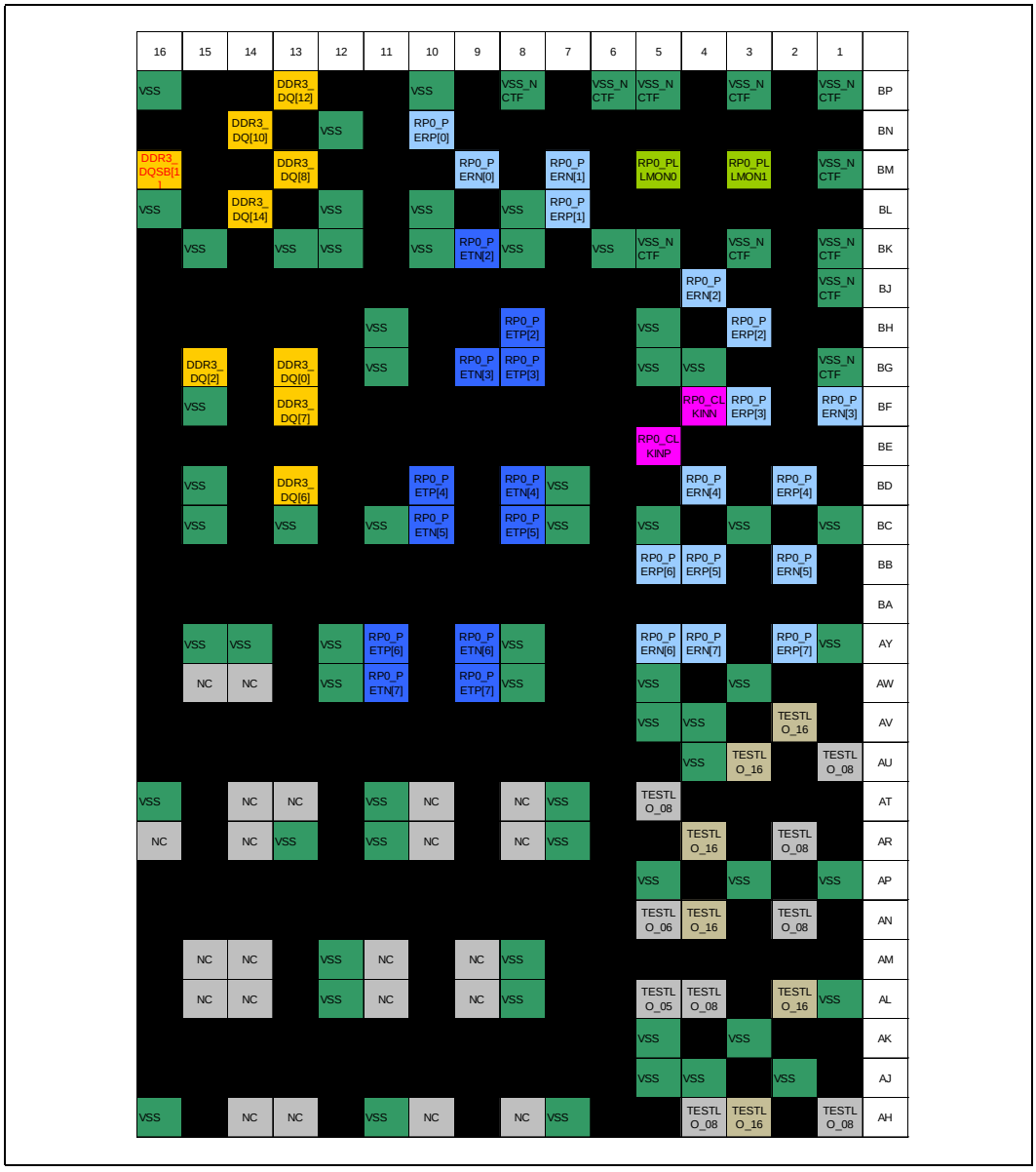


Figure 8-5. Ball Map - Part 4 of 8



16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VSS			DDR3_DQ[12]			VSS		VSS_NCTF		VSS_NCTF	VSS_NCTF		VSS_NCTF		VSS_NCTF	BP
		DDR3_DQ[10]		VSS		RP0_PERP[0]										BN
DDR3_DQSB[1]			DDR3_DQ[8]				RP0_PERN[0]		RP0_PERN[1]		RP0_PLLMON0		RP0_PLLMON1		VSS_NCTF	BM
VSS		DDR3_DQ[14]		VSS		VSS		VSS	RP0_PERP[1]							BL
	VSS		VSS	VSS		VSS	RP0_PETN[2]	VSS		VSS	VSS_NCTF		VSS_NCTF		VSS_NCTF	BK
												RP0_PERN[2]			VSS_NCTF	BJ
					VSS			RP0_PETP[2]			VSS		RP0_PERP[2]			BH
	DDR3_DQ[2]		DDR3_DQ[0]		VSS		RP0_PETN[3]	RP0_PETP[3]			VSS	VSS			VSS_NCTF	BG
	VSS		DDR3_DQ[7]									RP0_CLKINN	RP0_PERP[3]		RP0_PERN[3]	BF
											RP0_CLKINP					BE
	VSS		DDR3_DQ[6]			RP0_PETP[4]		RP0_PETN[4]	VSS			RP0_PERN[4]		RP0_PERP[4]		BD
	VSS		VSS		VSS	RP0_PETN[5]		RP0_PETP[5]	VSS		VSS		VSS		VSS	BC
											RP0_PERP[6]	RP0_PERP[5]		RP0_PERN[5]		BB
																BA
	VSS	VSS		VSS	RP0_PETP[6]		RP0_PETN[6]	VSS			RP0_PERN[6]	RP0_PERN[7]		RP0_PERP[7]	VSS	AY
	NC	NC		VSS	RP0_PETN[7]		RP0_PETP[7]	VSS			VSS		VSS			AW
											VSS	VSS		TESTLO_16		AV
												VSS	TESTLO_16		TESTLO_08	AU
VSS		NC	NC		VSS	NC		NC	VSS		TESTLO_08					AT
NC		NC	VSS		VSS	NC		NC	VSS			TESTLO_16		TESTLO_08		AR
											VSS		VSS		VSS	AP
											TESTLO_06	TESTLO_16		TESTLO_08		AN
	NC	NC		VSS	NC		NC	VSS								AM
	NC	NC		VSS	NC		NC	VSS			TESTLO_05	TESTLO_08		TESTLO_16	VSS	AL
											VSS		VSS			AK
											VSS	VSS		VSS		AJ
VSS		NC	NC		VSS	NC		NC	VSS			TESTLO_08	TESTLO_16		TESTLO_08	AH

Figure 8-6. Ball Map - Part 5 of 8

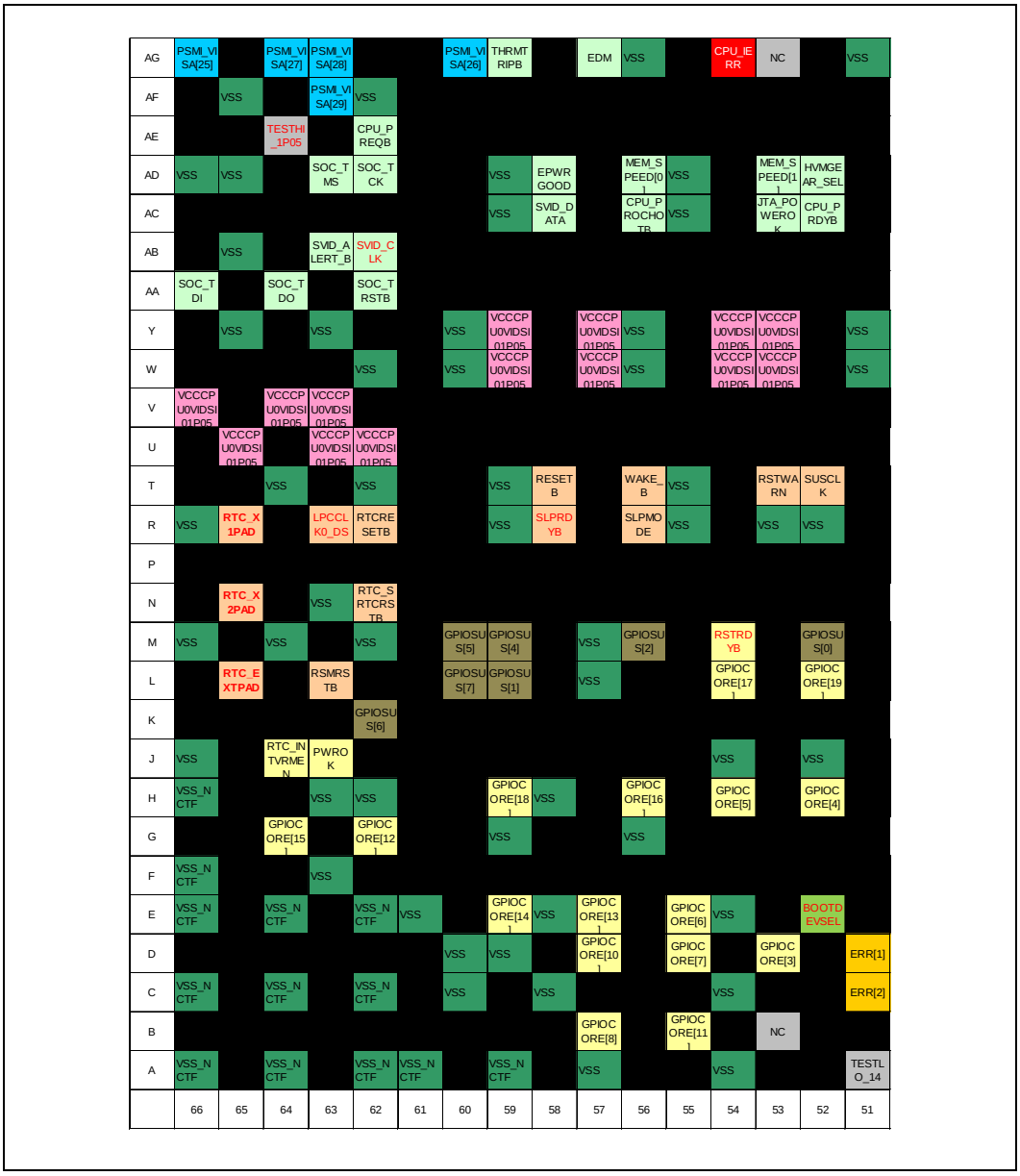


Figure 8-7. Ball Map - Part 6 of 8

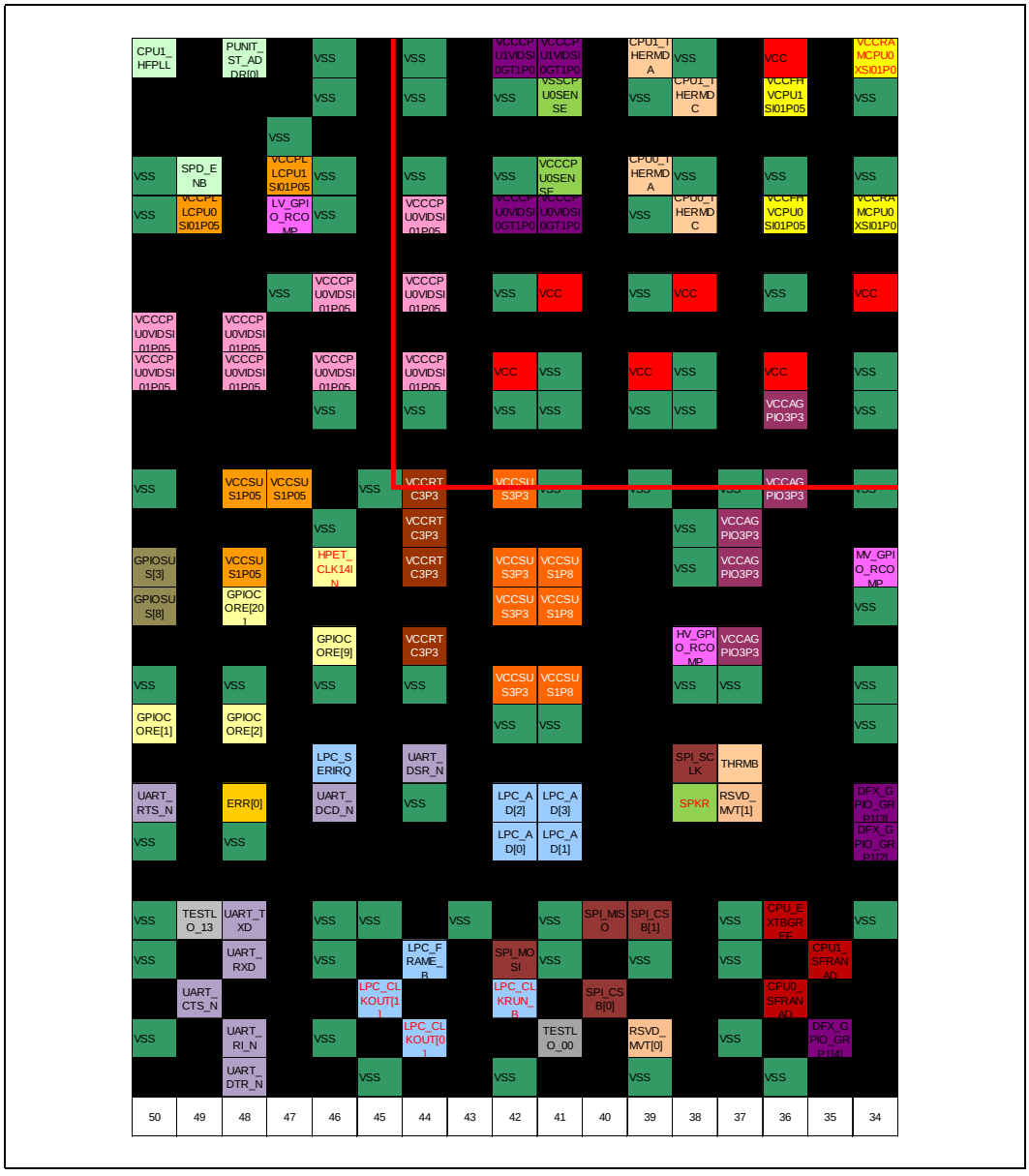


Figure 8-8. Ball Map - Part 7 of 8

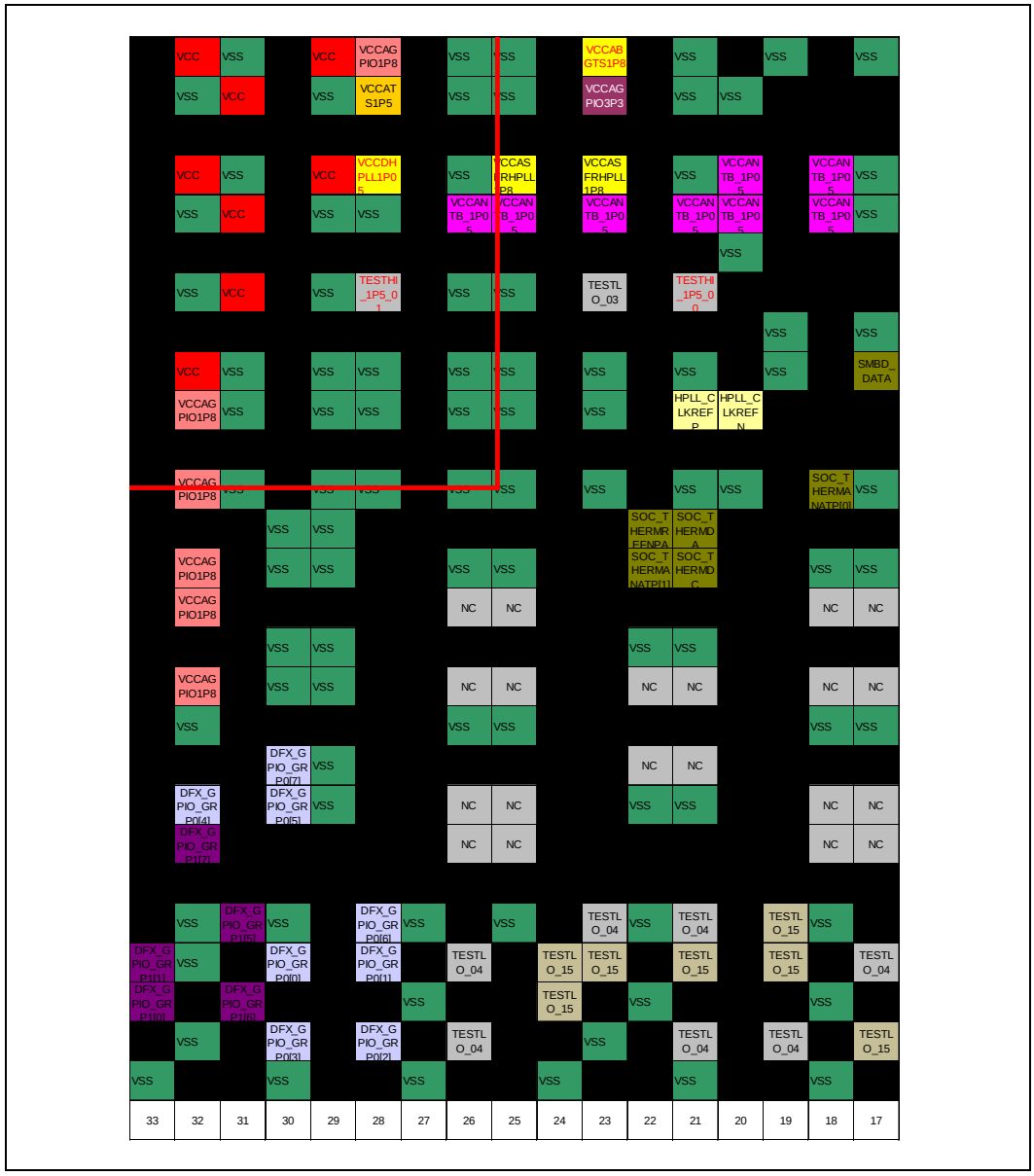
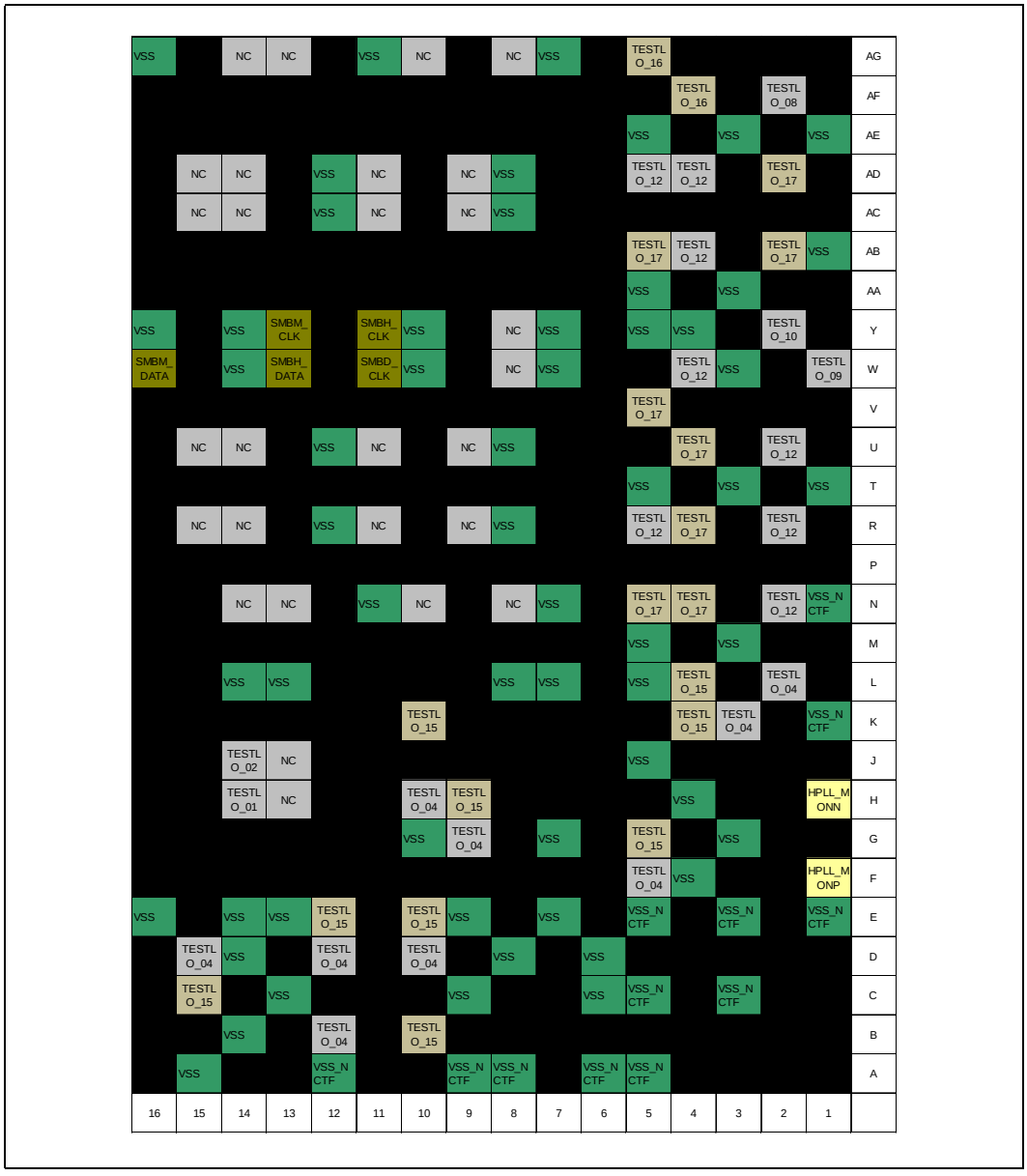


Figure 8-9. Ball Map - Part 8 of 8



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9 Mechanical

The S12x0 is manufactured as a 34mm x 28mm Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with 1283 solder balls on the bottom side. Capacitors are placed on the package top side in the area surrounding the die. Because die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out zone, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

While package drawings are shown in this chapter, refer to the *Intel® Atom™ Processor S1200 Product Family for Microserver Thermal and Mechanical Design Guide* for details on package mechanical dimensions and tolerance, as well as other key package attributes. The drawings shown here are for informational purposes and not meant to be the control documents for mechanical details of the package.

Dimensions:

- Package parameters: 34 mm x 28 mm
- Ball Count: 1283

Figure 9-1. Topside Showing Capacitors and Marking Areas

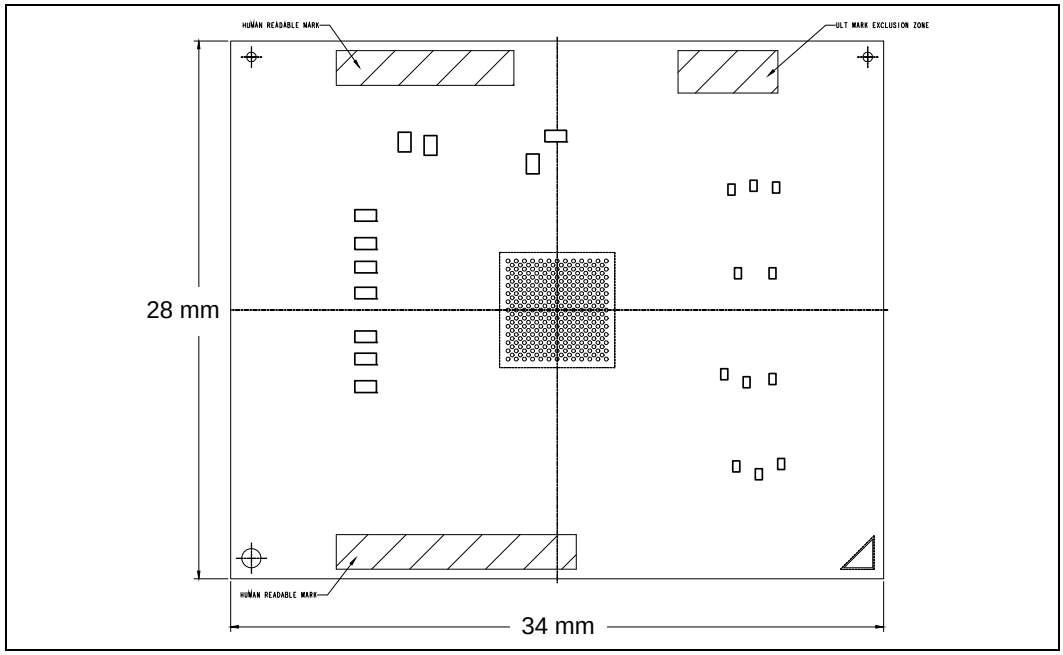
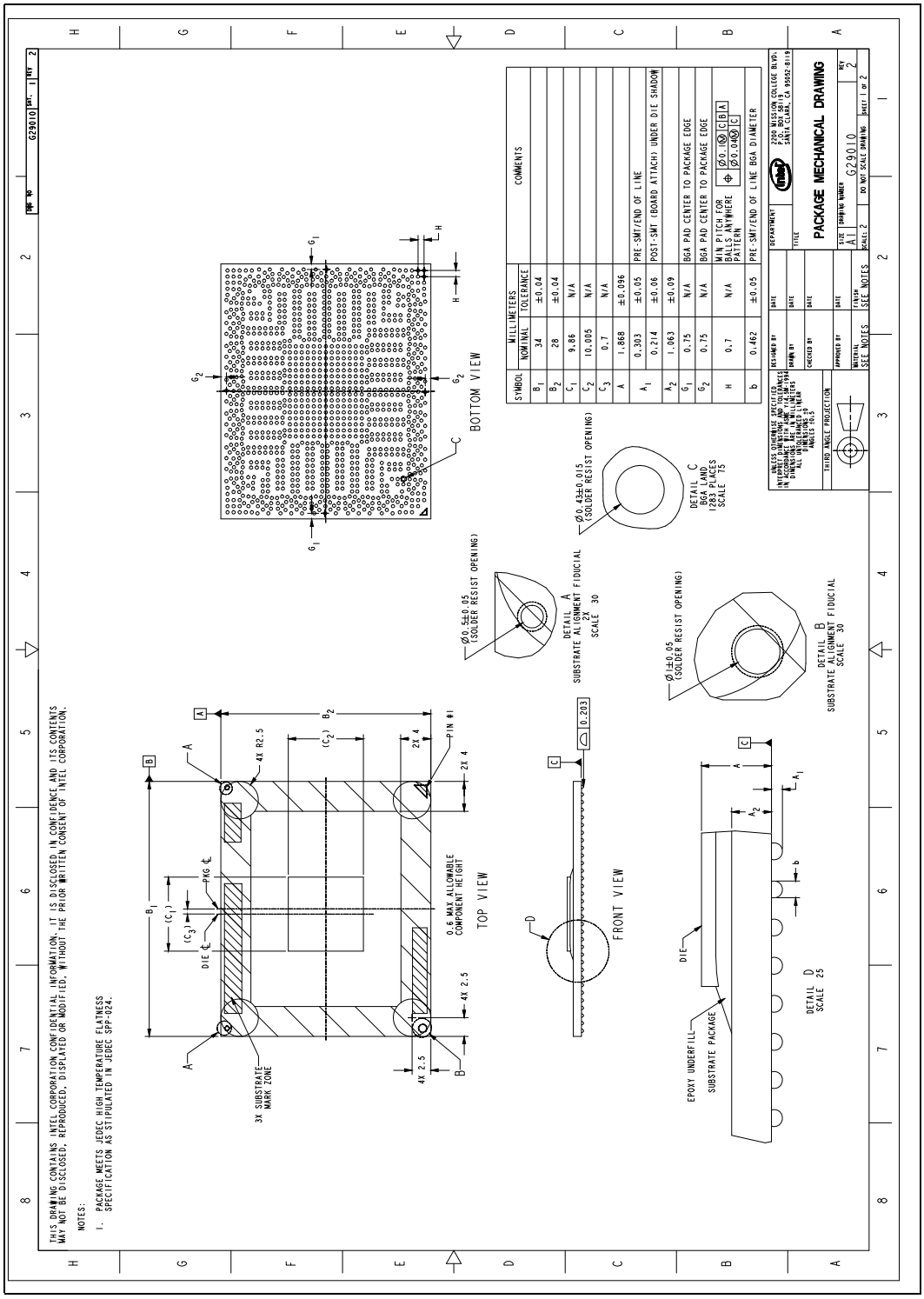


Figure 9-2. Package Mechanical Drawing



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