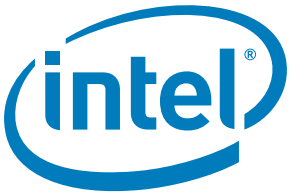

Intel® Atom™ Processor Z3600 and Z3700 Series

Datasheet (Volume 2 of 2)

For Volume 1 of 2 refer to Document ID: 329474-003

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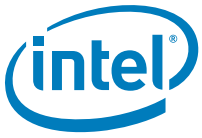
Revision 003

Document Number: 329518-003



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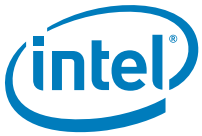

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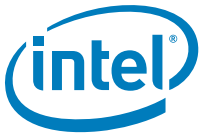

Revision History

Document Number	Revision Number	Description	Revision Date
329518	001	• Initial release	September 2013
329518	002	• Title change and revision update	April 2014
329518	003	• Revision Update only	February 2015

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1 Register Access Methods

Note: Throughout this document Intel® Atom™ Processor Z3600 and Z3700 Series is referred as Processor or SoC.

There are six different common register access methods:

- Fixed IO Register Access
- Fixed Memory Mapped Register Access
- IO Referenced Register Access
- Memory Referenced Register Access
- PCI Configuration Register Access (Indirect - via Memory or IO registers)
- Message Bus Register Access (Indirect - via PCI Configuration Registers)

1.1 Fixed IO Register Access

Fixed IO registers are accessed by specifying their 16-bit address in a PORT IN and/or PORT OUT transaction from the CPU core. This allows direct manipulation of the registers. Fixed IO registers are unmovable register in IO space.

Type: I/O Register (Size: 32 bits) **P80:** 80h

1.2 Fixed Memory Mapped Register Access

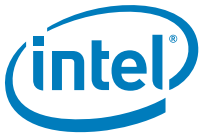
Fixed Memory Mapped IO (MMIO) registers are accessed by specifying their 32/36-bit address in a memory transaction from the CPU core. This allows direct manipulation of the registers. Fixed MMIO registers are unmovable registers in memory space.

Type: Memory Mapped I/O Register (Size: 32 bits) **IDX:** FEC00000h

1.3 IO Referenced Register Access

IO referenced registers use programmable base address registers (BARs) to select a range of IO addresses that it will use to decode PORT IN and/or PORT OUT transactions from the CPU to directly access a register. Thus, the IO BARs act as pointers to blocks of actual IO registers. To access an IO referenced register for a specific IO base address, start with that base address and add the register's offset. Example pseudo code for an IO referenced register read is shown below:

```
Register_Snapshot = IOREAD([IO_BAR]+Register_Offset)
```



Base address registers are often located in the PCI configuration space and are programmable by the BIOS/OS. Other base address register types may include fixed memory registers, fixed IO registers or message bus registers.

Type: I/O Register
(Size: 8bits)

HSTS: [PCU_IOBAR] + 0h

PCU_IOBAR Type: PCI Configuration Register (Size: 32 bits)
PCU_IOBAR Reference: [B:0, D:31, F:3] + 20h

1.4 Memory Referenced Register Access

The SoC uses programmable base address registers (BARs) to set a range of physical address (memory) locations that it will use to decode memory reads and writes from the CPU to directly access a register. These BARs act as pointers to blocks of actual memory mapped IO (MMIO) registers. To access a memory referenced register for a specific base address, start with that base address and add the register's offset. Example pseudo code for a read is shown below:

```
Register_Snapshot = MEMREAD([Mem_BAR]+Register_Offset)
```

Base address registers are often located in the PCI configuration space and are programmable by the BIOS/OS. Other common base address register types include fixed memory registers and IO registers that point to MMIO register blocks.

Type: Memory Mapped I/O Register
(Size: 8bits)

HSTS: [PCU_MBAR] + 0h

PCU_MBAR Type: PCI Configuration Register (Size: 32 bits)
PCU_MBAR Reference: [B:0, D:31, F:3] + 10h

1.5 PCI Configuration Register Access

Access to PCI configuration space registers is performed through one of two different configuration access methods (CAMs):

- IO indexed - PCI CAM
- Memory mapped - PCI Enhanced CAM (ECAM)

Each PCI function has a standard PCI header consisting of 256 bytes for the IO access scheme (CAM), or 4096 bytes for the enhanced memory access method (ECAM). Invalid read accesses return binary strings of 1s.

Type: PCI Configuration Register
(Size: 16bits)

VID: [B:0, D:31, F:3] + 0h

1.5.1 PCI Configuration Access - CAM: IO Indexed Scheme

Accesses to configuration space using the IO method relies on two 32-bit IO registers:

- **CONFIG_ADDRESS** - IO Port CF8h
- **CONFIG_DATA** - IO Port CFCh

These two registers are both 32-bit registers in IO space. Using this indirect access mode, software uses CONFIG_ADDRESS (CF8h) as an index register, indicating which configuration space register to access, and CONFIG_DATA (CFCh) acts as a window to the register pointed to in CONFIG_ADDRESS. Accesses to CONFIG_ADDRESS (CF8h) are internally captured. Upon a read or write access to CONFIG_DATA (CFCh), configuration cycles will be generated to the PCI function specified by the address captured in CONFIG_ADDRESS. The format of the address is shown below.

Table 1. PCI CONFIG_ADDRESS Register (IO PORT CF8h) Mapping

Field	CONFIG_ADDRESS Bits
Enable PCI Config. Space Mapping	31
Reserved	30:24
Bus Number	23:16
Device Number	15:11
Function Number	10:08
Register/Offset Number	07:02

Note: Bit 31 of CONFIG_ADDRESS must be set for a configuration cycle to be generated.

Pseudo code for a PCI register read is shown below:

- MyCfgAddr[23:16] = bus; MyCfgAddr[15:11] = device; MyCfgAddr[10:8] = funct;
- MyCfgAddr[7:2] = dWordMask(offset); MyCfgAddr[31] = 1;
- IOWRITE(0xCF8, MyCfgAddr)
- Register_Snapshot = IOREAD(0xCFC)

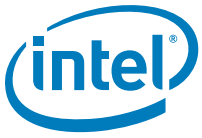
1.6 Message Bus Register Access

Accesses to the message bus space is through the SoC Transaction Router's PCI configuration registers. This unit relies on three 32-bit PCI configuration registers to generate messages:

- Message Bus Control Register (MCR) - PCI[B:0,D:0,F:0] + D0h
- Message Data Register (MDR) - PCI[B:0,D:0,F:0] + D4h
- Message Control Register eXtension (MCRX) - PCI[B:0,D:0,F:0] + D8h

This indirect access mode is similar to PCI CAM. Software uses the MCR/MCRX as an index register, indicating which message bus space register to access (MCRX only when required), and MDR as the data register. Writes to the MCR trigger message bus transactions.

Writes to MCRX and MDR will be captured. Writes to MCR will generate an internal 'message bus' transaction with the opcode and target (port, offset, bytes) specified in the MCR and the captured MCRX. When a write opcode is specified in MCR, the data



that was captured by MDR is used for the write. When a data read opcode is specified in MCR, the data will be available in the MDR register after the MCR write completes (non-posted). The format of MCR and MCRX are shown below.

Table 2. MCR Description

Field	MBPR Bits
OpCode (typically 10h for read, 11h for write)	31:24
Port	23:16
Offset/Register	15:08
Byte Enable	07:04

Table 3. MCRX Description

Field	MBPER Bits
Offset/Register Extension. This is used for messages sent to end points that require more than 8 bits for the offset/register. These bits are a direct extension of MCR[15:8].	31:08

Most message bus registers are located in the SoC Transaction Router. The default opcode messages for those registers are as follows:

- Message 'Read Register' Opcode: 06h
- Message 'Write Register' Opcode: 07h

Registers with different opcodes will be specified as applicable. Pseudo code of a message bus register read is shown below (where ReadOp==0x06):

- MyMCR[31:24] = ReadOp; MyMCR[23:16] = port; MyMCR[15:8] = offset;
- MyMCR[7:4] = 0xf
- PCIWRITE(0, 0, 0, 0xD0, MyMCR)
- Register_Snapshot = PCIREAD(0, 0, 0, 0xD4)

1.7 Register Field Access Types

Table 4. Register Access Types and Definitions

Access Type	Meaning	Description
RO	Read Only	In some cases, if a register is read only, writes to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register.
WO	Write Only	In some cases, if a register is write only, reads to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register.
R/W	Read/Write	A register with this attribute can be read and written.
R/WC	Read/Write Clear	A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.
R/WO	Read/Write-Once	A register bit with this attribute can be written only once after power up. After the first write, the bit becomes read only.
R/WLO	Read/Write, Lock-Once	A register bit with this attribute can be written to the non-locked value multiple times, but to the locked value only once. After the locked value has been written, the bit becomes read only.
Default	Default	When the processor is reset, it sets its registers to predetermined default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software to determine configuration, operating parameters, and optional system features that are applicable, and to program the processor registers accordingly.

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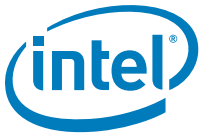


2 Mapping Address Spaces

The SoC supports four different address spaces:

- Physical Address Space Mappings
- IO Address Space
- PCI Configuration Space
- Message Bus Space

The CPU core can only directly access *memory space* through memory reads and writes and *IO space* through the IN and OUT IO port instructions. *PCI configuration space* is indirectly accessed through IO or memory space, and the *Message Bus space* is accessed through PCI configuration space. Refer Chapter 1, "Register Access Methods" for details.

This chapter describes how the memory, IO, PCI and Message Bus spaces are mapped to interfaces in the SoC.

2.1 Physical Address Space Mappings

There are 64 GB (36-bits) of physical address space that can be used as:

- Memory Mapped IO (MMIO - IO fabric)
- Physical Memory (DRAM)

The CPU core can access the full physical address space, while downstream devices can only access SoC DRAM, and each CPU core's local APIC. Peer to peer transactions are not supported.

Most devices map their registers and memory to the physical address space. This chapter summarizes the possible mappings.

2.1.1 SoC Transaction Router Memory Map

The SoC Transaction Router maps the physical address space as follows:

- CPU core to DRAM
- CPU core to IO fabric (MMIO)
- CPU core to extended PCI registers (ECAM accesses)
- IO fabric to CPU cores (local APIC interrupts)

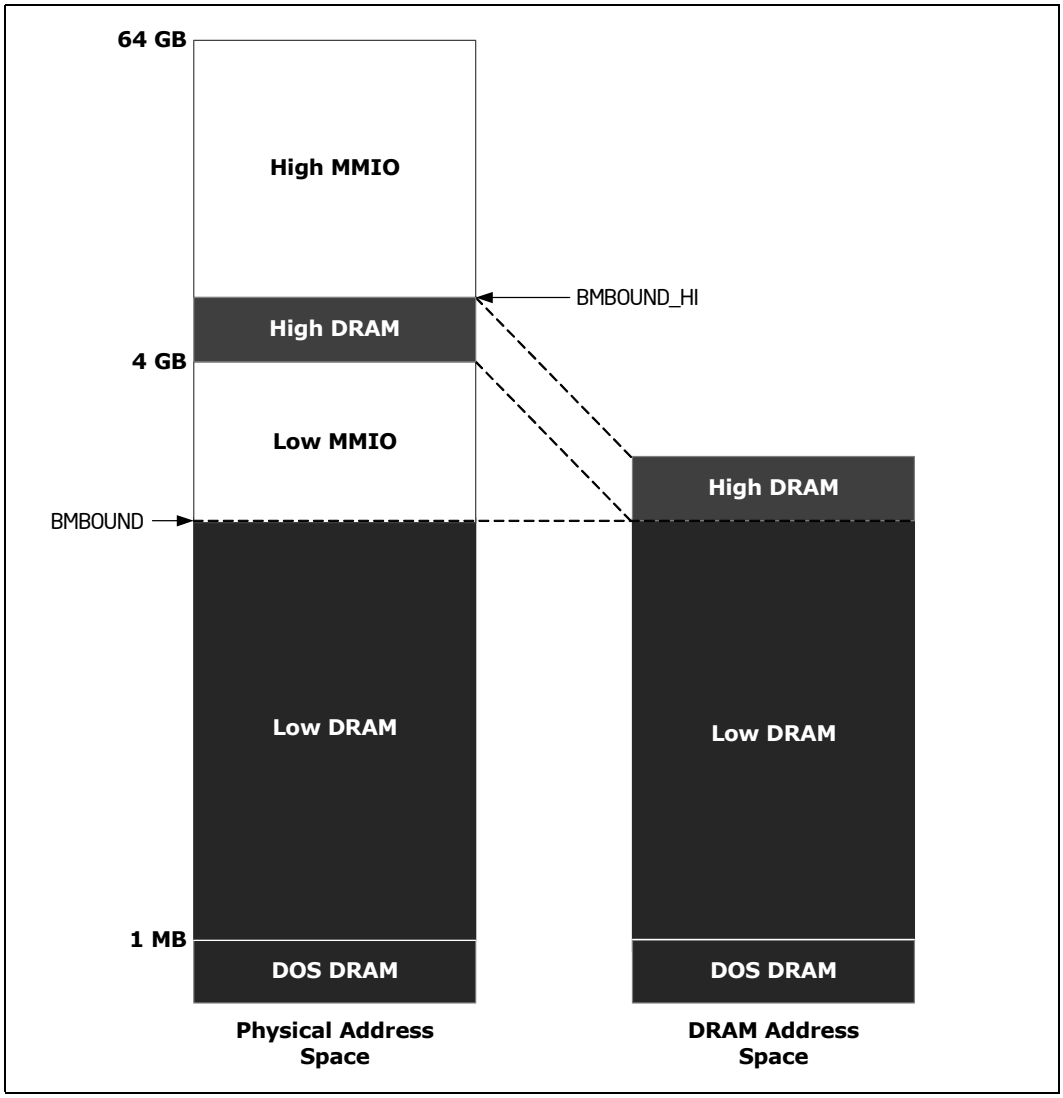
Although 64 GB (36-bits) of physical address space is accessible, some MMIO must exist for devices and software with 32-bit limits. Further, all DRAM should remain accessible for devices and software with access to memory above 4 GB. These goals

are accomplished by moving a section DRAM to start at the fixed 4 GB boundary, leaving a hole below 4 GB for MMIO. This creates the following distinct memory regions:

- DOS DRAM + Low DRAM
- Low MMIO
- High DRAM
- High MMIO

There are two registers used to create these regions, BMBOUND and BMBOUND_HI. Their use is shown in Figure 1.

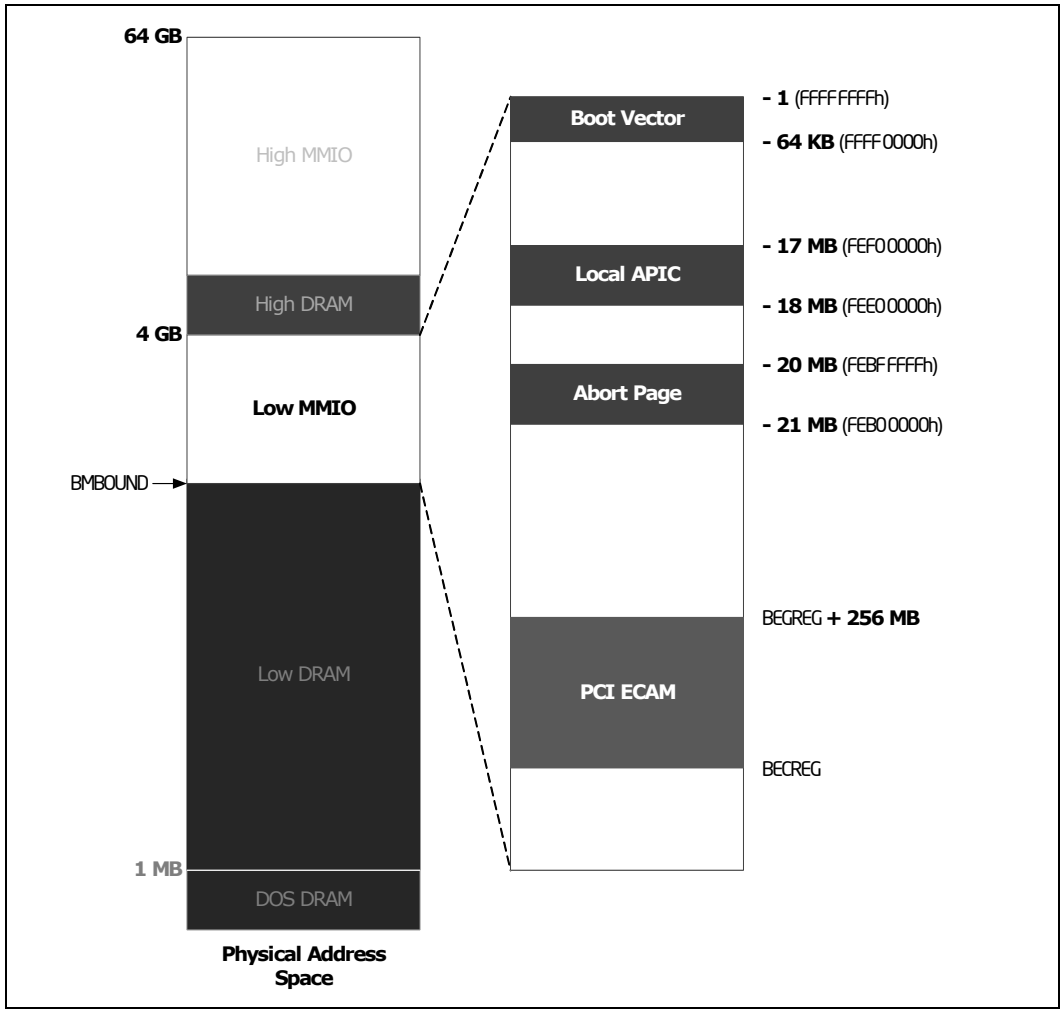
Figure 1. Physical Address Space - DRAM & MMIO



2.1.1.1 Low MMIO

The low MMIO mappings are shown in Figure 2.

Figure 2. Physical Address Space - Low MMIO



By default, CPU core reads targeting the **Boot Vector** range (FFFFFFFFh-FFFF0000h) are sent to the boot Flash connected to the Platform Controller Unit, and write accesses target DRAM. This allows the boot strap CPU core to fetch boot code from the boot Flash, and then shadow that code to DRAM.

Upstream writes from the IO fabric to the **Local APIC** range (FEE00000h-FEF00000h) are sent to the appropriate CPU core's APIC.

Write accesses from a CPU core to the **Abort Page** range (FEB00000h-FEBFFFFFh) will be dropped, and reads will always return all 1's in binary.

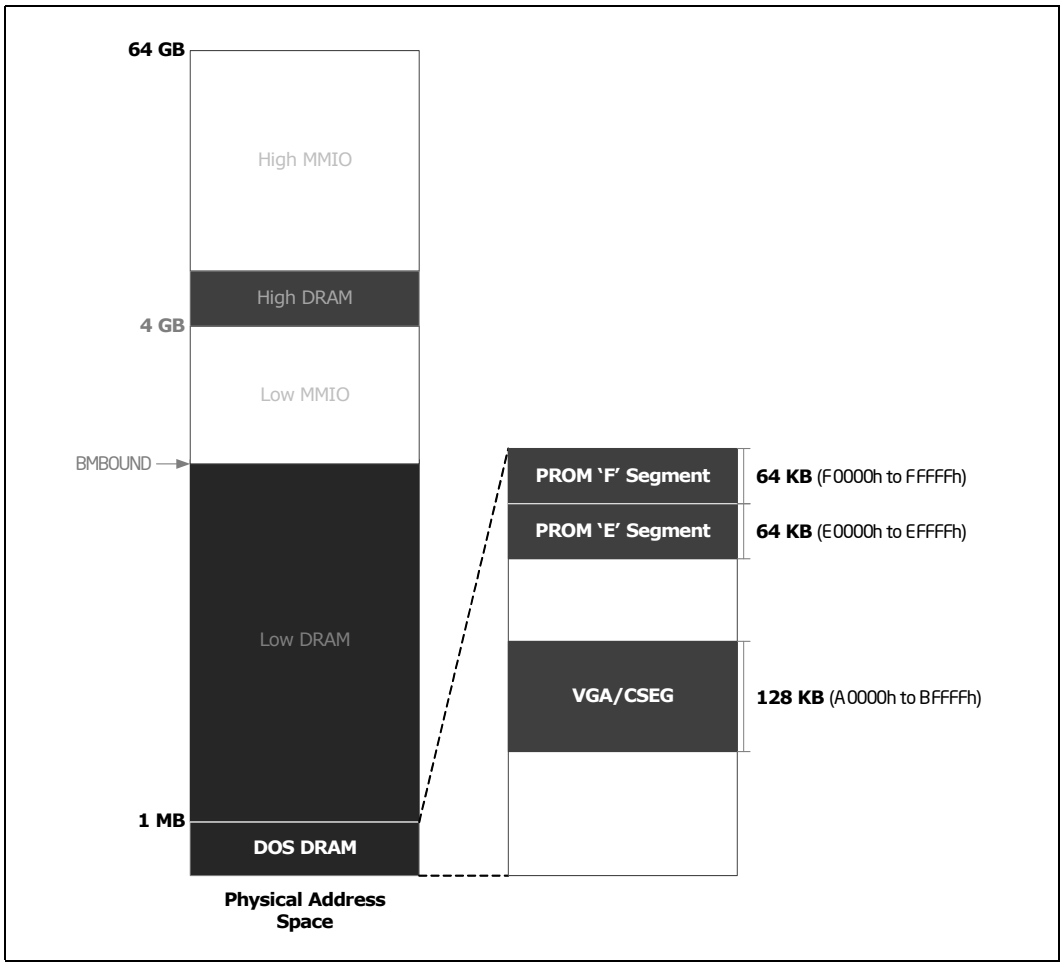
Accesses in the 256 MB **PCI ECAM** range starting at BECREG generate enhanced PCI configuration register accesses when enabled (BECREG.ECENABLE). Unlike traditional memory writes, writes to this range are non-posted when enabled. Refer Chapter 1, "Register Access Methods" for more details.

All other downstream accesses in the Low MMIO range are sent to the IO Fabric for further decode based on PCI resource allocations. The IO Fabric's subtractive agent (for unclaimed accesses) is the Platform Controller Hub.

2.1.1.2 DOS DRAM

The DOS DRAM is the memory space below 1 MB. In general, accesses from a processor targeting DOS DRAM target system DRAM. Exceptions are shown in the below figure.

Figure 3. Physical Address Space - DOS DRAM



Processor writes to the 64 KB (each) **PROM 'E'** and **'F'** segments (E0000h-EFFFFh and F0000h-FFFFFh) always target DRAM. The BMISC register is used to direct CPU core reads in these two segments to DRAM or the IO fabric (MMIO).

CPU core accesses to the 128 KB **VGA/CSEG** range (A0000h-BFFFFh) can target DRAM or the IO fabric (MMIO). The target is selected with the BMISC.ABSEGINDRAM register.

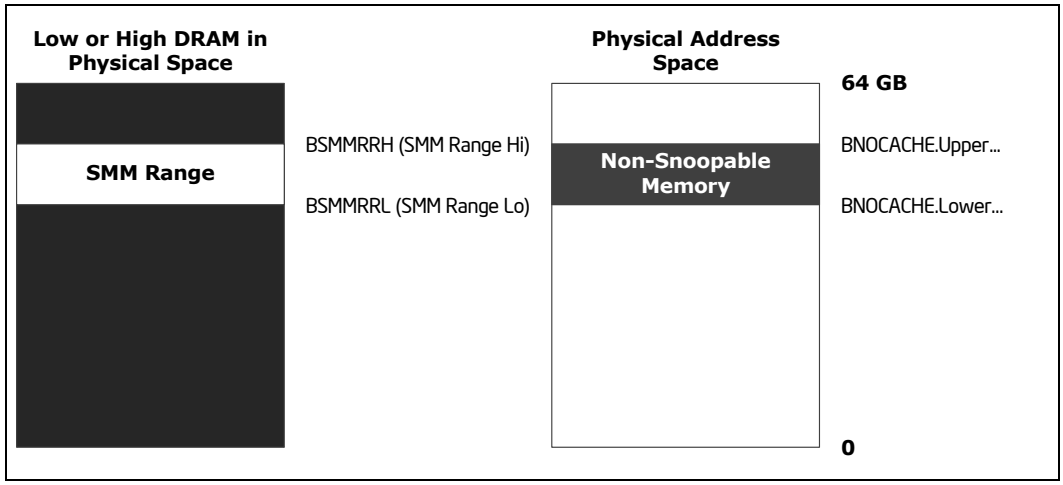
2.1.1.3 Additional Mappings

There are two additional mappings available in the SoC Transaction Router:

- SMM range
- Non-snoop range

Figure 4 shows these mappings.

Figure 4. Physical Address Space - SMM and Non-Snoop Mappings



SMI handlers running on a CPU core execute out of SMM memory. To protect this memory from non-CPU core access, the **SMM Range** (BSMMRRL-BSMMRRH) may be programmed anywhere in low or high DRAM space (1 MB aligned). This range will only allow accesses from the CPU cores.

To prevent snoops of the CPU cores when DMA devices access a specific memory region, the **Non-Snoopable Memory range** (BNOCACHE.Lower-BNOCACHE.Upper) can be programmed anywhere in physical address space. This range is enabled via the BNOCACHECTL register's enable bit (BNOCACHECTL.Enable).

2.1.2 IO Fabric (MMIO) Map

Memory accesses targeting MMIO are routed by the IO fabric to programmed PCI ranges, or routed to the PCU by default (subtractive agent). Programmed PCI ranges can be moved within low or high MMIO, and most can be disabled.

Note: Not all devices can be mapped to high MMIO.

Fixed MMIO is claimed by the Platform Controller Unit (PCU). The default regions are listed below. Movable ranges are not shown.

Table 5. Fixed Memory Ranges in the Platform Controller Unit (PCU)

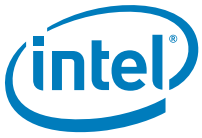
Device	Start Address	End Address	Comments
Low BIOS (Flash Boot)	000E0000h	000FFFFFh	Starts 128 KB below 1 MB; Firmware/ BIOS
IO APIC	FEC00000h	FEC00040h	Starts 20 MB below 4 GB
HPET	FED00000h	FED003FFh	Starts 19 MB below 4 GB
TPM (LPC)	FFD40000h	FFD40FFFh	Starts 16 KB above HPET range
High BIOS/Boot Vector	FFFF0000h	FFFFFFFFh	Starts 64 KB below 4 GB; Firmware/ BIOS

The following PCI devices may claim memory resources in MMIO space:

- Graphics/Display (High MMIO capable)
- SD/MMC/SDIO
- SIO
- Platform Controller Unit (PCU) (Multiple BARs)
- xHCI USB
- EHCI USB
- USB Device
- ISP/MIPI-CSI

Refer each device’s interface chapter for details.

Warning: Variable memory ranges should not be set to conflict with other memory ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.



2.2 IO Address Space

There are 64 KB + 3 bytes of IO space (0h-10002h) for accessing IO registers. Most IO registers exists for legacy functions in the PCU or for PCI devices, while some are claimed by the SoC Transaction Router for graphics and for the PCI configuration space access registers.

2.2.1 SoC Transaction Router IO Map

The SoC claims IO transactions for VGA/Extended VGA found in the display/graphics interface. It also claims the two 32-bit registers at port CF8h and CFCh used to access PCI configuration space.

2.2.2 IO Fabric IO Map

2.2.2.1 PCU Fixed IO Address Ranges

Below table shows the fixed IO space ranges seen by a processor.

Table 6. Fixed IO Ranges in the Platform Controller Unit (PCU)

Device	IO Address	Comments
8259 Master	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39-, 3Ch-3Dh	
8254s	40h-43h, 50h-53h	
PS2 Control	60h, 64h	
NMI Controller	61h, 63h, 65h, 67h	
RTC	70h-77h	
Port 80h	80h-83h	
Init Register	92h	
8259 Slave	A0h-A1h, A4h-A5h, A8h-A9h, ACh-ADh, B0h-B1h, B4h-B5h, B8h-B9h, BCh-BDh, 4D0h-4D1h	
PCU UART	3F8h-3FFh	
Reset Control	CF9h	Overlaps PCI IO registers
Active Power Management	B2h-B3h	

2.2.2.2 Variable IO Address Ranges

Table 7 shows the variable IO decode ranges. They are set using base address registers (BARs) or other similar means. Plug-and-play (PnP) software (PCI/ACPI) can use their configuration mechanisms to set and adjust these values.

Warning: The variable IO ranges should not be set to conflict with other IO ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.

Table 7. Movable IO Ranges Decoded by PCI Devices on the IO Fabric

Device	Size (bytes)	Target
ACPI Power Management (PCU)	128	ACPI_BASE_ADDR (PM1BLK): PCI[B:0,D:31,F:0] + 40h
GPIO (PCU)	256	GBA: PCI[B:0,D:31,F:0] + 48h
RCBA (PCU)	1024	RCRB_BA: PCI[B:0,D:31,F:0] + F0h

2.3 PCI Configuration Space

All PCI devices/functions are shown below.

Table 8. PCI Devices and Functions (Sheet 1 of 2)

Bus	Device	Function	Device ID	Device Description	Function Description
0	0	0	0F00h	SoC Transaction Router	
0	2	0	0F31h	Graphics & Display	
0	3	0	0F38h	Camera Image Signal Processor	
0	16	0	0F14h	Storage Control Cluster (SCC)	MMC Port
0	17	0	0F15h		SDIO Port
0	18	0	0F16h		SD Port
0	20	0	0F35h	xHCI USB	
0	21	0	0F28h	Low Power Engine Audio	Host Bridge + three I^2S Ports (0-2)
0	22	0	0F37h	USB Device	
0	24	0	0F40h	Serial IO (SIO)	DMA
		1	0F41h		I^2C Port 1
		2	0F42h		I^2C Port 2
		3	0F43h		I^2C Port 3
		4	0F44h		I^2C Port 4
		5	0F45h		I^2C Port 5
		6	0F46h		I^2C Port 6
		7	0F47h		I^2C Port 7

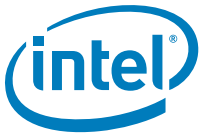


Table 8. PCI Devices and Functions (Sheet 2 of 2)

Bus	Device	Function	Device ID	Device Description	Function Description
0	26	0	0F18h	Trusted Execution Engine	
0	27	0	0F04h	HD Audio	
0	29	0	0F34h	EHCI USB	
0	30	0	0F06h	Serial IO (SIO)	DMA
		1	0F08h		PWM Port 1
		2	0F09h		PWM Port 2
		3	0F0Ah		HSUART Port 1
		4	0F0Ch		HSUART Port 2
		5	0F0Eh		SPI Port
0	31	0	0F1Ch	Platform Controller Unit	LPC: Bridge to Intel Legacy Block

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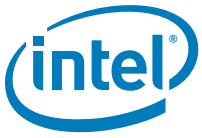
3 SoC Registers

Following pages provides register information for all registers applicable to SoC.



3.1 Display Memory Mapped Registers (1 of 2)

Table 9. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
3B4h	1	"CRX (CRX_MDA)—Offset 3B4h" on page 29	00h
3B5h	1	"CR (CR_MDA)—Offset 3B5h" on page 30	00h
3C0h	1	"ARX—Offset 3C0h" on page 30	00h
3C1h	1	"ARX—Offset 3C0h" on page 30	00h
3C4h	1	"SRX—Offset 3C4h" on page 32	00h
3C5h	1	"SRX—Offset 3C4h" on page 32	00h
3C6h	1	"DACMASK—Offset 3C6h" on page 33	00h
3C8h	1	"DACWX—Offset 3C8h" on page 34	00h
3C9h	1	"DACDATA—Offset 3C9h" on page 34	00h
3CAh	1	"FCR (FCR_Read)—Offset 3CAh" on page 35	00h
3CCh	1	"MSR (MSR_READ)—Offset 3CCh" on page 36	00h
3CEh	1	"GRX—Offset 3CEh" on page 38	00h
3CFh	1	"GRX—Offset 3CEh" on page 38	00h
3D4h	1	"CRX (CRX_CGA)—Offset 3D4h" on page 39	00h
3D5h	1	"CR (CR_CGA)—Offset 3D5h" on page 40	00h
5010h	4	"GPIOCTL_0—Offset 5010h" on page 41	00000808h
5014h	4	"GPIOCTL_1—Offset 5014h" on page 43	00000808h
5018h	4	"GPIOCTL_2—Offset 5018h" on page 45	00000808h
501Ch	4	"GPIOCTL_3—Offset 501Ch" on page 47	00000808h
5020h	4	"GPIOCTL_4—Offset 5020h" on page 49	00000808h
5100h	4	"GMBUS0—Offset 5100h" on page 51	00000000h
5104h	4	"GMBUS1—Offset 5104h" on page 52	00000000h
5108h	4	"GMBUS2—Offset 5108h" on page 54	00000800h
510Ch	4	"GMBUS3—Offset 510Ch" on page 56	00000000h
5110h	4	"GMBUS4—Offset 5110h" on page 57	00000000h
5120h	4	"GMBUS5—Offset 5120h" on page 58	00000000h
5130h	4	"GMBUS6—Offset 5130h" on page 59	00000000h
5134h	4	"GMBUS7—Offset 5134h" on page 59	00000000h
6014h	4	"DPLLA_CTRL—Offset 6014h" on page 60	00002000h
6018h	4	"DPLLB_CTRL—Offset 6018h" on page 63	00006000h
601Ch	4	"DPLLAMD—Offset 601Ch" on page 66	00000003h
6020h	4	"DPLLBMD—Offset 6020h" on page 67	00000003h
6024h	4	"RAWCLK_FREQ—Offset 6024h" on page 69	0000007Dh
6104h	4	"D_STATE—Offset 6104h" on page 69	20D00400h

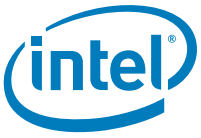


Table 9. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
6200h	4	"DSPCLK_GATE_D—Offset 6200h" on page 71	10000000h
6204h	4	"DPPSR_CGDIS—Offset 6204h" on page 73	00000200h
6210h	4	"RAMCLK_GATE_D—Offset 6210h" on page 76	00000000h
6500h	4	"FW_BLC_SELF—Offset 6500h" on page 79	00000000h
6504h	4	"MI_ARB—Offset 6504h" on page 80	00000000h
6508h	4	"CZCLK_CDCLK_FREQ_RATIO—Offset 6508h" on page 80	00000077h
650Ch	4	"GCI_CONTROL—Offset 650Ch" on page 84	00004000h
6510h	4	"GMBUSFREQ—Offset 6510h" on page 85	000000A0h
A000h	4	"DPALETTE_A—Offset A000h" on page 86	00000000h
A800h	4	"DPALETTE_B—Offset A800h" on page 87	00000000h
B000h	4	"MIPIA_DEVICE_READY_REG—Offset B000h" on page 88	00000000h
B004h	4	"MIPIA_INTR_STAT_REG—Offset B004h" on page 89	00000000h
B008h	4	"MIPIA_INTR_EN_REG—Offset B008h" on page 91	00000000h
B00Ch	4	"MIPIA_DSI_FUNC_PRG__REG—Offset B00Ch" on page 93	00000001h
B010h	4	"MIPIA_HS_TX_TIMEOUT_REG—Offset B010h" on page 95	00000000h
B014h	4	"MIPIA_LP_RX_TIMEOUT_REG—Offset B014h" on page 95	00000000h
B018h	4	"MIPIA_TURN_AROUND_TIMEOUT_REG—Offset B018h" on page 96	00000000h
B01Ch	4	"MIPIA_DEVICE_RESET_TIMER—Offset B01Ch" on page 97	00000000h
B020h	4	"MIPIA_DPI_RESOLUTION_REG—Offset B020h" on page 98	00000000h
B024h	4	"MIPIA_DBI_RESOLUTION_REG—Offset B024h" on page 98	00000000h
B028h	4	"MIPIA_HORIZ_SYNC_PADDING_COUNT—Offset B028h" on page 99	00000000h
B02Ch	4	"MIPIA_HORIZ_BACK_PORCH_COUNT—Offset B02Ch" on page 100	00000000h
B030h	4	"MIPIA_HORIZ_FRONT_PORCH_COUNT—Offset B030h" on page 100	00000000h
B034h	4	"MIPIA_HORIZ_ACTIVE_AREA_COUNT—Offset B034h" on page 101	00000000h
B038h	4	"MIPIA_VERT_SYNC_PADDING_COUNT—Offset B038h" on page 102	00000000h
B03Ch	4	"MIPIA_VERT_BACK_PORCH_COUNT—Offset B03Ch" on page 103	00000000h
B040h	4	"MIPIA_VERT_FRONT_PORCH_COUNT—Offset B040h" on page 104	00000000h
B044h	4	"MIPIA_HIGH_LOW_SWITCH_COUNT—Offset B044h" on page 104	00000000h
B048h	4	"MIPIA_DPI_CTRL_REG—Offset B048h" on page 106	00000000h
B04Ch	4	"MIPIA_DPI_DATA_REGISTER—Offset B04Ch" on page 106	00000000h

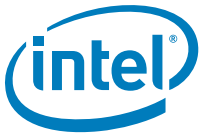


Table 9. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
B050h	4	"MIPIA_INIT_COUNT_REGISTER—Offset B050h" on page 107	00000000h
B054h	4	"MIPIA_MAX_RETURN_PKT_SIZE_REGISTER—Offset B054h" on page 108	00000000h
B058h	4	"MIPIA_VIDEO_MODE_FORMAT_REGISTER—Offset B058h" on page 108	00000000h
B05Ch	4	"MIPIA_EOT_DISABLE_REGISTER—Offset B05Ch" on page 110	00000000h
B060h	4	"MIPIA_LP_BYTECLK_REGISTER—Offset B060h" on page 112	00000000h
B064h	4	"MIPIA_LP_GEN_DATA_REGISTER—Offset B064h" on page 112	00000000h
B068h	4	"MIPIA_HS_GEN_DATA_REGISTER—Offset B068h" on page 113	00000000h
B06Ch	4	"MIPIA_LP_GEN_CTRL_REGISTER—Offset B06Ch" on page 113	00000000h
B070h	4	"MIPIA_HS_GEN_CTRL_REGISTER—Offset B070h" on page 114	00000000h
B074h	4	"MIPIA_GEN_FIFO_STAT_REGISTER—Offset B074h" on page 115	1E060606h
B078h	4	"MIPIA_HS_LS_DBI_ENABLE_REG—Offset B078h" on page 117	00000000h
B07Ch	4	"MIPIA_RESERVED—Offset B07Ch" on page 117	00000000h
B080h	4	"MIPIA_DPHY_PARAM_REG—Offset B080h" on page 118	0B061A04h
B084h	4	"MIPIA_DBI_BW_CTRL_REG—Offset B084h" on page 119	00000000h
B088h	4	"MIPIA_CLK_LANE_SWITCHING_TIME_CNT—Offset B088h" on page 119	00000000h
B08Ch	4	"MIPIA_STOP_STATE_STALL—Offset B08Ch" on page 120	00000000h
B090h	4	"MIPIA_INTR_STAT_REG_1—Offset B090h" on page 121	00000000h
B094h	4	"MIPIA_INTR_EN_REG_1—Offset B094h" on page 122	00000000h
B100h	4	"MIPIA_DBI_TYPEC_CTRL—Offset B100h" on page 123	00000000h
B104h	4	"MIPIA_CTRL—Offset B104h" on page 124	00000000h
B108h	4	"MIPIA_DATA_ADD—Offset B108h" on page 125	00000000h
B10Ch	4	"MIPIA_DATA_LEN—Offset B10Ch" on page 126	00000000h
B110h	4	"MIPIA_CMD_ADD—Offset B110h" on page 127	00000000h
B114h	4	"MIPIA_CMD_LEN—Offset B114h" on page 127	00000000h
B118h	4	"MIPIA_RD_DATA_RETURN0—Offset B118h" on page 128	00000000h
B11Ch	4	"MIPIA_RD_DATA_RETURN1—Offset B11Ch" on page 129	00000000h
B120h	4	"MIPIA_RD_DATA_RETURN2—Offset B120h" on page 130	00000000h
B124h	4	"MIPIA_RD_DATA_RETURN3—Offset B124h" on page 130	00000000h
B128h	4	"MIPIA_RD_DATA_RETURN4—Offset B128h" on page 131	00000000h
B12Ch	4	"MIPIA_RD_DATA_RETURN5—Offset B12Ch" on page 132	00000000h
B130h	4	"MIPIA_RD_DATA_RETURN6—Offset B130h" on page 132	00000000h
B134h	4	"MIPIA_RD_DATA_RETURN7—Offset B134h" on page 133	00000000h
B138h	4	"MIPIA_RD_DATA_VALID—Offset B138h" on page 134	00000000h
B800h	4	"MIPIC_DEVICE_READY_REG—Offset B800h" on page 134	00000000h

Table 9. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
B804h	4	"MIPIC_INTR_STAT_REG—Offset B804h" on page 135	00000000h
B808h	4	"MIPIC_INTR_EN_REG—Offset B808h" on page 137	00000000h
B80Ch	4	"MIPIC_DSI_FUNC_PRG__REG—Offset B80Ch" on page 139	00000001h
B810h	4	"MIPIC_HS_TX_TIMEOUT_REG—Offset B810h" on page 141	00000000h
B814h	4	"MIPIC_LP_RX_TIMEOUT_REG—Offset B814h" on page 141	00000000h
B818h	4	"MIPIC_TURN_AROUND_TIMEOUT_REG—Offset B818h" on page 142	00000000h
B81Ch	4	"MIPIC_DEVICE_RESET_TIMER—Offset B81Ch" on page 143	00000000h
B820h	4	"MIPIC_DPI_RESOLUTION_REG—Offset B820h" on page 144	00000000h
B824h	4	"MIPIC_DBI_RESOLUTION_REG—Offset B824h" on page 144	00000000h
B828h	4	"MIPIC_HORIZ_SYNC_PADDING_COUNT—Offset B828h" on page 145	00000000h
B82Ch	4	"MIPIC_HORIZ_BACK_PORCH_COUNT—Offset B82Ch" on page 146	00000000h
B830h	4	"MIPIC_HORIZ_FRONT_PORCH_COUNT—Offset B830h" on page 146	00000000h
B834h	4	"MIPIC_HORIZ_ACTIVE_AREA_COUNT—Offset B834h" on page 147	00000000h
B838h	4	"MIPIC_VERT_SYNC_PADDING_COUNT—Offset B838h" on page 148	00000000h
B83Ch	4	"MIPIC_VERT_BACK_PORCH_COUNT—Offset B83Ch" on page 149	00000000h
B840h	4	"MIPIC_VERT_FRONT_PORCH_COUNT—Offset B840h" on page 150	00000000h
B844h	4	"MIPIC_HIGH_LOW_SWITCH_COUNT—Offset B844h" on page 150	00000000h
B848h	4	"MIPIC_DPI_CTRL_REG—Offset B848h" on page 152	00000000h
B84Ch	4	"MIPIC_DPI_DATA_REGISTER—Offset B84Ch" on page 152	00000000h
B850h	4	"MIPIC_INIT_COUNT_REGISTER—Offset B850h" on page 153	00000000h
B854h	4	"MIPIC_MAX_RETURN_PKT_SIZE_REGISTER—Offset B854h" on page 154	00000000h
B858h	4	"MIPIC_VIDEO_MODE_FORMAT_REGISTER—Offset B858h" on page 154	00000000h
B85Ch	4	"MIPIC_EOT_DISABLE_REGISTER—Offset B85Ch" on page 156	00000000h
B860h	4	"MIPIC_LP_BYTECLK_REGISTER—Offset B860h" on page 158	00000000h
B864h	4	"MIPIC_LP_GEN_DATA_REGISTER—Offset B864h" on page 158	00000000h
B868h	4	"MIPIC_HS_GEN_DATA_REGISTER—Offset B868h" on page 159	00000000h
B86Ch	4	"MIPIC_LP_GEN_CTRL_REGISTER—Offset B86Ch" on page 159	00000000h
B870h	4	"MIPIC_HS_GEN_CTRL_REGISTER—Offset B870h" on page 160	00000000h
B874h	4	"MIPIC_GEN_FIFO_STAT_REGISTER—Offset B874h" on page 161	1E060606h

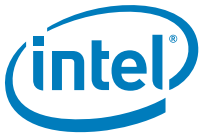


Table 9. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
B878h	4	"MIPIC_HS_LS_DBI_ENABLE_REG—Offset B878h" on page 163	00000000h
B87Ch	4	"MIPIC_RESERVED—Offset B87Ch" on page 163	00000000h
B880h	4	"MIPIC_DPHY_PARAM_REG—Offset B880h" on page 164	0B061A04h
B884h	4	"MIPIC_DBI_BW_CTRL_REG—Offset B884h" on page 165	00000000h
B888h	4	"MIPIC_CLK_LANE_SWITCHING_TIME_CNT—Offset B888h" on page 165	00000000h
B88Ch	4	"MIPIC_STOP_STATE_STALL—Offset B88Ch" on page 166	00000000h
B890h	4	"MIPIC_INTR_STAT_REG_1—Offset B890h" on page 167	00000000h
B894h	4	"MIPIC_INTR_EN_REG_1—Offset B894h" on page 168	00000000h
B904h	4	"MIPIC_CTRL—Offset B904h" on page 169	00000000h
B908h	4	"MIPIC_DATA_ADD—Offset B908h" on page 170	00000000h
B90Ch	4	"MIPIC_DATA_LEN—Offset B90Ch" on page 171	00000000h
B910h	4	"MIPIC_CMD_ADD—Offset B910h" on page 171	00000000h
B914h	4	"MIPIC_CMD_LEN—Offset B914h" on page 172	00000000h
B918h	4	"MIPIC_RD_DATA_RETURN0—Offset B918h" on page 173	00000000h
B91Ch	4	"MIPIC_RD_DATA_RETURN1—Offset B91Ch" on page 173	00000000h
B920h	4	"MIPIC_RD_DATA_RETURN2—Offset B920h" on page 174	00000000h
B924h	4	"MIPIC_RD_DATA_RETURN3—Offset B924h" on page 175	00000000h
B928h	4	"MIPIC_RD_DATA_RETURN4—Offset B928h" on page 175	00000000h
B92Ch	4	"MIPIC_RD_DATA_RETURN5—Offset B92Ch" on page 176	00000000h
B930h	4	"MIPIC_RD_DATA_RETURN6—Offset B930h" on page 177	00000000h
B934h	4	"MIPIC_RD_DATA_RETURN7—Offset B934h" on page 177	00000000h
B938h	4	"MIPIC_RD_DATA_VALID—Offset B938h" on page 178	00000000h
60000h	4	"HTOTAL_A—Offset 60000h" on page 179	00000000h
60004h	4	"HBLANK_A—Offset 60004h" on page 180	00000000h
60008h	4	"HSYNC_A—Offset 60008h" on page 181	00000000h
6000Ch	4	"VTOTAL_A—Offset 6000Ch" on page 182	00000000h
60010h	4	"VBLANK_A—Offset 60010h" on page 184	00000000h
60014h	4	"VSYNC_A—Offset 60014h" on page 185	00000000h
6001Ch	4	"PIPESRCA—Offset 6001Ch" on page 186	00000000h
60020h	4	"BCLRPAT_A—Offset 60020h" on page 187	00000000h
60028h	4	"VSYNCSHIFT_A—Offset 60028h" on page 188	00000000h
60030h	4	"TRANSADATAM1—Offset 60030h" on page 189	7E000000h
60034h	4	"TRANSADATAN1—Offset 60034h" on page 190	00000000h
60038h	4	"TRANSADATAM2—Offset 60038h" on page 191	7E000000h
6003Ch	4	"TRANSADATAN2—Offset 6003Ch" on page 191	00000000h
60040h	4	"TRANSADPLINKM1—Offset 60040h" on page 192	00000000h

Table 9. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
60044h	4	"TRANSADPLINKN1—Offset 60044h" on page 193	00000000h
60048h	4	"TRANSADPLINKM2—Offset 60048h" on page 193	00000000h
6004Ch	4	"TRANSADPLINKN2—Offset 6004Ch" on page 194	00000000h
60050h	4	"CRCCTRLREDA—Offset 60050h" on page 195	00000000h
60054h	4	"CRCCTRLGREENA—Offset 60054h" on page 196	00000000h
60058h	4	"CRCCTRLBLUEA—Offset 60058h" on page 196	00000000h
6005Ch	4	"CRCCTRLALPHAA—Offset 6005Ch" on page 197	00000000h
60060h	4	"CRCRESREDA—Offset 60060h" on page 198	00000000h
60064h	4	"CRCRESGREENA—Offset 60064h" on page 198	00000000h
60068h	4	"CRCRESBLUEA—Offset 60068h" on page 199	00000000h
6006Ch	4	"CRCRESALPHAA—Offset 6006Ch" on page 200	00000000h
60070h	4	"CRCCTRLRESIDUE2A—Offset 60070h" on page 201	00000000h
60080h	4	"CRCRESRESIDUE2A—Offset 60080h" on page 202	00000000h
60090h	4	"PSRCTLA—Offset 60090h" on page 203	00000000h
60094h	4	"PSRSTATA—Offset 60094h" on page 204	00000000h
60098h	4	"PSRCRC1A—Offset 60098h" on page 205	00000000h
6009Ch	4	"PSRCRC2A—Offset 6009Ch" on page 206	00000000h
600A0h	4	"VSCSDPA—Offset 600A0h" on page 207	00000000h
600B0h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 600B0h" on page 208	00000000h
600B4h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 600B4h" on page 209	00000000h
600B8h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 600B8h" on page 209	00000000h
600BCh	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 600BCh" on page 210	00000000h
600C0h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 600C0h" on page 211	00000000h
600C4h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 600C4h" on page 212	00000000h
60200h	4	"VIDEO_DIP_CTL_A—Offset 60200h" on page 212	20200900h
60208h	4	"VIDEO_DIP_DATA_A—Offset 60208h" on page 214	00000000h
60210h	4	"VIDEO_DIP_GDCP_PAYLOAD_A—Offset 60210h" on page 215	00000000h
61000h	4	"HTOTAL_B—Offset 61000h" on page 216	00000000h
61004h	4	"HBLANK_B—Offset 61004h" on page 217	00000000h
61008h	4	"HSYNC_B—Offset 61008h" on page 218	00000000h
6100Ch	4	"VTOTAL_B—Offset 6100Ch" on page 219	00000000h
61010h	4	"VBLANK_B—Offset 61010h" on page 220	00000000h

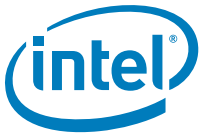


Table 9. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
61014h	4	"VSYNC_B—Offset 61014h" on page 221	00000000h
6101Ch	4	"PIPEBSRC—Offset 6101Ch" on page 222	00000000h
61020h	4	"BCLRPAT_B—Offset 61020h" on page 223	00000000h
61028h	4	"VSYNCSHIFT_B—Offset 61028h" on page 224	00000000h
61030h	4	"TRANSBDATAM1—Offset 61030h" on page 225	7E000000h
61034h	4	"TRANSBDATAN1—Offset 61034h" on page 226	00000000h
61038h	4	"TRANSBDATAM2—Offset 61038h" on page 227	7E000000h
6103Ch	4	"TRANSBDATAN2—Offset 6103Ch" on page 227	00000000h
61040h	4	"TRANSBDPLINKM1—Offset 61040h" on page 228	00000000h
61044h	4	"TRANSBDPLINKN1—Offset 61044h" on page 229	00000000h
61048h	4	"TRANSBDPLINKM2—Offset 61048h" on page 229	00000000h
6104Ch	4	"TRANSBDPLINKN2—Offset 6104Ch" on page 230	00000000h

3.1.1 CRX (CRX_MDA)—Offset 3B4h

CRT Controller Index Register

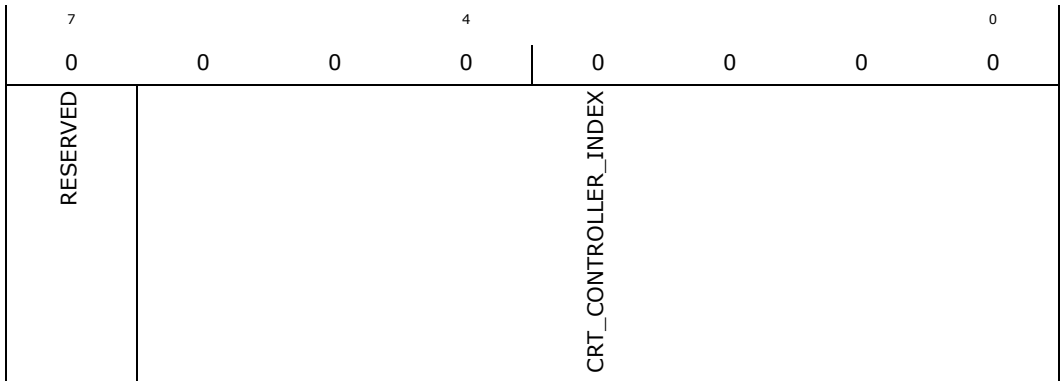
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

CRX_MDA: [GTTMMADR_LSB + 2BF20h] + 3B4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RW	**RESERVED:** Read as 0.

Bit Range	Default & Access	Description
6:0	0b RW	**CRT_CONTROLLER_INDEX:** These 7 bits are used to select any one of the CRT controller registers to be accessed via the data port at I/O location 3B5h or 3D5h, depending upon whether the graphics system is configured for MDA or CGA emulation. The data port memory address offsets are 3B5h/3D5h.

3.1.2 CR (CR_MDA)—Offset 3B5h

CR index registers

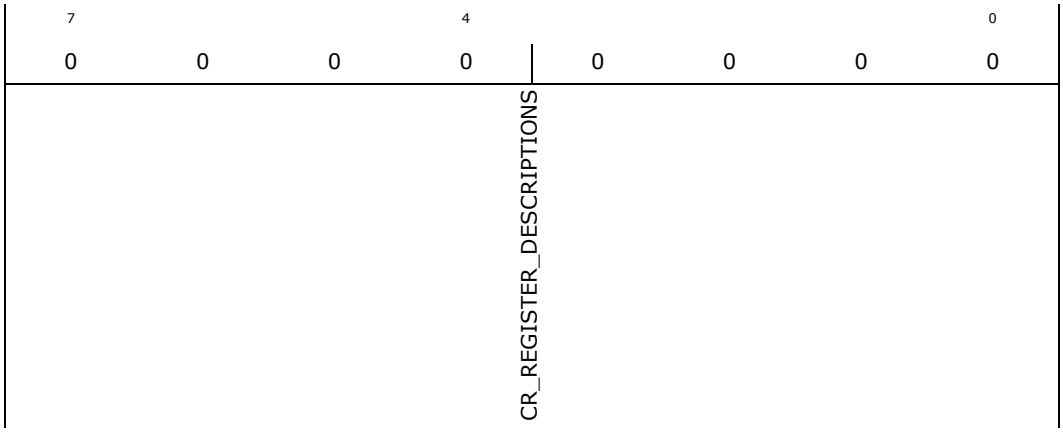
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

CR_MDA: [GTTMMADR_LSB + 2BF20h] + 3B5h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**CR_REGISTER_DESCRIPTIONS:** CR indexed register descriptions

3.1.3 ARX—Offset 3C0h

Attribute Controller Index Register. Includes the 22 registers that share this offset (with different indexes). -enum ARX_e

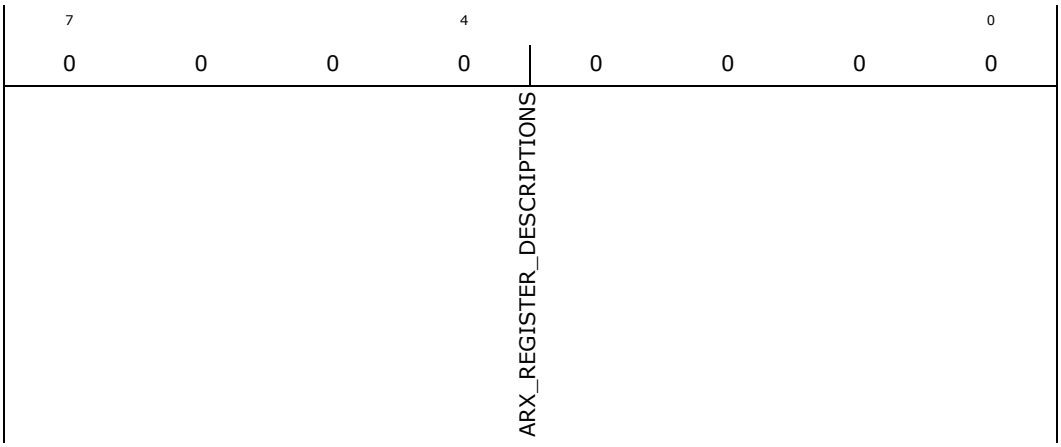
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

ARX: [GTTMMADR_LSB + 2BF20h] + 3C0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**ARX_REGISTER_DESCRIPTIONS:** ARX indexed register descriptions

3.1.4 AR—Offset 3C1h

AR index registers. Includes the 21 registers that share this offset (with different indexes.) -enum AR_e- in this document will lead to register definitions

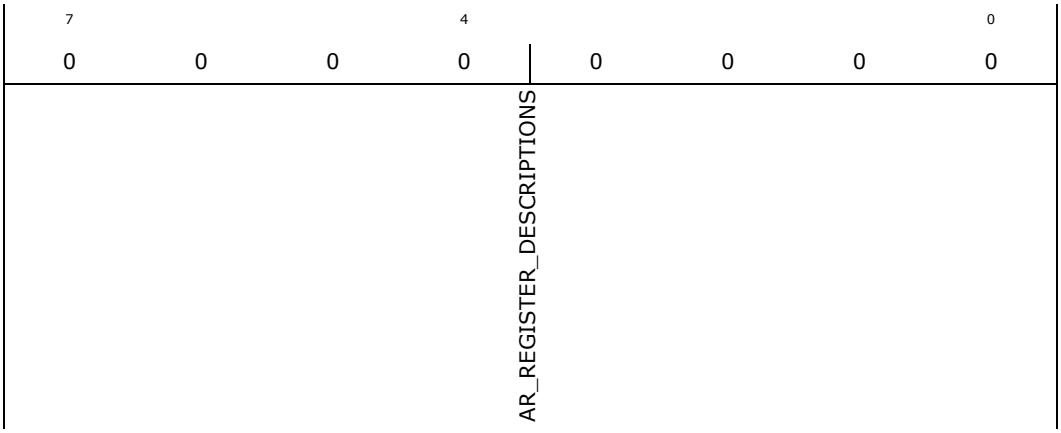
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

AR: [GTTMMADR_LSB + 2BF20h] + 3C1h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**AR_REGISTER_DESCRIPTIONS:** AR indexed register descriptions

3.1.5 SRX—Offset 3C4h

Sequencer Index

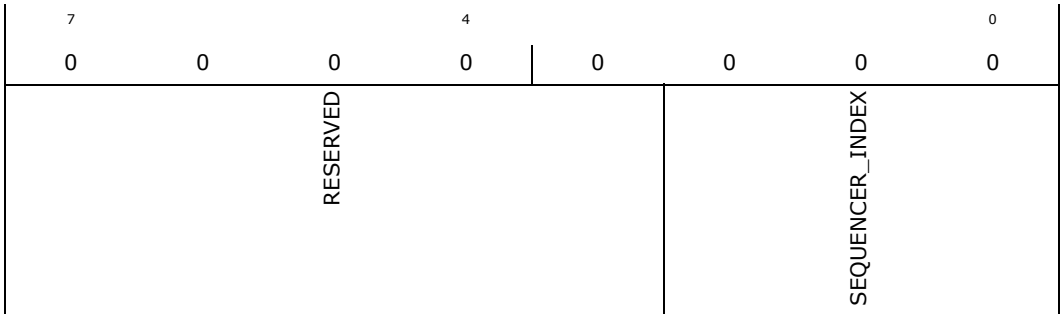
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SRX: [GTTMMADR_LSB + 2BF20h] + 3C4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0b RW	**RESERVED:** Read as 0s.
2:0	0b RW	**SEQUENCER_INDEX:** This field contains a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7. Notes: SR02 is referred to in the VGA standard as the Map Mask Register. However, the word map is used with multiple meanings in the VGA standard and was, therefore, deemed too confusing; hence, the reason for calling it the Plane Mask Register. SR07 is a standard VGA register that was not documented by IBM. It is not a graphics controller extension.

3.1.6 SR—Offset 3C5h

SR index registers

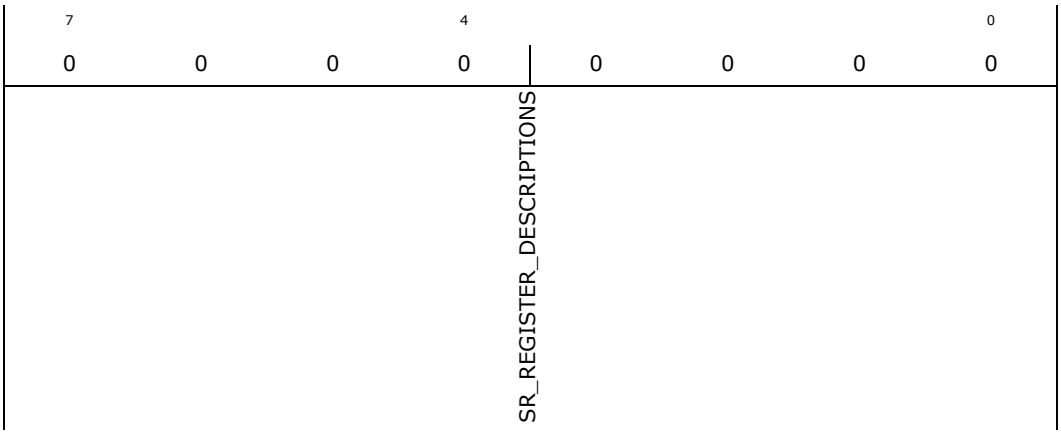
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SR: [GTTMMADR_LSB + 2BF20h] + 3C5h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**SR_REGISTER_DESCRIPTIONS:** SR indexed register descriptions

3.1.7 DACMASK—Offset 3C6h

Pixel Data Mask Register

Access Method

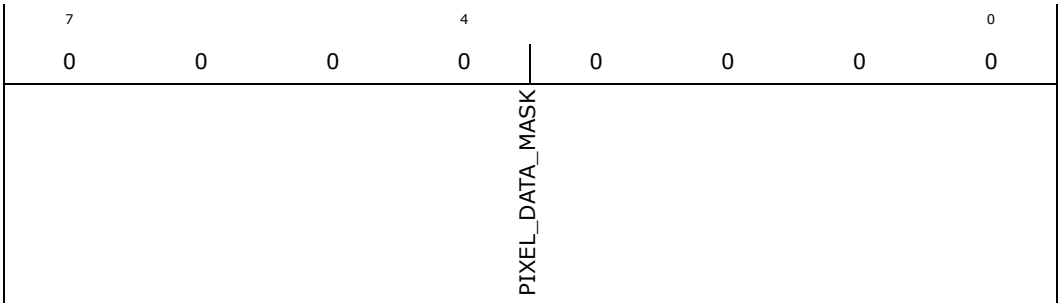
Type: Memory Mapped I/O Register (Size: 8 bits)

DACMASK: [GTTMMADR_LSB + 2BF20h] + 3C6h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**PIXEL_DATA_MASK:** In indexed-color mode, the 8 bits of this register are logically ANDed with the 8 bits of pixel data received from the frame buffer for each pixel. The result of this ANDing process becomes the actual index used to select color data positions within the palette. This has the effect of limiting the choice of color data positions that may be specified by the incoming 8-bit data. 0 = Corresponding bit in the resulting 8-bit index being forced to 0. 1 = Allows the corresponding bit in the resulting index to reflect the actual value of the corresponding bit in the incoming 8-bit pixel data.

3.1.8 DACWX—Offset 3C8h

Palette Write Index Register

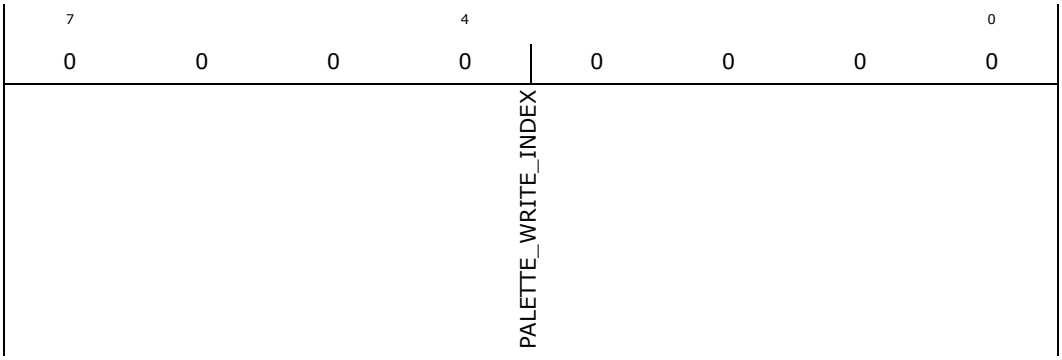
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

DACWX: [GTTMMADR_LSB + 2BF20h] + 3C8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b WO	**PALETTE_WRITE_INDEX:** The 8-bit index value programmed into this register chooses which of 256 standard color data positions within the palette are to be made accessible for being written via the Palette Data Register (DACDATA). The index value held in this register is automatically incremented when all three bytes of the color data position selected by the current index have been written. This register allows access to the palette even when running non-VGA display modes.

3.1.9 DACDATA—Offset 3C9h

Palette Data Register

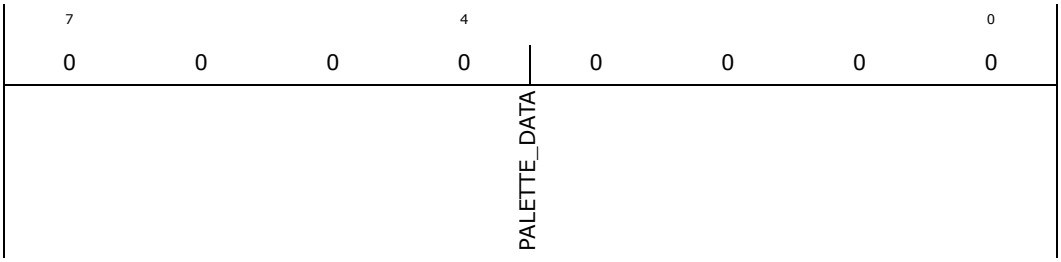
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

DACDATA: [GTTMMADR_LSB + 2BF20h] + 3C9h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**PALETTE_DATA:** This byte-wide data port provides read or write access to the three bytes of data of each color data position selected using the Palette Read Index Register (DACRX) or the Palette Write Index Register (DACWX). The three bytes in each color data position are read or written in three successive read or write operations. The first byte read or written specifies the intensity of the red component of the color specified in the selected color data position. The second byte is for the green component, and the third byte is for the blue component. When writing data to a color data position, all three bytes must be written before the hardware will actually update the three bytes of the selected color data position. When reading or writing to a color data position, ensure that neither the Palette Read Index Register (DACRX) or the Palette Write Index Register (DACWX) are written to before all three bytes are read or written. A write to either of these two registers causes the circuitry that automatically cycles through providing access to the bytes for red, green and blue components to be reset such that the byte for the red component is the one that will be accessed by the next read or write operation via this register. This register allows access to the palette even when running non-VGA display modes. Writes to the palette can cause sparkle if not done during inactive video periods. This sparkle is caused by an attempt to write and read the same address on the same cycle. Anti-sparkle circuits will substitute the previous pixel value for the read output.

3.1.10 FCR (FCR_Read)—Offset 3CAh

Feature Control

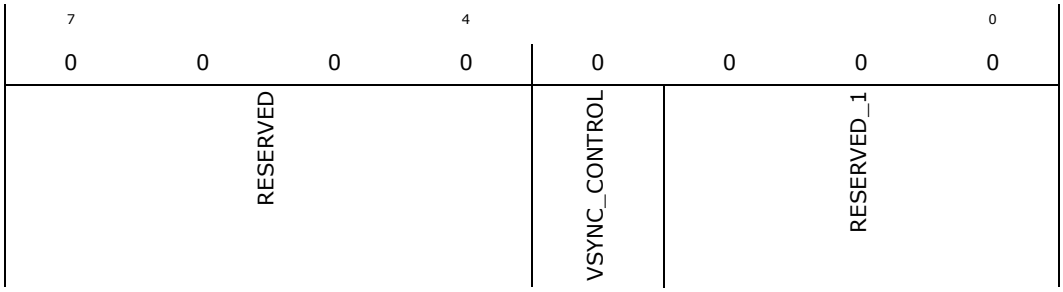
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

FCR_Read: [GTTMMADR_LSB + 2BF20h] + 3CAh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:4	0b RW	**RESERVED:** Read as 0.
3	0b RW	**VSYNC_CONTROL:** This bit is provided for compatibility only and has no other function. Reads and writes to this bit have no effect other than to change the value of this bit. The previous definition of this bit selected the output on the VSYNC pin. 0 = Was used to set VSYNC out put on the VSYNC pin (default). 1 = Was used to set the log i cal 'OR' of VSYNC and Display Enable output on the VSYNC pin. This capability was not typically very useful..
2:0	0b RW	**RESERVED_1:** Read as 0.

3.1.11 MSR (MSR_READ)—Offset 3CCh

Miscellaneous Output

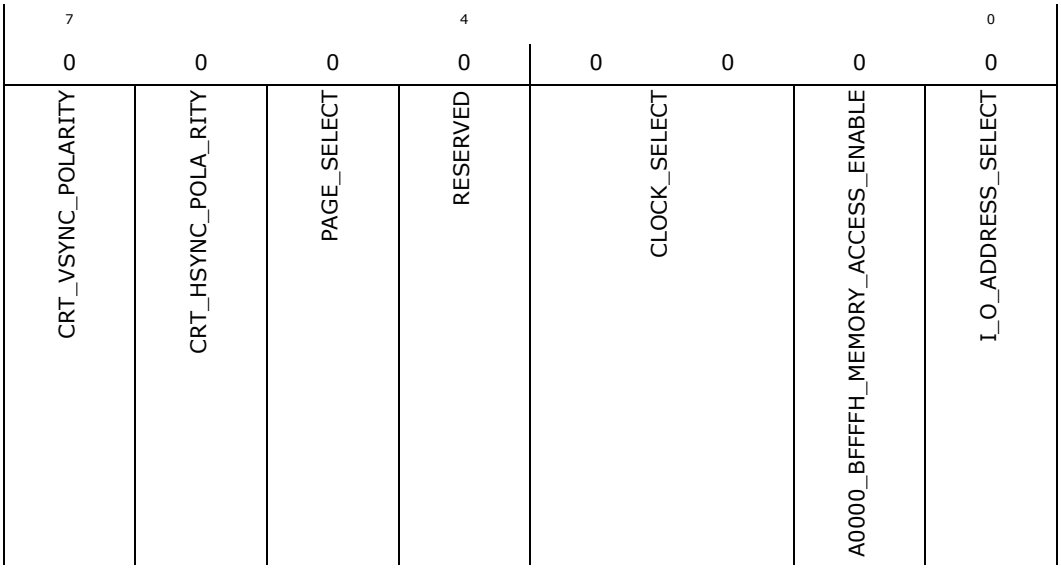
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

MSR_READ: [GTTMMADR_LSB + 2BF20h] + 3CCh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RW	**CRT_VSYNC_POLARITY:** This is a legacy function that is used in native VGA modes. For most cases, sync polarity will be controlled by the port control bits. The VGA settings can be optionally selected for compatibility with the original VGA when used in the VGA native mode. Sync polarity was used in VGA to signal the monitor how many lines of active display are being generated. 0 = Positive Polarity (default). 1 = Negative Polarity.
6	0b RW	**CRT_HSYNC_POLA_RITY:** This is a legacy function that is used in native VGA modes. For most cases, sync polarity will be controlled by the port control bits. The VGA settings can be optionally selected for compatibility with the original VGA when used in the VGA native mode. 0 = Positive Polarity (default). 1 = Negative Polarity
5	0b RW	**PAGE_SELECT:** In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KB page in dis play memory for CPU access: 0 = Upper page (default) 1 = Lower page. Selects between two 64KB pages of frame buffer memory during standard VGA odd/even modes (modes 0h through 5h). Bit 1 of register GR06 can also program this bit in other modes. Note that this bit is would normally set to 1 by the software.
4	0b RW	**RESERVED:** Read as 0.
3:2	0b RW	**CLOCK_SELECT:** These bits can select the dot clock source for the CRT interface. The bits should be used to select the dot clock in standard native VGA modes only. When in the centering or upper left corner modes, these bits should be set to have no effect on the clock rate. The actual frequencies that these bits select, if they have any affect at all, is programmable through the DPLL registers that default to the standard values used for VGA. 00 = CLK0, 25.175 MHz (for standard VGA modes with 640 pixel (8-dot) horizontal resolution) (default) 01 = CLK1, 28.322 MHz. (for standard VGA modes with 720 pixel (9-dot) horizontal resolution) 10 = Was used to select an external clock (now unused) 11 = Reserved

Bit Range	Default & Access	Description
1	0b RW	**A0000_BFFFFH_MEMORY_ACCESS_ENABLE:** VGA Compatibility bit enables access to local video memory (frame buffer) at A0000(BFFFFh. When disabled, accesses to VGA memory are blocked in this region. This bit is independent of and does not block CPU access to the video linear frame buffer at other addresses. Note that it is typical for AGP chipsets to shadow this register to allow proper steering of memory accesses to the proper bus. 0 = Prevent CPU access to memory/registers/ROM through the A0000-BFFFF VGA memory aperture (default). 1 = Allow CPU access to memory/registers/ ROM through the A0000-BFFFF VGA memory aperture. This memory must be mapped as UC by the CPU; see VGA Host Access Memory Munging in Display and Overlay Functions.
0	0b RW	**I_O_ADDRESS_SELECT:** This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01). Presently ignored (whole range is claimed), but will ignore 3Bx for color configuration or 3Dx for monochrome. Note that it is typical in AGP chipsets to shadow this bit and properly steer I/O cycles to the proper bus for operation where a MDA exists on another bus such as ISA. 0 = Select 3Bxh I/O address (MDA emulation) (default). 1 = Select 3Dxh I/O address (CGA emulation).

3.1.12 GRX—Offset 3CEh

GRX Graphics Controller Index Register

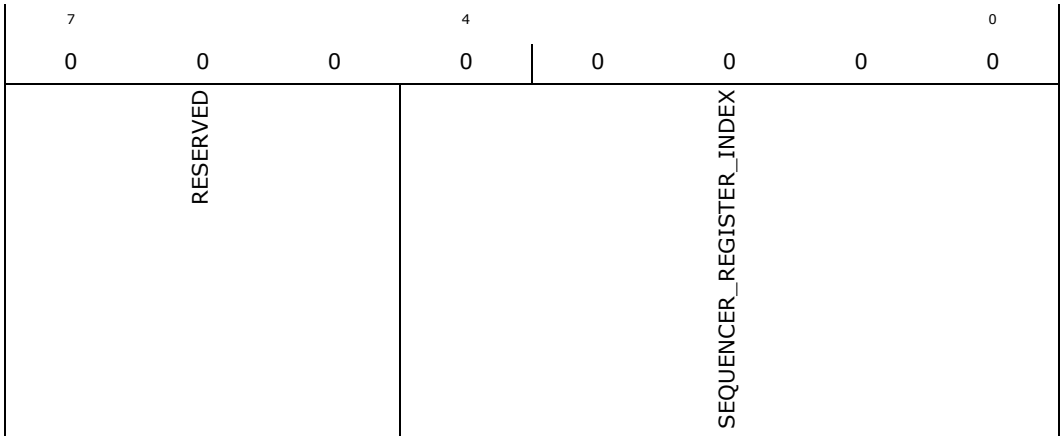
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

GRX: [GTTMMADR_LSB + 2BF20h] + 3CEh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:5	0b RW	**RESERVED:** Read as 0.
4:0	0b RW	**SEQUENCER_REGISTER_INDEX:** This field selects any one of the graphics controller registers (GR00-GR11]) to be accessed via the data port at I/O (or memory offset) location 3CFh.

3.1.13 GR—Offset 3CFh

GR index registers

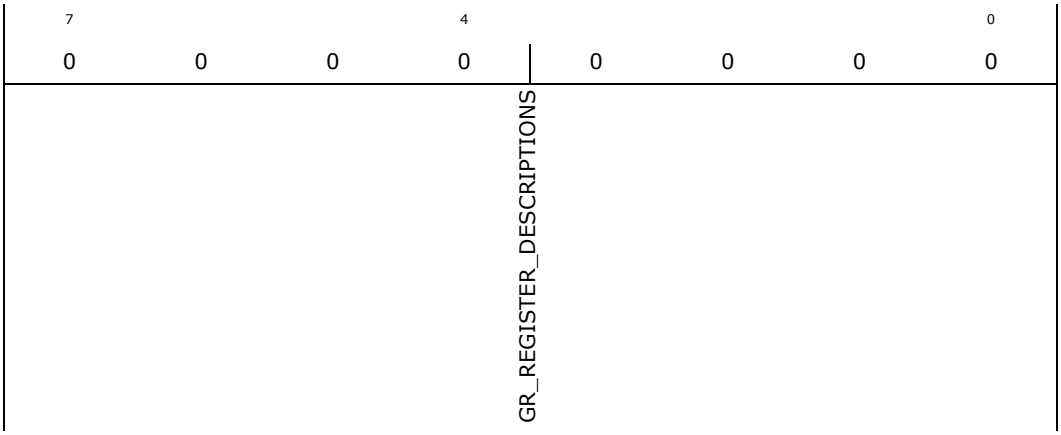
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

GR: [GTTMMADR_LSB + 2BF20h] + 3CFh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**GR_REGISTER_DESCRIPTIONS:** GR indexed register descriptions

3.1.14 CRX (CRX_CGA)—Offset 3D4h

CRT Controller Index Register

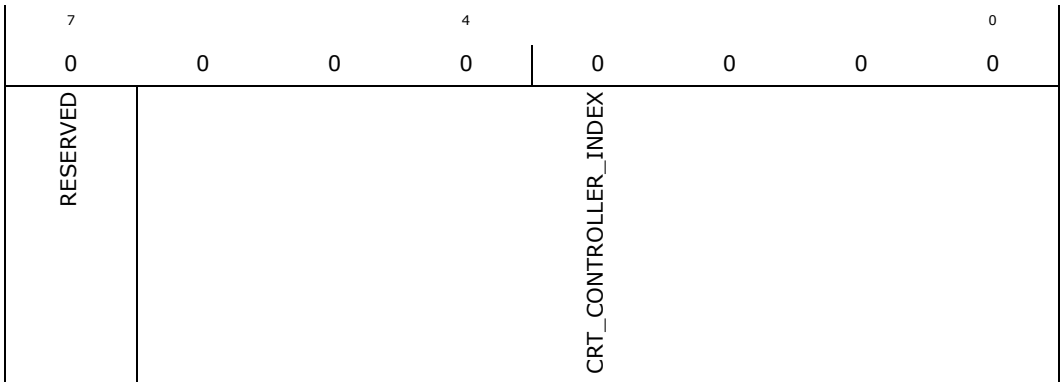
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

CRX_CGA: [GTTMMADR_LSB + 2BF20h] + 3D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RW	**RESERVED:** Read as 0.
6:0	0b RW	**CRT_CONTROLLER_INDEX:** These 7 bits are used to select any one of the CRT controller registers to be accessed via the data port at I/O location 3B5h or 3D5h, depending upon whether the graphics system is configured for MDA or CGA emulation. The data port memory address offsets are 3B5h/3D5h.

3.1.15 CR (CR_CGA)—Offset 3D5h

CR index registers

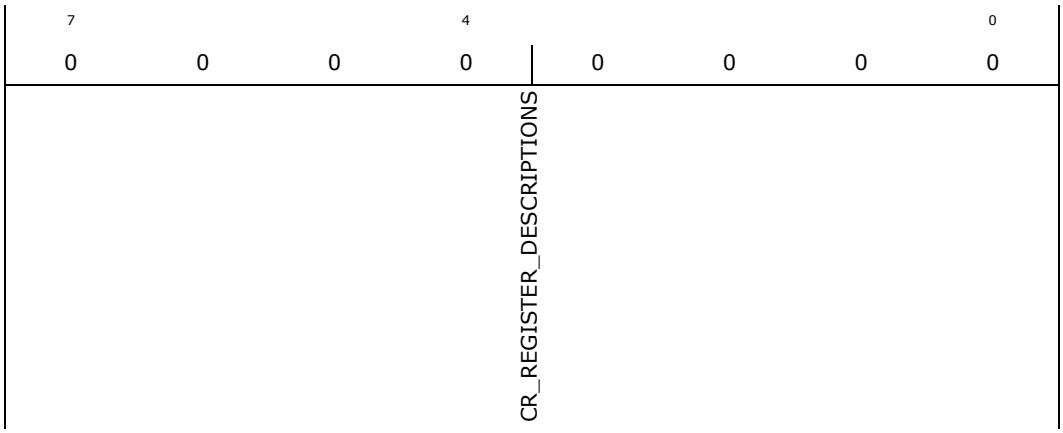
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

CR_CGA: [GTTMMADR_LSB + 2BF20h] + 3D5h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**CR_REGISTER_DESCRIPTIONS:** CR indexed register descriptions

3.1.16 GPIOCTL_0—Offset 5010h

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

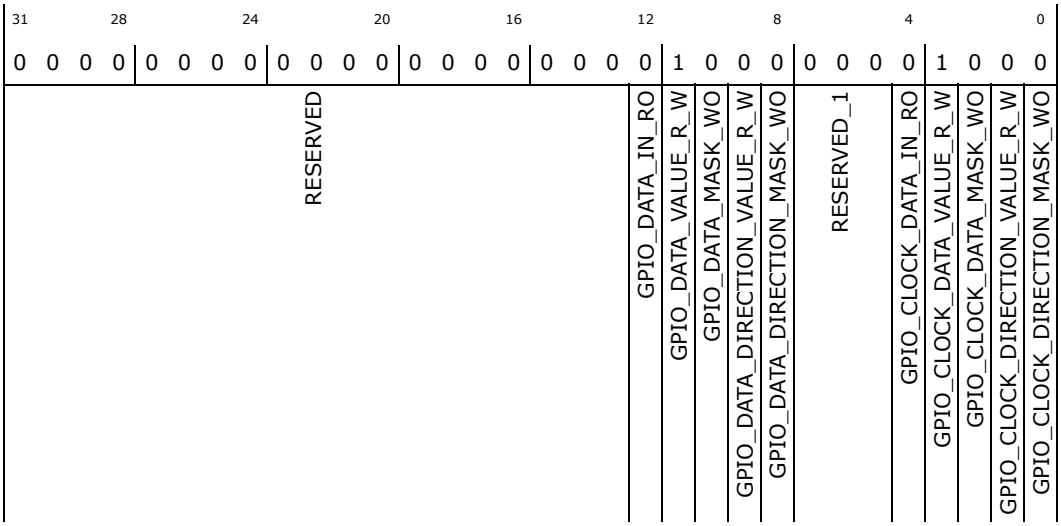
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

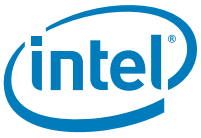
GPIOCTL_0: [GTTMMADR_LSB + 2BF20h] + 5010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000808h



Bit Range	Default & Access	Description
31:13	0b RW	**RESERVED:** Reserved.
12	0b RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only



Bit Range	Default & Access	Description
11	1b RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0b WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0b RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0b WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0b RW	**RESERVED_1:** must be written with zeros.
4	0b RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	1b RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
2	0b WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0b RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.

Bit Range	Default & Access	Description
0	0b WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

3.1.17 GPIOCTL_1—Offset 5014h

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

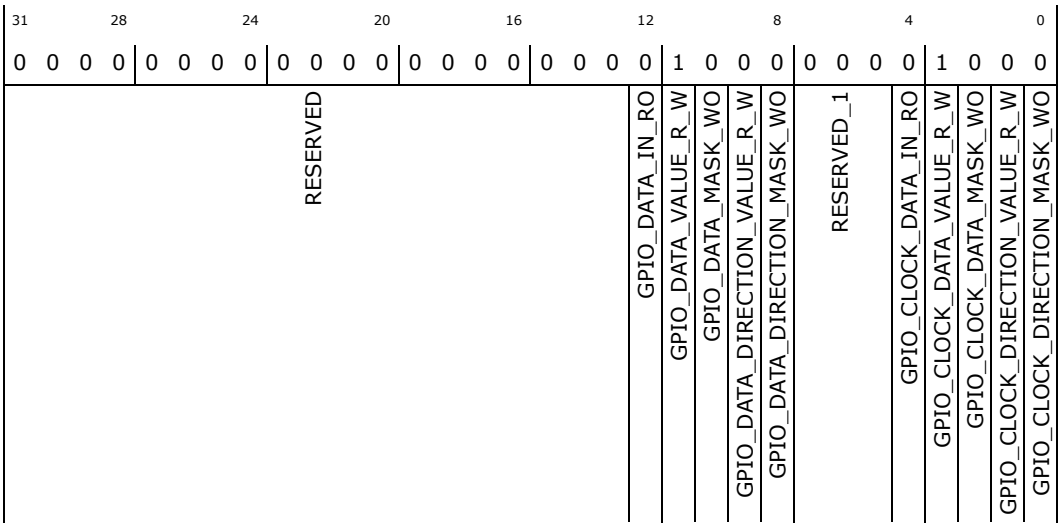
Type: Memory Mapped I/O Register (Size: 32 bits)

GPIOCTL_1: [GTTMMADR_LSB + 2BF20h] + 5014h

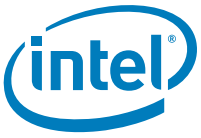
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000808h



Bit Range	Default & Access	Description
31:13	0b RW	**RESERVED:** Reserved.
12	0b RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only



Bit Range	Default & Access	Description
11	1b RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0b WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0b RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0b WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0b RW	**RESERVED_1:** must be written with zeros.
4	0b RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	1b RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
2	0b WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0b RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.

Bit Range	Default & Access	Description
0	0b WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

3.1.18 GPIOCTL_2—Offset 5018h

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

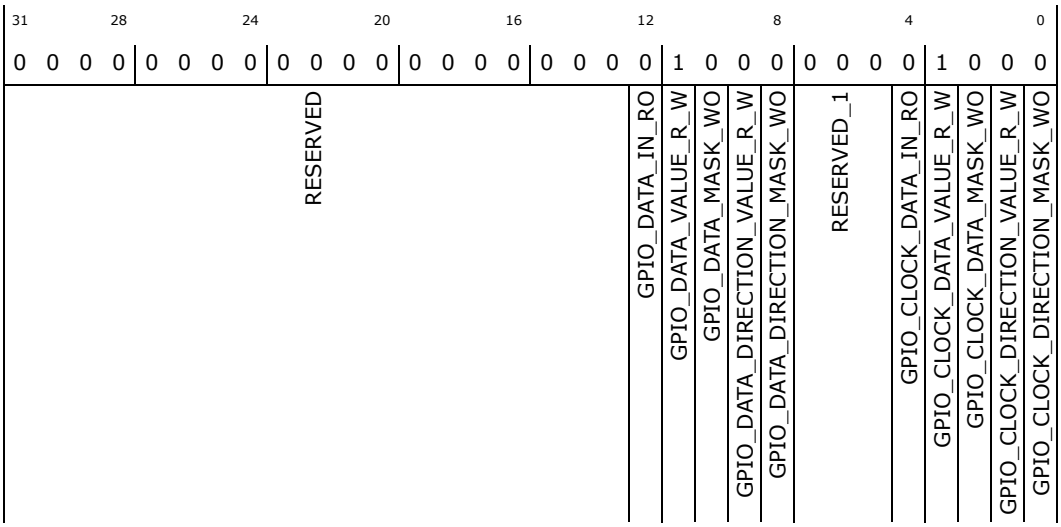
Type: Memory Mapped I/O Register (Size: 32 bits)

GPIOCTL_2: [GTTMMADR_LSB + 2BF20h] + 5018h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000808h



Bit Range	Default & Access	Description
31:13	0b RW	**RESERVED:** Reserved.
12	0b RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only

Bit Range	Default & Access	Description
11	1b RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0b WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0b RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0b WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0b RW	**RESERVED_1:** must be written with zeros.
4	0b RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	1b RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
2	0b WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0b RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.

Bit Range	Default & Access	Description
0	0b WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

3.1.19 GPIOCTL_3—Offset 501Ch

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

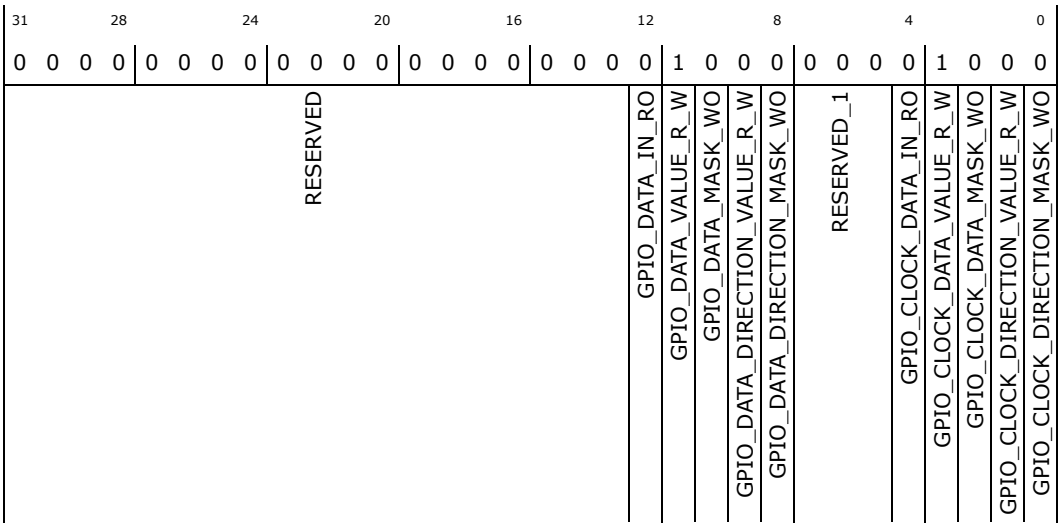
Type: Memory Mapped I/O Register (Size: 32 bits)

GPIOCTL_3: [GTTMMADR_LSB + 2BF20h] + 501Ch

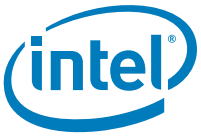
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000808h



Bit Range	Default & Access	Description
31:13	0b RW	**RESERVED:** Reserved.
12	0b RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only



Bit Range	Default & Access	Description
11	1b RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0b WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0b RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0b WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0b RW	**RESERVED_1:** must be written with zeros.
4	0b RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	1b RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
2	0b WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0b RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.

Bit Range	Default & Access	Description
0	0b WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

3.1.20 GPIOCTL_4—Offset 5020h

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

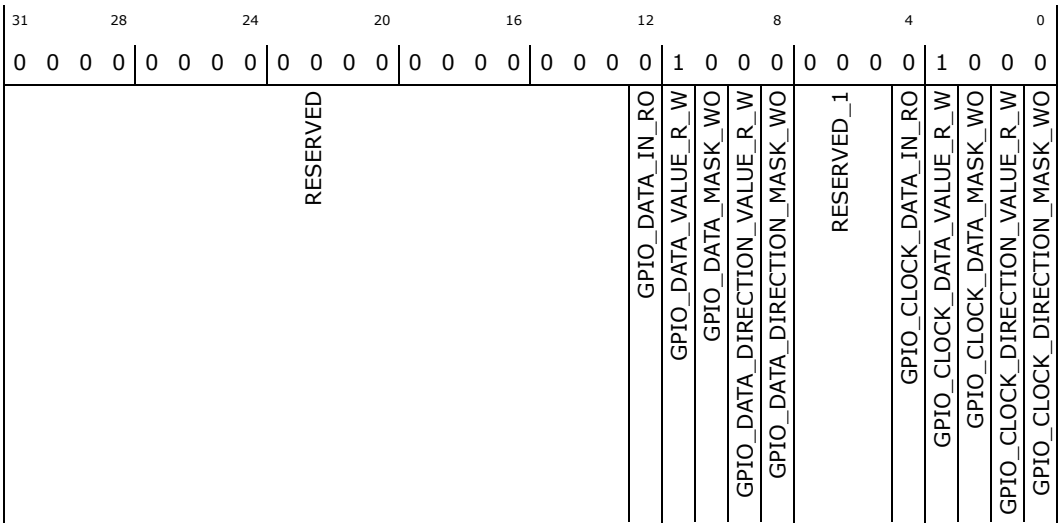
Type: Memory Mapped I/O Register (Size: 32 bits)

GPIOCTL_4: [GTTMMADR_LSB + 2BF20h] + 5020h

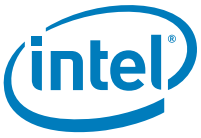
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000808h



Bit Range	Default & Access	Description
31:13	0b RW	**RESERVED:** Reserved.
12	0b RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only



Bit Range	Default & Access	Description
11	1b RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0b WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0b RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0b WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0b RW	**RESERVED_1:** must be written with zeros.
4	0b RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	1b RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
2	0b WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0b RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.

Bit Range	Default & Access	Description
0	0b WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

3.1.21 GMBUS0—Offset 5100h

GMBUS Clock/Port Select gmbus clock and port select (gmbus_register.v reg_gmbus0)

Access Method

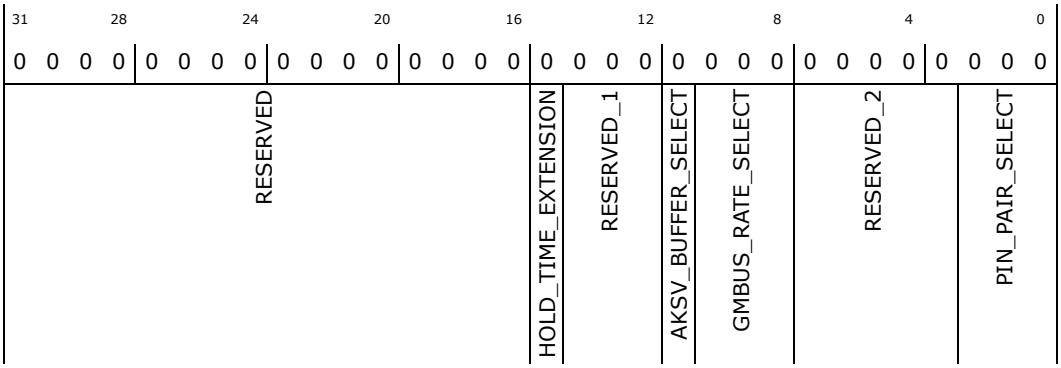
Type: Memory Mapped I/O Register (Size: 32 bits)

GMBUS0: [GTTMMADR_LSB + 2BF20h] + 5100h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15	0b RW	**HOLD_TIME_EXTENSION:** This bit selects the hold time on the data line driven from the GMCH. 0 = Hold time of 0ns 1 = Hold time of 300 ns
14:12	0b RW	**RESERVED_1:** Reserved.
11	0b RW	**AKSV_BUFFER_SELECT:** [DevBLC, DevCTG, DevCDV] This bit selects whether the data to be written over GMBUS comes from the Aksv buffer for HDCP authentication, or from the GMBUS data buffer. Please note that when writing data from the Aksv buffer, all GMBUS protocol must be followed, including indicating the number of bytes to be transferred during the DATA phase of a GMBUS cycle. 0 (Default) Use the GMBUS data buffer (GMBUS3) for data transmission 1 Use the Aksv data buffer (GMBUS6 and GMBUS7) for data transmission. [DevBW, DevCL] Reserved:

Bit Range	Default & Access	Description
10:8	0b RW	**GMBUS_RATE_SELECT:** These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. It should only be changed when between transfers when the GMBUS is idle. 1xx = Reserved. 000 = 100 KHz 001 = 50 KHz 010 = 400 KHz 011 = 1 MHz for SDVO
7:3	0b RW	**RESERVED_2:** Reserved.
2:0	0b RW	**PIN_PAIR_SELECT:** This field selects an GMBUS pin pair for use in the GMBUS communication. Use the table above to determine which pin pairs are available for a particular device and the intended function of that pin pair. Note that it is not a straight forward mapping of port numbers to pair select numbers. 000 = None (disabled) 001 = MIPI I2C use 010 = Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK) 011 = Reserved 100 = DP/HDMI port C Use [DevCTG] 101 = sDVO/HDMI Use 110 = Reserved 111 = D connector control signals

3.1.22 GMBUS1—Offset 5104h

GMBUS Command and Status gmbus command and status (gmbus_register.v reg_gmbus1)

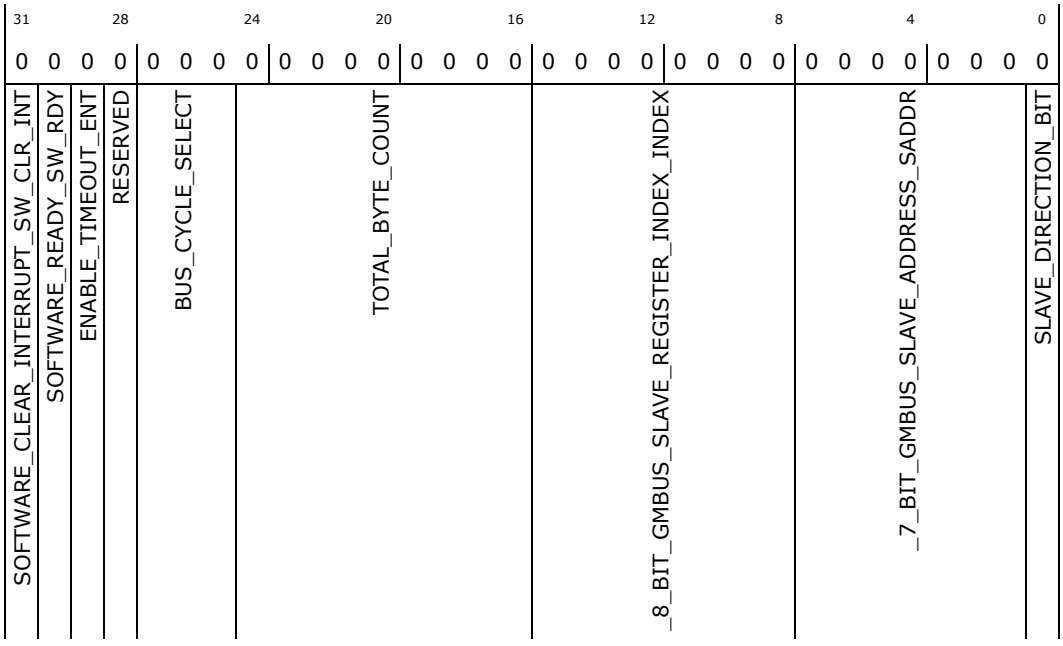
Access Method

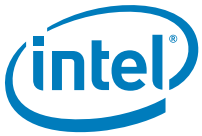
Type: Memory Mapped I/O Register (Size: 32 bits)

GMBUS1: [GTTMMADR_LSB + 2BF20h] + 5104h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31	0b RW	**SOFTWARE_CLEAR_INTERRUPT_SW_CLR_INT:** This bit must be clear for normal operation. Setting the bit , then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK. 0 = If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur. 1 = Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.
30	0b RW	**SOFTWARE_READY_SW_RDY:** Data handshake bit used in conjunction with HW_RDY bit. 0 = De-asserted via the assertion event for HW_RDY bit 1 = When asserted by software, results in de-assertion of HW_RDY bit
29	0b RW	**ENABLE_TIMEOUT_ENT:** Enables timeout for slave response. When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set. 0 = disable timeout counter 1 = enable timeout counter
28	0b RW	**RESERVED:** Reserved.
27:25	0b RW	**BUS_CYCLE_SELECT:** 000 = No GMBUS cycle is generated. 001 = GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT 010 = Reserved 011 = GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT 100 = Generates a STOP if currently in a WAIT or after the completion of the current byte if active. 101 = GMBUS cycle is generated without an INDEX and with a STOP 110 = Reserved 111 = GMBUS cycle is generated with an INDEX and with a STOP GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase. A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase. The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle. This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase: Note that the three bits can be decoded as follows: 27 = STOP generated 26 = INDEX used 25 = cycle ends in a WAIT
24:16	0b RW	**TOTAL_BYTE_COUNT:** (9-bits). This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle. The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select). Do not change the value of this field during GMBUS cycles transactions.
15:8	0b RW	**_8_BIT_GMBUS_SLAVE_REGISTER_INDEX_INDEX:** This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair. It only has an effect if the enable Index bit is set. Do not change this field during a GMBUS transaction.

Bit Range	Default & Access	Description
7:1	0b RW	**_7_BIT_GMBUS_SLAVE_ADDRESS_SADDR:** When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (xx) are the two MSBs of the 10-bit address) and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10-bit slave address. Special Slave Addresses 0000 000R = General Call Address 0000 000W = Start byte 0000 001x = CBUS Address 0000 010x = Reserved 0000 011x = Reserved 0000 1xxx = Reserved 1111 1xxx = Reserved 1111 0xxx = 10-Bit addressing
0	0b RW	**SLAVE_DIRECTION_BIT:** When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. 1 = Indicates that a Read from the slave device operation is to be performed. 0 = Indicates that a Write to slave device operation is to be performed.

3.1.23 GMBUS2—Offset 5108h

GMBUS Status Register gmbus status (gmbus_register.v reg_gmbus2)

Access Method

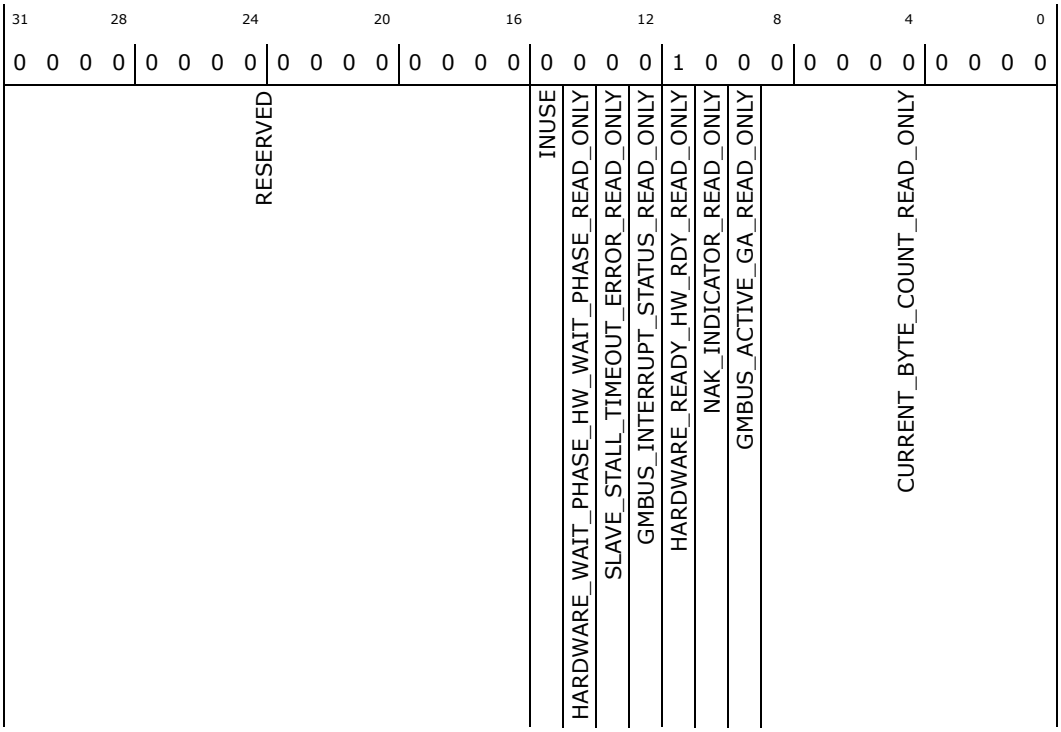
Type: Memory Mapped I/O Register (Size: 32 bits)

GMBUS2: [GTTMMADR_LSB + 2BF20h] + 5108h

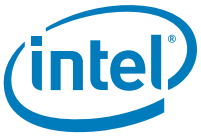
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000800h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15	0b RW/1C	**INUSE:** 0 = read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect. 1 = read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and In use . Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0. Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads that don t know how to synchronize their use of this resource that may need to use the GMBUS logic. Writing a one to this bit is software s indication that the software use of this resource is now terminated and it is available for other clients. AccessType: One to clear
14	0b RO	**HARDWARE_WAIT_PHASE_HW_WAIT_PHASE_READ_ONLY:** 0 = The GMBUS engine is not in a wait phase. 1 = Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP. Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction on the GMBUS. AccessType: Read Only



Bit Range	Default & Access	Description
13	0b RO	**SLAVE_STALL_TIMEOUT_ERROR_READ_ONLY:** This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit. 0 = No slave timeout has occurred. 1 = A slave acknowledge timeout has occurred AccessType: Read Only
12	0b RO	**GMBUS_INTERRUPT_STATUS_READ_ONLY:** This bit indicates that an event that causes a GMBUS interrupt has occurred. 0 = The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the SW_CLR_INT bit. 1 = GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register. [DevCDV, DevCTG]: Reserved AccessType: Read Only
11	1b RO	**HARDWARE_READY_HW_RDY_READ_ONLY:** This provides a method of detecting when the current software client routine can proceed with the next step in a sequence of GMBUS operations. This data handshake bit is used in conjunction with the SW_RDY bit. When this bit is changed to asserted by the GMBUS controller, it results in the de-assertion of the SW_RDY bit. 0 = Condition required for assertion has not occurred or when this bit was a one and: SW_RDY bit has been asserted. During a GMBUS read transaction, after the each read of the data register. During a GMBUS write transaction, after each write of the data register. SW_CLR_INT bit has been cleared. 1 = This bit is asserted under the following conditions: After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit. When an active GMBUS cycle has terminated with a STOP. When during a GMBUS write transaction, the data register needs and can accept another four bytes of data. During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data. This bit resumes to normal operation when the SW_CLR_INT bit is written to a 0. AccessType: Read Only
10	0b RO	**NAK_INDICATOR_READ_ONLY:** Was previously called Slave Acknowledge Timeout Error SATOER. 0 = No bus error has been detected or SW_CLR_INT has been written as a zero since the last bus error. 1 = Set by hardware if any expected device acknowledge is not received from the slave within the timeout. AccessType: Read Only
9	0b RO	**GMBUS_ACTIVE_GA_READ_ONLY:** This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not. 0 = The GMBUS controller is currently IDLE. 1 = This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE. AccessType: Read Only
8:0	0b RO	**CURRENT_BYTE_COUNT_READ_ONLY:** Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware. Set to zero at the start of a GMBUS transaction data transfer and incremented after the completion of each byte of the data phase. Note that because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register. AccessType: Read Only

3.1.24 GMBUS3—Offset 510Ch

GMBUS Data Buffer gmbus data buffer (gmbus_register.v reg_gmbus3)

Access Method

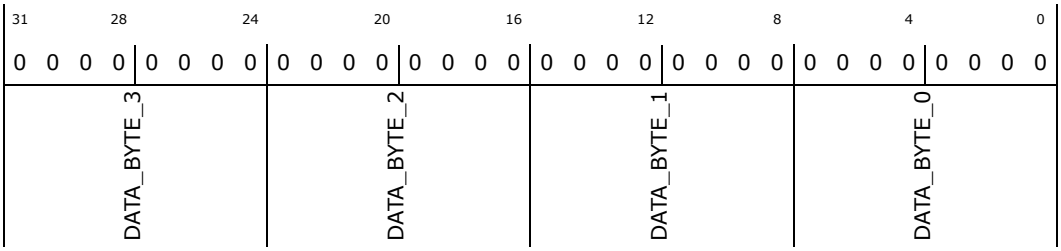
Type: Memory Mapped I/O Register (Size: 32 bits)

GMBUS3: [GTTMMADR_LSB + 2BF20h] + 510Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**DATA_BYTE_3:** gmbus data buffer DATA Byte 3
23:16	0b RW	**DATA_BYTE_2:** gmbus data buffer DATA Byte 2
15:8	0b RW	**DATA_BYTE_1:** gmbus data buffer DATA Byte 1
7:0	0b RW	**DATA_BYTE_0:** gmbus data buffer DATA Byte 0

3.1.25 GMBUS4—Offset 5110h

GMBUS Interrupt Mask gmbus interrupt mask (gmbus_register.v reg_gmbus4)

Access Method

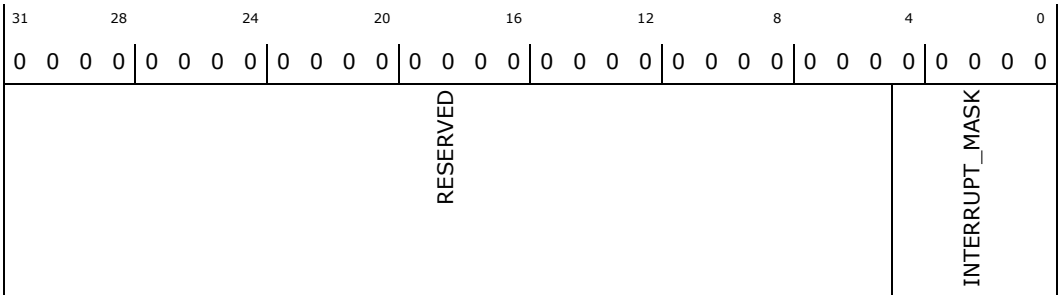
Type: Memory Mapped I/O Register (Size: 32 bits)

GMBUS4: [GTTMMADR_LSB + 2BF20h] + 5110h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RW	**RESERVED:** Reserved.
4:0	0b RW	**INTERRUPT_MASK:** This field specifies which GMBUS interrupts events may contribute to the setting of gmbus interrupt status bit in second level interrupt status register PIPEASTAT. Bit 4: GMBUS Slave stall timeout Bit 3: GMBUS NAK Bit 2: GMBUS Idle Bit 1: Hardware wait (GMBUS cycle without a stop has completed) Bit 0: Hardware ready (Data has been transferred) 0 = Disable this type of GMBUS interrupt 1 = Enable this type of GMBUS interrupt

3.1.26 GMBUS5—Offset 5120h

2 Byte Index Register gmbus index (gmbus_register.v reg_gmbus5)

Access Method

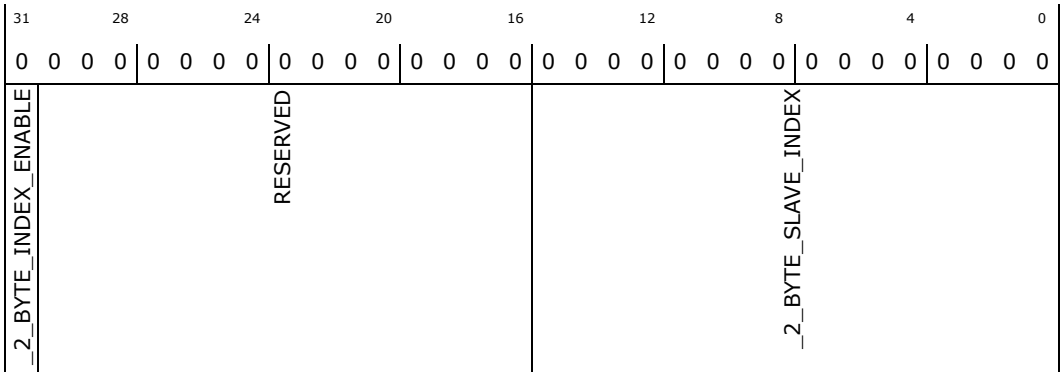
Type: Memory Mapped I/O Register (Size: 32 bits)

GMBUS5: [GTTMMADR_LSB + 2BF20h] + 5120h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**_2_BYTE_INDEX_ENABLE:** When this bit is asserted (1), then bits 15:00 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1(15:8) are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
30:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**_2_BYTE_SLAVE_INDEX:** This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted (1).

3.1.27 GMBUS6—Offset 5130h

GMBUS Aksv Buffer Low [DevBLC, DevCTG, DevCDV] gmbus data buffer (gmbus_register.v reg_gmbus6)

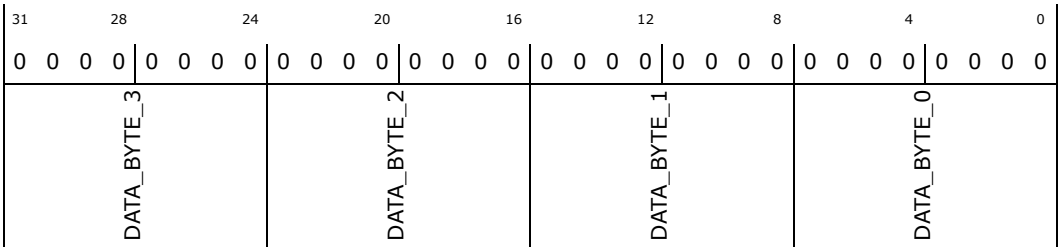
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GMBUS6: [GTTMMADR_LSB + 2BF20h] + 5130h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b WO	**DATA_BYTE_3:** gmbus data buffer DATA Byte 3
23:16	0b WO	**DATA_BYTE_2:** gmbus data buffer DATA Byte 2
15:8	0b WO	**DATA_BYTE_1:** gmbus data buffer DATA Byte 1
7:0	0b WO	**DATA_BYTE_0:** gmbus data buffer DATA Byte 0

3.1.28 GMBUS7—Offset 5134h

GMBUS Aksv Buffer High [DevBLC, DevCTG, DevCDV] gmbus data buffer (gmbus_register.v reg_gmbus7)

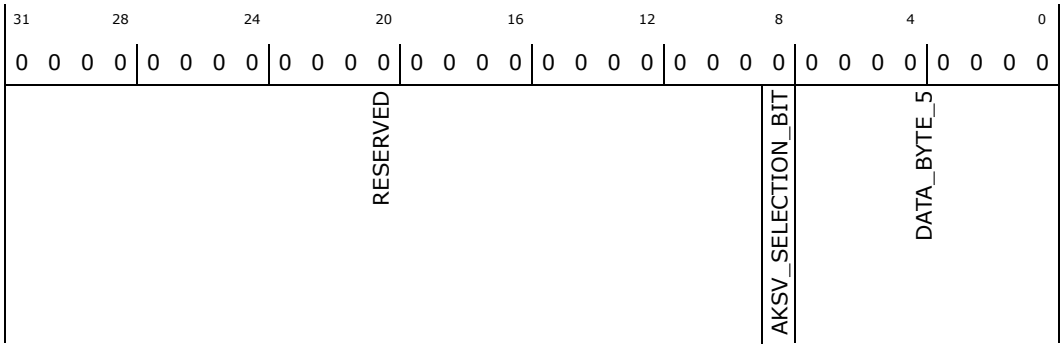
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GMBUS7: [GTTMMADR_LSB + 2BF20h] + 5134h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b WO	**RESERVED:** MBZ
8	0b WO	**AKSV_SELECTION_BIT:** [DevVLVP]: • 0 = The fuse value of the Aksv is used. • 1 = The register value of the Aksv is used. Aksv Selection Bit [DevELK, DevCDV]: • 0 = The register value of the Aksv is used. • 1 = The fuse value of the Aksv is used. [DevBLC, DevCTG] Reserved
7:0	0b WO	**DATA_BYTE_5:** gmbus data buffer DATA Byte 5

3.1.29 DPLLA_CTRL—Offset 6014h

DPLL A Control Register DPLL A Control (cpdmmreg.v reg03_lt)

Access Method

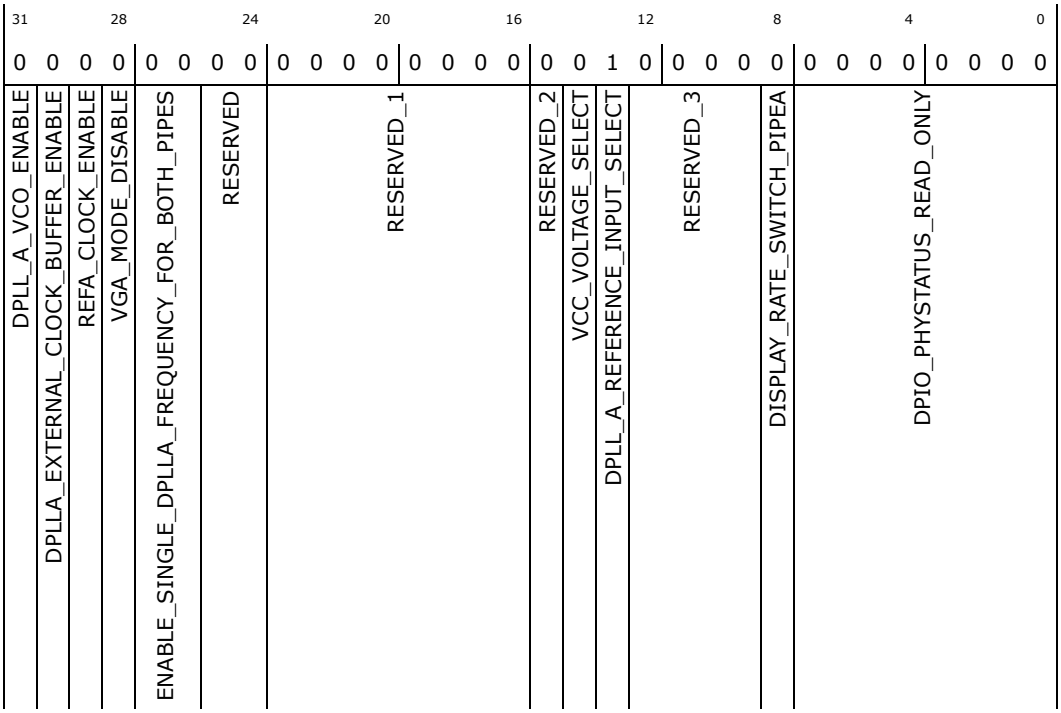
Type: Memory Mapped I/O Register (Size: 32 bits)

DPLLA_CTRL: [GTTMMADR_LSB + 2BF20h] + 6014h

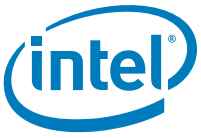
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00002000h



Bit Range	Default & Access	Description
31	0b RW	**DPLL_A_VCO_ENABLE:** Disabling the PLLA will cause the display dot clock to stop. 0 = DPLLA is disabled in its lowest power state (default) 1 = DPLLA is enabled and operational (42usec until lock without calibration and 110usec for calibration)
30	0b RW	**DPLLA_EXTERNAL_CLOCK_BUFFER_ENABLE:** [DevVLVP] 0 = Disable DPLLA clock from being driven out 1 = Enable DPLLA clock to be drive out [DevCDV] Reserved DPLLA Serial DVO High Speed IO clock Enable 0 = High Speed IO Clock Disabled (default) 1 = High Speed IO Clock Enabled (must be set in Serial DVO and HDMI modes)
29	0b RW	**REFA_CLOCK_ENABLE:** [DevCDV, DevVLVP]: Indicate the reference clock of PLL A is enable 0 Disable (default) 1 Enable
28	0b RW	**VGA_MODE_DISABLE:** When in native VGA modes, writes to the VGA MSR register causes the value in the selected (by MSR bits) VGA clock control register to be loaded into the active register. This allows the VGA clock select to select the pixel frequency between the two standard VGA pixel frequencies. 0 = VGA MSR(3:2) Clock Control bits select DPLL A Frequency 1 = Disable VGA Control



Bit Range	Default & Access	Description
27:26	0b RW	**ENABLE_SINGLE_DPLLA_FREQUENCY_FOR_BOTH_PIPES:** [DevVLVP] When two pipes are enabled for eDP and both pipes can run with the same DP frequency either 162MHz or 270MHz. Setting this mode can allow using only DPLLA to feed both pipes. DPLLB should be shutdown to save power. This control is double buffered. 00 = Disabled 01 = Enabled 10 = Reserved 11 = Reserved [DevCDV] Reserved DPLLA Mode Select : Configure the DPLLA for various supported Display Modes 00 = Reserved 01 = DPLLA in DAC/Serial DVO/UDI/Integrated TV mode 10 = DPLLA in LVDS mode (Mobile devices ONLY) otherwise RESERVED 11 = DP
25:24	0b RW	**RESERVED:** [DevCDV, DevVLVP] FPA0/FPA1 P2 Clock Divide: 00 = Divide by 10. This is used when Dot Clock =(270MHz in sDVO, HDMI, or DAC modes 01 = Divide by 5. This is used when Dot Clock)270MHz 10 = Reserved 11 = Reserved For DPLLA in LVDS mode, BITS(27:26)=10 00 = Divide by 14. This is used in Single-Channel LVDS 01 = Divide by 7. This is used in Dual-Channel LVDS 10 = Reserved 11 = Reserved
23:16	0b RW	**RESERVED_1:** [DevCDV, DevVLVP] FPA0/ FPA1 P1 Post Divisor: Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b = Divide by one 00000010b = Divide by two 00000100b = Divide by three 00001000b = Divide by four 00010000b = Divide by five 00100000b = Divide by six 01000000b = Divide by seven 10000000b = Divide by Eight All other values are illegal and should not be used
15	0b RW	**RESERVED_2:** Write as zero PLLA Lock [DevCDV, DevVLVP] (RO) 1 - PLLA Lock 0 PLLA unlock
14	0b RW	**VCC_VOLTAGE_SELECT:** [DevVLVP] This control selects the VCC voltage in DPLL 0 = 1.0 V (default) 1 = voltage for LDO circuit (for TNG use) [DevCDV] Reserved
13	1b RW	**DPLL_A_REFERENCE_INPUT_SELECT:** [DevVLVP] This control selects the integrated core refclk or external OSC refclk as the input clock source to DPLL A. 0 = External refclk pad (27MHz) 1 = Integrated core refclk (default is 100 MHz) [DevCDV] Reserved PLL Reference Input Select: The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog display port or LCD panels for both the sDVO connected transmitter or the integrated LVDS. TV Clock in should be selected when driving an sDVO connected TV encoder.
12:9	0b RW	**RESERVED_3:** [DevCDV, DevVLVP] Parallel to Serial Load Pulse phase selection: Programmable select bits to choose the relative phase of the high speed (10X) DPLL clock used for generating the parallel to serial load pulse for digital display port on PCIe. The relative phase is the number of flop delays (phase 0 represents 1 flop delay) of the 1X parallel data synchronization signal in the 10X clock domain. The earliest selectable clock phase is 4. A phase selection of 10 or greater simply extends the flop delay count to sample delayed data. 0100 = use clock phase-4 0101 = use clock phase-5 0110 = use clock phase-6 (Default value) 0111 = use clock phase-7 1000 = use clock phase-8 1001 = use clock phase-9 1010 = use clock phase-10 1011 = use clock phase-11 1100 = use clock phase-12 1101 = use clock phase-13 Phases 0 through 3 are not available for Load Pulse selection. [DevCL] The following programming is recommended for Crestline based on PV timing analysis: 1101 use clock phase-13 [DevBLC, DevCTG] Reserved. Programming for load pulse is in PXP AFE config space.

Bit Range	Default & Access	Description
8	0b RW	**DISPLAY_RATE_SWITCH_PIPEA:** [DevCTG, DevCDV, DevVLVP] Switching this bit (transition 0 to 1 or 1 to 0) causes the DSP HW to disable and than enable the DPLL during vblank (2 row) in order to switch the frequency at the DPLL (new dividers stored at the DPIO which is double buffered) (This bit is only available when bits 17:16 of the PIPEACONF register are 00) [DevBW, DevCL, DevBLC] Reserved
7:0	0b RO	**DPIO_PHYSTATUS_READ_ONLY:** [DevVLVP] This field contains the two 4-bit ModPhy lane status. One for PortB and one for PortC Bit 7:4 = Port C PhyStatus[3:0] Bit 3:0 = Port B PhyStatus[3:0] [DevBW, DevCL, DevBLC, DevCDV] Reserved [DevCTG] FPA1 P1 Post Divisor: Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b - Divide by one 00000010b - Divide by two 00000100b - Divide by three 00001000b - Divide by four 00010000b - Divide by five 00100000b - Divide by six 01000000b - Divide by seven 10000000b - Divide by Eight All other values are illegal and should not be used AccessType: Read Only

3.1.30 DPLLB_CTRL—Offset 6018h

DPLL B Control Registers DPLL B Control (cpdmmreg.v reg04_lt)

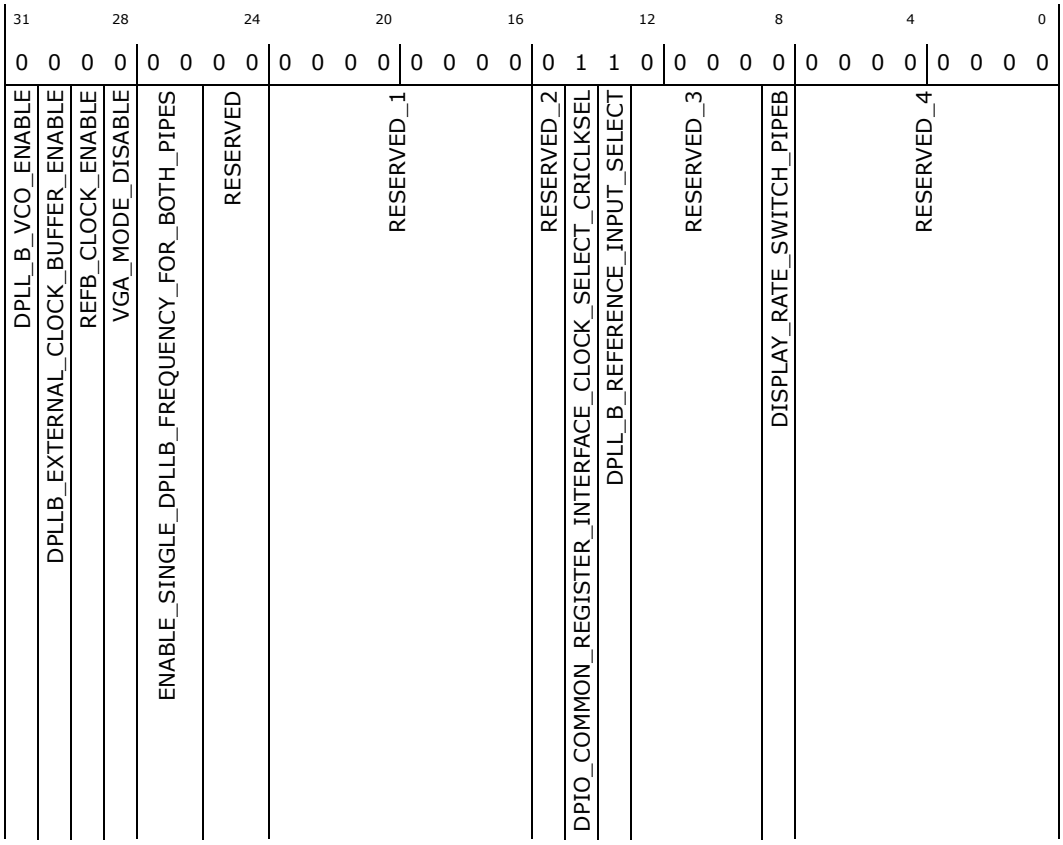
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

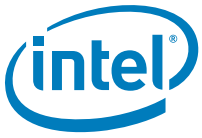
DPLLB_CTRL: [GTTMMADR_LSB + 2BF20h] + 6018h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00006000h



Bit Range	Default & Access	Description
31	0b RW	**DPLL_B_VCO_ENABLE:** Disabling the PLLB will cause the display dot clock to stop. 0 = DPLLB is disabled in its lowest power state (default) 1 = DPLLB is enabled and operational (42usec until lock without calibration and 110usec for calibration)
30	0b RW	**DPLLB_EXTERNAL_CLOCK_BUFFER_ENABLE:** [DevVLVP] 0 = Disable DPLLB clock from being driven out 1 = Enable DPLLB clock to be drive out [DevCDV] Reserved DPLLB Serial DVO High Speed IO clock Enable 0 = High Speed IO Clock Disabled (default) 1 = High Speed IO Clock Enabled (must be set in Serial DVO and HDMI modes)
29	0b RW	**REFB_CLOCK_ENABLE:** [DevCDV, DevVLVP]: Indicate the reference clock of PLL A is enable 0 Disable (default) 1 Enable
28	0b RW	**VGA_MODE_DISABLE:** When in native VGA modes, writes to the VGA MSR register causes the value in the selected (by MSR bits) VGA clock control register to be loaded into the active register. This allows the VGA clock select to select the pixel frequency between the two standard VGA pixel frequencies. 0 = VGA MSR(3:2) Clock Control bits select DPLL A Frequency 1 = Disable VGA Control



Bit Range	Default & Access	Description
27:26	0b RW	**ENABLE_SINGLE_DPLLB_FREQUENCY_FOR_BOTH_PIPES:** [DevVLVP] When two pipes are enabled for eDP and both pipes can run with the same DP frequency either 162MHz or 270MHz. Setting this mode can allow using only DPLLB to feed both pipes. DPLLA should be shutdown to save power. 00 = Disabled 01 = Enabled 10 = Reserved 11 = Reserved [DevCDV] Reserved DPLLB Mode Select : Configure the DPLLB for various supported Display Modes 00 = Reserved 01 = DPLLA in DAC/Serial DVO/UDI/Integrated TV mode 10 = DPLLA in LVDS mode (Mobile devices ONLY) otherwise RESERVED 11 = DP
25:24	0b RW	**RESERVED:** [DevCDV, DevVLVP] FPB0/FPB1 P2 Clock Divide: 00 = Divide by 10. This is used when Dot Clock =(270MHz in sDVO, HDMI, or DAC modes 01 = Divide by 5. This is used when Dot Clock)270MHz 10 = Reserved 11 = Reserved For DPLLB in LVDS mode, BITS(27:26)=10 00 = Divide by 14. This is used in Single-Channel LVDS 01 = Divide by 7. This is used in Dual-Channel LVDS 10 = Reserved 11 = Reserved
23:16	0b RW	**RESERVED_1:** [DevCDV, DevVLVP] FPB0/ FPB1 P1 Post Divisor: Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b = Divide by one 00000010b = Divide by two 00000100b = Divide by three 00001000b = Divide by four 00010000b = Divide by five 00100000b = Divide by six 01000000b = Divide by seven 10000000b = Divide by Eight All other values are illegal and should not be used
15	0b RW	**RESERVED_2:** Write as zero PLLB Lock [DevCDV, DevVLVP] (RO) 1 - PLLB Lock 0 PLLB unlock
14	1b RW	**DPIO_COMMON_REGISTER_INTERFACE_CLOCK_SELECT_CRICLKSEL :** [DevVLVP] This bit is to control the clock source for DPIO Common Register Interface 0 = Use external reclk pad 1 = Use integrated core refclk (default)
13	1b RW	**DPLL_B_REFERENCE_INPUT_SELECT:** [DevVLVP] This control selects the integrated core refclk or external OSC refclk as the input clock source to DPLL B. 0 = External refclk pad (27MHz) 1 = Integrated core refclk (default is 100 MHz) [DevCDV] Reserved PLL Reference Input Select: The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog display port or LCD panels for both the sDVO connected transmitter or the integrated LVDS. TV Clock in should be selected when driving an sDVO connected TV encoder.
12:9	0b RW	**RESERVED_3:** [DevCDV, DevVLVP] Parallel to Serial Load Pulse phase selection: Programmable select bits to choose the relative phase of the high speed (10X) DPLL clock used for generating the parallel to serial load pulse for digital display port on PCIe. The relative phase is the number of flop delays (phase 0 represents 1 flop delay) of the 1X parallel data synchronization signal in the 10X clock domain. The earliest selectable clock phase is 4. A phase selection of 10 or greater simply extends the flop delay count to sample delayed data. 0100 = use clock phase-4 0101 = use clock phase-5 0110 = use clock phase-6 (Default value) 0111 = use clock phase-7 1000 = use clock phase-8 1001 = use clock phase-9 1010 = use clock phase-10 1011 = use clock phase-11 1100 = use clock phase-12 1101 = use clock phase-13 Phases 0 through 3 are not available for Load Pulse selection. [DevCL] The following programming is recommended for Crestline based on PV timing analysis: 1101 use clock phase-13 [DevBLC, DevCTG] Reserved. Programming for load pulse is in PXP AFE config space.

Bit Range	Default & Access	Description
8	0b RW	**DISPLAY_RATE_SWITCH_PIPEB:** [DevCTG, DevCDV, DevVLVP] Switching this bit (transition 0 to 1 or 1 to 0) causes the DSP HW to disable and than enable the DPLL during vblank (2 row) in order to switch the frequency at the DPLL (new dividers stored at the DPIO which is double buffered) (This bit is only available when bits 17:16 of the PIPEACONF register are 00) [DevBW, DevCL, DevBLC] Reserved
7:0	0b RW	**RESERVED_4:** [DevBW, DevCL, DevBLC, DevCDV, DevVLVP] [DevCTG] FPB1 P1 Post Divisor: Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b - Divide by one 00000010b - Divide by two 00000100b - Divide by three 00001000b - Divide by four 00010000b - Divide by five 00100000b - Divide by six 01000000b - Divide by seven 10000000b - Divide by Eight All other values are illegal and should not be used

3.1.31 DPLLAMD—Offset 601Ch

DPLL A SDVO/HDMI Multiplier/Divisor Register Pipe A multiply (cpdmmreg.v reg15_lt)

Access Method

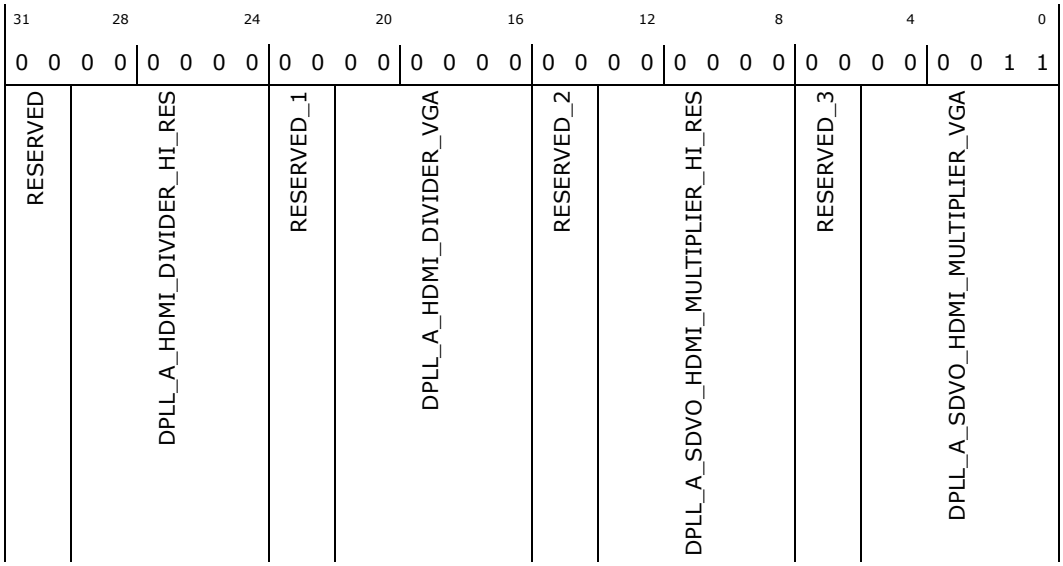
Type: Memory Mapped I/O Register (Size: 32 bits)

DPLLAMD: [GTTMMADR_LSB + 2BF20h] + 601Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** Reserved.
29:24	0b RW	**DPLL_A_HDMI_DIVIDER_HI_RES:** When the source is high resolution, this field determines the number of pixels to be included in the multiplied packet defined by the SDVO/HDMI multiplier. For SDVO and CRT, the only valid setting is 1x. HDMI example: If the pixel clock on the display should be 180MHz and the display PLL is set to 270MHz, two pixels and one fill code must be sent over HDMI (fixed frequency mode only). Therefore, the HDMI divider should be set to 2 and the SDVO/HDMI multiplier should be set to 3, since 180 MHz (pixel clock) = 2/3*270MHz (link character clock) This divider must be set to 1x for any mode except HDMI fixed frequency mode. Value in this register = number of pixels per packet 1 Default: 0000 1 pixel per packet (Default value, must be set to 1x for any mode except HDMI fixed frequency mode) Range: 0-63 (1 pixel per packet 64 pixels per packet)
23:22	0b RW	**RESERVED_1:** Reserved.
21:16	0b RW	**DPLL_A_HDMI_DIVIDER_VGA:** When the source is VGA, these bits specify the HDMI divider. The format of this field is the same as that of the hi-res divider.
15:14	0b RW	**RESERVED_2:** Reserved.
13:8	0b RW	**DPLL_A_SDVO_HDMI_MULTIPLIER_HI_RES:** This field determines the data multiplier for sDVO and is also applied to CRT. In order to keep the clock rate to a more narrow range of rates, the multiplier is set and the Display PLL programmed to a multiple of the display mode s actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000000 (1X) Range: 0 63 (1X 64X)
7:6	0b RW	**RESERVED_3:** Reserved.
5:0	000011b RW	**DPLL_A_SDVO_HDMI_MULTIPLIER_VGA:** When the source is VGA, these bits specify the HDMI multiplier. The format of this field is the same as that of the hi-res multiplier. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000011 (4X) Range: 0 63 (1X 64X)

3.1.32 DPLLBMD—Offset 6020h

DPLL B SDVO/HDMI Multiplier/Divisor Register Pipe B multiplier (cpdmmreg.v reg16_lt)

Access Method

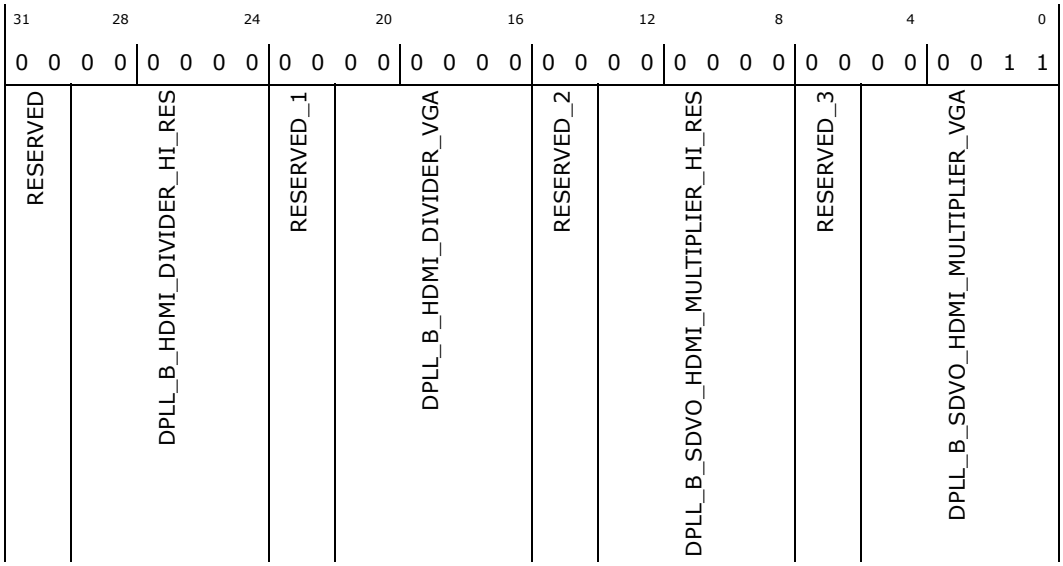
Type: Memory Mapped I/O Register (Size: 32 bits)

DPLLBMD: [GTTMMADR_LSB + 2BF20h] + 6020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** Reserved.
29:24	0b RW	**DPLL_B_HDMI_DIVIDER_HI_RES:** When the source is high resolution, this field determines the number of pixels to be included in the multiplied packet defined by the SDVO/HDMI multiplier. For SDVO and CRT, the only valid setting is 1x. HDMI example: If the pixel clock on the display should be 180MHz and the display PLL is set to 270MHz, two pixels and one fill code must be sent over HDMI (fixed frequency mode only). Therefore, the HDMI divider should be set to 2 and the SDVO/HDMI multiplier should be set to 3, since 180 MHz (pixel clock) = 2/3*270MHz (link character clock) This divider must be set to 1x for any mode except HDMI fixed frequency mode. Value in this register = number of pixels per packet 1 Default: 0000 1 pixel per packet (Default value, must be set to 1x for any mode except HDMI fixed frequency mode) Range: 0-63 (1 pixel per packet 64 pixels per packet)
23:22	0b RW	**RESERVED_1:** Reserved.
21:16	0b RW	**DPLL_B_HDMI_DIVIDER_VGA:** When the source is VGA, these bits specify the HDMI divider. The format of this field is the same as that of the hi-res divider.
15:14	0b RW	**RESERVED_2:** Reserved.
13:8	0b RW	**DPLL_B_SDVO_HDMI_MULTIPLIER_HI_RES:** This field determines the data multiplier for sDVO and is also applied to CRT. In order to keep the clock rate to a more narrow range of rates, the multiplier is set and the Display PLL programmed to a multiple of the display mode s actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000011 (4X) Range: 0 63 (1X 64X)
7:6	0b RW	**RESERVED_3:** Reserved.

Bit Range	Default & Access	Description
5:0	000011b RW	**DPLL_B_SDVO_HDMI_MULTIPLIER_VGA:** When the source is VGA, these bits specify the HDMI multiplier. The format of this field is the same as that of the hi-res multiplier. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000000 (1X) Range: 0 63 (1X 64X)

3.1.33 RAWCLK_FREQ—Offset 6024h

Rawclk Frequency

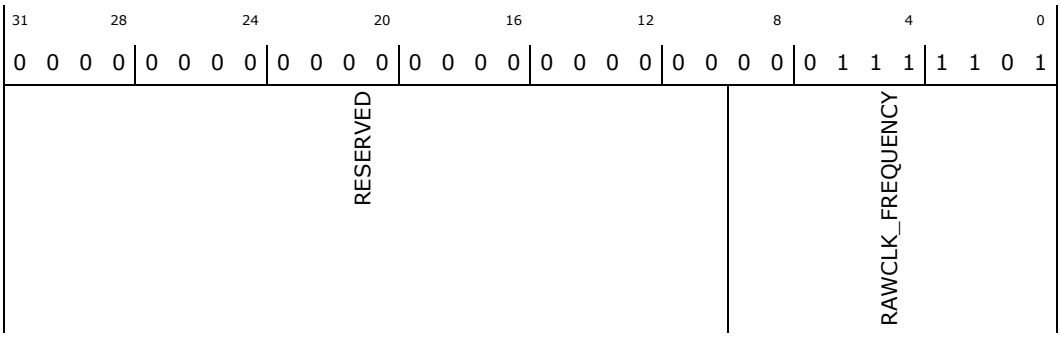
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RAWCLK_FREQ: [GTTMMADR_LSB + 2BF20h] + 6024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 0000007Dh



Bit Range	Default & Access	Description
31:10	0b RW	**RESERVED:** Project: All Format:
9:0	0001111101b RW	**RAWCLK_FREQUENCY:** Project: All Format: Program this field with rawclk frequency. This is used to generate a divided down clock for miscellaneous timers in display.

3.1.34 D_STATE—Offset 6104h

D State Function Control Register Power state behavior (cpdmmreg.v reg11_lt)

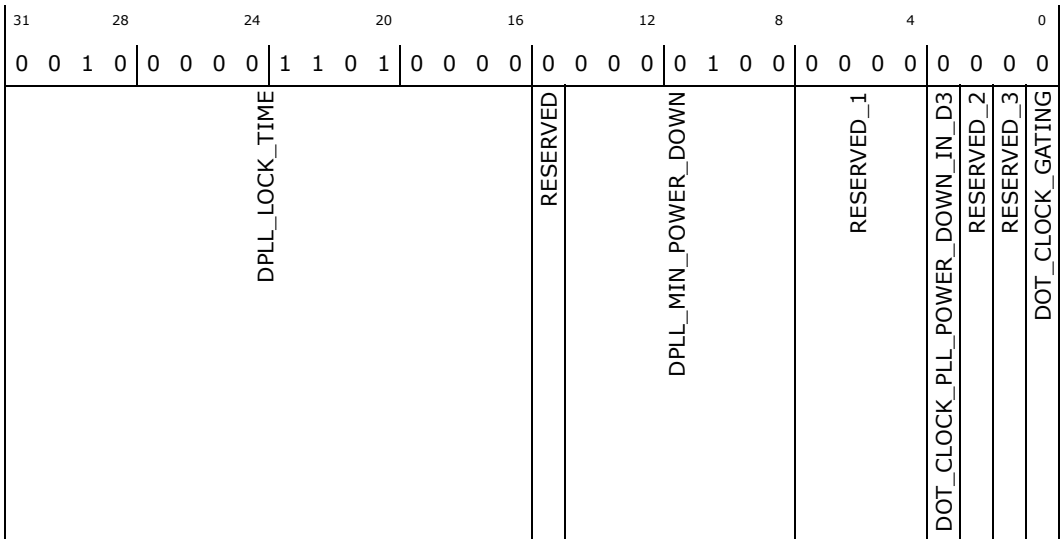
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

D_STATE: [GTTMMADR_LSB + 2BF20h] + 6104h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 20D00400h



Bit Range	Default & Access	Description
31:16	00100000110100000b RW	**DPLL_LOCK_TIME:** (DevCDV): This is the time required to the DPLL to relock. The counter using the HRAW clk (5nsec) and resolution of 5nsec. (SEG DPLL lock time is 42usec)
15	0b RW	**RESERVED:** : MBZ
14:8	0000100b RW	**DPLL_MIN_POWER_DOWN:** (DevCDV): This is the minimum time required the DPLL to be power down until it is allowed to turn it on again. The HW counter using HRAW clk (5nsec) and has resolution of 160nsec (SEG DPLL required time is 0.5usec)
7:4	0b RW	**RESERVED_1:** : MBZ
3	0b RW	**DOT_CLOCK_PLL_POWER_DOWN_IN_D3:** This bit determines whether the PCI Power State Powers down the Dot Clock PLLs when in D3. A 0 on this bit does not power down the DPLLs, requiring software to gate them if necessary. When this bit is a 1, the dot PLLs are powered down when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register.
2	0b RW	**RESERVED_2:** Reserved.
1	0b RW	**RESERVED_3:** [DevCDV] Graphics Core Clock Gating: This bit determines whether the PCI Power State gates the Graphics Core clocks when in the D3 state. A 0 on this bit does not gate the clocks, requiring software to gate them if necessary. When this bit is a 1, the graphics core clocks are gated at the outputs of the PLLs when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register. This register field has no use in current products.

Bit Range	Default & Access	Description
0	0b RW	**DOT_CLOCK_GATING:** This bit determines whether the PCI Power State gates the Dot clocks when in the D3 state. A 0 on this bit does not gate the clocks, requiring software to gate them if necessary. When this bit is a 1, the dot clocks are gated at the outputs of the PLLs when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register.

3.1.35 DSPCLK_GATE_D—Offset 6200h

Clock Gating Disable for Display Register clock gating (cpdmmreg.v reg12_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPCLK_GATE_D: [GTTMMADR_LSB + 2BF20h] + 6200h

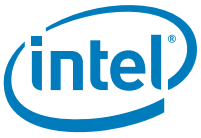
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 10000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HDCPUNIT_CLOCK_GATING_DISABLE	DPUNIT_PIPEB_CLOCK_GATING_DISABLE	VSUNIT_PIPE_A_CLOCK_GATING_DISABLE	VRHUNIT_CLOCK_GATING_DISABLE	VRDUNIT_CLOCK_GATING_DISABLE	AUDUNIT_CLOCK_GATING_DISABLE	DPUNIT_PIPEA_CLOCK_GATING_DISABLE	DPCUNIT_CLOCK_GATING_DISABLE	VSUNIT_PIPE_B_CLOCK_GATING_DISABLE	SPRITE_D_CLOCK_GATING_DISABLE	SPRITE_C_CLOCK_GATING_DISABLE	SPRITE_B_CLOCK_GATING_DISABLE	DVSUNIT_SPRITE_A_CLOCK_GATING_DISABLE	DDBUNIT_CLOCK_GATING_DISABLE	GMBUSUNIT_CLOCK_GATING_DISABLE	DPRUNIT_CLOCK_GATING_DISABLE	DPFUNIT_CLOCK_GATING_DISABLE	DPLRUNIT_PIPE_A_CLOCK_GATING_DISABLE	DPLSUNIT_PIPE_A_CLOCK_GATING_DISABLE	DPTUNIT_CLOCK_GATING_DISABLE	DPOUNIT_CLOCK_GATING_DISABLE	DPBUNIT_PIPE_A_CLOCK_GATING_DISABLE	DCUNIT_PIPE_A_CLOCK_GATING_DISABLE	DPGCUNIT_PIPE_B_CLOCK_GATING_DISABLE	DPGCUNIT_PIPE_A_CLOCK_GATING_DISABLE	DPIOUNIT_CLOCK_GATING_DISABLE	OVFUNIT_CLOCK_GATING_DISABLE	OVBUNIT_CLOCK_GATING_DISABLE	DPLRUNIT_PIPE_B_CLOCK_GATING_DISABLE	DPLSUNIT_PIPE_B_CLOCK_GATING_DISABLE	DPBUNIT_PIPE_B_CLOCK_GATING_DISABLE	DCUNIT_PIPE_B_CLOCK_GATING_DISABLE

Bit Range	Default & Access	Description
31	0b RW	**HDCPUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
30	0b RW	**DPUNIT_PIPEB_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function



Bit Range	Default & Access	Description
29	0b RW	**VSUNIT_PIPE_A_CLOCK_GATING_DISABLE:** [DevVLVP] (this bit used to be in PCI space in Calistoga) 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
28	1b RW	**VRHUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logicg 1 = Disable clock gating function Clock gating should not be enabled for this unit (this bit should always be set to 1.) [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
27	0b RW	**VRDUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
26	0b RW	**AUDUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
25	0b RW	**DPUNIT_PIPEA_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
24	0b RW	**DPCUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
23	0b RW	**VSUNIT_PIPE_B_CLOCK_GATING_DISABLE:** [DevVLVP] 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW]. [DevCDV] and [DevVLVP]: Reserved
22	0b RW	**SPRITE_D_CLOCK_GATING_DISABLE:** [DevVLVP] 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW]. [DevCDV]: Reserved
21	0b RW	**SPRITE_C_CLOCK_GATING_DISABLE:** [DevVLVP] 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW]. [DevCDV]: Reserved
20	0b RW	**SPRITE_B_CLOCK_GATING_DISABLE:** [DevVLVP] 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC]. [DevCDV]: Reserved
19	0b RW	**DVSUNIT_SPRITE_A_CLOCK_GATING_DISABLE:** [DevBW] and [DevCL] 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBLC] and [DevCTG]: Reserved. MBZ. This bit is not connected on [DevBLC] and [DevCTG].
18	0b RW	**DDBUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevCTG] Always program this bit to 1
17	0b RW	**GMBUSUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
16	0b RW	**DPRUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
15	0b RW	**DPFUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
14	0b RW	**DPLRUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC].

Bit Range	Default & Access	Description
13	0b RW	**DPLSUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC].
12	0b RW	**DPTUNIT_CLOCK_GATING_DISABLE:** [DevVLVP] [DevCDV] Dplunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC].
11	0b RW	**DPOUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
10	0b RW	**DPBUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
9	0b RW	**DCUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
8	0b RW	**DPGCUNIT_PIPE_B_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
7	0b RW	**DPGCUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
6	0b RW	**DPIOUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
5	0b RW	**OVFUNIT_CLOCK_GATING_DISABLE:** [DevBW, DevCL, DevCDV] [DevCTG] DPFCunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
4	0b RW	**OVBUNIT_CLOCK_GATING_DISABLE:** [DevBW, DevCL, DevCDV] [DevCTG] DPFDunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
3	0b RW	**DPLRUNIT_PIPE_B_CLOCK_GATING_DISABLE:** (not in CDV)
2	0b RW	**DPLSUNIT_PIPE_B_CLOCK_GATING_DISABLE:** (not in CDV)
1	0b RW	**DPBUNIT_PIPE_B_CLOCK_GATING_DISABLE:** [DevVLVP] [DevBW, DevCL, DevCDV] Ovuunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBLC] and [DevCTG]: Reserved. MBZ. This bit is not connected on [DevBLC] and [DevCTG].
0	0b RW	**DCUNIT_PIPE_B_CLOCK_GATING_DISABLE:** [DevVLVP] [DevBW, DevCL, DevCDV] Ovlunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBLC] and [DevCTG]: Reserved. MBZ. This bit is not connected on [DevBLC] and [DevCTG].

3.1.36 DPPSR_CGDIS—Offset 6204h

Panel Self Refresh Clock Gating Disable for Display PSR clock gating disable controls (cpdmmreg.v)

Access Method

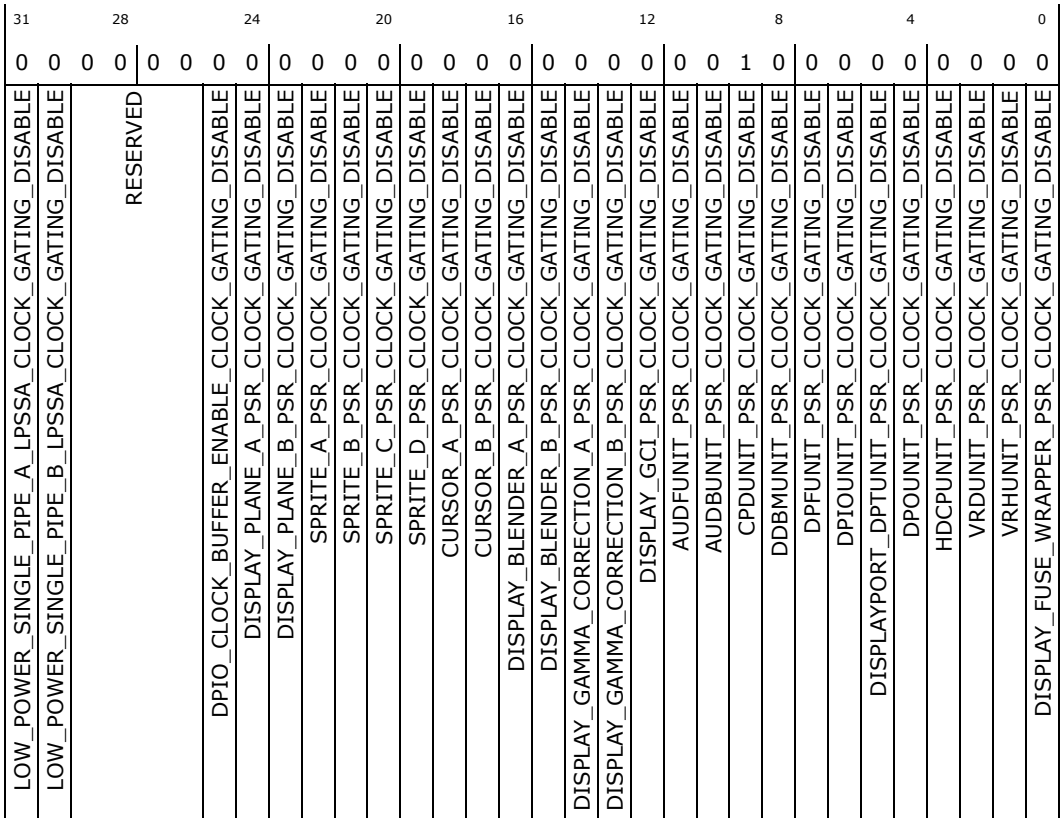
Type: Memory Mapped I/O Register (Size: 32 bits)

DPPSR_CGDIS: [GTTMMADR_LSB + 2BF20h] + 6204h

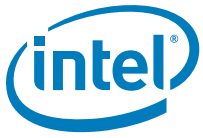
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000200h



Bit Range	Default & Access	Description
31	0b RW	**LOW_POWER_SINGLE_PIPE_A_LPSSA_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. Pipe A shall be enabled 1 = Disable trunk clock gating on pipe A even when LPSSA is on
30	0b RW	**LOW_POWER_SINGLE_PIPE_B_LPSSA_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. Pipe B shall be enabled 1 = Disable trunk clock gating on pipe B even when LPSSA is on
29:26	0b RW	**RESERVED:** Reserved.
25	0b RW	**DPIO_CLOCK_BUFFER_ENABLE_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by DPIO clock buffer enable 1=Disable clock gating function by DPIO clock buffer enable
24	0b RW	**DISPLAY_PLANE_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function



Bit Range	Default & Access	Description
23	0b RW	**DISPLAY_PLANE_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
22	0b RW	**SPRITE_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
21	0b RW	**SPRITE_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
20	0b RW	**SPRITE_C_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
19	0b RW	**SPRITE_D_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
18	0b RW	**CURSOR_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
17	0b RW	**CURSOR_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
16	0b RW	**DISPLAY_BLENDER_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
15	0b RW	**DISPLAY_BLENDER_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
14	0b RW	**DISPLAY_GAMMA_CORRECTION_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
13	0b RW	**DISPLAY_GAMMA_CORRECTION_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
12	0b RW	**DISPLAY_GCI_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
11	0b RW	**AUDFUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function(default)
10	0b RW	**AUDBUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
9	1b RW	**CPDUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function (default)
8	0b RW	**DDBMUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
7	0b RW	**DPFUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
6	0b RW	**DPIOUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
5	0b RW	**DISPLAYPORT_DPTUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
4	0b RW	**DPOUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
3	0b RW	**HDCPUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function

Bit Range	Default & Access	Description
2	0b RW	**VRDUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
1	0b RW	**VRHUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
0	0b RW	**DISPLAY_FUSE_WRAPPER_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function

3.1.37 RAMCLK_GATE_D—Offset 6210h

GFX RAM Clock Gating Disable Register ([DevBLC, DevCTG, DevCDV, DevCL]) memory clock gating (cpdmmreg.v gfxramcg2)

Access Method

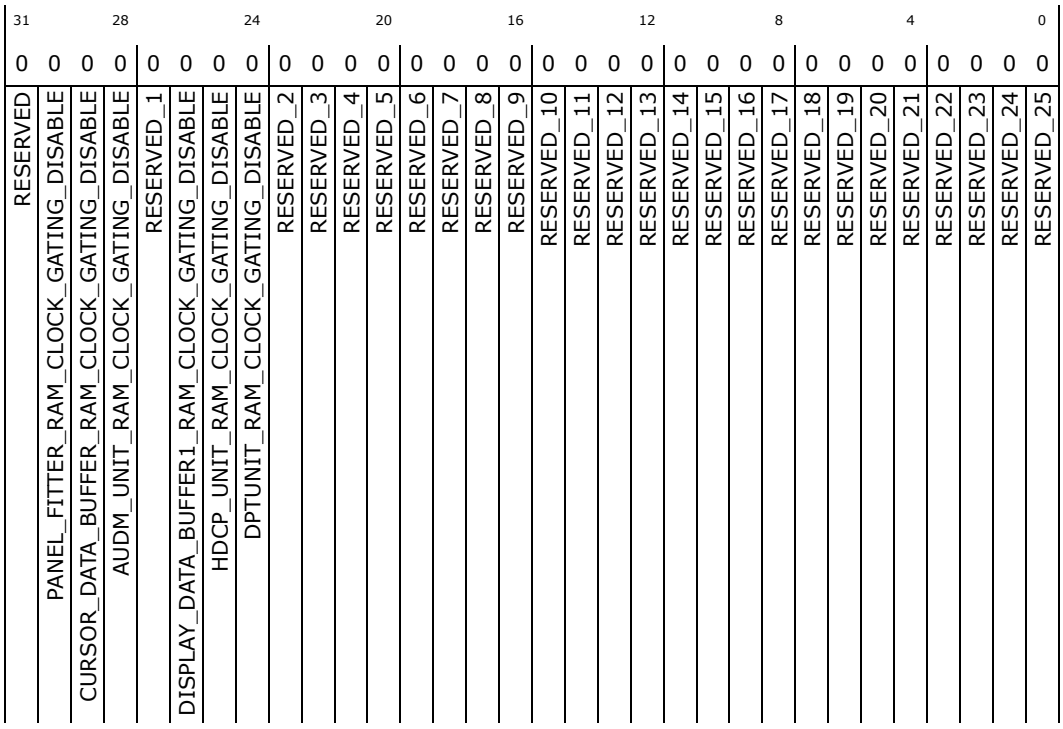
Type: Memory Mapped I/O Register (Size: 32 bits)

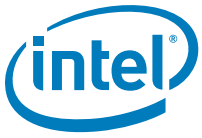
RAMCLK_GATE_D: [GTTMMADR_LSB + 2BF20h] + 6210h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

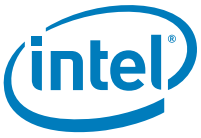
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** [DevCDV] TVOUT RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
30	0b RW	**PANEL_FITTER_RAM_CLOCK_GATING_DISABLE:** 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
29	0b RW	**CURSOR_DATA_BUFFER_RAM_CLOCK_GATING_DISABLE:** 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
28	0b RW	**AUDM_UNIT_RAM_CLOCK_GATING_DISABLE:** [DevCTG, DevCDV] [DeBLC] Reserved. [DevCL] WIZ Z coeff readback return FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
27	0b RW	**RESERVED_1:** [DevCDV] [DevCTG] DPFC Unit RAM Clock Gating Disable: [DevBLC] Reserved. [DevCL] Display Data Buffer2 (Overlay) Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
26	0b RW	**DISPLAY_DATA_BUFFER1_RAM_CLOCK_GATING_DISABLE:** 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
25	0b RW	**HDCP_UNIT_RAM_CLOCK_GATING_DISABLE:** [DevBLC, DevCTG, DevCDV] [DevCL] ME RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
24	0b RW	**DPTUNIT_RAM_CLOCK_GATING_DISABLE:** [DevVLVP] [DevCTG, DevCDV] DPIOM Unit RAM Clock Gating Disable: [DevBLC] Reserved. [DevCL] WIZ polygon FIFO RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
23	0b RW	**RESERVED_2:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] VF RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
22	0b RW	**RESERVED_3:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] SF RAMClock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
21	0b RW	**RESERVED_4:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] WMIZ Latency FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
20	0b RW	**RESERVED_5:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] TC FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
19	0b RW	**RESERVED_6:** [DevBLC, DevCTG, DevCDV] [DevCL] SV FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
18	0b RW	**RESERVED_7:** [DevCDV] [DevBLC] and [DevCTG] BD Unit RAM Clock Gating Disable: [DevCL] Latency FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
17	0b RW	**RESERVED_8:** [DevCDV] [DevBLC] and [DevCTG] BF Unit RAM Clock Gating Disable: [DevCL] URB Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function



Bit Range	Default & Access	Description
16	0b RW	**RESERVED_9:** [DevCDV] [DevBLC] and [DevCTG] CS Unit RAM Clock Gating Disable: [DevCL] L2 Instruction Tag RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
15	0b RW	**RESERVED_10:** [DevBLC, DevCDV] [DevCTG] FH Unit RAM Clock Gating Disable: [DevCL] Data RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
14	0b RW	**RESERVED_11:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] TAG RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
13	0b RW	**RESERVED_12:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] L2 Instruction Cache Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
12	0b RW	**RESERVED_13:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] MRFRAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
11	0b RW	**RESERVED_14:** [DevCDV] [DevBLC] and [DevCTG] VFM Unit RAM Clock Gating Disable: [DevCL] GRF RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
10	0b RW	**RESERVED_15:** [DevCDV] [DevBLC] and [DevCTG] SFM Unit RAM Clock Gating Disable: [DevCL] Data Cache CAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
9	0b RW	**RESERVED_16:** [DevCDV] [DevBLC] and [DevCTG] WIZM Unit RAM Clock Gating Disable: [DevCL] Data Cache Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
8	0b RW	**RESERVED_17:** [DevCDV] [DevBLC] and [DevCTG] URB Unit RAM Clock Gating Disable: [DevCL] Render Cache Latency FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
7	0b RW	**RESERVED_18:** [DevCDV] [DevBLC] and [DevCTG] IC Unit RAM Clock Gating Disable: [DevCL] Render PA Tag RAM (Z) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
6	0b RW	**RESERVED_19:** [DevCDV] [DevBLC] and [DevCTG] ISC Unit RAM Clock Gating Disable: [DevCL] Render PA Tag RAM (Color) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
5	0b RW	**RESERVED_20:** [DevCDV] [DevBLC] and [DevCTG] GA Unit RAM Clock Gating Disable: [DevCL] Render Cache Write Back FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
4	0b RW	**RESERVED_21:** [DevCDV] [DevBLC] and [DevCTG] MS Unit RAM Clock Gating Disable: [DevCL] Render Cache (Z) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function

Bit Range	Default & Access	Description
3	0b RW	**RESERVED_22:** [DevCDV] [DevBLC] and [DevCTG] RCBP Unit RAM Clock Gating Disable: [DevCL] Render Cache (color) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
2	0b RW	**RESERVED_23:** [DevCDV] [DevBLC] and [DevCTG] RCC Unit RAM Clock Gating Disable: [DevCL] L2 Mapping Cache CAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
1	0b RW	**RESERVED_24:** [DevCDV] [DevBLC] and [DevCTG] RCZ Unit RAM Clock Gating Disable: [DevCL] L2 Mapping Tag RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
0	0b RW	**RESERVED_25:** [DevCDV] [DevBLC] and [DevCTG] MT Unit RAM Clock Gating Disable: [DevCL] L2 Mapping Cache Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function

3.1.38 FW_BLC_SELF—Offset 6500h

Display FIFO Watermark

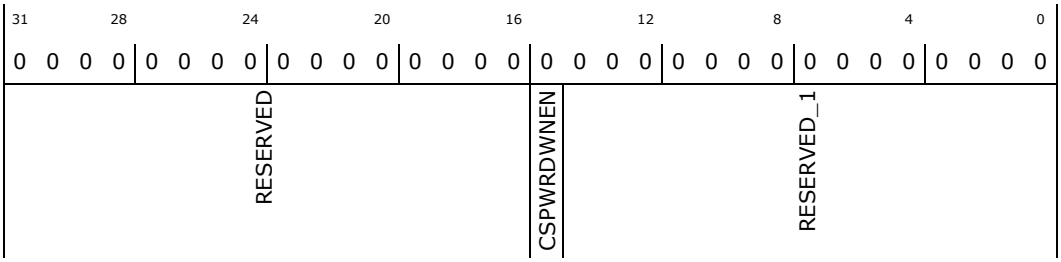
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FW_BLC_SELF: [GTTMMADR_LSB + 2BF20h] + 6500h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15	0b RW	**CSPWRDWNEN:** 1 = Display FIFO can go into max_fifo configuration if only one plane A/B is enabled and all other planes, including overlay, are off. 0 = Do not put display FIFO in max_fifo configuration
14:0	0b RW	**RESERVED_1:** Reserved.

3.1.39 MI_ARB—Offset 6504h

Display Arbiter

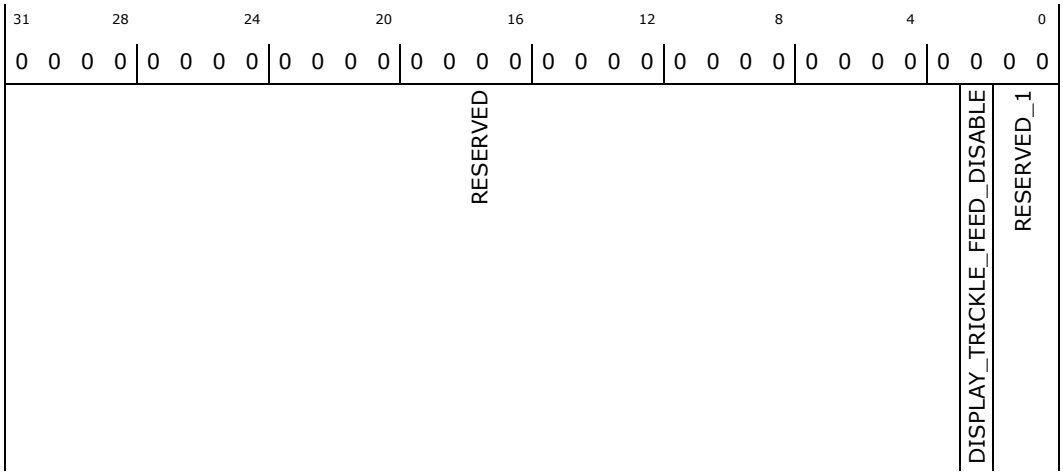
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MI_ARB: [GTTMMADR_LSB + 2BF20h] + 6504h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**RESERVED:** Reserved.
2	0b RW	**DISPLAY_TRICKLE_FEED_DISABLE:** 1 Disable (Turn off trickle feed Display request). 0 Enable (Default)
1:0	0b RW	**RESERVED_1:** Reserved.

3.1.40 CZCLK_CDCLK_FREQ_RATIO—Offset 6508h

Display CZCLK/CDCLK FREQ Ratio for RMBUS sync

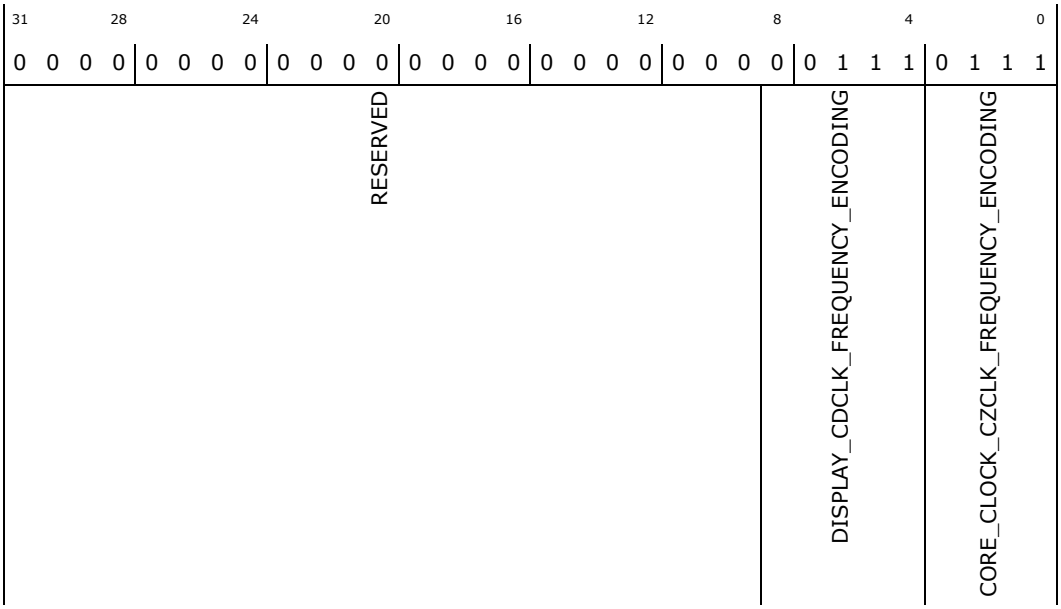
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CZCLK_CDCLK_FREQ_RATIO: [GTTMMADR_LSB + 2BF20h] + 6508h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000077h



Bit Range	Default & Access	Description
31:9	0b RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
8:4	00111b RO	**DISPLAY_CDCLK_FREQUENCY_ENCODING:** DISPLAY CDCLK FREQUENCY ENCODING (* symbol frequencies are POR) |_____| |=====CDCLK FREQ.======|===CDCLK DEVIDE RATIO===|==CD REGISTER ENCODING==|===SKU200==|===SKU266====|====SKU333===|===CD======| |=====ENCODING=========|=======(DECIMAL)========|===VCO 800=|===VCO 1600==|====VCO 2000=|===QUAL GEN=| |======5'b00001========|==========1==========|=========1==========|=====800===|====1600=====|===2000=====|======1=====| |======5'b00010========|=========1.5==========|=========2==========|=====533===|====1067=====|===1333=====|======2=====| |======5'b00011========|==========2==========|=========3==========|=====400===|=====800=====|===1000=====|======3=====| |======5'b00100========|=========2.5==========|=========4==========|=====320*==|=====640=====|====800=====|======4=====| |======5'b00101========|==========3==========|=========5==========|=====267*==|=====533=====|====667=====|======5=====| |======5'b00111========|==========4==========|=========6==========|=====200*==|=====400=====|====500=====|======7=====| |======5'b01000========|=========4.5==========|=========7==========|=====178===|=====356=====|====444=====|======8=====| |======5'b01001========|==========5==========|=========9==========|=====160===|=====320*====|====400=====|======9=====| |_____|

Bit Range	Default & Access	Description
3:0	0111b RO	**CORE_CLOCK_CZCLK_FREQUENCY_ENCODING:** CORE CLOCK (CZCLK) FREQUENCY ENCODING (* symbol are POR freq for each SKU) |_____ _____ _____| |=====CZCLK FREQ.======|===CZCLK DEVIDE RATIO===|==CZ REGISTER ENCODING==|===SKU200==|===SKU266====|====SKU333===|====CZ======| |=====ENCODING=========|=========================|=======(DECIMAL)========|===VCO 800=|===VCO 1600==|====VCO 2000=|===QUAL GEN=| |======================|=========================|=========================|====(MHz)==|===(MHz)=====|=====(MHz)===|====RATIO===| |_____ _____ _____| |======5'b00001========|==========1==========|==========1==========|=====800===|====1600=====|===2000=====|======1=====| |_____ _____ _____| |======5'b00010========|=========1.5==========|==========2==========|=====533===|====1067=====|===1333=====|======2=====| |_____ _____ _____| |======5'b00011========|==========2==========|==========3==========|=====400===|=====800=====|===1000=====|======3=====| |_____ _____ _____| |======5'b00100========|=========2.5==========|==========4==========|=====320===|=====640=====|====800=====|======4=====| |_____ _____ _____| |======5'b00101========|==========3==========|==========5==========|=====267===|=====533=====|====667=====|======5=====| |_____ _____ _____| |======5'b00111========|==========4==========|==========6==========|=====200*==|=====400=====|====500=====|======7=====| |_____ _____ _____| |======5'b01000========|=========4.5==========|==========7==========|=====178===|=====356=====|====444=====|======8=====| |_____ _____ _____| |======5'b01001========|==========5==========|==========9==========|=====160===|=====320=====|====400=====|======9=====| |_____ _____ _____|

3.1.41 GCI_CONTROL—Offset 650Ch

GCI Control Register.

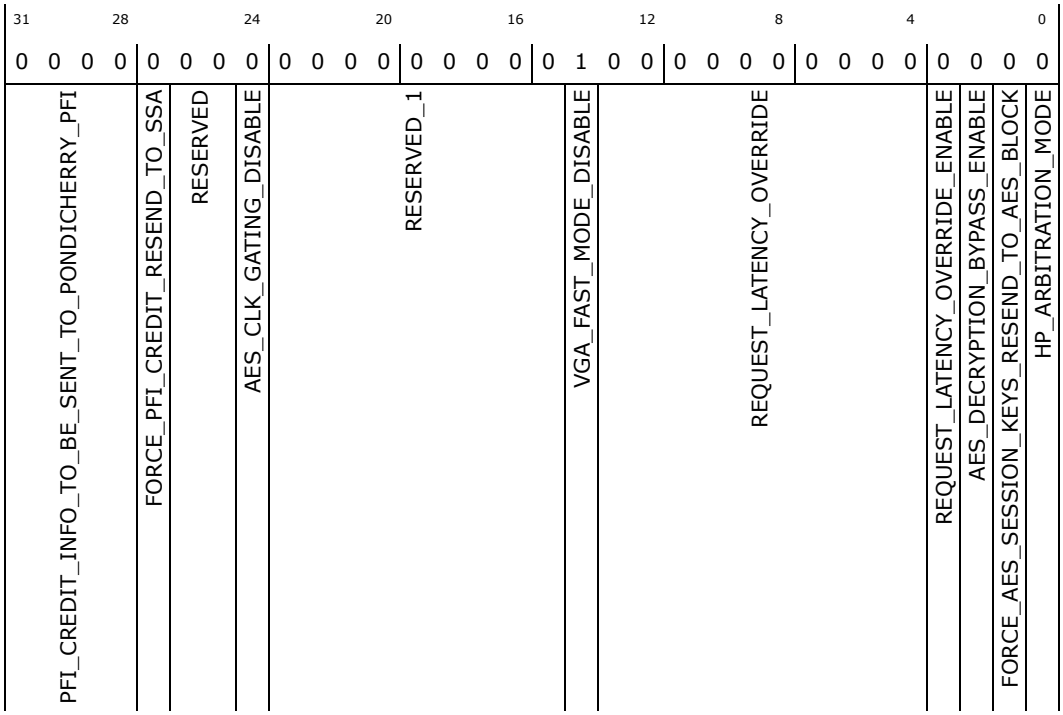
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GCI_CONTROL: [GTTMMADR_LSB + 2BF20h] + 650Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00004000h



Bit Range	Default & Access	Description
31:28	0b RW	**PFI_CREDIT_INFO_TO_BE_SENT_TO_PONDICHERRY_PFI:** Others = reserved 0111 = 15 credits 0110 = 14 credits 0101 = 13 credits 0100 = 12 credits 0011 = 11 credits 0010 = 10 credits 0001 = 9 credits 0000 = 8 credits available to PND (default) Based on the czclk/cdclk ratio, display driver has to determine the appropriate PFI credits to be used
27	0b RW	**FORCE PFI CREDIT RESEND TO SSA (FORCE_PFI_CREDIT_RESEND_TO_SSA):** 0 = Disable PFI credit to resend to SSA. Hardware is responsible to clear this bit after the PFI credit initialization request is sent. 1 = Enable PFI credit to resend to SSA. When driver sets this bit, Display PFI request engine will resend the new PFI credit bit [31:28] to SSA. Hardware is responsible to clear this bit after the PFI credit initialization request is sent.
26:25	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
24	0b RW	**AES_CLK_GATING_DISABLE:** 0 = Enable clock gating for AES clock (default) 1 = Disable clock gating for AES clock
23:15	0b RW	**RESERVED_1:** Reserved.
14	1b RW	**VGA_FAST_MODE_DISABLE:** 0 = Fast Mode enabled. The Gfx mem arbiter can accept a vga display read request every clock. Note that the HP Address (G_HP_CONTROL[28:24]) and ID (G_HP_CONTROL[21:16]) FIFO depths must be set to a value greater than 1 when Fast Mode is enabled. 1 = Fast Mode disabled. (default) The Gfx mem arbiter can accept a vga display read request every other clock Programming note: VGA FAST MODE is not supported in VLVP.
13:4	0b RW	**REQUEST_LATENCY_OVERRIDE:** If bit 3 of this register is set, the 10-btt Request Latency Override value programmed here is used as the latency offset from the global timer for requests that win arbitration. If bit 3 is not set, normal request latency from streamers is used. Programming note: This value should not be larger than the actual required request latency. Otherwise, it will cause underrun. The guideline is to use latency corresponds to low watermark level or even smaller. When this field is used, the actual request latency is defeatured, either zero or a small value is used but still not causing underrun.
3	0b RW	**REQUEST_LATENCY_OVERRIDE_ENABLE:** 1 = Request Latency Override values in bit[13:4] is used as the latency offset from global timer 0 = Request Latency Override values is disabled. Normal request latency from streamer is used. (default)
2	0b RW	**AES_DECRYPTION_BYPASS_ENABLE:** 0 = AES decryption engine is enabled (Default) 1 = AES decryption engine is bypassed
1	0b RW	**FORCE_AES_SESSION_KEYS_RESEND_TO_AES_BLOCK:** 0 = Disable sending AES session keys to AES when going from Panel Self Refresh (PSR) inactive to PSR active mode (Default). Hardware is responsible to clear this bit after this bit is set to resend the session keys. 1 = Enable sending AES session keys to AES engine when going from PSR inactive to PSR active mode. When driver sets this bit, PAVP engine will resend the session keys to AES engine. Hardware is responsible to clear this bit after the session keys are sent.
0	0b RW	**HP_ARBITRATION_MODE:** 0 = Select hierarchical arbiter 1 = Select backup round robin arbiter

3.1.42 GMBUSFREQ—Offset 6510h

GMBUS frequency binary encoding GMBUS Frequency Binary Encoding Register.

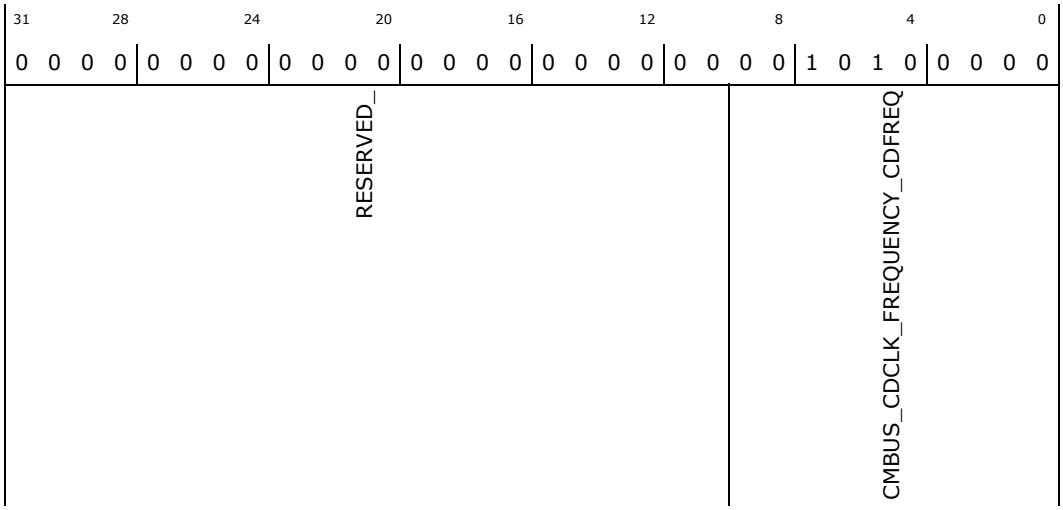
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GMBUSFREQ: [GTTMMADR_LSB + 2BF20h] + 6510h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 000000A0h



Bit Range	Default & Access	Description
31:10	0b RW	**RESERVED_:** Reserved.
9:0	0010100000b RW	**CMBUS_CDCLK_FREQUENCY_CDFREQ:** Programming note: bit[9:2] should be programmed to the number of cdclk that generates 4MHz reference clock freq which is used to generate GMBus clock. This will vary with the cdclk freq. Programming note: For hot plug detect on exact 100ms as long pulse, driver shall program [9:0] = cdclk_1.01

3.1.43 DPALETTE_A—Offset A000h

Pipe A Display Palette

Access Method

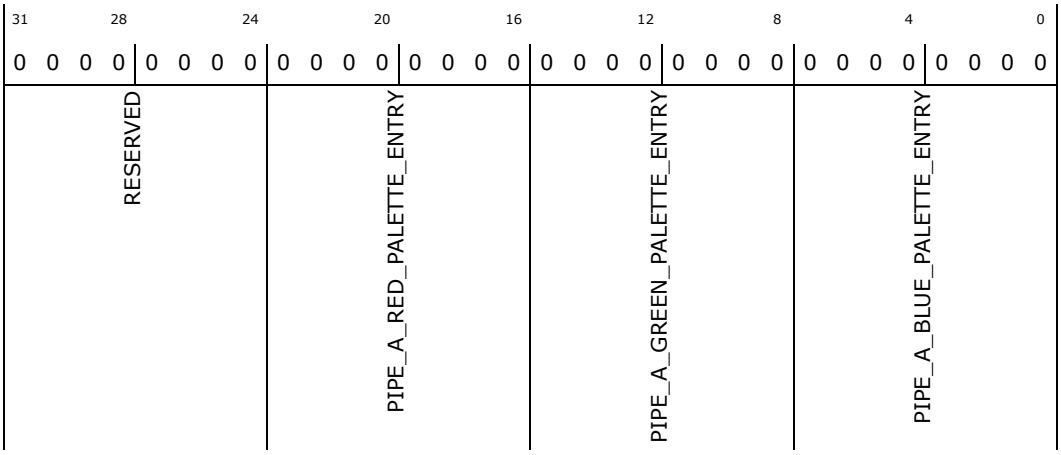
Type: Memory Mapped I/O Register (Size: 32 bits)

DPALETTE_A: [GTTMMADR_LSB + 2BF20h] + A000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** (read only).
23:16	0b RW	**PIPE_A_RED_PALETTE_ENTRY:** 8-bit entries per red color channel in the palette
15:8	0b RW	**PIPE_A_GREEN_PALETTE_ENTRY:** 8-bit entries per green color channel in the palette
7:0	0b RW	**PIPE_A_BLUE_PALETTE_ENTRY:** 8-bit entries per blue color channel in the palette

3.1.44 DPALETTE_B—Offset A800h

Pipe B Display Palette

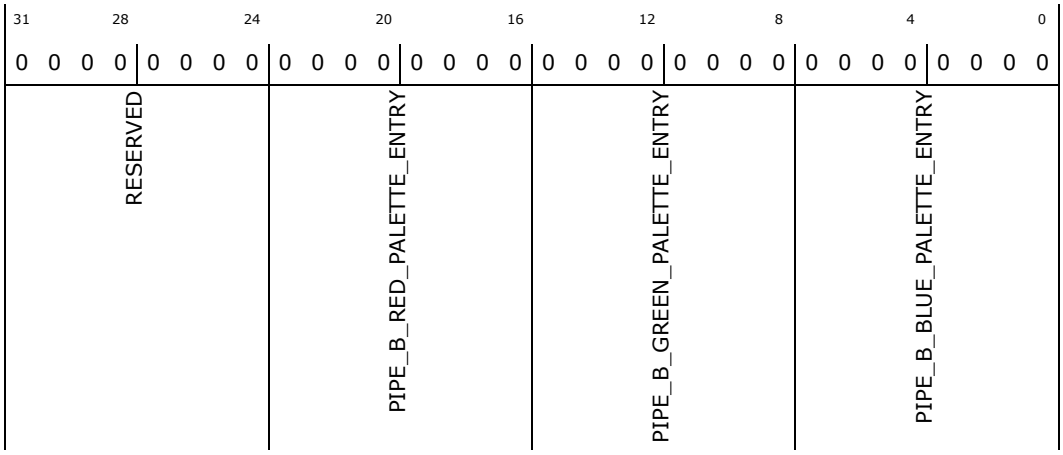
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPALETTE_B: [GTTMMADR_LSB + 2BF20h] + A800h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Read Only.
23:16	0b RW	**PIPE_B_RED_PALETTE_ENTRY:** 8-bit entries per red color channel in the palette
15:8	0b RW	**PIPE_B_GREEN_PALETTE_ENTRY:** 8-bit entries per green color channel in the palette
7:0	0b RW	**PIPE_B_BLUE_PALETTE_ENTRY:** 8-bit entries per blue color channel in the palette

3.1.45 MIPIA_DEVICE_READY_REG—Offset B000h

MIPI A Device Ready Register

Access Method

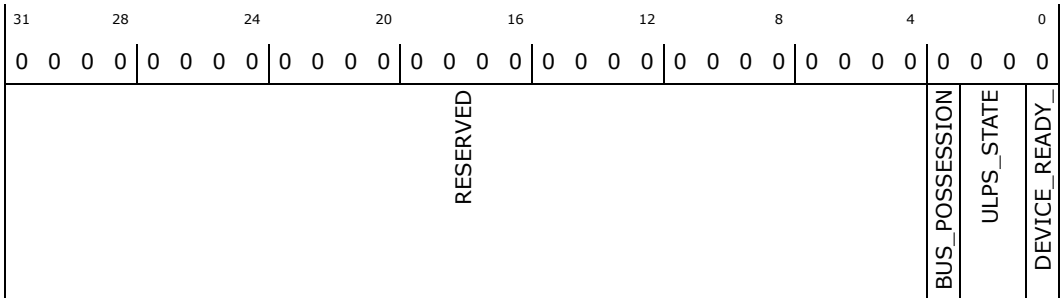
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DEVICE_READY_REG: [GTTMMADR_LSB + 2BF20h] + B000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0b RW	**RESERVED:** Reserved.
3	0b RW	**BUS_POSSESSION:** BUS possession for mipiA
2:1	0b RW	**ULPS_STATE:** ULPS state for mipi pipe A
0	0b RW	**DEVICE_READY_:** Set by the processor to inform that device is ready

3.1.46 MIPIA_INTR_STAT_REG—Offset B004h

interrupt stat reg for mipi pipe A

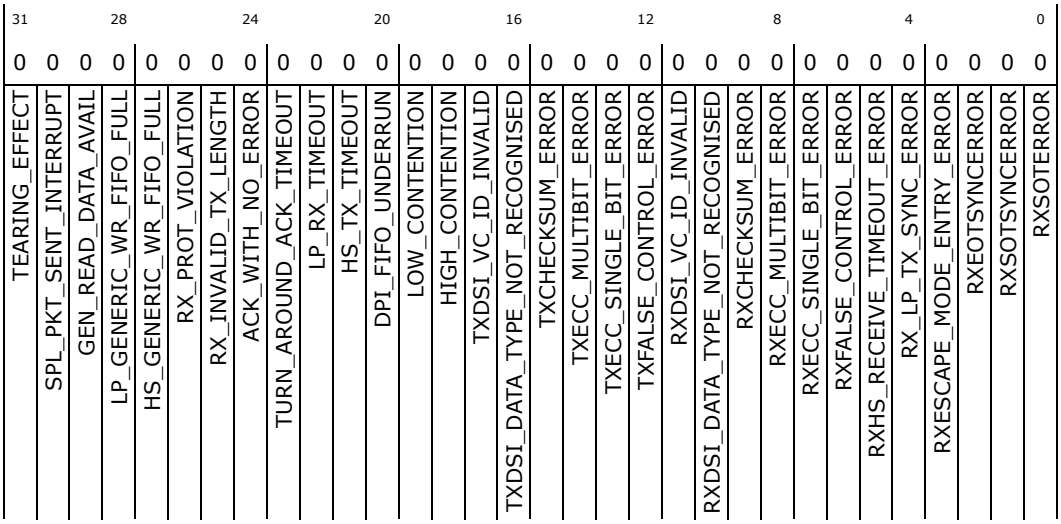
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_INTR_STAT_REG: [GTTMMADR_LSB + 2BF20h] + B004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**TEARING_EFFECT:** Set to indicate that tearing effect trigger message is Received
30	0b RW	**SPL_PKT_SENT_INTERRUPT:** Set to confirm the transmission of the DPI event specific commands set in the dpi control and dpi data register

Bit Range	Default & Access	Description
29	0b RW	**GEN_READ_DATA_AVAIL:** Set to indicate that the requested data for a Generic Read request is available in the buffer i.e., generic read response data is available in the read FIFO
28	0b RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full
27	0b RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0b RW	**RX_PROT_VIOLATION:** Set if DSI protocol violation error is reported in the acknowledge packet by the display device
25	0b RW	**RX_INVALID_TX_LENGTH:** Set if invalid transmission length error is reported in the acknowledge packet by the display device
24	0b RW	**ACK_WITH_NO_ERROR:** Set if acknowledge trigger message is received with out any error
23	0b RW	**TURN_AROUND_ACK_TIMEOUT:** Set if a turn around acknowledgement sequence is not received from the display device
22	0b RW	**LP_RX_TIMEOUT:** Set if a low power reception count expires this interrupt is generated
21	0b RW	**HS_TX_TIMEOUT:** Set if a high speed transmission prevails for more than the expected count value this interrupt is raised
20	0b RW	**DPI_FIFO_UNDERRUN:** Set to '1' if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0b RW	**LOW_CONTENTION:** Set to '1' if a LP low fault is registered by at the D-PHY contention detector
18	0b RW	**HIGH_CONTENTION:** Set to '1' if a LP high fault is registered by at the D-PHY contention detector
17	0b RW	**TXDSI_VC_ID_INVALID:** Set to '1' if the received virtual channel ID is invalid
16	0b RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the received data type is not recognized
15	0b RW	**TXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value during the reception of packets by Arasan_DSI host.
14	0b RW	**TXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan_DSI_host
13	0b RW	**TXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan_DSI_host
12	0b RW	**TXFALSE_CONTROL_ERROR:** Set to '1' if a control error is observed on the lanes by the Arasan_DSI_host
11	0b RW	**RXDSI_VC_ID_INVALID:** Set to '1' if the virtual channel ID is invalid by the display device is reported in the Acknowledge packet by the display device
10	0b RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the data type is not recognized by the display device is reported in the Acknowledge packet by the display device

Bit Range	Default & Access	Description
9	0b RW	**RXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value and is reported in the Acknowledge packet by the display device
8	0b RW	**RXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet is reported in the Acknowledge packet by the display device
7	0b RW	**RXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and corrected for one bit error is reported in the Acknowledge packet by the display device
6	0b RW	**RXFALSE_CONTROL_ERROR:** Set to '1' if a control error is reported in the Acknowledge packet by the display device
5	0b RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to '1' if the high speed receive timer value expires and data transfer lasts on the data lane is reported in the Acknowledge packet by the display device
4	0b RW	**RX_LP_TX_SYNC_ERROR:** Set to '1' if Low power transmission sync error occurs in the display device and is reported in the Acknowledge packet by the display device
3	0b RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to '1' if Escape Mode Entry command is not understandable by the display device and is reported in the Acknowledge packet by the display device
2	0b RW	**RXEOTSYNCERROR:** RX eot sync Error
1	0b RW	**RXSOTSYNCERROR:** Set to '1' if a start of transmission synchronisation error is reported in the Acknowledge packet by the display device
0	0b RW	**RXSOTERROR:** Set to '1' if a start of transmission error is reported in the Acknowledge packet by the display device

3.1.47 MIPIA_INTR_EN_REG—Offset B008h

mipi pipe A interrupt enable register

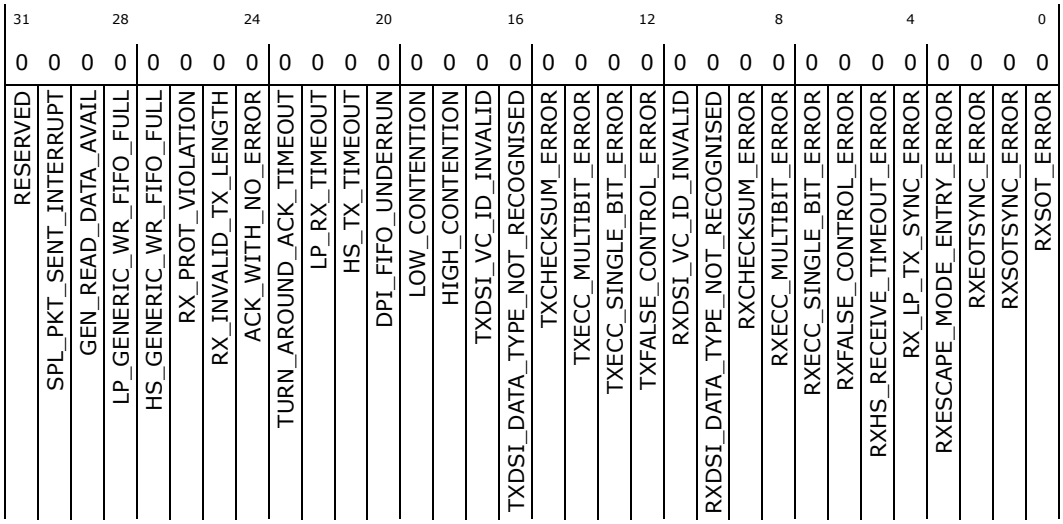
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_INTR_EN_REG: [GTTMMADR_LSB + 2BF20h] + B008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**TEARING_EFFECT (RESERVED):** set to enable tearing effect interrupt.
30	0b RW	**SPL_PKT_SENT_INTERRUPT:** Set to enable the confirmation of transmission of the DPI event specific commands set in the dpi control and dpi data register
29	0b RW	**GEN_READ_DATA_AVAIL:** Set to enable Generic Read available interrupt
28	0b RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full
27	0b RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0b RW	**RX_PROT_VIOLATION:** Set to enable protocol violation error
25	0b RW	**RX_INVALID_TX_LENGTH:** Set to enable invalid transmission length error
24	0b RW	**ACK_WITH_NO_ERROR:** Set to enable acknowledge trigger message reception with out any error
23	0b RW	**TURN_AROUND_ACK_TIMEOUT:** Set to enable turn around acknowledgement ,sequence timeout
22	0b RW	**LP_RX_TIMEOUT:** Set to enable low power reception count time outs
21	0b RW	**HS_TX_TIMEOUT:** Set to enable a high speed transmission timeout
20	0b RW	**DPI_FIFO_UNDERRUN:** Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0b RW	**LOW_CONTENTION:** Set to enable a LP low fault interrupt
18	0b RW	**HIGH_CONTENTION:** Set to enable a LP high fault interrupt

Bit Range	Default & Access	Description
17	0b RW	**TXDSI_VC_ID_INVALID:** Set to enable the interrupt if the received packets virtual channel ID is invalid
16	0b RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt if the received packets data type is not recognized
15	0b RW	**TXCHECKSUM_ERROR:** Set to enable the interrupt if the computed CRC differs from the received CRC value for the received packets
14	0b RW	**TXECC_MULTIBIT_ERROR:** Set to enable the interrupt if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan DSI host
13	0b RW	**TXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan DSIhost
12	0b RW	**TXFALSE_CONTROL_ERROR:** Set to enable the interrupt for the control error.,observed on the lanes by the Arasan_DSI_host
11	0b RW	**RXDSI_VC_ID_INVALID:** Set to enable the interrupt for invalid virtual channel ID in the acknowledgment packet reports
10	0b RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt for the un recognized data type in the acknowledgment packet reports
9	0b RW	**RXCHECKSUM_ERROR:** Set to enable the interrupt for the computed CRC differs from the received CRC value in the acknowledgment packet reports
8	0b RW	**RXECC_MULTIBIT_ERROR:** Set to enable the interrupt for no ECC correction for the packet or there are more than 2 bit errors reported in the acknowledgment packet
7	0b RW	**RXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt for ECC syndrome computation and one bit error correction for the acknowledgment packet
6	0b RW	**RXFALSE_CONTROL_ERROR:** Set to enable the interrupt for control error in the acknowledgment packet reports
5	0b RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to enable the interrupt for the high speed receive timeout Error in the acknowledgment packet reports
4	0b RW	**RX_LP_TX_SYNC_ERROR:** Set to enable the interrupt for Low power transmission sync error in the acknowledgment packet reports
3	0b RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to enable the interrupt for Escape Mode Entry command error in the acknowledgment packet reports
2	0b RW	**RXEOTSYNC_ERROR:** Set to enable the interrupt for End of transmission synchronisation Error in the acknowledgement packet reports
1	0b RW	**RXSOTSYNC_ERROR:** Set to enable the interrupt for start of transmission synchronisation error in the acknowledgement packet reports
0	0b RW	**RXSOT_ERROR:** Set to enable the interrupt for start of transmission error in the acknowledgment packet reports

3.1.48 MIPIA_DSI_FUNC_PRG__REG—Offset B00Ch

mipi pipe A dsi function program register

Access Method

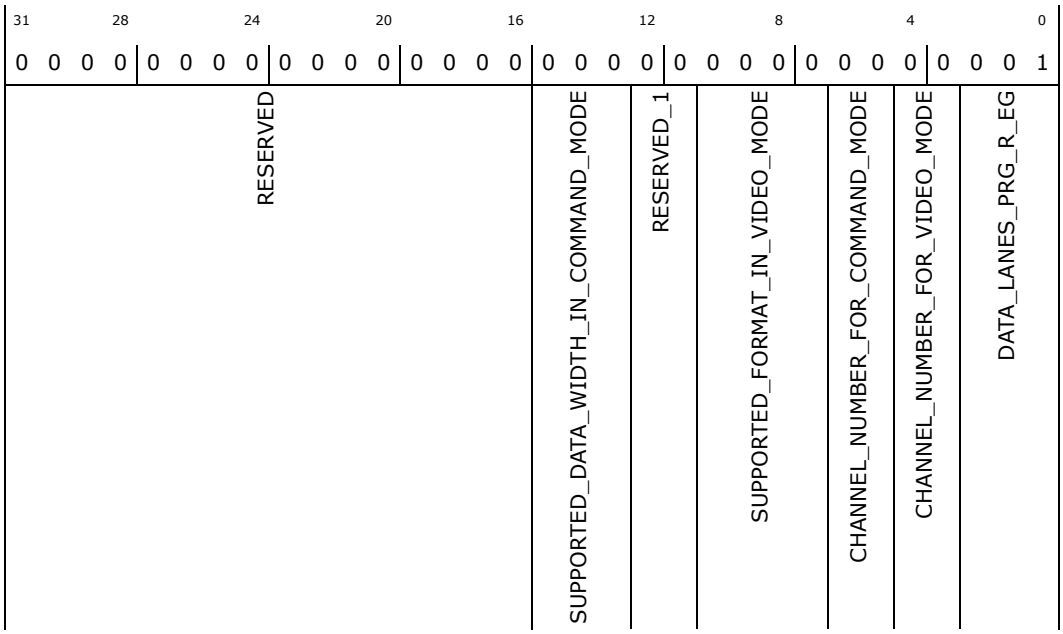
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DSI_FUNC_PRG__REG: [GTTMMADR_LSB + 2BF20h] + B00Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:13	0b RW	**SUPPORTED_DATA_WIDTH_IN_COMMAND_MODE:** 000 --) Reserved, 001 --) 16 bit data , 010 --) 9 bit data , 011 --) 8 bit data , 100 --) option 1 : 101 --) option 2 : 110 to 111 --) Reserved
12:11	0b RW	**RESERVED_1:** Reserved.
10:7	0b RW	**SUPPORTED_FORMAT_IN_VIDEO_MODE:** Supported color format, 0001 --) RGB565, 0010 --) RGB666, 0011 --) RGB 666 loosely packed format, 0100 --) RGB888
6:5	0b RW	**CHANNEL_NUMBER_FOR_COMMAND_MODE:** Virtual channel number for command mode is programmed by the processor
4:3	0b RW	**CHANNEL_NUMBER_FOR_VIDEO_MODE:** Virtual channel number for command mode is programmed by the processor
2:0	001b RW	**DATA_LANES_PRG_R_EG:** Number of data lanes to be supported is programmed by the processor

3.1.49 MIPIA_HS_TX_TIMEOUT_REG—Offset B010h

mipi piepe A HS TX time-out register

Access Method

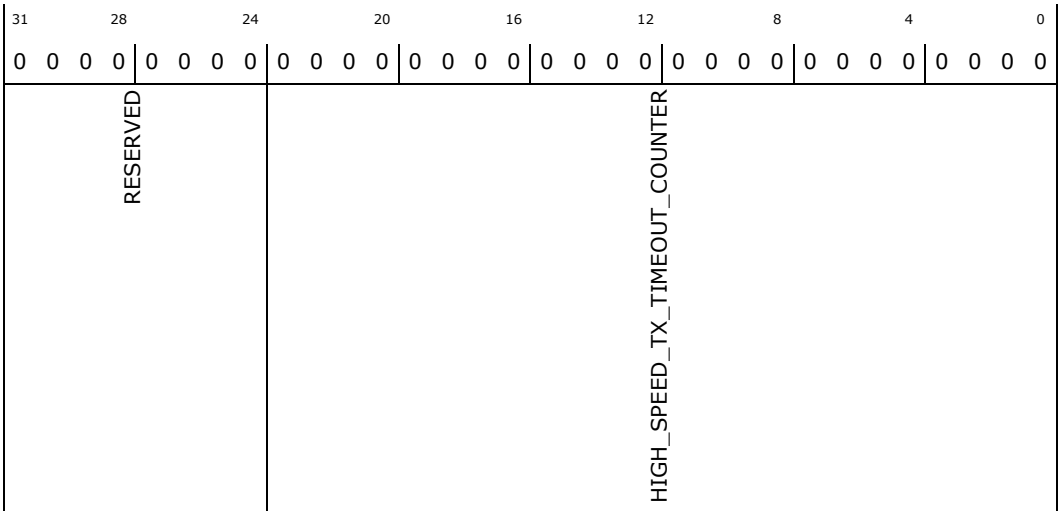
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_HS_TX_TIMEOUT_REG: [GTTMMADR_LSB + 2BF20h] + B010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:0	0b RW	**HIGH_SPEED_TX_TIMEOUT_COUNTER:** The maximum duration allowed for the DSI host ,to remain in high speed mode for a transmission. If the counter expires, HS mode is terminated with EOT and the lanes enter stop state

3.1.50 MIPIA_LP_RX_TIMEOUT_REG—Offset B014h

mipi pipe A LP RX timeout register

Access Method

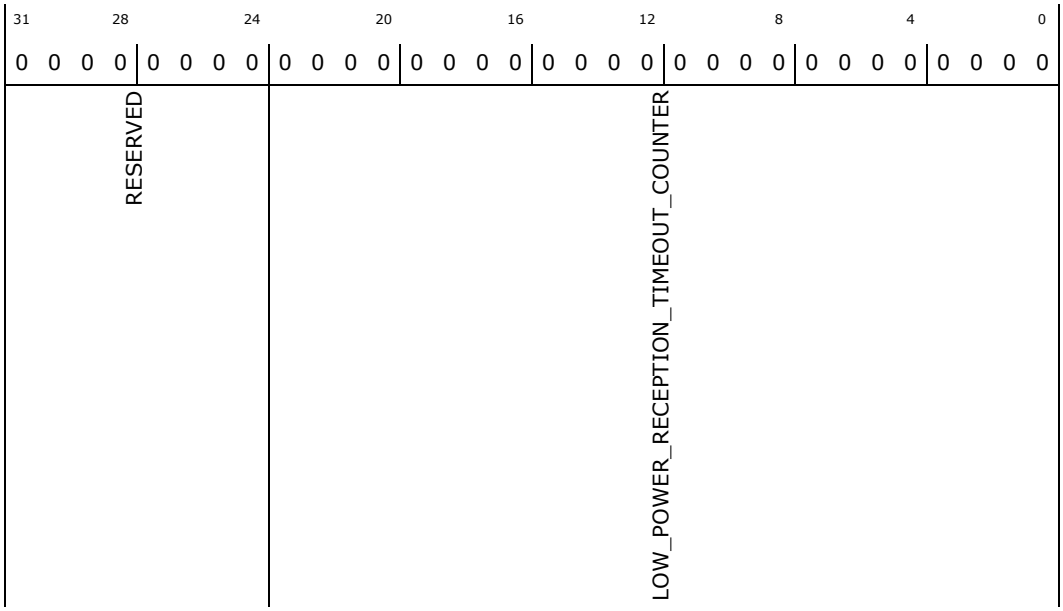
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_LP_RX_TIMEOUT_REG: [GTTMMADR_LSB + 2BF20h] + B014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:0	0b RW	**LOW_POWER_RECEPTION_TIMEOUT_COUNTER:** Timeout value to be checked for received short packets .If the timer expires the DSI Host enters stop state

3.1.51 MIPIA_TURN_AROUND_TIMEOUT_REG—Offset B018h

mipi pipe A turn around timeout register

Access Method

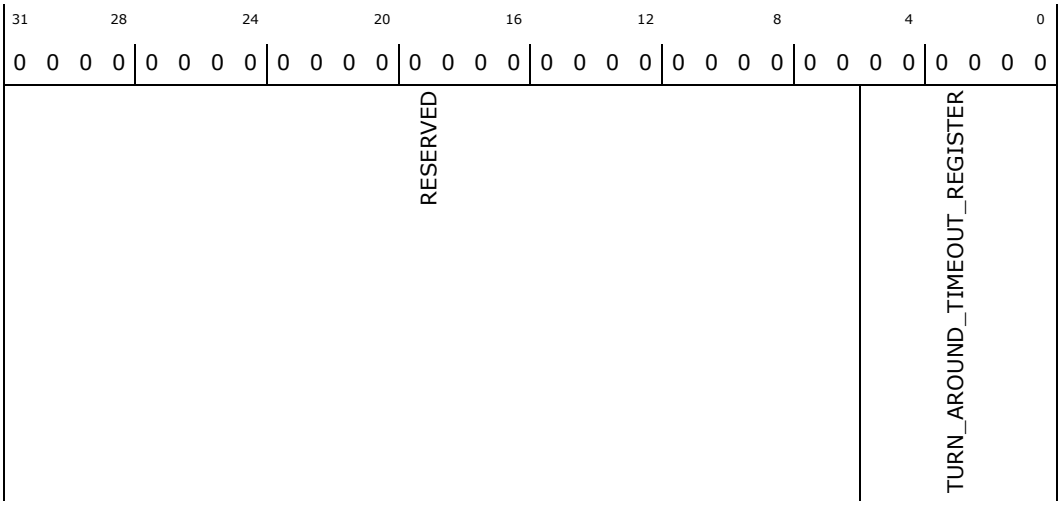
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_TURN_AROUND_TIMEOUT_REG: [GTTMMADR_LSB + 2BF20h] + B018h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**RESERVED:** Reserved.
5:0	0b RW	**TURN_AROUND_TIMEOUT_REGISTER:** Timeout value to be checked after the DSI host makes a turn around in the direction of transfers. If the timer expires the DSI Host enters stop state

3.1.52 MIPIA_DEVICE_RESET_TIMER—Offset B01Ch

mipi pipe A device reset timer

Access Method

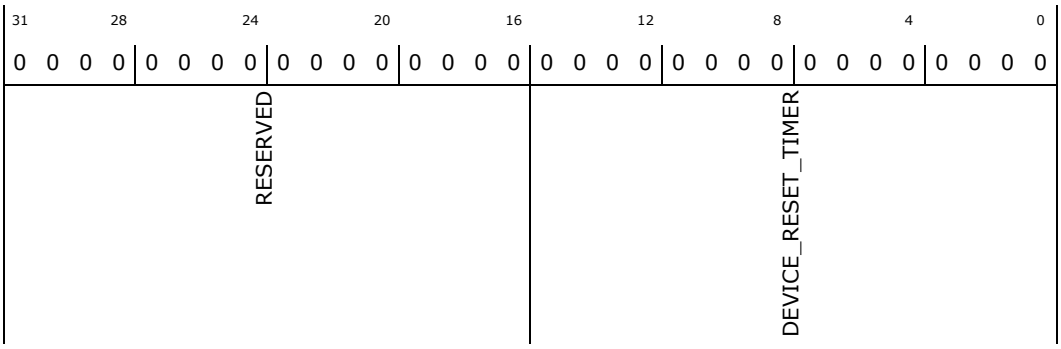
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DEVICE_RESET_TIMER: [GTTMMADR_LSB + 2BF20h] + B01Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**DEVICE_RESET_TIMER:** Timeout value to be checked for device to be reset after issuing reset entry command. If the timer expires the DSI Host enters normal operation

3.1.53 MIPIA_DPI_RESOLUTION_REG—Offset B020h

mipi piepe A DPI Resolution reg

Access Method

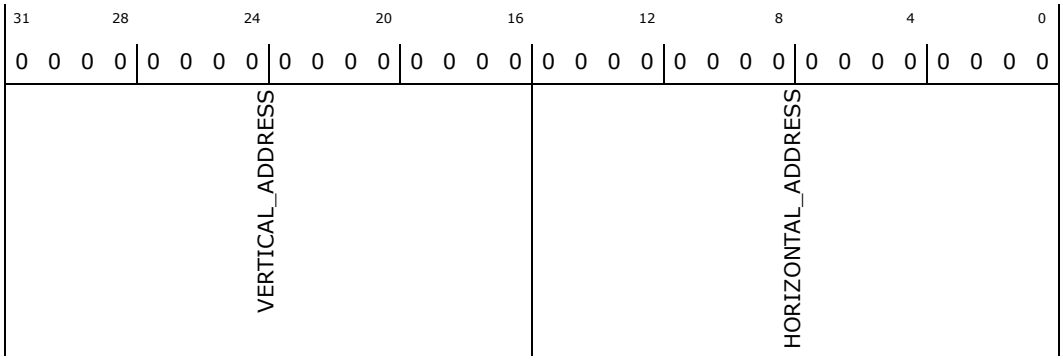
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DPI_RESOLUTION_REG: [GTTMMADR_LSB + 2BF20h] + B020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**VERTICAL_ADDRESS:** Shows the vertical address count in lines
15:0	0b RW	**HORIZONTAL_ADDRESS:** Shows the horizontal address count in pixels

3.1.54 MIPIA_DBI_RESOLUTION_REG—Offset B024h

mipi A DBI resolution reg

Access Method

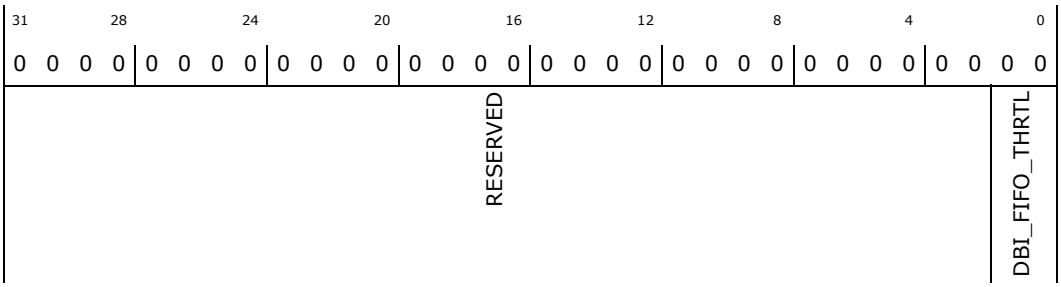
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DBI_RESOLUTION_REG: [GTTMMADR_LSB + 2BF20h] + B024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**RESERVED:** Reserved.
1:0	0b RW	**DBI_FIFO_THRTL:** DBI FIFO's watermark can be set using the following bits so as to enable dbi_stall de-assertion whenever the below FIFO condition is reached: 00 - (1/2) DBI fifo empty 01 - (1/4) DBI fifo empty 10 - 7 locations are empty 11 - Reserved

3.1.55 MIPIA_HORIZ_SYNC_PADDING_COUNT—Offset B028h

mipi A horizontal sync padding out

Access Method

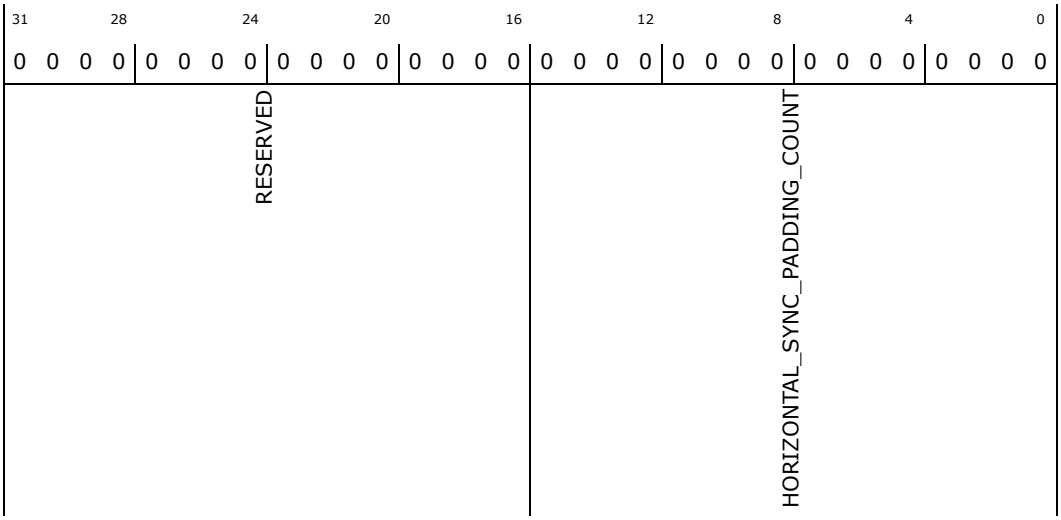
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_HORIZ_SYNC_PADDING_COUNT: [GTTMMADR_LSB + 2BF20h] + B028h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_SYNC_PADDING_COUNT:** Shows the horizontal sync padding value in terms of txbyteclkhs

3.1.56 MIPIA_HORIZ_BACK_PORCH_COUNT—Offset B02Ch

mipi pipe A horizontal back porch counter

Access Method

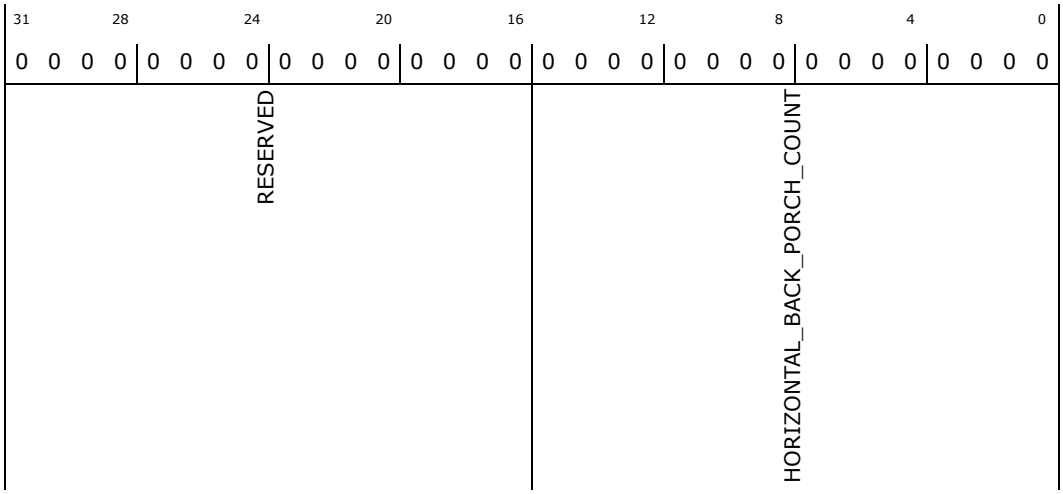
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_HORIZ_BACK_PORCH_COUNT: [GTTMMADR_LSB + 2BF20h] + B02Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_BACK_PORCH_COUNT:** Shows the horizontal back porch value in terms of txbyteclkhs

3.1.57 MIPIA_HORIZ_FRONT_PORCH_COUNT—Offset B030h

mipi pipe A horizontal front porch counter

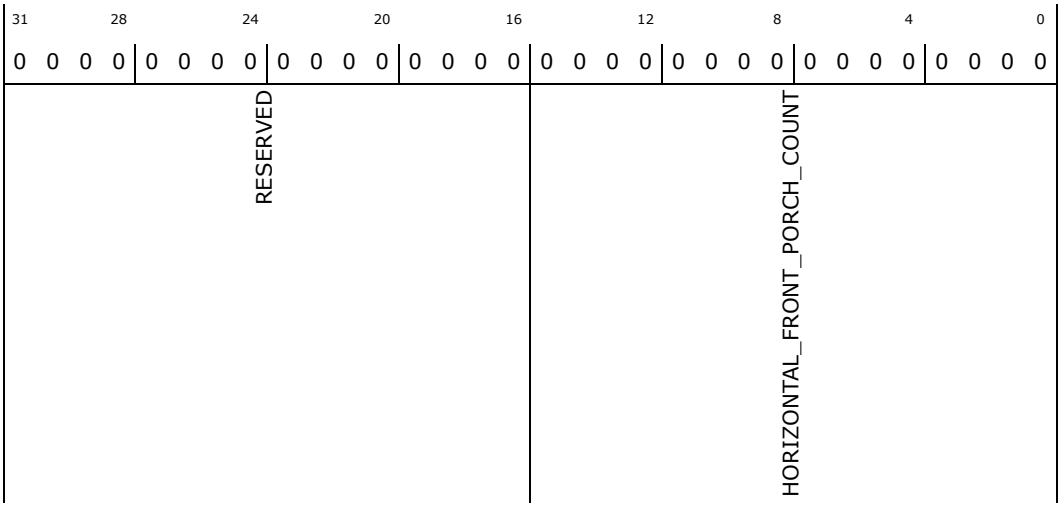
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_HORIZ_FRONT_PORCH_COUNT: [GTTMMADR_LSB + 2BF20h] + B030h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_FRONT_PORCH_COUNT:** Shows the horizontal front porch value in terms of txbyteclkhs

3.1.58 MIPIA_HORIZ_ACTIVE_AREA_COUNT—Offset B034h

mipi A horizontal active area counter

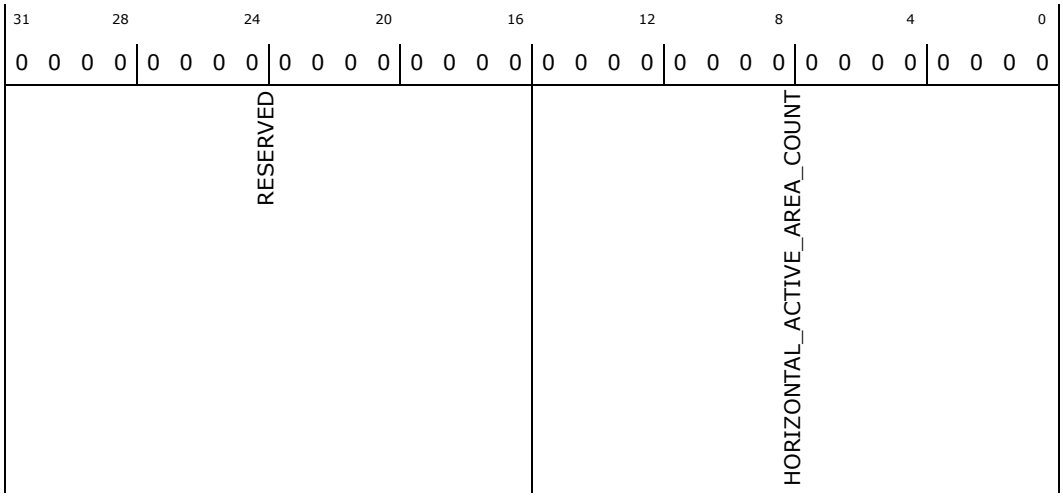
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_HORIZ_ACTIVE_AREA_COUNT: [GTTMMADR_LSB + 2BF20h] + B034h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_ACTIVE_AREA_COUNT:** Shows the horizontal active area value in terms of txbyteclkhs

3.1.59 MIPIA_VERT_SYNC_PADDING_COUNT—Offset B038h

mipi pipe A vertical sync padding counter

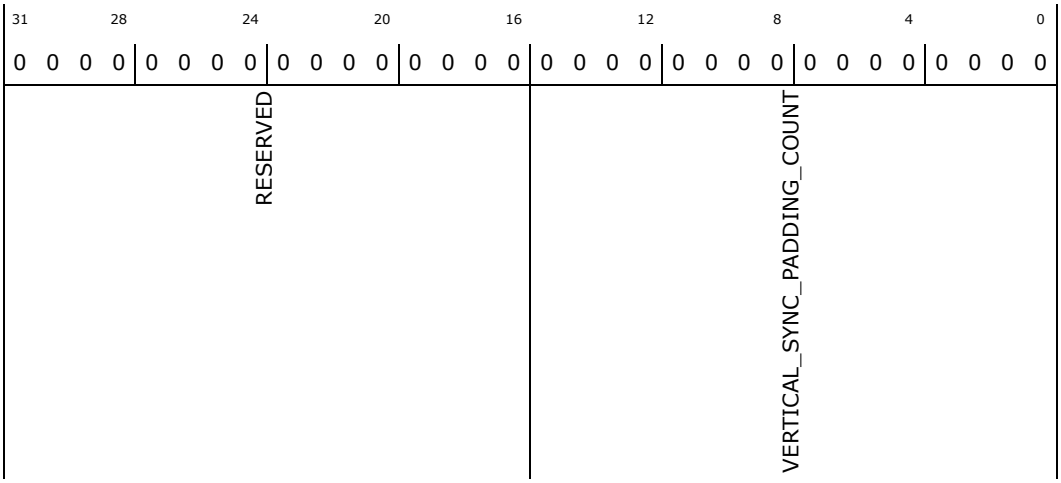
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_VERT_SYNC_PADDING_COUNT: [GTTMMADR_LSB + 2BF20h] + B038h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_SYNC_PADDING_COUNT:** Shows the vertical sync padding value in terms of lines

3.1.60 MIPIA_VERT_BACK_PORCH_COUNT—Offset B03Ch

mipi pipe A vertical back portch counter

Access Method

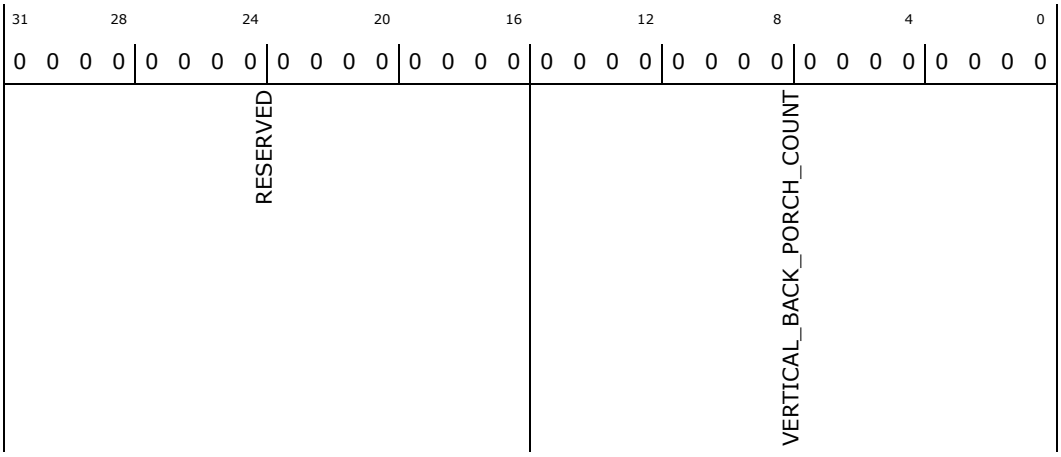
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_VERT_BACK_PORCH_COUNT: [GTTMMADR_LSB + 2BF20h] + B03Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_BACK_PORCH_COUNT:** Shows the vertical back porch value in terms of lines

3.1.61 MIPIA_VERT_FRONT_PORCH_COUNT—Offset B040h

mipi pipe A vertical front portch counter

Access Method

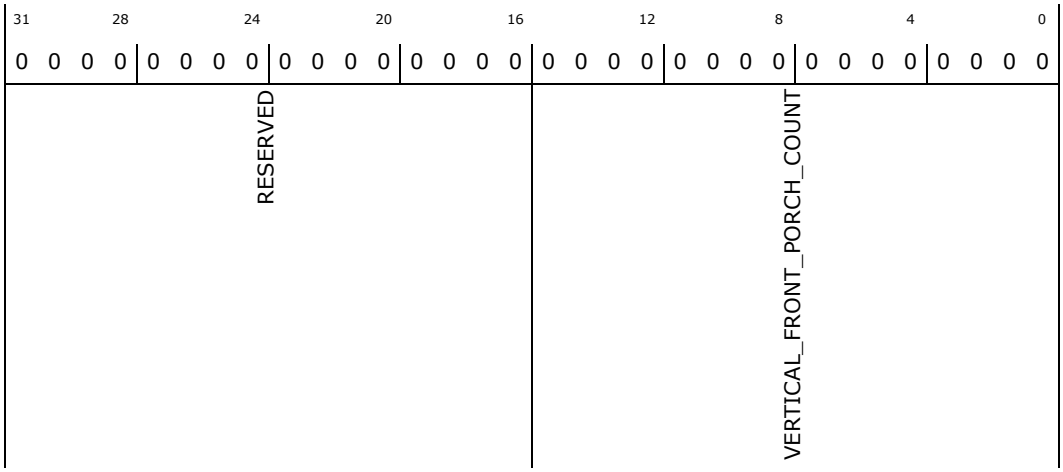
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_VERT_FRONT_PORCH_COUNT: [GTTMMADR_LSB + 2BF20h] + B040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_FRONT_PORCH_COUNT:** Shows the vertical front porch value in terms of lines

3.1.62 MIPIA_HIGH_LOW_SWITCH_COUNT—Offset B044h

mipi A high low switch count

Access Method

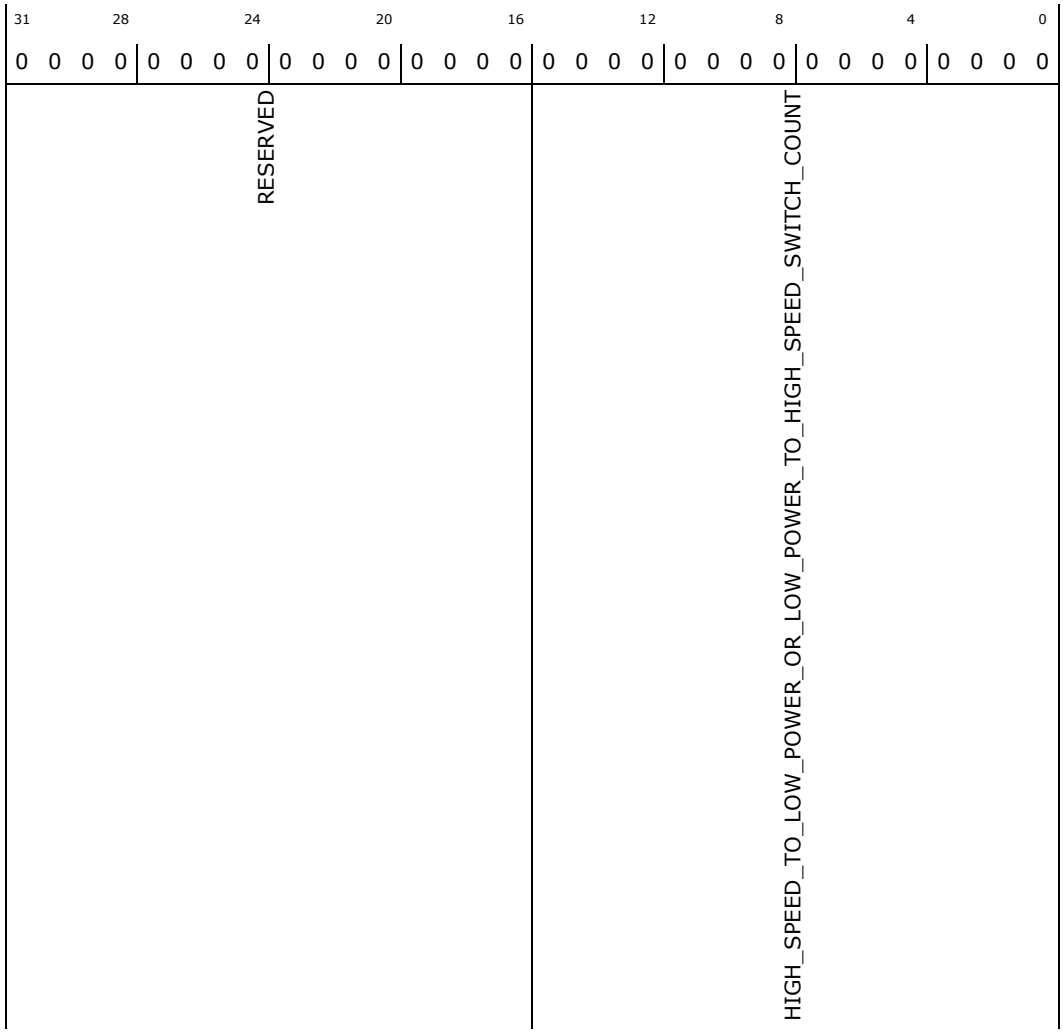
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_HIGH_LOW_SWITCH_COUNT: [GTTMMADR_LSB + 2BF20h] + B044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs
15:0	0b RW	**HIGH_SPEED_TO_LOW_POWER_OR_LOW_POWER_TO_HIGH_SPEED_SWITCH_COUNT:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs

3.1.63 MIPIA_DPI_CTRL_REG—Offset B048h

mipi A dpi ctrl register

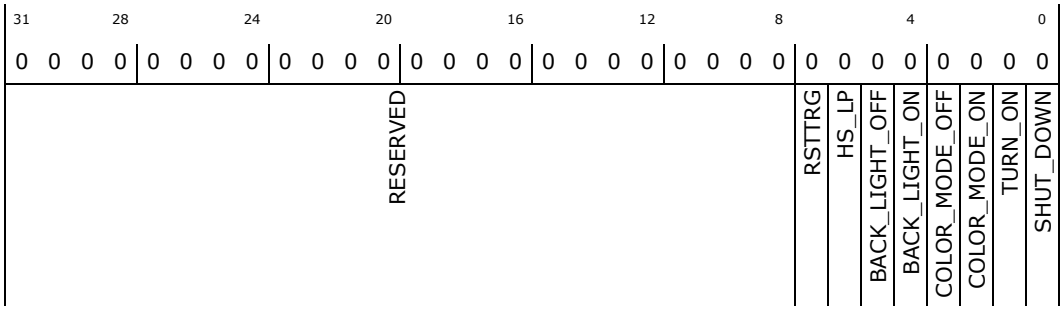
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DPI_CTRL_REG: [GTTMMADR_LSB + 2BF20h] + B048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**RESERVED:**
7	0b RW	**RSTTRG:** mipi A dpi ctrl reg RSTTRG
6	0b RW	**HS_LP:** Set to '0' to indicate the special packets are sent through the DSI link using HS transmission and set to '1' to indicate that the special packets are sent through the DSI link using low power mode
5	0b RW	**BACK_LIGHT_OFF:** Set to '1' to indicate a backlight OFF short packet has to be packetised for the DPI's virtual channel
4	0b RW	**BACK_LIGHT_ON:** Set to '1' to indicate a backlight ON short packet has to be packetised for the DPI's virtual channel
3	0b RW	**COLOR_MODE_OFF:** Set to '1' to indicate a color mode OFF short packet has to be packetised for the DPI's virtual channel
2	0b RW	**COLOR_MODE_ON:** Set to '1' to indicate a color mode ON short packet has to be packetised for the DPI's virtual channel
1	0b RW	**TURN_ON:** Set to '1' to indicate a turn on short packet has to be packetised for the DPI's virtual channel
0	0b RW	**SHUT_DOWN:** Set to '1' to indicate a shut down short packet has to be packetised for the DPI's virtual channel

3.1.64 MIPIA_DPI_DATA_REGISTER—Offset B04Ch

mipi A dpi data register

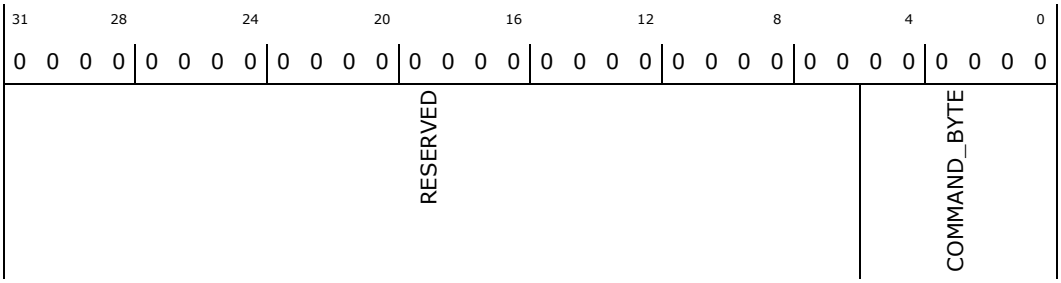
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DPI_DATA_REGISTER: [GTTMMADR_LSB + 2BF20h] + B04Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**RESERVED:** Reserved.
5:0	0b RW	**COMMAND_BYTE:** Command Byte to represent the new or not defined command bytes usage for special features representation. [Like backlight ON and OFF]. This register should be programmed before the DPI control register is being programmed for backlight ON/OFF

3.1.65 MIPIA_INIT_COUNT_REGISTER—Offset B050h

mipi A init count register

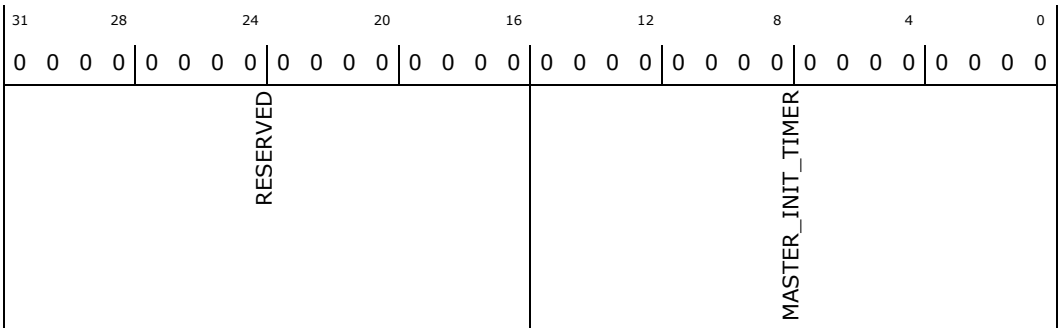
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_INIT_COUNT_REGISTER: [GTTMMADR_LSB + 2BF20h] + B050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**MASTER_INIT_TIMER:** Counter value in terms of low power clock to initialise the DSI Host IP [TINT] that drives a stop state on the mipi's D-PHY bus

3.1.66 MIPIA_MAX_RETURN_PKT_SIZE_REGISTER—Offset B054h

mipi A max return pkt size register

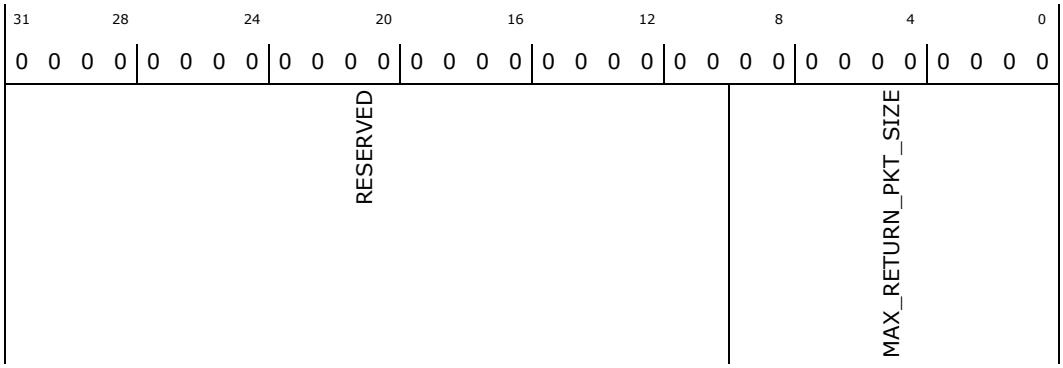
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_MAX_RETURN_PKT_SIZE_REGISTER: [GTTMMADR_LSB + 2BF20h] + B054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0b RW	**RESERVED:** Reserved.
9:0	0b RW	**MAX_RETURN_PKT_SIZE:** Set the count value in bytes to collect the return data packet for reverse direction data flow in data lane0 in response to a DBI read operation

3.1.67 MIPIA_VIDEO_MODE_FORMAT_REGISTER—Offset B058h

mipi A video mode format register

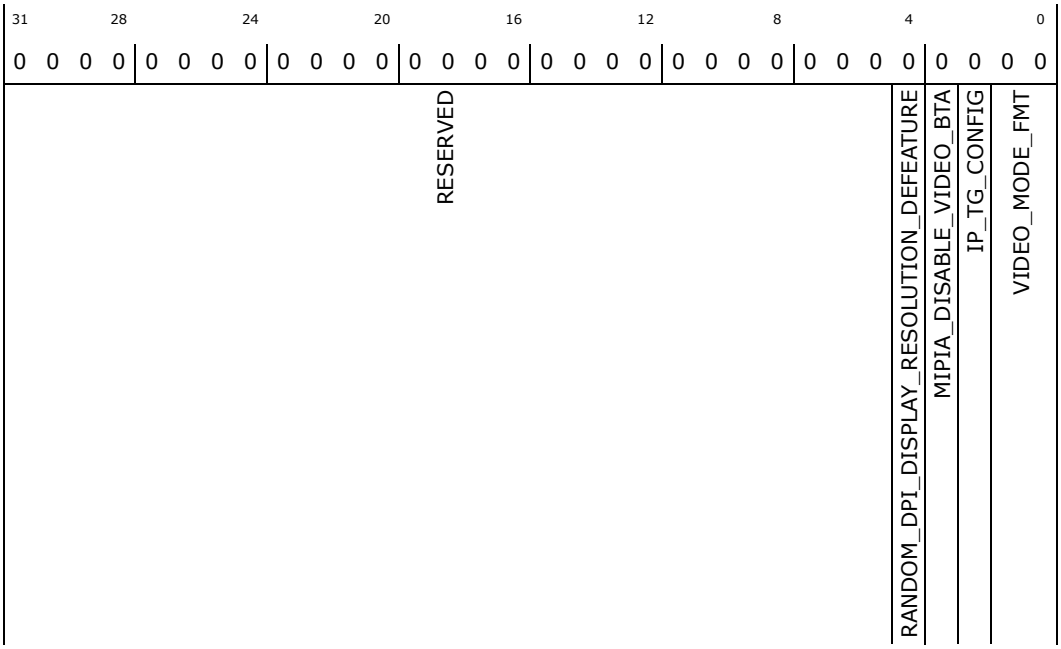
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_VIDEO_MODE_FORMAT_REGISTER: [GTTMMADR_LSB + 2BF20h] + B058h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RW	**RESERVED:** Reserved.
4	0b RW	**RANDOM_DPI_DISPLAY_RESOLUTION_DEFEATURE:** Set by the processor to support random DPI display resolution 0 - random DPI display resolution support disabled. 1 - random DPI display resolution support enabled.
3	0b RW	**MIPIA_DISABLE_VIDEO_BTA:** Set by the processor to inform the DSI controller to disable the BTA sent at the last blanking line of VFP. By default, this bit is set to 0.0 BTA sending at the last blanking line of VFP is enabled. 1 BTA sending at the last blanking line of VFP is disabled.
2	0b RW	**IP_TG_CONFIG:** Set by the processor to inform that the DSI controller should discontinue the DPI transfer after the last line of the VFP after ip_tg_enable deassertion. By default, this bit is set to 0. 0 - After ip_tg_enable deassertion, DSI Tx controller stops the DPI transfer immediately after the current packet is transmitted. 1 - After ip_tg_enable deassertion, DSI Tx controller discontinues the DPI transfer after the last line of the VFP

Bit Range	Default & Access	Description
1:0	0b RW	**VIDEO_MODE_FMT:** Sets the Video mode format (packet sequence) to be supported in DSI. In Non Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed equal to RGB word count value In Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed greater than the RGB word count value, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link. 00 Reserved 01 - Non Burst Mode with Sync Pulse 10 - Non Burst Mode with Sync events 11 - Burst Mode

3.1.68 MIPIA_EOT_DISABLE_REGISTER—Offset B05Ch

mipi A eot disable register

Access Method

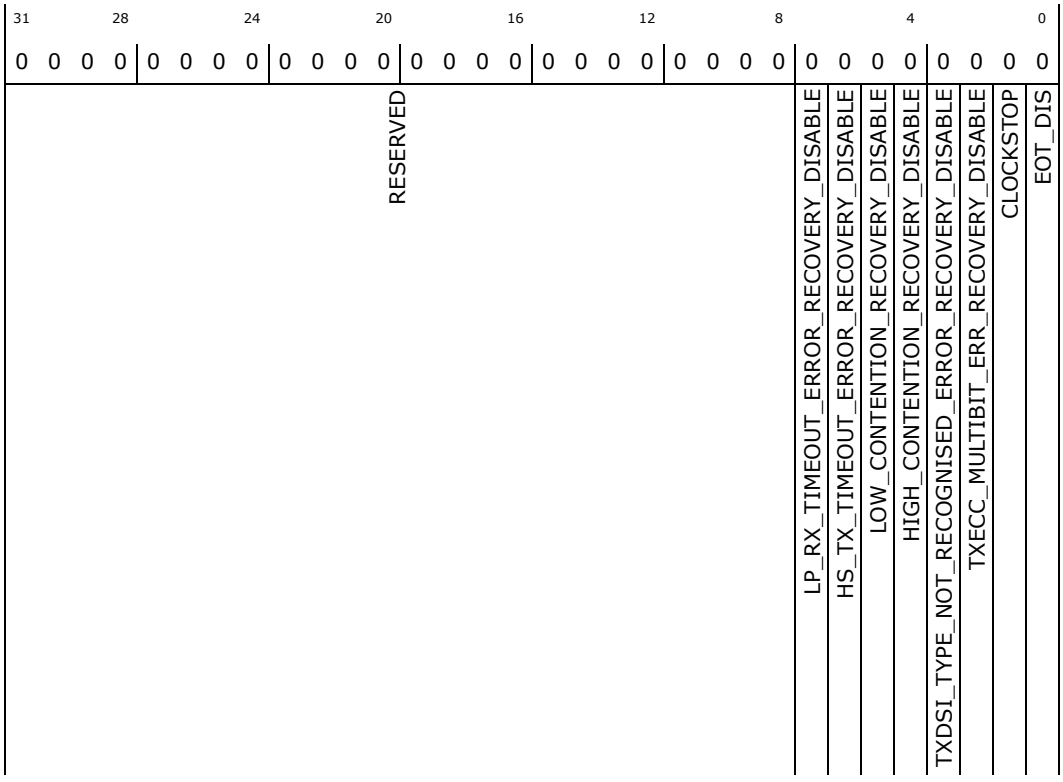
Type: Memory Mapped I/O Register (Size: 32 bits)

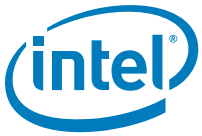
MIPIA_EOT_DISABLE_REGISTER: [GTTMMADR_LSB + 2BF20h] + B05Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31:8	0b RW	**RESERVED:** Reserved.
7	0b RW	**LP_RX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the LP_Rx_timeout error recovery if the processor clears LP_Rx_timeout error interrupt. 0 - LP_Rx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the LP_Rx_timeout error interrupt. 1 - If the processor clears the LP_Rx_timeout error interrupt, LP_Rx_timeout error recovery action will not happen in DSI Tx controller. LP Rx timeout error interrupt will act as an informative interrupt
6	0b RW	**HS_TX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the HS_Tx_timeout error recovery if the processor clears HS_Tx_timeout interrupt. 0 - HS_Tx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the HS_Tx_timeout error interrupt. 1 - If the processor clears the HS_Tx_timeout error interrupt, HS_Tx_timeout error recovery action will not happen in DSI Tx controller. HS Tx timeout error interrupt will act as an informative interrupt
5	0b RW	**LOW_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears Low contention interrupt. 0 - Contention recovery will happen if the processor clears Low contention interrupt. 1 - If the processor clears the low contention interrupt, contention recovery procedure will not be initiated by the DSI Tx controller. Low contention interrupt will act as an informative interrupt
4	0b RW	**HIGH_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears High contention interrupt. 0 - Contention recovery will happen if the processor clears High contention interrupt. 1 - If the processor clears the high contention interrupt, contention recovery procedure will not be initiated by the DSI Tx controller. Ignore the High Contention Interrupt in MIPI_INTR_STAT_REG
3	0b RW	**TXDSI_TYPE_NOT_RECOGNISED_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if TxDSI data type not recognized error interrupt is cleared by the processor. 0 - Error recovery action will be taken if TxDSI data type not recognized error interrupt is cleared by the processor. 1 - If TxDSI data type not recognized error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx DSI data type not recognized error interrupt will act as an informative interrupt
2	0b RW	**TXECC_MULTIBIT_ERR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if Tx ECC multibit error interrupt is cleared by the processor. 0 - Error recovery action will be taken if Tx ECC multibit error interrupt is cleared by the processor. 1 - If Tx ECC multibit error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx multibit error interrupt will act as an informative interrupt
1	0b RW	**CLOCKSTOP:** Set by the processor to enable or disable clock stopping feature during BLLP timing in a DPI transfer in dual channel mode or during DPI only mode and also when there is no traffic in the DBI interface in DBI only enabled mode. By default this register value is 0. 0 - clock stopping disabled 1 - clock stopping enabled

Bit Range	Default & Access	Description
0	0b RW	**EOT_DIS:** Set by the processor to enable or disable EOT short packet transmission. By default this register value is 0. For backward compatibility of earlier DSI systems, EOT short packet transmission can be disabled. 0 - EOT short packet transmission enabled 1 - EOT short packet transmission disabled

3.1.69 MIPIA_LP_BYTECLK_REGISTER—Offset B060h

mipi A LP bytclk register

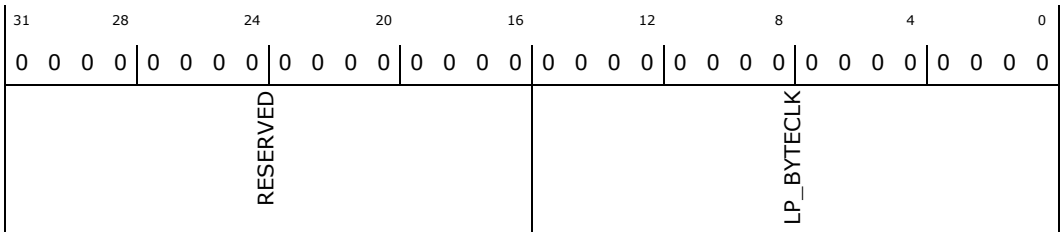
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_LP_BYTECLK_REGISTER: [GTTMMADR_LSB + 2BF20h] + B060h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**LP_BYTECLK:** Low power clock equivalence in terms of byte clock. The value programmed in this register is equal to the number of byte clocks occupied in one low power clock. This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc)

3.1.70 MIPIA_LP_GEN_DATA_REGISTER—Offset B064h

mipi A LP gen DATA register

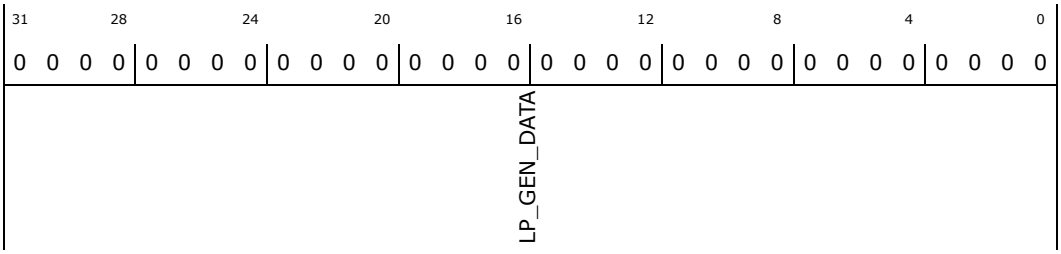
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_LP_GEN_DATA_REGISTER: [GTTMMADR_LSB + 2BF20h] + B064h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**LP_GEN_DATA:** Data port register used for generic data transfers in low power mode

3.1.71 MIPIA_HS_GEN_DATA_REGISTER—Offset B068h

mipi A HS GEN data register

Access Method

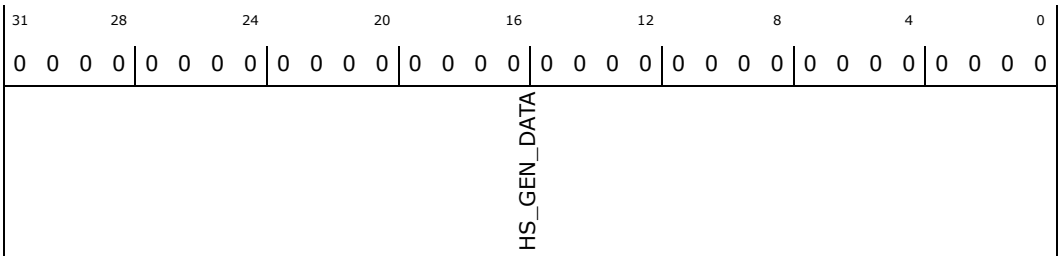
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_HS_GEN_DATA_REGISTER: [GTTMMADR_LSB + 2BF20h] + B068h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**HS_GEN_DATA:** Data port register used for generic data transfers in low power mode

3.1.72 MIPIA_LP_GEN_CTRL_REGISTER—Offset B06Ch

mipi A LP Gen CTRL register

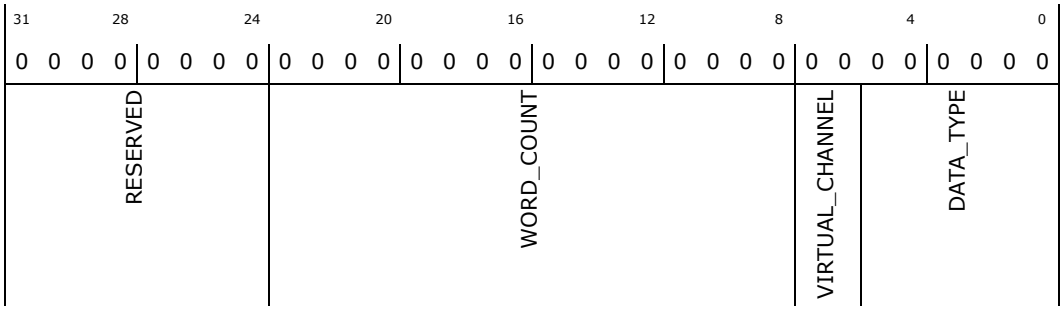
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_LP_GEN_CTRL_REGISTER: [GTTMMADR_LSB + 2BF20h] + B06Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b WO	**RESERVED:** Reserved.
23:8	0b WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0b WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended
5:0	0b WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write , one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

3.1.73 MIPIA_HS_GEN_CTRL_REGISTER—Offset B070h

mipi A HS GEN CTRL register

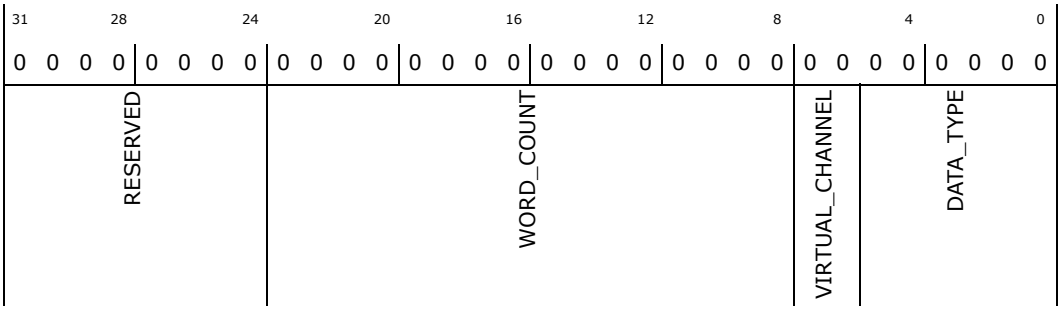
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_HS_GEN_CTRL_REGISTER: [GTTMMADR_LSB + 2BF20h] + B070h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b WO	**RESERVED:** Reserved.
23:8	0b WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0b WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended
5:0	0b WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write, one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

3.1.74 MIPIA_GEN_FIFO_STAT_REGISTER—Offset B074h

mipi A gen fifo stat register

Access Method

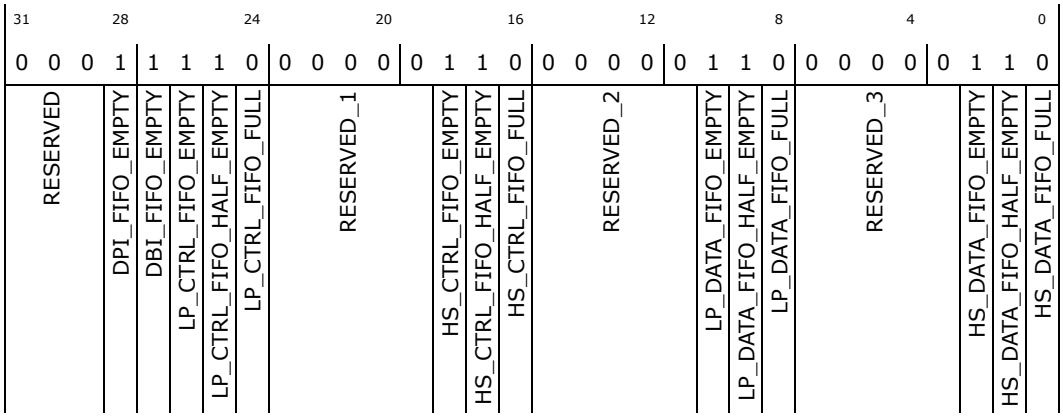
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_GEN_FIFO_STAT_REGISTER: [GTTMMADR_LSB + 2BF20h] + B074h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 1E060606h



Bit Range	Default & Access	Description
31:29	0b RO	**RESERVED:** Reserved.
28	1b RO	**DPI_FIFO_EMPTY:** Default 1
27	1b RO	**DBI_FIFO_EMPTY:** Default 1
26	1b RO	**LP_CTRL_FIFO_EMPTY:** Default 1
25	1b RO	**LP_CTRL_FIFO_HALF_EMPTY:** Default 1
24	0b RO	**LP_CTRL_FIFO_FULL:** Default 0
23:19	0b RO	**RESERVED_1:** Reserved.
18	1b RO	**HS_CTRL_FIFO_EMPTY:** Default 1
17	1b RO	**HS_CTRL_FIFO_HALF_EMPTY:** Default 1
16	0b RO	**HS_CTRL_FIFO_FULL:** Default 0
15:11	0b RO	**RESERVED_2:** Reserved.
10	1b RO	**LP_DATA_FIFO_EMPTY:** Default 1
9	1b RO	**LP_DATA_FIFO_HALF_EMPTY:** Default 1
8	0b RO	**LP_DATA_FIFO_FULL:** Default 0
7:3	0b RO	**RESERVED_3:** Reserved.
2	1b RO	**HS_DATA_FIFO_EMPTY:** Default 1

Bit Range	Default & Access	Description
1	1b RO	**HS_DATA_FIFO_HALF_EMPTY:** Default 1
0	0b RO	**HS_DATA_FIFO_FULL:** Default 0

3.1.75 MIPIA_HS_LS_DBI_ENABLE_REG—Offset B078h

Note : dbi_hs_lp_switch_reg has to be written only if DBI FIFO is empty

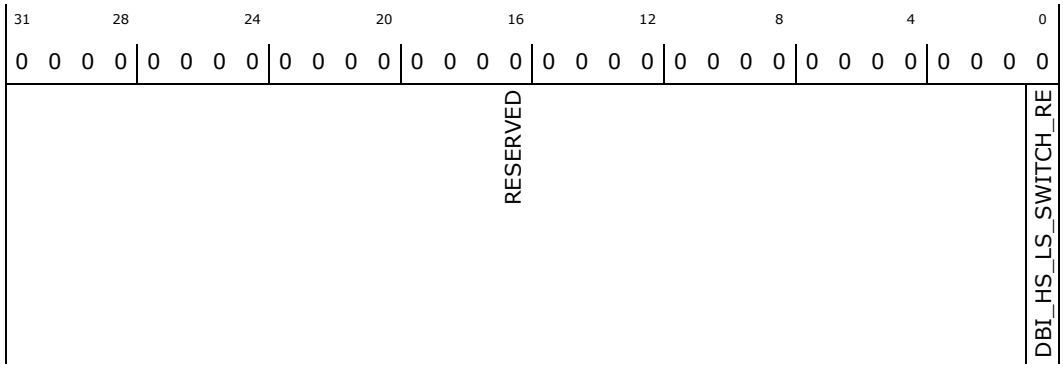
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_HS_LS_DBI_ENABLE_REG: [GTTMMADR_LSB + 2BF20h] + B078h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**RESERVED:** Reserved.
0	0b RW	**DBI_HS_LS_SWITCH_RE:** Set to 1 if DBI packets have to be transmitted in Low power mode Set to 0 if DBI packets have to be transmitted in High speed mode

3.1.76 MIPIA_RESERVED—Offset B07Ch

Reserved.

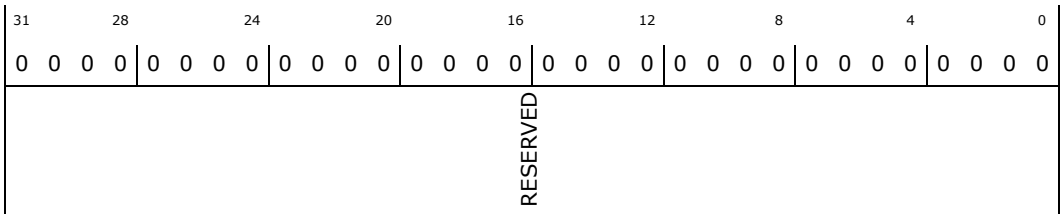
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_RESERVED: [GTTMMADR_LSB + 2BF20h] + B07Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RESERVED:** Reserved.

3.1.77 MIPIA_DPHY_PARAM_REG—Offset B080h

mipi A dphy parameter register

Access Method

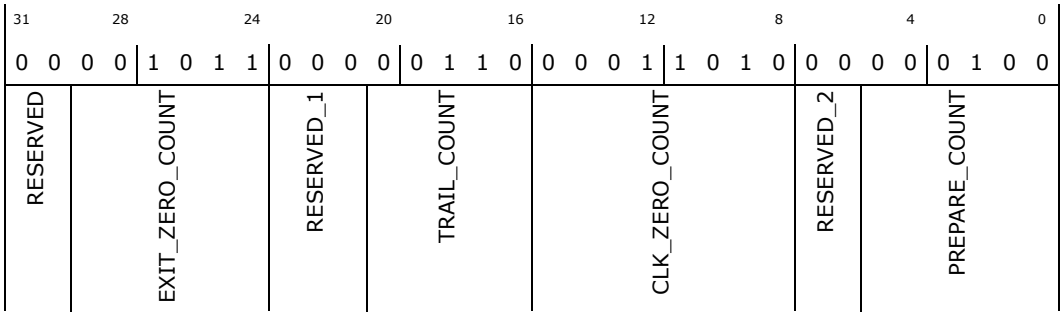
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DPHY_PARAM_REG: [GTTMMADR_LSB + 2BF20h] + B080h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 0B061A04h



Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** Reserved.
29:24	001011b RW	**EXIT_ZERO_COUNT:** THS_0_TIM_UI_CNT and THS_EXIT_TIM_UI_CNT for dphy are programmed as exit zero count by the processor
23:21	0b RW	**RESERVED_1:** Reserved.
20:16	00110b RW	**TRAIL_COUNT:** TCLK_POST_TIM_UI_CNT and TCLK_TRAIL_TIM_UI_CNT for dphy are programmed as trail count by the processor
15:8	00011010b RW	**CLK_ZERO_COUNT:** TCLK_0_TIM_UI_CNT for dphy is programmed as clk zero count by the processor

Bit Range	Default & Access	Description
7:6	0b RW	**RESERVED_2:** Reserved.
5:0	000100b RW	**PREPARE_COUNT:** TCLK_PREP_TIM_UI_CNT and THS_PREP_TIM_UI_CNT for dphy are programmed as prepare count by the processor

3.1.78 MIPIA_DBI_BW_CTRL_REG—Offset B084h

mipi A DBI BW ctrl register

Access Method

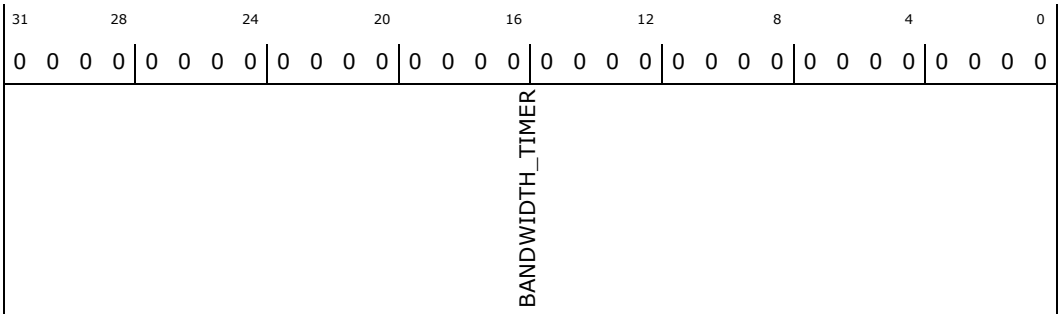
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DBI_BW_CTRL_REG: [GTTMMADR_LSB + 2BF20h] + B084h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**BANDWIDTH_TIMER:** DBI Bandwidth control Register. The bandwidth essential for transmitting 16 long packets containing 252 bytes meant for DCS write memory command is programmed in this register in terms of byte clocks. Based on the DSI transfer rate and the number of lanes configured the time taken to transmit 16 long packets in a DSI stream varies. Note: The value programmed in this timer must be greater than the actual time taken to carry out 16 long packets transmission in DSI stream plus the time taken to transmit two blanking packets

3.1.79 MIPIA_CLK_LANE_SWITCHING_TIME_CNT—Offset B088h

mipi A clk clane switching time counter

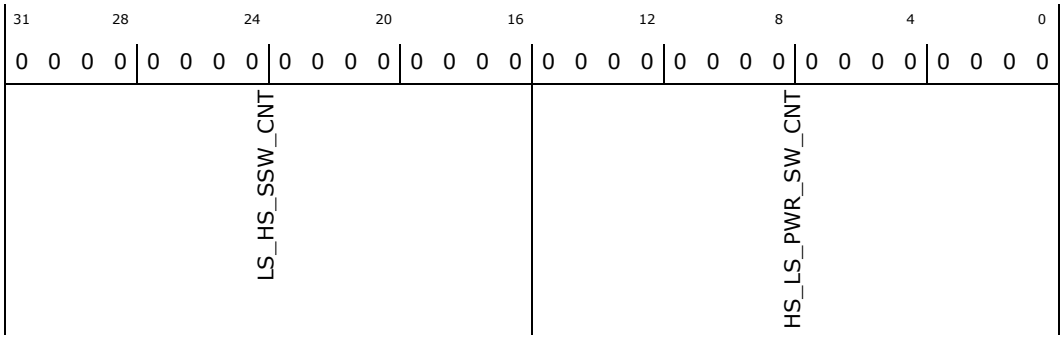
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_CLK_LANE_SWITCHING_TIME_CNT: [GTTMMADR_LSB + 2BF20h] + B088h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**LS_HS_SSW_CNT:** Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
15:0	0b RW	**HS_LS_PWR_SW_CNT:** High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs

3.1.80 MIPIA_STOP_STATE_STALL—Offset B08Ch

mipi A stop state stall

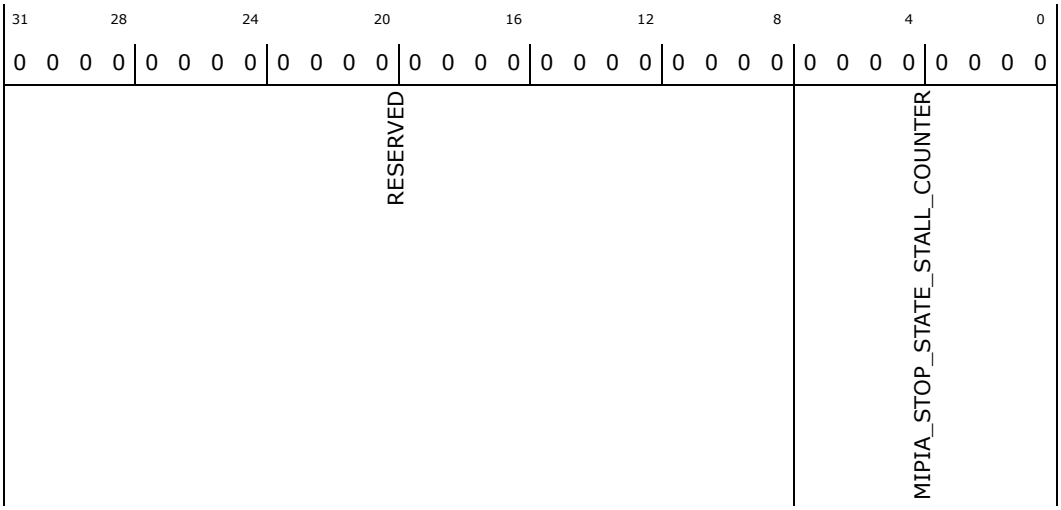
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_STOP_STATE_STALL: [GTTMMADR_LSB + 2BF20h] + B08Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**RESERVED:** reserved
7:0	0b RW	**MIPIA_STOP_STATE_STALL_COUNTER:** Delay between (stall the stop state signal) the data transfer is increased based on this counter value. This counter is calculated from txclkesc. Note: If processor programs this register then it needs to reprogram the high_low_ switch counter in B044h and lp_equivalent_byteclk reg in B060h to compensate this delay. High_low_switch_count B044h: High to low switch counter = Actual High to low switch + stop_sta_stall_reg value * Low power clock equivalence value in terms of byte clock LP equivalent byteclk register B060h: LP equivalent byteclk value = txclkesc time/ txbyteclk time * (105 + stop_sta_stall_reg value) / 105 Minimum time of Low Power short packet transfer = 105 txclkesc

3.1.81 MIPIA_INTR_STAT_REG_1—Offset B090h

mipi A interrupt state register 1

Access Method

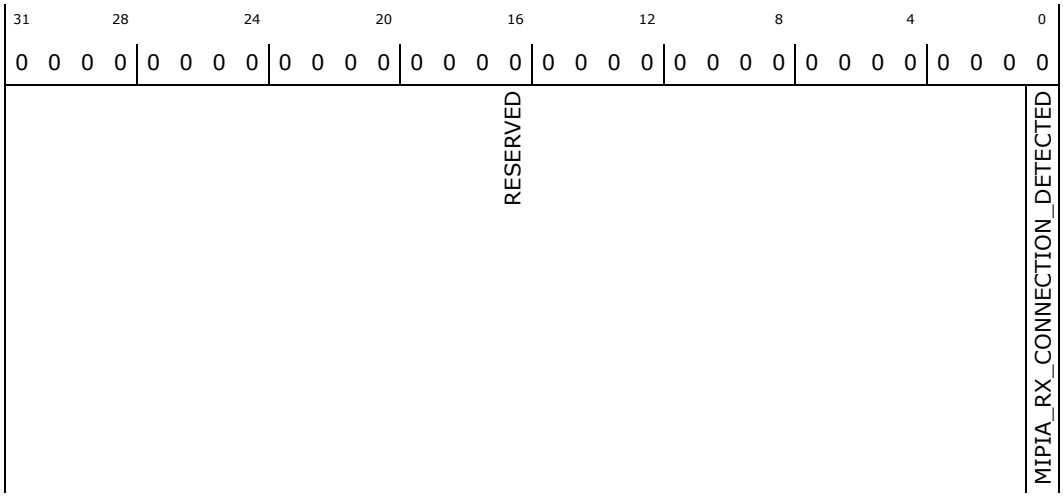
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_INTR_STAT_REG_1: [GTTMMADR_LSB + 2BF20h] + B090h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**RESERVED:** reserved
0	0b RW	**MIPIA_RX_CONNECTION_DETECTED:** Set to 1'b1 if the contention detected in the display device and is reported in the Acknowledge packet by the display device

3.1.82 MIPIA_INTR_EN_REG_1—Offset B094h

mipi A interrupt enable register 1

Access Method

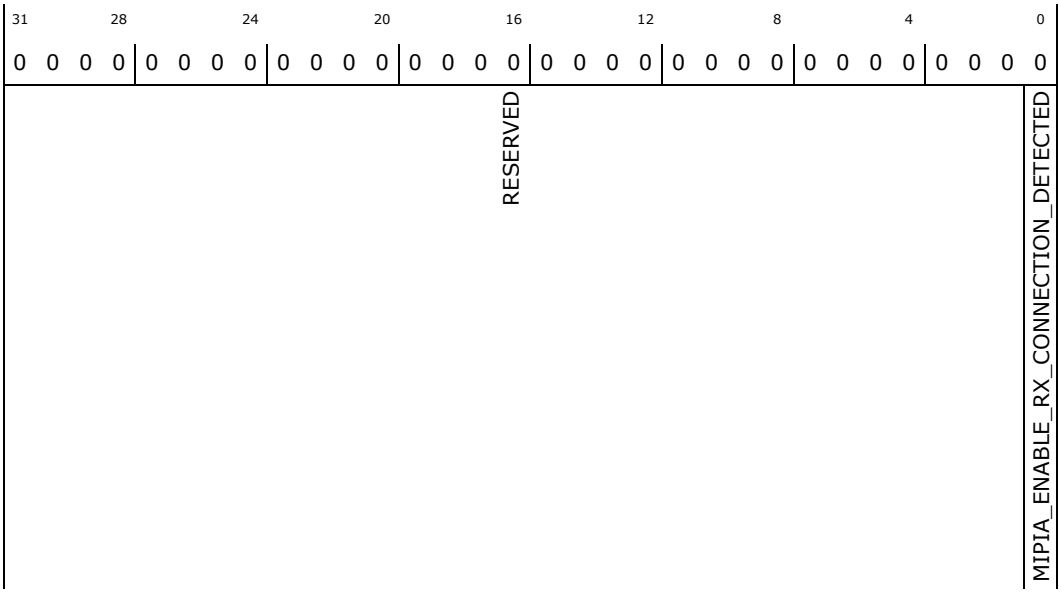
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_INTR_EN_REG_1: [GTTMMADR_LSB + 2BF20h] + B094h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**RESERVED:** reserved
0	0b RW	**MIPIA_ENABLE_RX_CONNECTION_DETECTED:** Set to enable the interrupt for contention detected error in the acknowledgement packet reports

3.1.83 MIPIA_DBI_TYPEC_CTRL—Offset B100h

mipi A Dbit typeC ctrl

Access Method

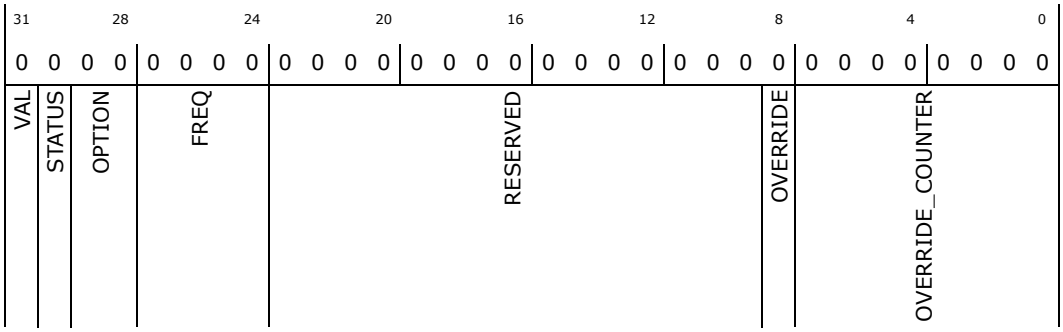
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DBI_TYPEC_CTRL: [GTTMMADR_LSB + 2BF20h] + B100h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**VAL:** 0= disable DBI TYPE-C interface (default) 1= enable DBI TYPE-C interface Driver to make sure that the command and data buffers are cleared before this bit is changed
30	0b RW	**STATUS:** command and data buffer empty and link completed sending out all serialized data and IDLE 0 = IDLE 1 = work in progress
29:28	0b RW	**OPTION:** TYPE-C option selection 00 option 1 01 option 2 10 option 3 11 no defined functionality
27:24	0b RW	**FREQ:** Type-C clock frequency ; A counter based onczclk is used to generate the TYPE-C Clock. So based on the czclk, a frequency close to the specified below will be generated. Not the exact frequency. (TBD we may just support a subset frequencies) 0000 1Mhz (default) 0001 1Mhz 0010 2Mhz 1111 15Mhz
23:9	0b RW	**RESERVED:** Reserved.
8	0b RW	**OVERRIDE:** Use override counter value to derive the TYPE-C clock frequency
7:0	0b RW	**OVERRIDE_COUNTER:** Override counter value to generate the TYPE-C clock

3.1.84 MIPIA_CTRL—Offset B104h

MIPI adapter has a control register with options to control width of the dbi bus and the divide value of the clock that needs to be supplied to the Clocks module so that a 2x divided clock can be provided to the MIPI D-PHY IP. Self refresh capability is in DCS commands. The other 3 controls bits (SD, CM and back light control) are now moved to MIPI IP registers.

Access Method

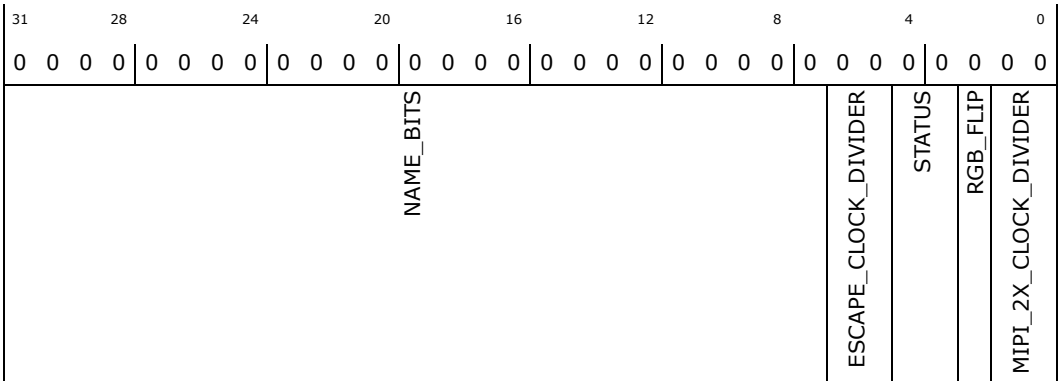
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_CTRL: [GTTMMADR_LSB + 2BF20h] + B104h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0b RW	**NAME_BITS:** Reserved
6:5	0b RW	**ESCAPE_CLOCK_DIVIDER:** Read Only Escape clock divider select for Pipe A and Pipe C Escape clock is shared by both Pipe A and Pipe C so it cant be set different. 00= 1 X (20 Mhz) (default) 01= X (10Mhz) 10= X (5Mhz) Changing this register can only be done when the MIPI device_ready is turned OFF
4:3	0b RW	**STATUS:** 2'b00: low priority on read requests to G-unit 2'b11 : high priority
2	0b RW	**RGB_FLIP:** 1'b0 : RGB data from disp2d is reverted to BGR 1'b1 : RGB data from disp2d is passed as is to MIPI IP
1:0	0b RW	**MIPI_2X_CLOCK_DIVIDER:** Reserved

3.1.85 MIPIA_DATA_ADD—Offset B108h

mipi A data ADD

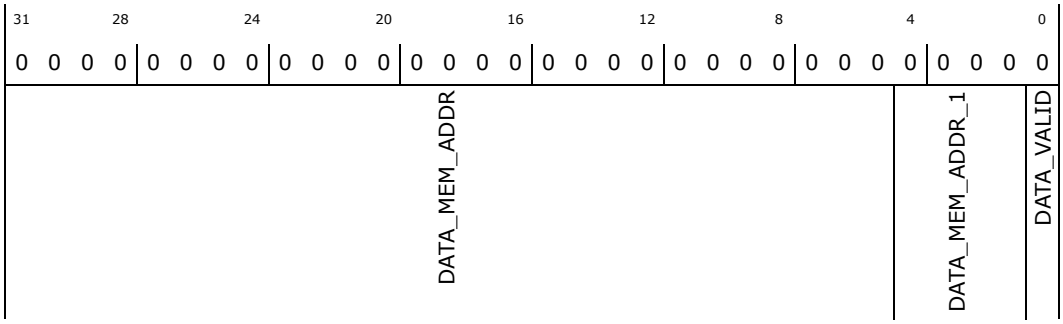
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DATA_ADD: [GTTMMADR_LSB + 2BF20h] + B108h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RW	**DATA_MEM_ADDR:** When there is updated data for the display panel, S/W programs this register with the memory address to read from
4:1	0b RW	**DATA_MEM_ADDR_1:** Reserved
0	0b RW	**DATA_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.1.86 MIPIA_DATA_LEN—Offset B10Ch

mipiA data length

Access Method

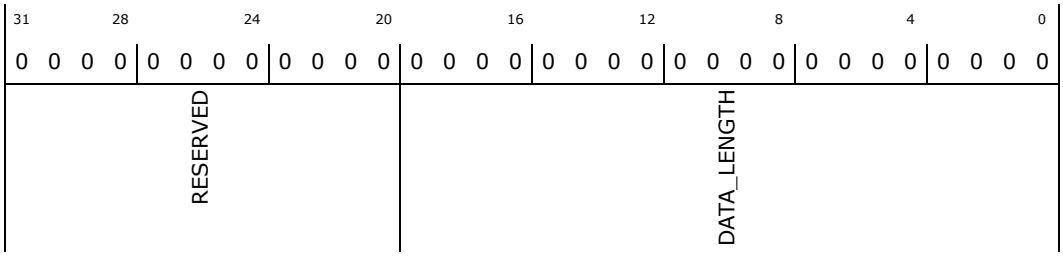
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_DATA_LEN: [GTTMMADR_LSB + 2BF20h] + B10Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**DATA_LENGTH:** This field shows the remaining length of data that needs to be read from memory, Initially set by S/W and is decremented by H/W as reads are issued

3.1.87 MIPIA_CMD_ADD—Offset B110h

mipi A cmd ADD

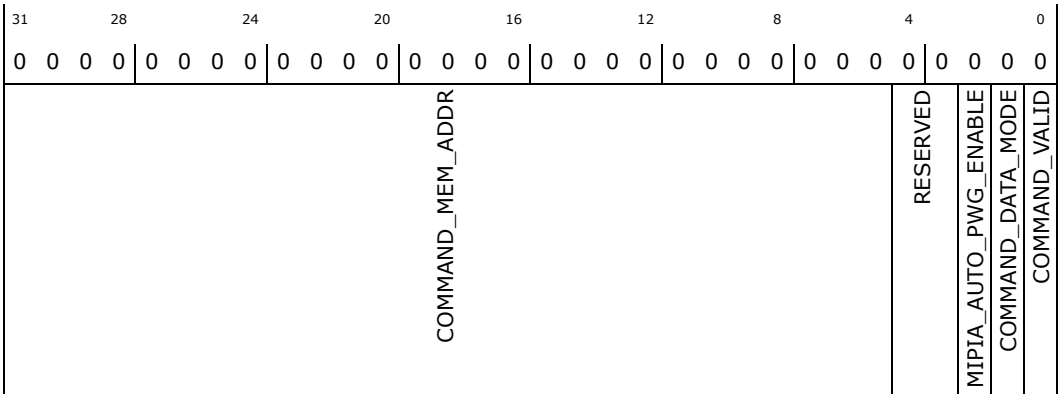
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_CMD_ADD: [GTTMMADR_LSB + 2BF20h] + B110h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RW	**COMMAND_MEM_ADDR:** When there are new commands that need to be sent to the display panel, S/W programs this register with the memory address to read the commands from
4:3	0b RW	**RESERVED:** MBZ
2	0b RW	**MIPIA_AUTO_PWG_ENABLE:** Idle state: SW driver writes to this bit to enable auto power gating for MIPIA controller 0: default 1: auto power gate is enabled
1	0b RW	**COMMAND_DATA_MODE:** 0: data for memory write command from system buffer that is specified by MIPI data address register 1: data for memory write command from pipe A rendering
0	0b RW	**COMMAND_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.1.88 MIPIA_CMD_LEN—Offset B114h

mipi A clm length

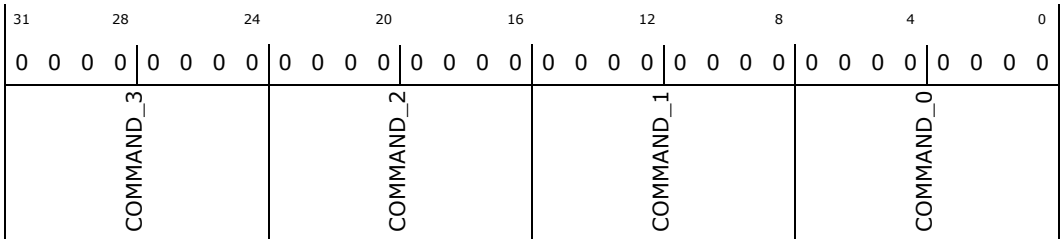
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_CMD_LEN: [GTTMMADR_LSB + 2BF20h] + B114h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**COMMAND_3:** This is command 3 length (command + parameters) in bytes
23:16	0b RW	**COMMAND_2:** This is command 2 length (command + parameters) in bytes
15:8	0b RW	**COMMAND_1:** This is command 1 length (command + parameters) in bytes
7:0	0b RW	**COMMAND_0:** This is command 0 length (command + parameters) in bytes

3.1.89 MIPIA_RD_DATA_RETURN0—Offset B118h

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes.

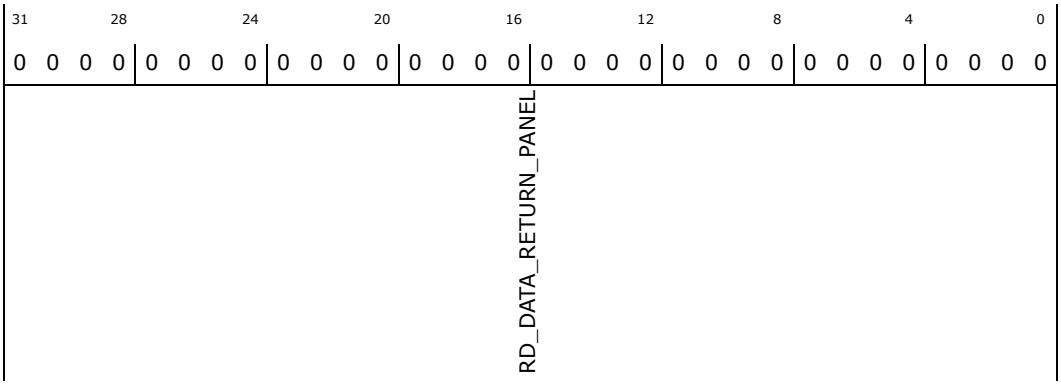
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_RD_DATA_RETURN0: [GTTMMADR_LSB + 2BF20h] + B118h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.90 MIPIA_RD_DATA_RETURN1—Offset B11Ch

Refer to the description of MIPIA_RD_DATA_RETURN0.

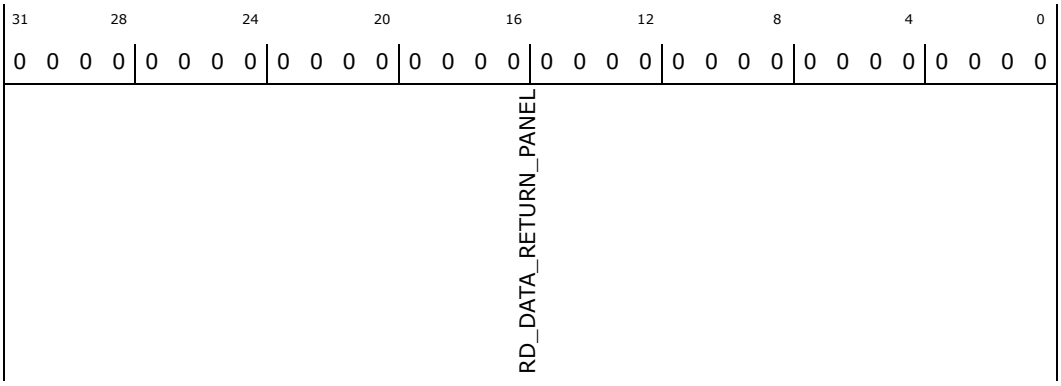
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_RD_DATA_RETURN1: [GTTMMADR_LSB + 2BF20h] + B11Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.91 MIPIA_RD_DATA_RETURN2—Offset B120h

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

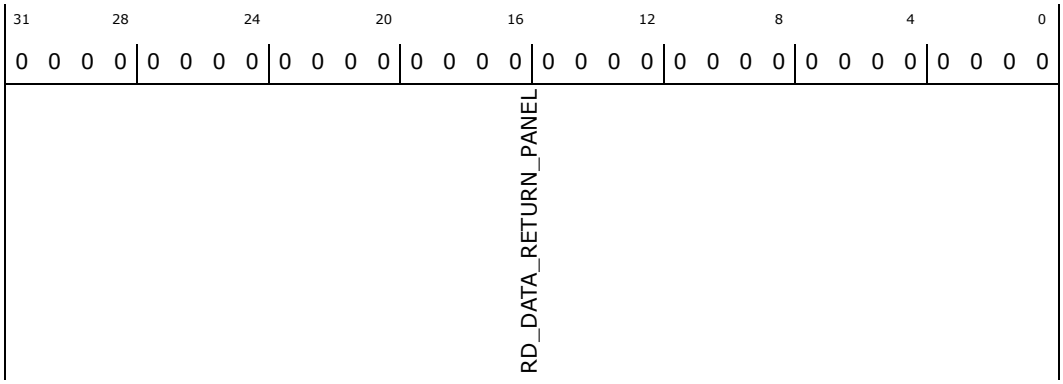
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_RD_DATA_RETURN2: [GTTMMADR_LSB + 2BF20h] + B120h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.92 MIPIA_RD_DATA_RETURN3—Offset B124h

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

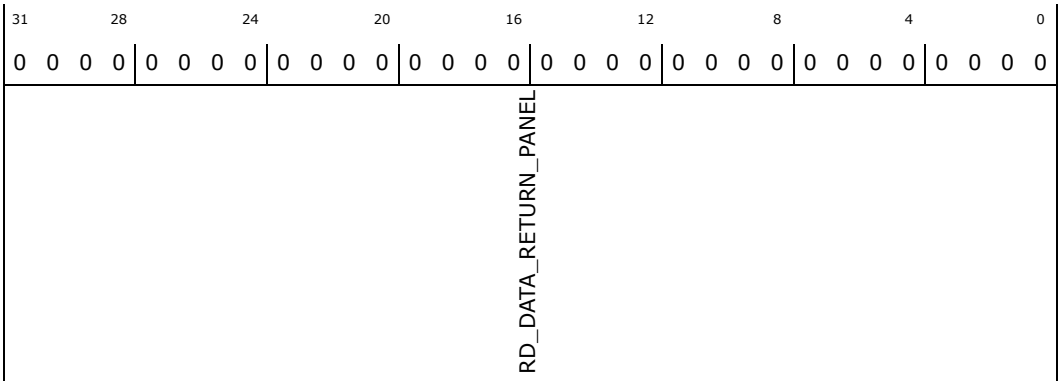
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_RD_DATA_RETURN3: [GTTMMADR_LSB + 2BF20h] + B124h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.93 MIPIA_RD_DATA_RETURN4—Offset B128h

Refer to the description of MIPIA_RD_DATA_RETURN0.

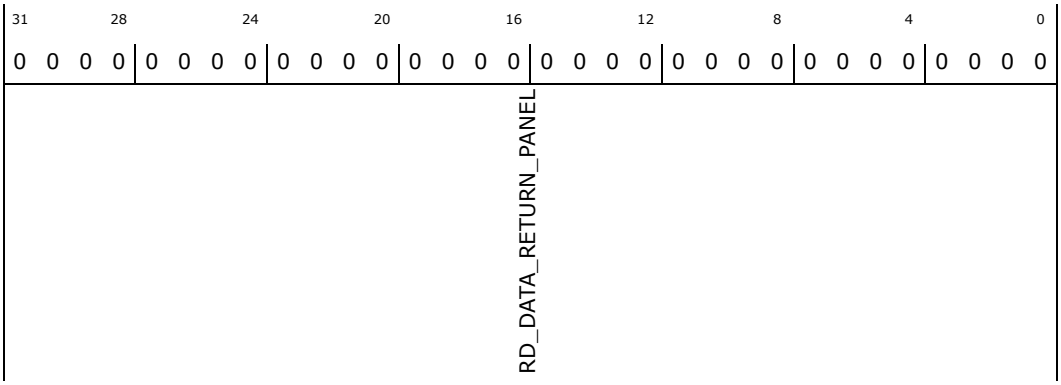
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_RD_DATA_RETURN4: [GTTMMADR_LSB + 2BF20h] + B128h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.94 MIPIA_RD_DATA_RETURN5—Offset B12Ch

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

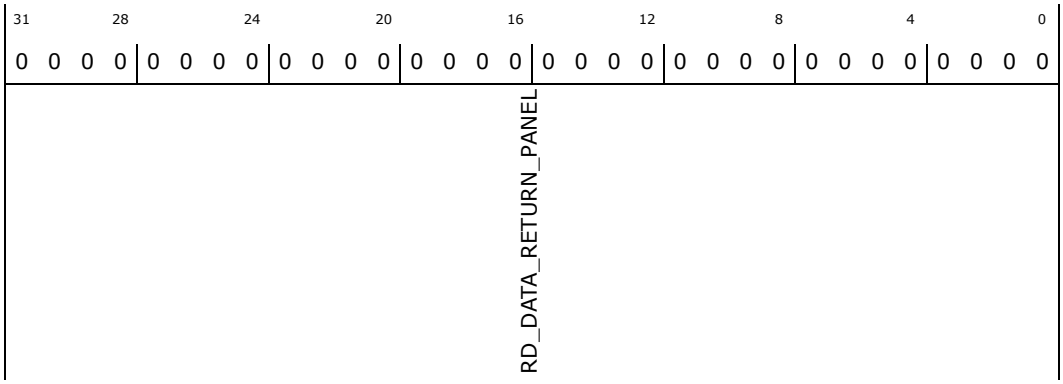
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_RD_DATA_RETURN5: [GTTMMADR_LSB + 2BF20h] + B12Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.95 MIPIA_RD_DATA_RETURN6—Offset B130h

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

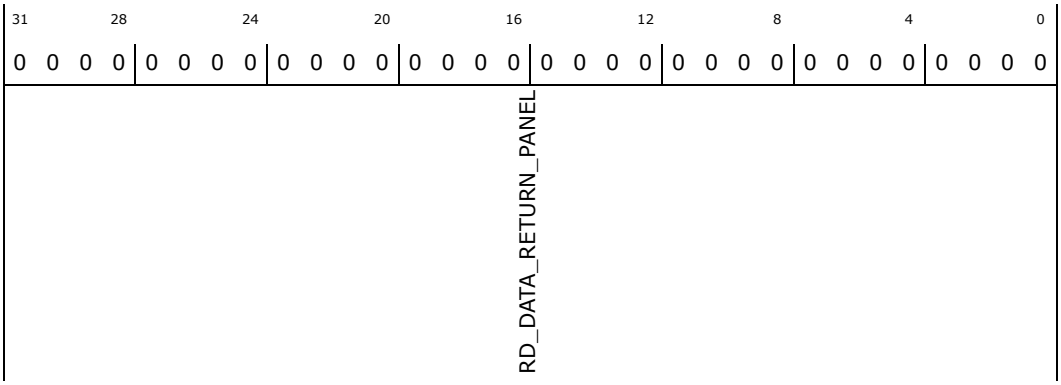
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_RD_DATA_RETURN6: [GTTMMADR_LSB + 2BF20h] + B130h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.96 MIPIA_RD_DATA_RETURN7—Offset B134h

Refer to the description of MIPIA_RD_DATA_RETURN0.

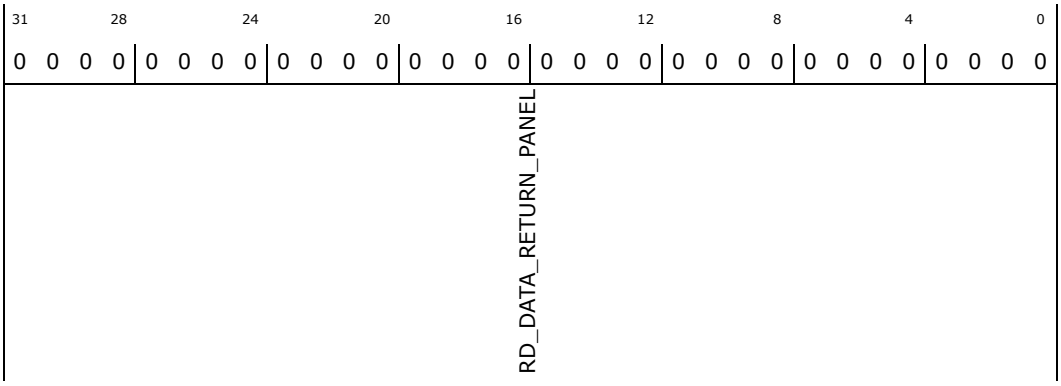
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_RD_DATA_RETURN7: [GTTMMADR_LSB + 2BF20h] + B134h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.97 MIPIA_RD_DATA_VALID—Offset B138h

Refer to the description of MIPIA_RD_DATA_RETURN1.

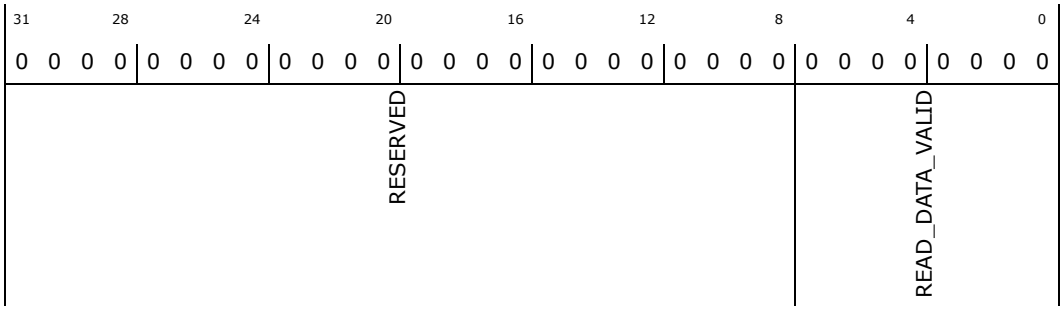
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_RD_DATA_VALID: [GTTMMADR_LSB + 2BF20h] + B138h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**RESERVED:** Reserved.
7:0	0b RW	**READ_DATA_VALID:** Each bit corresponds to presence of valid data in the registers above. When data is returned from the panel, H/W will write into these registers in sequence, and set the corresponding valid bit. When S/W issues a write '1 to the registers, this bit is cleared

3.1.98 MIPIC_DEVICE_READY_REG—Offset B800h

MIPI C Device Ready Register

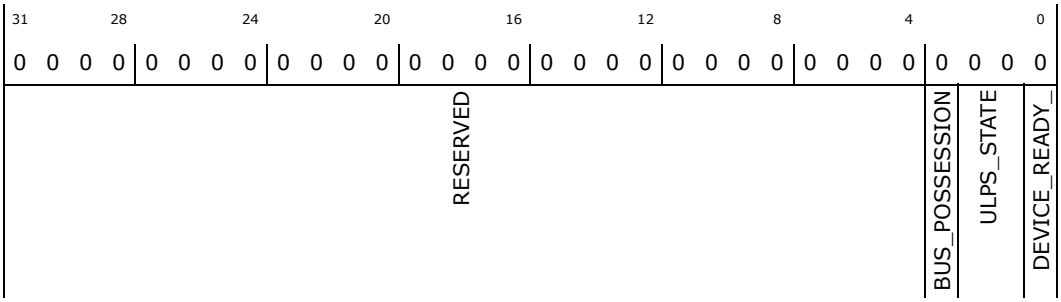
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DEVICE_READY_REG: [GTTMMADR_LSB + 2BF20h] + B800h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0b RW	**RESERVED:** Reserved.
3	0b RW	**BUS_POSSESSION:** mipi C Bus Possession
2:1	0b RW	**ULPS_STATE:** mipi C ULPS state
0	0b RW	**DEVICE_READY_:** Set by the processor to inform that device is ready

3.1.99 MIPIC_INTR_STAT_REG—Offset B804h

mipi C interrupt state register

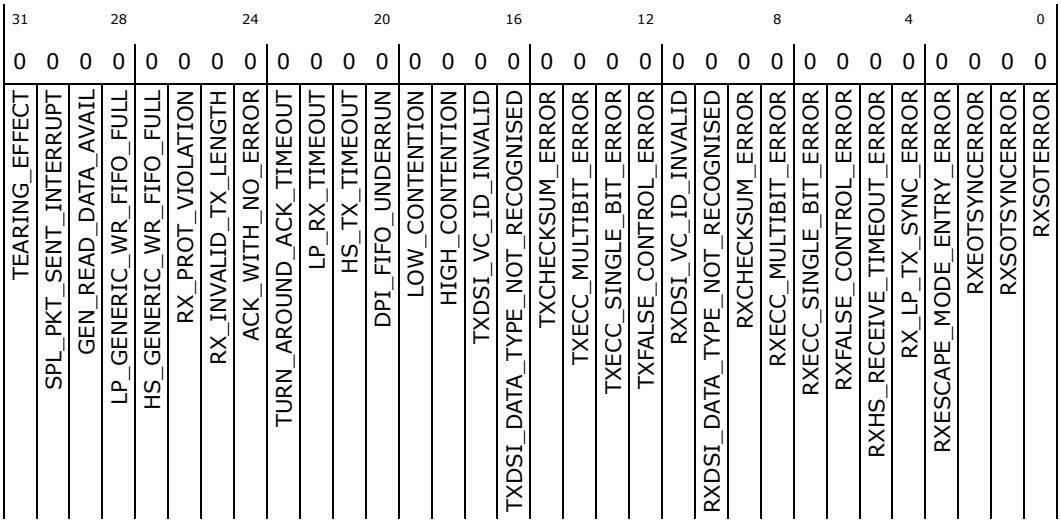
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_INTR_STAT_REG: [GTTMMADR_LSB + 2BF20h] + B804h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**TEARING_EFFECT:** Set to indicate that tearing effect trigger message is received
30	0b RW	**SPL_PKT_SENT_INTERRUPT:** Set to confirm the transmission of the DPI event specific commands set in the dpi control and dpi data register
29	0b RW	**GEN_READ_DATA_AVAIL:** Set to indicate that the requested data for a Generic Read request is available in the buffer i.e., generic read response data is available in the read FIFO
28	0b RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full
27	0b RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0b RW	**RX_PROT_VIOLATION:** Set if DSI protocol violation error is reported in the acknowledge packet by the display device
25	0b RW	**RX_INVALID_TX_LENGTH:** Set if invalid transmission length error is reported in the acknowledge packet by the display device
24	0b RW	**ACK_WITH_NO_ERROR:** Set if acknowledge trigger message is received with out any error
23	0b RW	**TURN_AROUND_ACK_TIMEOUT:** Set if a turn around acknowledgement sequence is not received from the display device
22	0b RW	**LP_RX_TIMEOUT:** Set if a low power reception count expires this interrupt is generated
21	0b RW	**HS_TX_TIMEOUT:** Set if a high speed transmission prevails for more than the expected count value this interrupt is raised
20	0b RW	**DPI_FIFO_UNDERRUN:** Set to '1' if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0b RW	**LOW_CONTENTION:** Set to '1' if a LP low fault is registered by at the D-PHY contention detector
18	0b RW	**HIGH_CONTENTION:** Set to '1' if a LP high fault is registered by at the D-PHY contention detector
17	0b RW	**TXDSI_VC_ID_INVALID:** Set to '1' if the received virtual channel ID is invalid
16	0b RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the received data type is not recognized
15	0b RW	**TXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value during the reception of packets by Arasan_DSI host.
14	0b RW	**TXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan_DSI_host
13	0b RW	**TXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan_DSI_host
12	0b RW	**TXFALSE_CONTROL_ERROR:** Set to '1' if a control error is observed on the lanes by the Arasan_DSI_host

Bit Range	Default & Access	Description
11	0b RW	**RXDSI_VC_ID_INVALID:** Set to '1' if the virtual channel ID is invalid by the display device is reported in the Acknowledge packet by the display device
10	0b RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the data type is not recognized by the display device is reported in the Acknowledge packet by the display device
9	0b RW	**RXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value and is reported in the Acknowledge packet by the display device
8	0b RW	**RXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet is reported in the Acknowledge packet by the display device
7	0b RW	**RXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and corrected for one bit error is reported in the Acknowledge packet by the display device
6	0b RW	**RXFALSE_CONTROL_ERROR:** Set to '1' if a control error is reported in the Acknowledge packet by the display device
5	0b RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to '1' if the high speed receive timer value expires and data transfer lasts on the data lane is reported in the Acknowledge packet by the display device
4	0b RW	**RX_LP_TX_SYNC_ERROR:** Set to '1' if Low power transmission sync error occurs in the display device and is reported in the Acknowledge packet by the display device
3	0b RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to '1' if Escape Mode Entry command is not understandable by the display device and is reported in the Acknowledge packet by the display device
2	0b RW	**RXEOTSYNCERROR:** mipi C RX eot sync error
1	0b RW	**RXSOTSYNCERROR:** Set to '1' if a start of transmission synchronisation error is reported in the Acknowledge packet by the display device
0	0b RW	**RXSOTERROR:** Set to '1' if a start of transmission error is reported in the Acknowledge packet by the display device

3.1.100 MIPIC_INTR_EN_REG—Offset B808h

mipi C interrupt En reg

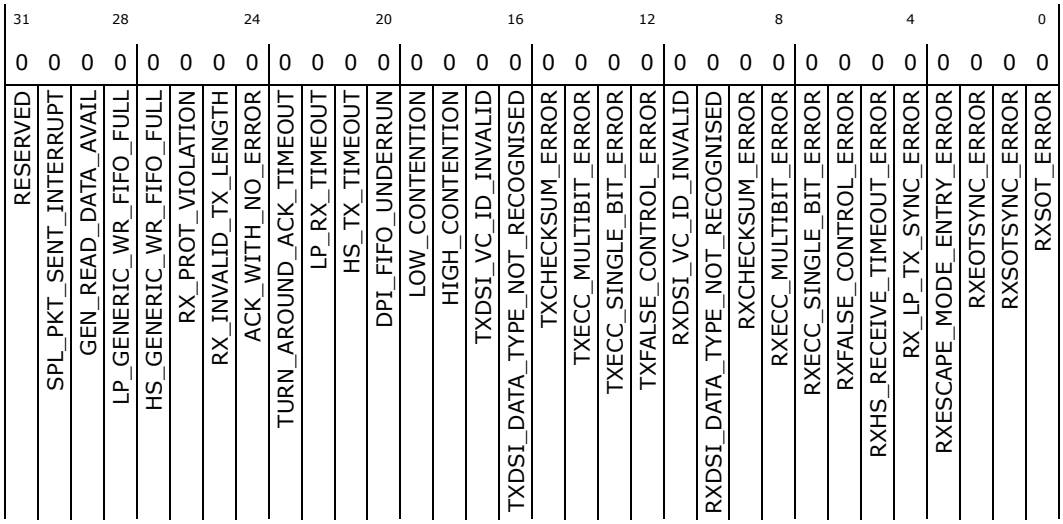
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

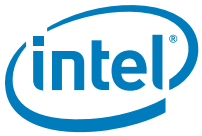
MIPIC_INTR_EN_REG: [GTTMMADR_LSB + 2BF20h] + B808h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**TEARING_EFFECT (RESERVED):** Set to enable tearing effect
30	0b RW	**SPL_PKT_SENT_INTERRUPT:** Set to enable the confirmation of transmission of the DPI event specific commands set in the dpi control and dpi data register
29	0b RW	**GEN_READ_DATA_AVAIL:** Set to enable Generic Read available interrupt
28	0b RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full
27	0b RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0b RW	**RX_PROT_VIOLATION:** Set to enable protocol violation error
25	0b RW	**RX_INVALID_TX_LENGTH:** Set to enable invalid transmission length error
24	0b RW	**ACK_WITH_NO_ERROR:** Set to enable acknowledge trigger message reception with out any error
23	0b RW	**TURN_AROUND_ACK_TIMEOUT:** Set to enable turn around acknowledgement ,sequence timeout
22	0b RW	**LP_RX_TIMEOUT:** Set to enable low power reception count time outs
21	0b RW	**HS_TX_TIMEOUT:** Set to enable a high speed transmission timeout
20	0b RW	**DPI_FIFO_UNDERRUN:** Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0b RW	**LOW_CONTENTION:** Set to enable a LP low fault interrupt
18	0b RW	**HIGH_CONTENTION:** Set to enable a LP high fault interrupt



Bit Range	Default & Access	Description
17	0b RW	**TXDSI_VC_ID_INVALID:** Set to enable the interrupt if the received packets virtual channel ID is invalid
16	0b RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt if the received packets data type is not recognized
15	0b RW	**TXCHECKSUM_ERROR:** Set to enable the interrupt if the computed CRC differs from the received CRC value for the received packets
14	0b RW	**TXECC_MULTIBIT_ERROR:** Set to enable the interrupt if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan DSI host
13	0b RW	**TXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan DSIhost
12	0b RW	**TXFALSE_CONTROL_ERROR:** Set to enable the interrupt for the control error.,observed on the lanes by the Arasan_DSI_host
11	0b RW	**RXDSI_VC_ID_INVALID:** Set to enable the interrupt for invalid virtual channel ID in the acknowledgment packet reports
10	0b RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt for the un recognized data type in the acknowledgment packet reports
9	0b RW	**RXCHECKSUM_ERROR:** Set to enable the interrupt for the computed CRC differs from the received CRC value in the acknowledgment packet reports
8	0b RW	**RXECC_MULTIBIT_ERROR:** Set to enable the interrupt for no ECC correction for the packet or there are more than 2 bit errors reported in the acknowledgment packet
7	0b RW	**RXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt for ECC syndrome computation and one bit error correction for the acknowledgment packet
6	0b RW	**RXFALSE_CONTROL_ERROR:** Set to enable the interrupt for control error in the acknowledgment packet reports
5	0b RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to enable the interrupt for the high speed receive timeout Error in the acknowledgment packet reports
4	0b RW	**RX_LP_TX_SYNC_ERROR:** Set to enable the interrupt for Low power transmission sync error in the acknowledgment packet reports
3	0b RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to enable the interrupt for Escape Mode Entry command error in the acknowledgment packet reports
2	0b RW	**RXEOTSYNC_ERROR:** Set to enable the interrupt for End of transmission synchronisation Error in the acknowledgement packet reports
1	0b RW	**RXSOTSYNC_ERROR:** Set to enable the interrupt for start of transmission synchronisation error in the acknowledgement packet reports
0	0b RW	**RXSOT_ERROR:** Set to enable the interrupt for start of transmission error in the acknowledgment packet reports

3.1.101 MIPIC_DSI_FUNC_PRG__REG—Offset B80Ch

mipi C DSI func prg reg

Access Method

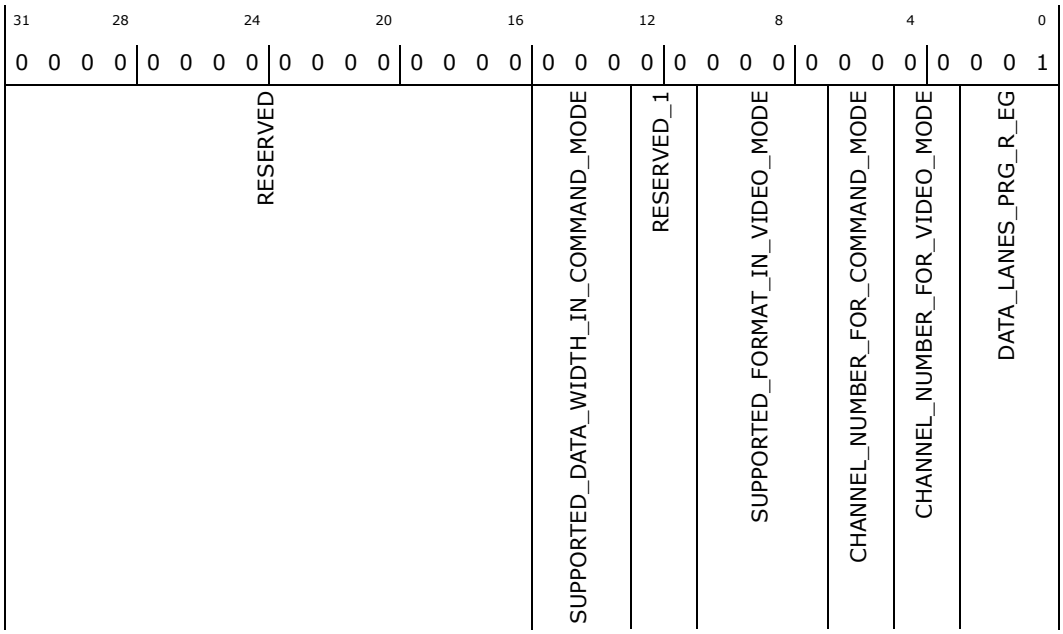
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DSI_FUNC_PRG__REG: [GTTMMADR_LSB + 2BF20h] + B80Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:13	0b RW	**SUPPORTED_DATA_WIDTH_IN_COMMAND_MODE:** 000 --) Reserved, 001 --) 16 bit data , 010 --) 9 bit data , 011 --) 8 bit data , 100 --) option 1 : 101 --) option 2 : 110 to 111 --) Reserved
12:11	0b RW	**RESERVED_1:** Reserved.
10:7	0b RW	**SUPPORTED_FORMAT_IN_VIDEO_MODE:** Supported color format, 0001 --) RGB565, 0010 --) RGB666, 0011 --) RGB 666 loosely packed format, 0100 --) RGB888
6:5	0b RW	**CHANNEL_NUMBER_FOR_COMMAND_MODE:** Virtual channel number for command mode is programmed by the processor
4:3	0b RW	**CHANNEL_NUMBER_FOR_VIDEO_MODE:** Virtual channel number for command mode is programmed by the processor
2:0	001b RW	**DATA_LANES_PRG_R_EG:** Number of data lanes to be supported is programmed by the processor

3.1.102 MIPIC_HS_TX_TIMEOUT_REG—Offset B810h

mipi C HS TX timeout reg

Access Method

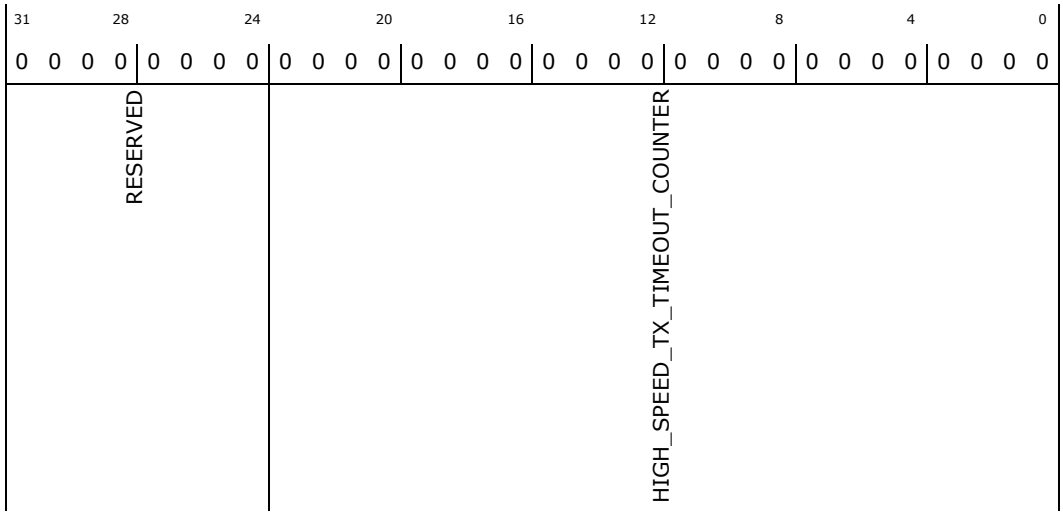
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_HS_TX_TIMEOUT_REG: [GTTMMADR_LSB + 2BF20h] + B810h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:0	0b RW	**HIGH_SPEED_TX_TIMEOUT_COUNTER:** The maximum duration allowed for the DSI host ,to remain in high speed mode for a transmission. If the counter expires, HS mode is terminated with EOT and the lanes enter stop state

3.1.103 MIPIC_LP_RX_TIMEOUT_REG—Offset B814h

mipi C LP RX timeout reg

Access Method

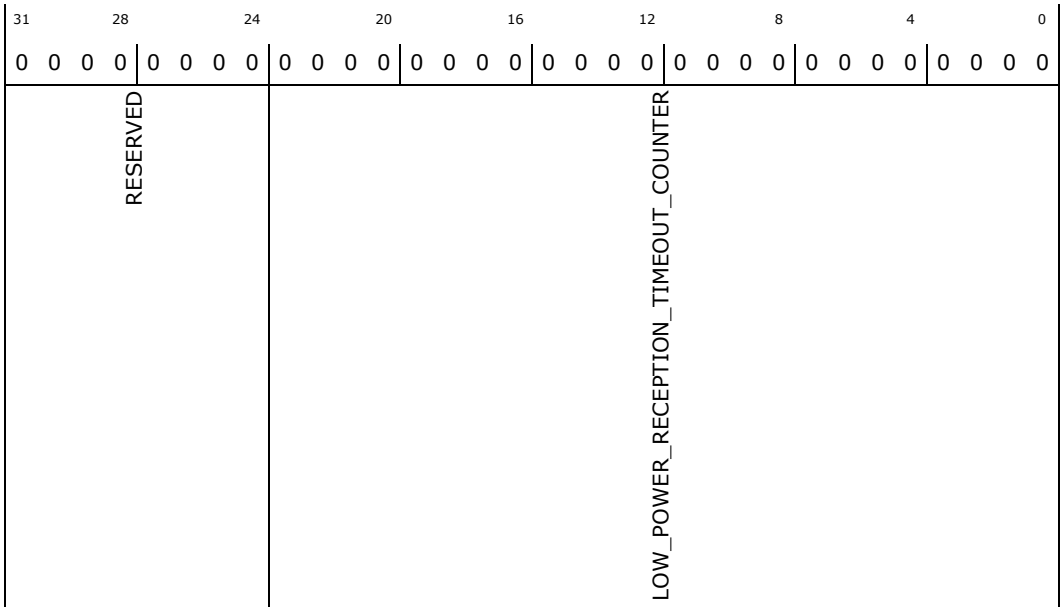
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_LP_RX_TIMEOUT_REG: [GTTMMADR_LSB + 2BF20h] + B814h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:0	0b RW	**LOW_POWER_RECEPTION_TIMEOUT_COUNTER:** Timeout value to be checked for received short packets .If the timer expires the DSI Host enters stop state

3.1.104 MIPIC_TURN_AROUND_TIMEOUT_REG—Offset B818h

mipi C Turn Around timeout reg

Access Method

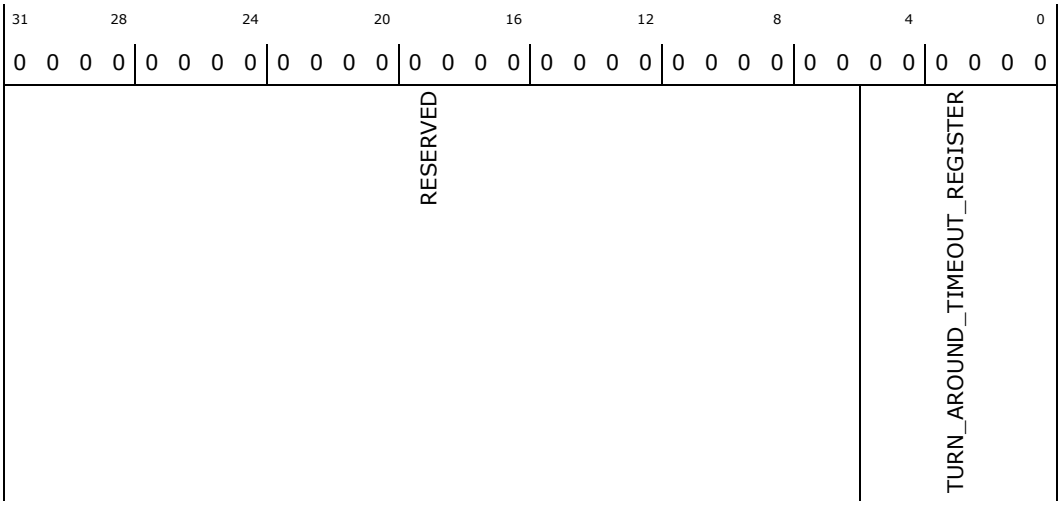
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_TURN_AROUND_TIMEOUT_REG: [GTTMMADR_LSB + 2BF20h] + B818h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**RESERVED:** Reserved.
5:0	0b RW	**TURN_AROUND_TIMEOUT_REGISTER:** Timeout value to be checked after the DSI host makes a turn around in the direction of transfers. If the timer expires the DSI Host enters stop state

3.1.105 MIPIC_DEVICE_RESET_TIMER—Offset B81Ch

mipi C Device reset timer

Access Method

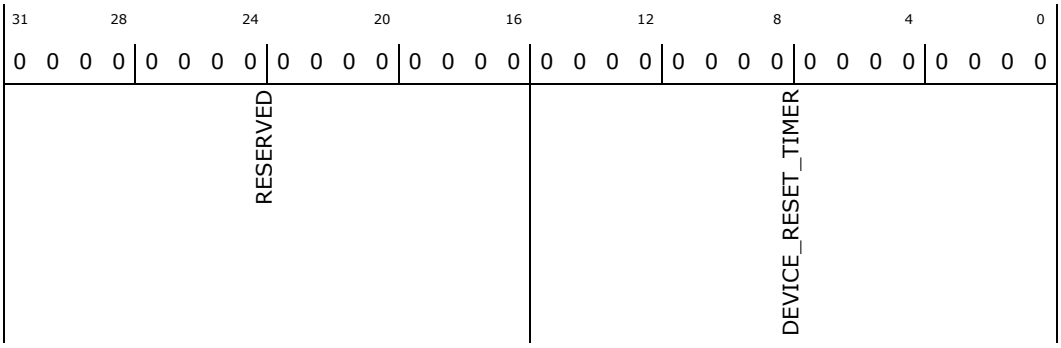
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DEVICE_RESET_TIMER: [GTTMMADR_LSB + 2BF20h] + B81Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**DEVICE_RESET_TIMER:** Timeout value to be checked for device to be reset after issuing reset entry command. If the timer expires the DSI Host enters normal operation

3.1.106 MIPIC_DPI_RESOLUTION_REG—Offset B820h

mipi C dpi Resolution reg

Access Method

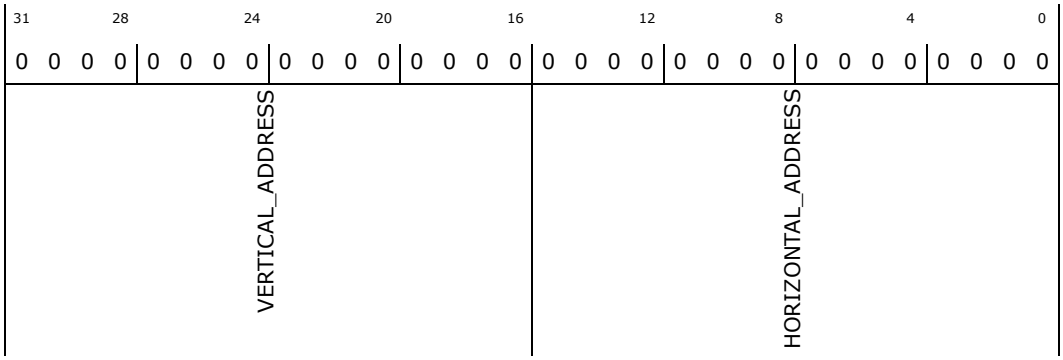
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DPI_RESOLUTION_REG: [GTTMMADR_LSB + 2BF20h] + B820h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**VERTICAL_ADDRESS:** Shows the vertical address count in lines
15:0	0b RW	**HORIZONTAL_ADDRESS:** Shows the horizontal address count in pixels

3.1.107 MIPIC_DBI_RESOLUTION_REG—Offset B824h

mipi C DBI resolution reg

Access Method

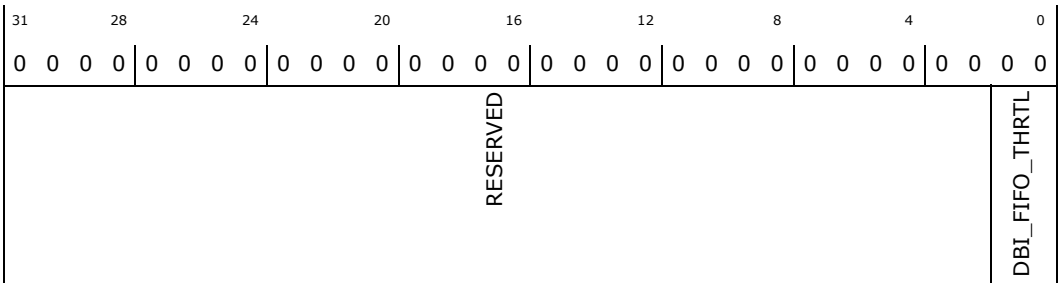
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DBI_RESOLUTION_REG: [GTTMMADR_LSB + 2BF20h] + B824h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**RESERVED:** Reserved.
1:0	0b RW	**DBI_FIFO_THRTL:** DBI FIFO's watermark can be set using the following bits so as to enable dbi_stall de-assertion whenever the below FIFO condition is reached: 00 - (1/2) DBI fifo empty 01 - (1/4) DBI fifo empty 10 - 7 locations are empty 11 - Reserved

3.1.108 MIPIC_HORIZ_SYNC_PADDING_COUNT—Offset B828h

mipi C horizontal sync padding out

Access Method

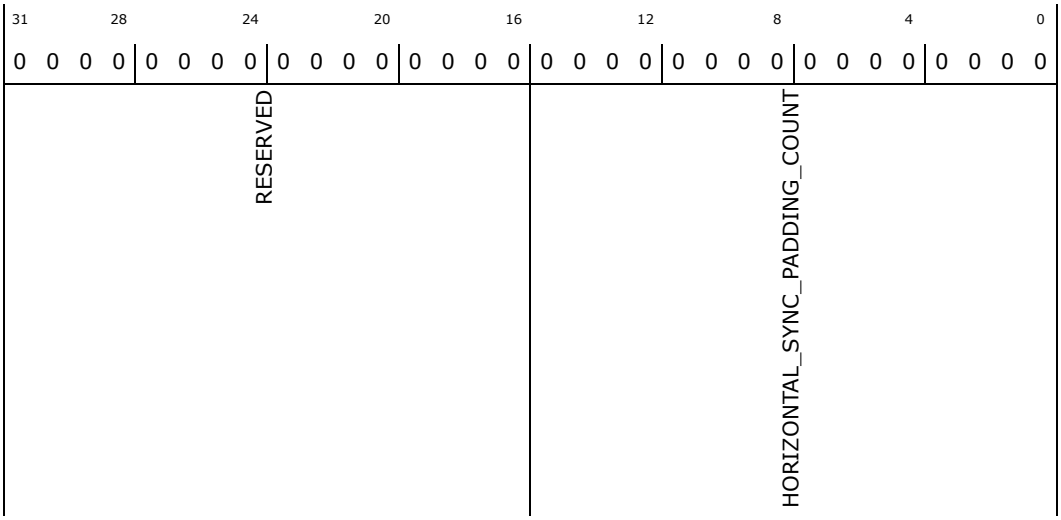
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_HORIZ_SYNC_PADDING_COUNT: [GTTMMADR_LSB + 2BF20h] + B828h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_SYNC_PADDING_COUNT:** Shows the horizontal sync padding value in terms of txbyteclkhs

3.1.109 MIPIC_HORIZ_BACK_PORCH_COUNT—Offset B82Ch

mipi C horizontal back portch counter

Access Method

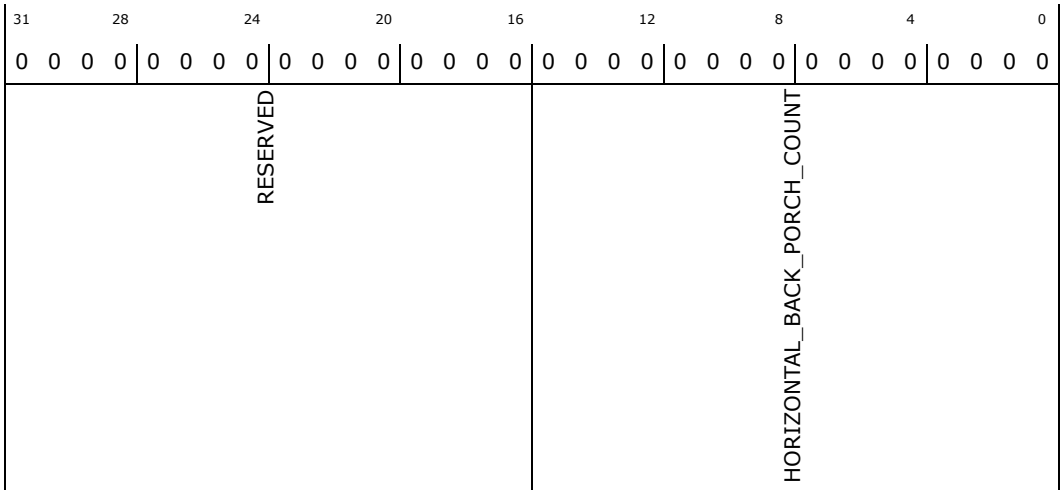
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_HORIZ_BACK_PORCH_COUNT: [GTTMMADR_LSB + 2BF20h] + B82Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_BACK_PORCH_COUNT:** Shows the horizontal back porch value in terms of txbyteclkhs

3.1.110 MIPIC_HORIZ_FRONT_PORCH_COUNT—Offset B830h

mipi C horizontal front Porch counter

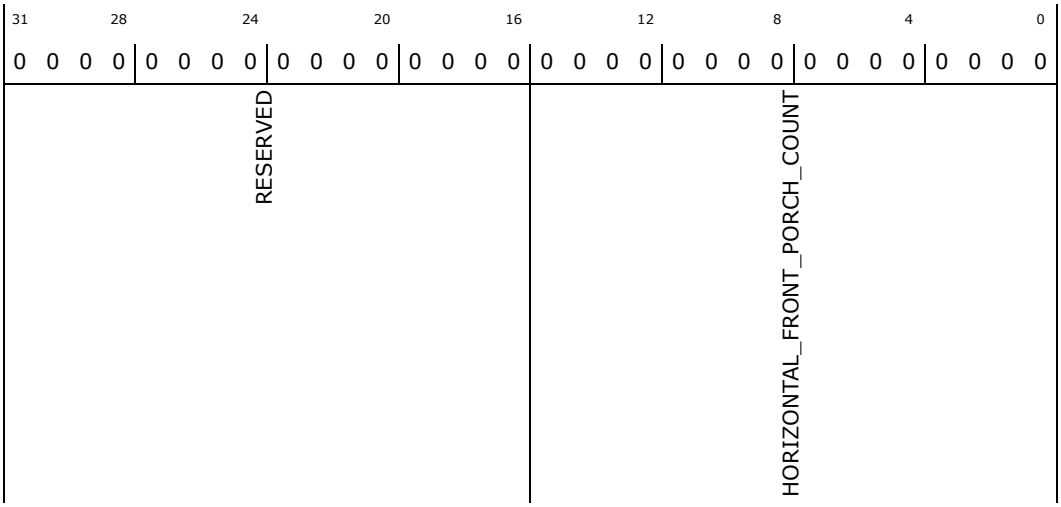
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_HORIZ_FRONT_PORCH_COUNT: [GTTMMADR_LSB + 2BF20h] + B830h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_FRONT_PORCH_COUNT:** Shows the horizontal front porch value in terms of txbyteclkhs

3.1.111 MIPIC_HORIZ_ACTIVE_AREA_COUNT—Offset B834h

mipi C horizontal active area count

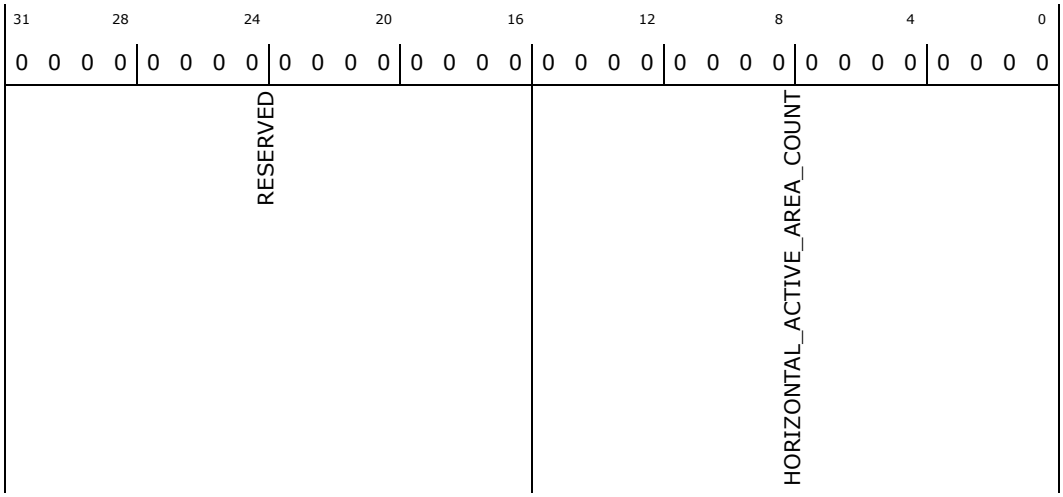
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_HORIZ_ACTIVE_AREA_COUNT: [GTTMMADR_LSB + 2BF20h] + B834h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_ACTIVE_AREA_COUNT:** Shows the horizontal active area value in terms of txbyteclkhs

3.1.112 MIPIC_VERT_SYNC_PADDING_COUNT—Offset B838h

mipi C vertical sync padding count

Access Method

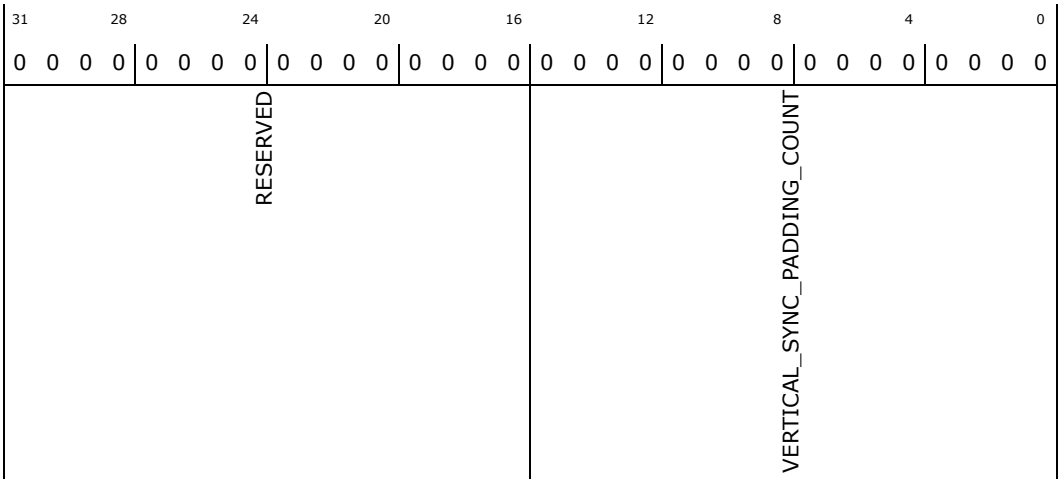
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_VERT_SYNC_PADDING_COUNT: [GTTMMADR_LSB + 2BF20h] + B838h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_SYNC_PADDING_COUNT:** Shows the vertical sync padding value in terms of lines

3.1.113 MIPIC_VERT_BACK_PORCH_COUNT—Offset B83Ch

mipic Vertical back porch count

Access Method

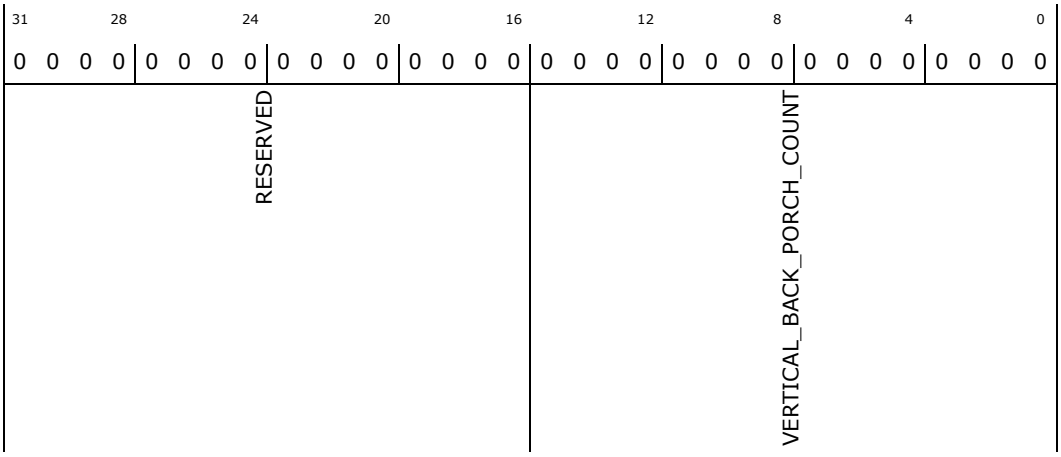
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_VERT_BACK_PORCH_COUNT: [GTTMMADR_LSB + 2BF20h] + B83Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_BACK_PORCH_COUNT:** Shows the vertical back porch value in terms of lines

3.1.114 MIPIC_VERT_FRONT_PORCH_COUNT—Offset B840h

mipi C vertical front porch count

Access Method

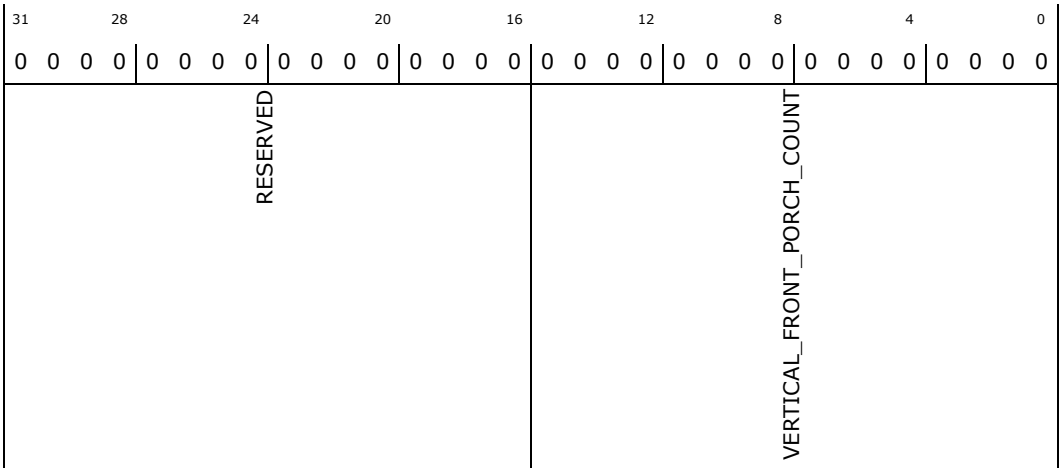
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_VERT_FRONT_PORCH_COUNT: [GTTMMADR_LSB + 2BF20h] + B840h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_FRONT_PORCH_COUNT:** Shows the vertical front porch value in terms of lines

3.1.115 MIPIC_HIGH_LOW_SWITCH_COUNT—Offset B844h

mipi C high low switch count

Access Method

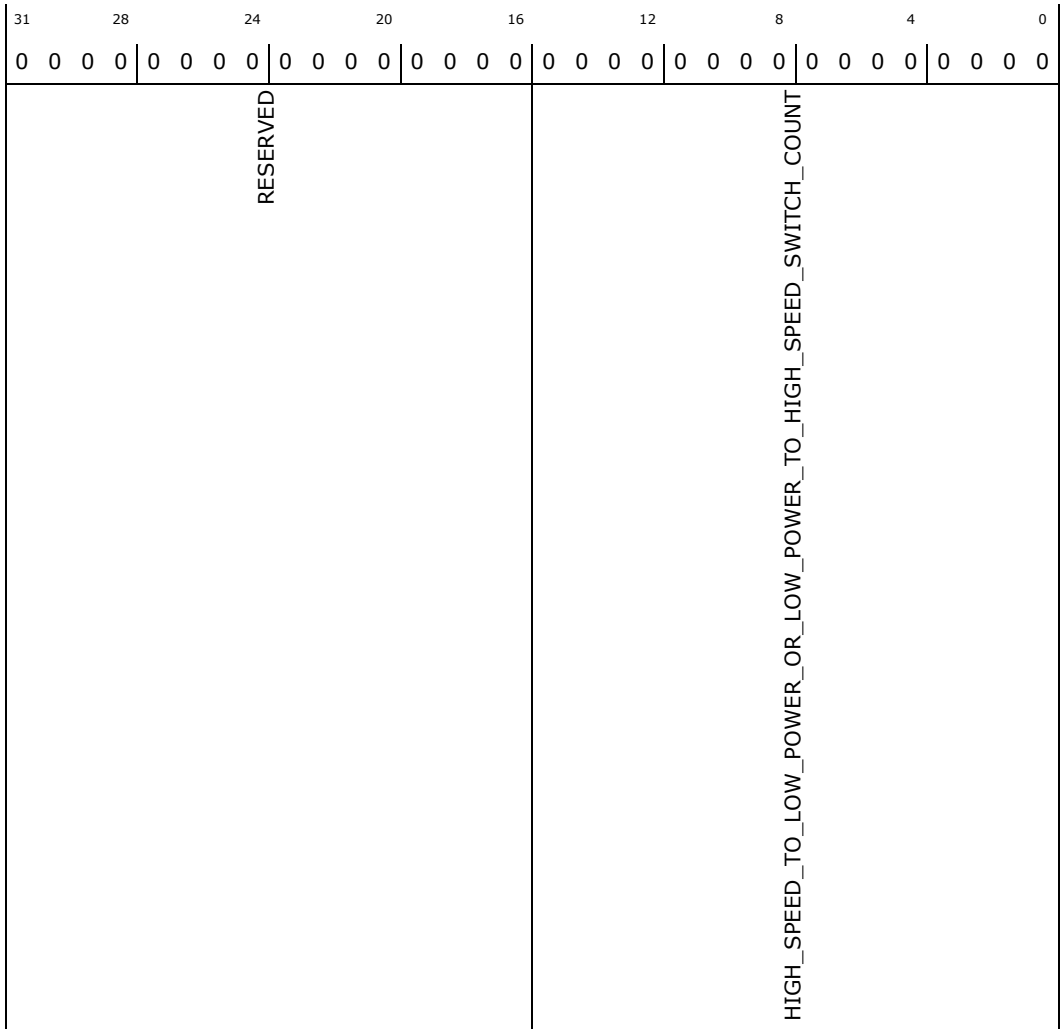
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_HIGH_LOW_SWITCH_COUNT: [GTTMMADR_LSB + 2BF20h] + B844h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs
15:0	0b RW	**HIGH_SPEED_TO_LOW_POWER_OR_LOW_POWER_TO_HIGH_SPEED_SWITCH_COUNT:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs

3.1.116 MIPIC_DPI_CTRL_REG—Offset B848h

mipi C dpi ctrl reg

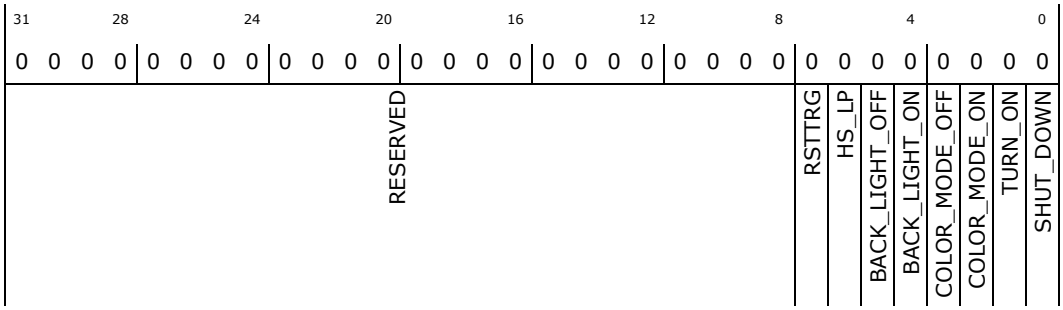
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DPI_CTRL_REG: [GTTMMADR_LSB + 2BF20h] + B848h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**RESERVED:** Reserved.
7	0b RW	**RSTTRG:** mipi C dpi ctrl Reg RSTTRG
6	0b RW	**HS_LP:** Set to '0' to indicate the special packets are sent through the DSI link using HS transmission and set to '1' to indicate that the special packets are sent through the DSI link using low power mode
5	0b RW	**BACK_LIGHT_OFF:** Set to '1' to indicate a backlight OFF short packet has to be packetised for the DPI's virtual channel
4	0b RW	**BACK_LIGHT_ON:** Set to '1' to indicate a backlight ON short packet has to be packetised for the DPI's virtual channel
3	0b RW	**COLOR_MODE_OFF:** Set to '1' to indicate a color mode OFF short packet has to be packetised for the DPI's virtual channel
2	0b RW	**COLOR_MODE_ON:** Set to '1' to indicate a color mode ON short packet has to be packetised for the DPI's virtual channel
1	0b RW	**TURN_ON:** Set to '1' to indicate a turn on short packet has to be packetised for the DPI's virtual channel
0	0b RW	**SHUT_DOWN:** Set to '1' to indicate a shut down short packet has to be packetised for the DPI's virtual channel

3.1.117 MIPIC_DPI_DATA_REGISTER—Offset B84Ch

mipiC dpi data register

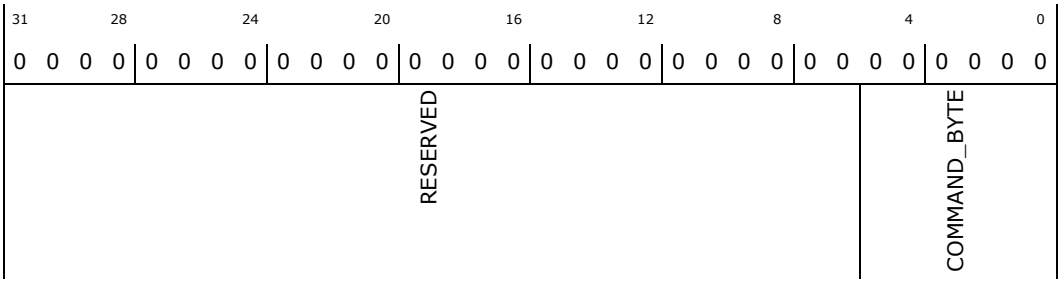
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DPI_DATA_REGISTER: [GTTMMADR_LSB + 2BF20h] + B84Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**RESERVED:** Reserved.
5:0	0b RW	**COMMAND_BYTE:** Command Byte to represent the new or not defined command bytes usage for special features representation. [Like backlight ON and OFF]. This register should be programmed before the DPI control register is being programmed for backlight ON/OFF

3.1.118 MIPIC_INIT_COUNT_REGISTER—Offset B850h

mipi C init counter register

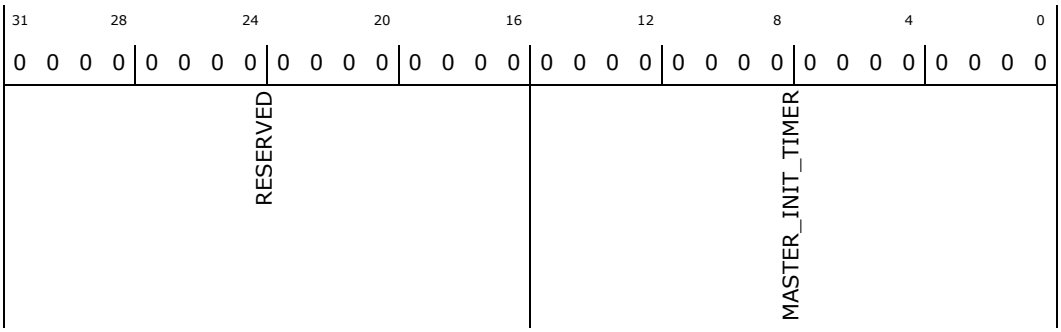
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_INIT_COUNT_REGISTER: [GTTMMADR_LSB + 2BF20h] + B850h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**MASTER_INIT_TIMER:** Counter value in terms of low power clock to initialise the DSI Host IP [TINT] that drives a stop state on the mipi's D-PHY bus

3.1.119 MIPIC_MAX_RETURN_PKT_SIZE_REGISTER—Offset B854h

mipi C max return PKT size register

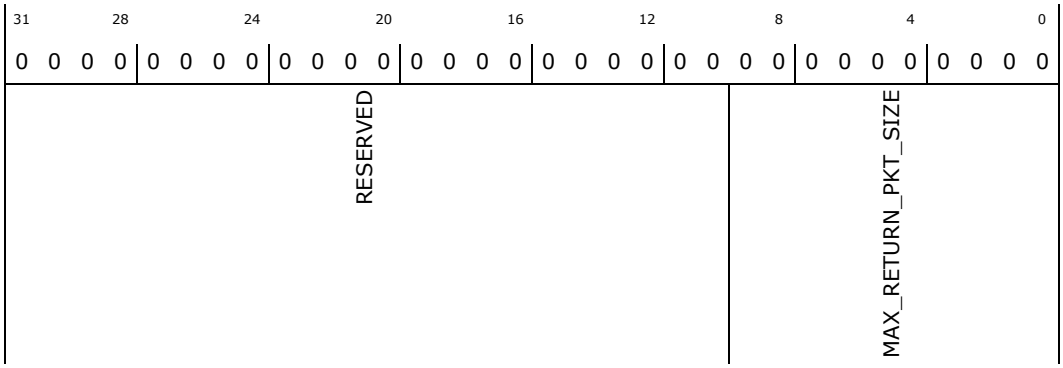
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_MAX_RETURN_PKT_SIZE_REGISTER: [GTTMMADR_LSB + 2BF20h] + B854h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0b RW	**RESERVED:** Reserved.
9:0	0b RW	**MAX_RETURN_PKT_SIZE:** Set the count value in bytes to collect the return data packet for reverse direction data flow in data lane0 in response to a DBI read operation

3.1.120 MIPIC_VIDEO_MODE_FORMAT_REGISTER—Offset B858h

mipi C video mode format register

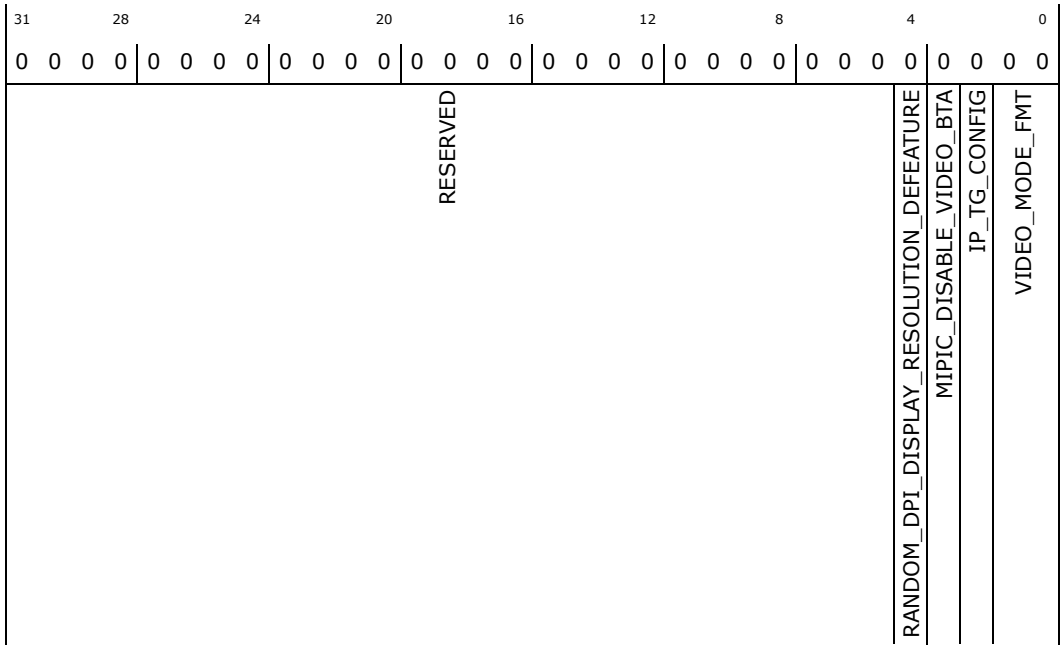
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_VIDEO_MODE_FORMAT_REGISTER: [GTTMMADR_LSB + 2BF20h] + B858h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RW	**RESERVED:** Reserved.
4	0b RW	**RANDOM_DPI_DISPLAY_RESOLUTION_DEFEATURE:** Set by the processor to support random DPI display resolution 0 - random DPI display resolution support disabled. 1 - random DPI display resolution support enabled.
3	0b RW	**MIPIC_DISABLE_VIDEO_BTA:** Set by the processor to inform the DSI controller to disable the BTA sent at the last blanking line of VFP. By default, this bit is set to 0. 0- BTA sending at the last blanking line of VFP is enabled. 1 - BTA sending at the last blanking line of VFP is disabled.
2	0b RW	**IP_TG_CONFIG:** Set by the processor to inform that the DSI controller should discontinue the DPI transfer after the last line of the VFP after ip_tg_enable deassertion. By default, this bit is set to 0. 0 - After ip_tg_enable deassertion, DSI Tx controller stops the DPI transfer immediately after the current packet is transmitted. 1 - After ip_tg_enable deassertion, DSI Tx controller discontinues the DPI transfer after the last line of the VFP

Bit Range	Default & Access	Description
1:0	0b RW	**VIDEO_MODE_FMT:** Sets the Video mode format (packet sequence) to be supported in DSI. In Non Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed equal to RGB word count value In Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed greater than the RGB word count value, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link. 00 Reserved 01 - Non Burst Mode with Sync Pulse 10 - Non Burst Mode with Sync events 11 - Burst Mode

3.1.121 MIPIC_EOT_DISABLE_REGISTER—Offset B85Ch

mipi C EOT disable register

Access Method

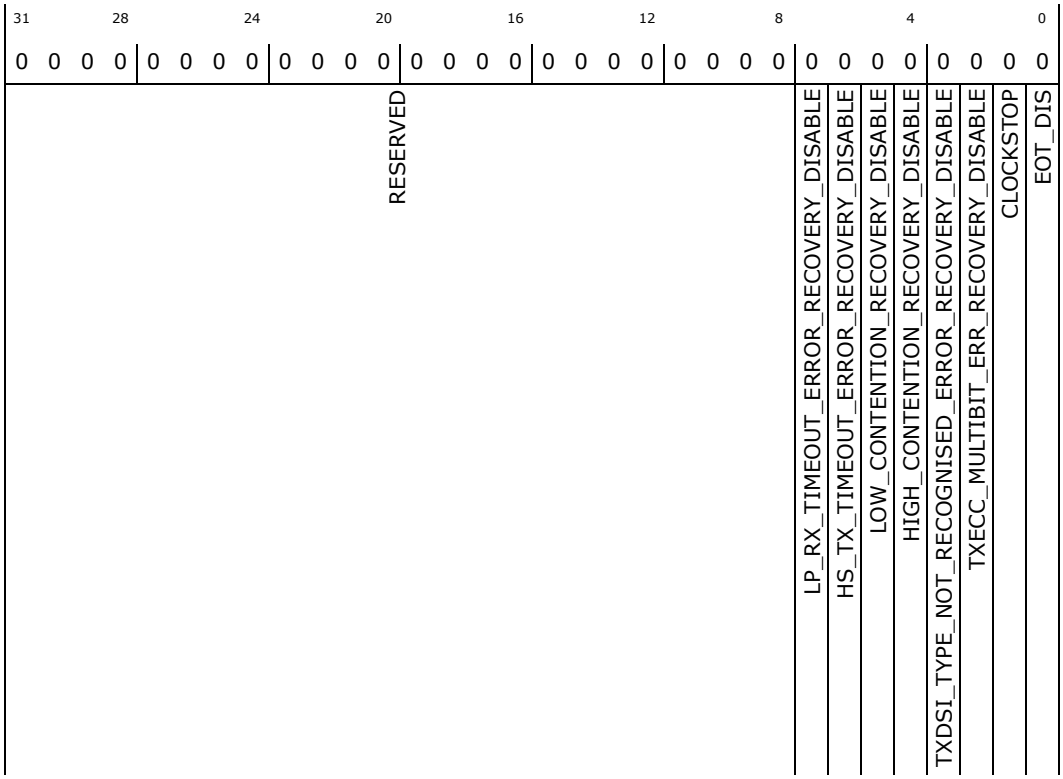
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_EOT_DISABLE_REGISTER: [GTTMMADR_LSB + 2BF20h] + B85Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**RESERVED:** Reserved.
7	0b RW	**LP_RX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the LP_Rx_timeout error recovery if the processor clears LP_Rx_timeout error interrupt. 0 - LP_Rx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the LP_Rx_timeout error interrupt. 1 - If the processor clears the LP_Rx_timeout error interrupt, LP_Rx_timeout error recovery action will not happen in DSI Tx controller. LP Rx timeout error interrupt will act as an informative interrupt
6	0b RW	**HS_TX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the HS_Tx_timeout error recovery if the processor clears HS_Tx_timeout interrupt. 0 - HS_Tx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the HS_Tx_timeout error interrupt. 1 - If the processor clears the HS_Tx_timeout error interrupt, HS_Tx_timeout error recovery action will not happen in DSI Tx controller. HS Tx timeout error interrupt will act as an informative interrupt
5	0b RW	**LOW_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears Low contention interrupt. 0 - Contention recovery will happen if the processor clears Low contention interrupt. 1 - If the processor clears the low contention interrupt, contention recovery procedure will not be initiated by the DSI Tx controller. Low contention interrupt will act as an informative interrupt
4	0b RW	**HIGH_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears High contention interrupt. 0 - Contention recovery will happen if the processor clears High contention interrupt. 1 - If the processor clears the high contention interrupt, contention recovery procedure will not be initiated by the DSI Tx controller. Ignore the High Contention Interrupt in MIPI_INTR_STAT_REG
3	0b RW	**TXDSI_TYPE_NOT_RECOGNISED_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if TxDSI data type not recognized error interrupt is cleared by the processor. 0 - Error recovery action will be taken if TxDSI data type not recognized error interrupt is cleared by the processor. 1 - If TxDSI data type not recognized error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx DSI data type not recognized error interrupt will act as an informative interrupt
2	0b RW	**TXECC_MULTIBIT_ERR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if Tx ECC multibit error interrupt is cleared by the processor. 0 - Error recovery action will be taken if Tx ECC multibit error interrupt is cleared by the processor. 1 - If Tx ECC multibit error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx multibit error interrupt will act as an informative interrupt
1	0b RW	**CLOCKSTOP:** Set by the processor to enable or disable clock stopping feature during BLLP timing in a DPI transfer in dual channel mode or during DPI only mode and also when there is no traffic in the DBI interface in DBI only enabled mode. By default this register value is 0. 0 - clock stopping disabled 1 - clock stopping enabled

Bit Range	Default & Access	Description
0	0b RW	**EOT_DIS:** Set by the processor to enable or disable EOT short packet transmission. By default this register value is 0. For backward compatibility of earlier DSI systems, EOT short packet transmission can be disabled. 0 - EOT short packet transmission enabled 1 - EOT short packet transmission disabled

3.1.122 MIPIC_LP_BYTECLK_REGISTER—Offset B860h

mipi C LP byteclk register

Access Method

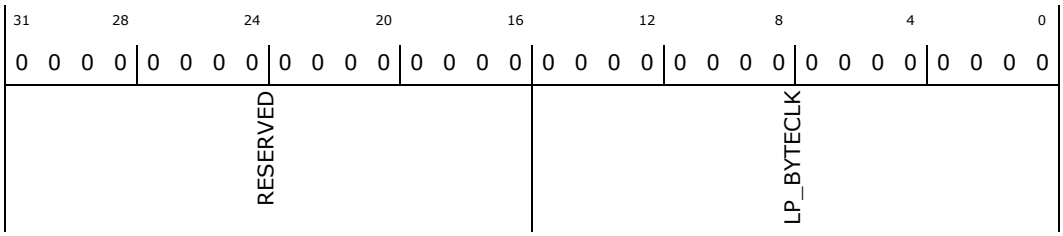
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_LP_BYTECLK_REGISTER: [GTTMMADR_LSB + 2BF20h] + B860h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**LP_BYTECLK:** Low power clock equivalence in terms of byte clock. The value programmed in this register is equal to the number of byte clocks occupied in one low power clock. This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc)

3.1.123 MIPIC_LP_GEN_DATA_REGISTER—Offset B864h

mipi C LP gen DATA register

Access Method

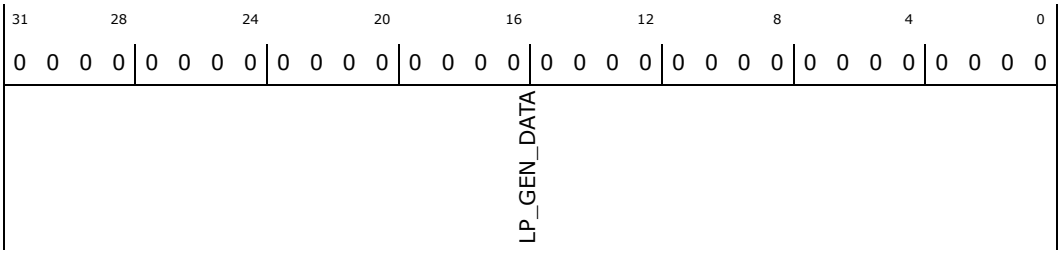
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_LP_GEN_DATA_REGISTER: [GTTMMADR_LSB + 2BF20h] + B864h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**LP_GEN_DATA:** Data port register used for generic data transfers in low power mode

3.1.124 MIPIC_HS_GEN_DATA_REGISTER—Offset B868h

mipi C HS Gen data register

Access Method

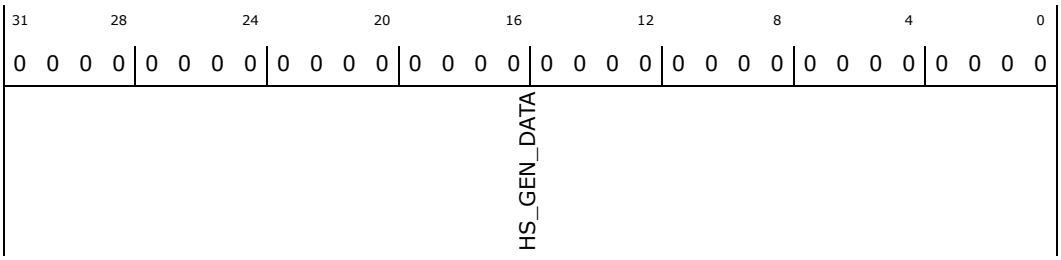
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_HS_GEN_DATA_REGISTER: [GTTMMADR_LSB + 2BF20h] + B868h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**HS_GEN_DATA:** Data port register used for generic data transfers in low power mode

3.1.125 MIPIC_LP_GEN_CTRL_REGISTER—Offset B86Ch

mipi C LP Gen ctrl register

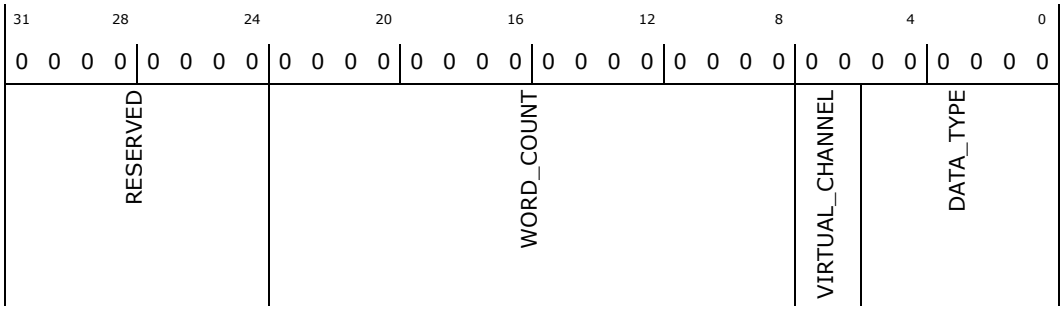
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_LP_GEN_CTRL_REGISTER: [GTTMMADR_LSB + 2BF20h] + B86Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b WO	**RESERVED:** Reserved.
23:8	0b WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0b WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended
5:0	0b WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write, one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

3.1.126 MIPIC_HS_GEN_CTRL_REGISTER—Offset B870h

mipiC HS

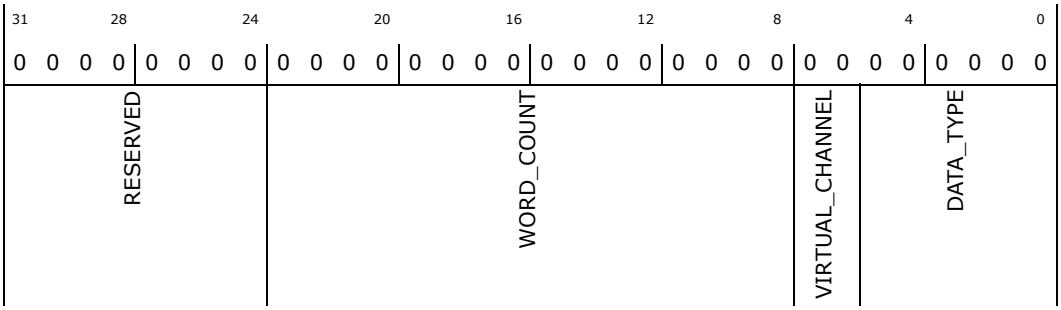
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_HS_GEN_CTRL_REGISTER: [GTTMMADR_LSB + 2BF20h] + B870h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b WO	**RESERVED:** Reserved.
23:8	0b WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0b WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended
5:0	0b WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write, one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

3.1.127 MIPIC_GEN_FIFO_STAT_REGISTER—Offset B874h

mipi C gen fifo stat register

Access Method

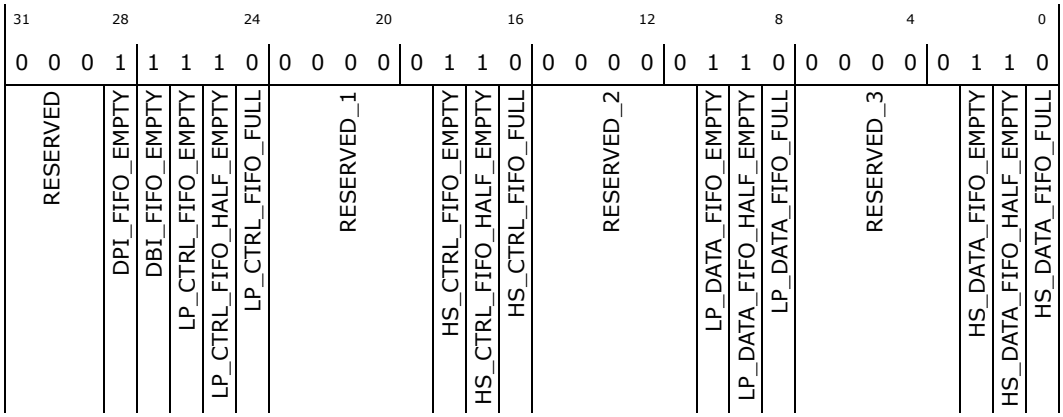
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_GEN_FIFO_STAT_REGISTER: [GTTMMADR_LSB + 2BF20h] + B874h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 1E060606h



Bit Range	Default & Access	Description
31:29	0b RO	**RESERVED:** Reserved.
28	1b RO	**DPI_FIFO_EMPTY:** Default 1
27	1b RO	**DBI_FIFO_EMPTY:** Default 1
26	1b RO	**LP_CTRL_FIFO_EMPTY:** Default 1
25	1b RO	**LP_CTRL_FIFO_HALF_EMPTY:** Default 1
24	0b RO	**LP_CTRL_FIFO_FULL:** Default 0
23:19	0b RO	**RESERVED_1:** Reserved.
18	1b RO	**HS_CTRL_FIFO_EMPTY:** Default 1
17	1b RO	**HS_CTRL_FIFO_HALF_EMPTY:** Default 1
16	0b RO	**HS_CTRL_FIFO_FULL:** Default 0
15:11	0b RO	**RESERVED_2:** Reserved.
10	1b RO	**LP_DATA_FIFO_EMPTY:** Default 1
9	1b RO	**LP_DATA_FIFO_HALF_EMPTY:** Default 1
8	0b RO	**LP_DATA_FIFO_FULL:** Default 0
7:3	0b RO	**RESERVED_3:** Reserved.
2	1b RO	**HS_DATA_FIFO_EMPTY:** Default 1

Bit Range	Default & Access	Description
1	1b RO	**HS_DATA_FIFO_HALF_EMPTY:** Default 1
0	0b RO	**HS_DATA_FIFO_FULL:** Default 0

3.1.128 MIPIC_HS_LS_DBI_ENABLE_REG—Offset B878h

Note : dbi_hs_lp_switch_reg has to be written only if DBI FIFO is empty

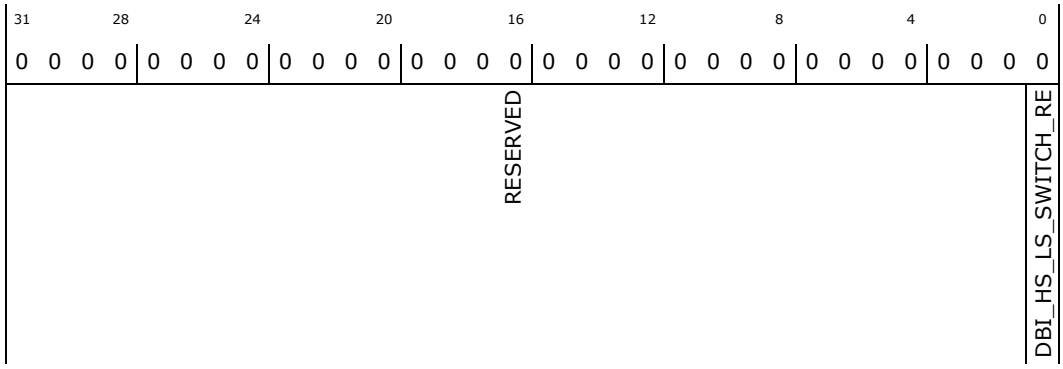
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_HS_LS_DBI_ENABLE_REG: [GTTMMADR_LSB + 2BF20h] + B878h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**RESERVED:** Reserved.
0	0b RW	**DBI_HS_LS_SWITCH_RE:** Set to 1 if DBI packets have to be transmitted in Low power mode Set to 0 if DBI packets have to be transmitted in High speed mode

3.1.129 MIPIC_RESERVED—Offset B87Ch

Reserved.

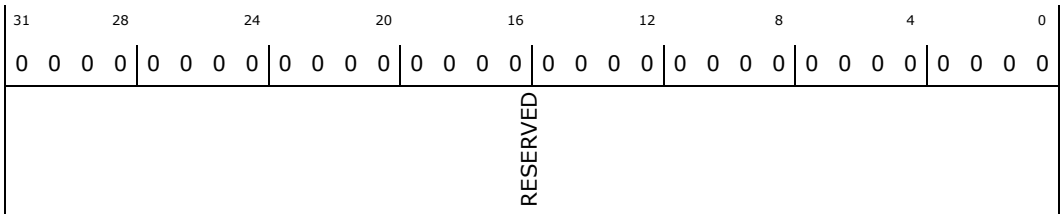
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_RESERVED: [GTTMMADR_LSB + 2BF20h] + B87Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RESERVED:** Reserved.

3.1.130 MIPIC_DPHY_PARAM_REG—Offset B880h

mipi C dphy param reg

Access Method

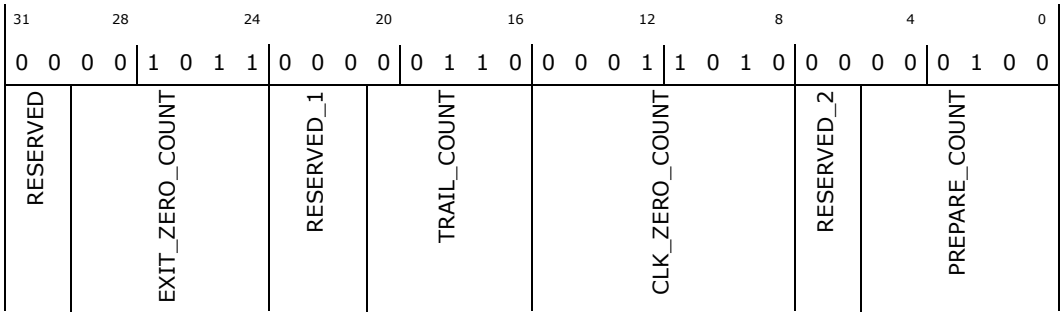
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DPHY_PARAM_REG: [GTTMMADR_LSB + 2BF20h] + B880h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 0B061A04h



Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** Reserved.
29:24	001011b RW	**EXIT_ZERO_COUNT:** THS_0_TIM_UI_CNT and THS_EXIT_TIM_UI_CNT for dphy are programmed as exit zero count by the processor
23:21	0b RW	**RESERVED_1:** Reserved.
20:16	00110b RW	**TRAIL_COUNT:** TCLK_POST_TIM_UI_CNT and TCLK_TRAIL_TIM_UI_CNT for dphy are programmed as trail count by the processor
15:8	00011010b RW	**CLK_ZERO_COUNT:** TCLK_0_TIM_UI_CNT for dphy is programmed as clk zero count by the processor

Bit Range	Default & Access	Description
7:6	0b RW	**RESERVED_2:** Reserved.
5:0	000100b RW	**PREPARE_COUNT:** TCLK_PREP_TIM_UI_CNT and THS_PREP_TIM_UI_CNT for dphy are programmed as prepare count by the processor

3.1.131 MIPIC_DBI_BW_CTRL_REG—Offset B884h

mipi C DBI BW ctrl reg

Access Method

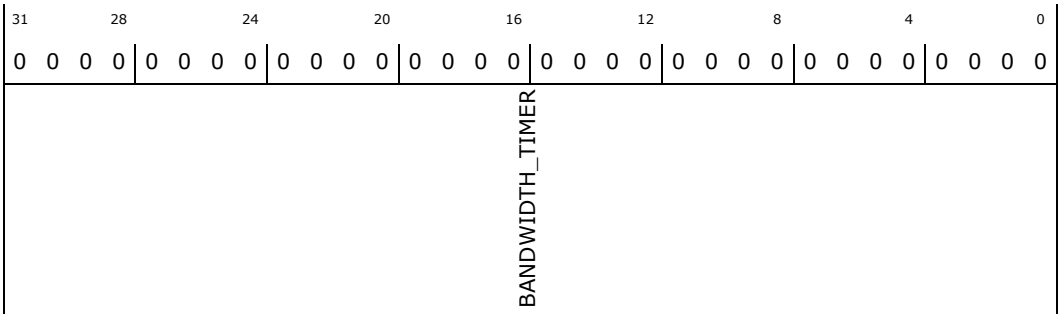
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DBI_BW_CTRL_REG: [GTTMMADR_LSB + 2BF20h] + B884h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**BANDWIDTH_TIMER:** DBI Bandwidth control Register. The bandwidth essential for transmitting 16 long packets containing 252 bytes meant for DCS write memory command is programmed in this register in terms of byte clocks. Based on the DSI transfer rate and the number of lanes configured the time taken to transmit 16 long packets in a DSI stream varies. **NOTE:** : The value programmed in this timer must be greater than the actual time taken to carry out 16 long packets transmission in DSI stream plus the time taken to transmit two blanking packets

3.1.132 MIPIC_CLK_LANE_SWITCHING_TIME_CNT—Offset B888h

mipi C clk lane switching time count

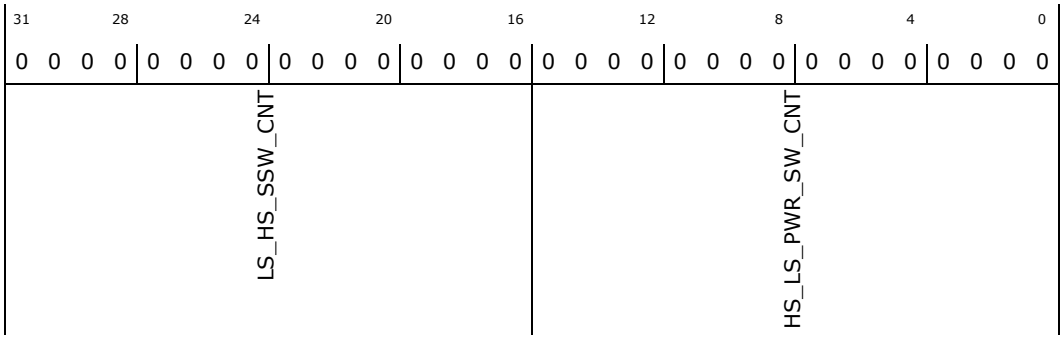
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_CLK_LANE_SWITCHING_TIME_CNT: [GTTMMADR_LSB + 2BF20h] + B888h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**LS_HS_SSW_CNT:** Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
15:0	0b RW	**HS_LS_PWR_SW_CNT:** High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs

3.1.133 MIPIC_STOP_STATE_STALL—Offset B88Ch

mipi C stop state stall

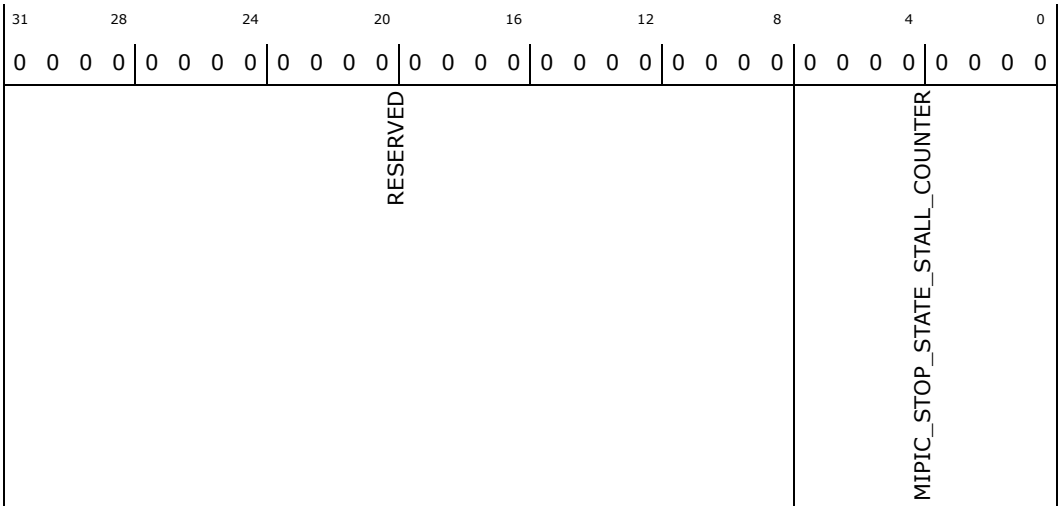
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_STOP_STATE_STALL: [GTTMMADR_LSB + 2BF20h] + B88Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**RESERVED:** reserved
7:0	0b RW	**MIPIC_STOP_STATE_STALL_COUNTER:** Delay between (stall the stop state signal) the data transfer is increased based on this counter value. This counter is calculated from txclkesc. **NOTE:** If processor programs this register then it needs to reprogram the high_low_ switch counter in B844h and lp_equivalent_byteclk reg in B860h to compensate this delay. High_low_switch_count B844h: High to low switch counter = Actual High to low switch + stop_sta_stall_reg value * Low power clock equivalence value in terms of byte clock LP equivalent byteclk register B860h: LP equivalent byteclk value = txclkesc time/ txbyteclk time * (105 + stop_sta_stall_reg value) / 105 Minimum time of Low Power short packet transfer = 105 txclkesc

3.1.134 MIPIC_INTR_STAT_REG_1—Offset B890h

mipi C interrupt stat register 1

Access Method

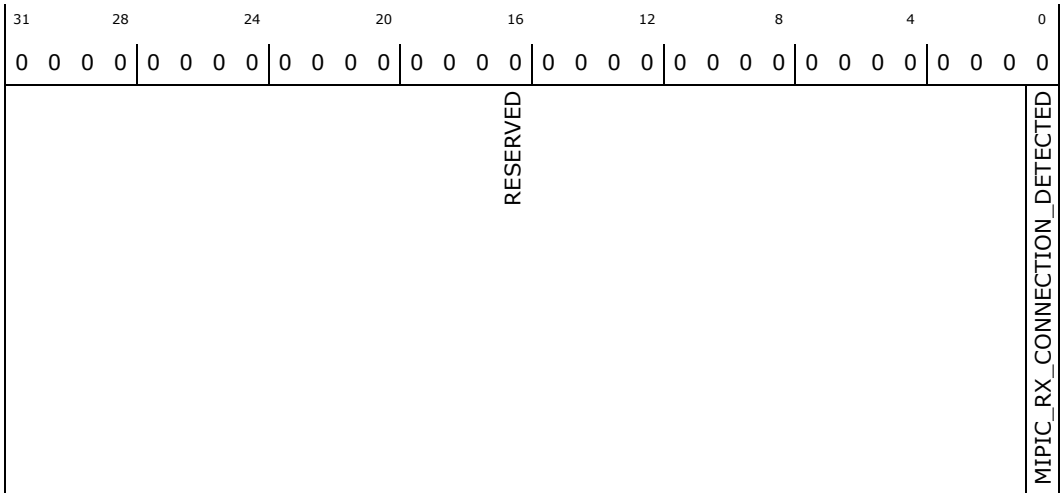
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_INTR_STAT_REG_1: [GTTMMADR_LSB + 2BF20h] + B890h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**RESERVED:** reserved
0	0b RW	**MIPIC_RX_CONNECTION_DETECTED:** Set to 1'b1 if the contention detected in the display device and is reported in the Acknowledge packet by the display device

3.1.135 MIPIC_INTR_EN_REG_1—Offset B894h

mipic interrupt enable register

Access Method

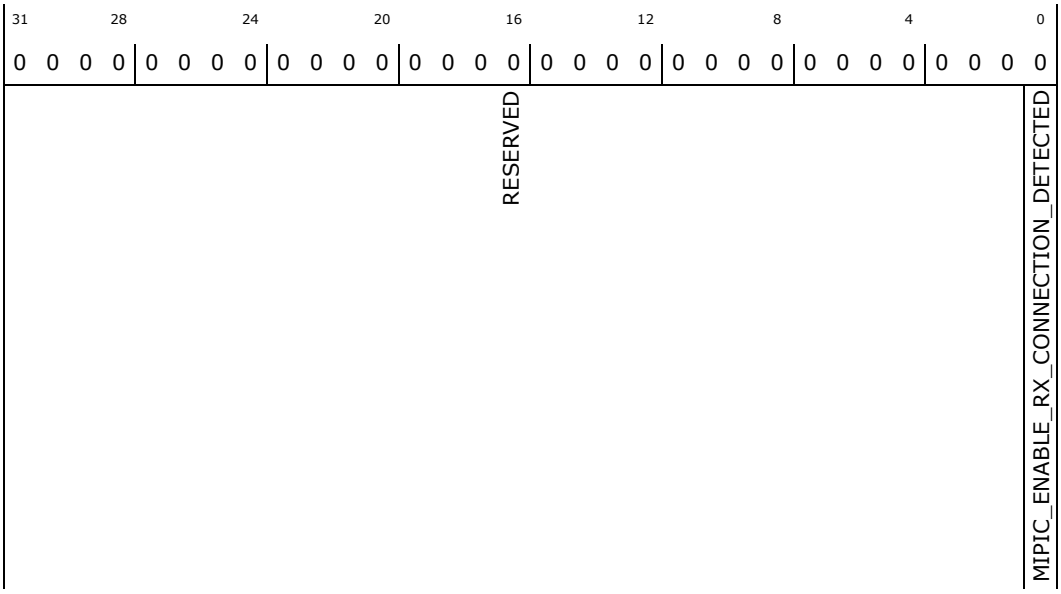
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_INTR_EN_REG_1: [GTTMMADR_LSB + 2BF20h] + B894h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**RESERVED:** reserved
0	0b RW	**MIPIC_ENABLE_RX_CONNECTION_DETECTED:** Set to enable the interrupt for contention detected error in the acknowledgement packet reports

3.1.136 MIPIC_CTRL—Offset B904h

mipi ctrl reg

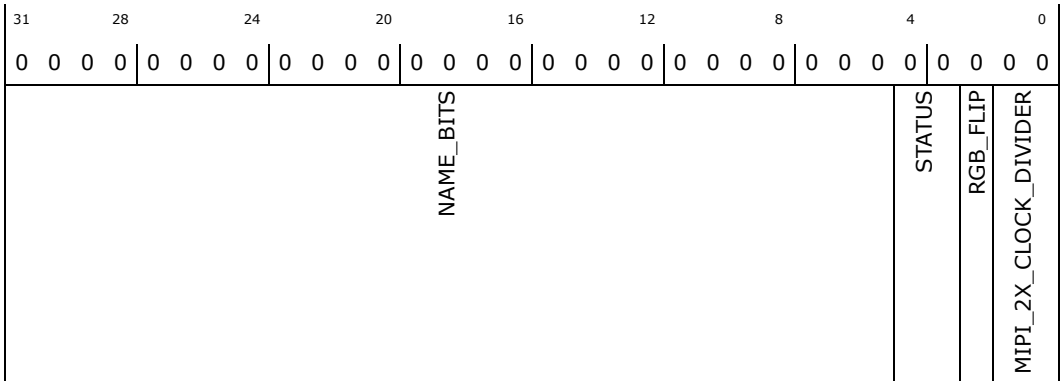
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_CTRL: [GTTMMADR_LSB + 2BF20h] + B904h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RW	**NAME_BITS:** Reserved
4:3	0b RW	**STATUS:** 2'b00: low priority on read requests to G-unit 2'b11 : high priority
2	0b RW	**RGB_FLIP:** 1'b0 : RGB data from disp2d is reverted to BGR 1'b1 : RGB data from disp2d is passed as is to MIPI IP
1:0	0b RW	**MIPI_2X_CLOCK_DIVIDER:** Reserved

3.1.137 MIPIC_DATA_ADD—Offset B908h

mipi C data ADD

Access Method

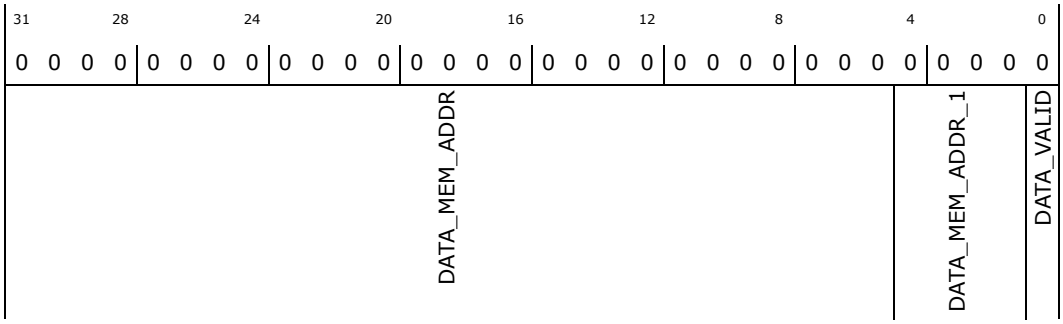
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DATA_ADD: [GTTMMADR_LSB + 2BF20h] + B908h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RW	**DATA_MEM_ADDR:** When there is updated data for the display panel, S/W programs this register with the memory address to read from
4:1	0b RW	**DATA_MEM_ADDR_1:** Reserved
0	0b RW	**DATA_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.1.138 MIPIC_DATA_LEN—Offset B90Ch

mipiC data length

Access Method

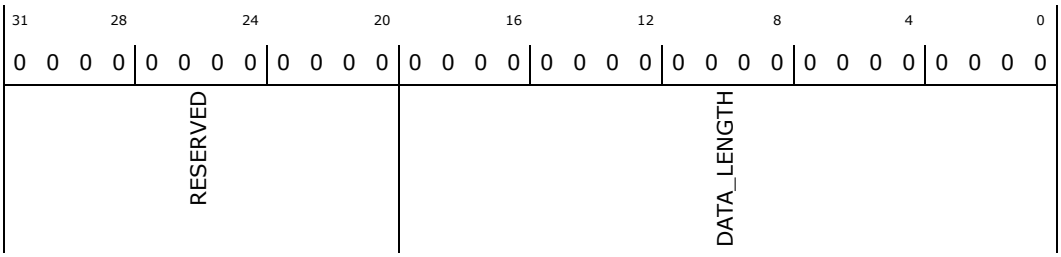
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_DATA_LEN: [GTTMMADR_LSB + 2BF20h] + B90Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**DATA_LENGTH:** This field shows the remaining length of data that needs to be read from memory, Initially set by S/W and is decremented by H/W as reads are issued

3.1.139 MIPIC_CMD_ADD—Offset B910h

mipiC command add

Access Method

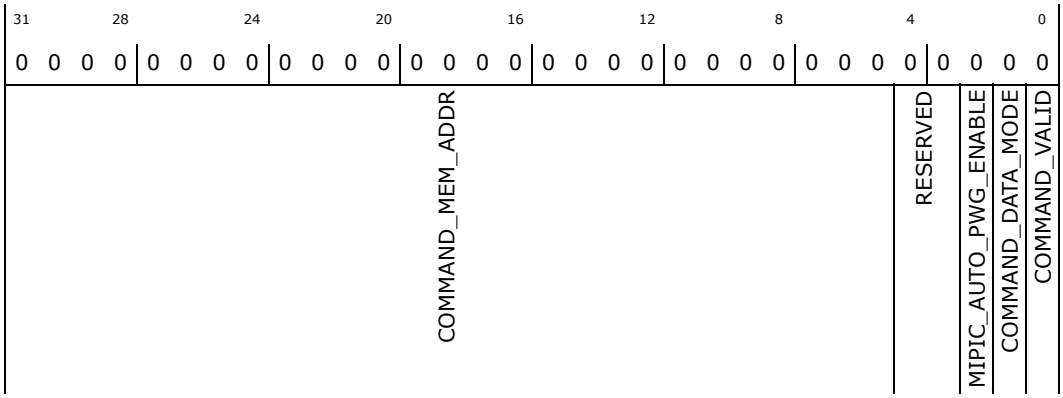
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_CMD_ADD: [GTTMMADR_LSB + 2BF20h] + B910h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RW	**COMMAND_MEM_ADDR:** When there are new commands that need to be sent to the display panel, S/W programs this register with the memory address to read the commands from
4:3	0b RW	**RESERVED:** MBZ
2	0b RW	**MIPIC_AUTO_PWG_ENABLE:** Idle state: SW driver writes to this bit to enable auto power gating for MIPIC controller 0: default 1: auto power gate is enabled
1	0b RW	**COMMAND_DATA_MODE:** 0: data for memory write command from system buffer that is specified by MIPI data address register 1: data for memory write command from pipe A rendering
0	0b RW	**COMMAND_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.1.140 MIPIC_CMD_LEN—Offset B914h

mipiC command Length

Access Method

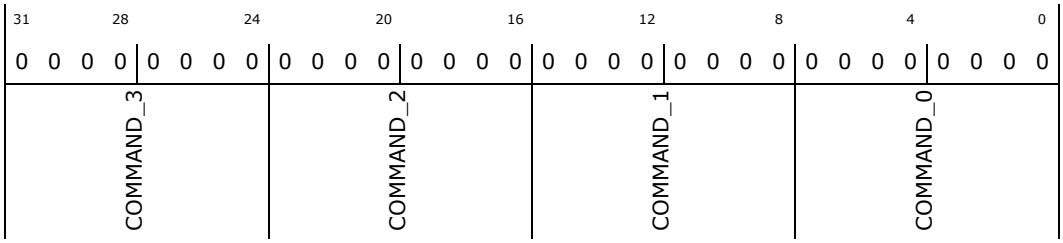
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_CMD_LEN: [GTTMMADR_LSB + 2BF20h] + B914h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**COMMAND_3:** This is command 3 length (command + parameters) in bytes
23:16	0b RW	**COMMAND_2:** This is command 2 length (command + parameters) in bytes
15:8	0b RW	**COMMAND_1:** This is command 1 length (command + parameters) in bytes
7:0	0b RW	**COMMAND_0:** This is command 0 length (command + parameters) in bytes

3.1.141 MIPIC_RD_DATA_RETURN0—Offset B918h

mipi C Read data return 0

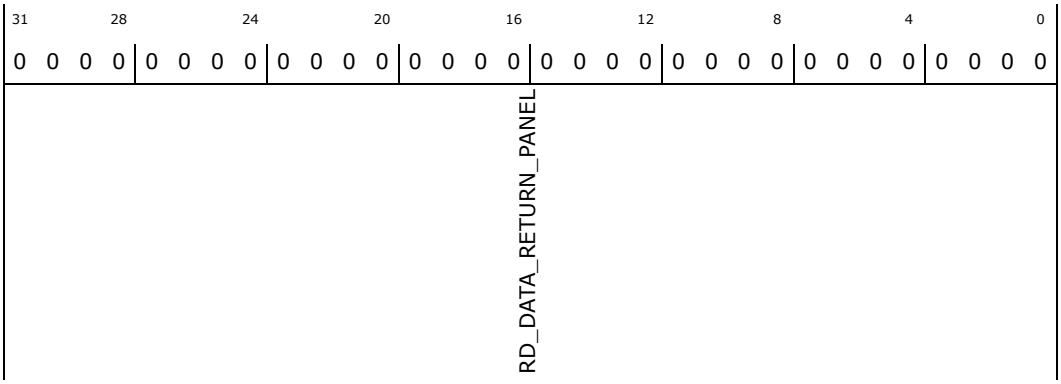
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_RD_DATA_RETURN0: [GTTMMADR_LSB + 2BF20h] + B918h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.142 MIPIC_RD_DATA_RETURN1—Offset B91Ch

mipi C read data return 1

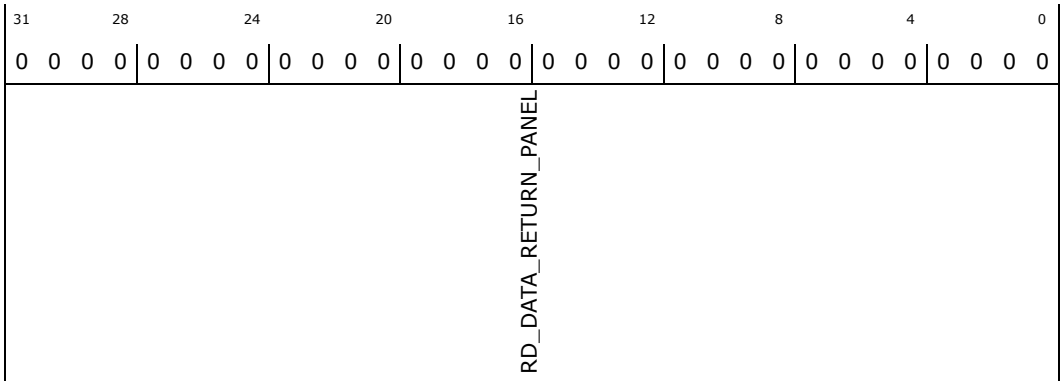
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_RD_DATA_RETURN1: [GTTMMADR_LSB + 2BF20h] + B91Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.143 MIPIC_RD_DATA_RETURN2—Offset B920h

mipi C read data return 2

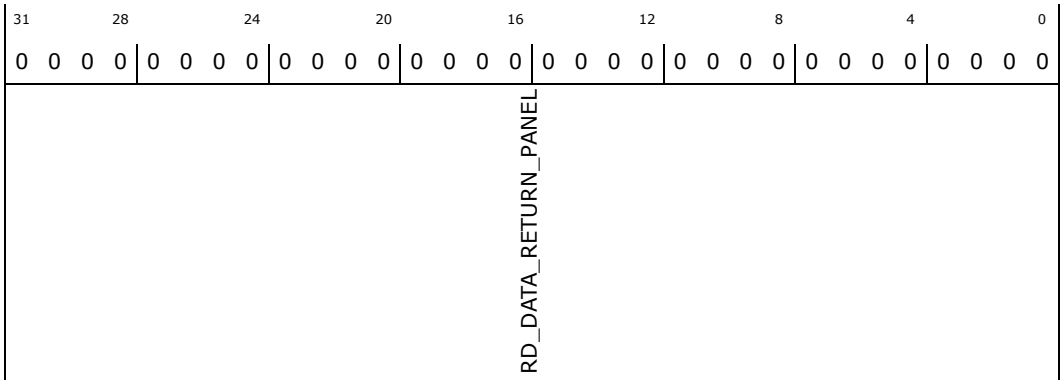
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_RD_DATA_RETURN2: [GTTMMADR_LSB + 2BF20h] + B920h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.144 MIPIC_RD_DATA_RETURN3—Offset B924h

mipi C read data return 3

Access Method

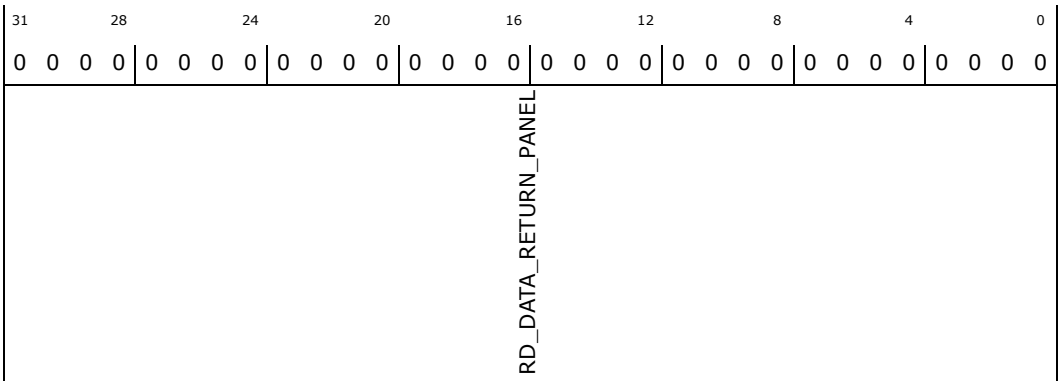
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_RD_DATA_RETURN3: [GTTMMADR_LSB + 2BF20h] + B924h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.145 MIPIC_RD_DATA_RETURN4—Offset B928h

mipi C read data return 4

Access Method

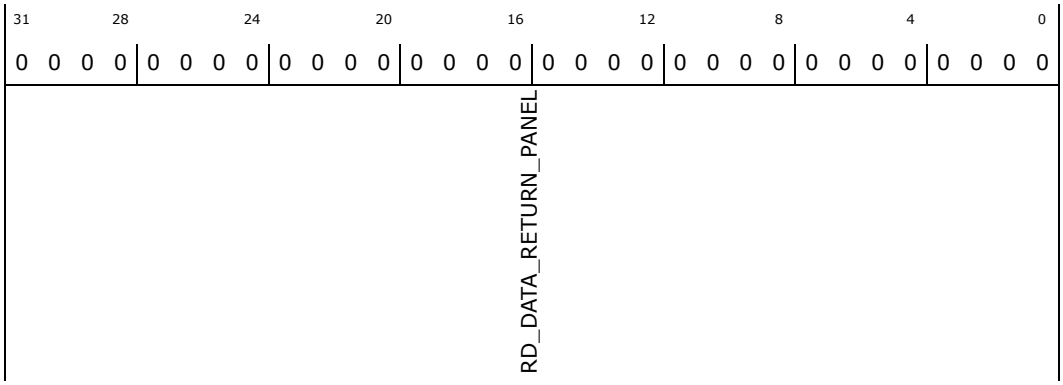
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_RD_DATA_RETURN4: [GTTMMADR_LSB + 2BF20h] + B928h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.146 MIPIC_RD_DATA_RETURN5—Offset B92Ch

mipi C read data return 5

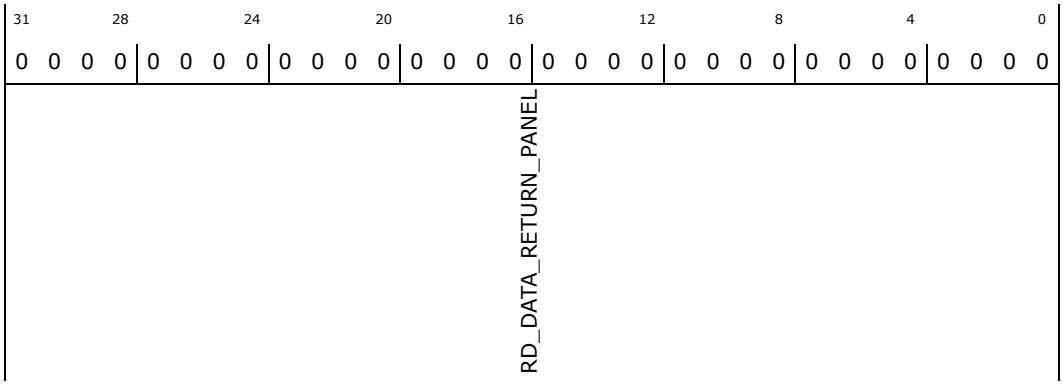
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_RD_DATA_RETURN5: [GTTMMADR_LSB + 2BF20h] + B92Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.147 MIPIC_RD_DATA_RETURN6—Offset B930h

mipi C read data return 6

Access Method

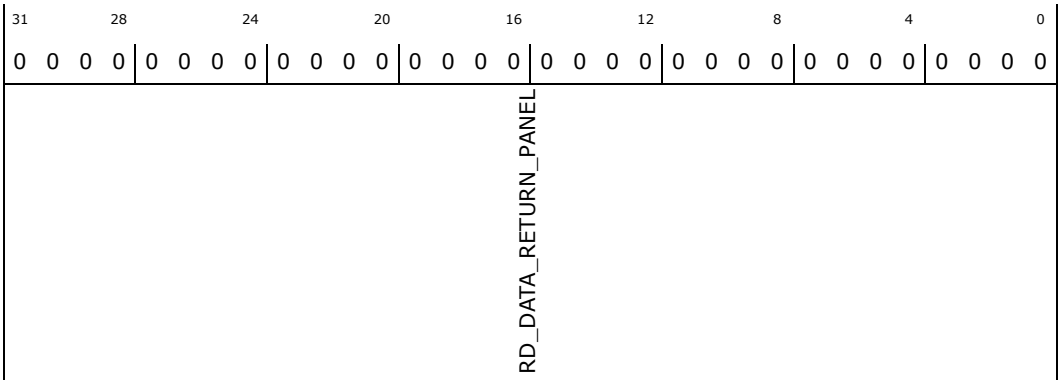
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_RD_DATA_RETURN6: [GTTMMADR_LSB + 2BF20h] + B930h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.148 MIPIC_RD_DATA_RETURN7—Offset B934h

mipi C read data return 7

Access Method

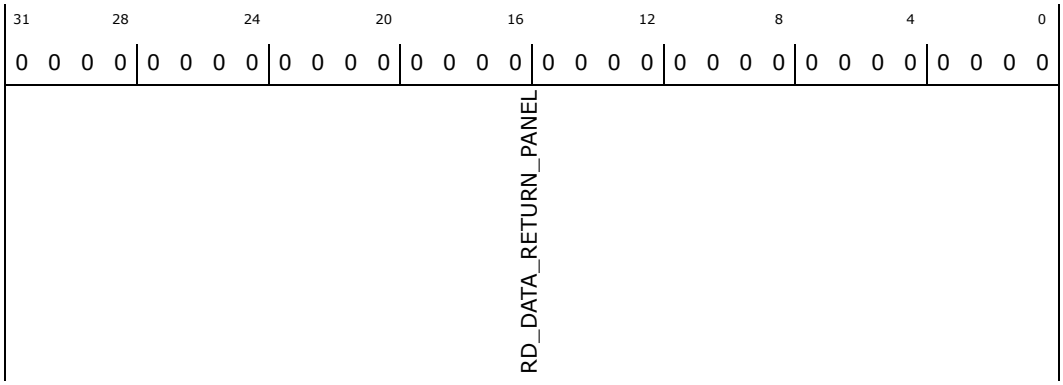
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_RD_DATA_RETURN7: [GTTMMADR_LSB + 2BF20h] + B934h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

3.1.149 MIPIC_RD_DATA_VALID—Offset B938h

mipi C read data valid

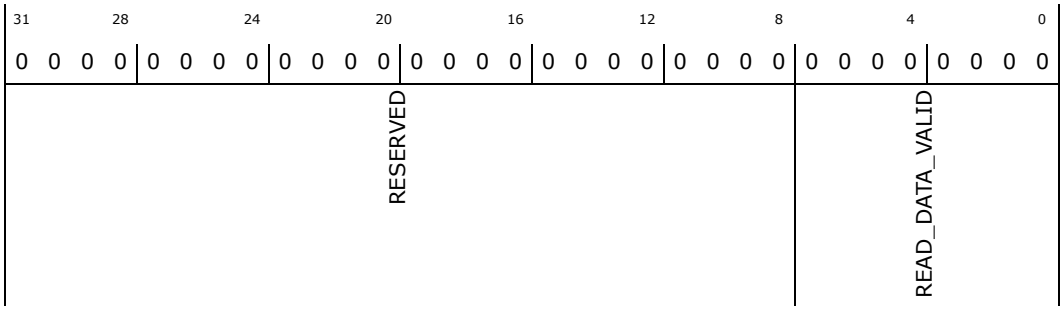
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_RD_DATA_VALID: [GTTMMADR_LSB + 2BF20h] + B938h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**RESERVED:** Reserved.
7:0	0b RW	**READ_DATA_VALID:** Each bit corresponds to presence of valid data in the registers above. When data is returned from the panel, H/W will write into these registers in sequence, and set the corresponding valid bit. When S/W issues a write '1 to the registers, this bit is cleared

3.1.150 HTOTAL_A—Offset 60000h

Pipe A Horizontal Total Register

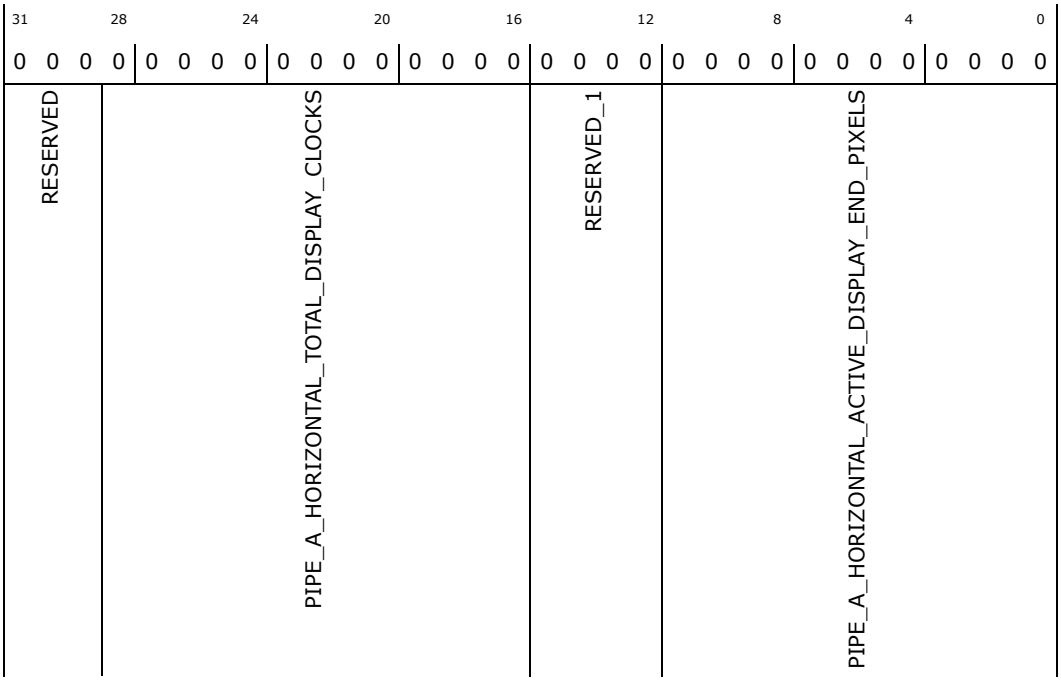
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HTOTAL_A: [GTTMMADR_LSB + 2BF20h] + 60000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_A_HORIZONTAL_TOTAL_DISPLAY_CLOCKS:** This 13-bit field provides Horizontal Total up to 8192 pixels encompassing the Horizontal Active Display period, front/back border and retrace period. Any pending event (HSYNC, ACTIVE, HBLANK) is reset at HTOTAL and the programmed sequence begins again. This field is programmed to the number of clocks desired minus one. This number of clocks needs to be a multiple of two when driving data out the digital port out the LVDS port in two channel mode. This value should always be equal or greater to the sum of the horizontal active and the horizontal blank, and border region sizes.
15:12	0b RW	**RESERVED_1:** Write as zero.

Bit Range	Default & Access	Description
11:0	0b RW	**PIPE_A_HORIZONTAL_ACTIVE_DISPLAY_END_PIXELS:** This 12-bit field provides Horizontal Active Display resolutions up to 4096 pixels. **NOTE:** The first horizontal active display pixel is considered pixel number 0. The value programmed should be the (active pixels/line 1). The number of active pixels will be limited to multiples of two pixels when driving the integrated LVDS port in two channel mode. For proper results during VGA centering mode this value needs to be large enough to fit the largest VGA mode supported, this should be at least 720/1440 pixels for standard VGA type modes or 640/1280 pixels if the nine-dot disable bit in the VGA control register is set. When using the internal panel fitting logic, the minimum horizontal size allowed will be three pixels.

3.1.151 HBLANK_A—Offset 60004h

Pipe A Horizontal Blank Register

Access Method

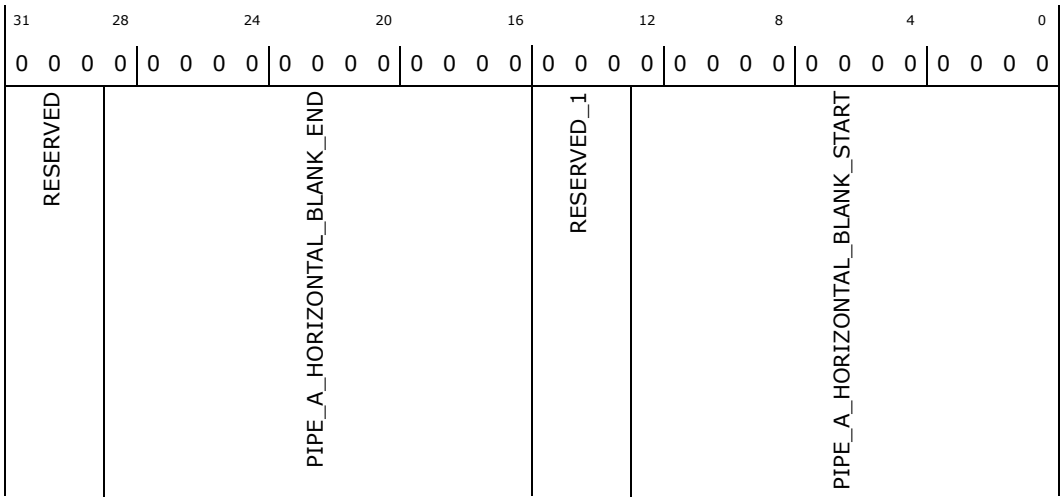
Type: Memory Mapped I/O Register (Size: 32 bits)

HBLANK_A: [GTTMMADR_LSB + 2BF20h] + 60004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Read Only.

Bit Range	Default & Access	Description
28:16	0b RW	**PIPE_A_HORIZONTAL_BLANK_END:** This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. The number of clocks within blank needs to be a multiple of two when driving data out LVDS in two channel mode. The value loaded in the register would be equal to RightBorder+Active+HBlank-1. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the HTOTAL register.
15:13	0b RW	**RESERVED_1:** Read Only.
12:0	0b RW	**PIPE_A_HORIZONTAL_BLANK_START:** This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks for both left and right borders need to be a multiple of two when driving data out the LVDS port in two channel mode. Horizontal blank should only start after the end of the horizontal active region. The value loaded in the register would be equal to RightBorder+Active-1. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the HACTIVE register.

3.1.152 HSYNC_A—Offset 60008h

Pipe A Horizontal Sync Register

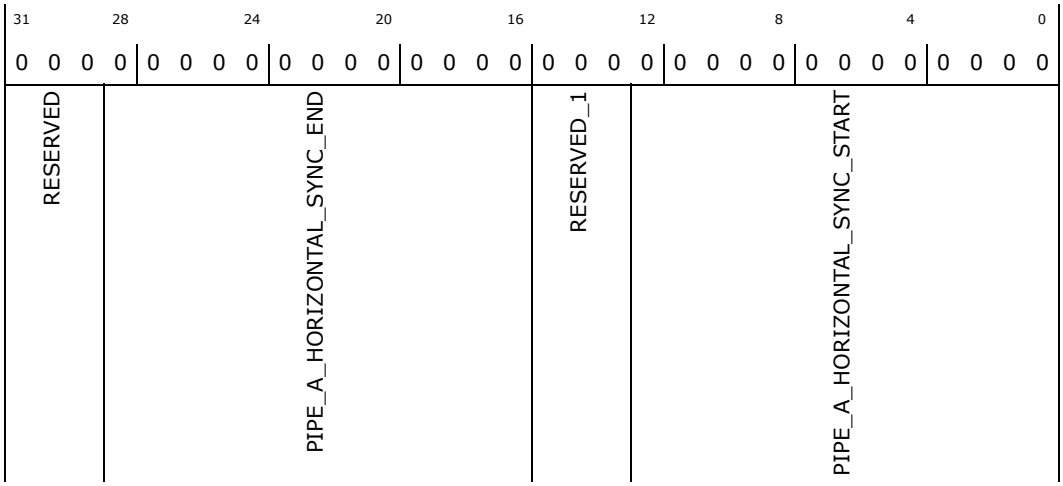
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HSYNC_A: [GTTMMADR_LSB + 2BF20h] + 60008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_A_HORIZONTAL_SYNC_END:** This 13-bit field specifies the horizontal Sync End position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks in the sync period needs to be a multiple of two when driving data out the LVDS port in two channel mode. This value should be greater than the horizontal sync start position and would be loaded with the Active+RightBorder+FrontPorch+Sync-1.
15:13	0b RW	**RESERVED_1:** Read Only.
12:0	0b RW	**PIPE_A_HORIZONTAL_SYNC_START:** This 13-bit field specifies the horizontal Sync Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Note that when HSYNC Start is programmed equal to HBLANK Start, both HSYNC and HBLANK will be asserted on the same pixel clock. It should never be programmed to less than HBLANK start. The number of cycles from the beginning of the line needs to be a multiple of two when driving data out the LVDS port in two channel mode. This register should not be less than the horizontal active end. This register should be loaded with the Active+RightBorder+FrontPorch-1.

3.1.153 VTOTAL_A—Offset 6000Ch

Pipe A Vertical Total Register

Access Method

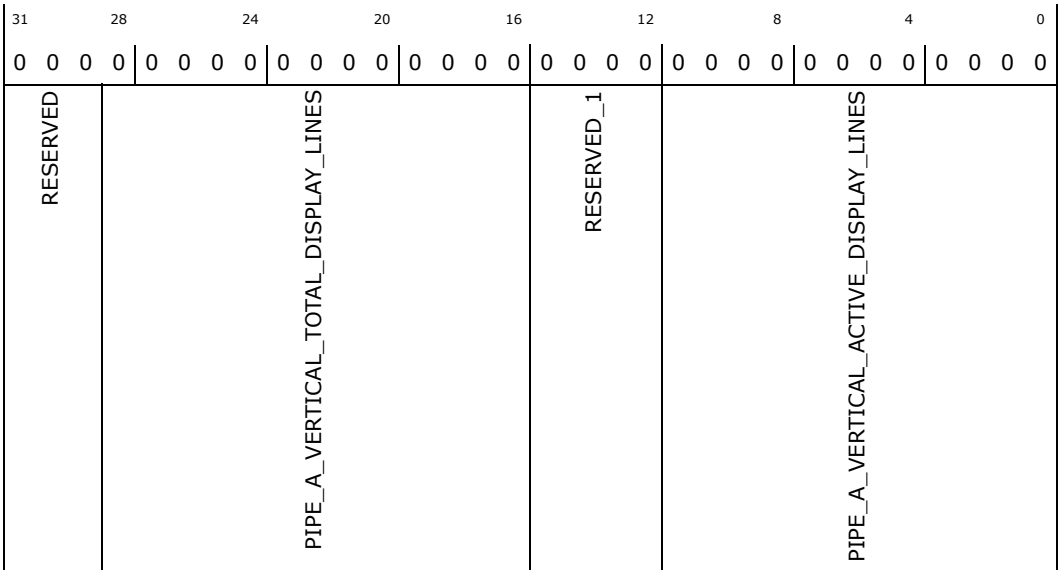
Type: Memory Mapped I/O Register (Size: 32 bits)

VTOTAL_A: [GTTMMADR_LSB + 2BF20h] + 6000Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Read Only.
28:16	0b RW	**PIPE_A_VERTICAL_TOTAL_DISPLAY_LINES:** This 13 bit field provides Vertical Total up to 8192 lines encompassing the Vertical Active Display Lines, top/bottom border and retrace period. The value programmed should be the number of lines required minus one. Vertical total needs to be large enough to be greater than the sum of the vertical active, vertical border, and the vertical blank regions. The vertical counter is incremented on the leading edge of the horizontal sync. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of lines in each field.
15:12	0b RW	**RESERVED_1:** Read Only.
11:0	0b RW	**PIPE_A_VERTICAL_ACTIVE_DISPLAY_LINES:** This 12-bit field provides vertical active display resolutions up to 4096 lines. It should be programmed with the desired number of lines minus one. When using the internal panel fitting logic, the minimum vertical active area must be three lines. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of lines in each field.

3.1.154 VBLANK_A—Offset 60010h

Pipe A Vertical Blank Register

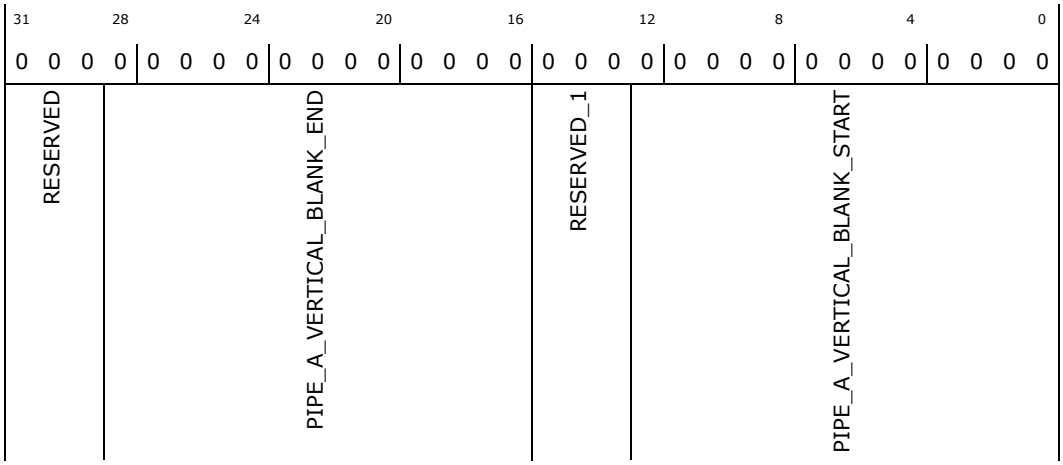
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VBLANK_A: [GTTMMADR_LSB + 2BF20h] + 60010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Read Only.
28:16	0b RW	**PIPE_A_VERTICAL_BLANK_END:** This 13-bit field specifies the Vertical Blank End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VBLANK End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. The end of vertical blank should be after the start of vertical blank and before or equal to the vertical total. This register should be loaded with the Vactive+BottomBorder+VBlank-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank end in each field. It does not count the two half lines that get added when operating in modes with half lines. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the VTOTAL register.
15:13	0b RW	**RESERVED_1:** Read Only.

Bit Range	Default & Access	Description
12:0	0b RW	**PIPE_A_VERTICAL_BLANK_START:** This 13-bit field specifies the Vertical Blank Start expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VBLANK Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. Minimum vertical blank size is required to be at least three lines. Blank should start after the end of active. This register is loaded with the Vactive+BottomBorder-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank start in each field. It does not count the two half lines that get added when operating in modes with half lines. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the VACTIVE register.

3.1.155 VSYNC_A—Offset 60014h

Pipe A Vertical Sync Register

Access Method

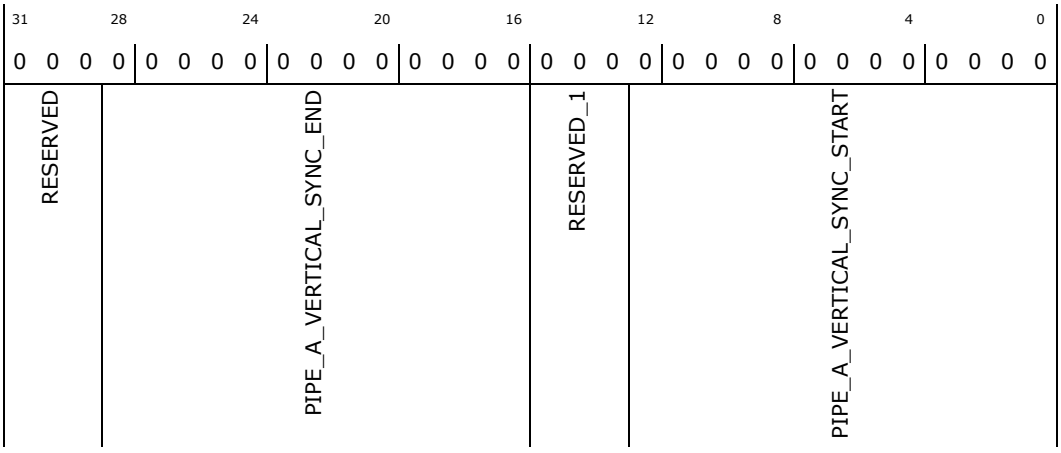
Type: Memory Mapped I/O Register (Size: 32 bits)

VSYNC_A: [GTTMMADR_LSB + 2BF20h] + 60014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Read Only.

Bit Range	Default & Access	Description
28:16	0b RW	**PIPE_A_VERTICAL_SYNC_END:** This 13-bit field specifies the Vertical Sync End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VSYNC End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. This register should be loaded with Vactive+BottomBorder+FrontPorch+Sync-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical sync end in each field. It does not count the two half lines that get added when operating in modes with half lines.
15:13	0b RW	**RESERVED_1:** Read Only.
12:0	0b RW	**PIPE_A_VERTICAL_SYNC_START:** This 13-bit field specifies the Vertical Sync Start position expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VSYNC Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. This register would be loaded with Vactive+BottomBorder+FrontPorch-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical sync start in each field. It does not count the two half lines that get added when operating in modes with half lines.

3.1.156 PIPESRCA—Offset 6001Ch

Pipe A Source Image Size

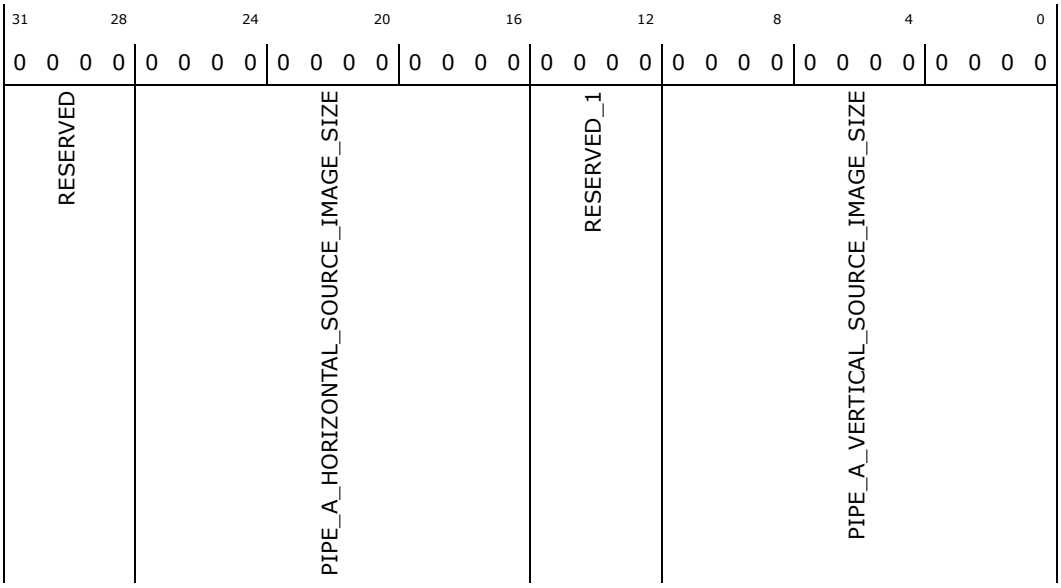
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPESRCA: [GTTMMADR_LSB + 2BF20h] + 6001Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PIPE_A_HORIZONTAL_SOURCE_IMAGE_SIZE:** This 12-bit field specifies Horizontal source image size up to 4096. This determines the size of the image created by the display planes sent to the blender. The value programmed should be the source image size minus one. The actual source size must be two times the programmed value in the pixel multiply mode. It must represent a size that is a multiple of two (even numbers) when driving the LVDS port in two channel mode. This implies that for this mode, the value programmed will always be an odd number. Except in the case of panel fitting internal or in an external device, this register field would be programmed to a value identical to the horizontal active. This is the only register of the timing registers that is allowed to be programmed while the pipe is enabled.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PIPE_A_VERTICAL_SOURCE_IMAGE_SIZE:** This 12-bit field specifies the vertical source image size up to 4096 lines. This determines the size of the image created by the display planes sent to the blender. The value programmed should be the source image size minus one. Note that the actual number of lines needs to be at least twice the planes programmed value when in the pixel multiply mode. Except in the case of panel fitting internal or in an external device, this register field would be programmed to a value identical to the vertical active. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical source image size in each field.

3.1.157 BCLRPAT_A—Offset 60020h

Pipe A Border Color Pattern Register

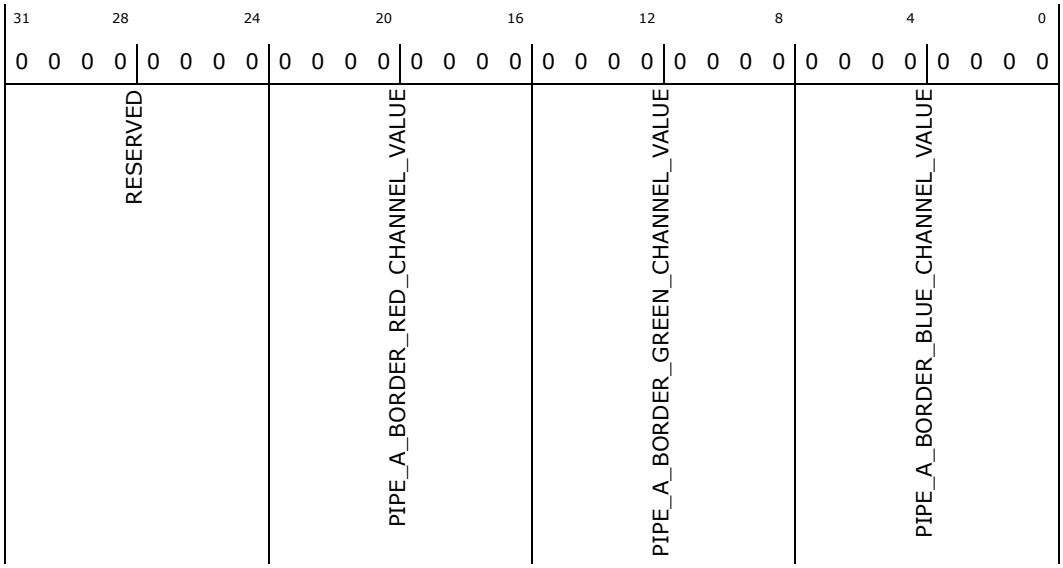
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BCLRPAT_A: [GTTMMADR_LSB + 2BF20h] + 60020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**PIPE_A_BORDER_RED_CHANNEL_VALUE:** pipeA border red channel values
15:8	0b RW	**PIPE_A_BORDER_GREEN_CHANNEL_VALUE:** pipeA border green channel values
7:0	0b RW	**PIPE_A_BORDER_BLUE_CHANNEL_VALUE:** pipeA border blue channel values

3.1.158 VSYNCSHIFT_A—Offset 60028h

Vertical Sync Shift Register

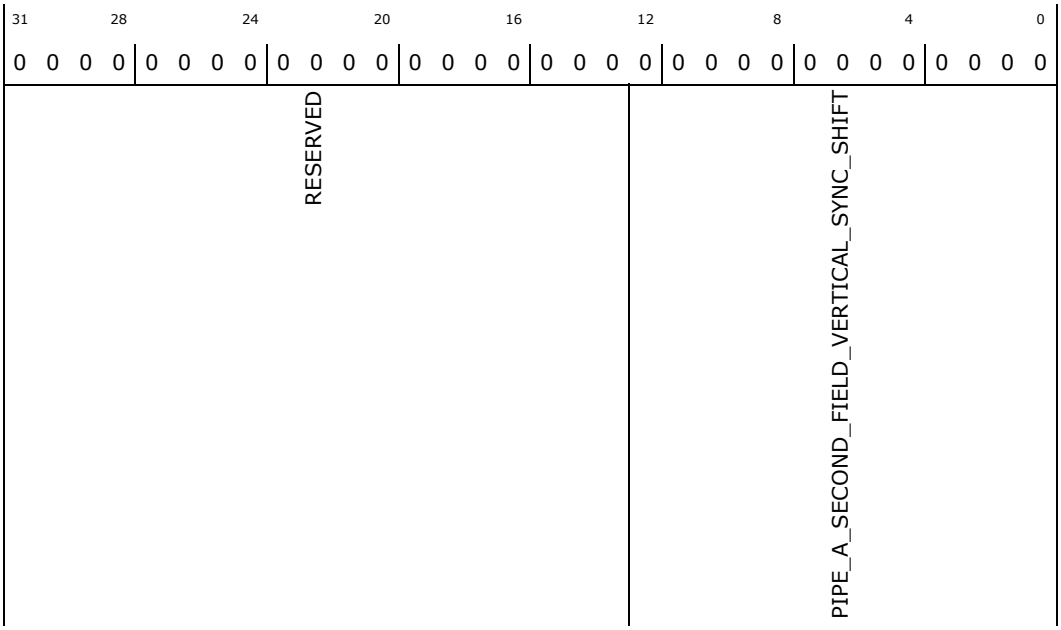
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VSYNCSHIFT_A: [GTTMMADR_LSB + 2BF20h] + 60028h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:13	0b RW	**RESERVED:** Write as zero.
12:0	0b RW	**PIPE_A_SECOND_FIELD_VERTICAL_SYNC_SHIFT:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the PIPEACONF is programmed to an interlaced mode using vsync shift. Otherwise a legacy value of floor[htotal / 2] will be used. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into registers). This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

3.1.159 TRANSADATAM1—Offset 60030h

Pipe A Data M value 1

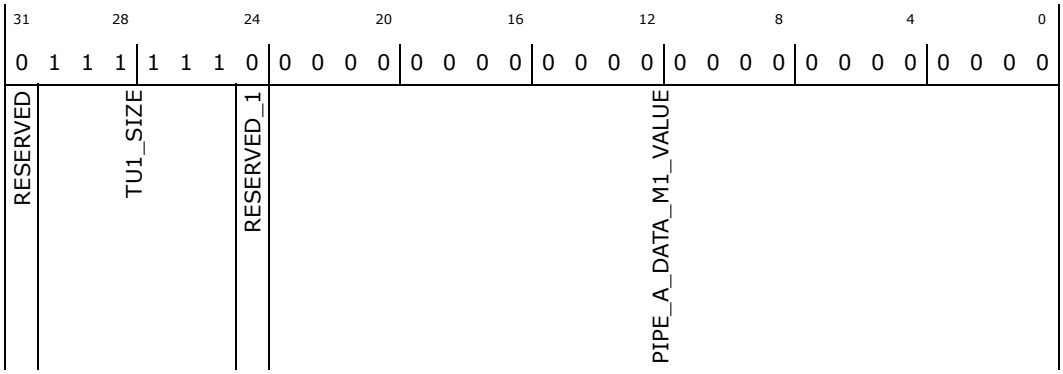
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSADATAM1: [GTTMMADR_LSB + 2BF20h] + 60030h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 7E000000h



Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:25	111111b RW	**TU1_SIZE:** Project: All This field is the size of the transfer unit for DP, minus one.
24	0b RW	**RESERVED_1:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_DATA_M1_VALUE:** Project: All This field is the M1 value for internal use of the DDA.

3.1.160 TRANSADATAN1—Offset 60034h

Pipe A Data N value 1

Access Method

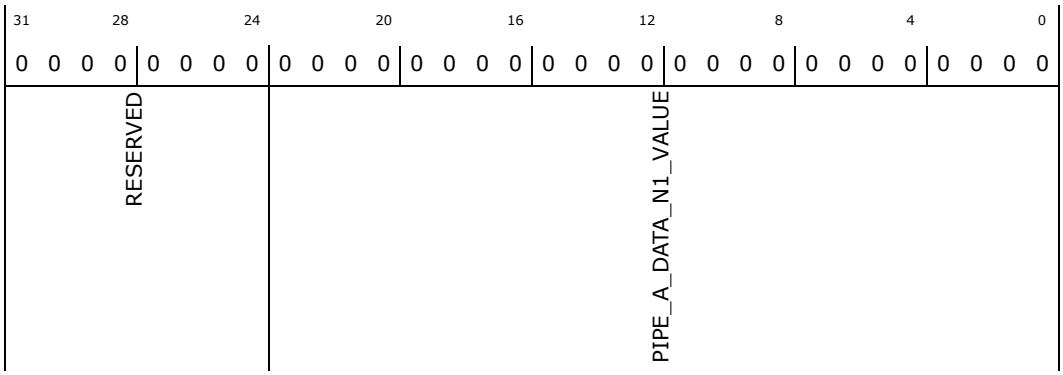
Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSADATAN1: [GTTMMADR_LSB + 2BF20h] + 60034h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_DATA_N1_VALUE:** Project: All This field is the N1 value for internal use of the DDA.

3.1.161 TRANSADATAM2—Offset 60038h

Pipe A Data M value 2

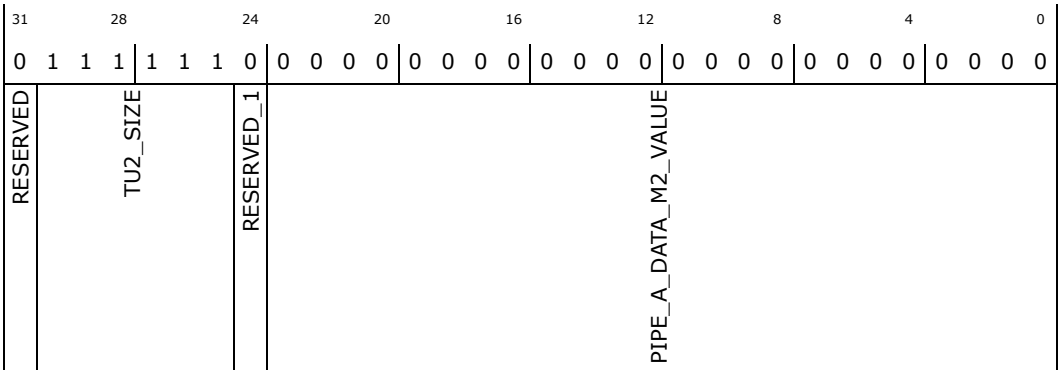
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSADATAM2: [GTTMMADR_LSB + 2BF20h] + 60038h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 7E000000h



Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:25	111111b RW	**TU2_SIZE:** Project: All Default Value: ;111111b 64 This field is the size of the transfer unit for DP, minus one.
24	0b RW	**RESERVED_1:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_DATA_M2_VALUE:** Project: All This field is the M2 value for internal use of the DDA.

3.1.162 TRANSADATAN2—Offset 6003Ch

Pipe A Data N value 2

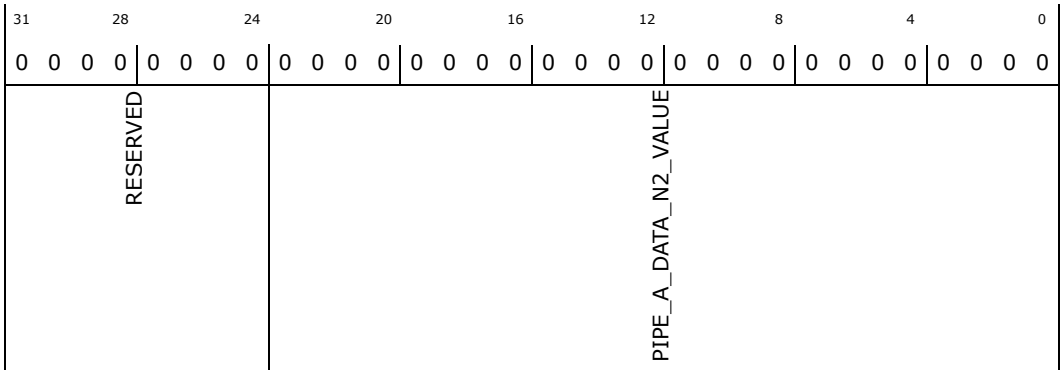
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSADATAN2: [GTTMMADR_LSB + 2BF20h] + 6003Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_DATA_N2_VALUE:** Project: All This field is the N2 value for internal use of the DDA.

3.1.163 TRANSADPLINKM1—Offset 60040h

Pipe A Link M value 1

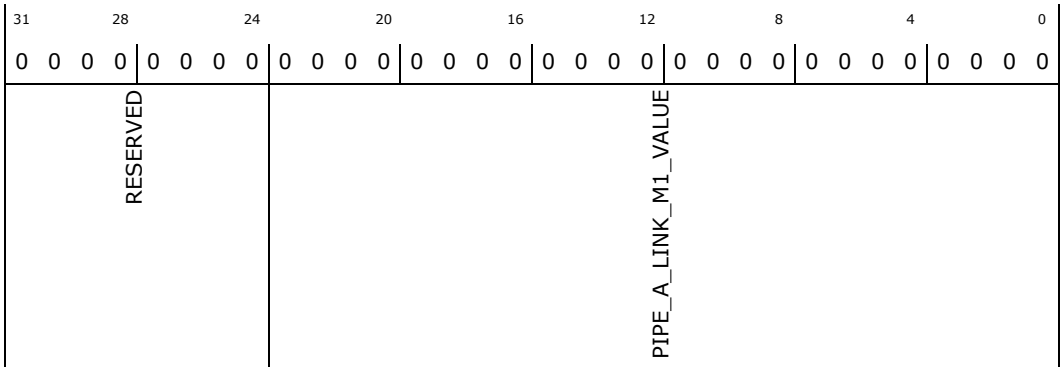
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSADPLINKM1: [GTTMMADR_LSB + 2BF20h] + 60040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_LINK_M1_VALUE:** Project: All This field is the M1 value for external transmission in the Main Stream Attributes.

3.1.164 TRANSADPLINKN1—Offset 60044h

Pipe A Link N value 1

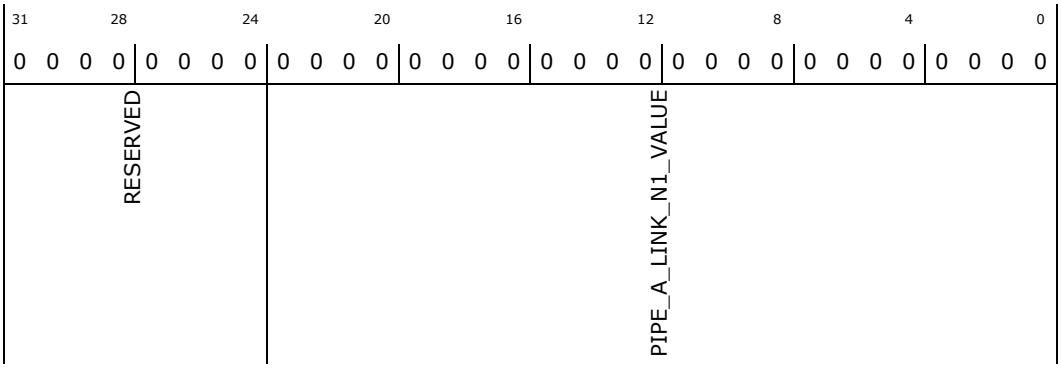
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSADPLINKN1: [GTTMMADR_LSB + 2BF20h] + 60044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_LINK_N1_VALUE:** Project: All This field is the N1 value for external transmission in the Main Stream Attributes and VB-ID.

3.1.165 TRANSADPLINKM2—Offset 60048h

Pipe A Link M value 2

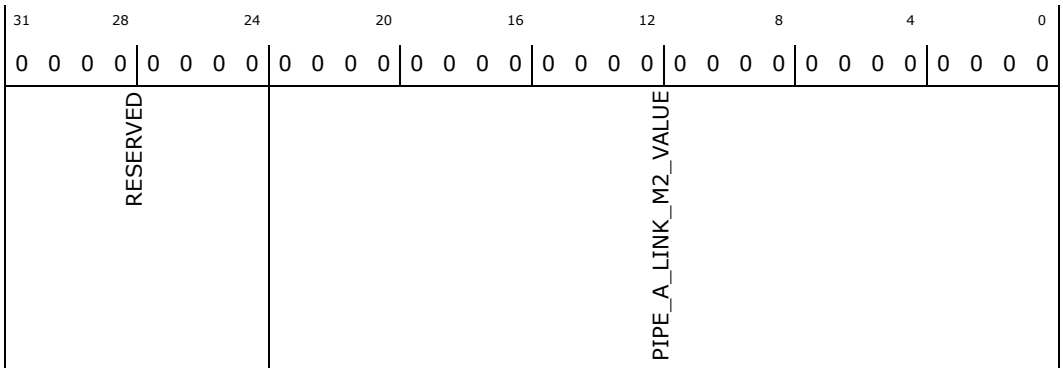
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSADPLINKM2: [GTTMMADR_LSB + 2BF20h] + 60048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_LINK_M2_VALUE:** Project: All This field is the M2 value for external transmission in the Main Stream Attributes.

3.1.166 TRANSADPLINKN2—Offset 6004Ch

Pipe A Link N value 2

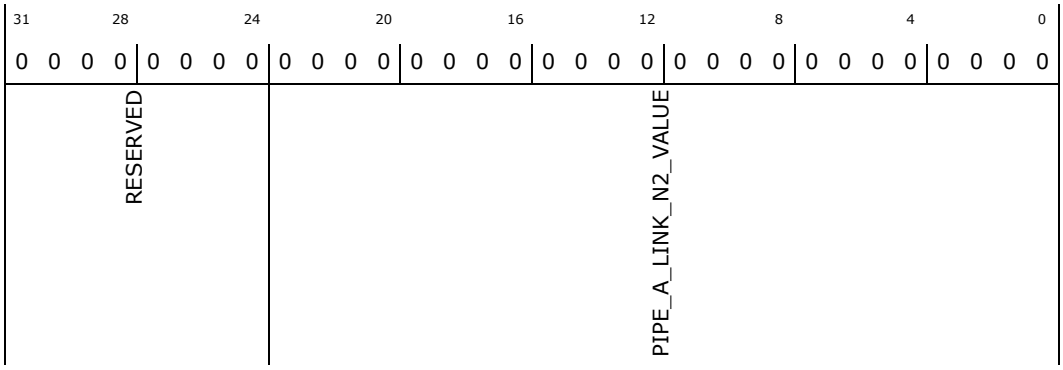
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSADPLINKN2: [GTTMMADR_LSB + 2BF20h] + 6004Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ

Bit Range	Default & Access	Description
23:0	0b RW	**PIPE_A_LINK_N2_VALUE:** Project: All This field is the N2 value for external transmission in the Main Stream Attributes and VB-ID.

3.1.167 CRCCTRLREDA—Offset 60050h

Pipe A CRC Color Channel Control Register (Red)

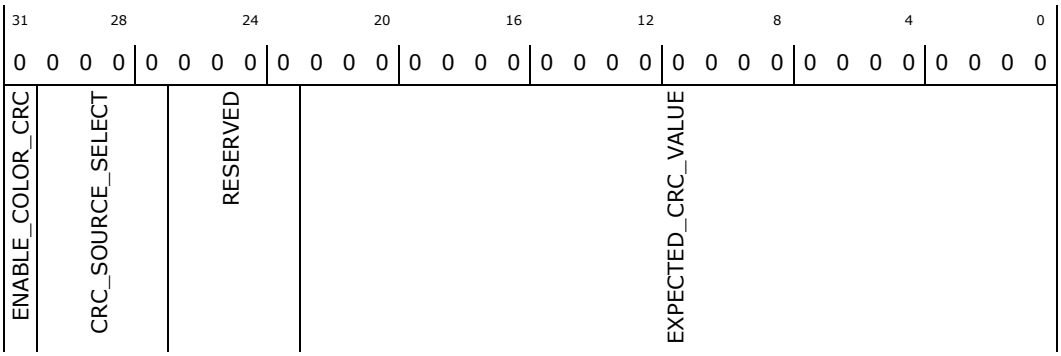
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCCTRLREDA: [GTTMMADR_LSB + 2BF20h] + 60050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**ENABLE_COLOR_CRC:** Enables the CRC calculations. After being enabled for the first time, you need to wait for two VBLANK events for a valid CRC result. After that, a CRC will be generated each frame. 0 = CRC Calculations are disabled 1 = CRC Calculations are enabled
30:27	0b RW	**CRC_SOURCE_SELECT:** These bits select the source of the data to put into the CRC logic. 0000: Pipe A (Not available when DisplayPort or TV is enabled on this pipe) [DevVLVP] 0001: sDVOB/HDMIB (30 bit format. Only select when HDMIB is set to pipeA) [DevVLVP] 0010: sDVOC/HDMIC (30 bit format. Only select when HDMIC is set to pipeA) [DevVLVP] 0011: DisplayPort D (40 bit format) [DevCTG] 0100: TV Encoder outputs (30 bit format) 0101: TV filter outputs (30 bit format) 0110: DisplayPort B (40 bit format) [DevCTG, DevCDV, DevVLVP] 0111: DisplayPort C (40 bit format) [DevCTG, DevCDV, DevVLVP] 1000: Audio DP (Audio for DisplayPort (pcdclk). Only select when Audio is on DisplayPort on Pipe A) [DevVLVP] 1001: Audio HDMI (Audio for HDMI (dotclock) Only select when Audio is on HDMI on Pipe A) Others: Reserved
26:23	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Description
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

3.1.168 CRCCTRLGREENA—Offset 60054h

Pipe A CRC Color Channel Control Register (, Residual)

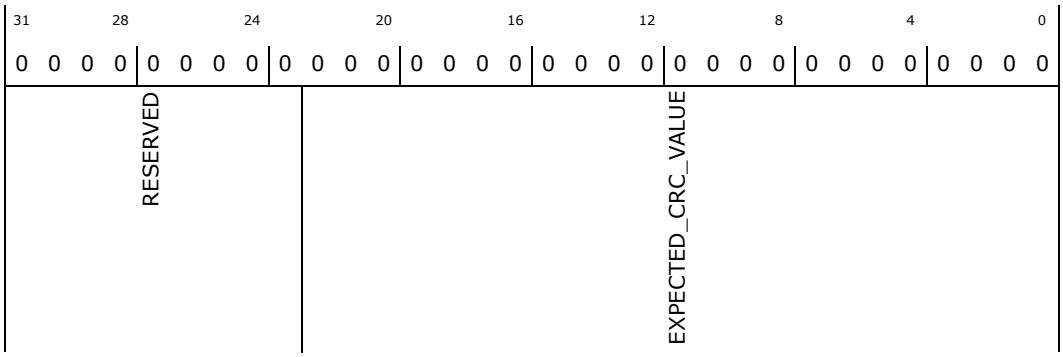
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCCTRLGREENA: [GTTMMADR_LSB + 2BF20h] + 60054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

3.1.169 CRCCTRLBLUEA—Offset 60058h

Pipe A CRC Color Channel Control Register

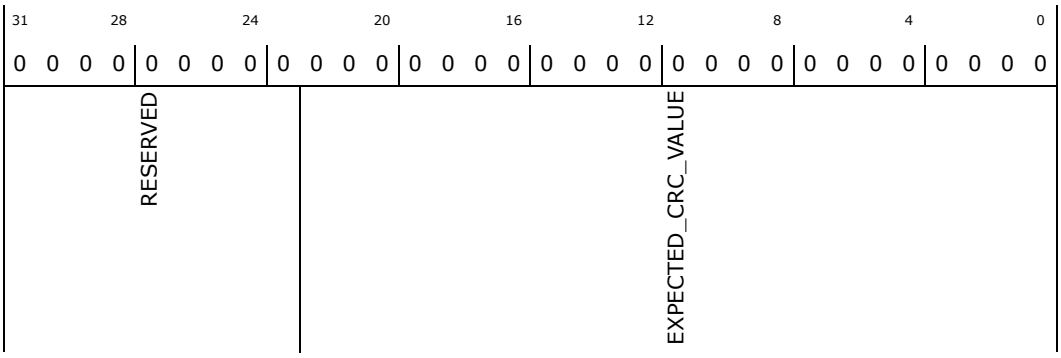
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCCTRLBLUEA: [GTTMMADR_LSB + 2BF20h] + 60058h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

3.1.170 CRCCTRLALPHAA—Offset 6005Ch

Pipe A CRC Color Channel Control Register

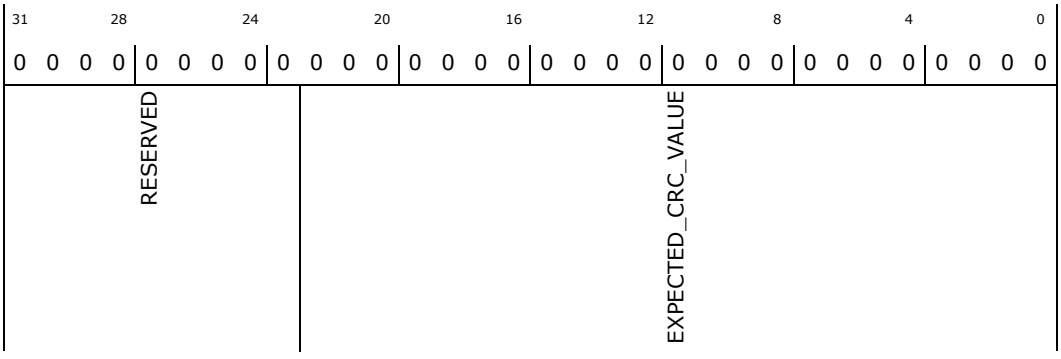
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCCTRLALPHAA: [GTTMMADR_LSB + 2BF20h] + 6005Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Description
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

3.1.171 CRCRESREDA—Offset 60060h

Pipe A A CRC Color Channel Result Register

Access Method

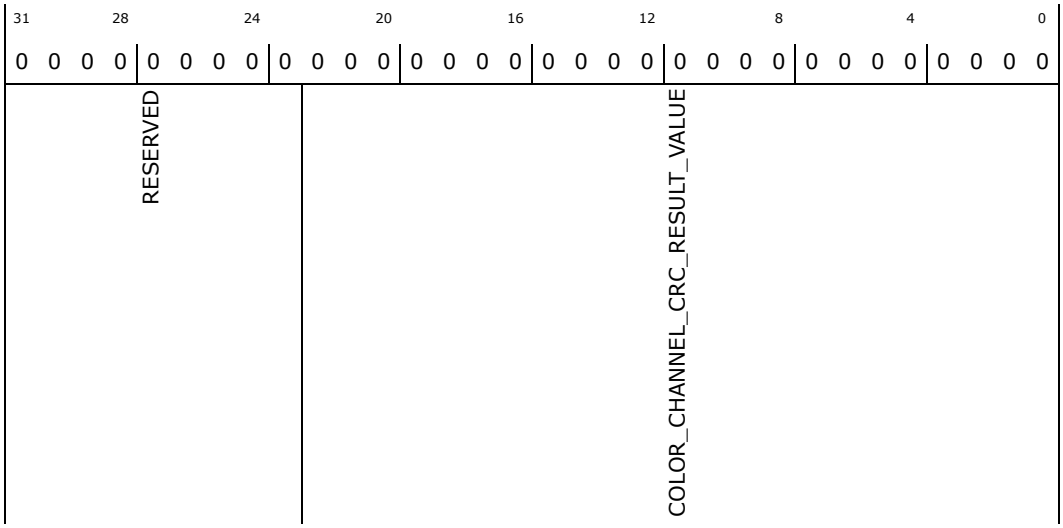
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCRESREDA: [GTTMMADR_LSB + 2BF20h] + 60060h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

3.1.172 CRCRESGREENA—Offset 60064h

Pipe A A CRC Color Channel Result Register

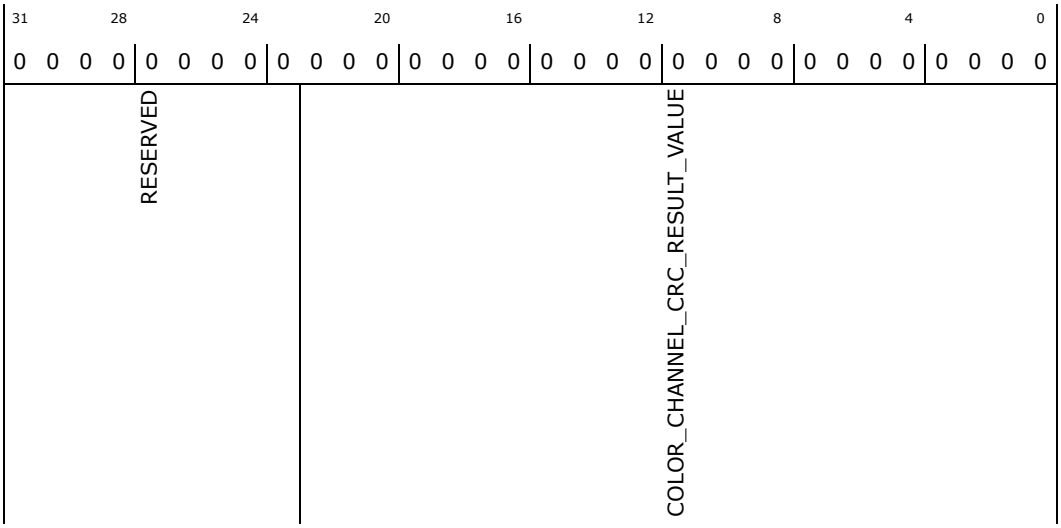
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCRESGREENA: [GTTMMADR_LSB + 2BF20h] + 60064h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

3.1.173 CRCRESBLUEA—Offset 60068h

Pipe A A CRC Color Channel Result Register

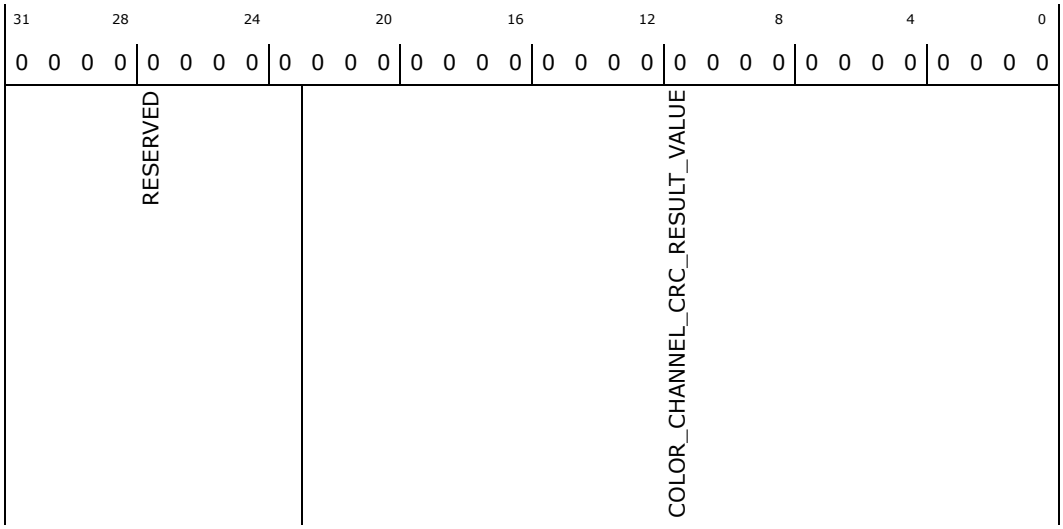
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCRESBLUEA: [GTTMMADR_LSB + 2BF20h] + 60068h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

3.1.174 CRCRESALPHAA—Offset 6006Ch

Pipe A A CRC Color Channel Result Register

Access Method

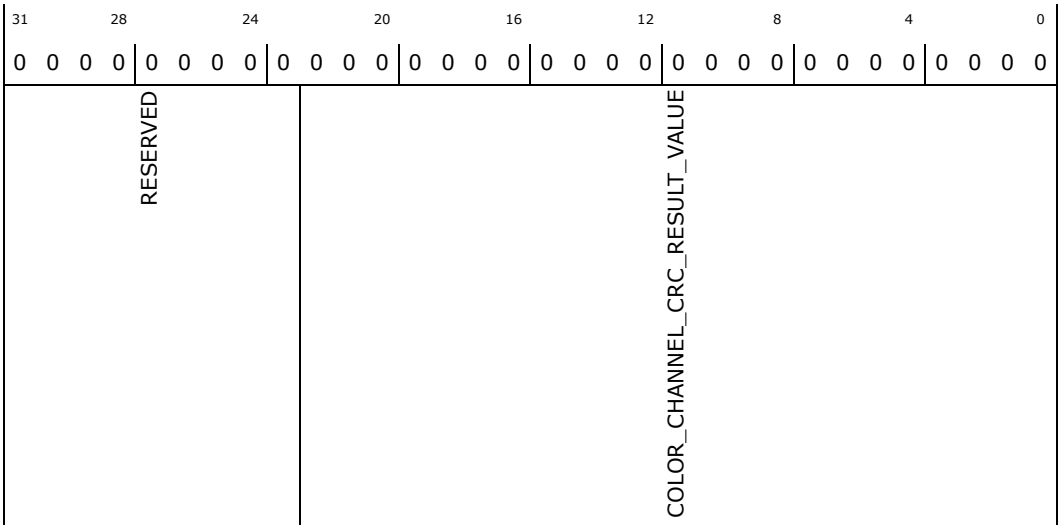
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCRESALPHAA: [GTTMMADR_LSB + 2BF20h] + 6006Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

3.1.175 CRCCTRLRESIDUE2A—Offset 60070h

Pipe A CRC Color Channel Control Register

Access Method

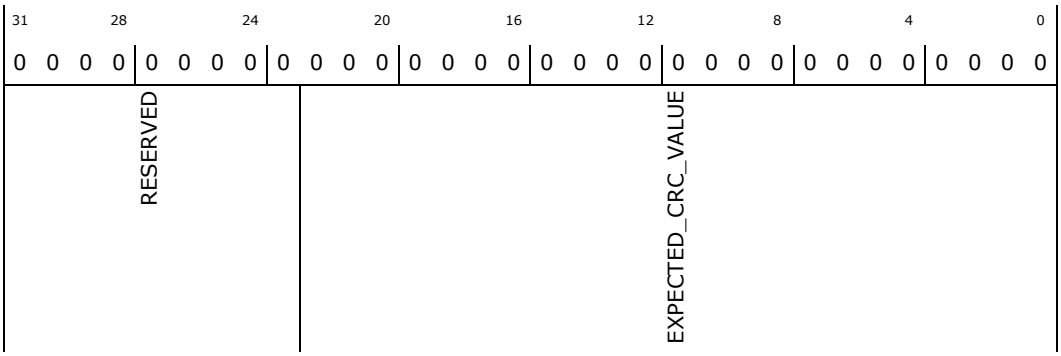
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCCTRLRESIDUE2A: [GTTMMADR_LSB + 2BF20h] + 60070h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

3.1.176 CRCRESRESIDUE2A—Offset 60080h

Pipe A CRC Color Channel Result Register

Access Method

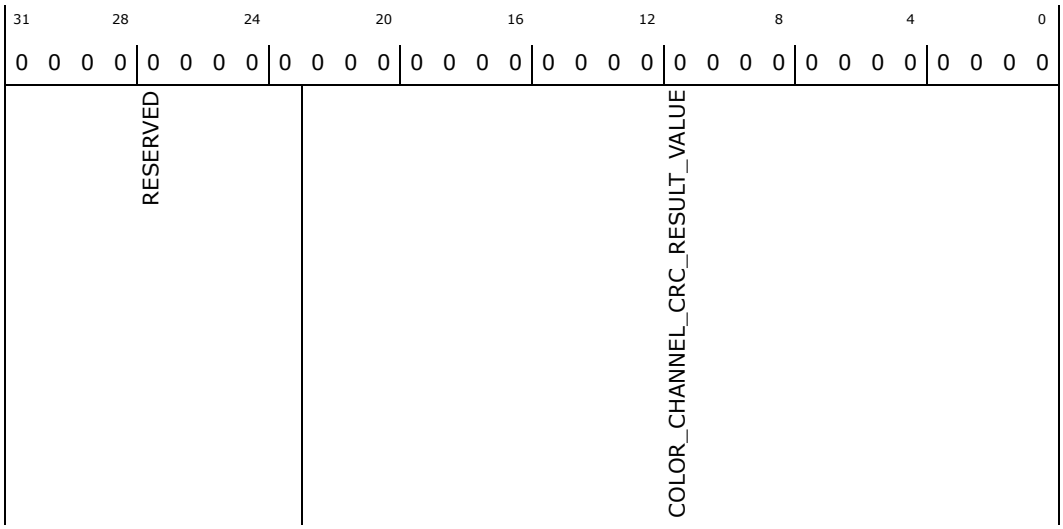
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCRESRESIDUE2A: [GTTMMADR_LSB + 2BF20h] + 60080h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

3.1.177 PSRCTLA—Offset 60090h

Pipe A Panel Self Refresh Control

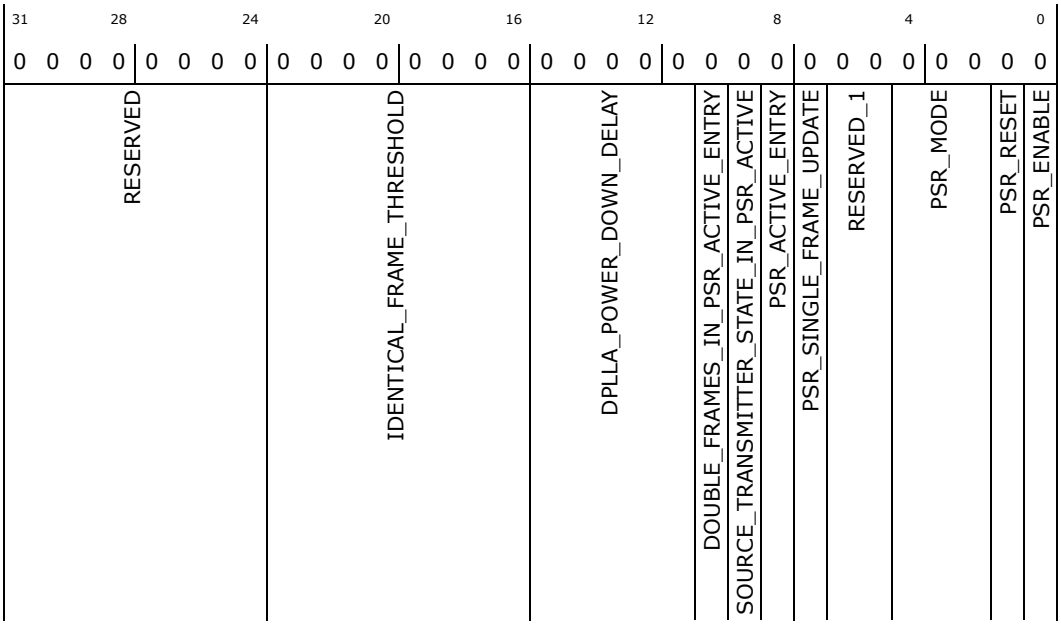
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PSRCTLA: [GTTMMADR_LSB + 2BF20h] + 60090h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**IDENTICAL_FRAME_THRESHOLD:** : Number of identical frames that display controller needs to exceed in order to transition to PSR active state in HW timer mode
15:11	0b RW	**DPLLA_POWER_DOWN_DELAY:** programmable delay from main link powerdown to DPLLA powerdown. The delay is in number of cdclk clocks.
10	0b RW	**DOUBLE_FRAMES_IN_PSR_ACTIVE_ENTRY:** . If asserted, HW will send two frames with same SDP active setting when entry PSR active state. This bit is set if the vertical blanking time is less than 330us.
9	0b RW	**SOURCE_TRANSMITTER_STATE_IN_PSR_ACTIVE:** . If asserted, HW will keep transmitter active during PSR active state and sends only idle symbols. If deasserted, HW will turn off transmitter during PSR active state. Display driver will keep this bit consistent with Source transmitter state in PSR active bit in DPCD register of the sink.

Bit Range	Default & Access	Description
8	0b RW	**PSR_ACTIVE_ENTRY:** This bit is only valid in PSR_mode is SW timer mode. If it is asserted, HW will transition into PSR_active state. If it is deasserted, HW will transition to PSR_inactive state. SW should not set or clear this bit more than once within one vblank period.
7	0b RW	**PSR_SINGLE_FRAME_UPDATE:** In PSR persistent mode, SW set this bit before writing registers for a flip. After HW finishes single frame update, it goes back to PSR active ? no RFB state. SW driver may send new single frame update request. Programming note: Reading this bit is updated at the next vblank. Writing this bit to 1 will cause PSR FSM to perform single frame update automatically, no vblank is required. When single frame update is done, it will automatically go back to PSR active ? no RFB update. 60094[2:0] = 3b011.
6:5	0b RW	**RESERVED_1:** Reserved.
4:2	0b RW	**PSR_MODE:** b011-111: reserved. b010: PSR with HW timer. HW timer decides PSR active entry point. PSR active state exits upon MMIO write registers that may change the frame buffer. b001: PSR with SW timer. In this mode, SW will keep track of idle frames and buffer modification in the driver and explicitly specify the entry and exit PSR active state point. b000: PSR manual (debug) mode. All of PSR state transitions and SDP content is managed by SW driver. SW is responsible to change SDP content for every frame with appropriate values to keep PSR panel in synchronized states.
1	0b RW	**PSR_RESET:** If assert all PSR functions are reset back to PSR inactive state. When it needs to re synchronize source and sync, SW writes 0x2 to DPCD register 600h and to this bit to get system back to PSR active states. This bit is self clear.
0	0b RW	**PSR_ENABLE:** Panel Self-refresh is enabled. When it is asserted PSR is enabled and operate in one of the mode that specified by PSR mode.

3.1.178 PSRSTATA—Offset 60094h

Pipe A PSR status register

Access Method

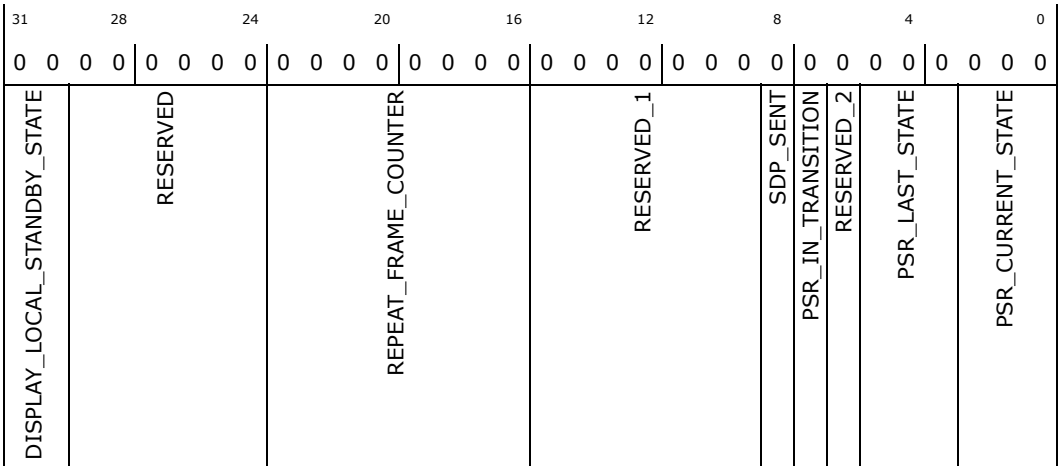
Type: Memory Mapped I/O Register (Size: 32 bits)

PSRSTATA: [GTTMMADR_LSB + 2BF20h] + 60094h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RO	**DISPLAY_LOCAL_STANDBY_STATE:** :00: D0 idle state, fetch frame buffer from system memory 01: D0i1 not defined in VLVP 02: D0i2 PSR is active, display controller is trunk gated 03: D0i3 PSR is active, display controller is power gated
29:24	0b RO	**RESERVED:** Reserved.
23:16	0b RO	**REPEAT_FRAME_COUNTER:** : Number of identical frames has been sent by display controller. Value is not roll over at 255.
15:9	0b RO	**RESERVED_1:** Reserved.
8	0b RO	**SDP_SENT:** it indicates if SDP packet has been sent in current frame.
7	0b RO	**PSR_IN_TRANSITION:** There is a period that source already committed to PSR active but sink did not. SW should not change the source state at this time but wait until this status bit is clear. The wait time should in the range of 120-250us in the worst case.
6	0b RO	**RESERVED_2:** Reserved.
5:3	0b RO	**PSR_LAST_STATE:** indicate last source state that VLVP PSR state machine were in (debug) 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit
2:0	0b RO	**PSR_CURRENT_STATE:** indicate current source state that VLVP PSR state machine are in 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit

3.1.179 PSRCRC1A—Offset 60098h

Pipe A PSR CRC1 register

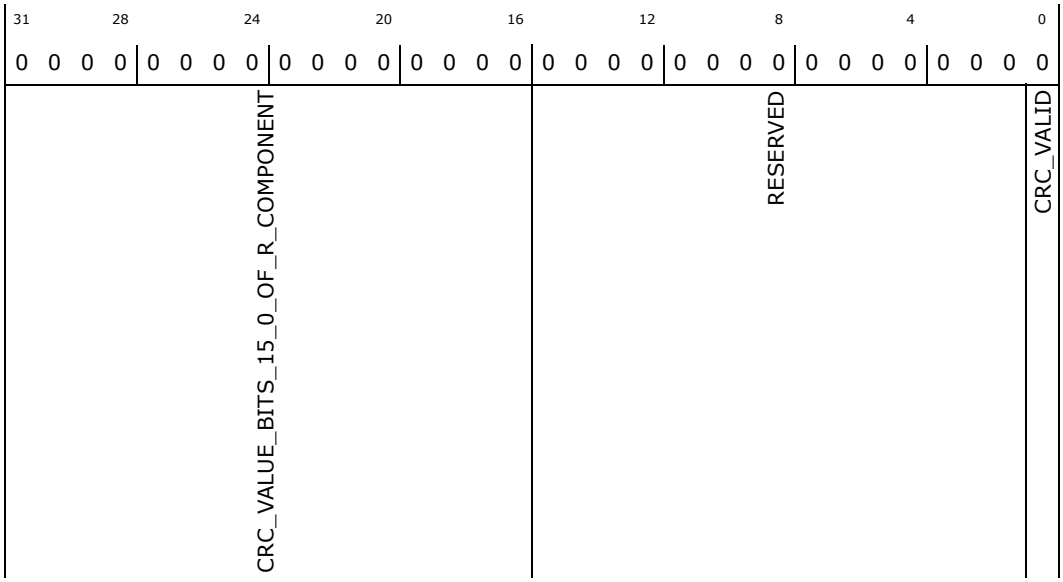
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PSRCRC1A: [GTTMMADR_LSB + 2BF20h] + 60098h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**CRC_VALUE_BITS_15_0_OF_R_COMPONENT:** crc values bits 15 to 0 of Red component
15:1	0b RO	**RESERVED:** Reserved.
0	0b RO	**CRC_VALID:** CRC calculation complete and valid for previous frame.

3.1.180 PSRCRC2A—Offset 6009Ch

Pipe A PSR CRC2 register

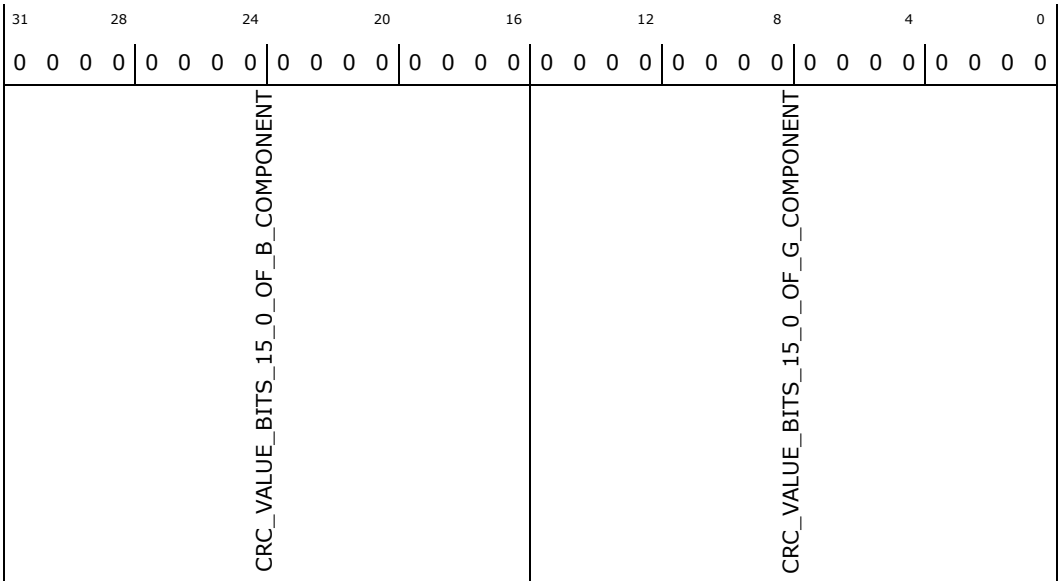
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PSRCRC2A: [GTTMMADR_LSB + 2BF20h] + 6009Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**CRC_VALUE_BITS_15_0_OF_B_COMPONENT:** crc values bits 15 to 0 of Blue component
15:0	0b RO	**CRC_VALUE_BITS_15_0_OF_G_COMPONENT:** crc values bits 15 to 0 of green component

3.1.181 VSCSDPA—Offset 600A0h

Pipe A VSC SDP register

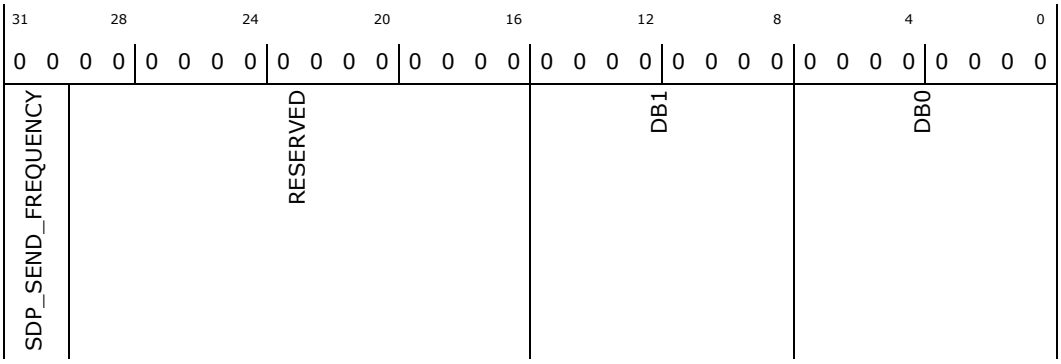
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VSCSDPA: [GTTMMADR_LSB + 2BF20h] + 600A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RW	**SDP_SEND_FREQUENCY:** 00: off, not sending 01: send one every frame 10: send once 11: reserved Programming note: This field shall be programmed either send once or send one every frame when SW driver sets PSR active entry bit. When PSR is enabling this field is ignored. One SDP is sent in every frame until source is in PSR active state
29:16	0b RW	**RESERVED:** Reserved.
15:8	0b RW	**DB1:** : Programmed by display driver in manual mode, auto-generate by display controller in all other modes
7:0	0b RW	**DB0:** : Bits 7:4: Stereo Interface Method Specific ParameterBits 3:0: Stereo Interface Method Code. This field is programmed by display driver for stereo display configuration

3.1.182 PIPEAWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 600B0h

When color correction matrix enable bit is set in PIPEACONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix like gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Access Method

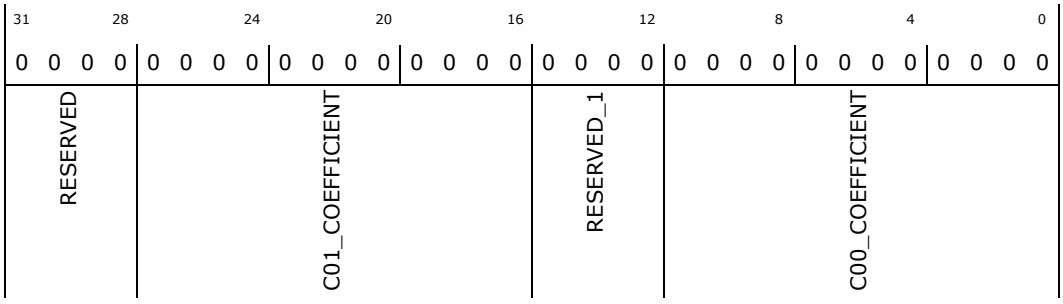
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS: [GTTMMADR_LSB + 2BF20h] + 600B0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
27:16	0b RW	**C01_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.
11:0	0b RW	**C00_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.1.183 PIPEAWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 600B4h

Refer to the description of the Pipe A Wide Gamut Color Correction C01_C00 register.

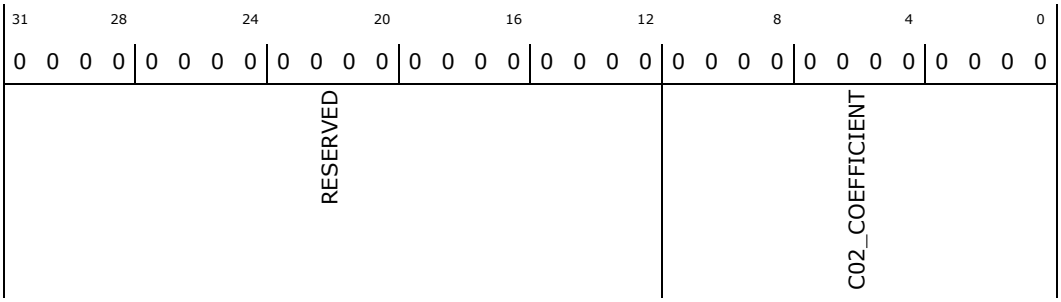
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT: [GTTMMADR_LSB + 2BF20h] + 600B4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C02_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.1.184 PIPEAWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 600B8h

Refer to the description of the Pipe A Wide Gamut Color Correction C01_C00 register.

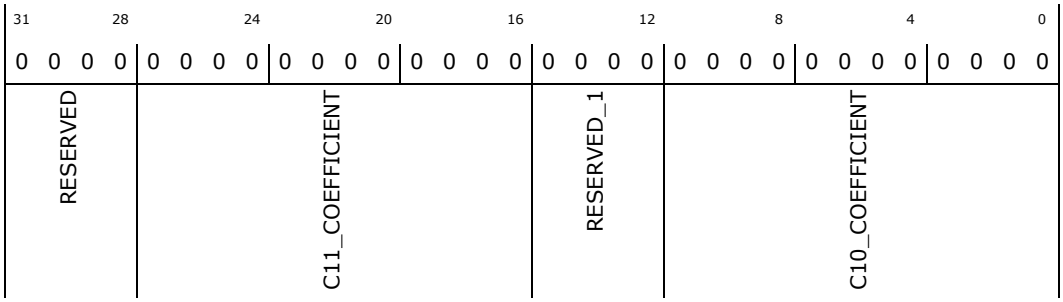
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS: [GTTMMADR_LSB + 2BF20h] + 600B8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Reserved.
27:16	0b RW	**C11_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.
11:0	0b RW	**C10_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.1.185 PIPEAWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 600BCh

Refer to the description of the Pipe A Wide Gamut Color Correction C01_C00 register.

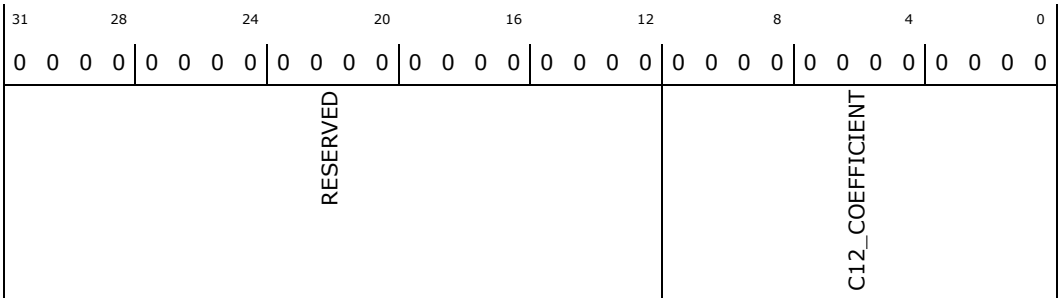
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT: [GTTMMADR_LSB + 2BF20h] + 600BCh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C12_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.1.186 PIPEAWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 600C0h

Refer to the description of the Pipe A Wide Gamut Color Correction C01_C00 register.

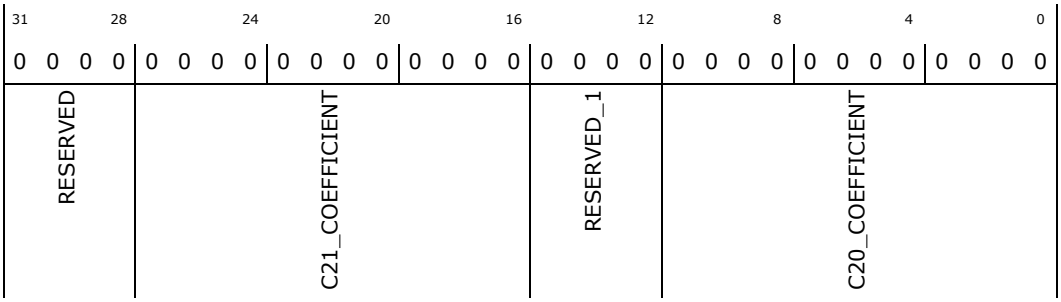
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS: [GTTMMADR_LSB + 2BF20h] + 600C0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Reserved.
27:16	0b RW	**C21_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.

Bit Range	Default & Access	Description
11:0	0b RW	**C20_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.1.187 PIPEAWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 600C4h

Refer to the description of the Pipe A Wide Gamut Color Correction C01_C00 register.

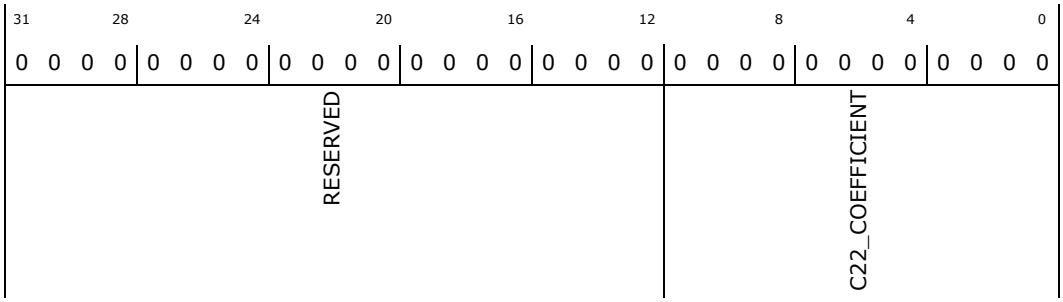
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT: [GTTMMADR_LSB + 2BF20h] + 600C4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C22_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.1.188 VIDEO_DIP_CTL_A—Offset 60200h

Video DIP Control for Pipe A

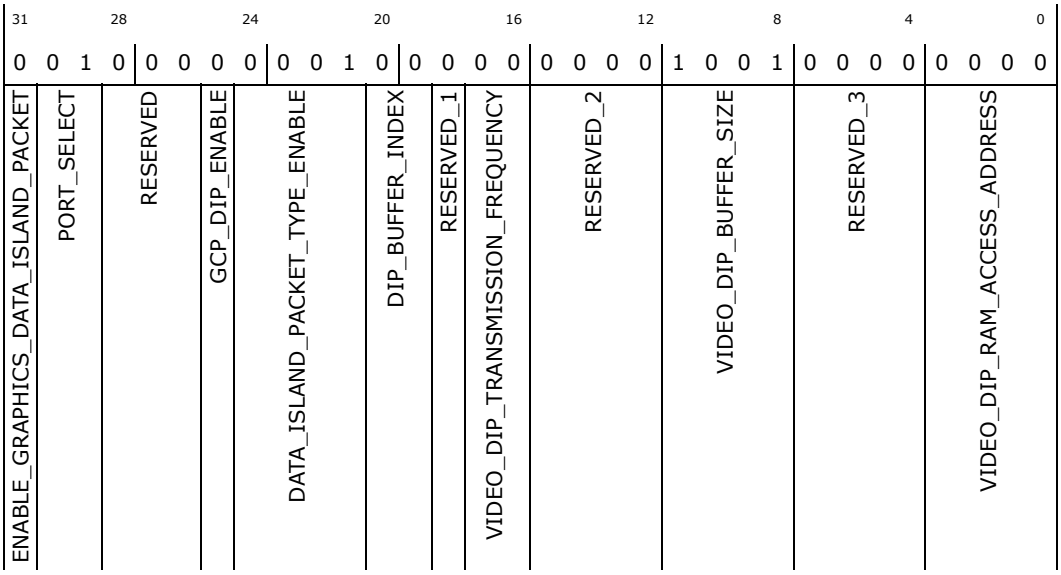
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VIDEO_DIP_CTL_A: [GTTMMADR_LSB + 2BF20h] + 60200h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 20200900h



Bit Range	Default & Access	Description
31	0b RW	**ENABLE_GRAPHICS_DATA_ISLAND_PACKET:** mode (bit #9 of port control register) overrides this behavior.
30:29	01b RW	**PORT_SELECT:** Project: All Default Value: 01b Digital Port B This selects which port is to transmit the data island. This field must not be changed while data island transmission is enabled. Value Name Description Project 00b Reserved Reserved All 01b Digital Port B Digital Port B (Default) All 10b Digital Port C Digital Port C All 11b Reserved Reserved All
28:26	0b RW	**RESERVED:** Project: All Format:
25	0b RW	**GCP_DIP_ENABLE:** Project: All Default Value: 0b This bit enables the output of the General Control Packet. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore a DIP buffer for GCP is not needed. Please refer to the GCP payload register for payload details. Writes to this bit take effect immediately. This bit should not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode. Value Name Description Project 0b Disable GCP DIP disabled All 1b Enable GCP DIP enabled All
24:21	0001b RW	**DATA_ISLAND_PACKET_TYPE_ENABLE:** Project: All Default Value: 0001b Enable AVI DIP These bits enable the output of a given data island packet (DIP) type. It can be updated while the port is enabled and is immediately updated (not double-buffered). Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Value Name Description Project XXX1b Enable AVI Enable AVI DIP (Default = enabled) All XX1Xb Enable Vendor Enable Vendor-specific DIP (Default = disabled) All X1XXb Enable Gamut Enable Gamut Metadata Packet (Default = disabled) All 1XXXb Enable Source Enable Source Product Description DIP (Default = disabled) All

Bit Range	Default & Access	Description
20:19	0b RW	**DIP_BUFFER_INDEX:** Project: All Default Value: 00b This field is used during programming of different DIPs. These bits are used as an index to their respective DIP buffers. The transmission frequency must also be written when programming the buffer. Value Name Description Project 00b AVI AVI DIP (31 bytes of space available) All 01b Vendor-specific Vendor-specific DIP All 10b Reserved Reserved All 11b Source Product Source Product Description DIP All
18	0b RW	**RESERVED_1:** Project: All Format:
17:16	0b RW	**VIDEO_DIP_TRANSMISSION_FREQUENCY:** Project: All Default Value: 00b These bits dictate the frequency of Video DIP transmission for the DIP buffer index designated in bits 20:19. When writing Video DIP data, this value is also latched when the first DW of the Video DIP is written. When read, this value reflects the Video DIP transmission frequency for the Video DIP buffer designated in bits 20:19. This field shall be ignored for Gamut Metadata Packet transmission. Value Name Description Project 00b Send Once Send Once All 01b Every VSync Send Every VSync (Default for AVI) All 10b Every Other Vsync Send at least every other VSync All 11b Reserved Reserved All
15:12	0b RW	**RESERVED_2:** Project: All Format: MBZ
11:8	1001b RO	**VIDEO_DIP_BUFFER_SIZE:** Project: All AccessType: Read Only Default Value: ;1001b This reflects the buffer size in dwords available for the type of Video DIP being indexed by bits 20:19 of this register, including the header. It is hardwired to the maximum size of a Video DIP, 36 bytes. Please note that this count includes ECC bytes, which are not writable by software. These bits are immediately valid after write of the DIP index.
7:4	0b RW	**RESERVED_3:** Project: All Format: MBZ
3:0	0b RO	**VIDEO_DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read Only Selects the DWORD address for access to the Video DIP buffers. This value is automatically incremented after each read or write of the Video DIP Data Register. The value wraps back to zero when it auto increments past the max address value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

3.1.189 VIDEO_DIP_DATA_A—Offset 60208h

Video Data Island Packet Data for Pipe A

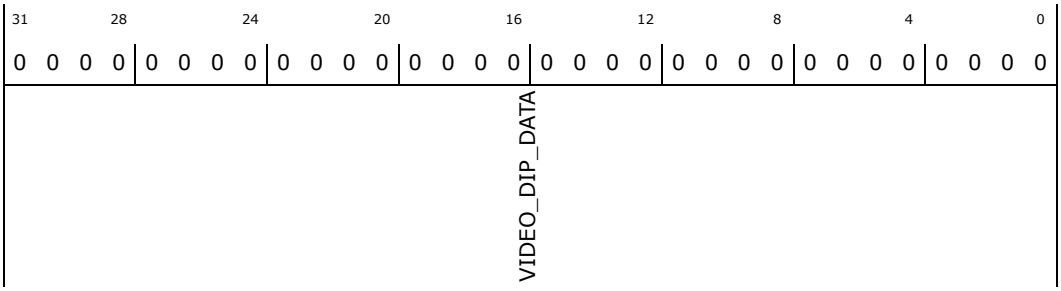
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VIDEO_DIP_DATA_A: [GTTMMADR_LSB + 2BF20h] + 60208h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**VIDEO_DIP_DATA:** Project: All When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis.

3.1.190 VIDEO_DIP_GDCP_PAYLOAD_A—Offset 60210h

Video Data Island Payload for Pipe A

Access Method

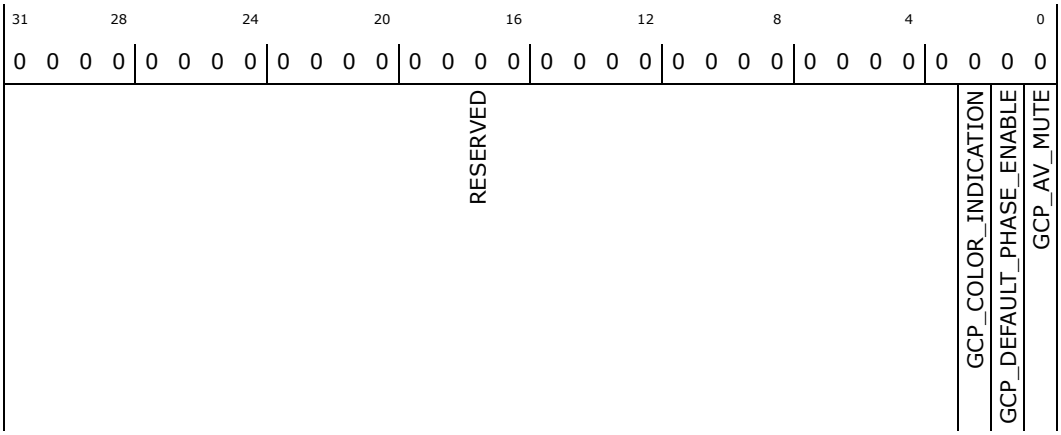
Type: Memory Mapped I/O Register (Size: 32 bits)

VIDEO_DIP_GDCP_PAYLOAD_A: [GTTMMADR_LSB + 2BF20h] + 60210h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**RESERVED:** Project: All Format: MBZ
2	0b RW	**GCP_COLOR_INDICATION:** Project: All Default Value: 0b This bit must be set when in deep color mode. It may optionally be set for 24-bit mode. It must be set if the sink attached to Pipe A can receive GCP data. Value Name Description Project 0b Do not Indicate do not indicate color depth. CD and PP bits in GCP set to zero All 1b Indicate Indicate color depth using CD bits in GCP. It will be set depending on programmed pixel depth in port control register All
1	0b RW	**GCP_DEFAULT_PHASE_ENABLE:** Project: All Default Value: 0b Indicates the video timings meet alignment requirements such that the following conditions are met: Htotal is an even number Hactive is an even number Hsync is an even number Front and back porches for Hsync are even numbers Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0) Value Name Description Project 0b Clear Default phase bit in GCP is cleared All 1b Require Met Default phase bit in GCP is set. All requirements must be met before setting this bit All
0	0b RW	**GCP_AV_MUTE:** Project: All Default Value: 0b Set AV mute bit in GCP Value Name Description Project 0b Clear AV mute bit in GCP is cleared. When this bit transitions to 0, the AV mute clear flag is sent in the next GCP packet All 1b Set AV mute bit in GCP is set. When this bit transitions to 1, the AV mute set flag is sent in the next GCP packet All

3.1.191 HTOTAL_B—Offset 61000h

Pipe B Horizontal Total Register

Access Method

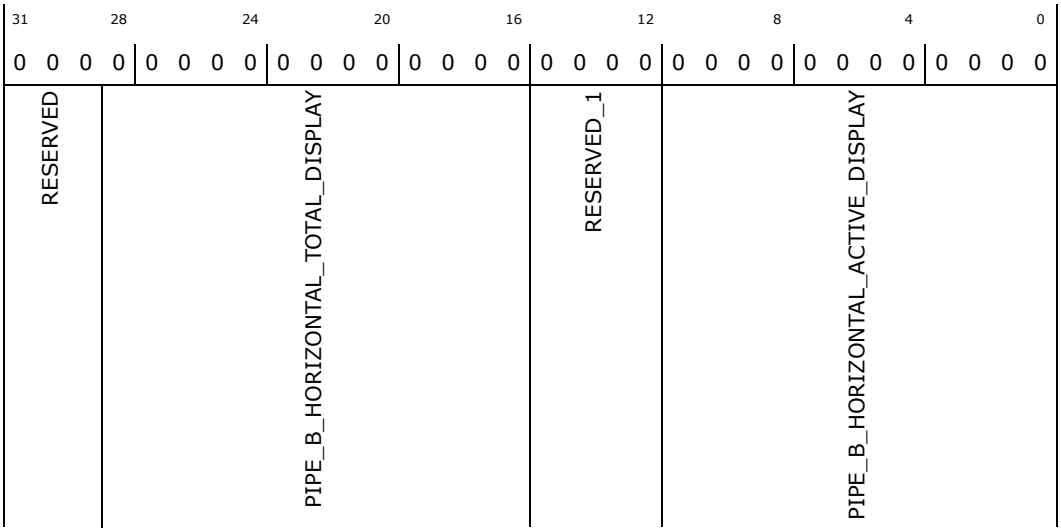
Type: Memory Mapped I/O Register (Size: 32 bits)

HTOTAL_B: [GTTMMADR_LSB + 2BF20h] + 61000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_B_HORIZONTAL_TOTAL_DISPLAY:** See pipe A description.
15:12	0b RW	**RESERVED_1:** Write as zero.
11:0	0b RW	**PIPE_B_HORIZONTAL_ACTIVE_DISPLAY:** See pipe A description

3.1.192 HBLANK_B—Offset 61004h

Pipe B Horizontal Blank Register

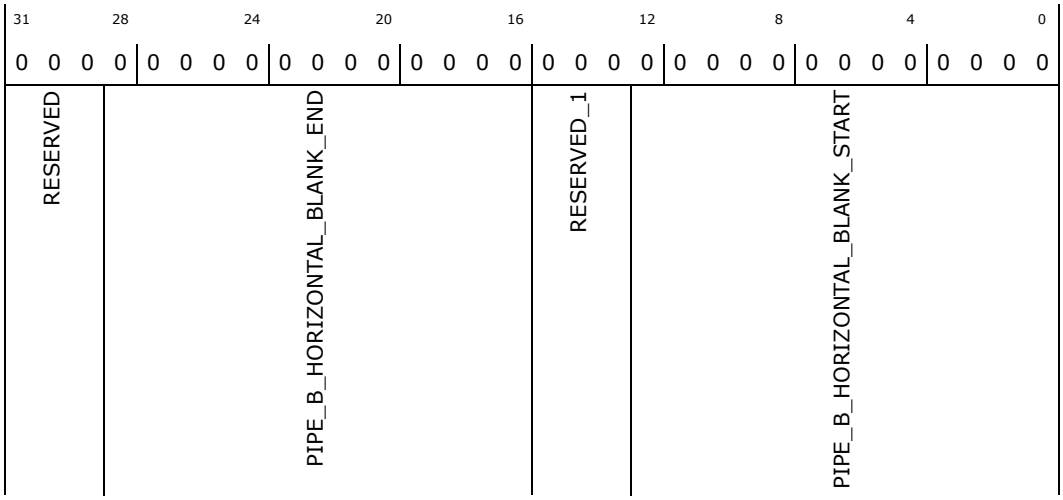
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HBLANK_B: [GTTMMADR_LSB + 2BF20h] + 61004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** . Write as zero.
28:16	0b RW	**PIPE_B_HORIZONTAL_BLANK_END:** See pipe A description
15:13	0b RW	**RESERVED_1:** Write as zero.
12:0	0b RW	**PIPE_B_HORIZONTAL_BLANK_START:** See pipe A description.

3.1.193 HSYNC_B—Offset 61008h

Pipe B Horizontal Sync Register

Access Method

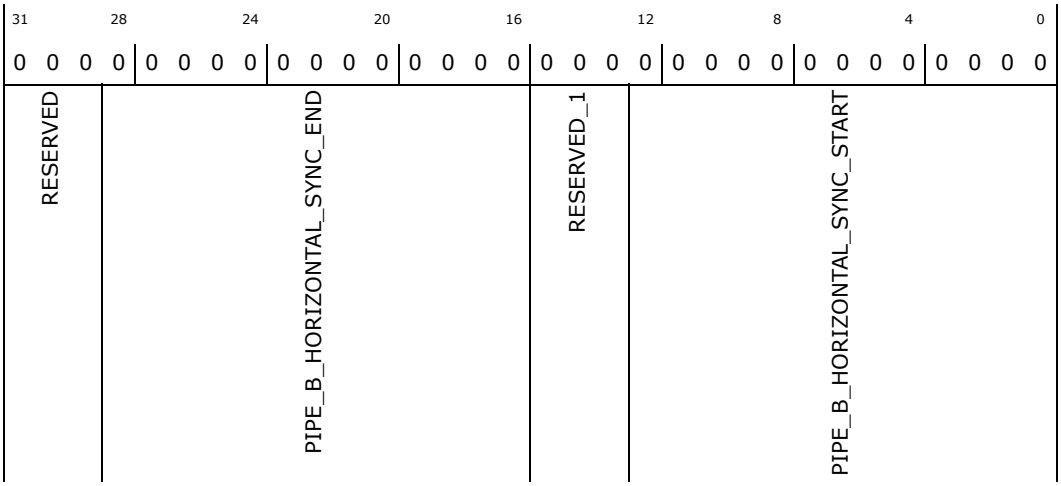
Type: Memory Mapped I/O Register (Size: 32 bits)

HSYNC_B: [GTTMMADR_LSB + 2BF20h] + 61008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_B_HORIZONTAL_SYNC_END:** See pipe A description.
15:13	0b RW	**RESERVED_1:** Write as zero.
12:0	0b RW	**PIPE_B_HORIZONTAL_SYNC_START:** See pipe A description

3.1.194 VTOTAL_B—Offset 6100Ch

Pipe B Vertical Total Register

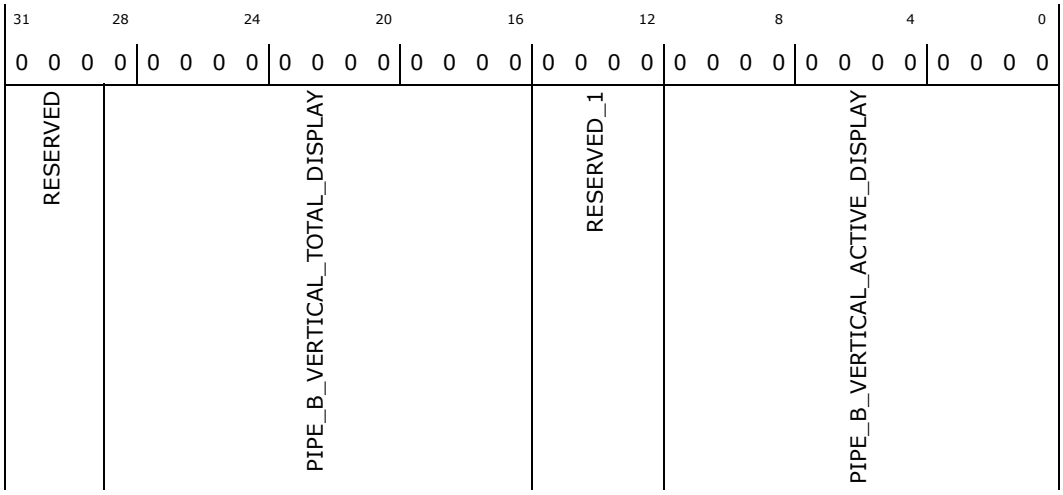
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VTOTAL_B: [GTTMMADR_LSB + 2BF20h] + 6100Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_B_VERTICAL_TOTAL_DISPLAY:** See pipe A description.
15:12	0b RW	**RESERVED_1:** Write as zero.
11:0	0b RW	**PIPE_B_VERTICAL_ACTIVE_DISPLAY:** See pipe A description.

3.1.195 VBLANK_B—Offset 61010h

Pipe B Vertical Blank Register

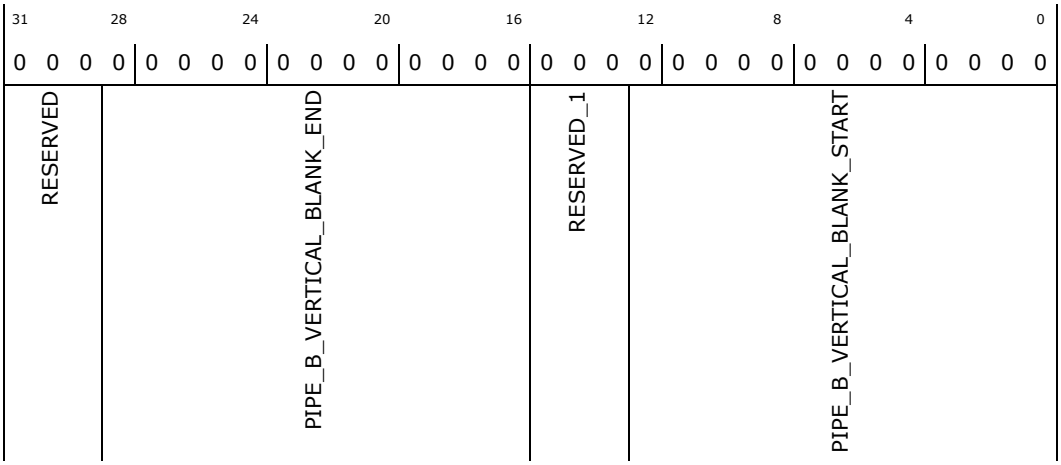
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VBLANK_B: [GTTMMADR_LSB + 2BF20h] + 61010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_B_VERTICAL_BLANK_END:** See pipe A description.
15:13	0b RW	**RESERVED_1:** Write as zero.
12:0	0b RW	**PIPE_B_VERTICAL_BLANK_START:** See pipe A description.

3.1.196 VSYNC_B—Offset 61014h

Pipe B Vertical Sync Register

Access Method

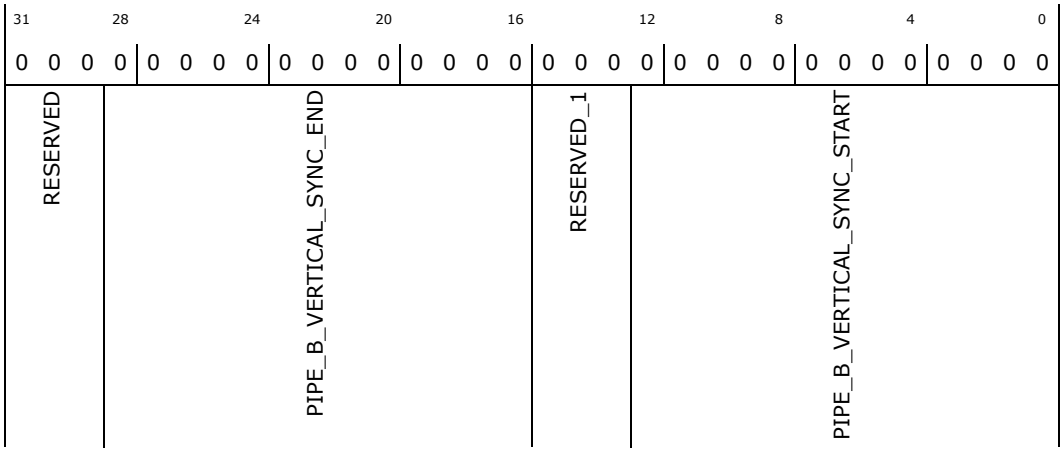
Type: Memory Mapped I/O Register (Size: 32 bits)

VSYNC_B: [GTTMMADR_LSB + 2BF20h] + 61014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_B_VERTICAL_SYNC_END:** See pipe A description.
15:13	0b RW	**RESERVED_1:** Write as zero.
12:0	0b RW	**PIPE_B_VERTICAL_SYNC_START:** See pipe A description.

3.1.197 PIPEBSRC—Offset 6101Ch

Pipe B Source Image Size

Access Method

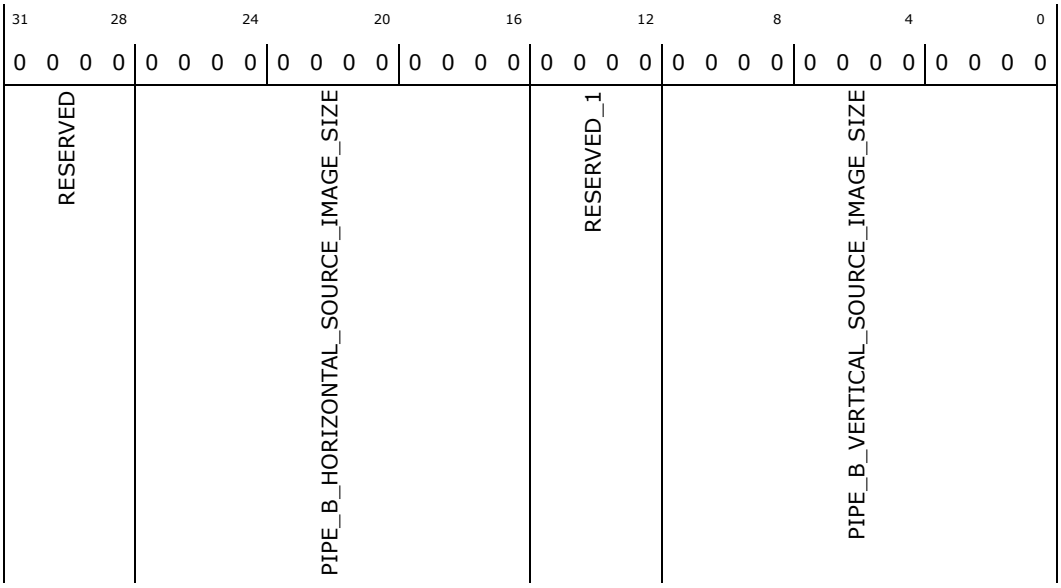
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBSRC: [GTTMMADR_LSB + 2BF20h] + 6101Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PIPE_B_HORIZONTAL_SOURCE_IMAGE_SIZE:** See pipe A description.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PIPE_B_VERTICAL_SOURCE_IMAGE_SIZE:** See pipe A description.

3.1.198 BCLRPAT_B—Offset 61020h

Pipe B Border Color Pattern Register

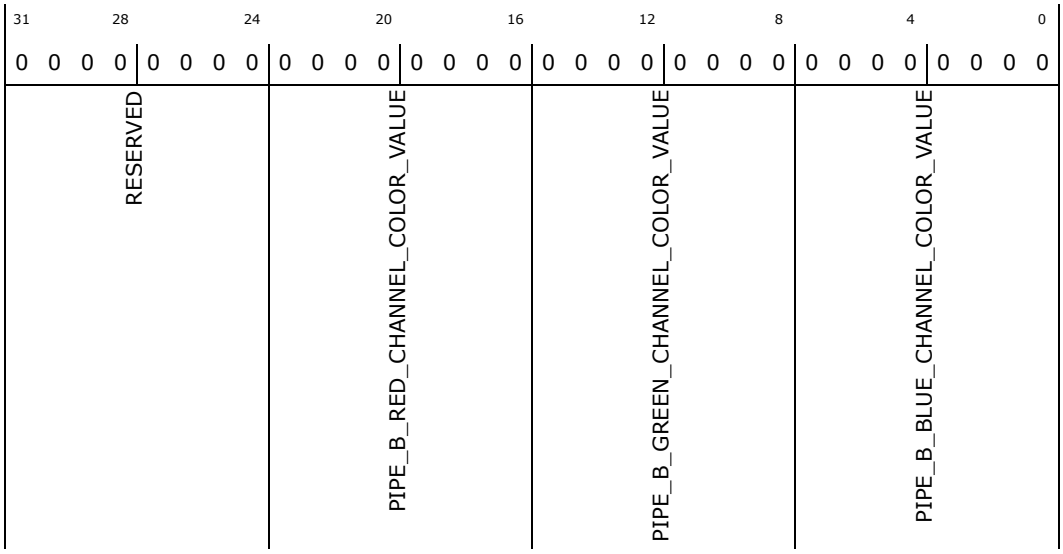
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BCLRPAT_B: [GTTMMADR_LSB + 2BF20h] + 61020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**PIPE_B_RED_CHANNEL_COLOR_VALUE:** pipeB red color channel values
15:8	0b RW	**PIPE_B_GREEN_CHANNEL_COLOR_VALUE:** pipeB green color channel values
7:0	0b RW	**PIPE_B_BLUE_CHANNEL_COLOR_VALUE:** pipeB blue color channel values

3.1.199 VSYNCSHIFT_B—Offset 61028h

Vertical Sync Shift Register

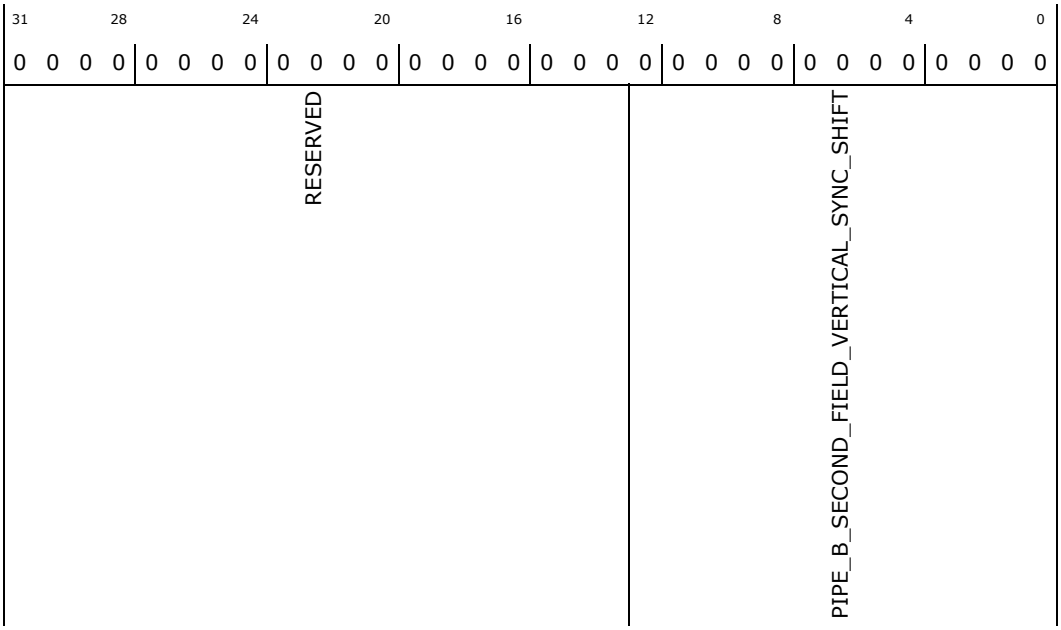
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VSYNCSHIFT_B: [GTTMMADR_LSB + 2BF20h] + 61028h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:13	0b RW	**RESERVED:** Write as zero.
12:0	0b RW	**PIPE_B_SECOND_FIELD_VERTICAL_SYNC_SHIFT:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the PIPEBCONF is programmed to an interlaced mode using vsync shift. Otherwise a legacy value of floor[htotal / 2] will be used. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into registers). This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

3.1.200 TRANSBDATAM1—Offset 61030h

Pipe B Data M value 1

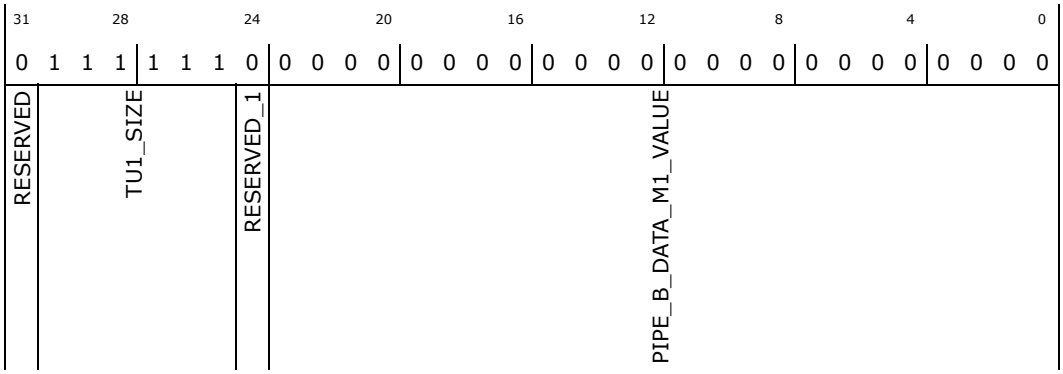
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSBDATAM1: [GTTMMADR_LSB + 2BF20h] + 61030h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 7E000000h



Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:25	111111b RW	**TU1_SIZE:** Project: All Default Value: ;111111b 64 See Pipe A description.
24	0b RW	**RESERVED_1:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_DATA_M1_VALUE:** Project: All See Pipe A description.

3.1.201 TRANSBDATAN1—Offset 61034h

Pipe B Data N value 1

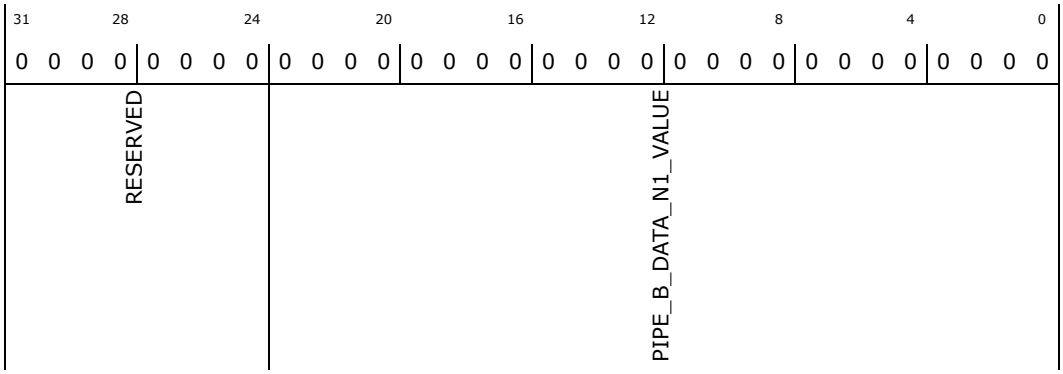
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSBDATAN1: [GTTMMADR_LSB + 2BF20h] + 61034h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_DATA_N1_VALUE:** Project: All See Pipe A description.

3.1.202 TRANSBDATAM2—Offset 61038h

Pipe B Data M value 2

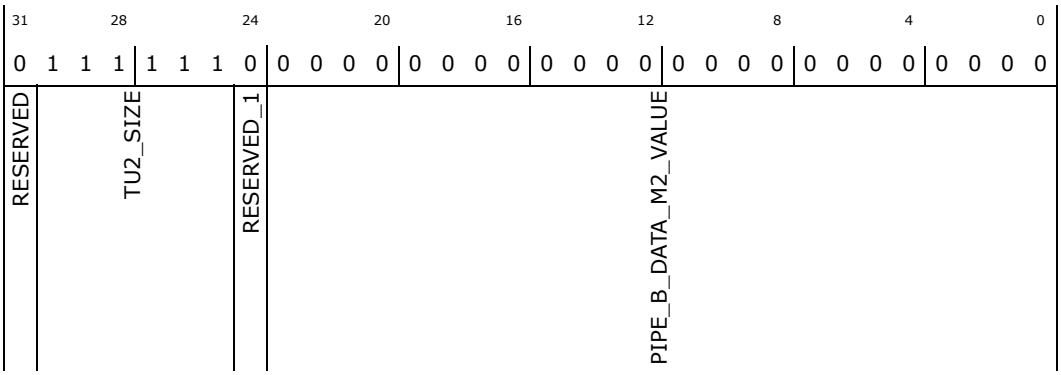
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSBDATAM2: [GTTMMADR_LSB + 2BF20h] + 61038h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 7E000000h



Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:25	111111b RW	**TU2_SIZE:** Project: All Default Value: ;111111b 64 See Pipe A description.
24	0b RW	**RESERVED_1:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_DATA_M2_VALUE:** Project: All See Pipe A description.

3.1.203 TRANSBDATAN2—Offset 6103Ch

Pipe B Data N value 2

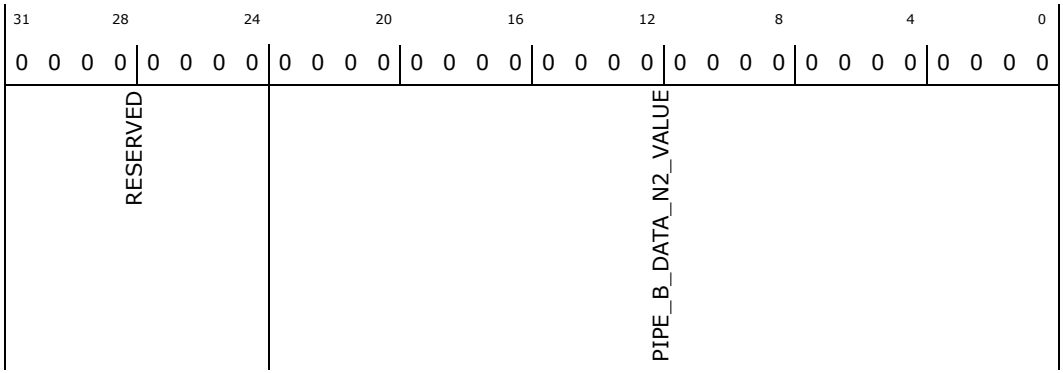
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSBDATAN2: [GTTMMADR_LSB + 2BF20h] + 6103Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_DATA_N2_VALUE:** Project: All See Pipe A description.

3.1.204 TRANSBDPLINKM1—Offset 61040h

Pipe B Link M value 1

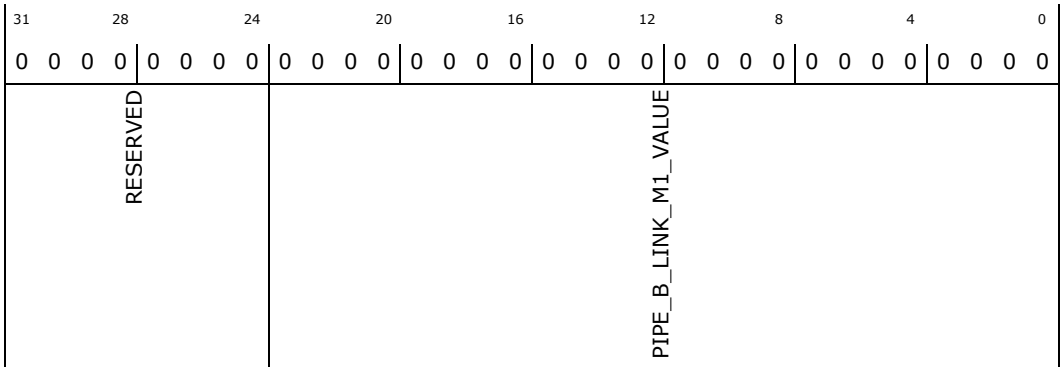
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSBDPLINKM1: [GTTMMADR_LSB + 2BF20h] + 61040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_LINK_M1_VALUE:** Project: All See Pipe A description.

3.1.205 TRANSBDPLINKN1—Offset 61044h

Pipe B Link N value 1

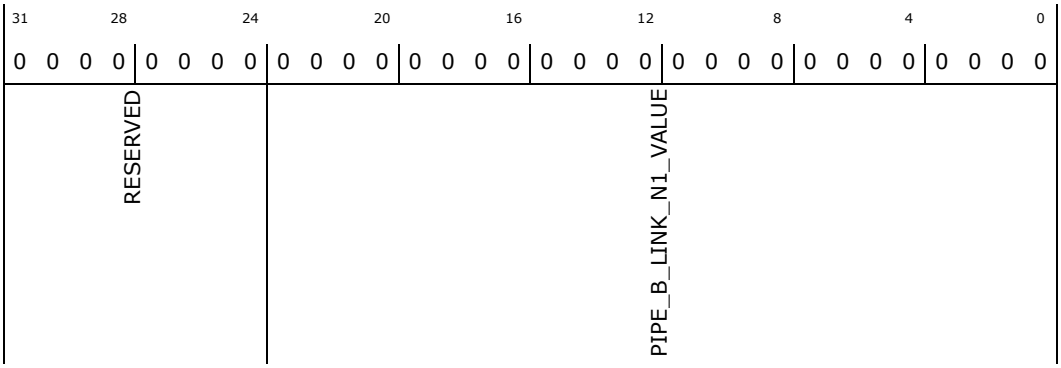
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSBDPLINKN1: [GTTMMADR_LSB + 2BF20h] + 61044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_LINK_N1_VALUE:** Project: All See Pipe A description.

3.1.206 TRANSBDPLINKM2—Offset 61048h

Pipe B Link M value 2

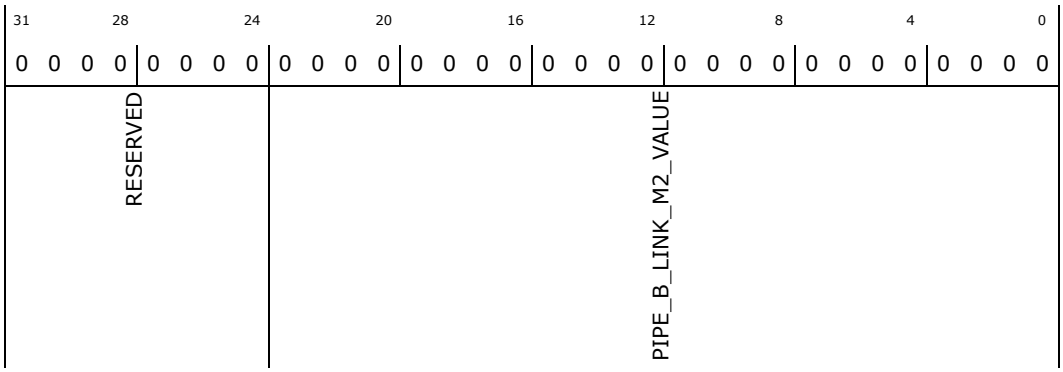
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSBDPLINKM2: [GTTMMADR_LSB + 2BF20h] + 61048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_LINK_M2_VALUE:** Project: All See Pipe A description.

3.1.207 TRANSBDPLINKN2—Offset 6104Ch

Pipe B Link N value 2

Access Method

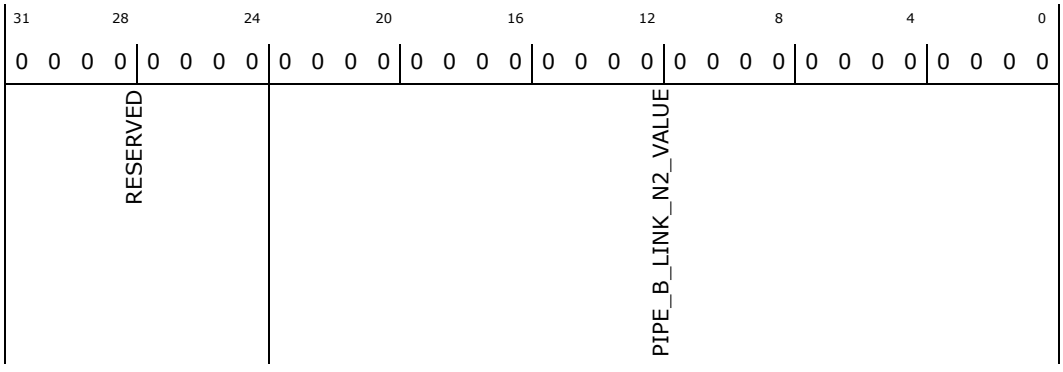
Type: Memory Mapped I/O Register (Size: 32 bits)

TRANSBDPLINKN2: [GTTMMADR_LSB + 2BF20h] + 6104Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ

Bit Range	Default & Access	Description
23:0	0b RW	**PIPE_B_LINK_N2_VALUE:** Project: All See Pipe A description.

3.2 Display Memory Mapped Registers (Read Only)

Table 10. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
3BAh	1	"ST01 (ST01_MDA)—Offset 3BAh" on page 232	00h
3C2h	1	"ST00—Offset 3C2h" on page 233	00h
3C7h	1	"DACSTATE—Offset 3C7h" on page 234	00h
3DAh	1	"ST01 (ST01_CGA)—Offset 3DAh" on page 235	00h

3.2.1 ST01 (ST01_MDA)—Offset 3BAh

Input Status 1

Access Method

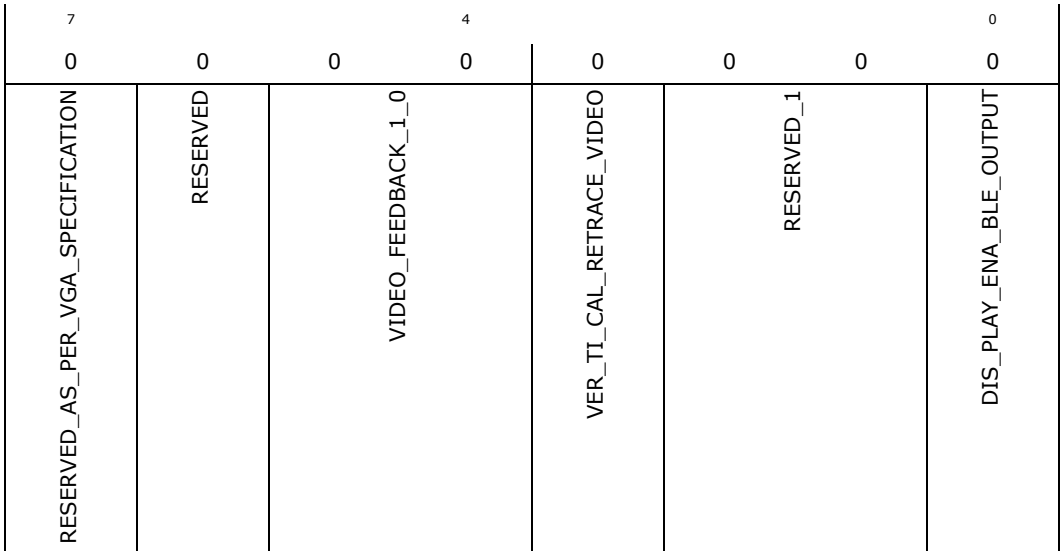
Type: Memory Mapped I/O Register (Size: 8 bits)

ST01_MDA: [GTTMMADR_LSB + 2BF20h] + 3BAh

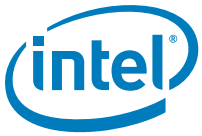
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RO	**RESERVED_AS_PER_VGA_SPECIFICATION:** Read as 0s.
6	0b RO	**RESERVED:** Read as 0.



Bit Range	Default & Access	Description
5:4	0b RO	**VIDEO_FEEDBACK_1_0:** These are diagnostic video bits that are selected by the Color Plane Enable Register. These bits that are programmably connected to 2 of the 8 color bits sent to the palette. Bits 4 and 5 of the Color Plane Enable Register (AR12) selects which two of the 8 possible color bits become connected to these 2 bits of this register. The current software normally does not use these 2 bits. They exist for EGA compatibility.
3	0b RO	**VER_TI_CAL_RETRACE_VIDEO:** 0 = VSYNC inactive (Indicates that a vertical retrace interval is not taking place). 1 = VSYNC active (Indicates that a vertical retrace interval is taking place). Note: VGA pixel generation is not locked to the display output but is loosely coupled. A VSYNC indication may not occur during the actual VSYNC going to the display but during the VSYNC that is generated as part of the VGA pixel generation. The exact relationship will vary with the VGA display operational mode. This status bit will remain active when the VGA is disabled and the device is running in high resolution modes (non-VGA) to allow for applications that (now it is incorrect) use these status registers bits. In this case, the status will come from the pipe that the VGA is assigned to. Bits 4 and 5 of the Vertical Retrace End Register (CR11) previously could program this bit to generate an interrupt at the start of the vertical retrace interval. This ability to generate interrupts at the start of the vertical retrace interval is a feature that is largely unused by legacy software. Interrupts are not supported through the VGA register bits.
2:1	0b RO	**RESERVED_1:** Read as 0s.
0	0b RO	**DIS_PLAY_ENA_BLE_OUTPUT:** Display Enable is a status bit (bit 0) in VGA Input Status Register 1 that indicates when either a horizontal retrace interval or a vertical retrace interval is taking place. This was used with the IBM* EGA graphics system (and the ones that preceded it, including MDA and CGA). In those cases, it was important to check the status of this bit to ensure that one or the other retrace intervals was taking place before reading from or writing to the frame buffer. In these earlier systems, reading from or writing to frame buffer at times outside the retrace intervals meant that the CRT controller would be denied access to the frame buffer. This resulted in either snow or a flickering display. This bit provides compatibility with software designed for those early graphics controllers. This bit is currently used in DOS applications that access the palette to prevent the sparkle associated with read and write accesses to the palette ram with the same address on the same clock cycle. This status bit will remain active when the VGA display is disabled and the device is running in high resolution modes (non-VGA) to allow for applications that (now considered incorrect) use these status registers bits. In this case, the status will come from the pipe that the VGA is assigned to. When in panel fitting VGA or centered VGA operation, the meaning of these bits will not be consistent with native VGA timings. 0 = Active display data is being sent to the display. Neither a horizontal retrace interval or a vertical retrace interval is currently taking place. 1 = Either a horizontal retrace interval (horizontal blanking) or a vertical retrace interval (vertical blanking) is currently taking place.

3.2.2 ST00—Offset 3C2h

Input Status 0

Access Method

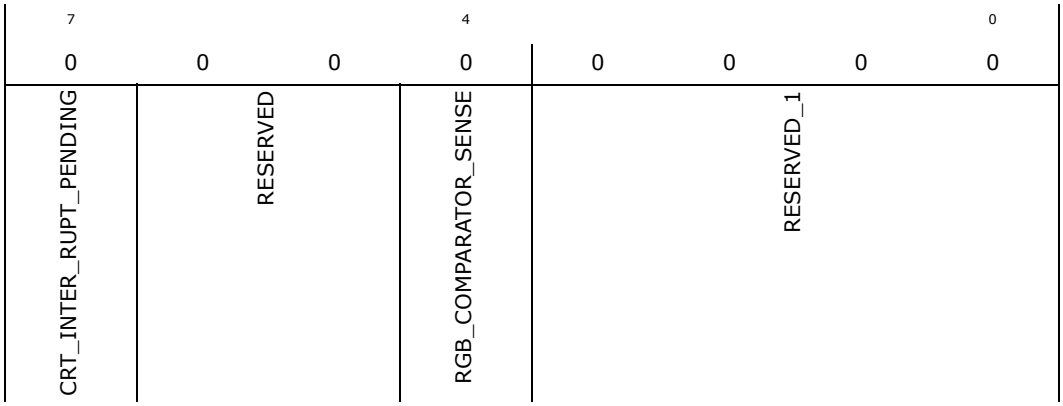
Type: Memory Mapped I/O Register (Size: 8 bits)

ST00: [GTTMMADR_LSB + 2BF20h] + 3C2h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RO	**CRT_INTER_RUPT_PENDING:** This bit is here for EGA compatibility and will always return zero. Note that the generation of interrupts was originally enabled, through bits [4,5] of the Vertical Retrace End Register (CR11). This ability to generate interrupts at the start of the vertical retrace interval is a feature that is typically unused by DOS software and therefore is only supported through other means for use under a operating system support. 0 = CRT (vertical retrace interval) interrupt is not pending. 1 = CRT (vertical retrace interval) interrupt is pending
6:5	0b RO	**RESERVED:** Read as 0s.
4	0b RO	**RGB_COMPARATOR_SENSE:** This bit returns the state of the output of the RGB output comparator(s). Video BIOS uses this bit during POST to determine whether the display is connected and if it is a color or monochrome CRT. BIOS blanks the screen or clears the frame buffer to display only black. Next, BIOS outputs a ramp to the D-to-A converters to test for the presence of a color display by determining which code cause the comparator to switch. Finally, if the BIOS does not detect any termination resistors on Red or Blue, it tests for the presence of a display using the Green signal. The result of each such test is read via this bit. 0 = Below threshold 1 = Above threshold
3:0	0b RO	**RESERVED_1:** Read as 0s.

3.2.3 DACSTATE—Offset 3C7h

DAC State Register

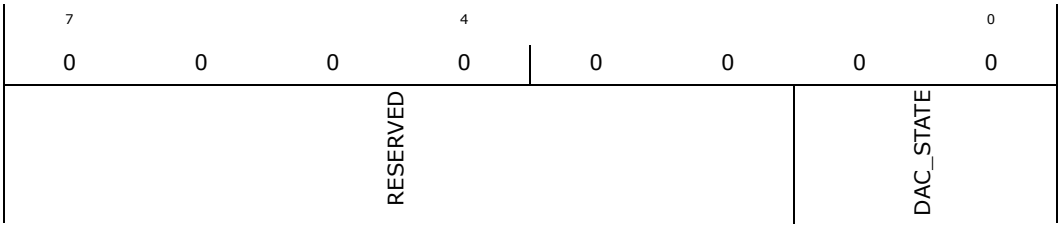
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

DACSTATE: [GTTMMADR_LSB + 2BF20h] + 3C7h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:2	0b RO	**RESERVED:** Read as 0.
1:0	0b RO	**DAC_STATE:** This field indicates which of the two index registers was most recently written. Bits [1:0] Index Register Indicated 00 Palette Write Index Register at I/O Address 3C7h (default) 01 Reserved 10 Reserved 11 Palette Read Index Register at I/O Address 3C8h

3.2.4 ST01 (ST01_CGA)—Offset 3DAh

Input Status 1

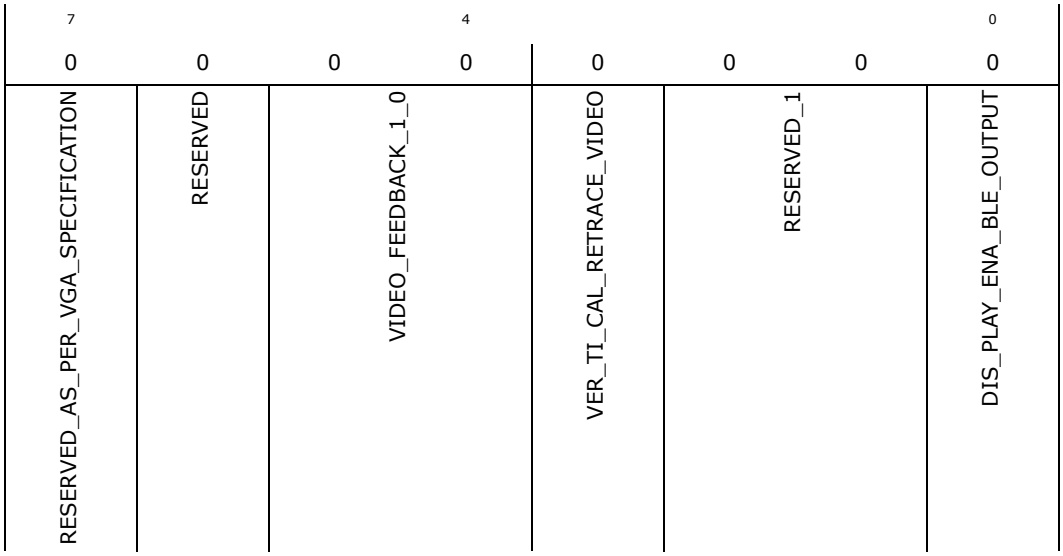
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

ST01_CGA: [GTTMMADR_LSB + 2BF20h] + 3DAh

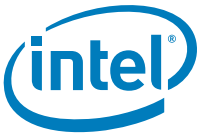
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RO	**RESERVED_AS_PER_VGA_SPECIFICATION:** Read as 0s.
6	0b RO	**RESERVED:** Read as 0.
5:4	0b RO	**VIDEO_FEEDBACK_1_0:** These are diagnostic video bits that are selected by the Color Plane Enable Register. These bits that are programmably connected to 2 of the 8 color bits sent to the palette. Bits 4 and 5 of the Color Plane Enable Register (AR12) selects which two of the 8 possible color bits become connected to these 2 bits of this register. The current software normally does not use these 2 bits. They exist for EGA compatibility.
3	0b RO	**VER_TI_CAL_RETRACE_VIDEO:** 0 = VSYNC inactive (Indicates that a vertical retrace interval is not taking place). 1 = VSYNC active (Indicates that a vertical retrace interval is taking place). Note: VGA pixel generation is not locked to the display output but is loosely coupled. A VSYNC indication may not occur during the actual VSYNC going to the display but during the VSYNC that is generated as part of the VGA pixel generation. The exact relationship will vary with the VGA display operational mode. This status bit will remain active when the VGA is disabled and the device is running in high resolution modes (non-VGA) to allow for applications that (now it is incorrect) use these status registers bits. In this case, the status will come from the pipe that the VGA is assigned to. Bits 4 and 5 of the Vertical Retrace End Register (CR11) previously could program this bit to generate an interrupt at the start of the vertical retrace interval. This ability to generate interrupts at the start of the vertical retrace interval is a feature that is largely unused by legacy software. Interrupts are not supported through the VGA register bits.
2:1	0b RO	**RESERVED_1:** Read as 0s.

Bit Range	Default & Access	Description
0	0b RO	**DIS_PLAY_ENA_BLE_OUTPUT:** Display Enable is a status bit (bit 0) in VGA Input Status Register 1 that indicates when either a horizontal retrace interval or a vertical retrace interval is taking place. This was used with the IBM* EGA graphics system (and the ones that preceded it, including MDA and CGA). In those cases, it was important to check the status of this bit to ensure that one or the other retrace intervals was taking place before reading from or writing to the frame buffer. In these earlier systems, reading from or writing to frame buffer at times outside the retrace intervals meant that the CRT controller would be denied access to the frame buffer. This resulted in either snow or a flickering display. This bit provides compatibility with software designed for those early graphics controllers. This bit is currently used in DOS applications that access the palette to prevent the sparkle associated with read and write accesses to the palette ram with the same address on the same clock cycle. This status bit will remain active when the VGA display is disabled and the device is running in high resolution modes (non-VGA) to allow for applications that (now considered incorrect) use these status registers bits. In this case, the status will come from the pipe that the VGA is assigned to. When in panel fitting VGA or centered VGA operation, the meaning of these bits will not be consistent with native VGA timings. 0 = Active display data is being sent to the display. Neither a horizontal retrace interval or a vertical retrace interval is currently taking place. 1 = Either a horizontal retrace interval (horizontal blanking) or a vertical retrace interval (vertical blanking) is currently taking place.



3.3 Display PCI Configuration Registers

Table 11. Summary of Graphics, Video and Display PCI Configuration Registers—0/2/0

Offset	Size	Register ID—Description	Default Value
0h	4	"DID—Offset 0h" on page 239	0F318086h
4h	4	"PCICMD_STS—Offset 4h" on page 239	00100000h
8h	4	"RID_CC—Offset 8h" on page 240	03000000h
Ch	4	"HDR—Offset Ch" on page 241	00000000h
10h	4	"GTTMMADR_LSB—Offset 10h" on page 242	00000000h
14h	4	"GTTMMADR_MSB—Offset 14h" on page 242	00000000h
18h	4	"GMADR_LSB—Offset 18h" on page 243	00000008h
1Ch	4	"GMADR_MSB—Offset 1Ch" on page 244	00000000h
20h	4	"IOBAR—Offset 20h" on page 244	00000001h
2Ch	4	"SSID_SID—Offset 2Ch" on page 245	00000000h
34h	4	"CAPPOINT—Offset 34h" on page 246	000000D0h
3Ch	4	"INTRLINE—Offset 3Ch" on page 247	00000100h
50h	4	"GGC—Offset 50h" on page 248	00000028h
5Ch	4	"BDSM—Offset 5Ch" on page 249	00000000h
60h	4	"MSAC—Offset 60h" on page 250	00020000h
70h	4	"BGSM—Offset 70h" on page 251	00000000h
74h	4	"PAVPC—Offset 74h" on page 252	00000000h
90h	4	"MSI_CAPID_MC—Offset 90h" on page 253	0000B005h
94h	4	"MA—Offset 94h" on page 254	00000000h
98h	4	"MD—Offset 98h" on page 255	00000000h
A4h	4	"AFLC—Offset A4h" on page 255	03060013h
A8h	4	"AFCTLSTS—Offset A8h" on page 256	00000000h
B0h	4	"VCID—Offset B0h" on page 257	01070009h
B4h	4	"VCID—Offset B0h" on page 257	00000000h
C4h	4	"FD—Offset C4h" on page 258	00000000h
D0h	4	"PMCAPID—Offset D0h" on page 259	00229001h
D4h	4	"PMCS—Offset D4h" on page 260	00000000h
E0h	4	"SWSMISCI—Offset E0h" on page 261	00000000h
E4h	4	"ASLE—Offset E4h" on page 262	00000000h
F8h	4	"MANID—Offset F8h" on page 263	00000000h
FCh	4	"ASLS—Offset FCh" on page 264	00000000h

3.3.1 DID—Offset 0h

PCI Device ID and Vendor ID Register

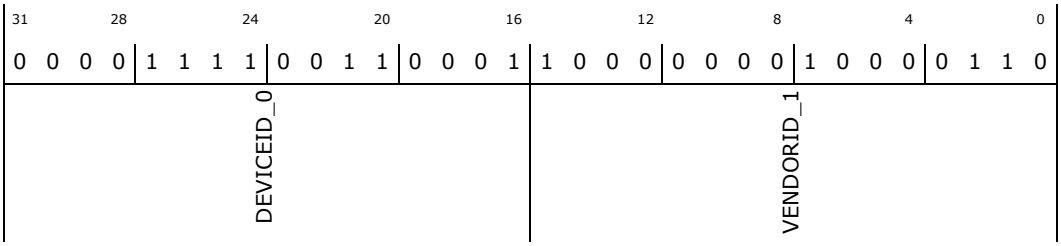
Access Method

Type: PCI Configuration Register (Size: 32 bits)

DID: [B:0, D:2, F:0] + 0h

Power Well: Core

Default: 0F318086h



Bit Range	Default & Access	Description
31:16	0F31h RO	**DEVICEID (DEVICEID_0):** DID: Identifier assigned to the dev2 PCI
15:0	8086h RO	**VENDORID (VENDORID_1):** VID: PCI standard identification for Intel

3.3.2 PCICMD_STS—Offset 4h

PCI Command Register and Status Register

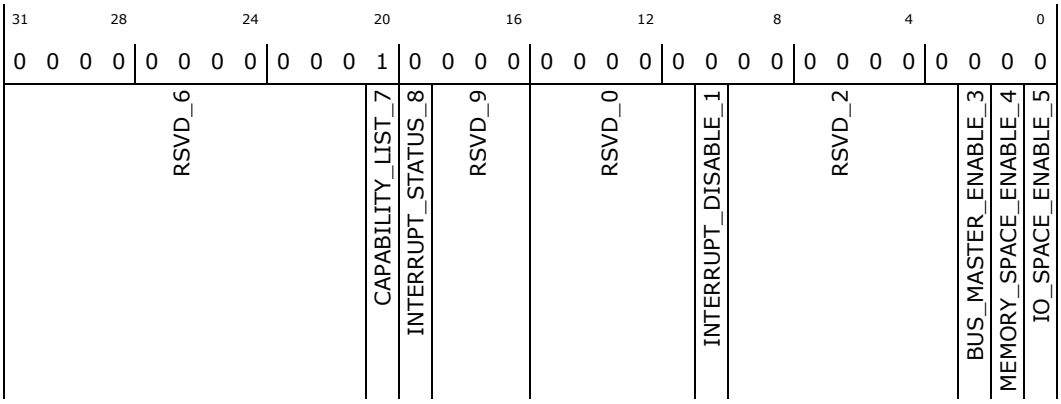
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCICMD_STS: [B:0, D:2, F:0] + 4h

Power Well: Core

Default: 00100000h



Bit Range	Default & Access	Description
31:21	000h RO	**RSVD (RSVD_6):** Reserved
20	1b RO	**CAPABILITY_LIST (CAPABILITY_LIST_7):** CAP: CAPPOINT register at 34h provides an offset
19	0b RO	**INTERRUPT_STATUS (INTERRUPT_STATUS_8):** IS: 1= Determined by IIR and IER memory interface register, 0=no interrupt pending
18:16	000b RO	**RSVD (RSVD_9):** Reserved
15:11	00h RO	**RSVD (RSVD_0):** Reserved
10	0b RW	**INTERRUPT_DISABLE (INTERRUPT_DISABLE_1):** ID: 0= Interrupt message enabled, 1= disabled
9:3	00h RO	**RSVD (RSVD_2):** Reserved
2	0b RW	**BUS_MASTER_ENABLE (BUS_MASTER_ENABLE_3):** BME: 0= Blocks the sending of MSI interrupts, 1= permits
1	0b RW	**MEMORY_SPACE_ENABLE (MEMORY_SPACE_ENABLE_4):** MSE: 0= Memory space disabled, 1= enabled
0	0b RW	**IO_SPACE_ENABLE (IO_SPACE_ENABLE_5):** IOSE: 0= I/O space is disabled, 1=enabled

3.3.3 RID_CC—Offset 8h

Revision Identification and Class code registerSOXi Context Save/Restore: Yes

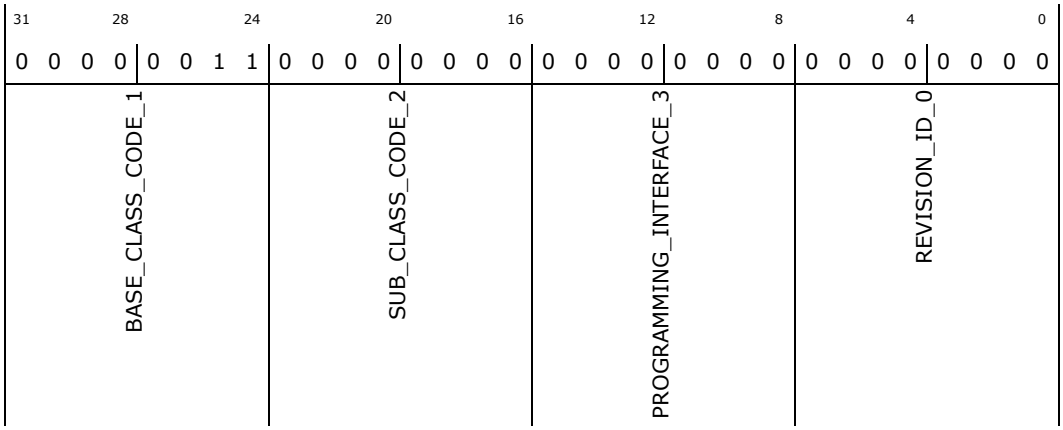
Access Method

Type: PCI Configuration Register (Size: 32 bits)

RID_CC: [B:0, D:2, F:0] + 8h

Power Well: Core

Default: 03000000h



Bit Range	Default & Access	Description
31:24	00000011b RO	**BASE_CLASS_CODE (BASE_CLASS_CODE_1):** BCC: MGGC0[VAMEN]=0, 03h else 04h
23:16	00000000b RO	**SUB_CLASS_CODE (SUB_CLASS_CODE_2):** MGGC0[VAMEN]= 1, 80h, MGGC0[VAMEN]=0,determined based on GGC register, GMS and IVD
15:8	00h RO	**PROGRAMMING_INTERFACE (PROGRAMMING_INTERFACE_3):** MGGC0[VAMEN]= 0, 00h display controller, =1, 00h NOP
7:0	00000000b RO	**REVISION_ID (REVISION_ID_0):** RID: value of strapRID[7:0] input pin to GVD

3.3.4 HDR—Offset Ch

Header Type

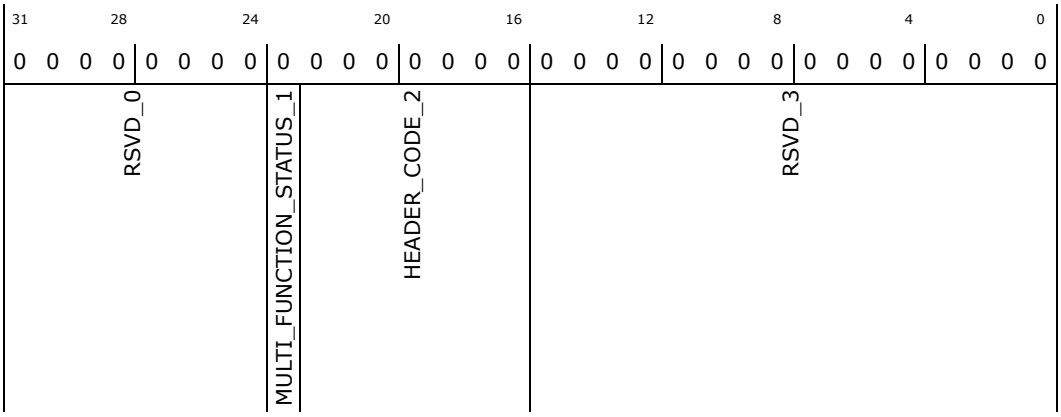
Access Method

Type: PCI Configuration Register (Size: 32 bits)

HDR: [B:0, D:2, F:0] + Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**RSVD (RSVD_0):** Reserved
23	0b RO	**MULTI_FUNCTION_STATUS (MULTI_FUNCTION_STATUS_1):** MFUNC: Integrated graphics is a single function
22:16	00h RO	**HEADER_CODE (HEADER_CODE_2):** HDR: Indicates a type 0 configuration space header format
15:0	0000h RO	**RSVD (RSVD_3):** Reserved

3.3.5 GTTMMADR_LSB—Offset 10h

Gfx Memory Mapped Address Range. This is the base address for all memory mapped registers and GTT table. SOXi Context Save/Restore : Yes This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 512K of that used by MMIO and 2MB used by GTT. GTTADR will begin at (GTTMMADR + 2 MB) while the MMIO base address will be the same as GTTMMADR. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The allocation is for 4MB and the base address is defined by bits [35:22].

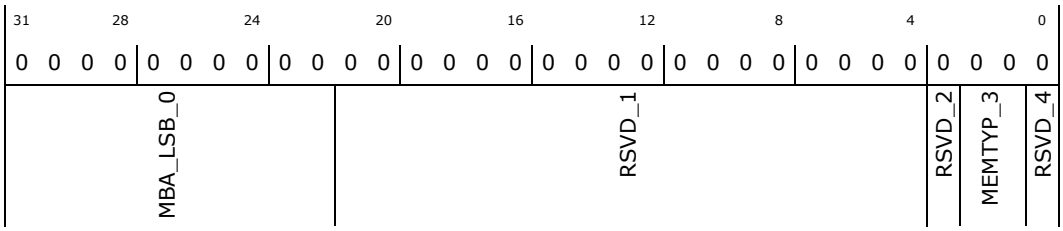
Access Method

Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB: [B:0, D:2, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:22	000h RW	**MBA_LSB (MBA_LSB_0):** Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).
21:4	00000h RO	**RSVD (RSVD_1):** RSVD: Hardwired to 0 to indicate at least 4MB address range.
3	0b RO	**RSVD (RSVD_2):** Prefetchable Memory (PREFMEM): Hardwired to 0to prevent prefetching.
2:1	00b RO	**MEMTYP (MEMTYP_3):** Memory Type (MEMTYP): 00 : To indicate 32 bit base address 01: Reserved 10 : To indicate 64 bit base address 11: Reserved
0	0b RO	**RSVD (RSVD_4):** Memory/IO Space (MIOS): Hardwired to 0 to indicate memory space.

3.3.6 GTTMMADR_MSB—Offset 14h

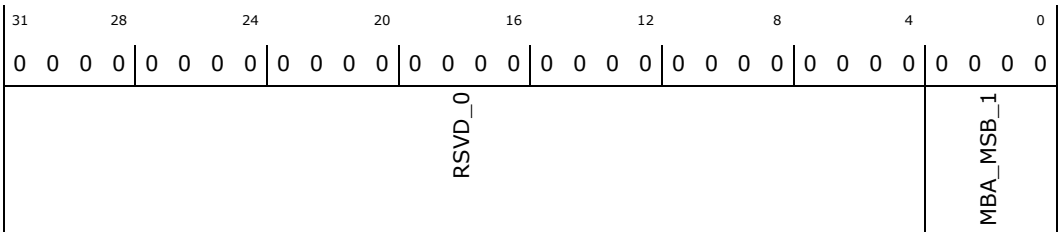
Access Method

Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_MSB: [B:0, D:2, F:0] + 14h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:4	00000000h RO	**RSVD (RSVD_0):** Reserved for Memory Base Address (RSVD): Must be set to 0 since addressing above 64GB is not supported.
3:0	0h RO	**MBA_MSB (MBA_MSB_1):** Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).

3.3.7 GMADR_LSB—Offset 18h

Gfx Aperture location. SOXi Context Save/Restore : Yes GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining. Accesses to this range will be translated to DRAM Physical memory addresses. Fence registers may be used to sub-divide this range and allow tiled surfaces (determined by fence registers). The following sizes are supported : 128MB, 256MB, 512MB. (Determined by the MSAC register)

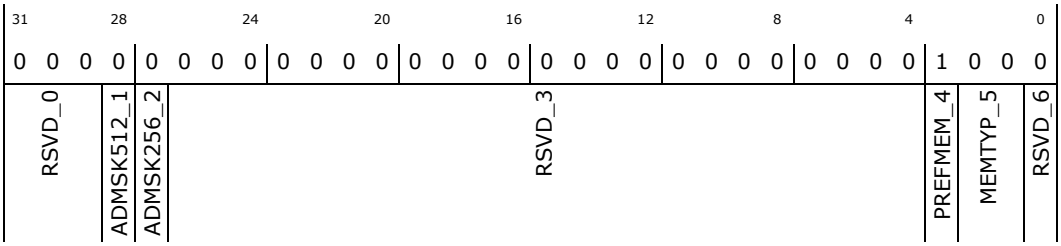
Access Method

Type: PCI Configuration Register (Size: 32 bits)

GMADR_LSB: [B:0, D:2, F:0] + 18h

Power Well: Core

Default: 00000008h



Bit Range	Default & Access	Description
31:29	000b RO	**RSVD (RSVD_0):** Memory Base Address (MBA): Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:29].

Bit Range	Default & Access	Description
28	0b RW/L	**ADMSK512 (ADMSK512_1):** 512MB Address Mask (ADMSK512): This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[2:1]. See MSAC (Dev2, Func 0, offset 62h) for details.
27	0b RW/L	**ADMSK256 (ADMSK256_2):** 256MB Address Mask (ADMSK256): This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[2:1]. See MSAC (Dev 2, Func 0, offset 62h) for details.
26:4	0000000h RO	**RSVD (RSVD_3):** Address Mask (ADM): Hardwired to 0s to indicate at least 128MB address range.
3	1b RO	**PREFMEM (PREFMEM_4):** Prefetchable Memory (PREFMEM): Hardwired to 1 to enable prefetching.
2:1	00b RO	**MEMTYP (MEMTYP_5):** Memory Type (MEMTYP): 00 : To indicate 32 bit base address 01: Reserved 10 : To indicate 64 bit base address 11: Reserved
0	0b RO	**RSVD (RSVD_6):** Memory/IO Space (MIOS): Hardwired to 0 to indicate memory space.

3.3.8 GMADR_MSB—Offset 1Ch

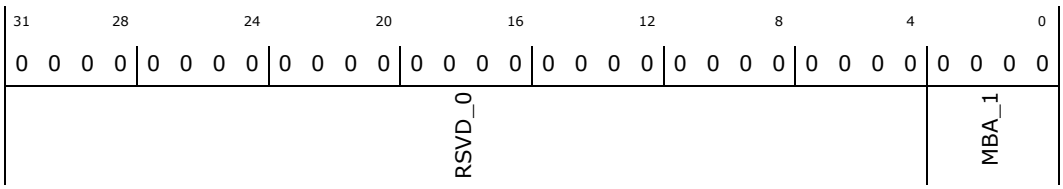
Access Method

Type: PCI Configuration Register (Size: 32 bits)

GMADR_MSB: [B:0, D:2, F:0] + 1Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0000000h RO	**RSVD (RSVD_0):** Memory Base Address (MBA2): Set by the OS, these bits correspond to address signals [63:36].
3:0	0h RO	**MBA (MBA_1):** Memory Base Address (MBA)Set by the OS, these bits correspond to address signals [35:32]

3.3.9 IOBAR—Offset 20h

I/O Base Address. This is used only by SBIOS. This register is the base address for the MMIO_INDEX and MMIO_DATA registers SOXi Context Save/Restore : Yes NOTE : This was at 14h for CDV. This register provides the Base offset of the I/O registers within Device #2. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed : 1)in PM states D1-D3 or 2)if IO Enable is

clear or 3)if Device #2 is turned off or 4)if Internal graphics is disabled thru the fuse or fuse override mechanisms. Note that access to this IO BAR is independent of VGA functionality within Device #2. If accesses to this IO bar is allowed then the GMCH claims all 8, 16 or 32 bit IO cycles from the CPU that falls within the 8B claimed.

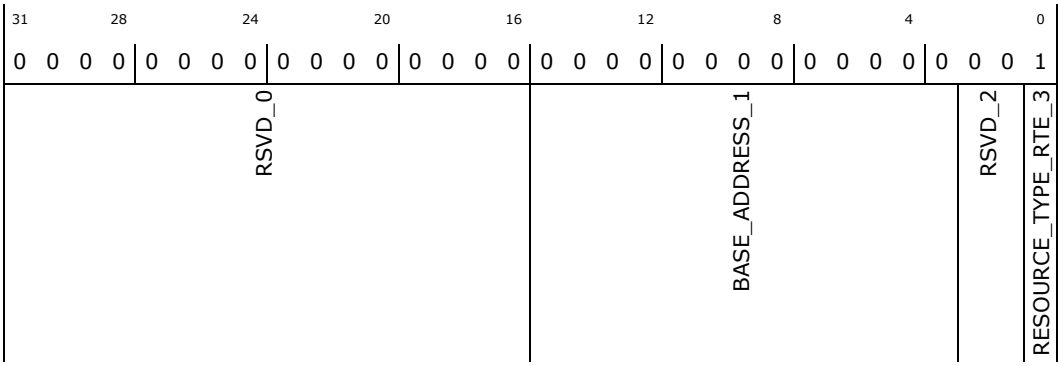
Access Method

Type: PCI Configuration Register (Size: 32 bits)

IOBAR: [B:0, D:2, F:0] + 20h

Power Well: Core

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0000h RO	**RSVD (RSVD_0):** Reserved
15:3	0000h RW	**BASE_ADDRESS (BASE_ADDRESS_1):** BA: Set by the OS, these bits correspond to address signals [15:6].IOBAR is to be used for both GTLC register programming and GTT table programming. This is an indirect access method.
2:1	00b RO	**RSVD (RSVD_2):** Reserved
0	1b RO	**RESOURCE_TYPE_RTE (RESOURCE_TYPE_RTE_3):** Indicates a request for I/O space

3.3.10 SSID_SID—Offset 2Ch

This register is used to uniquely identify the subsystem where the PCI device resides.

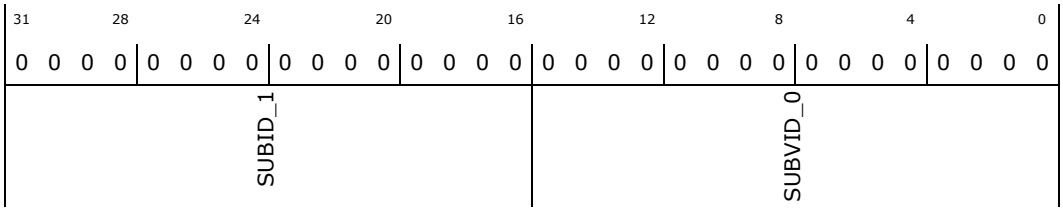
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SSID_SID: [B:0, D:2, F:0] + 2Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBID (SUBID_1):** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.
15:0	0000h RW/O	**SUBVID (SUBVID_0):** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

3.3.11 CAPPOINT—Offset 34h

This register points to a linked list of capabilities implemented by this device.For VV, the capability linked list is expected to be : (Head-34, PMCAP-D0, MSI-90, VID-B0, ..End)Old : (Head-34, PMCAP-D0, MSI-90, AFLC-A4, VID-B0, .. End)

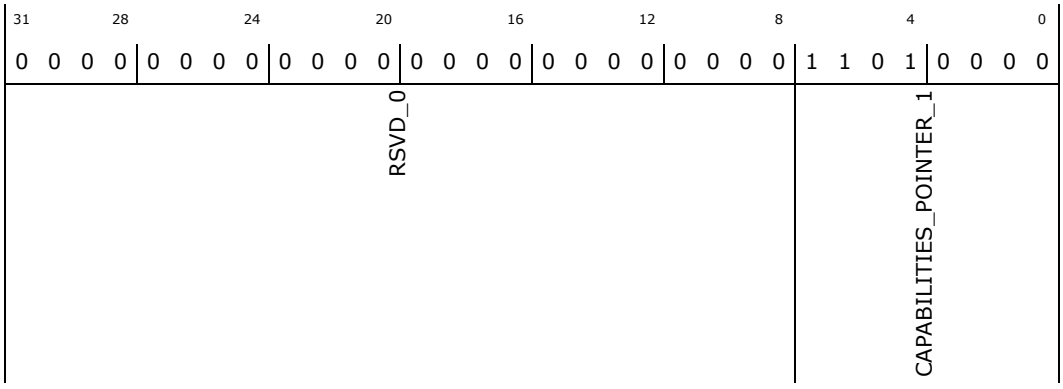
Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPPOINT: [B:0, D:2, F:0] + 34h

Power Well: Core

Default: 000000D0h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD (RSVD_0):** Reserved

Bit Range	Default & Access	Description
7:0	D0h RW/O	**CAPABILITIES_POINTER (CAPABILITIES_POINTER_1):** The first item in the capabilities list is at address D0h (PMCS). This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

3.3.12 INTRLINE—Offset 3Ch

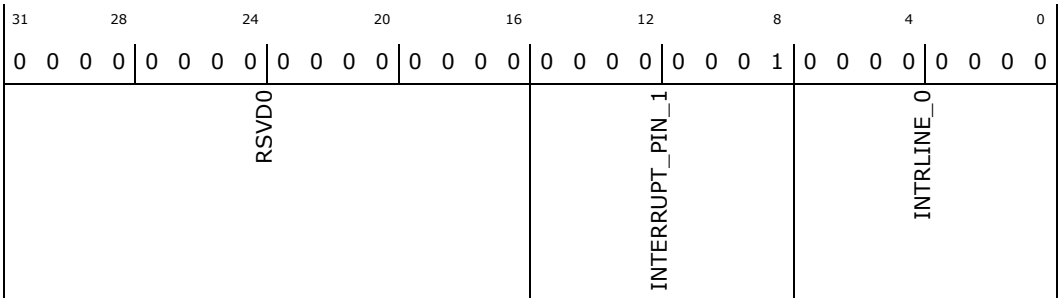
3C - Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver. This 8-bit register is used to communicate interrupt line routing information. It is read/write and must be implemented by the device. POST software will write the routing information into this register as it initializes and configures the system. SOXi Context Save/Restore : Yes The value in this register tells which input of the system interrupt controller(s) the devices interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information. 3D - Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver SOXi Context Save/Restore : Not required

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTRLINE: [B:0, D:2, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	01h RO	**INTERRUPT_PIN (INTERRUPT_PIN_1):** IPIN: Value indicates which interrupt pin this device uses. This field is hard coded to 1h since SoC device 2 is a single function device. The PCI spec requires that it use INTA#.01h: INTA
7:0	00h RW	**INTRLINE (INTRLINE_0):** ILIN: BIOS written value to communicate interrupt line routing information to the device driverUsed to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the devices interrupt pin is connected.

3.3.13 GGC—Offset 50h

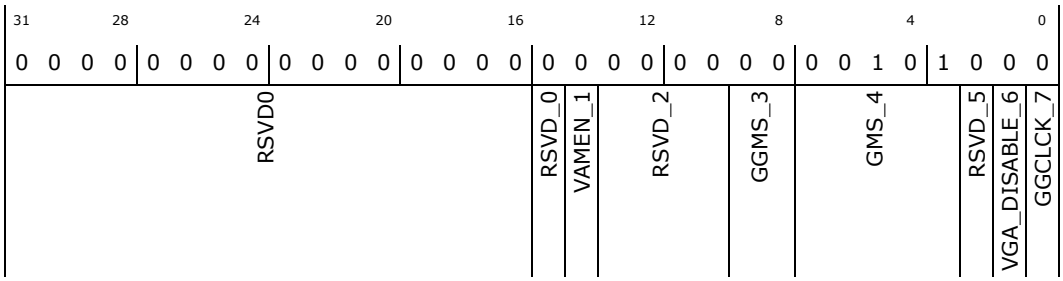
GMCH Graphics Control Register. SOXi Context Save/Restore : Yes Note : CDV supported 64MB maximum. CDV had no GGMS field. Note : CDV had more granularity on the encoding for graphics mode select and only 3 bits.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GGC: [B:0, D:2, F:0] + 50h

Default: 00000028h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15	0b RO	**RSVD (RSVD_0):** Reserved
14	0b RW/L	**VAMEN (VAMEN_1):** Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
13:10	0h RO	**RSVD (RSVD_2):** Reserved
9:8	00b RW/L	**GGMS (GGMS_3):** GTT Graphics Memory Size (GGMS): This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will drive the base of GSM from DSM only using the GSM size programmed in the register. 0h: No memory pre-allocated. GTT cycles (Mem and IO) are not claimed. 1h: 1 MB of memory pre-allocated for GTT. 2h: 2 MB of memory pre-allocated for GTT. 3h: Reserved. All unspecified encoding of this register field are reserved, hardware functionality is not guaranteed if used.

Bit Range	Default & Access	Description
7:3	00101b RW/L	**GMS (GMS_4):** Graphics Mode Select (GMS). This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. 0h = 0MB 10h = 512MB 1h = 32MB 2h = 64MB 3h = 96MB 4h = 128MB 5h = 160MB 6h = 192MB 7h = 224MB 8h = 256MB 9h = 288MB Ah = 320MB Bh = 352MB Ch = 384MB Dh = 416MB Eh = 448MB Fh = 480MB Other = Reserved When GMS != 000 (and VD=0): Address[31:0] is compared with VGA memory range. (The VGA memory range is A_0000h to B_FFFFh.). If there is a match and MSE = 1 and MEMRD or MEMWR, the access will route as a Rmdwvgamemen_cr cycle on the RMbus. If the RMbus returns a hit the GVD will select the command. As well, when 0 the GVD will check if scldown3_address[15:0] is one of the VGA IO register range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) If there is a match and IOSE = 1 and the SCL command is either an IORD or IOWR, the GVD will initiate a (VGA) register cycle on the RMbus. If the RMbus returns a hit the GVD will select the command When GMS == 000 : No address compare will occur against VGA memory range or the VGA IO register range. Also, CC[15:8] is changed to 8?h80 from 8'h00
2	0b RO	**RSVD (RSVD_5):** Reserved
1	0b RW/L	**VGA_DISABLE (VGA_DISABLE_6):** VGA Disable (VD): 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[38] = 1) or via a register (DEVEN[3] = 0).
0	0b RW/L	**GGCLCK (GGCLCK_7):** When set to 1b, this bit will lock all bits in this register.

3.3.14 BDSM—Offset 5Ch

This register contains the base address of Graphics Data Stolen DRAM memory. Note : IVB located this register in device 0, 0xB0. Mirrored into device 2, 0x5C.Graphics Stolen Memory is within DRAM space. The base of stolen memory will always be below 4G.

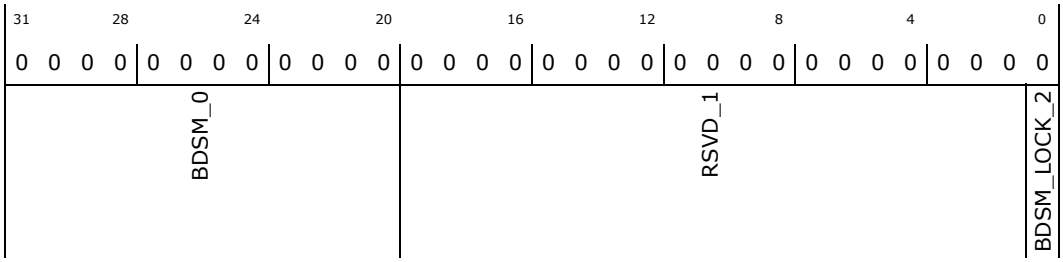
Access Method

Type: PCI Configuration Register (Size: 32 bits)

BDSM: [B:0, D:2, F:0] + 5Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:20	000h RW/L	**BDSM (BDSM_0):** BDSM: BASE_OF_Data_STOLEN_MEMORY. This register contains bits 31 to 20 of the base address of Data stolen DRAM memory. For certain GTLC generated accesses, this base register will be added to the GTLC provided offset address, forming the full physical address for the PFI fabric. This is also used as a base for VGA paged accesses. The display engine also uses the register. Signal : gvd_dsp_cfg_BSM_zcznfwh[31:20].
19:1	00000h RO	**RSVD (RSVD_1):** Reserved
0	0b RW/L	**BDSM_LOCK (BDSM_LOCK_2):** This bit will lock all writeable settings in this register, including itself.

3.3.15 MSAC—Offset 60h

This register determines the size of the graphics memory aperture. Only the system BIOS will write this register based on pre- boot address allocation efforts. Graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume. SOXi Context Save/Restore : Yes.

The size of the aperture must not be modified by software after its location is written into GMADR (offset 18h).

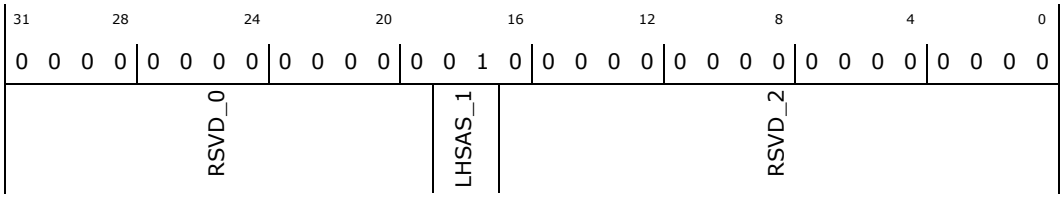
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MSAC: [B:0, D:2, F:0] + 60h

Power Well: Core

Default: 00020000h



Bit Range	Default & Access	Description
31:19	0000h RO	**RSVD (RSVD_0):** Reserved
18:17	01b RW	**LHSAS (LHSAS_1):** Untrusted Aperture Size (LHSAS): 00 : bits [28:27] of GMADR register are made R/W allowing 128MB of GMADR. 01 : bit [28] of GMADR is made R/W and bit [27] of GMADR is forced to zero allowing 256MB of GMADR. 10 : Illegal programming. 11: bits [28:27] of GMADR register are made Read only and forced to zero, allowing only 512MB of GMADR.
16:0	00000h RO	**RSVD (RSVD_2):** Reserved

3.3.16 BGSM—Offset 70h

Base of GTT table in Gfx Stolen Memory SOXi Context Save/Restore : Yes. Note : IVB located this register in device 0, 0xB4. Mirrored into Device 2. The GTT table is located within Graphics Stolen Memory in DRAM space. The base of stolen memory will always be below 4G.

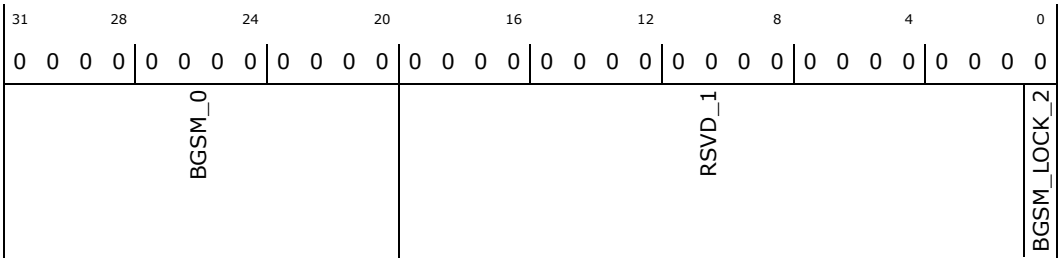
Access Method

Type: PCI Configuration Register (Size: 32 bits)

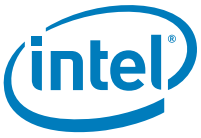
BGSM: [B:0, D:2, F:0] + 70h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:20	000h RW/L	**BGSM (BGSM_0):** BGSM: Gfx Base of GTT Stolen Memory. This register contains bits 31 to 20 of the base address of GTT Table in stolen DRAM memory. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 2 offset 50 bits 9:8) from the Graphics Base of Data Stolen Memory (PCI Device 2 offset 5C bits 31:20). Signal : gvd_dsp_Cspgtbladdr_dczfwohdczfwoh[31:20].Note : was 4KB aligned on CDV ie. [31:12]
19:1	00000h RO	**RSVD (RSVD_1):** Reserved
0	0b RW/L	**BGSM_LOCK (BGSM_LOCK_2):** This bit will lock all writeable settings in this register including itself



3.3.17 PAVPC—Offset 74h

Protected Audio Video Control. Similar to IVB, BIOS will program this register for SoC (not the Gfx Driver). SOXi Context Save/Restore : Yes. For device 2 configuration accesses to 0x74 and Gfx MMIO accesses to 0x1082C0 will both alias to the same register. This register will be located within Gunit.WOPCMBASE is derived from : BDSMbase + GMS size - WOPCMSZ. Note : IVB currently derives from : TOLUD + WOPCMSZ

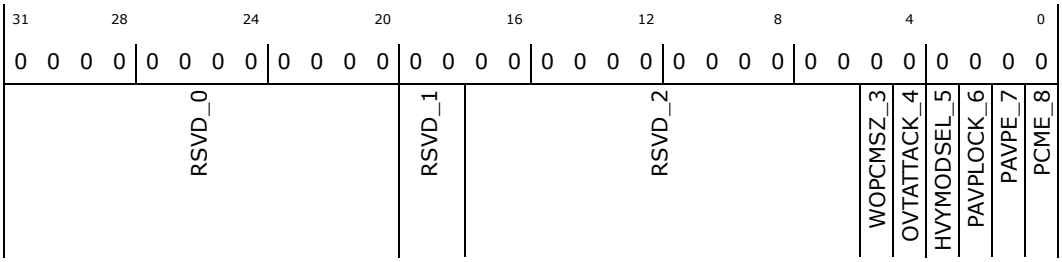
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PAVPC: [B:0, D:2, F:0] + 74h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:20	000h RO	**RSVD (RSVD_0):** Reserved. This field is used to set the base of Protected Content Memory. This corresponds to bits 31:20 of the system memory address range, giving a 1MB granularity. This value MUST be at least 1MB above the base and below the top of stolen memory. This register is locked (becomes read-only) when PAVPLOCK = 1b.
19:18	00b RO	**RSVD (RSVD_1):** Reserved. Note : IVB provided 256KB granularity, so these 2 bits were RW to support that size option. However, VV will only support 1MB so Gunit will tie bits 19:18 to '00'.
17:6	000h RO	**RSVD (RSVD_2):** Reserved
5	0b RO	**WOPCMSZ (WOPCMSZ_3):** 0b ? 1MB Note : IVB had this as a RW bit with value '1' indicating size 256KB support. Since VV only supports 1MB size, this register is RO for VV. These are the only sizes supported for IVB. The IVB is going to run PAVP3 Mode Serpent applications using per-App selection. Therefore, the size chosen should always be 1MB configuration even if Lite mode is chosen using PAVPC register (bit_3 = 0) for PAVP2 Mode Applications. This is because CB^2 code needs to be always loaded, since an App. Which opts for per-App Serpent mode will also execute the CB^2 code). The driver may consider it a BIOS programming error, if PAVPC Serpent Mode is selected with only 256KB of WOPCM size. However PAVPC Lite Mode with 1M WOPCM size is acceptable and not an error, as this may involve per-App selected Serpent Mode.

Bit Range	Default & Access	Description
4	0b RW/L	**OVTATTACK (OVTATTACK_4):** Override of Unsolicited Connection State Attack and Terminate. 0b Disable Override. Attack Terminate allowed. 1b Enable Override. Attack Terminate disallowed. This register bit is locked (becomes read-only) when PAVPLOCK = 1b
3	0b RW/L	**HVYMODSEL (HVYMODSEL_5):** In IVB, this bit is a care only for PAVP2 mode of operation (and a chicken bit is also set). For IVB PAVP2 mode: 0 : Lite Mode (Non-Serpent Mode) 1: Serpent Mode For PAVP3 mode of operation, this bit_3 is a care, only if the per-App Memory Config is disabled due to the clearing of an additional Chicken bit_9 in IVB Crypto Function Control_1 Reg (@ address 0x320F0h). For chicken bit enabled IVB PAVP3 mode, this one type boot time programming has been replaced by per-Media App. Programming (through the Media Crypto Copy command). Note that IVB PAVP2 or PAVP3 Mode selection is done by programming bit_8 of MFX_MODE ? Video Mode Register. (Note again, that when in PAVP3 Mode, the per-App Memory Config. (Serpent/Lite) feature for enabling, requires the further setting of a global one time chicken bit to be set (bit_9 = ?1/ mask_bit_25 = ?1) in the IVB Crypto Function Control_1 Register @ address 0x320F0h).
2	0b RW/L	**PAVPLOCK (PAVPLOCK_6):** This bit will lock all writeable contents in this register when set(including itself).Only a hw reset can unlock the register again. This Lock bit if PAVP is enabled (PAVPE = 1)
1	0b RW/L	**PAVPE (PAVPE_7):** 0: PAVP functionality is disabled. 1: enabled. This register is locked when PAVPLOCK=1
0	0b RW/L	**PCME (PCME_8):** PCME = Protected Content Memory Enable This field enables Protected Content Memory within Graphics Stolen Memory. This memory is the same as the WOPCM area. The size of the WOPCM area is defined by bit_5 of this register. WOPCM is the only remaining flavor of range protected memory. 0: WOPCM protection disabled. 1 : WOPCM protection enabled. This bit must be programmed to 1 when PAVP is enabled. With per-App Memory configuration support in IVB, the range check for the WOPCM memory area should always happen when this bit is set, irrespective of Lite or AES mode programming, or PAVP2 or PAVP3 Mode programming.

3.3.18 MSI_CAPID_MC—Offset 90h

Message Signaled Interrupts Capability ID.SOXi Context Save/Restore : Yes. Message Signaled Control Register. SOXi Context Save/Restore : Yes

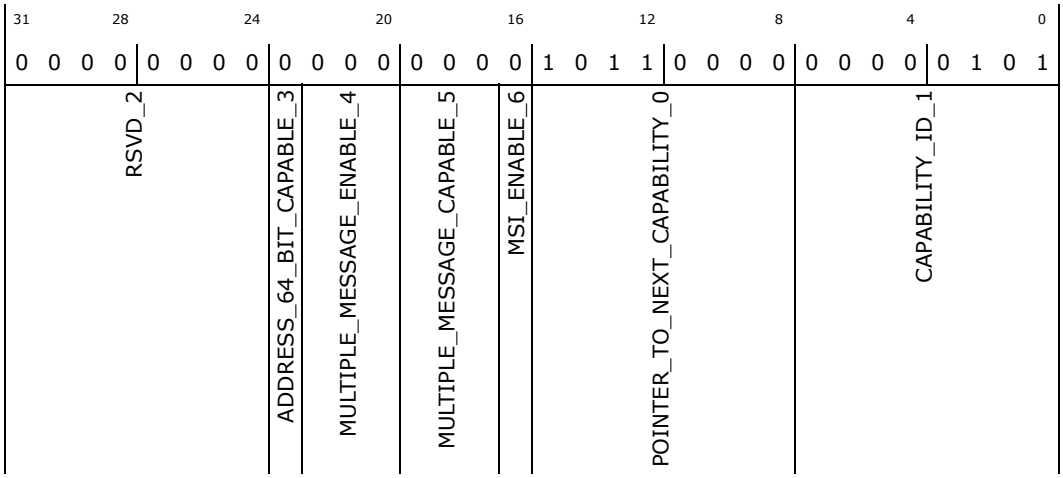
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MSI_CAPID_MC: [B:0, D:2, F:0] + 90h

Power Well: Core

Default: 0000B005h



Bit Range	Default & Access	Description
31:24	00h RO	**RSVD (RSVD_2):** Reserved
23	0b RO	**ADDRESS_64_BIT_CAPABLE (ADDRESS_64_BIT_CAPABLE_3):** C64: 32-bit capable only
22:20	000b RW	**MULTIPLE_MESSAGE_ENABLE (MULTIPLE_MESSAGE_ENABLE_4):** MME: This field is RW for software compatibility, but only a single message is ever generated. System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
19:17	000b RO	**MULTIPLE_MESSAGE_CAPABLE (MULTIPLE_MESSAGE_CAPABLE_5):** MMC: This device is only single message capable System Software reads this field to determine the number of messages being requested by this device. Value: Number of requests 000: 1. 001- 111: Reserved
16	0b RW	**MSI_ENABLE (MSI_ENABLE_6):** MSIE: If set, MSI is enabled and traditional interrupts are not used to generate interrupts. PCICMDSTS.BME must be set for an MSI to be generated. 0 : MSI interrupts are disabled. 1 : MSI interrupts are enabled. Permits sending an MSI interrupt.
15:8	B0h RW/O	**POINTER_TO_NEXT_CAPABILITY (POINTER_TO_NEXT_CAPABILITY_0):** Points to the next item in the list (B0=VCID support). This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.
7:0	05h RO	**CAPABILITY_ID (CAPABILITY_ID_1):** CAPID: Indicates an MSI capability

3.3.19 MA—Offset 94h

Message Address.SOXi Context Save/Restore : Yes

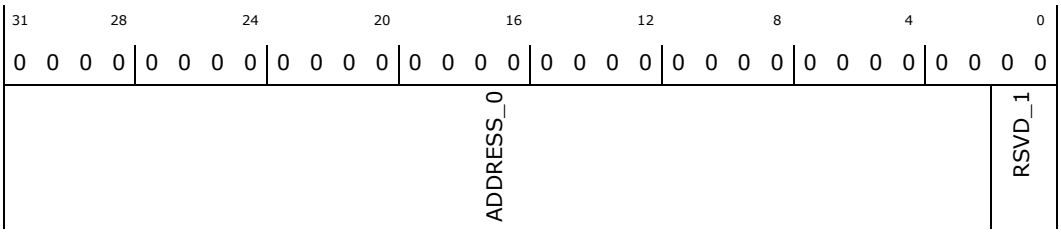
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MA: [B:0, D:2, F:0] + 94h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**ADDRESS (ADDRESS_0):** MA: Lower 32-bits of the system specified message address, always DW aligned. When the GVD issues an MSI interrupt as a MEMWR on the SCL, the memory address corresponds to the value of this field
1:0	00b RO	**RSVD (RSVD_1):** Reserved

3.3.20 MD—Offset 98h

Message Data.SOXi Context Save/Restore : Yes

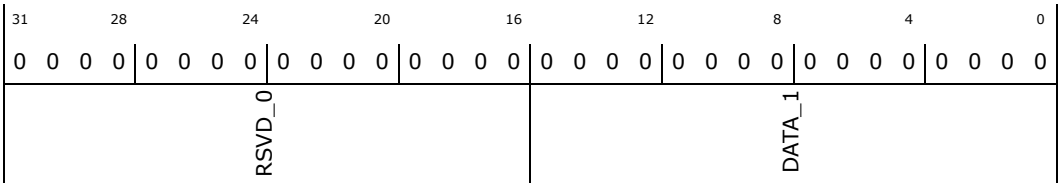
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MD: [B:0, D:2, F:0] + 98h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**RSVD (RSVD_0):** Reserved
15:0	0000h RW	**DATA (DATA_1):** MD: This 16-bit field is programmed by system software. This is forms the lower word of data for the MSI write transaction.

3.3.21 AFLC—Offset A4h

FLR capability advertisement.SOXi Context Save/Restore : Yes

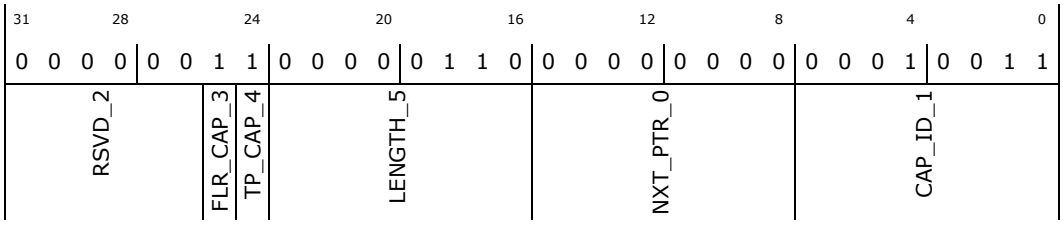
Access Method

Type: PCI Configuration Register (Size: 32 bits)

AFLC: [B:0, D:2, F:0] + A4h

Power Well: Core

Default: 03060013h



Bit Range	Default & Access	Description
31:26	00h RO	**RSVD (RSVD_2):** Reserved
25	1b RO	**FLR_CAP (FLR_CAP_3):** Function Level Reset Capability (FLR_CAP): 0: Function Level Reset is not supported 1: Function Level Reset is supported
24	1b RO	**TP_CAP (TP_CAP_4):** Transactions Pending Capability (TP_CAP): 0: Transactions Pending bit is not supported 1: Transactions Pending bit is supported
23:16	06h RO	**LENGTH (LENGTH_5):** Advanced Features Structure Length (LENGTH): The Advanced Features Capability structure is 6 bytes long.
15:8	00h RW/O	**NXT_PTR (NXT_PTR_0):** Next Pointer (NXT_PTR): Removed FLR capability per HSD 259253. Nulled the next pointer. Points to the next item in the list (B0=Vendor Capabilities ID)This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write once so capabilities list can be changed if needed.
7:0	13h RO	**CAP_ID (CAP_ID_1):** Capability Identifier (CAP_ID): A value of 13h identifies that this PCI Function is capable of Advanced Features.

3.3.22 AFCTLSTS—Offset A8h

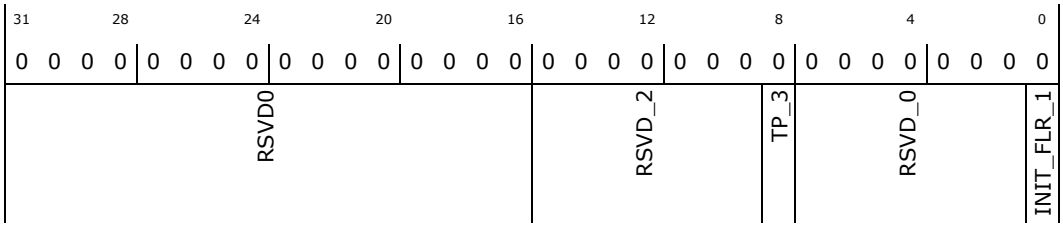
FLR control. Advanced Feature Status.SOXi Context Save/Restore : Not required

Access Method

Type: PCI Configuration Register (Size: 32 bits)

AFCTLSTS: [B:0, D:2, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:9	00h RO	**RSVD (RSVD_2):** Reserved (RSVD):
8	0b RO	**TP (TP_3):** Transaction Pending (TP): 1: The Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. 0: All non-posted transactions have been completed.
7:1	00h RO	**RSVD (RSVD_0):** Reserved (RSVD):
0	0b RW/1S	**INIT_FLR (INIT_FLR_1):** Initiate Function Level Reset (INIT_FLR): A write of 1b initiates Function Level Reset (FLR). FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there. Once written 1, FLR will be initiated. During FLR, a read will return 1?s since device 2 reads abort. Once FLR completes, hardware will clear the bit to 0.

3.3.23 VCID—Offset B0h

Vendor Capability ID.SOXi Context Save/Restore : Yes

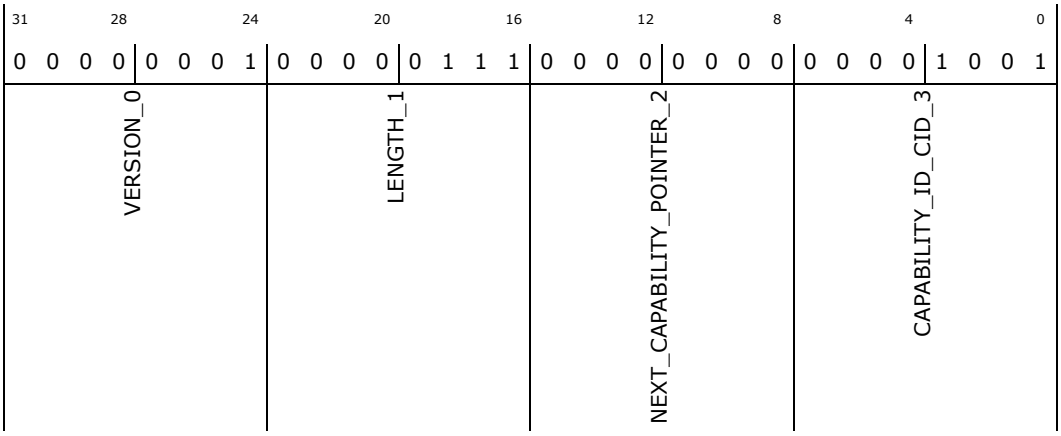
Access Method

Type: PCI Configuration Register (Size: 32 bits)

VCID: [B:0, D:2, F:0] + B0h

Power Well: Core

Default: 01070009h



Bit Range	Default & Access	Description
31:24	01h RO	**VERSION (VERSION_0):** VS: Identifies this as the first revision of the CAPID register definition

Bit Range	Default & Access	Description
23:16	07h RO	**LENGTH (LENGTH_1):** LEN: this field has the value of 07h to indicate structure length (8 bytes)
15:8	00h RW/O	**NEXT_CAPABILITY_POINTER (NEXT_CAPABILITY_POINTER_2):** 00 indicates capability list ends here. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.Write-once allowing the capability list to be changed.
7:0	09h RO	**CAPABILITY_ID_CID (CAPABILITY_ID_CID_3):** Identifies this as a vendor dependent capability pointers

3.3.24 VC—Offset B4h

Vendor Capabilities. Any SKU related fuses would be added here.SOXi Context Save/ Restore : Not required

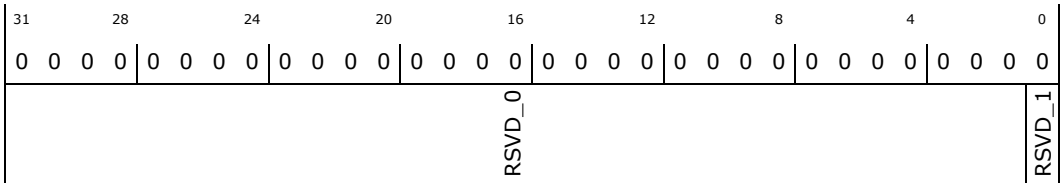
Access Method

Type: PCI Configuration Register (Size: 32 bits)

VC: [B:0, D:2, F:0] + B4h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0000000h RO	**Reserved (RSVD_0):** Reserved
0	0b RO	**Reserved (RSVD_1):** Placeholder for sku related fusing. VLV has no need for this

3.3.25 FD—Offset C4h

Functional Disable. used by SBIOS, not by driver.SOXi Context Save/Restore : Yes

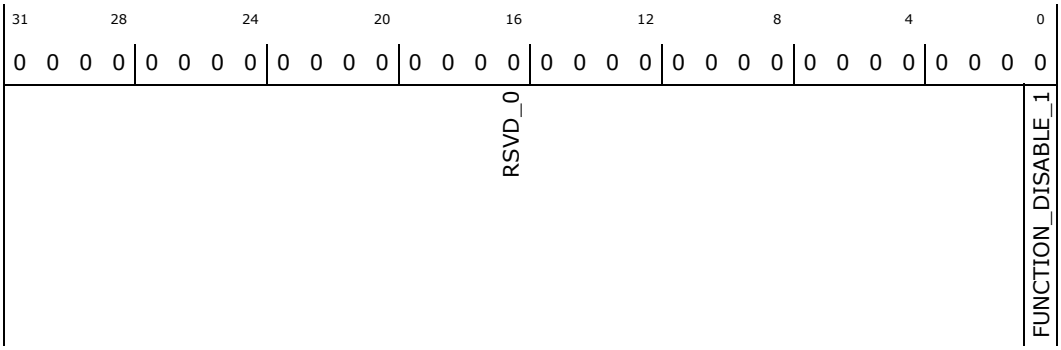
Access Method

Type: PCI Configuration Register (Size: 32 bits)

FD: [B:0, D:2, F:0] + C4h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:1	00000000h RO	**RSVD (RSVD_0):** Reserved
0	0b RW	**FUNCTION_DISABLE (FUNCTION_DISABLE_1):** FD: 0 : Default - normal operation. 1 : When set, the function is disabled (configuration space is disabled). All new requests on the IOSF Primary bus, including any new configuration cycle requests are not claimed on IOSF Primary. This bit as no effect register accessibility via IOSF SB. Once programmed to '1', the only way to re-enable device 2 is via an IOSF SB write of '0' to this register.

3.3.26 PMCAPID—Offset D0h

Power Management Capabilities ID and PM capabilities.SOXi Context Save/Restore : Yes

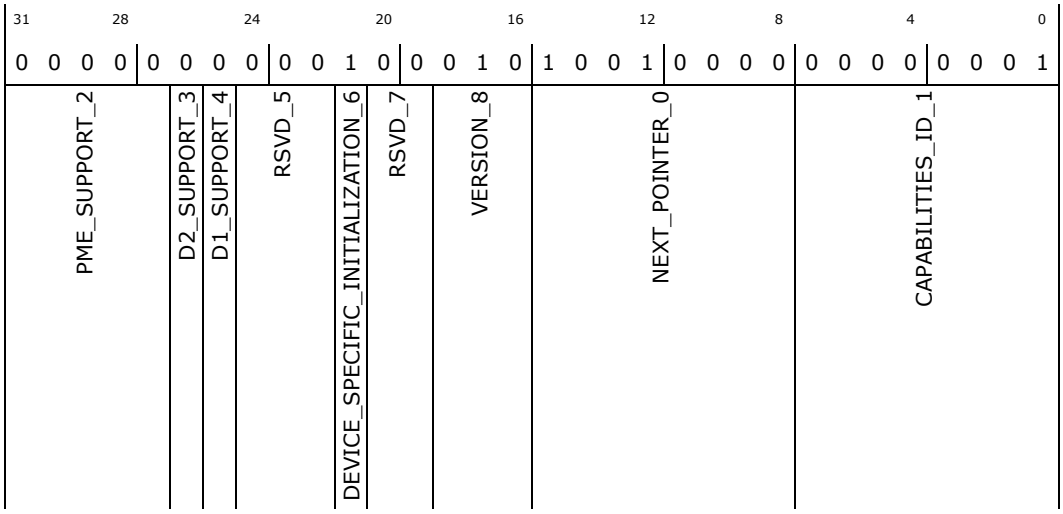
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMCAPID: [B:0, D:2, F:0] + D0h

Power Well: Core

Default: 00229001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_SUPPORT (PME_SUPPORT_2):** PMES The graphics controller does not generate PME
26	0b RO	**D2_SUPPORT (D2_SUPPORT_3):** D2S: D2 not supported
25	0b RO	**D1_SUPPORT (D1_SUPPORT_4):** D1S: D1 not supported
24:22	000b RO	**RSVD (RSVD_5):** Reserved
21	1b RO	**DEVICE_SPECIFIC_INITIALIZATION (DEVICE_SPECIFIC_INITIALIZATION_6):** Hardwired to 1
20:19	00b RO	**RSVD (RSVD_7):** Reserved
18:16	010b RO	**VERSION (VERSION_8):** Version compliance with revision 1.1 of PCI PM spec
15:8	90h RW/O	**NEXT_POINTER (NEXT_POINTER_0):** Indicates the next item in the capabilities list.This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write once allowing changing of the capabilities list.
7:0	01h RO	**CAPABILITIES_ID (CAPABILITIES_ID_1):** CAPID: SIG defines this ID is 01h for PM

3.3.27 PMCS—Offset D4h

Power Management Control/Status. Driver doesn't use this register. SBIOS doesn't use this register SOXi Context Save/Restore : Yes.

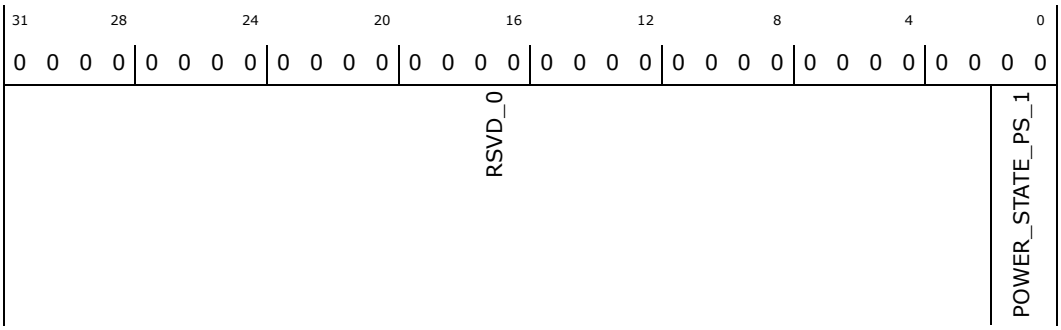
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMCS: [B:0, D:2, F:0] + D4h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RO	**RSVD (RSVD_0):** Reserved
1:0	00b RW	**POWER_STATE_PS (POWER_STATE_PS_1):** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the Bspec. Bits[1:0] Power state 00: D0 Default 01: D1 Not Supported 10: D2 Not Supported 11: D3 Signal : gvd_dsp_power_state_d3_zncznfwoh output to 2D.

3.3.28 SWSMISCI—Offset E0h

Software SMI or SCI.To generate a SW SMI event, software should program bit 15:0 and trigger SMI. Note : ILK/SNB/IVB had SCI and SMI separated (E0 and E8) As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, this must be reserved for this register. The SCI mechanism for driver / BIOS communication. SMI is a system wide lock interrupt (halts the all the cores) as opposed to SCI. Vista and Win7 recommend to use the SCI. The SMI is slowly being phased out. This register serves 2 purposes: 1) Support selection of SMI or SCI event source (SMISCISEL - bit15) 2) Event trigger (bit 0). To generate a SW SCI event, software (System BIOS/Graphics driver) should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a ?0? to ?1? subsequent transition in bit 0 of this register (caused by a software write operation), GMCH sends a single SCI message. The SCI will set the DMISCI bit in its TCO1_STS register and TCOSCI_STS bit in its GPE0 register upon receiving this message from DMI. Once written as 1, software must write a ?0? to this bit to clear it, and all other write transitions (1-)0, 0-)0, 1-)1) or if bit 15 is ?0? will not cause GMCH to send SCI message to DMI link. To generate a SW SMI event, software should program bit 15 to 0 and trigger an SMI.

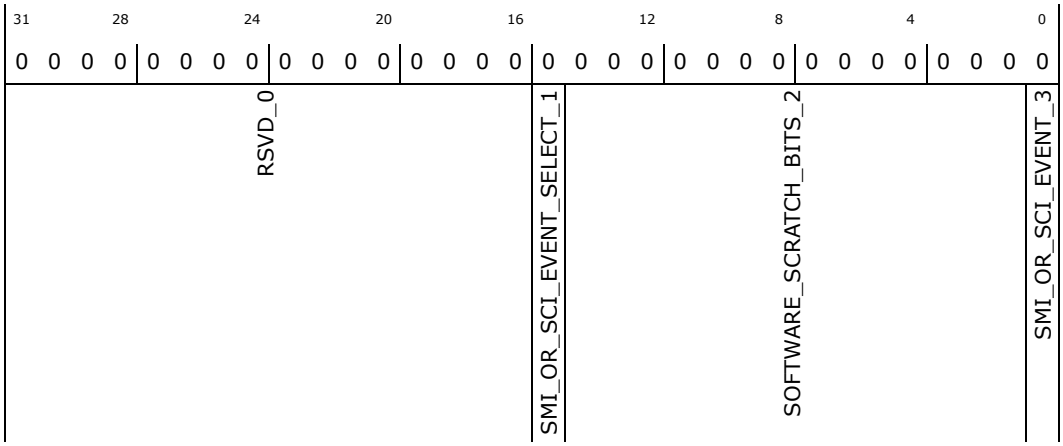
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SWSMISCI: [B:0, D:2, F:0] + E0h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**RSVD (RSVD_0):** Reserved
15	0b RW	**SMI_OR_SCI_EVENT_SELECT (SMI_OR_SCI_EVENT_SELECT_1):** MCS: SMI or SCI event select. 0 = SMI,1 = SCI
14:1	0000h RW	**SOFTWARE_SCRATCH_BITS (SOFTWARE_SCRATCH_BITS_2):** Used by driver to communicate information to SBIOS
0	0b RW	**SMI_OR_SCI_EVENT (SMI_OR_SCI_EVENT_3):** MCE:MCS=1, setting this bit causes an SCI. MCS=0, setting this bit causes an SMI. A 1 to 0, 0 to 0 or 1 to 1 transition of this bit does not trigger any events. The graphics driver writes to this register as a means to interrupt the SBIOS

3.3.29 ASLE—Offset E4h

System Display Event Register. SBIOS writes this reg to generate interrupt to graphics/ display driver.

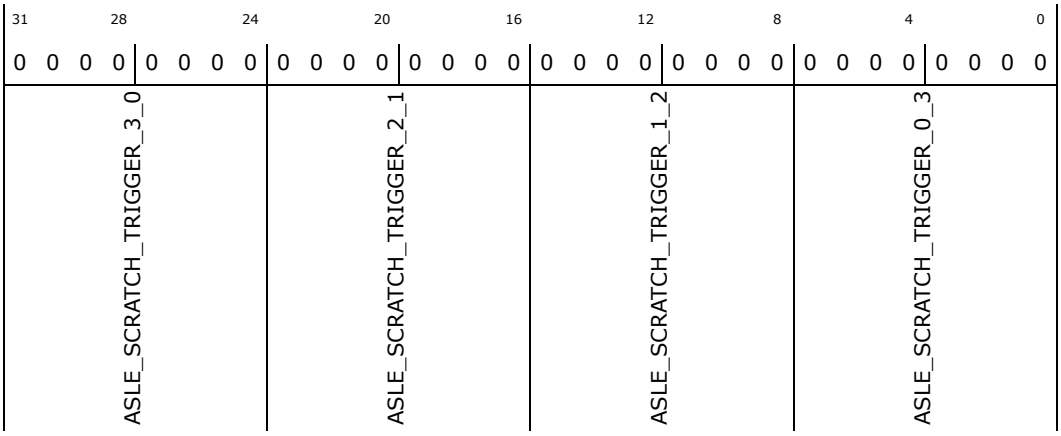
Access Method

Type: PCI Configuration Register (Size: 32 bits)

ASLE: [B:0, D:2, F:0] + E4h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RW	**ASLE_SCRATCH_TRIGGER_3 (ASLE_SCRATCH_TRIGGER_3_0):** AST3: The writing of this by field (byte) ? even if just writing back the original contents ? will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common
23:16	00h RW	**ASLE_SCRATCH_TRIGGER_2 (ASLE_SCRATCH_TRIGGER_2_1):** AST2: The writing of this by field (byte) ? even if just writing back the original contents ? will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common
15:8	00h RW	**ASLE_SCRATCH_TRIGGER_1 (ASLE_SCRATCH_TRIGGER_1_2):** AST1: The writing of this by field (byte) ? even if just writing back the original contents ? will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common
7:0	00h RW	**ASLE_SCRATCH_TRIGGER_0 (ASLE_SCRATCH_TRIGGER_0_3):** AST0: The writing of this by field (byte) ? even if just writing back the original contents ? will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common

3.3.30 MANID—Offset F8h

Manufacturing ID. SOXi Context Save/Restore : Not required

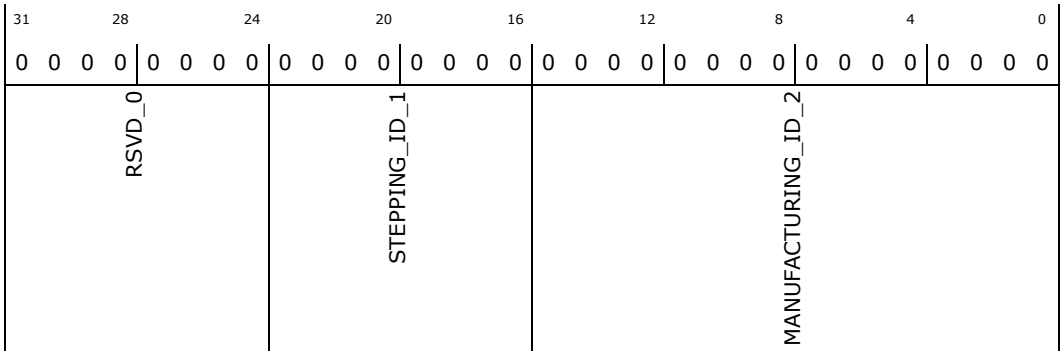
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:2, F:0] + F8h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**RSVD (RSVD_0):** Reserved
23:16	00000000b RO	**Stepping_ID (STEPPING_ID_1):** Hardwired to strapRID[7:0] via top level metal.23:16 - Manufacturing Stepping ID (00 = A0)
15:0	0000h RO	**MANUFACTURING_ID (MANUFACTURING_ID_2):** Hardwired to strapMANID[15:0] via top level metal. 15:8 - Foundry (0Fh = Intel, Others = Reserved) 7:3 - Fab process 12h : Fab code for P1263 13h : P1264 14h : P1265 15h : P1266 ... 1Ah : P1271 (VV POR) Others : Reserved 2:0 - Identifies the dot process 000 = Code for 0 001 = Code for .1 (VV POR) 010 = Code for .2 110 = Code for .4 011 = Code for .7

3.3.31 ASLS—Offset FCh

ASL Storage. The display driver does not need this register since memory Operational Region (OpRegion) is available. This register is kept for use as scratch space. SOXi Context Save/Restore : Yes This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

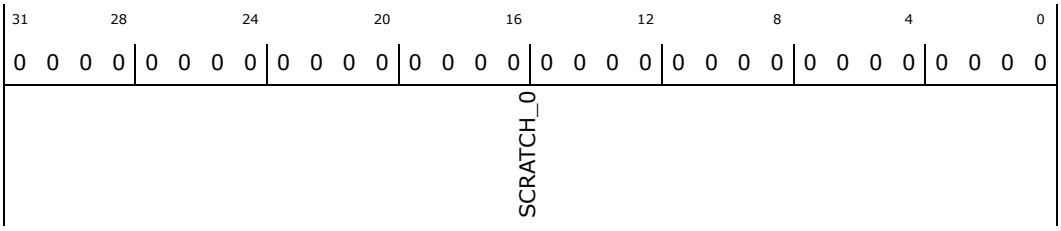
Access Method

Type: PCI Configuration Register (Size: 32 bits)

ASLS: [B:0, D:2, F:0] + FCh

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**SCRATCH (SCRATCH_0):** This register provides a means for the BIOS to communicate with the driver. This definition of this scratch register is worked out in common between System BIOS and driver software. Storage for up to 6 devices is possible. For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).

3.4 Display Memory Mapped Registers (2 of 2)

Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
61050h	4	"CRCCTRLREDB—Offset 61050h" on page 276	00000000h
61054h	4	"CRCCTRLGREENB—Offset 61054h" on page 277	00000000h
61058h	4	"CRCCTRLBLUEB—Offset 61058h" on page 278	00000000h
6105Ch	4	"CRCCTRLALPHAB—Offset 6105Ch" on page 279	00000000h
61060h	4	"CRCRESREDB—Offset 61060h" on page 279	00000000h
61064h	4	"CRCRESGREENB—Offset 61064h" on page 280	00000000h
61068h	4	"CRCRESBLUEB—Offset 61068h" on page 281	00000000h
6106Ch	4	"CRCRESALPHAB—Offset 6106Ch" on page 282	00000000h
61070h	4	"CRCCTRLRESIDUE2B—Offset 61070h" on page 283	00000000h
61080h	4	"CRCRESRESIDUAL2B—Offset 61080h" on page 284	00000000h
61090h	4	"PSRCTLB—Offset 61090h" on page 285	00000000h
61094h	4	"PSRSTATB—Offset 61094h" on page 286	00000000h
61098h	4	"PSRCRC1B—Offset 61098h" on page 287	00000000h
6109Ch	4	"PSRCRC2B—Offset 6109Ch" on page 288	00000000h
610A0h	4	"VSCSDPB—Offset 610A0h" on page 289	00000000h
610B0h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 610B0h" on page 290	00000000h
610B4h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 610B4h" on page 291	00000000h
610B8h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 610B8h" on page 291	00000000h
610BCh	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 610BCh" on page 292	00000000h
610C0h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 610C0h" on page 293	00000000h
610C4h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 610C4h" on page 294	00000000h
61100h	4	"ADPA—Offset 61100h" on page 294	00040000h
61104h	4	"CRTIO_DFX—Offset 61104h" on page 297	00008000h
61110h	4	"PORT_HOTPLUG_EN—Offset 61110h" on page 298	00000020h
61114h	4	"PORT_HOTPLUG_STAT—Offset 61114h" on page 300	00000000h
61140h	4	"SDVOHDMIB—Offset 61140h" on page 305	00000018h
61154h	4	"SDVOHDMIB—Offset 61140h" on page 305	00000000h
61160h	4	"HDMIC—Offset 61160h" on page 310	00000018h
61164h	4	"DISPLAY_DIGITAL_PORT_HOT_PLUG_CONTROL_REGISTER—Offset 61164h" on page 314	00000000h

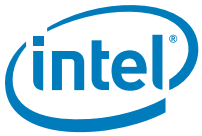


Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
61168h	4	"DV_DETERM—Offset 61168h" on page 317	00000000h
61170h	4	"VIDEO_DIP_CTL_B—Offset 61170h" on page 319	20200900h
61174h	4	"VIDEO_DIP_DATA_B—Offset 61174h" on page 320	00000000h
61178h	4	"VIDEO_DIP_GDCP_PAYLOAD_B—Offset 61178h" on page 321	00000000h
61190h	4	"MIPIA_PORT_CTRL—Offset 61190h" on page 321	00000000h
61194h	4	"MIPIA_TEARING_CTR—Offset 61194h" on page 327	00000000h
61198h	4	"DPA_PIX_GEN_CTRL—Offset 61198h" on page 328	00000000h
611A0h	4	"MIPIA_AUTOPWG—Offset 611A0h" on page 329	00000000h
611B0h	4	"DPB_PIX_GEN_CTRL—Offset 611B0h" on page 329	00000000h
61200h	4	"PIPEA_PP_STATUS—Offset 61200h" on page 331	08000000h
61204h	4	"PIPEA_PP_CONTROL—Offset 61204h" on page 332	00000000h
61208h	4	"PIPEA_PP_ON_DELAYS—Offset 61208h" on page 334	00000000h
6120Ch	4	"PIPEA_PP_OFF_DELAYS—Offset 6120Ch" on page 335	00000000h
61210h	4	"PIPEA_PP_DIVISOR—Offset 61210h" on page 336	00270F04h
61230h	4	"PFIT_CONTROL—Offset 61230h" on page 337	20000000h
61234h	4	"PFIT_PGM_RATIOS—Offset 61234h" on page 339	00000000h
61238h	4	"RESERVEDUSEDTOBEAUTOSCALINGRATIOSREADBACK—Offset 61238h" on page 340	00000000h
6123Ch	4	"RESERVEDUSEDTOBESCALINGINITIALPHASE—Offset 6123Ch" on page 341	00000000h
61250h	4	"PIPEA_BLC_PWM_CLT2—Offset 61250h" on page 341	00000000h
61254h	4	"PIPEA_BLC_PWM_CTL—Offset 61254h" on page 343	00000000h
61260h	4	"PIPEA_BLM_HIST_CTL—Offset 61260h" on page 343	00000000h
61264h	4	"PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61264h" on page 345	00000000h
61268h	4	"PIPEAHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61268h" on page 346	00000000h
61300h	4	"PIPEB_PP_STATUS—Offset 61300h" on page 347	08000000h
61304h	4	"PIPEB_PP_CONTROL—Offset 61304h" on page 349	00000000h
61308h	4	"PIPEB_PP_ON_DELAYS—Offset 61308h" on page 351	00000000h
6130Ch	4	"PIPEB_PP_OFF_DELAYS—Offset 6130Ch" on page 352	00000000h
61310h	4	"PIPEB_PP_DIVISOR—Offset 61310h" on page 353	00270F04h
61350h	4	"PIPEB_BLC_PWM_CLT2—Offset 61350h" on page 354	00000000h
61354h	4	"PIPEB_BLC_PWM_CTL—Offset 61354h" on page 355	00000000h
61360h	4	"PIPEB_BLM_HIST_CTL—Offset 61360h" on page 356	00000000h
61364h	4	"PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61364h" on page 358	00000000h

Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
61368h	4	"PIPEBHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61368h" on page 359	00000000h
61700h	4	"MIPIC_PORT_CTRL—Offset 61700h" on page 360	00000000h
61704h	4	"MIPIC_TEARING_CTR—Offset 61704h" on page 361	00000000h
62000h	4	"AUD_CONFIG_A—Offset 62000h" on page 362	00000000h
62010h	4	"AUD_MISC_CTRL_A—Offset 62010h" on page 363	00000044h
62020h	4	"AUD_VID_DID—Offset 62020h" on page 364	80862882h
62024h	4	"AUD_RID—Offset 62024h" on page 365	00100000h
62028h	4	"AUD_CTS_ENABLE_A—Offset 62028h" on page 366	00000000h
6204Ch	4	"AUD_PWRST—Offset 6204Ch" on page 367	00FFFFFFh
62050h	4	"AUD_HDMIW_HDMIEDID_A—Offset 62050h" on page 369	00000000h
62054h	4	"AUD_HDMIW_INFOFR_A—Offset 62054h" on page 369	00000000h
6207Ch	4	"AUD_PORT_EN_HD_CFG—Offset 6207Ch" on page 370	00077003h
62080h	4	"AUD_OUT_DIG_CNVT_A—Offset 62080h" on page 372	00000000h
62084h	4	"AUD_OUT_STR_DESC_A—Offset 62084h" on page 373	00000032h
62088h	4	"AUD_OUT_CH_STR—Offset 62088h" on page 375	00000000h
620A8h	4	"AUD_PINW_CONNLNG_LIST—Offset 620A8h" on page 376	00030202h
620ACh	4	"AUD_PINW_CONNLNG_SEL—Offset 620ACh" on page 377	00000000h
620B4h	4	"AUD_CNTL_ST_A—Offset 620B4h" on page 378	00005400h
620C0h	4	"AUD_CNTL_ST2—Offset 620C0h" on page 379	00000000h
620D4h	4	"AUD_HDMIW_STATUS—Offset 620D4h" on page 381	00000000h
62100h	4	"AUD_CONFIG_B—Offset 62100h" on page 382	00000000h
62110h	4	"AUD_MISC_CTRL_B—Offset 62110h" on page 383	00000044h
62128h	4	"AUD_CTS_ENABLE_B—Offset 62128h" on page 384	00000000h
62150h	4	"AUD_HDMIW_HDMIEDID_B—Offset 62150h" on page 385	00000000h
62154h	4	"AUD_HDMIW_INFOFR_B—Offset 62154h" on page 386	00000000h
62180h	4	"AUD_OUT_DIG_CNVT_B—Offset 62180h" on page 387	00000000h
62184h	4	"AUD_OUT_STR_DESC_B—Offset 62184h" on page 388	00000032h
621B4h	4	"AUD_CNTL_ST_B—Offset 621B4h" on page 389	00005400h
62F00h	4	"AUD_SSID_DBG—Offset 62F00h" on page 391	80860101h
62F04h	4	"AUD_PWST1_DBG—Offset 62F04h" on page 391	00000C0Fh
62F08h	4	"AUD_OUT_STR_DESC_A_DBG—Offset 62F08h" on page 392	00000032h
62F0Ch	4	"AUD_OUT_DIG_CNVT_A_DBG—Offset 62F0Ch" on page 394	00000001h
62F14h	4	"AUD_PWST2_DBG—Offset 62F14h" on page 395	0000000Fh
62F18h	4	"AUD_OUT_STR_DESC_B_DBG—Offset 62F18h" on page 396	00000032h
62F1Ch	4	"AUD_OUT_DIG_CNVT_B_DBG—Offset 62F1Ch" on page 398	00000001h

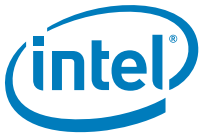


Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
62F20h	4	"AUD_PORT_EN_B_DBG—Offset 62F20h" on page 400	00000003h
62F24h	4	"AUD_PWST3_DBG—Offset 62F24h" on page 401	00000003h
62F28h	4	"AUD_PORT_EN_C_DBG—Offset 62F28h" on page 401	00000003h
62F2Ch	4	"AUD_PORT_EN_D_DBG—Offset 62F2Ch" on page 403	00000003h
62F38h	4	"AUD_CHICKENBIT_REG—Offset 62F38h" on page 404	00000001h
62F40h	4	"AUD_OUT_DIG_CNVTA_DBG—Offset 62F40h" on page 405	00000000h
62F44h	4	"AUD_OUT_DIG_CNVTB_DBG—Offset 62F44h" on page 406	00000000h
62F60h	4	"AUD_CNTL_ST_B_DBG—Offset 62F60h" on page 406	00000000h
62F64h	4	"AUD_HDMIW_INFOFR_B_DBG—Offset 62F64h" on page 407	00000000h
62F70h	4	"AUD_CNTL_ST_C_DBG—Offset 62F70h" on page 408	00000000h
62F74h	4	"AUD_HDMIW_INFOFR_C_DBG—Offset 62F74h" on page 409	00000000h
62F80h	4	"AUD_CNTL_ST_D_DBG—Offset 62F80h" on page 410	00000000h
62F84h	4	"AUD_HDMIW_INFOFR_D_DBG—Offset 62F84h" on page 411	00000000h
62F88h	4	"AUD_CONFIG_DEFAULT2_REG_PORTB—Offset 62F88h" on page 412	00000000h
62F8Ch	4	"AUD_CONFIG_DEFAULT2_REG_PORTC—Offset 62F8Ch" on page 413	00000000h
62F90h	4	"AUD_CONFIG_DEFAULT2_REG_PORTD—Offset 62F90h" on page 413	00000000h
62F94h	4	"AUD_MCTSA—Offset 62F94h" on page 414	00000000h
62F98h	4	"AUD_MCTSB—Offset 62F98h" on page 414	00000000h
64100h	4	"DP_B—Offset 64100h" on page 415	00000018h
64110h	4	"DPB_AUX_CH_CTL—Offset 64110h" on page 417	00050000h
64114h	4	"DPB_AUX_CH_DATA1—Offset 64114h" on page 419	00000000h
64118h	4	"DPB_AUX_CH_DATA2—Offset 64118h" on page 420	00000000h
6411Ch	4	"DPB_AUX_CH_DATA3—Offset 6411Ch" on page 421	00000000h
64120h	4	"DPB_AUX_CH_DATA4—Offset 64120h" on page 421	00000000h
64124h	4	"DPB_AUX_CH_DATA5—Offset 64124h" on page 422	00000000h
64130h	4	"DP_AUX_CH_AKSV_HI—Offset 64130h" on page 423	00000000h
64134h	4	"DP_AUX_CH_AKSV_LO—Offset 64134h" on page 423	00000000h
64150h	4	"DPB_AUX_TST—Offset 64150h" on page 424	00000000h
64200h	4	"DP_C—Offset 64200h" on page 427	00000018h
64210h	4	"DPC_AUX_CH_CTL—Offset 64210h" on page 429	00050000h
64214h	4	"DPC_AUX_CH_DATA1—Offset 64214h" on page 431	00000000h
64218h	4	"DPC_AUX_CH_DATA2—Offset 64218h" on page 432	00000000h
6421Ch	4	"DPC_AUX_CH_DATA3—Offset 6421Ch" on page 433	00000000h
64220h	4	"DPC_AUX_CH_DATA4—Offset 64220h" on page 433	00000000h
64224h	4	"DPC_AUX_CH_DATA5—Offset 64224h" on page 434	00000000h
64228h	4	"DPC_AUX_TST—Offset 64228h" on page 434	00000000h

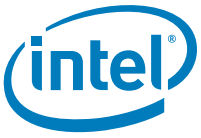


Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
65000h	4	"STREAM_A_LPE_AUD_CONFIG—Offset 65000h" on page 436	00000280h
65008h	4	"STREAM_A_LPE_AUD_CH_STATUS_0—Offset 65008h" on page 438	00000000h
6500Ch	4	"STREAM_A_LPE_AUD_CH_STATUS_1—Offset 6500Ch" on page 439	00000000h
65010h	4	"STREAM_A_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65010h" on page 440	00000000h
65014h	4	"STREAM_A_LPE_AUD_HDMI_N_DP_NAUD—Offset 65014h" on page 441	00000000h
65020h	4	"STREAM_A_LPE_AUD_BUFFER_CONFIG—Offset 65020h" on page 442	00000100h
65024h	4	"STREAM_A_LPE_AUD_BUF_CH_SWP—Offset 65024h" on page 442	00FAC688h
65040h	4	"STREAM_A_LPE_AUD_BUF_A_ADDR—Offset 65040h" on page 444	00000000h
65044h	4	"STREAM_A_LPE_AUD_BUF_A_LENGTH—Offset 65044h" on page 445	00000000h
65048h	4	"STREAM_A_LPE_AUD_BUF_B_ADDR—Offset 65048h" on page 445	00000000h
6504Ch	4	"STREAM_A_LPE_AUD_BUF_B_LENGTH—Offset 6504Ch" on page 446	00000000h
65050h	4	"STREAM_A_LPE_AUD_BUF_C_ADDR—Offset 65050h" on page 447	00000000h
65054h	4	"STREAM_A_LPE_AUD_BUF_C_LENGTH—Offset 65054h" on page 447	00000000h
65058h	4	"STREAM_A_LPE_AUD_BUF_D_ADDR—Offset 65058h" on page 448	00000000h
6505Ch	4	"STREAM_A_LPE_AUD_BUF_D_LENGTH—Offset 6505Ch" on page 449	00000000h
65060h	4	"STREAM_A_LPE_AUD_CNTL_ST—Offset 65060h" on page 449	00000000h
65064h	4	"STREAM_A_LPE_AUD_HDMI_STATUS—Offset 65064h" on page 451	00000000h
65068h	4	"STREAM_A_LPE_AUD_HDMIW_INFOFR—Offset 65068h" on page 453	00000000h
65800h	4	"STREAM_B_LPE_AUD_CONFIG—Offset 65800h" on page 454	00000280h
65808h	4	"STREAM_B_LPE_AUD_CH_STATUS_0—Offset 65808h" on page 456	00000000h
6580Ch	4	"STREAM_B_LPE_AUD_CH_STATUS_1—Offset 6580Ch" on page 457	00000000h
65810h	4	"STREAM_B_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65810h" on page 457	00000000h
65814h	4	"STREAM_B_LPE_AUD_HDMI_N_DP_NAUD—Offset 65814h" on page 458	00000000h
65820h	4	"STREAM_B_LPE_AUD_BUFFER_CONFIG—Offset 65820h" on page 459	00000100h
65824h	4	"STREAM_B_LPE_AUD_BUF_CH_SWP—Offset 65824h" on page 460	00FAC688h
65840h	4	"STREAM_B_LPE_AUD_BUF_A_ADDR—Offset 65840h" on page 462	00000000h
65844h	4	"STREAM_B_LPE_AUD_BUF_A_LENGTH—Offset 65844h" on page 462	00000000h
65848h	4	"STREAM_B_LPE_AUD_BUF_B_ADDR—Offset 65848h" on page 463	00000000h
6584Ch	4	"STREAM_B_LPE_AUD_BUF_B_LENGTH—Offset 6584Ch" on page 464	00000000h
65850h	4	"STREAM_B_LPE_AUD_BUF_C_ADDR—Offset 65850h" on page 464	00000000h
65854h	4	"STREAM_B_LPE_AUD_BUF_C_LENGTH—Offset 65854h" on page 465	00000000h
65858h	4	"STREAM_B_LPE_AUD_BUF_D_ADDR—Offset 65858h" on page 466	00000000h
6585Ch	4	"STREAM_B_LPE_AUD_BUF_D_LENGTH—Offset 6585Ch" on page 467	00000000h
65860h	4	"STREAM_B_LPE_AUD_CNTL_ST—Offset 65860h" on page 467	00000000h

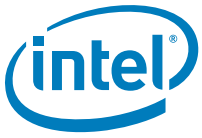


Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
65864h	4	"STREAM_B_LPE_AUD_HDMI_STATUS—Offset 65864h" on page 469	00000000h
65868h	4	"STREAM_B_LPE_AUD_HDMIW_INFOFR—Offset 65868h" on page 471	00000000h
70000h	4	"PIPEA_DSL—Offset 70000h" on page 472	00000000h
70004h	4	"PIPEA_SLC—Offset 70004h" on page 473	00000000h
70008h	4	"PIPEACONF—Offset 70008h" on page 474	00000000h
70010h	4	"PIPEAGCMAXRED—Offset 70010h" on page 480	00010000h
70014h	4	"PIPEAGCMAXGREEN—Offset 70014h" on page 481	00010000h
70018h	4	"PIPEAGCMAXBLUE—Offset 70018h" on page 482	00010000h
70024h	4	"PIPEASTAT—Offset 70024h" on page 483	00000000h
70028h	4	"DPFLIPSTAT—Offset 70028h" on page 487	00000000h
7002Ch	4	"DPINVGTT—Offset 7002Ch" on page 491	00000000h
70030h	4	"DSPARB—Offset 70030h" on page 493	80008000h
70034h	4	"FW1—Offset 70034h" on page 494	3F8F0F0Fh
70038h	4	"FW2—Offset 70038h" on page 496	0B0F0F0Fh
7003Ch	4	"FW3—Offset 7003Ch" on page 497	00000000h
70040h	4	"PIPEAFRAMECOUNT—Offset 70040h" on page 498	00000000h
70044h	4	"PIPEAFLIPCOUNT—Offset 70044h" on page 499	00000000h
70048h	4	"PIPEAMSAMISC—Offset 70048h" on page 500	00000000h
70050h	4	"DDL1—Offset 70050h" on page 501	00000000h
70054h	4	"DDL2—Offset 70054h" on page 502	00000000h
70060h	4	"DSPARB2—Offset 70060h" on page 504	00001111h
70064h	4	"DSPHOWM—Offset 70064h" on page 505	00000000h
70068h	4	"DSPHOWM1—Offset 70068h" on page 508	00000000h
70070h	4	"FW4—Offset 70070h" on page 510	00040404h
70074h	4	"FW5—Offset 70074h" on page 511	04040404h
70078h	4	"FW6—Offset 70078h" on page 512	00000078h
7007Ch	4	"FW7—Offset 7007Ch" on page 513	040F040Fh
70080h	4	"CURACNTR—Offset 70080h" on page 514	00000000h
70084h	4	"CURABASE—Offset 70084h" on page 515	00000000h
70088h	4	"CURAPOS—Offset 70088h" on page 517	00000000h
70090h	4	"CURAPALET_0—Offset 70090h" on page 518	00000000h
70094h	4	"CURAPALET_1—Offset 70094h" on page 519	00000000h
70098h	4	"CURAPALET_2—Offset 70098h" on page 520	00000000h
7009Ch	4	"CURAPALET_3—Offset 7009Ch" on page 521	00000000h
700ACh	4	"CURALIVEBASE—Offset 700ACh" on page 522	00000000h
700C0h	4	"CURBCNTR—Offset 700C0h" on page 523	00000000h

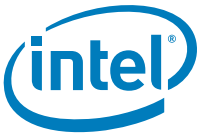


Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
700C4h	4	"CURBBASE—Offset 700C4h" on page 524	00000000h
700C8h	4	"CURBPOS—Offset 700C8h" on page 526	00000000h
700D0h	4	"CURBPALET_0—Offset 700D0h" on page 528	00000000h
700D4h	4	"CURBPALET_1—Offset 700D4h" on page 528	00000000h
700D8h	4	"CURBPALET_2—Offset 700D8h" on page 529	00000000h
700DCh	4	"CURBPALET_3—Offset 700DCh" on page 530	00000000h
700ECh	4	"CURBLIVEBASE—Offset 700ECh" on page 531	00000000h
7017Ch	4	"DSPAADDR—Offset 7017Ch" on page 533	00000000h
70180h	4	"DSPACNTR—Offset 70180h" on page 534	00000000h
70184h	4	"DSPALINOFF—Offset 70184h" on page 537	00000000h
70188h	4	"DSPASTRIDE—Offset 70188h" on page 538	00000000h
70194h	4	"DSPAKEYVAL—Offset 70194h" on page 539	00000000h
70198h	4	"DSPAKEYMSK—Offset 70198h" on page 539	00000000h
7019Ch	4	"DSPASURF—Offset 7019Ch" on page 540	00000000h
701A4h	4	"DSPATILEOFF—Offset 701A4h" on page 541	00000000h
701ACh	4	"DSPASURFLIVE—Offset 701ACh" on page 542	00000000h
70400h	4	"CBR1—Offset 70400h" on page 543	00000000h
70404h	4	"CBR2—Offset 70404h" on page 546	00000000h
70408h	4	"CCBR—Offset 70408h" on page 548	00000000h
7040Ch	4	"CBR3—Offset 7040Ch" on page 549	00000000h
70410h	4	"SWF00—Offset 70410h" on page 551	00000000h
70414h	4	"SWF01—Offset 70414h" on page 551	00000000h
70418h	4	"SWF02—Offset 70418h" on page 552	00000000h
7041Ch	4	"SWF03—Offset 7041Ch" on page 552	00000000h
70420h	4	"SWF04—Offset 70420h" on page 553	00000000h
70424h	4	"SWF05—Offset 70424h" on page 553	00000000h
70428h	4	"SWF06—Offset 70428h" on page 554	00000000h
7042Ch	4	"SWF07—Offset 7042Ch" on page 554	00000000h
70430h	4	"SWF08—Offset 70430h" on page 555	00000000h
70434h	4	"SWF09—Offset 70434h" on page 555	00000000h
70438h	4	"SWF0A—Offset 70438h" on page 556	00000000h
7043Ch	4	"SWF0B—Offset 7043Ch" on page 556	00000000h
70440h	4	"SWF0C—Offset 70440h" on page 557	00000000h
70444h	4	"SWF0D—Offset 70444h" on page 557	00000000h
70448h	4	"SWF0E—Offset 70448h" on page 558	00000000h
7044Ch	4	"SWF0F—Offset 7044Ch" on page 558	00000000h

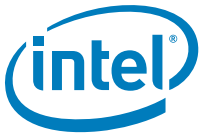


Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
70450h	4	"CBR4—Offset 70450h" on page 559	00000000h
71000h	4	"PIPEB_DSL—Offset 71000h" on page 561	00000000h
71004h	4	"PIPEB_SLC—Offset 71004h" on page 562	00000000h
71008h	4	"PIPEBCONF—Offset 71008h" on page 563	00000000h
71010h	4	"PIPEBGCMAXRED—Offset 71010h" on page 566	00010000h
71014h	4	"PIPEBGCMAXGREEN—Offset 71014h" on page 567	00010000h
71018h	4	"PIPEBGCMAXBLUE—Offset 71018h" on page 568	00010000h
71024h	4	"PIPEBSTAT—Offset 71024h" on page 569	00000000h
71040h	4	"PIPEBFRAMECOUNT—Offset 71040h" on page 573	00000000h
71044h	4	"PIPEBFLIPCOUNT—Offset 71044h" on page 574	00000000h
71048h	4	"PIPEBMSAMISC—Offset 71048h" on page 574	00000000h
7117Ch	4	"DSPBADDR—Offset 7117Ch" on page 575	00000000h
71180h	4	"DSPBCNTR—Offset 71180h" on page 577	01000000h
71184h	4	"DSPBLINOFFSET—Offset 71184h" on page 579	00000000h
71188h	4	"DSPBSTRIDE—Offset 71188h" on page 580	00000000h
71194h	4	"DSPBKEYVAL—Offset 71194h" on page 581	00000000h
71198h	4	"DSPBKEYMSK—Offset 71198h" on page 582	00000000h
7119Ch	4	"DSPBSURF—Offset 7119Ch" on page 582	00000000h
711A4h	4	"DSPBTILEOFF—Offset 711A4h" on page 583	00000000h
711ACh	4	"DSPBSURFLIVE—Offset 711ACh" on page 584	00000000h
71200h	4	"DSPBFLPQSTAT—Offset 71200h" on page 585	00000000h
71400h	4	"VGACNTRL—Offset 71400h" on page 586	00000000h
71410h	4	"SWF10—Offset 71410h" on page 589	00000000h
71414h	4	"SWF11—Offset 71414h" on page 590	00000000h
71418h	4	"SWF12—Offset 71418h" on page 590	00000000h
7141Ch	4	"SWF13—Offset 7141Ch" on page 591	00000000h
71420h	4	"SWF14—Offset 71420h" on page 591	00000000h
71424h	4	"SWF15—Offset 71424h" on page 592	00000000h
71428h	4	"SWF16—Offset 71428h" on page 592	00000000h
7142Ch	4	"SWF17—Offset 7142Ch" on page 593	00000000h
71430h	4	"SWF18—Offset 71430h" on page 593	00000000h
71434h	4	"SWF19—Offset 71434h" on page 594	00000000h
71438h	4	"SWF1A—Offset 71438h" on page 594	00000000h
7143Ch	4	"SWF1B—Offset 7143Ch" on page 595	00000000h
71440h	4	"SWF1C—Offset 71440h" on page 595	00000000h
71444h	4	"SWF1D—Offset 71444h" on page 596	00000000h

Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
71448h	4	"SWF1E—Offset 71448h" on page 596	00000000h
7144Ch	4	"SWF1F—Offset 7144Ch" on page 597	00000000h
72180h	4	"SPACNTR—Offset 72180h" on page 597	00000000h
72184h	4	"SPALINOFF—Offset 72184h" on page 600	00000000h
72188h	4	"SPASTRIDE—Offset 72188h" on page 601	00000000h
7218Ch	4	"SPAPOS—Offset 7218Ch" on page 601	00000000h
72190h	4	"SPASIZE—Offset 72190h" on page 602	00000000h
72194h	4	"SPAKEYMINVAL—Offset 72194h" on page 603	00000000h
72198h	4	"SPAKEYMSK—Offset 72198h" on page 604	00000000h
7219Ch	4	"SPASURF—Offset 7219Ch" on page 605	00000000h
721A0h	4	"SPAKEYMAXVAL—Offset 721A0h" on page 606	00000000h
721A4h	4	"SPATILEOFF—Offset 721A4h" on page 607	00000000h
721A8h	4	"SPACONTALPHA—Offset 721A8h" on page 608	00000000h
721ACh	4	"SPALIVESURF—Offset 721ACh" on page 609	00000000h
721D0h	4	"SPACLRC0—Offset 721D0h" on page 610	01000000h
721D4h	4	"SPACLRC1—Offset 721D4h" on page 611	00000080h
721E0h	4	"SPAGAMC5—Offset 721E0h" on page 612	00C0C0C0h
721E4h	4	"SPAGAMC4—Offset 721E4h" on page 613	00808080h
721E8h	4	"SPAGAMC3—Offset 721E8h" on page 613	00404040h
721ECh	4	"SPAGAMC2—Offset 721ECh" on page 614	00202020h
721F0h	4	"SPAGAMC1—Offset 721F0h" on page 615	00101010h
721F4h	4	"SPAGAMC0—Offset 721F4h" on page 615	00080808h
72280h	4	"SPBCNTR—Offset 72280h" on page 616	00000000h
72284h	4	"SPBLINOFF—Offset 72284h" on page 619	00000000h
72288h	4	"SPBSTRIDE—Offset 72288h" on page 619	00000000h
7228Ch	4	"SPBPOS—Offset 7228Ch" on page 620	00000000h
72290h	4	"SPBSIZE—Offset 72290h" on page 621	00000000h
72294h	4	"SPBKEYMINVAL—Offset 72294h" on page 622	00000000h
72298h	4	"SPBKEYMSK—Offset 72298h" on page 623	00000000h
7229Ch	4	"SPBSURF—Offset 7229Ch" on page 624	00000000h
722A0h	4	"SPBKEYMAXVAL—Offset 722A0h" on page 625	00000000h
722A4h	4	"SPBTILEOFF—Offset 722A4h" on page 626	00000000h
722A8h	4	"SPBCONTALPHA—Offset 722A8h" on page 627	00000000h
722ACh	4	"SPBLIVESURF—Offset 722ACh" on page 628	00000000h
722D0h	4	"SPBCLRC0—Offset 722D0h" on page 629	01000000h
722D4h	4	"SPBCLRC1—Offset 722D4h" on page 630	00000080h

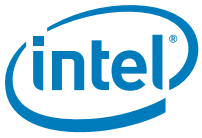


Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
722E0h	4	"SPBGAMC5—Offset 722E0h" on page 631	00C0C0C0h
722E4h	4	"SPBGAMC4—Offset 722E4h" on page 632	00808080h
722E8h	4	"SPBGAMC3—Offset 722E8h" on page 632	00404040h
722ECh	4	"SPBGAMC2—Offset 722ECh" on page 633	00202020h
722F0h	4	"SPBGAMC1—Offset 722F0h" on page 634	00101010h
722F4h	4	"SPBGAMC0—Offset 722F4h" on page 634	00080808h
72380h	4	"SPCCNTR—Offset 72380h" on page 635	00000000h
72384h	4	"SPCLINOFF—Offset 72384h" on page 638	00000000h
72388h	4	"SPCSTRIDE—Offset 72388h" on page 638	00000000h
7238Ch	4	"SPCPOS—Offset 7238Ch" on page 639	00000000h
72390h	4	"SPCSIZE—Offset 72390h" on page 640	00000000h
72394h	4	"SPCKEYMINVAL—Offset 72394h" on page 641	00000000h
72398h	4	"SPCKEYMSK—Offset 72398h" on page 642	00000000h
7239Ch	4	"SPCSURF—Offset 7239Ch" on page 643	00000000h
723A0h	4	"SPCKEYMAXVAL—Offset 723A0h" on page 644	00000000h
723A4h	4	"SPCTILEOFF—Offset 723A4h" on page 645	00000000h
723A8h	4	"SPCCONTALPHA—Offset 723A8h" on page 646	00000000h
723ACh	4	"SPCLIVESURF—Offset 723ACh" on page 647	00000000h
723D0h	4	"SPCCLRC0—Offset 723D0h" on page 648	01000000h
723D4h	4	"SPCCLRC1—Offset 723D4h" on page 649	00000080h
723E0h	4	"SPCGAMC5—Offset 723E0h" on page 650	00C0C0C0h
723E4h	4	"SPCGAMC4—Offset 723E4h" on page 651	00808080h
723E8h	4	"SPCGAMC3—Offset 723E8h" on page 651	00404040h
723ECh	4	"SPCGAMC2—Offset 723ECh" on page 652	00202020h
723F0h	4	"SPCGAMC1—Offset 723F0h" on page 653	00101010h
723F4h	4	"SPCGAMC0—Offset 723F4h" on page 653	00080808h
72414h	4	"SWF30—Offset 72414h" on page 654	00000000h
72418h	4	"SWF31—Offset 72418h" on page 655	00000000h
7241Ch	4	"SWF32—Offset 7241Ch" on page 655	00000000h
72480h	4	"SPDCNTR—Offset 72480h" on page 656	00000000h
72484h	4	"SPDLINOFF—Offset 72484h" on page 658	00000000h
72488h	4	"SPDSTRIDE—Offset 72488h" on page 659	00000000h
7248Ch	4	"SPDPOS—Offset 7248Ch" on page 659	00000000h
72490h	4	"SPDSIZE—Offset 72490h" on page 660	00000000h
72494h	4	"SPDKEYMINVAL—Offset 72494h" on page 661	00000000h
72498h	4	"SPDKEYMSK—Offset 72498h" on page 662	00000000h

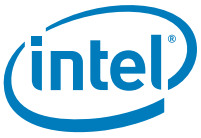


Table 12. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
7249Ch	4	"SPDSURF—Offset 7249Ch" on page 663	00000000h
724A0h	4	"SPDKEYMAXVAL—Offset 724A0h" on page 664	00000000h
724A4h	4	"SPDTILEOFF—Offset 724A4h" on page 665	00000000h
724A8h	4	"SPDCONTALPHA—Offset 724A8h" on page 666	00000000h
724ACh	4	"SPDLIVESURF—Offset 724ACh" on page 667	00000000h
724D0h	4	"SPDCLRC0—Offset 724D0h" on page 668	01000000h
724D4h	4	"SPDCLRC1—Offset 724D4h" on page 669	00000080h
724E0h	4	"SPDGAMC5—Offset 724E0h" on page 670	00C0C0C0h
724E4h	4	"SPDGAMC4—Offset 724E4h" on page 671	00808080h
724E8h	4	"SPDGAMC3—Offset 724E8h" on page 671	00404040h
724ECh	4	"SPDGAMC2—Offset 724ECh" on page 672	00202020h
724F0h	4	"SPDGAMC1—Offset 724F0h" on page 673	00101010h
724F4h	4	"SPDGAMC0—Offset 724F4h" on page 673	00080808h
73000h	4	"PCSRC—Offset 73000h" on page 674	00000000h
73004h	4	"PCSTAT—Offset 73004h" on page 676	00000000h
73008h	4	"PCSRC2—Offset 73008h" on page 678	00000000h
7300Ch	4	"PCSTAT2—Offset 7300Ch" on page 680	00000000h

3.4.1 CRCCTRLREDB—Offset 61050h

Pipe B CRC Color Control Register (Red)

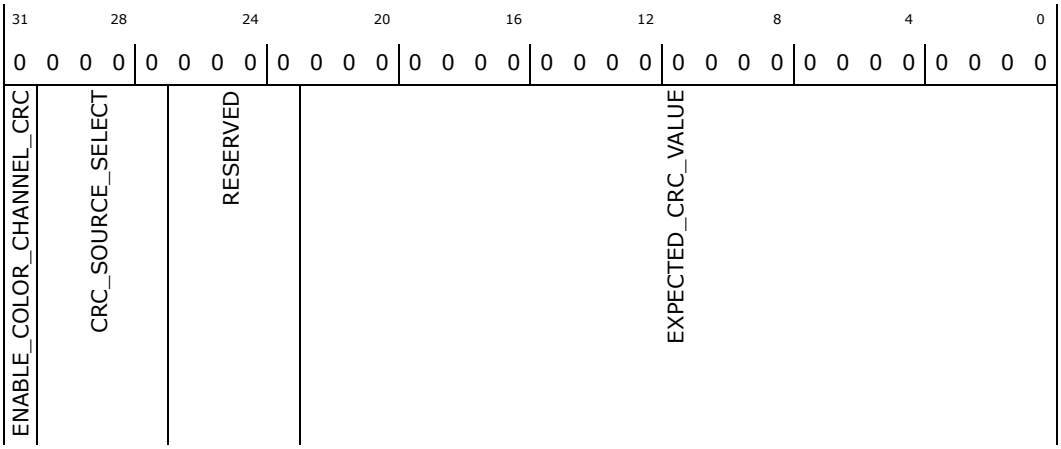
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCCTRLREDB: [GTTMMADR_LSB + 2BF20h] + 61050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**ENABLE_COLOR_CHANNEL_CRC:** After being enabled for the first time, you need to wait for two VBLANK events for a valid CRC result. After that, a CRC will be generated each frame. 0 = CRC Calculations are disabled 1 = CRC Calculations are enabled
30:27	0b RW	**CRC_SOURCE_SELECT:** These bits select the source of the data to put into the CRC logic. 0000: Pipe B (Not available when DisplayPort or TV is enabled on this pipe) [DevVLVP] 0001: sDVOB/HDMIB (30 bit format. Only select when HDMIB is set to pipe B) [DevVLVP] 0010: sDVOC/HDMIC (30 bit format. Only select when HDMIC is set to pipe B) [DevVLVP] 0011: DisplayPort D (40 bit format) [DevCTG] 0100: TV Encoder outputs (30 bit format) 0101: TV filter outputs (30 bit format) 0110: DisplayPort B (40 bit format) [DevCTG, DevCDV, DevVLVP] 0111: DisplayPort C (40 bit format) [DevCTG, DevCDV, DevVLVP] 1000: Audio DP (Audio for DisplayPort (pcdclk). Only select when Audio is on DisplayPort on Pipe B) [DevVLVP] 1001: Audio HDMI (Audio for HDMI (dotclock) Only select when Audio is on HDMI on Pipe B) Others: Reserved
26:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

3.4.2 CRCCTRLGREENB—Offset 61054h

Pipe B CRC Color Control Register

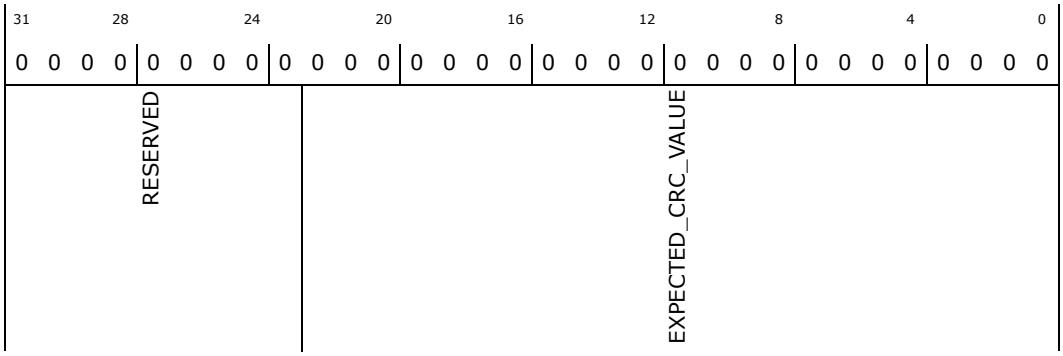
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCCTRLGREENB: [GTTMMADR_LSB + 2BF20h] + 61054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

3.4.3 CRCCTRLBLUEB—Offset 61058h

Pipe B CRC Color Control Register

Access Method

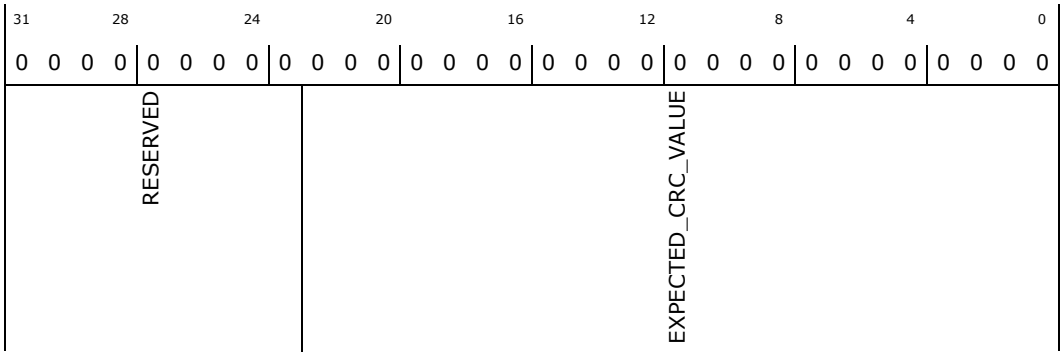
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCCTRLBLUEB: [GTTMMADR_LSB + 2BF20h] + 61058h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Description
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

3.4.4 CRCCTRLALPHAB—Offset 6105Ch

Pipe B CRC Color Control Register

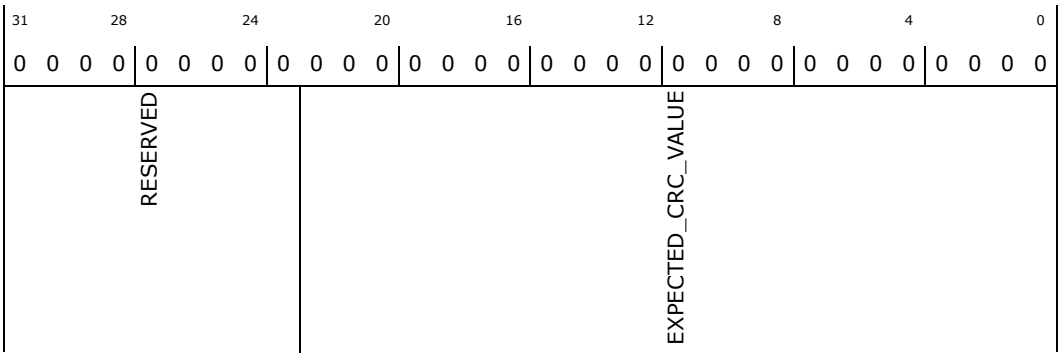
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCCTRLALPHAB: [GTTMMADR_LSB + 2BF20h] + 6105Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

3.4.5 CRCRESREDB—Offset 61060h

Pipe B CRC Result Register

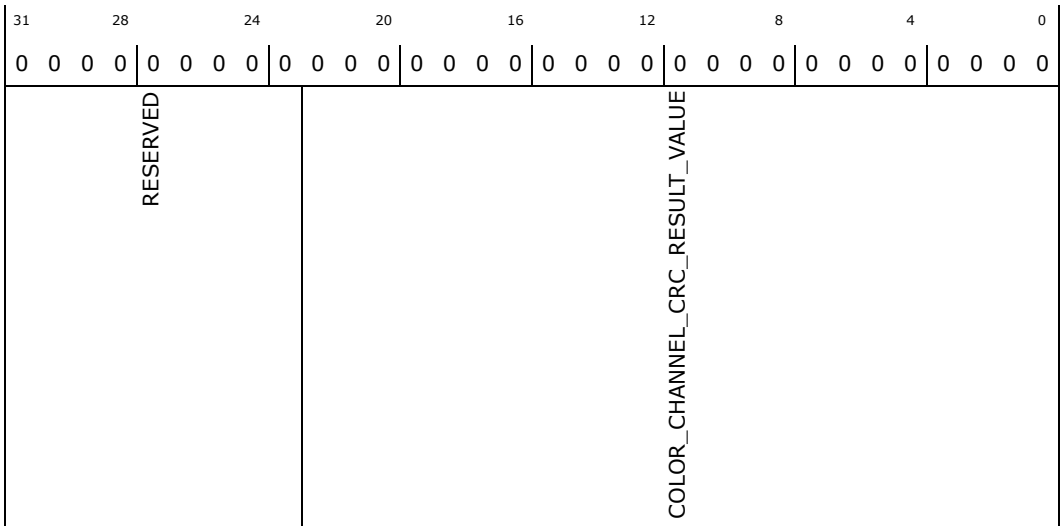
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCRESREDB: [GTTMMADR_LSB + 2BF20h] + 61060h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

3.4.6 CRCRESGREENB—Offset 61064h

Pipe B CRC Result Register

Access Method

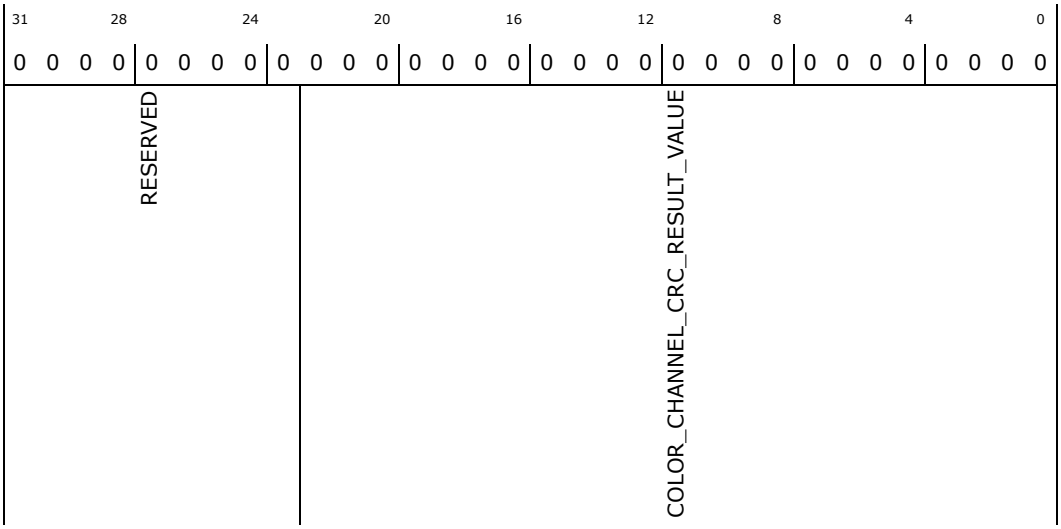
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCRESGREENB: [GTTMMADR_LSB + 2BF20h] + 61064h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

3.4.7 CRCRESBLUEB—Offset 61068h

Pipe B CRC Result Register

Access Method

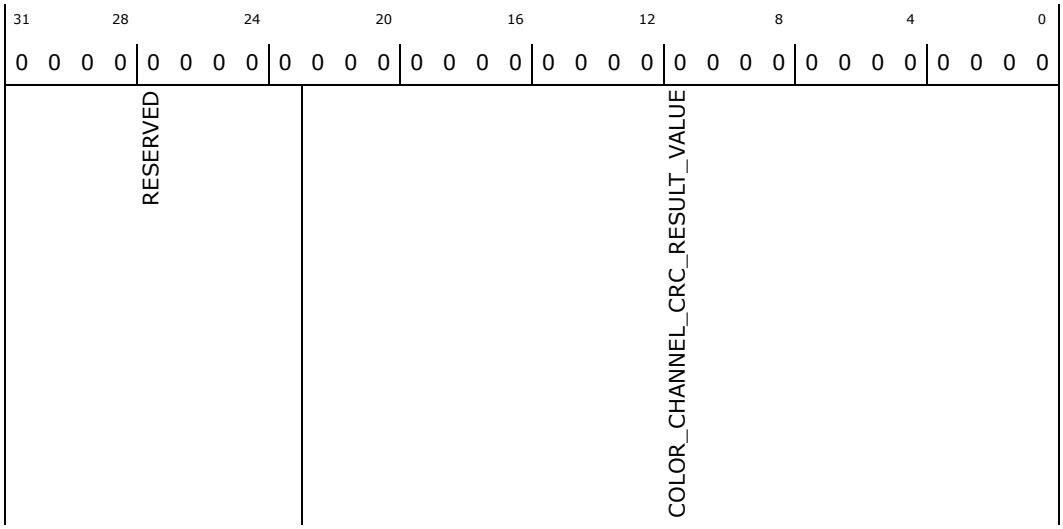
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCRESBLUEB: [GTTMMADR_LSB + 2BF20h] + 61068h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

3.4.8 CRCRESALPHAB—Offset 6106Ch

Pipe B CRC Result Register

Access Method

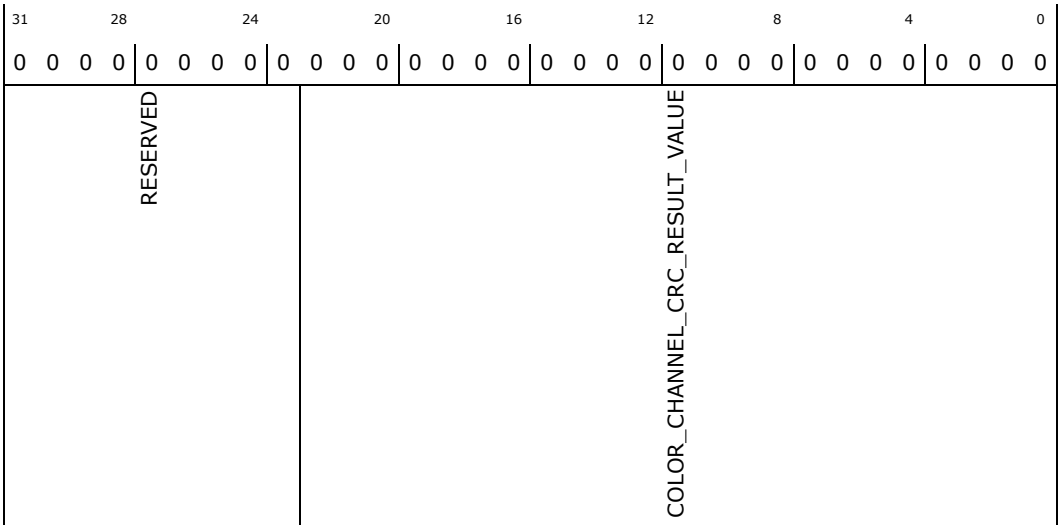
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCRESALPHAB: [GTTMMADR_LSB + 2BF20h] + 6106Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

3.4.9 CRCCTRLRESIDUE2B—Offset 61070h

Pipe B CRC Color Control Register

Access Method

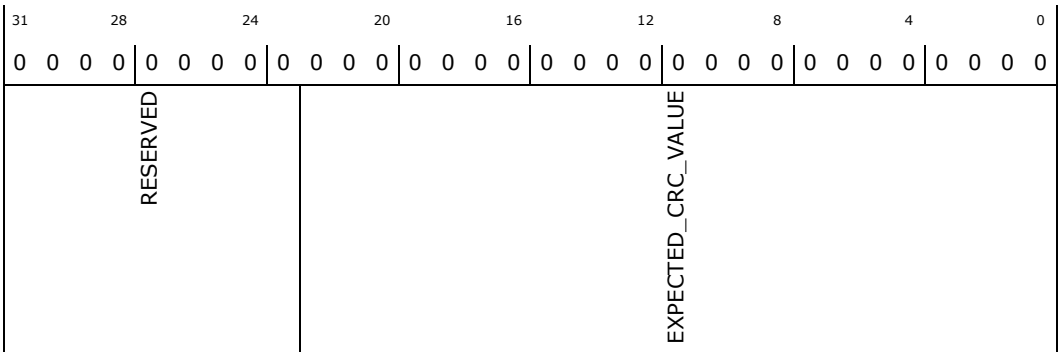
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCCTRLRESIDUE2B: [GTTMMADR_LSB + 2BF20h] + 61070h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

3.4.10 CRCRESRESIDUAL2B—Offset 61080h

Pipe B CRC Result Register

Access Method

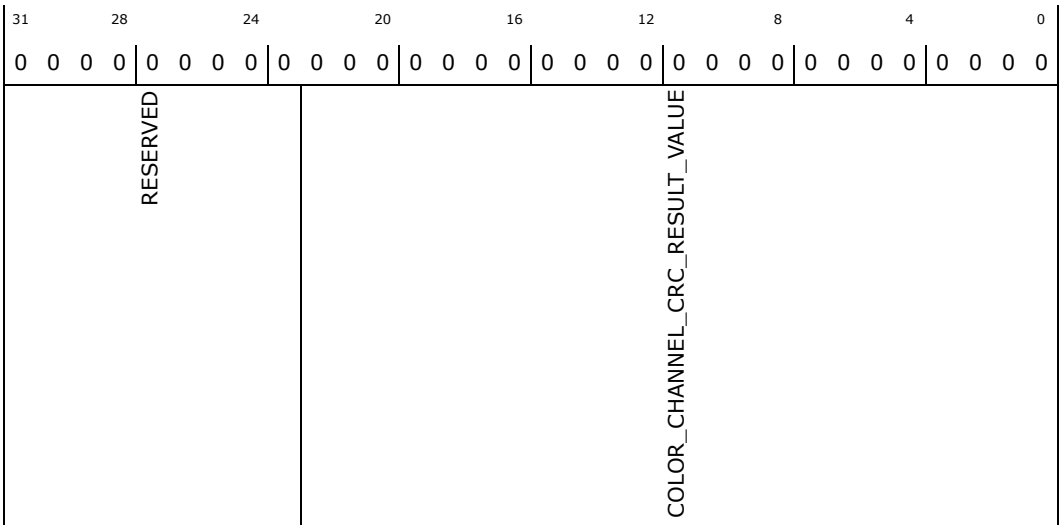
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCRESRESIDUAL2B: [GTTMMADR_LSB + 2BF20h] + 61080h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

3.4.11 PSRCTLB—Offset 61090h

Pipe B Panel Self Refresh Control

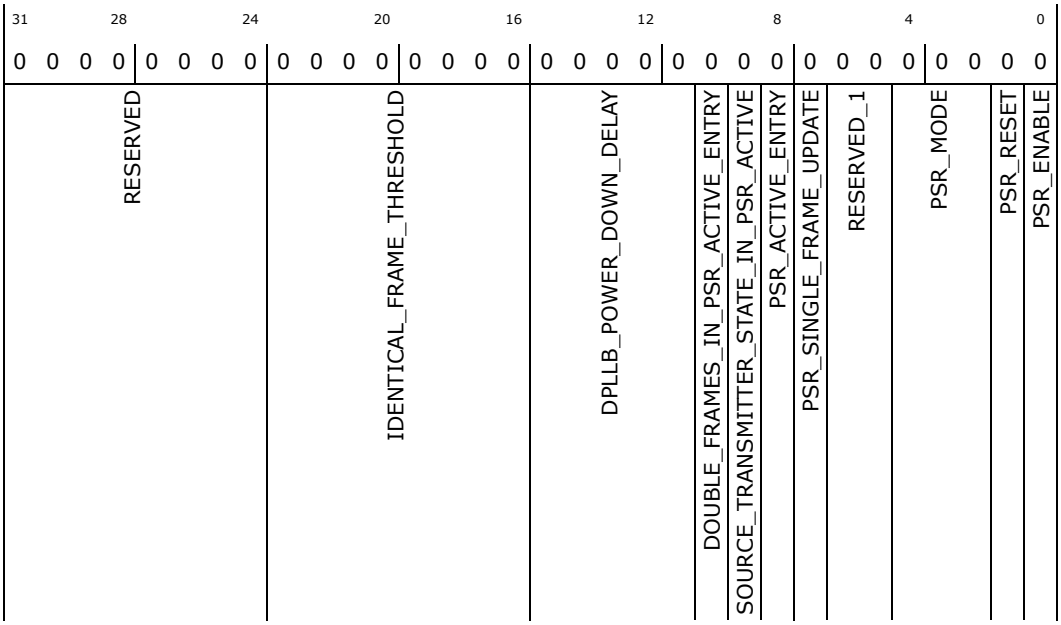
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PSRCTLB: [GTTMMADR_LSB + 2BF20h] + 61090h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**IDENTICAL_FRAME_THRESHOLD:** : Number of identical frames that display controller needs to exceed in order to transition to PSR active state in HW timer mode
15:11	0b RW	**DPLLB_POWER_DOWN_DELAY:** programmable delay from main link powerdown to DPLLB powerdown. The delay is in number of cdclk clocks.
10	0b RW	**DOUBLE_FRAMES_IN_PSR_ACTIVE_ENTRY:** . If asserted, HW will send two frames with same SDP active setting when entry PSR active state. This bit is set if the vertical blanking time is less than 330us.
9	0b RW	**SOURCE_TRANSMITTER_STATE_IN_PSR_ACTIVE:** . If asserted, HW will keep transmitter active during PSR active state and sends only idle symbols. If deasserted, HW will turn off transmitter during PSR active state. Display driver will keep this bit consistent with Source transmitter state in PSR active bit in DPCD register of the sink.

Bit Range	Default & Access	Description
8	0b RW	**PSR_ACTIVE_ENTRY:** This bit is only valid in PSR_mode is SW timer mode. If it is asserted, HW will transition into PSR_active state. If it is deasserted, HW will transition to PSR_inactive state. SW should not set or clear this bit more than once within one vblank period.
7	0b RW	**PSR_SINGLE_FRAME_UPDATE:** In PSR SW or HW mode, SW set this bit before writing registers for a flip. After HW finishes single frame update, it goes back to PSR active ? no RFB state. SW driver may send new single frame update request. Programming note: Reading this bit is updated at the next vblank. Writing this bit to 1 will cause PSR FSM to perform single frame update automatically, no vblank is required. When single frame update is done, it will automatically go back to PSR active ? no RFB update. 61094[2:0] = 3b011.
6:5	0b RW	**RESERVED_1:** Reserved.
4:2	0b RW	**PSR_MODE:** b011-111: reserved. b010: PSR with HW timer. HW timer decides PSR active entry point. PSR active state exits upon MMIO write registers that may change the frame buffer. b001: PSR with SW timer. In this mode, SW will keep track of idle frames and buffer modification in the driver and explicitly specify the entry and exit PSR active state point. b000: PSR manual (debug) mode. All of PSR state transitions and SDP content is managed by SW driver. SW is responsible to change SDP content for every frame with appropriate values to keep PSR panel in synchronized states.
1	0b RW	**PSR_RESET:** If assert all PSR functions are reset back to PSR inactive state. When it needs to resynchronize source and sync, SW writes 0x2 to DPCD register 600h and to this bit to get system back to PSR active states. This bit is self clear.
0	0b RW	**PSR_ENABLE:** Panel Self-refresh is enabled. When it is asserted PSR is enabled and operate in one of the mode that specified by PSR mode.

3.4.12 PSRSTATB—Offset 61094h

Pipe B PSR status register

Access Method

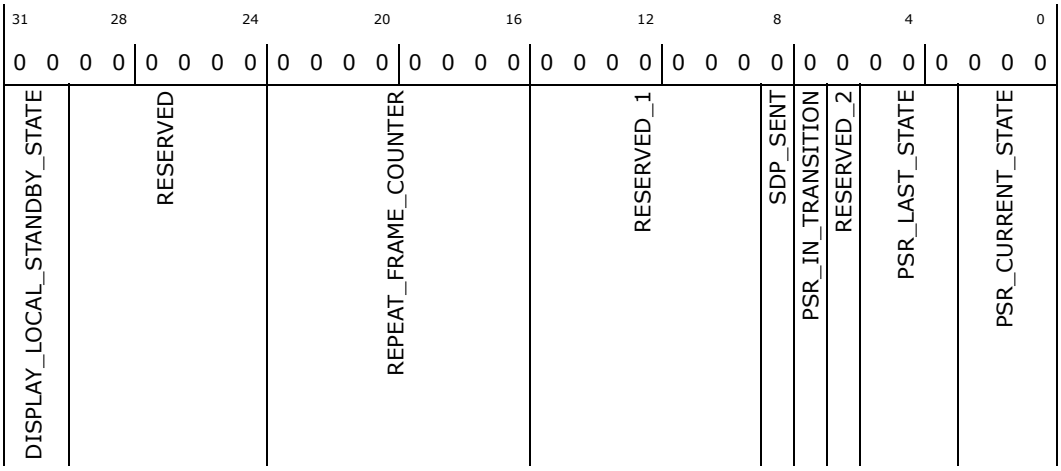
Type: Memory Mapped I/O Register (Size: 32 bits)

PSRSTATB: [GTTMMADR_LSB + 2BF20h] + 61094h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RO	**DISPLAY_LOCAL_STANDBY_STATE:** :00: D0 idle state, fetch frame buffer from system memory 01: D0i1 not defined in VLVP 02: D0i2 PSR is active, display controller is trunk gated 03: D0i3 PSR is active, display controller is power gated
29:24	0b RO	**RESERVED:** Reserved.
23:16	0b RO	**REPEAT_FRAME_COUNTER:** : Number of identical frames has been sent by display controller. Value is not roll over at 255.
15:9	0b RO	**RESERVED_1:** Reserved.
8	0b RO	**SDP_SENT:** it indicates if SDP packet has been sent in current frame.
7	0b RO	**PSR_IN_TRANSITION:** There is a period that source already committed to PSR active but sink did not. SW should not change the source state at this time but wait until this status bit is clear. The wait time should in the range of 120-250us in the worst case.
6	0b RO	**RESERVED_2:** Reserved.
5:3	0b RO	**PSR_LAST_STATE:** indicate last source state that VLVP PSR state machine were in (debug) 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit
2:0	0b RO	**PSR_CURRENT_STATE:** indicate current source state that VLVP PSR state machine are in 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit

3.4.13 PSRCRC1B—Offset 61098h

Pipe B PSR CRC1 register

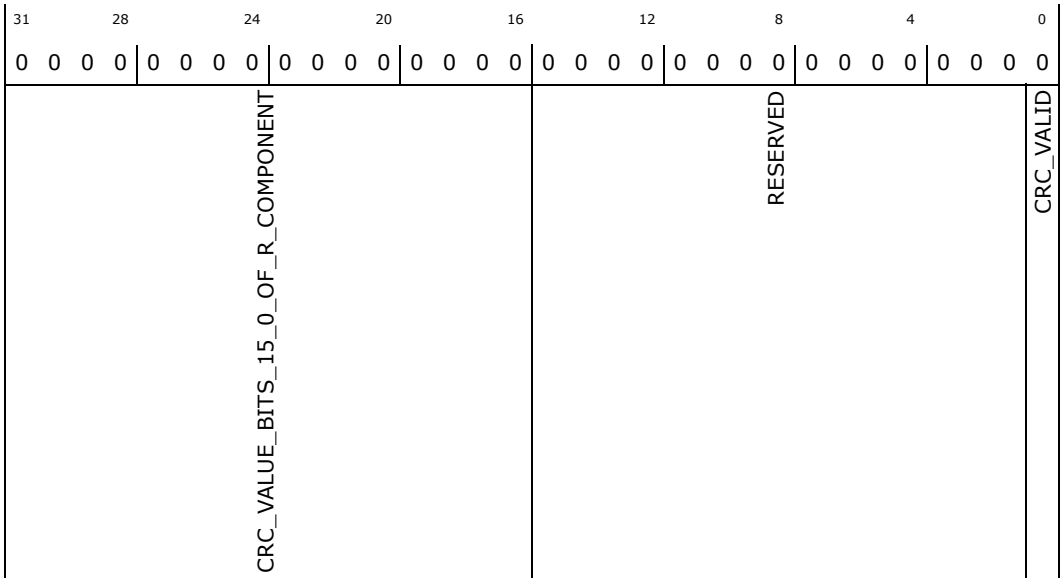
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PSRCRC1B: [GTTMMADR_LSB + 2BF20h] + 61098h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**CRC_VALUE_BITS_15_0_OF_R_COMPONENT:** crc values bits 15 to 0 of Red component
15:1	0b RO	**RESERVED:** Reserved.
0	0b RO	**CRC_VALID:** CRC calculation complete and valid for previous frame.

3.4.14 PSRCRC2B—Offset 6109Ch

Pipe B PSR CRC2 register

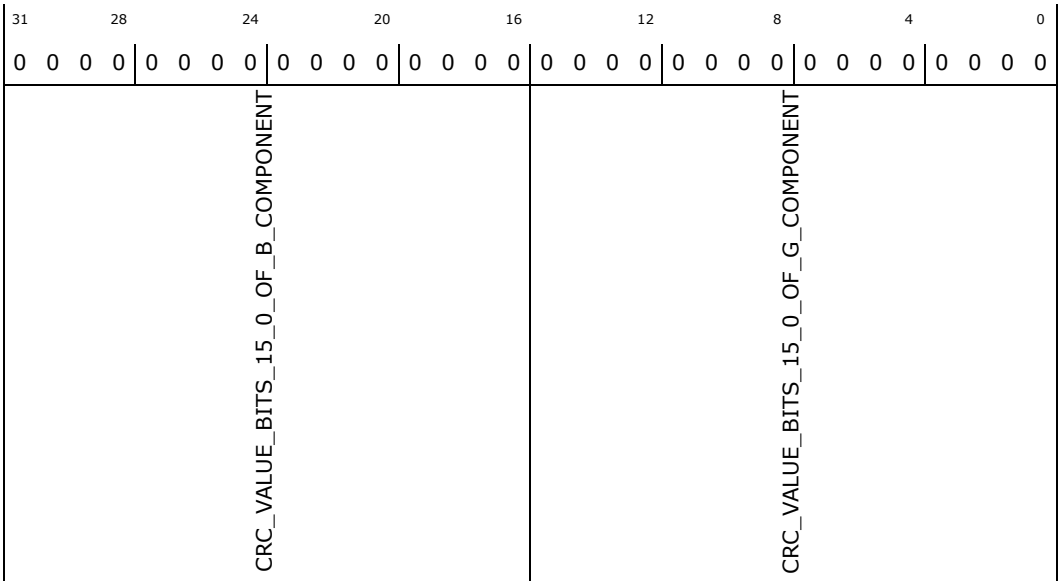
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PSRCRC2B: [GTTMMADR_LSB + 2BF20h] + 6109Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**CRC_VALUE_BITS_15_0_OF_B_COMPONENT:** crc values bits 15 to 0 of blue component
15:0	0b RO	**CRC_VALUE_BITS_15_0_OF_G_COMPONENT:** crc values bits 15 to 0 of green component

3.4.15 VSCSDPB—Offset 610A0h

Pipe B VSC SDP register

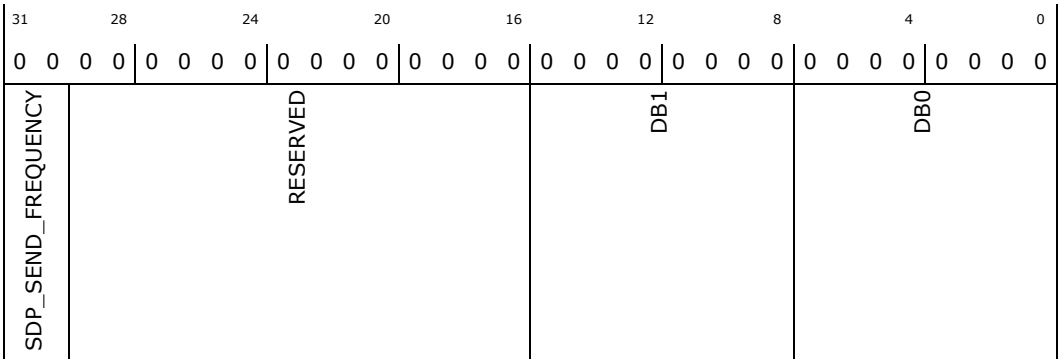
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VSCSDPB: [GTTMMADR_LSB + 2BF20h] + 610A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RW	**SDP_SEND_FREQUENCY:** 00: off, not sending 01: send one every frame 10: send once 11: reserved Programming note: This field shall be programmed either send once or send one every frame when SW driver sets PSR active entry bit. When PSR is enabling this field is ignored. One SDP is sent in every frame until source is in PSR active state
29:16	0b RW	**RESERVED:** Reserved.
15:8	0b RW	**DB1:** Programmed by display driver in manual mode, auto-generate by display controller in all other modes
7:0	0b RW	**DB0:** Bits 7:4: Stereo Interface Method Specific Parameter Bits 3:0: Stereo Interface Method Code. This field is programmed by display driver for stereo display configuration

3.4.16 PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 610B0h

When color correction matrix enable bit is set in PIPEBCONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix like gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Access Method

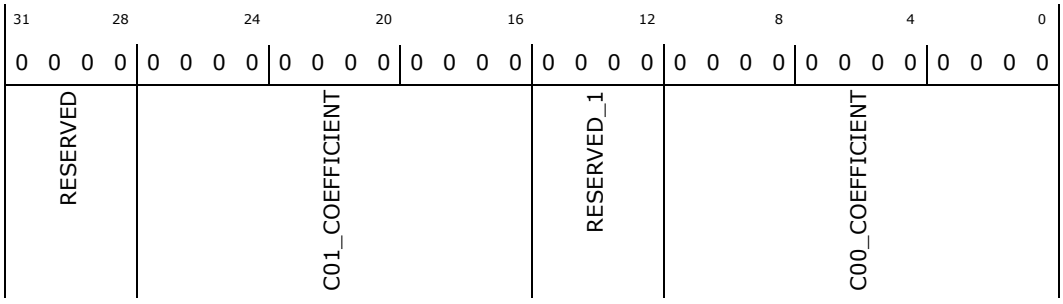
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS: [GTTMMADR_LSB + 2BF20h] + 610B0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
27:16	0b RW	**C01_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.
11:0	0b RW	**C00_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.4.17 PIPEBWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 610B4h

Refer to the description of register PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS.

Access Method

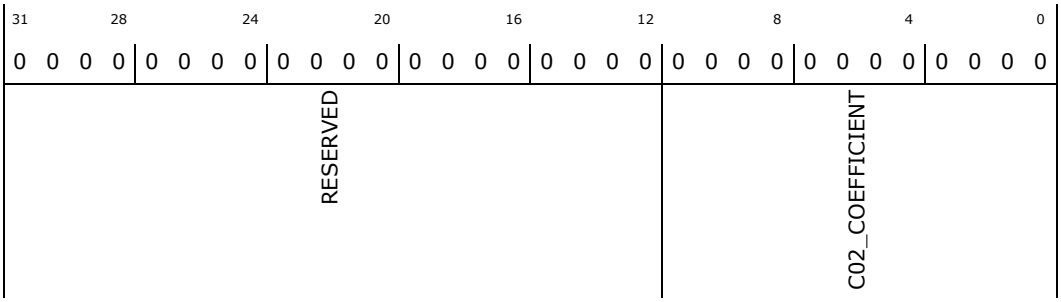
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT: [GTTMMADR_LSB + 2BF20h] + 610B4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C02_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.4.18 PIPEBWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 610B8h

Refer to the description of register PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS.

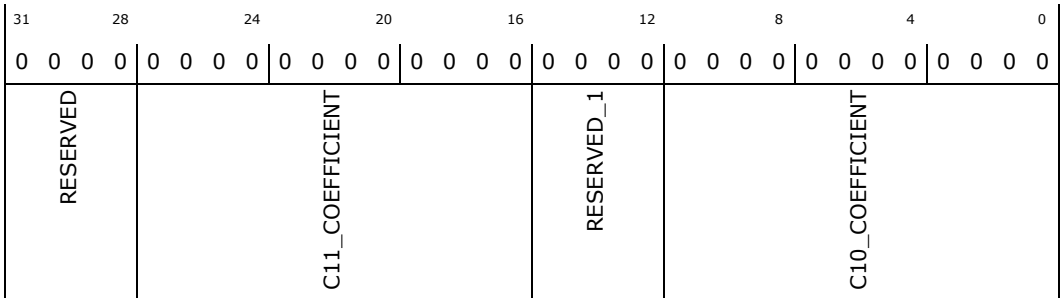
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS: [GTTMMADR_LSB + 2BF20h] + 610B8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Reserved.
27:16	0b RW	**C11_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.
11:0	0b RW	**C10_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.4.19 PIPEBWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 610BCh

Refer to the description of register PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS.

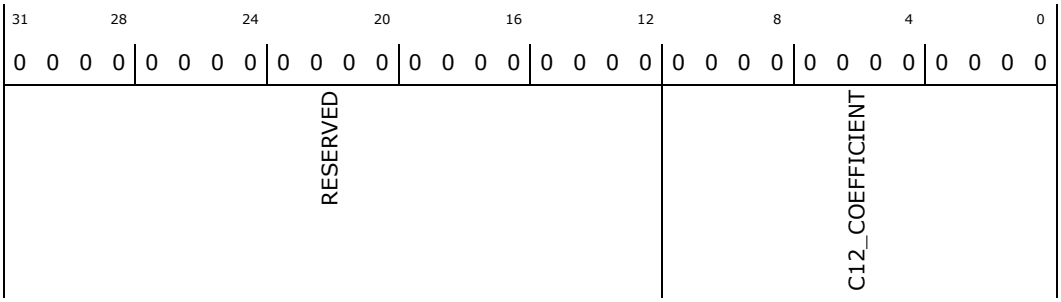
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT: [GTTMMADR_LSB + 2BF20h] + 610BCh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C12_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.4.20 PIPEBWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 610C0h

Refer to the description of register PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS.

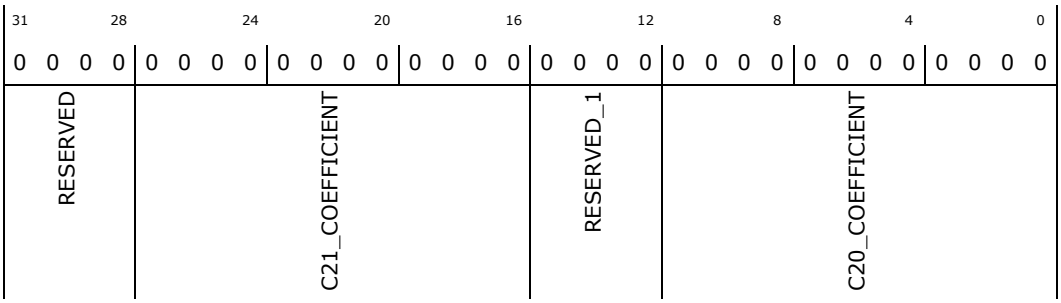
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS: [GTTMMADR_LSB + 2BF20h] + 610C0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Reserved.
27:16	0b RW	**C21_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Bit Range	Default & Access	Description
15:12	0b RW	**RESERVED_1:** Reserved.
11:0	0b RW	**C20_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.4.21 PIPEBWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 610C4h

Refer to the description of register PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS.

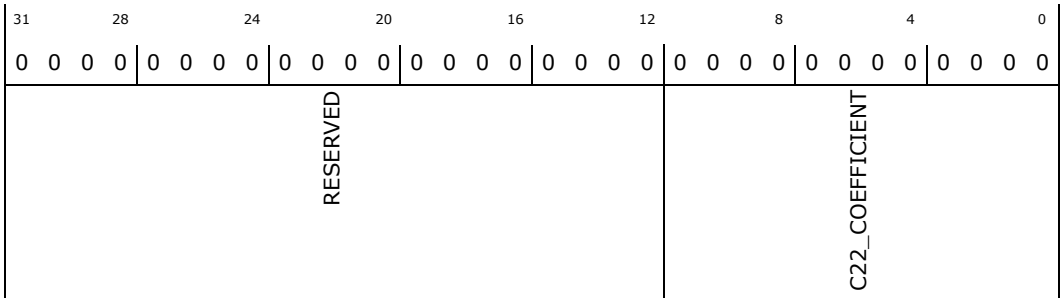
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT: [GTTMMADR_LSB + 2BF20h] + 610C4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C22_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

3.4.22 ADPA—Offset 61100h

Analog Display Port Register CRT port control (dprrega.v adp_Q)

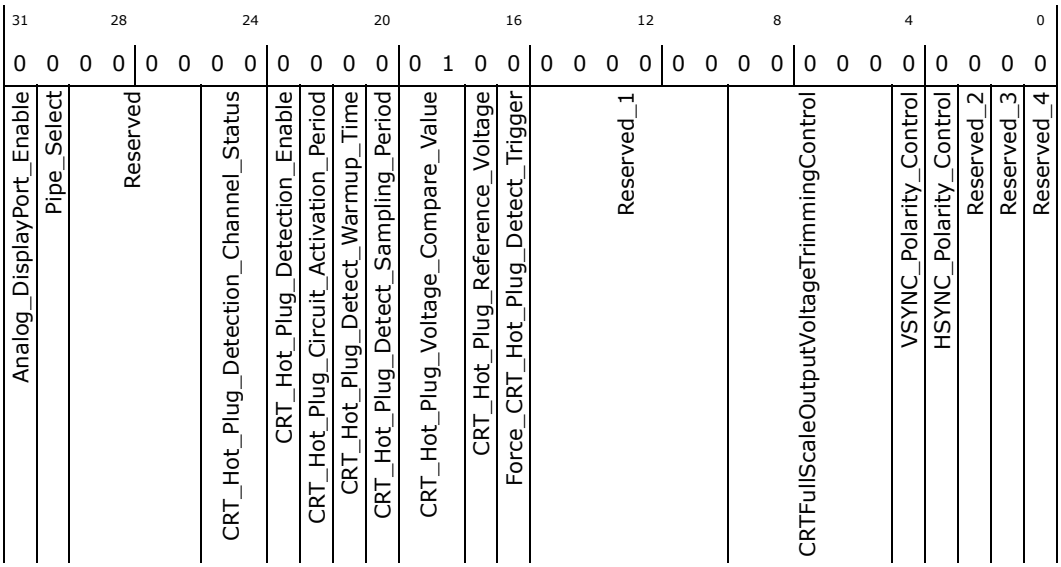
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

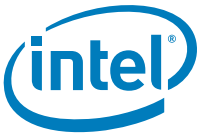
ADPA: [GTTMMADR_LSB + 2BF20h] + 61100h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00040000h



Bit Range	Default & Access	Description
31	0b RW	**Analog_DisplayPort_Enable:** Project: All Default Value: 0b This bit enables or disables the analog port CRT DAC and syncs outputs. Value Name Description Project 0b Disable Disable the analog port DAC and disable output of syncs All 1b Enable Enable the analog port DAC and enable output of syncs All
30	0b RW	**Pipe_Select:** Project: All Default Value: 0b Determines which pipe output will feed this DAC port. Value Name Description Project 0b Pipe A Pipe A All 1b Pipe B Pipe B All
29:26	0b RW	**Reserved:** Project: All Format:
25:24	0b RO	**CRT_Hot_Plug_Detection_Channel_Status:** Project: All AccessType: Read Only Default Value: 00b These bits are set when a CRT hot plug or unplug event has been detected and indicate which color channels were attached. Write a one to these bits to clear the status. The rising or falling edges of these bits are ORed together to go to the main ISR CRT hot plug register bit. Value Name Description Project 00b None No channels attached All 01b Blue Blue channel only is attached All 10b Green Green channel only is attached All 11b Both Both blue and green channel attached All
23	0b RW	**CRT_Hot_Plug_Detection_Enable:** Project: All Default Value: 0b Hot plug detection is used to set status bits or an interrupt on the connection or disconnection of a CRT to the analog display port. Value Name Description Project 0b Disable CRT hot plug detection is disabled All 1b Enable CRT hot plug detection is enabled All
22	0b RW	**CRT_Hot_Plug_Circuit_Activation_Period:** Project: All Default Value: 0b This bit sets the activation period for the CRT hot plug circuit. Value Name Description Project 0b 64 cdclk 64 cdclk periods All 1b 128 cdclk 128 cdclk periods All



Bit Range	Default & Access	Description
21	0b RW	**CRT_Hot_Plug_Detect_Warmup_Time:** Project: All Default Value: 0b This bit sets the warm up time for the CRT hot plug circuit. Value Name Description Project 0b 2M pcdclks 2M pcdclks warm up (approximately 5ms) All 1b 4M pcdclks 4M pcdclks warm up (approximately 10ms) All
20	0b RW	**CRT_Hot_Plug_Detect_Sampling_Period:** Project: All Default Value: 0b This bit determines the length of time between sampling periods when the transcoder is disabled. Value Name Description Project 0b 1G pcdclks 1G pcdclks (approximately 2 seconds) All 1b 2G pcdclks 2G pcdclks (approximately 4 seconds) All
19:18	01b RW	**CRT_Hot_Plug_Voltage_Compare_Value:** Project: All Default Value: 01b A0 Compare value for Vref to determine whether the analog port is connected to a CRT. Value Name Description Project 00b 80 80 All 01b A0 A0 (Default) All 10b C0 C0 All 11b E0 E0 (bit 17 must be = 1) All
17	0b RW	**CRT_Hot_Plug_Reference_Voltage:** Project: All Default Value: 0b Value Name Description Project 0b 325mv 325mv All 1b 475mv 475mv (bits 19:18 must be = 11) All
16	0b RW	**Force_CRT_Hot_Plug_Detect_Trigger:** Project: All Default Value: 0b Triggers a CRT hotplug/unplug detection cycle independent of the hot plug detection enable bit. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in the CRT Hot Plug Detection Status. Software must reset status after a force CRT detect trigger. Value Name Description Project 0b No Trigger No Trigger All 1b Force Trigger Force Trigger All
15:10	0b RW	**Reserved_1:** Project: All Format:
9:5	0b RW	**CRTFullScaleOutputVoltageTrimmingControl:** Project: All Default Value: 0b This controls CRT output voltage trimming to ensure the output voltage is within VESA spec.
4	0b RW	**VSYNC_Polarity_Control:** Project: All Default Value: 0b The output VSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal. Value Name Description Project 0b Low Active Low All 1b High Active High All
3	0b RW	**HSYNC_Polarity_Control:** Project: All Default Value: 0b The output HSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the HSYNC signal. Value Name Description Project 0b Low Active Low All 1b High Active High All
2	0b RW	**Reserved_2:** Project: All Forma
1	0b RW	**Reserved_3:** Project: All Forma Monochrome Enable: [DevVLVP] If the CRT display is a monochrome type, SW driver shall set this bit to enable the CRT circuit to drive only the green channel to CRT and gate off the red and blue channels. 0 = Monochrome disabled (default) 1 = Monochrome enabled

Bit Range	Default & Access	Description
0	0b RW	**Reserved_4:** Project: All Forma Monochrome Enable: [DevVLVP] If the CRT display is a monochrome type, SW driver shall set this bit to enable the CRT circuit to drive only the green channel to CRT and gate off the red and blue channels. 0 = Monochrome disabled (default) 1 = Monochrome enabled 0 = 1.35V is used for analog supply voltage (default) 1 = 1.25V is used for analog supply voltage

3.4.23 CRTIO_DFX—Offset 61104h

CRT port control (dprrega.v crt_dfx)

Access Method

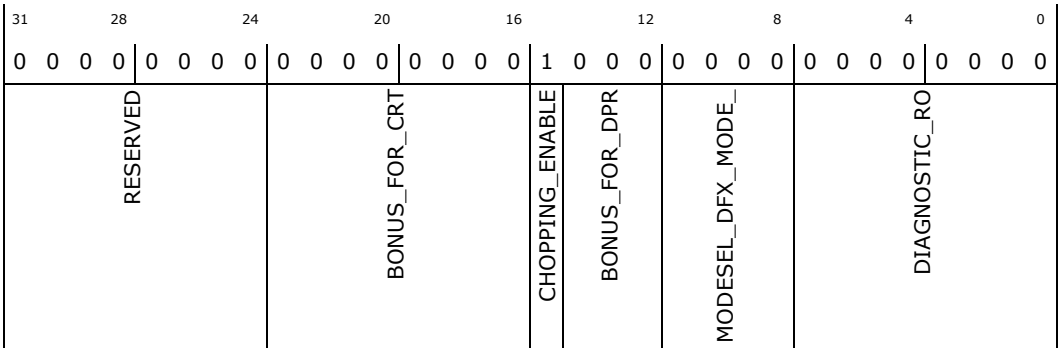
Type: Memory Mapped I/O Register (Size: 32 bits)

CRTIO_DFX: [GTTMMADR_LSB + 2BF20h] + 61104h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00008000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** read as zero
23:16	0b RW	**BONUS_FOR_CRT:** bonus for CRT port control
15	1b RW	**CHOPPING_ENABLE:** Chopping enable (for BG circuit)
14:12	0b RW	**BONUS_FOR_DPR:** bonus for DPR crt port control
11:8	0b RW	**MODESEL_DFX_MODE_:** ModeSel (DFx mode)
7:0	0b RO	**DIAGNOSTIC_RO:** Observe signals at CRTIO AccessType: Read Only

3.4.24 PORT_HOTPLUG_EN—Offset 61110h

DPD enable control (dprrega.v ql_hotplugen_Q)

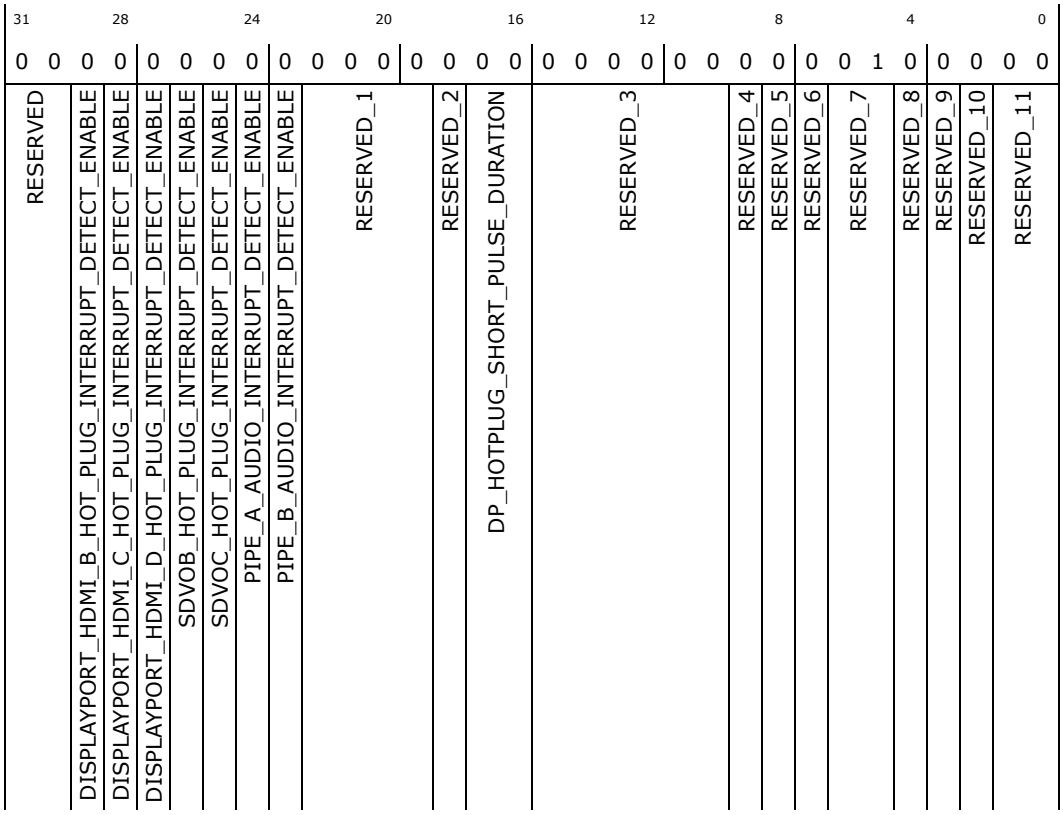
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

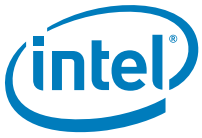
PORT_HOTPLUG_EN: [GTTMMADR_LSB + 2BF20h] + 61110h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

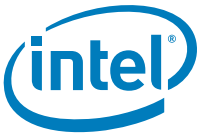
Default: 00000020h



Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** mbz
29	0b RW	**DISPLAYPORT_HDMI_B_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCDV, DevCTG, DevELK] This will enable the consideration of the hot plug interrupt status bit for DisplayPort B in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMIB Hot Plug Detect Disabled (Default) 1 = DisplayPort or HDMIB Hot Plug Detect Enabled



Bit Range	Default & Access	Description
28	0b RW	**DISPLAYPORT_HDMI_C_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCDV, DevCTG, DevELK] This will enable the consideration of the hot plug interrupt status bit for DisplayPort C in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMIC Hot Plug Detect Disabled (Default) 1 = DisplayPort or HDMIC Hot Plug Detect Enabled
27	0b RW	**DISPLAYPORT_HDMI_D_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCTG] This will enable the consideration of the hot plug interrupt status bit for DisplayPort D in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMID Hot Plug Detect Disabled (Default) 1 = DisplayPort or HDMID Hot Plug Detect Enabled
26	0b RW	**SDVOB_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCTG] This will enable the consideration of the hot plug interrupt status bit in the Port Hotplug Status register, offset 61114h. This bit enables detection on the SDVOB interrupt input pin pair. 0 = SDVOB Hot Plug Detect Disabled (Default) 1 = SDVOB Hot Plug Detect Enabled
25	0b RW	**SDVOC_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCTG] This will enable the consideration of the hot plug interrupt status bit in the Port Hotplug Status register, offset 61114h. This bit enables detection on the SDVOC interrupt input pin pair. 0 = SDVOC Hot Plug Detect Disabled (Default) 1 = SDVOC Hot Plug Detect Enabled
24	0b RW	**PIPE_A_AUDIO_INTERRUPT_DETECT_ENABLE:** [DevCDV, DevCL, DevCTG, DevVLVP] This bit enables consideration of the pipe A audio interrupt status bit in the Port Hotplug Status Register, offset 61114h. It relates to the HDMI port that has audio enabled and can only be used in combination with TMDS encoding. This bit is only to be used for integrated HDMI. 0 = Audio interrupt detect disabled (Default) 1 = Audio interrupt detect enabled
23	0b RW	**PIPE_B_AUDIO_INTERRUPT_DETECT_ENABLE:** [DevVLVP] This bit enables consideration of the pipe B audio interrupt status bit in the Port Hotplug Status Register, offset 61114h. It relates to the HDMI port that has audio enabled and can only be used in combination with TMDS encoding. This bit is only to be used for integrated HDMI. 0 = Audio interrupt detect disabled (Default) 1 = Audio interrupt detect enabled
22:19	0b RW	**RESERVED_1:** mbz
18	0b RW	**RESERVED_2:** [DevVLVP] MBZ TV Hot Plug Detect Interrupt Enable: [DevCL, DevCTG] This will enable the consideration of the TV hot plug interrupt status bit. 0 = TV Hot Plug Detect Disabled (bit 10 of the port hotplug status register no longer detects interrupts, Default) 1 = TV Hot Plug Detect Enabled
17:16	0b RW	**DP_HOTPLUG_SHORT_PULSE_DURATION:** [DevCDV, DevCTG, DevELK] These bits define the duration of the pulse defined as a short pulse for DisplayPort ports. Pulse less than this value is detected short pulse. Pulse larger than this value is detected long pulse. For DP, this shall use 2ms as threshold. 00 = 2mS (Default) 01 = 4.5mS 10 = 6mS 11 = 100mS



Bit Range	Default & Access	Description
15:10	0b RW	**RESERVED_3:** mbz
9	0b RW	**RESERVED_4:** [DevVLVP] MBZ. This bit is the same as bit 23 in 61100h [DevCDV, DevCTG, DevBW, DevCL, DevBLC] CRT Hot plug Interrupt Enable: Hotplug detection is used to cause an interrupt or status bit based on the connection or disconnection of a CRT to the analog video connection. 0 = No hot plug interrupt is enabled (Default) 1 = Hot plug detection is enabled
8	0b RW	**RESERVED_5:** [DevVLVP] MBZ. This bit is the same as bit 22 in 61100h [DevCDV, DevCTG] CRT Hot plug Circuit Activation Period: This bit sets the activation period for the CRT hot plug circuit detection. Setting this bit to 1 is required for the correct operation of CRT DAC detection. 0 = 32 cdclk periods (Default) 1 = 64 cdclk periods
7	0b RW	**RESERVED_6:** [DevVLVP] MBZ. This bit is the same as bit 21 in 61100h [DevCDV, DevCTG, DevBW, DevCL, DevBLC] CRT DAC on time Value: Powerup time for 0 = CRT DAC requires 2M cdclks for warm up (Default) 1 = CRT DAC requires 4M cdclks for warm up
6:5	01b RW	**RESERVED_7:** [DevVLVP] MBZ. This bit is the same as bit 19:18 in 61100h [DevCDV, DevCTG, DevBW, DevCL, DevBLC] CRT Hot plug Voltage Compare Value: Compare value for CRT hotplug detect Vref to determine whether the analog port is connected to a CRT. The voltage is forced at the beginning of the active region of the screen every 2 seconds. 00 = A0, 01 = B0, (Default) 10 = C0 11 = D0
4	0b RW	**RESERVED_8:** [DevVLVP] MBZ. This bit is the same as bit 20 in 61100h [DevCDV, DevCTG, DevBW, DevCL, DevBLC] CRT Hot Plug Detect Delay: This bit determines the length of time between polling periods when the DAC/pipe are disabled 0 = 1G cdclks (default) 1 = 2G cdclks
3	0b RW	**RESERVED_9:** [DevVLVP] MBZ [DevCDV, DevCTG, DevBW, DevCL, DevBLC] Force CRT detect trigger: Triggers a CRT hotplug/unplug detection cycle independent of the interrupt enable bit. Bits 5:8 of this register must be correctly programmed when forcing a trigger. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in bits 9:8 of the port hotplug interrupt status register. The CRT interrupt status bit #11 in the hot plug status register (61114) will get set the first time Force CRC detect trigger is used after reset. Software must reset status after a force CRT detect trigger. 0 = No trigger (Default) 1 = Trigger
2	0b RW	**RESERVED_10:** [DevVLVP] MBZ. This bit is the same as bit 17 in 61100h [DevCTG-B] CRT DAC hot plug detection reference voltage selection: 0 = 325mv, bits[6:5] should be set to 01 (Default) 1 = 475mv, bits[6:5] should be set to 11
1:0	0b RW	**RESERVED_11:** mbz

3.4.25 PORT_HOTPLUG_STAT—Offset 61114h

CRT port control (dprrega.v porthotst_aR)

Access Method

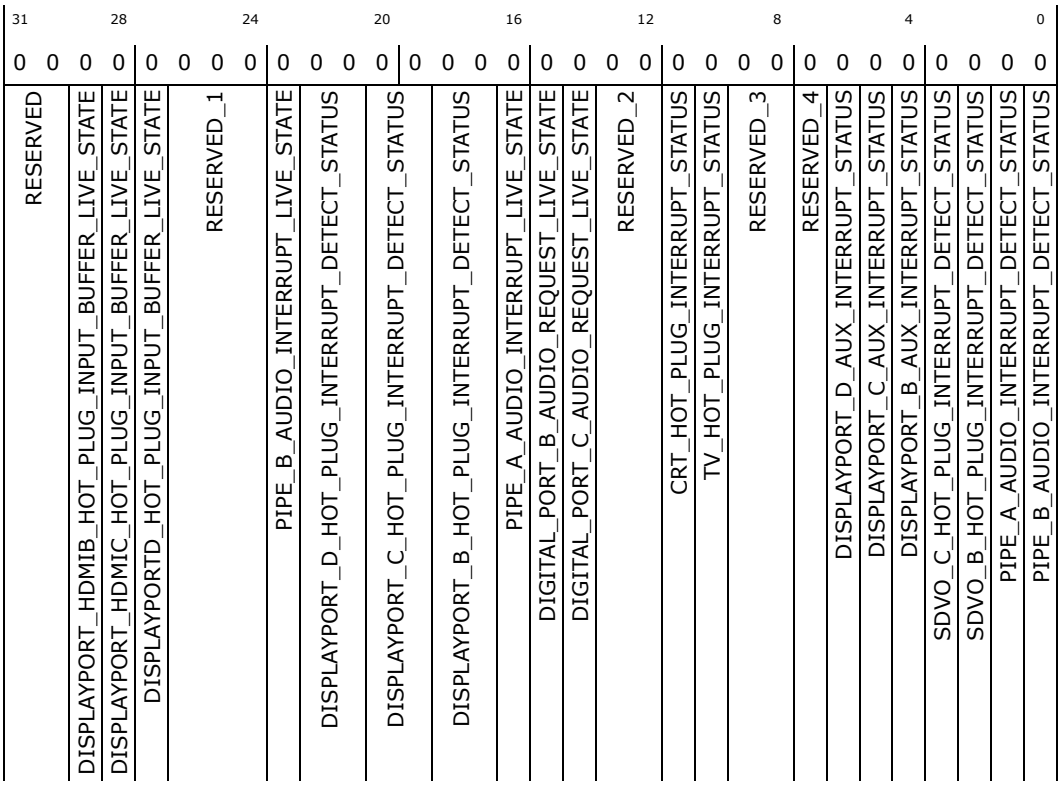
Type: Memory Mapped I/O Register (Size: 32 bits)

PORT_HOTPLUG_STAT: [GTTMMADR_LSB + 2BF20h] + 61114h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

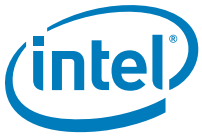
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** mbz
29	0b RO	**DISPLAYPORT_HDMIB_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** [DevCDV, DevCTG, DevELK] This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPort or HDMI B when bit 29 of the hotplug enable register, offset 61110h is set. This pin signal is active high. This does not feed into the first line interrupt status register. This bit should be read to confirm cable connection prior to attempting EDID read. 1 = HPD detected active 0 = HPD detected inactive AccessType: Read Only
28	0b RO	**DISPLAYPORT_HDMIC_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** [DevCDV, DevCTG, DevELK] This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPortC when bit of this register is set. This pin signal is active high. This does not feed into the first line interrupt status register. This bit should be read to confirm cable connection prior to attempting EDID read. 1 = HPD detected high 0 = HPD detected low AccessType: Read Only

Bit Range	Default & Access	Description
27	0b RO	**DISPLAYPORTD_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** [DevCTG] This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPortD when bit of this register is set. This pin signal is active high. This does not feed into the first line interrupt status register. Please note that port D is intended for LFP use and therefore HPD may not be present. Bit 2 of the DPD control register must therefore be read to determine whether DPD is used in the system. 1 = HPD detected high 0 = HPD detected low AccessType: Read Only
26:24	0b RW	**RESERVED_1:** mbz
23	0b RO	**PIPE_B_AUDIO_INTERRUPT_LIVE_STATE:** [DevVLVP] This read-only bit is used only in ports that use TMDS encoding. It reflects the state of the pipe B audio interrupt request for HDCP when bit 1 of this register is set. This pin signal is active high. It does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
22:21	0b RW/1C	**DISPLAYPORT_D_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCTG] This reflects hot plug interrupt status on DisplayPort D. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 27 of the hotplug enable status register is set. 00 = DisplayPort D Hot Plug event not detected 1x = DisplayPort D long pulse Hot Plug event detected X1 = DisplayPort D short pulse Hot Plug event detected AccessType: One to Clear
20:19	0b RW/1C	**DISPLAYPORT_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCDV, DevCTG, DevELK] This reflects hot plug interrupt status on DisplayPort or HDMI C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 28 of the hotplug enable status register is set. Please note that these bits should be considered in conjunction with bit 28, the hot plug input buffer live state, when determining further action: if bit 28 = 0, the bits should be cleared and the port must be disabled. 00 = DisplayPort/HDMI C Hot Plug event not detected 1x = DisplayPort/HDMI C long pulse Hot Plug event detected X1 = DisplayPort C short pulse Hot Plug event detected AccessType: One to Clear
18:17	0b RW/1C	**DISPLAYPORT_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCDV, DevCTG, DevELK] This reflects hot plug interrupt status on DisplayPort B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 29 of the hotplug enable status register is set. Please note that these bits should be considered in conjunction with bit 29, the hot plug input buffer live state, when determining further action: if bit 29 = 0, the bits should be cleared and the port must be disabled. 00 = DisplayPort/HDMI B Hot Plug event not detected 1x = DisplayPort/HDMI B long pulse Hot Plug event detected X1 = DisplayPort B short pulse Hot Plug event detected AccessType: One to Clear



Bit Range	Default & Access	Description
16	0b RO	**PIPE_A_AUDIO_INTERRUPT_LIVE_STATE:** [DevCDV, DevCTG, DevCL] This read-only bit is used only in ports that use TMDS encoding. It reflects the state of the pipe A audio interrupt request for HDCP when bit 1 of this register is set. This pin signal is active high. It does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
15	0b RO	**DIGITAL_PORT_B_AUDIO_REQUEST_LIVE_STATE:** [DevCDV, DevCTG, DevCL] This read-only bit is only used on ports using audio. It reflects the state of audio HDCP request when bit 17 of this register is set if audio is enabled on this port. This pin signal is active high. This does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
14	0b RO	**DIGITAL_PORT_C_AUDIO_REQUEST_LIVE_STATE:** [DevCDV, DevCTG, DevCL] This read-only bit is only used on ports using audio. It reflects the state of audio HDCP request when bit 19 of this register is set if audio is enabled on this port. This pin signal is active high. This does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
13:12	0b RW	**RESERVED_2:** mbz
11	0b RW/1C	**CRT_HOT_PLUG_INTERRUPT_STATUS:** [DevCDV, DevCTG, DevBW, DevCL, DevBLC] This bit is set when a CRT hot plug or unplug event has been detected. A hot plug or unplug event is defined as the change in connection state of the CRT as determined by the hardware CRT detect sequence which is enabled through bit #9 (CRT hot plug interrupt enable) or bit #3 (Force CRT detect trigger) in the Port_HotPlug_En register 0x61110. After reset, the CRT is considered unconnected even if physically connected until the first detect sequence occurs. Physically plugging or unplugging the CRT device will also be detected as a change of connection state. Writing a 1 to this bit clears it. 0 =CRT Interrupt has not occurred 1 = CRT Interrupt has occurred AccessType: One to Clear
10	0b RW/1C	**TV_HOT_PLUG_INTERRUPT_STATUS:** [DevCTG, DevBW, DevCL, DevBLC] This bit is set when a TV hot plug or unplug event has been detected. Reflects the state of bit 31 of the TV DAC state register, offset 68004-68007h. Software must write a one to these bits to clear the status. 0 =TV Interrupt has not occurred 1 = TV Interrupt has occurred AccessType: One to Clear
9:8	0b RW/1C	**RESERVED_3:** [DevVLVP] MBZ. These info are recorded in 61100h ADPA register[25:24] [DevCDV, DevCTG, DevBW, DevCL, DevBLC] CRT Hot Plug Detection Status (read only): These bits are set when a CRT hot plug or unplug event has been detected. 00 = No channels attached (default) 01 = Blue channel only is attached 10 = Green channel only is attached 11 = Both blue and green channel attached AccessType: One to Clear
7	0b RW	**RESERVED_4:** mbz
6	0b RW/1C	**DISPLAYPORT_D_AUX_INTERRUPT_STATUS:** [DevCTG] This bit is set when a transaction on AUX channel D has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel D control register is set. Writing a 1 to this bit clears it. 0 = AUX channel D Interrupt has not occurred 1 = AUX channel D Interrupt has occurred AccessType: One to Clear

Bit Range	Default & Access	Description
5	0b RW/1C	**DISPLAYPORT_C_AUX_INTERRUPT_STATUS:** [DevCTG, DevCDV] This bit is set when a transaction on AUX channel C has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel C control register is set. Writing a 1 to this bit clears it. 0 = AUX channel C Interrupt has not occurred 1 = AUX channel C Interrupt has occurred AccessType: One to Clear
4	0b RW/1C	**DISPLAYPORT_B_AUX_INTERRUPT_STATUS:** [DevCTG, DevCDV] This bit is set when a transaction on AUX channel B has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel B control register is set. Writing a 1 to this bit clears it. 0 = AUX channel B Interrupt has not occurred 1 = AUX channel B Interrupt has occurred AccessType: One to Clear
3	0b RW/1C	**SDVO_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCTG, DevCDV] This reflects hot plug interrupt status on SDVO port C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of an HDCP state change request from the audio driver over SDVO only. This bit feeds into the first line interrupt status register when bit 25 of the hotplug enable status register is set. 0 = SDVO Hot Plug event not detected 1 = SDVO Hot Plug event detected AccessType: One to Clear
2	0b RW/1C	**SDVO_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCTG, DevCDV] This reflects hot plug interrupt status on SDVO port B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of an HDCP state change request from the audio driver over SDVO only. This bit feeds into the first line interrupt status register when bit 26 of the hotplug enable status register is set. 0 = SDVO Hot Plug event not detected 1 = SDVO Hot Plug event detected AccessType: One to Clear
1	0b RW/1C	**PIPE_A_AUDIO_INTERRUPT_DETECT_STATUS:** [DevCTG, DevCDV, DevCL] This reflects a request for integrated HDCP state change set by audio driver and propagated through the audio hardware. The graphics software must write a one to this bit to clear the status. Upon clearing this bit, the audio ready bit is cleared in the audio registers. The graphics software then must reset audio ready bit 14 in the audio control register, offset 620B4h to 1 when the HDCP interrupt has been serviced. This bit feeds into the first line interrupt status register when bit 24 of the hotplug enable status register is set 0 = Audio interrupt event not detected 1 = Audio interrupt event detected AccessType: One to Clear
0	0b RW/1C	**PIPE_B_AUDIO_INTERRUPT_DETECT_STATUS:** [DevCTG, DevCDV, DevCL] This reflects a request for integrated HDCP state change set by audio driver and propagated through the audio hardware. The graphics software must write a one to this bit to clear the status. Upon clearing this bit, the audio ready bit is cleared in the audio registers. The graphics software then must reset audio ready bit 14 in the audio control register, offset 620B4h to 1 when the HDCP interrupt has been serviced. This bit feeds into the first line interrupt status register when bit 23 of the hotplug enable status register is set 0 = Audio interrupt event not detected 1 = Audio interrupt event detected AccessType: One to Clear

3.4.26 SDVOHDMIB—Offset 61140h

Digital Display Port B Control Register HDMIB port control (dprrega.v sdvo_bQ)

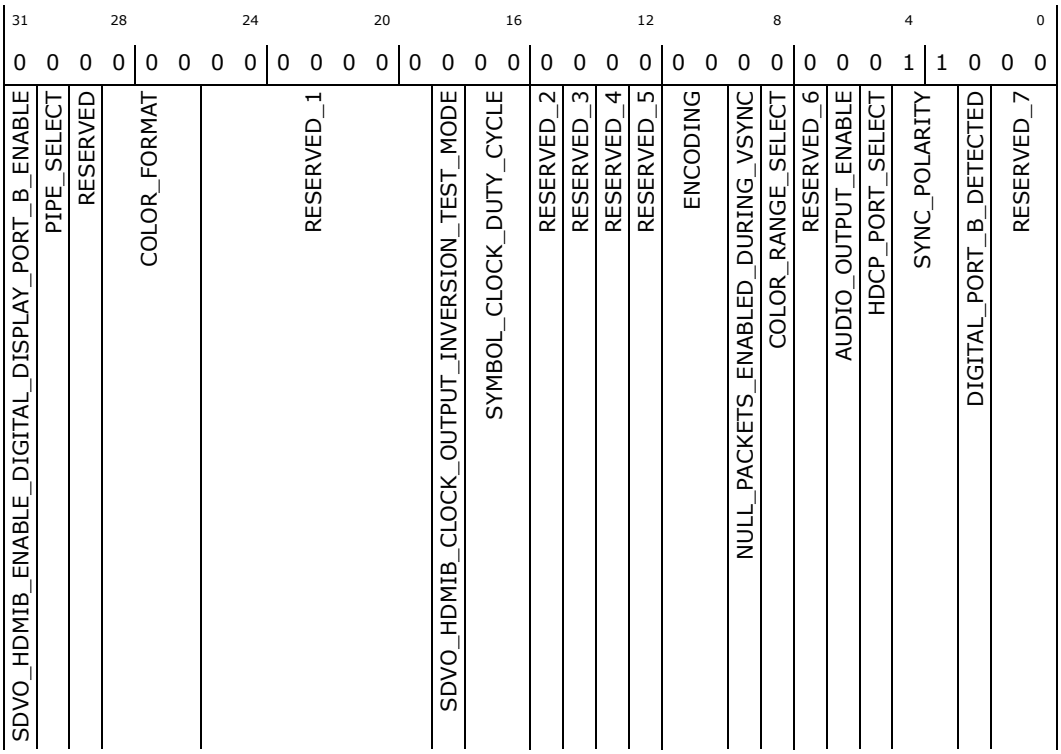
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

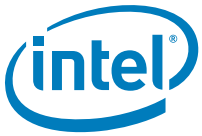
SDVOHDMIB: [GTTMMADR_LSB + 2BF20h] + 61140h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000018h



Bit Range	Default & Access	Description
31	0b RW	**SDVO_HDMIB_ENABLE_DIGITAL_DISPLAY_PORT_B_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. This port must not be enabled simultaneously with DisplayPort B. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to 0 after disabling the port. This is workaround for hardware issue where the transcoder select set to 1 will prevent DisplayPortB from being enabled on transcoder A. [DevIBX] Software must write this bit twice when enabling the port (setting to 1) as a workaround for hardware issue that may result in first write getting masked. [DevIBX] Toggle this bit off then on at the end of mode set sequence when enabling HDMI 12-bit per color with pixel repeat 1 = Enable. This bit enables the Digital Display Port B interface for HDMI or SDVO modes. 0 = Disable and tristates the Digital Display Port B interface for HDMI or SDVO modes.
30	0b RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29	0b RW	**RESERVED:** [DevCDV]: [DevCTG, DevBW, DevCL, DevBLC] Stall Select: This bit selects stall for external scaling functionality only on SDVO. Programming notes: It is only valid to have a single stall indication to a particular pipe. In cases where two ports are being driven from a single pipe, one of the ports must set this bit to 0. Only sDVOB or sDVOC can select the stall function, as only a single stall input is available between the two interfaces. Set the stall input to unused before programming the external device creating the stall. 0 = Stall input signal is unused on this port 1 = Stall input signal is used to stall the pipe attached to this port
28:26	0b RW	**COLOR_FORMAT:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 = 8 bits per color (Default, x3 mode) 001 = RESERVED for 10 bits per color 010 = RESERVED for 6 bits per color 011 = RESERVED 1xx = RESERVED
25:19	0b RW	**RESERVED_1:** Reserved.
18	0b RW	**SDVO_HDMIB_CLOCK_OUTPUT_INVERSION_TEST_MODE:** Please note that this applies to all modes and is instantly updated. 1 = sDVO/HDMIB Clock output is inverted 0 = sDVO/HDMIB Clock output is NOT inverted (DEFAULT)
17:16	0b RW	**SYMBOL_CLOCK_DUTY_CYCLE:** [DevCDV, DevCTG, DevCL] These bits control the output clock duty cycle to enable EMI mitigation on the external UDI link. 10/90 cycle has been measured to have ~13dB EMI improvement over a 50/50 duty cycle. 00 = (Default) 50/50 duty cycle: Clock output is 0000011111 01 = 10/90 duty cycle: Clock output is 0111111111 followed by 0000000001 10 = 20/80 duty cycle: Clock output is 0011111111 followed by 0000000011 11 = Reserved



Bit Range	Default & Access	Description
15	0b RW	**RESERVED_2:** [DevCDV, DevVLVP]: [DevBW, DevCL, DevBLC] Port Lane Reversal: This bit reverses the order of the 4 lanes within the port. Port lane reversal takes place on the Vblank after being written. It is an OEM configurable feature. 0 = (Default) Not reversed 1 = Reversed
14	0b RW	**RESERVED_3:** Reserved.
13	0b RW	**RESERVED_4:** [DevCDV, DevVLVP]: [DevBW, DevCL, DevBLC] Clock Output Disable: This bit disables the clock output on the digital output port. For 8b/10b modes the clock output should be disabled. 0 = (Default) Clock output enabled 1 = Clock output disabled
12	0b RW	**RESERVED_5:** [DevCDV, DevVLVP]: [DevBW, DevCL, DevBLC, DevCDV] Scrambling enable: This bit enables scrambling for UDI-related modes using ANSI 8b/10b or TMDS encoding. It is not used with SDVO encoding. Software must set this bit appropriately when enabling the port. Scrambling is reset at the beginning of horizontal sync. 0 = Scrambling disabled (Default) 1 = Scrambling enabled
11:10	0b RW	**ENCODING:** [DevCDV, DevCTG, DevCL] These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b/10b and TMDS encoding must be programmed using these bits. Please note that ANSI 8b/10b and TMDS encoding can only be enabled on one port at a time, as only one HPD pin is available for use between ports B and C. 00 = Reserved 01 = Reserved 10 = TMDS encoding ([DevCL, DevCTG, DevCDV, DevVLVP] external link and HDMI only) See the HDMI specification for control codes. In this mode, the external HPD pin is used to generate hotplug. In fixed frequency mode, start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 = Reserved
9	0b RW	**NULL_PACKETS_ENABLED_DURING_VSYNC:** This bit enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 = Disable null infoframe packets when Vsync=1 on this port. (Default) 1 = Enable null infoframe packets when Vsync=1 on this port.
8	0b RW	**COLOR_RANGE_SELECT:** [DevCDV, DevCTG, DevCL] This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output
7	0b RW	**RESERVED_6:** [DevCDV]: [DevCTG, DevBW, DevCL, DevBLC] sDVOB Border Enable: This bit determines if the border data from native VGA or the timing generator is to be considered valid pixel data at the external component. 1 = Border to the sDVOB encoder is enabled. Blank# is used to generate the DE output (used in all cases except when the external scaler is used in a DVI panel, over SDVO) . 0 = Border to the sDVOB encoder is disabled. DE (Display Enable) is used
6	0b RW	**AUDIO_OUTPUT_ENABLE:** [DevCDV, DevCTG, DevCL] This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. 0 = (Default) No audio output on this port 1 = Enable audio on this port

Bit Range	Default & Access	Description
5	0b RW	**HDCP_PORT_SELECT:** [DevCDV, DevCTG, DevCL] This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port
4:3	11b RW	**SYNC_POLARITY:** Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK. For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS BLANK+VS BLANK+VS+HS. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0b RO	**DIGITAL_PORT_B_DETECTED:** Read-only bit indicating whether a digital port B was detected during initialization. It signifies the level of the GMBUS port 4 (sDVO B/C) data line at boot. This bit is valid regardless of whether the port is enabled. 0 = Digital Port B not detected during initialization 1 = Digital Port B detected during initialization AccessType: Read Only
1:0	0b RW	**RESERVED_7:** MBZ

3.4.27 SDVO—Offset 61154h

DP2 - Digital Port DFT Register ;

Access Method

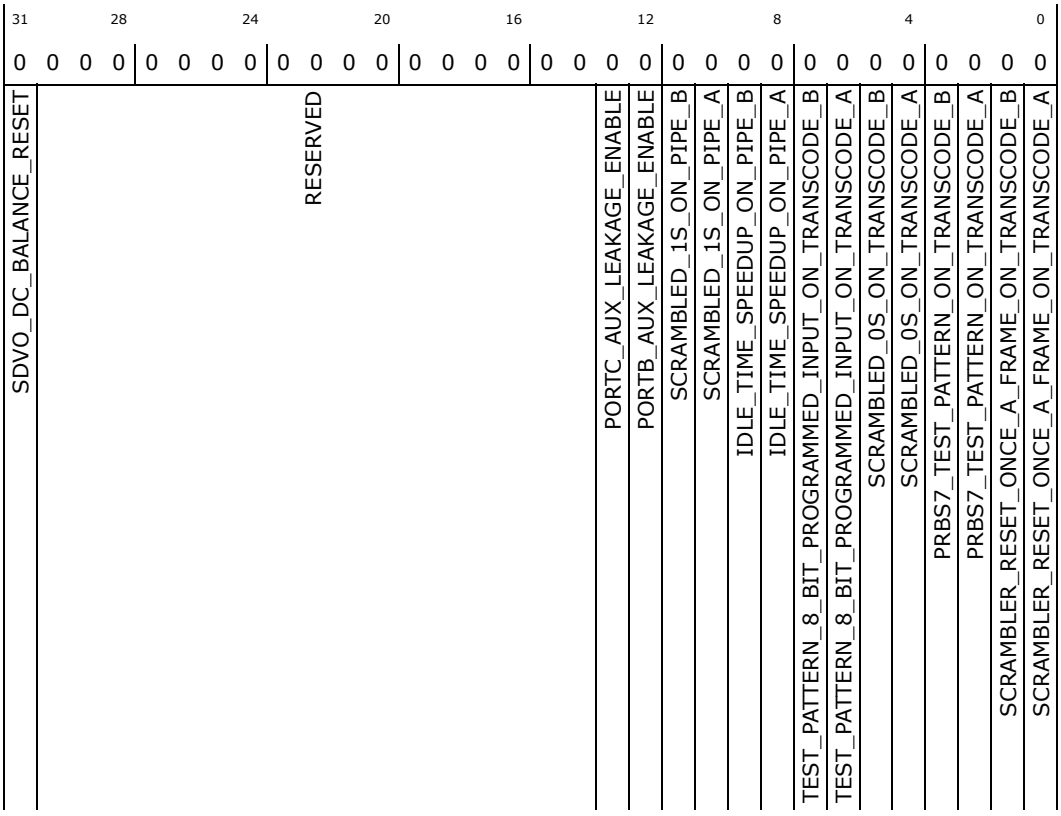
Type: Memory Mapped I/O Register (Size: 32 bits)

SDVO: [GTTMMADR_LSB + 2BF20h] + 61154h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**SDVO_DC_BALANCE_RESET:** Project: All Format: Value Name Description Project 0b Not Reset DC Balance circuitry will not be reset on every frame All 1b Reset DC Balance circuitry will be reset on every frame All
30:14	0b RW	**RESERVED:** Project: All Format: MBZ
13	0b RW	**PORTC_AUX_LEAKAGE_ENABLE:** Project: All Format:
12	0b RW	**PORTB_AUX_LEAKAGE_ENABLE:** Project: All Format:
11	0b RW	**SCRAMBLED_1S_ON_PIPE_B:** Project: All Format: Value Name Description Project 0b Disable Disable scrambled 1s All 1b Enable Enable scrambled 1s All
10	0b RW	**SCRAMBLED_1S_ON_PIPE_A:** Project: All Format: Value Name Description Project 0b Disable Disable scrambled 1s All 1b Enable Enable scrambled 1s All
9	0b RW	**IDLE_TIME_SPEEDUP_ON_PIPE_B:** Project: All Format: Value Name Description Project 0b Normal Normal idle time All 1b Speedup Speedup idle time All

Bit Range	Default & Access	Description
8	0b RW	**IDLE_TIME_SPEEDUP_ON_PIPE_A:** Project: All Format: Value Name Description Project 0b Normal Normal idle time All 1b Speedup Speedup idle time All
7	0b RW	**TEST_PATTERN_8_BIT_PROGRAMMED_INPUT_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
6	0b RW	**TEST_PATTERN_8_BIT_PROGRAMMED_INPUT_ON_TRANSCODE_A:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
5	0b RW	**SCRAMBLED_0S_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the scramble 0s All 1b Enable Enable the scramble 0s All
4	0b RW	**SCRAMBLED_0S_ON_TRANSCODE_A:** Project: All Format: Value Name Description Project 0b Disable Disable the scramble 0s All 1b Enable Enable the scramble 0s All
3	0b RW	**PRBS7_TEST_PATTERN_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
2	0b RW	**PRBS7_TEST_PATTERN_ON_TRANSCODE_A:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
1	0b RW	**SCRAMBLER_RESET_ONCE_A_FRAME_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the scrambler reset once a frame All 1b Enable Enable the scrambler reset once a frame All
0	0b RW	**SCRAMBLER_RESET_ONCE_A_FRAME_ON_TRANSCODE_A:** All Format: Value Name Description Project 0b Disable Disable the scrambler reset once a frame All 1b Enable Enable the scrambler reset once a frame All

3.4.28 HDMIC—Offset 61160h

Digital Display Port C Register HDMIC port control (dprrega.v sdvo_cQ)

Access Method

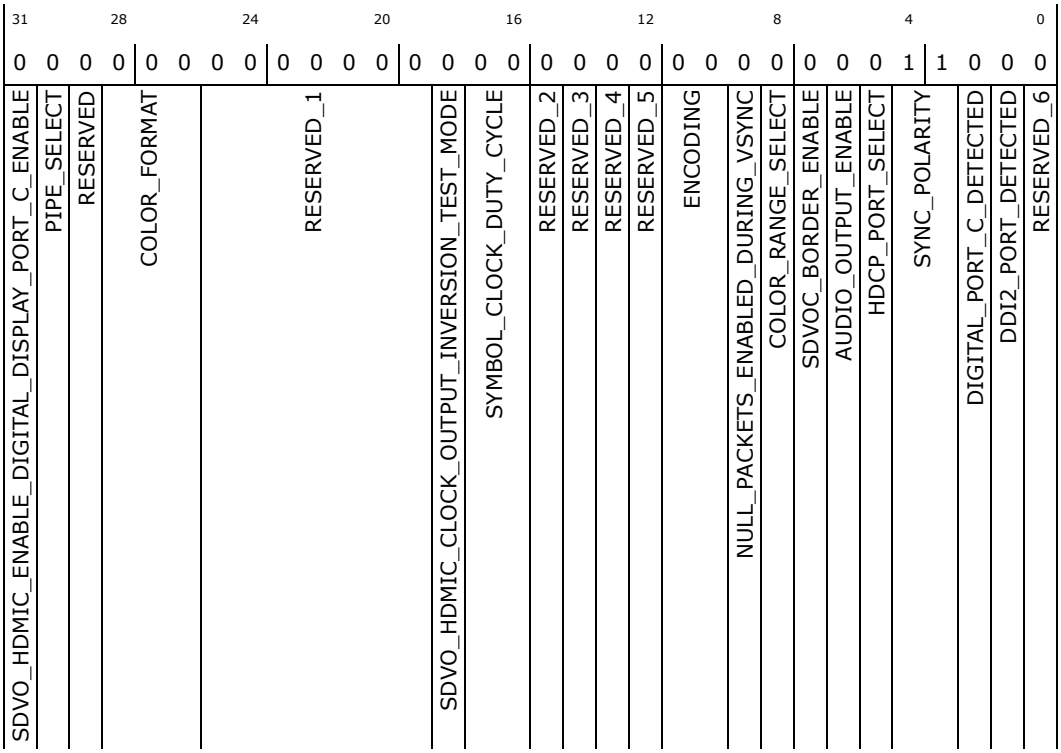
Type: Memory Mapped I/O Register (Size: 32 bits)

HDMIC: [GTTMMADR_LSB + 2BF20h] + 61160h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

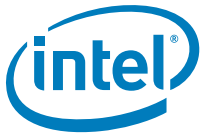
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000018h



Bit Range	Default & Access	Description
31	0b RW	**SDVO_HDMIC_ENABLE_DIGITAL_DISPLAY_PORT_C_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port in HDMI. This port must not be enabled simultaneously with DisplayPort C. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to 0 after disabling the port. This is workaround for hardware issue where the transcoder select set to 1 will prevent DPC from being enabled on transcoder A. [DevIBX] Software must write this bit twice when enabling the port (setting to 1) as a workaround for hardware issue that may result in first write getting masked. [DevIBX] Toggle this bit off then on at the end of mode set sequence when enabling HDMI 12-bit per color with pixel repeat. 1 = Enable. This bit enables the Digital Display Port C interface for HDMI or DVI modes. 0 = Disable and tristates the Digital Display Port C interface for HDMI or DVI modes.
30	0b RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B

Bit Range	Default & Access	Description
29	0b RW	**RESERVED:** [DevCDV]: stall Select: This bit selects stall for external scaling functionality only on SDVO. Programming notes: It is only valid to have a single stall indication to a particular pipe. In cases where two ports are being driven from a single pipe, one of the ports must set this bit to 0. Only sDVOB or sDVOC can select the stall function, as only a single stall input is available between the two interfaces. Set the stall input to unused before programming the external device creating the stall. 0 = Stall input signal is unused on this port 1 = Stall input signal is used to stall the pipe attached to this port
28:26	0b RW	**COLOR_FORMAT:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 = 8 bits per color (Default) 001 = RESERVED for 10 bits per color 010 = RESERVED for 6 bits per color 011 = RESERVED 1xx = RESERVED
25:19	0b RW	**RESERVED_1:** Reserved.
18	0b RW	**SDVO_HDMIC_CLOCK_OUTPUT_INVERSION_TEST_MODE:** Please note that this applies to all modes and is instantly updated. 1 = sDVO/HDMIB Clock output is inverted 0 = sDVO/HDMIB Clock output is NOT inverted (DEFAULT)
17:16	0b RW	**SYMBOL_CLOCK_DUTY_CYCLE:** These bits control the output clock duty cycle to enable EMI mitigation on the external HDMI link. 10/90 cycle has been measured to have ~13dB EMI improvement over a 50/50 duty cycle. 00 = (Default) 50/50 duty cycle: Clock output is 0000011111 01 = 10/90 duty cycle: Clock output is 0111111111 followed by 0000000001 ([DevCL, DevCTG, DevCDV] HDMI only) 10 = 20/80 duty cycle: Clock output is 0011111111 followed by 0000000011 ([DevCL, DevCTG, DevCDV] HDMI only) 11 = Reserved
15	0b RW	**RESERVED_2:** [DevCTG, DevCDV, DevVLVP] Port Lane Reversal: This bit reverses the order of the 4 lanes within the port. Port lane reversal takes place on the Vblank after being written. It is an OEM configurable feature. 0 = (Default) Not reversed 1 = Reversed
14	0b RW	**RESERVED_3:** Reserved.
13	0b RW	**RESERVED_4:** [DevCTG, DevCDV, DevVLVP] Clock Output Disable: This bit disables the clock output on the digital output port. For 8b/10b modes the clock output should be disabled. 0 = (Default) Clock output enabled 1 = Clock output disabled ([DevCL] only)
12	0b RW	**RESERVED_5:** [DevCTG, DevCDV, DevVLVP]: Scrambling enable: This bit enables scrambling for UDI-related modes using ANSI 8b/10b or TMDS encoding. It is not used with SDVO encoding. Software must set this bit appropriately when enabling the port. Scrambling is reset at the beginning of horizontal sync. 0 Scrambling disabled (Default) 1 = Scrambling enabled ([DevCL] only)



Bit Range	Default & Access	Description
11:10	0b RW	**ENCODING:** These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b/10b and TMDS encoding must be programmed using these bits. Please note that ANSI 8b/10b and TMDS encoding can only be enabled on one port at a time, as only one HPD pin is available for use between ports B and C. 00 = Reserved 01 = Reserved 10 = TMDS encoding ([DevCL, DevCTG, DevCDV, DevVLVP] external link and HDMI only) See the HDMI specification for control codes. In this mode, the external HPD pin is used to generate hotplug. In fixed frequency mode, start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 = Reserved
9	0b RW	**NULL_PACKETS_ENABLED_DURING_VSYNC:** This bit enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 = Disable null infoframe packets when Vsync=1 on this port. (Default) 1 = Enable null infoframe packets when Vsync=1 on this port.
8	0b RW	**COLOR_RANGE_SELECT:** This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output ([DevCL and DevCTG] only)
7	0b RW	**SDVOC_BORDER_ENABLE:** This bit determines if the border data from native VGA or the timing generator is to be considered valid pixel data at the external component. 1 = Border to the sDVOC encoder is enabled. Blank# is used to generate the DE output (used in all cases except when the external scaler is used in a DVI panel, over SDVO) . 0 = Border to the sDVOC encoder is disabled. DE (Display Enable) is used
6	0b RW	**AUDIO_OUTPUT_ENABLE:** ([DevCL, DevCTG, DevCDV]): This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. 0 = (Default) No audio output on this port 1 = Enable audio on this port ([DevCL, DevCTG, DevCDV] only)
5	0b RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port ([DevCL, DevCTG, DevCDV] only)
4:3	11b RW	**SYNC_POLARITY:** Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK. For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS BLANK+VS BLANK+VS+HS. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high

Bit Range	Default & Access	Description
2	0b RO	**DIGITAL_PORT_C_DETECTED:** Read-only bit indicating whether a digital port C was detected during initialization. It signifies the level of the GMBUS port 3 (port C) data line at boot. This bit is valid regardless of whether the port is enabled. 0 = Digital Port C not detected during initialization 1 = Digital Port C detected during initialization (default) AccessType: Read Only
1	0b RO	**DDI2_PORT_DETECTED:** Read-only bit indicating whether the DDI2 port was detected during initialization. It signifies the level of the GMBUS port 1 data line at boot. This bit is valid regardless of whether the port is enabled. 0 = DDI2 Port not detected during initialization 1 = DDI2 Port detected during initialization (default) AccessType: Read Only
0	0b RW	**RESERVED_6:** MBZ

3.4.29 DISPLAY_DIGITAL_PORT_HOT_PLUG_CONTROL_REGISTER—Offset 61164h

display digital poty hot plug control register

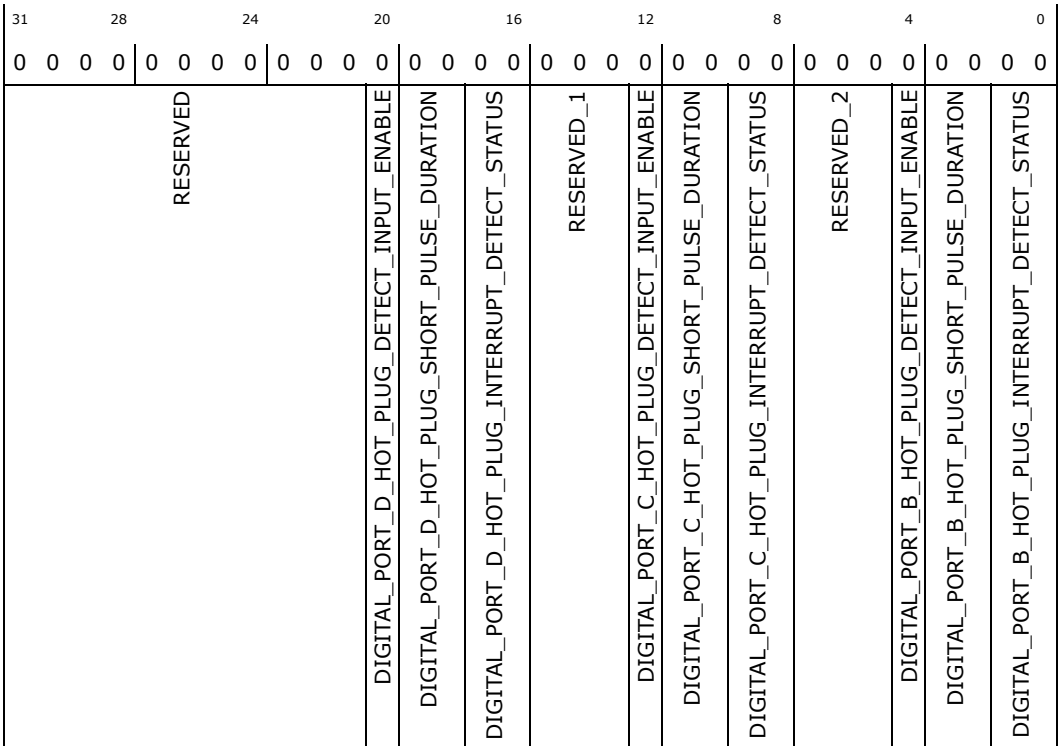
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DISPLAY_DIGITAL_PORT_HOT_PLUG_CONTROL_REGISTER : [GTTMMADR_LSB + 2BF20h] + 61164h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:21	0b RW	**RESERVED:** Project: All Format:
20	0b RW	**DIGITAL_PORT_D_HOT_PLUG_DETECT_INPUT_ENABLE:** Project: All Default Value: 0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. • Value / Name / Description / Project • 0 / Disable / Buffer disabled /All • 1 / Enable / Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin / All
19:18	0b RW	**DIGITAL_PORT_D_HOT_PLUG_SHORT_PULSE_DURATION:** Project: All Default Value: 0b These bits define the duration of the pulse defined as a short pulse. • Value / Name / Description / Project • 00 / 2ms / 2ms / All • 01 / 4.5ms / 4.5ms / All • 10 / 6ms / 6ms / All • 11 / 100ms / 100ms / All

Bit Range	Default & Access	Description
17:16	0b RW/1C	**DIGITAL_PORT_D_HOT_PLUG_INTERRUPT_DETECT_STATUS:** Project: All Default Value: 0b AccessType: One to Clear This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. • Value / Name / Description / Project • 00 / No Detect / Digital port hot plug event not detected / All • X1 / Short Detect / Digital port short pulse hot plug event detected / All • 1X / Long Detect / Digital port long pulse hot plug event detected / All
15:13	0b RW	**RESERVED_1:** Project: All Format:
12	0b RW	**DIGITAL_PORT_C_HOT_PLUG_DETECT_INPUT_ENABLE:** Project: All Default Value: 0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. • Value / Name / Description / Project • 0 / Disable / Buffer disabled / All • 1 / Enable / Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin / All
11:10	0b RW	**DIGITAL_PORT_C_HOT_PLUG_SHORT_PULSE_DURATION:** Project: All Default Value: 0b These bits define the duration of the pulse defined as a short pulse. • Value / Name / Description / Project • 00 / 2ms / 2ms / All • 01 / 4.5ms / 4.5mS / All • 10 / 6ms / 6mS / All • 11 / 100ms / 100mS / All
9:8	0b RW/1C	**DIGITAL_PORT_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** Project: All Default Value: 0b AccessType: One to Clear This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. • Value / Name / Description / Project • 00 / No Detect / Digital port hot plug event not detected / All • X1 / Short Detect / Digital port short pulse hot plug event detected / All • 1X / Long Detect / Digital port long pulse hot plug event detected / All
7:5	0b RW	**RESERVED_2:** Project: All Format:

Bit Range	Default & Access	Description
4	0b RW	**DIGITAL_PORT_B_HOT_PLUG_DETECT_INPUT_ENABLE:** Project: All Default Value: 0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. • Value / Name / Description / Project • 0 / Disable / Buffer disabled / All • 1 / Enable / Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin / All
3:2	0b RW	**DIGITAL_PORT_B_HOT_PLUG_SHORT_PULSE_DURATION:** Project: All Default Value: 0b These bits define the duration of the pulse defined as a short pulse. • Value / Name / Description / Project • 00 / 2ms / 2ms / All • 01 / 4.5ms / 4.5ms / All • 10 / 6ms / 6ms / All • 11 / 100ms / 100ms / All
1:0	0b RW/1C	**DIGITAL_PORT_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** Project: All Default Value: 0b AccessType: One to Clear This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. • Value / Name / Description / Project • 00 / No Detect / Digital port hot plug event not detected / All • X1 / Short Detect / Digital port short pulse hot plug event detected / All • 1X / Long Detect / Digital port long pulse hot plug event detected / All

3.4.30 DV_DETERM—Offset 61168h

DV Determinism Mode Register

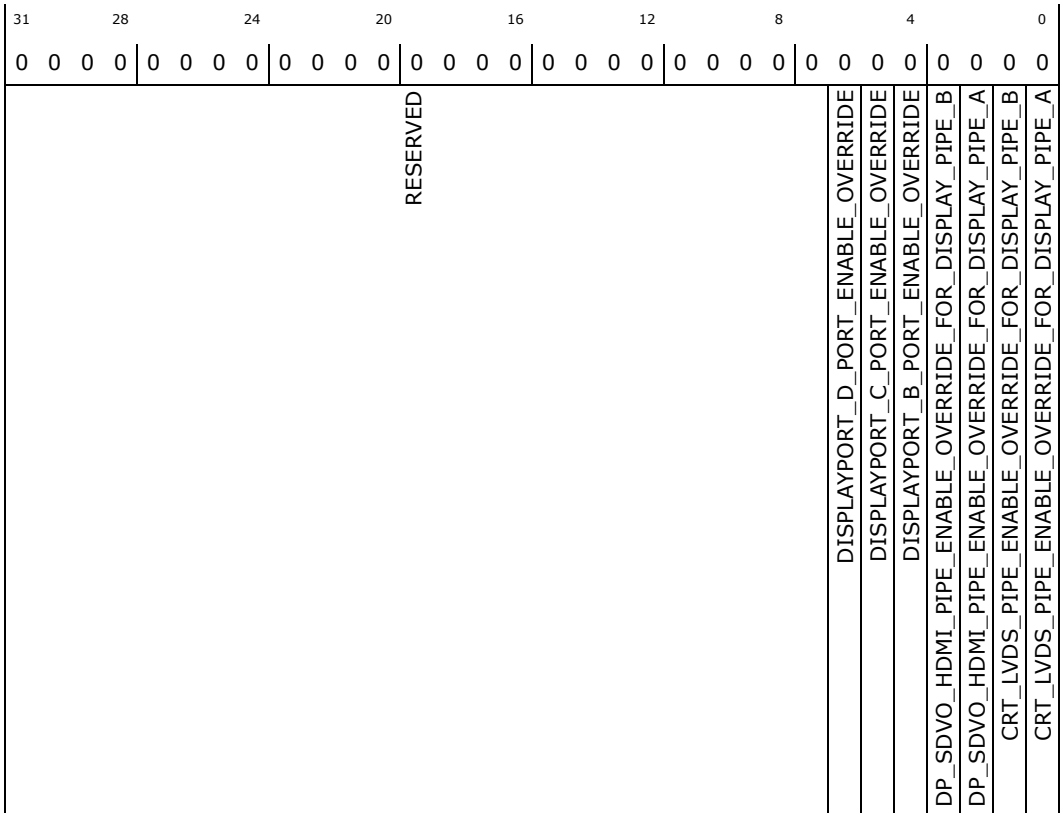
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DV_DETERM: [GTTMMADR_LSB + 2BF20h] + 61168h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0b RW	**RESERVED:** Project: All Format:
6	0b RW	**DISPLAYPORT_D_PORT_ENABLE_OVERRIDE:** Project: All Default Value: 0b • Value / Name / Description / Project • 0b / Normal / Normal operation / All • 1b / Override / DisplayPort D port enable override (controlled from sml0alertb_gp60_mgpio4 pin) / All
5	0b RW	**DISPLAYPORT_C_PORT_ENABLE_OVERRIDE:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override DisplayPort C port enable override (controlled from sus_statb_gp61 pin) All
4	0b RW	**DISPLAYPORT_B_PORT_ENABLE_OVERRIDE:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override DisplayPort B port enable override (controlled from gp57_mgpio5 pin) All
3	0b RW	**DP_SDVO_HDMI_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_B:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override DP/SDVO/HDMI pipe enable override for display pipe B (controlled from gp74_batlowb pin) All

Bit Range	Default & Access	Description
2	0b RW	**DP_SDVO_HDMI_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_A:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override DP/SDVO/HDMI pipe enable override for display pipe A (controlled from slp_s4b pin) All
1	0b RW	**CRT_LVDS_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_B:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override CRT/LVDS pipe enable override for display pipe B (controlled from susclk_gp62 pin) All
0	0b RW	**CRT_LVDS_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_A:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override CRT/LVDS pipe enable override for display pipe A (controlled from slp_mb pin) All

3.4.31 VIDEO_DIP_CTL_B—Offset 61170h

Video DIP Control for Pipe B

Access Method

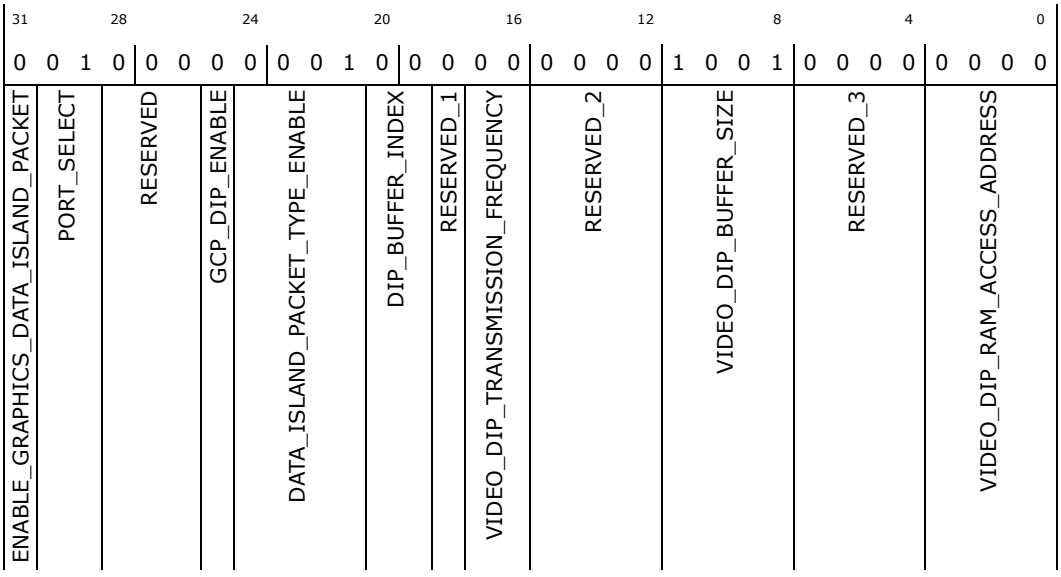
Type: Memory Mapped I/O Register (Size: 32 bits)

VIDEO_DIP_CTL_B: [GTTMMADR_LSB + 2BF20h] + 61170h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 20200900h



Bit Range	Default & Access	Description
31	0b RW	**ENABLE_GRAPHICS_DATA_ISLAND_PACKET:** Project: All See Pipe A description.

Bit Range	Default & Access	Description
30:29	01b RW	**PORT_SELECT:** Project: All See Pipe A description.
28:26	0b RW	**RESERVED:** Project: All Format:
25	0b RW	**GCP_DIP_ENABLE:** Project: All See Pipe A description. This bit should not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode.
24:21	0001b RW	**DATA_ISLAND_PACKET_TYPE_ENABLE:** Project: All See Pipe A description.
20:19	0b RW	**DIP_BUFFER_INDEX:** Project: All See Pipe A description.
18	0b RW	**RESERVED_1:** Project: All Format:
17:16	0b RW	**VIDEO_DIP_TRANSMISSION_FREQUENCY:** Project: All See Pipe A description.
15:12	0b RW	**RESERVED_2:** Project: All Format: MBZ
11:8	1001b RO	**VIDEO_DIP_BUFFER_SIZE:** Project: All AccessType: Read Only Default Value: ;1001b See Pipe A description.
7:4	0b RW	**RESERVED_3:** Project: All Format: MBZ
3:0	0b RO	**VIDEO_DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read only See Pipe A description.

3.4.32 VIDEO_DIP_DATA_B—Offset 61174h

Video Data Island Packet Data for Pipe B

Access Method

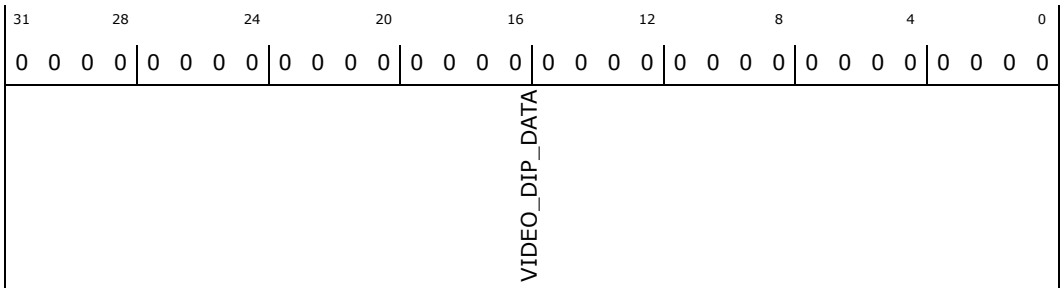
Type: Memory Mapped I/O Register (Size: 32 bits)

VIDEO_DIP_DATA_B: [GTTMMADR_LSB + 2BF20h] + 61174h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**VIDEO_DIP_DATA:** Project: All Format: See Pipe A description.

3.4.33 VIDEO_DIP_GDCP_PAYLOAD_B—Offset 61178h

Video Data Island Payload for Pipe B

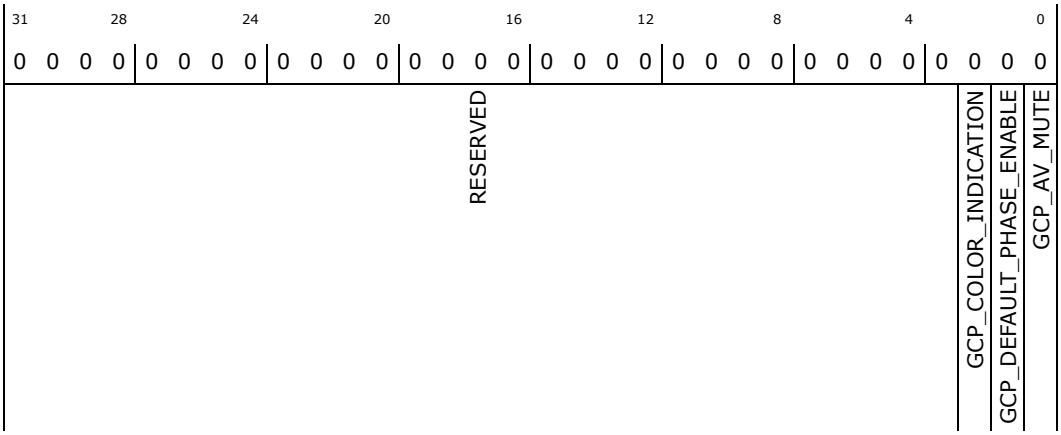
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VIDEO_DIP_GDCP_PAYLOAD_B: [GTTMMADR_LSB + 2BF20h] + 61178h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**RESERVED:** Project: All Format: MBZ
2	0b RW	**GCP_COLOR_INDICATION:** Project: All See Pipe A description.
1	0b RW	**GCP_DEFAULT_PHASE_ENABLE:** Project: All See Pipe A description.
0	0b RW	**GCP_AV_MUTE:** All See Pipe A description.

3.4.34 MIPIA_PORT_CTRL—Offset 61190h

mipi A port ctrl

Access Method

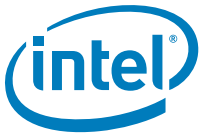
Type: Memory Mapped I/O Register (Size: 32 bits)

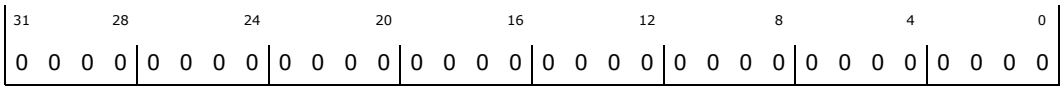
MIPIA_PORT_CTRL: [GTTMMADR_LSB + 2BF20h] + 61190h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h




31 28 24 20 16 12 8 4 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

EN
ADJDLY_HSTX
MIPI_DUAL_LINK_MODE_APPLICABLE_ONLY_IF_MIPI_DUAL_LINK_MODE_IS_ENABLED_THROUGH_MIPI_LANES_CONFIGURATION_BITS
DITHER
RESERVED
SELFLOPPED_HSTX
RESERVED_1
FLISDSI_ADJDLY_HSTX_MIPIA
AFE_LATCHOUT
LPOUTPUT_HOLD
FLISDSI_ADJDLYY_HSTX_MIPIC_HIGH_ORDER
MIPI4DPHY_AdjDly_HSTX_MIPI_C
CSB
CB
FLISDSI_AdjDly_HSTX_MIPI_C_LOWER_ORDER
DELAY
EFFECT
MIPI_LANES_CONFIGURATION

Bit Range	Default & Access	Description
31	0b RW	**EN:** When this bit is disabled the MIPI DPI (video mode) is inactive and in it's low power state. When it is enable it starts to generate timing for this MIPI port 0 = The port is disabled and all MIPI DPI interface are disable (timing generator is off) 1 = The port is enabled
30:27	0b RW	**ADJDLY_HSTX:** These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
26	0b RW	**MIPI_DUAL_LINK_MODE_APPLICABLE_ONLY_IF_MIPI_DUAL_LINK_MODE_IS_ENABLED_THROUGH_MIPI_LANES_CONFIGURATION_BITS:** 0 = Front-Back mode (default) 1 = Pixel alternative mode
25	0b RW	**DITHER:** This bit enables or disables (bypassing) 8-6-bit color dithering function. The usage of this bit would be on for 18-bpp panels and off for 24-bpp panels. 0 = disabled 1 = enabled
24	0b RW	**RESERVED:** Reserved.
23	0b RW	**SELFLOPPED_HSTX:** This bit will be used to mux between the flopped (new) and unflopped (original) versions of the TX HS clock and data. Default 0 = pass through original unflopped version, if set to 1 = pass through the new flopped version of these signals. We probably need to enable validation to always set these to 1 during startup so we're fully testing this logic as it is the intended way we will run A0
22	0b RW	**RESERVED_1:** Reserved.
21:18	0b RW	**FLISDSI_ADJDLY_HSTX_MIPIA:** These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
17	0b RW	**AFE_LATCHOUT:** This bit reflect the value of the output latch of CLK A lane in DSI AFE b1 = current value of output latch is 1 (D-PHY is in LP11 state) b0 = current value of output latch is 0 (D-PHY is in LP00 state) The software driver can read this bit to see if the hold value (LP11 or LP00) to initialize from a sleep state (s0i1 or S0i3) correctly
16	0b RW	**LPOUTPUT_HOLD:** 0= disable transparent latche inside DSI AFE. Output are driven by latch value. 1= enable transparent latch inside DSI AFE so data are driven by DSI DPHY
15	0b RW	**FLISDSI_ADJDLYY_HSTX_MIPIC_HIGH_ORDER:** The fourth bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 1'b0 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature

Bit Range	Default & Access	Description
14:11	0b RW	**MIPI4DPHY_AdjDly_HSTX_MIPI_C:** These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals.[Br] Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
10:9	0b RW	**CSB:** Clock input for bandgap voltage sample and hold circuit. Final setting will be based silicon characterization. 00b = 20mhz clock 01b = 10mhz clock 10b = 40mhz clock 11b = reserved
8	0b RW	**CB:** Bandgap chicken bit 0 = using Penwell band gap circuit 1 = back to LNC circuit
7:5	0b RW	**FLISDSI_AdjDly_HSTX_MIPI_C_LOWER_ORDER:** The lower 3-bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 3'b000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
4	0b RW	**DELAY:** When set, the TE counter will be count down until
3:2	0b RW	**EFFECT:** 00: No tearing effect required - memory write start as soon as write data is available 01: TE trigger by MIPI DPHY and DSI protocol 10: TE trigger by GPIO pin 11: Reserved
1:0	0b RW	**MIPI_LANES_CONFIGURATION:** 00: All 4 MIPI A lanes are assigned to pipe A. All 4 MIPI C lanes are assigned to pipe B. 01: MIPI dual-link mode with data from pipe A 10: MIPI dual-link mode with data from pipe B 11: Reserved Programming note: when MIPI dual-link mode is enabled, the port enable bits in both MIPI A control register and MIPI C control register shall be enabled.

3.4.35 MIPIA_TEARING_CTR—Offset 61194h

mipi A tearing CTR

Access Method

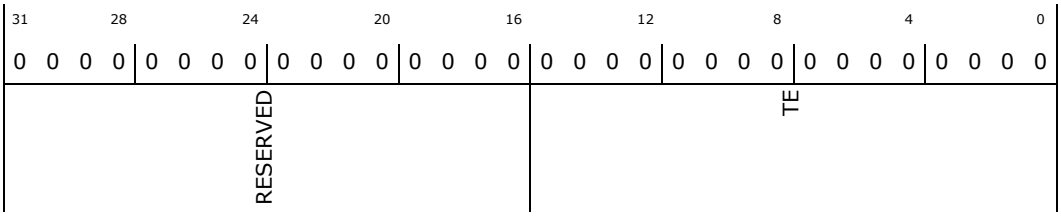
Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_TEARING_CTR: [GTTMMADR_LSB + 2BF20h] + 61194h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**TE:** Number of delay clocks from TE trigger to start sending data to DSI controller

3.4.36 DPA_PIX_GEN_CTRL—Offset 61198h

Display Pipe A Pixel Generator Control

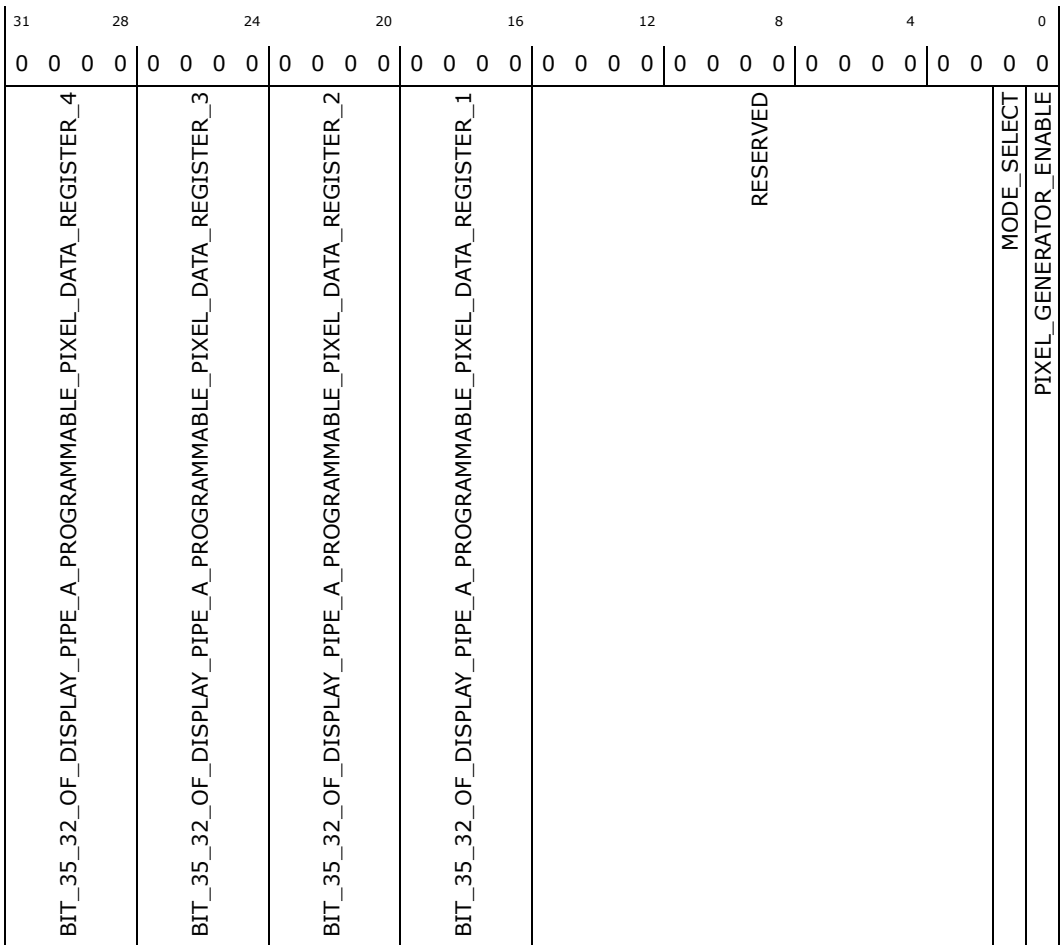
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPA_PIX_GEN_CTRL: [GTTMMADR_LSB + 2BF20h] + 61198h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_4:** Project: All Default Value: 0b
27:24	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_3:** Project: All Default Value: 0b
23:20	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_2:** Project: All Default Value: 0b
19:16	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_1:** Project: All Default Value: 0b
15:2	0b RW	**RESERVED:** Project: All Format:
1	0b RW	**MODE_SELECT:** Project: All Default Value: 0b Pixel generator mode select Value Name Description Project 0b LFSR LFSR All 1b Programmable Programmable pixel data register. Setting mode select to 1 will also start the 2-bit counter. All
0	0b RW	**PIXEL_GENERATOR_ENABLE:** All

3.4.37 MIPIA_AUTOPWG—Offset 611A0h

mipi A autopowergating

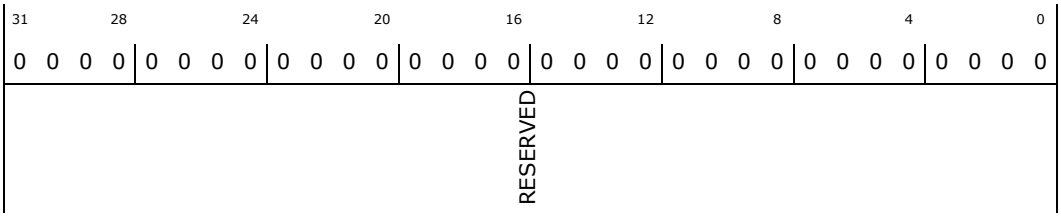
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIA_AUTOPWG: [GTTMMADR_LSB + 2BF20h] + 611A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED:** Reserved.

3.4.38 DPB_PIX_GEN_CTRL—Offset 611B0h

Display Pipe B Pixel Generator Control

Access Method

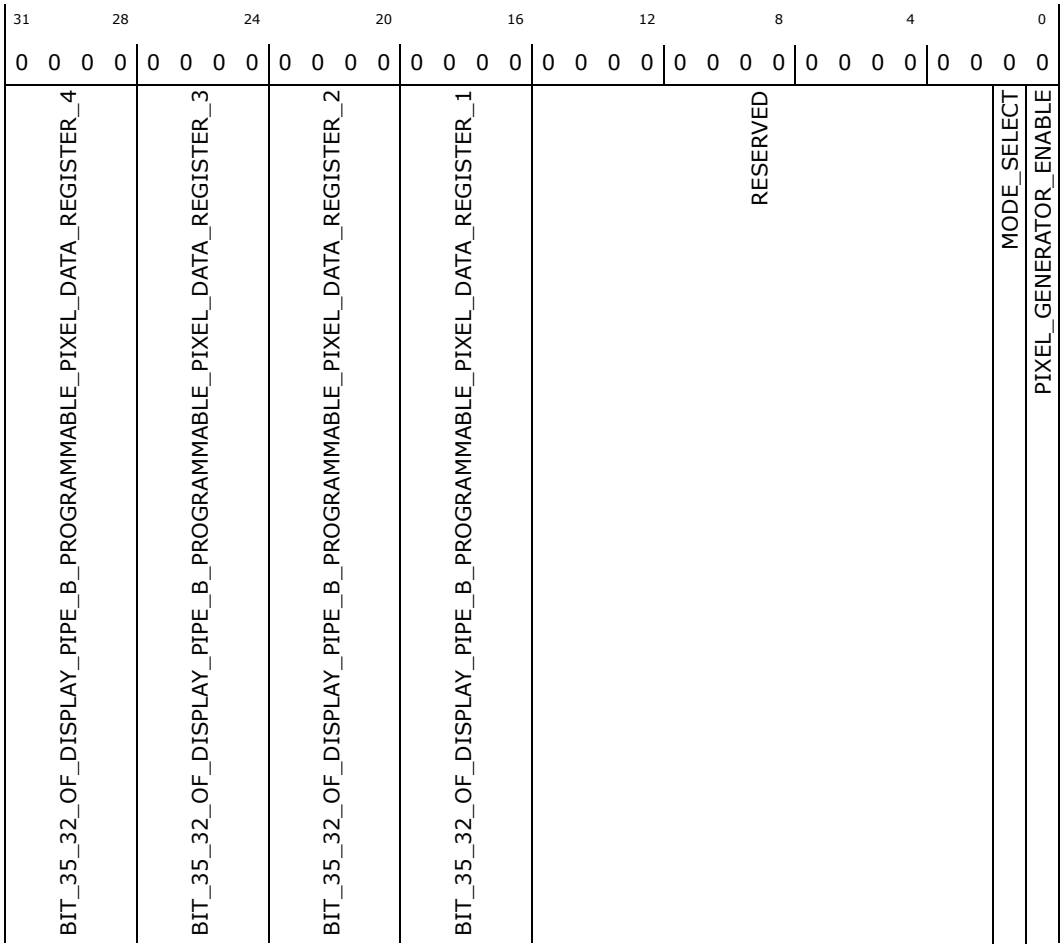
Type: Memory Mapped I/O Register (Size: 32 bits)

DPB_PIX_GEN_CTRL: [GTTMMADR_LSB + 2BF20h] + 611B0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_4:** Project: All Default Value: 0b
27:24	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_3:** Project: All Default Value: 0b Address: GraphicsAddress[35:32]
23:20	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_2:** Project: All Default Value: 0b
19:16	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_1:** Project: All Default Value: 0b

Bit Range	Default & Access	Description
15:2	0b RW	**RESERVED:** Project: All Format:
1	0b RW	**MODE_SELECT:** Project: All Default Value: 0b Pixel generator mode select Value Name Description Project 0b LFSR LFSR All 1b Programmable Programmable pixel data register. Setting mode select to 1 will also start the 2-bit counter. All
0	0b RW	**PIXEL_GENERATOR_ENABLE:** All Format: Enable

3.4.39 PIPEA_PP_STATUS—Offset 61200h

PipeA Panel Power Status Register ([DevCL, DevCTG, DevCDV]) PP Status (dplrreg.v panel_pwr_sr)

Access Method

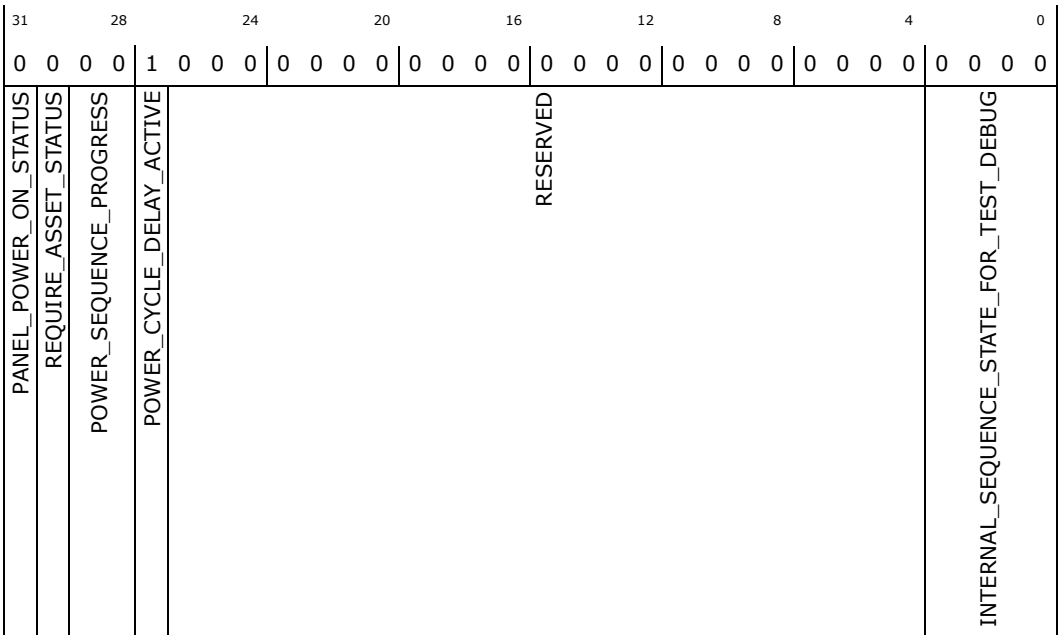
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_PP_STATUS: [GTTMMADR_LSB + 2BF20h] + 61200h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 08000000h



Bit Range	Default & Access	Description
31	0b RO	**PANEL_POWER_ON_STATUS:** 0 = Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program pipe timing and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. 1 = In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the pipe timing and DPLL registers for the pipe that is assigned to the embedded panel output. If the embedded panel port is selected as the target for the panel control, Software is responsible for enabling the LCD display by writing a 1 to the port enable bit only after all pipe timing, DPLL registers are properly programmed, and the PLL has locked to the reference signal. This bit is cleared (set to 0) only after the panel power down sequencing is completed.
30	0b RO	**REQUIRE_ASSET_STATUS:** This bit indicates the status of programming of the display PLL and the selected display port. This a power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. 0 = All required assets are not properly programmed. 1 = All required assets are ready for the driving of a panel. The following conditions determine that the assets are ready: 1) Display Pipe PLL Enabled and frequency locked (bit-31 of DPLL Control Register for the pipe attached to the embedded panel port). 2) Display Pipe Enabled (bit-31 of PIPECONF Pipe Configuration Register. For the pipe attached to the embedded panel port) 3) Embedded Panel Port is Programmed Enabled
29:28	0b RO	**POWER_SEQUENCE_PROGRESS:** 00 = Indicates that the panel is not in a power sequence 01 = Indicates that the panel is in a power up sequence (may include power cycle delay) 10 = Indicates that the panel is in a power down sequence 11 = Reserved
27	1b RO	**POWER_CYCLE_DELAY_ACTIVE:** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing. 0 = A power cycle delay is not currently active 1 = A power cycle delay (T4) is currently active
26:4	0b RO	**RESERVED:** Reserved.
3:0	0b RO	**INTERNAL_SEQUENCE_STATE_FOR_TEST_DEBUG:** 0000 = Power Off Idle (S0.0) 0001 = Power Off, Wait for cycle delay (S0.1) 0010 = Power Off (S0.2) 0011 = Power Off (S0.3) 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Power On Idle (S1.0) 1001 = Power On, (S1.1) 1010 = Power On, (S1.2) 1011 = Power On, Wait for cycle delay (S1.3) 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reset

3.4.40 PIPEA_PP_CONTROL—Offset 61204h

PipeA Panel Power Control Register ([DevCL, DevCTG, DevCDV]) PP Control (dplrreg.v pnl_pwr_cntl)

Access Method

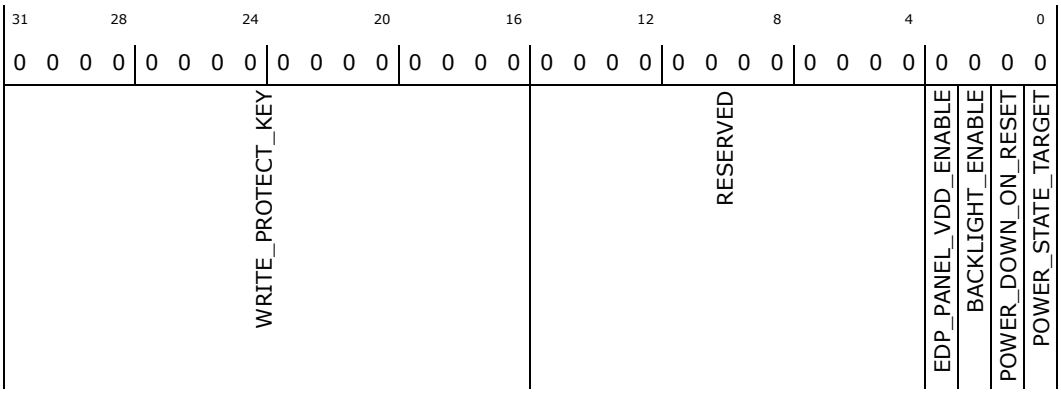
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_PP_CONTROL: [GTTMMADR_LSB + 2BF20h] + 61204h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**WRITE_PROTECT_KEY:** ABCD Write protect off When this field is programmed to anything except the write protect off setting and the panel is either powered up or in the process of a power up sequence, a set of registers involved in generation of panel timing or control become write protected. Any write cycles to those write protected registers, while they will complete as normal, will not change the value of the register when write protected. When this register field contains the write protect off key value, write protect will be unconditionally disabled. In situations where the embedded panel port is unused, the port should remain powered down and the write protect will be inactive. This field in normal operation should be left to all zeros and never programmed with the key value. It exists only to allow testing and workarounds. List of Write protected registers: (LVDS and Panel sequencing Registers): LVDS Digital Display Port Control Address: 61180h 61183h Pipe A Panel power on sequencing delays - Address: 61208-6120Bh Pipe A Panel power off sequencing delays Address: 6120Ch 6120Fh Pipe A Panel power cycle delay and Reference Divisor Address: 61210h 61213 (DPLL registers): DPLL Control Registers FPA0 DPLL Divisor Register FPA1 DPLL Divisor Register 1 FPB0 DPLL Divisor Register FPB1 DPLL Divisor Register 1 (Display Pipe timing registers except source size) HTOTAL Horizontal Total Register HBLANK Horizontal Blank Register HSYNC_ Horizontal Sync Register VTOTAL_ Vertical Total Register VBLANK_ Vertical Blank Register VSYNC_ Vertical Sync Register
15:4	0b RW	**RESERVED:** Reserved.
3	0b RW	**EDP_PANEL_VDD_ENABLE:** [DevCDV]: Enabling this bit enables the panel vdd if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit for eDP link training. After eDP link training is done, software must disable it and let the normal panel power sequencing to take control. 0 = eDP panel Vdd disabled 1 = eDP panel Vdd enabled [DevCLN] Reserved

Bit Range	Default & Access	Description
2	0b RW	**BACKLIGHT_ENABLE:** [DevCTG, DevCDV]: Enabling this bit enables the panel backlight if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit after training the link, and disable it when disabling the panel power state target. 0 = Backlight disabled 1 = Backlight enabled [DevCL] Reserved
1	0b RW	**POWER_DOWN_ON_RESET:** Enabling this bit causes the panel to power down when a reset warning comes to the GMCH from the ICH. When system reset is initiated, the embedded panel port automatically begins the panel power down sequence. If the panel is not on during a reset event, this bit is ignored. 0 = Do not run panel power down sequence when reset is detected 1 = Run panel power down sequence when system is reset
0	0b RW	**POWER_STATE_TARGET:** Writing this bit can occur any time, it will only be used at the completion of any current power cycle. 0 = The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. 1= The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.

3.4.41 PIPEA_PP_ON_DELAYS—Offset 61208h

PipeA Panel Power on Sequencing Delays ([DevCL, DevCTG, DevCDV]) PP On Delay values (dplrreg.v DPLRppon_sd)

Access Method

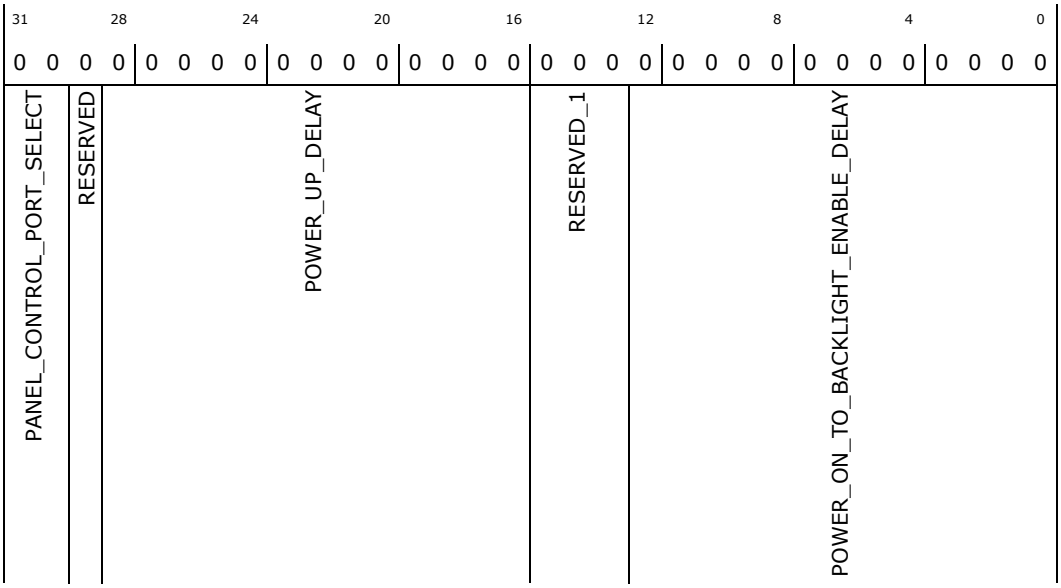
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_PP_ON_DELAYS: [GTTMMADR_LSB + 2BF20h] + 61208h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RW	**PANEL_CONTROL_PORT_SELECT:** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled or if the port is not on pipe-B, then, the power sequence will not allow a panel power up. 00 = Reserved 01 = Panel is connected to the embedded DisplayPort B 10 = Panel is connected to the embedded DisplayPort C 11 = Reserved The selection of non-existent ports are not allowed. This programming will disable panel power sequencing logic.
29	0b RW	**RESERVED:** Reserved.
28:16	0b RW	**POWER_UP_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.
15:13	0b RW	**RESERVED_1:** Reserved.
12:0	0b RW	**POWER_ON_TO_BACKLIGHT_ENABLE_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 (T3 for DisplayPort) time sequence. The time unit used is the 100us timer.

3.4.42 PIPEA_PP_OFF_DELAYS—Offset 6120Ch

PipeA Panel Power off Sequencing Delays ([DevCL, DevCTG, DevCDV]) PP Delay Off values (dplrreg.v DPLRppoff_sd)

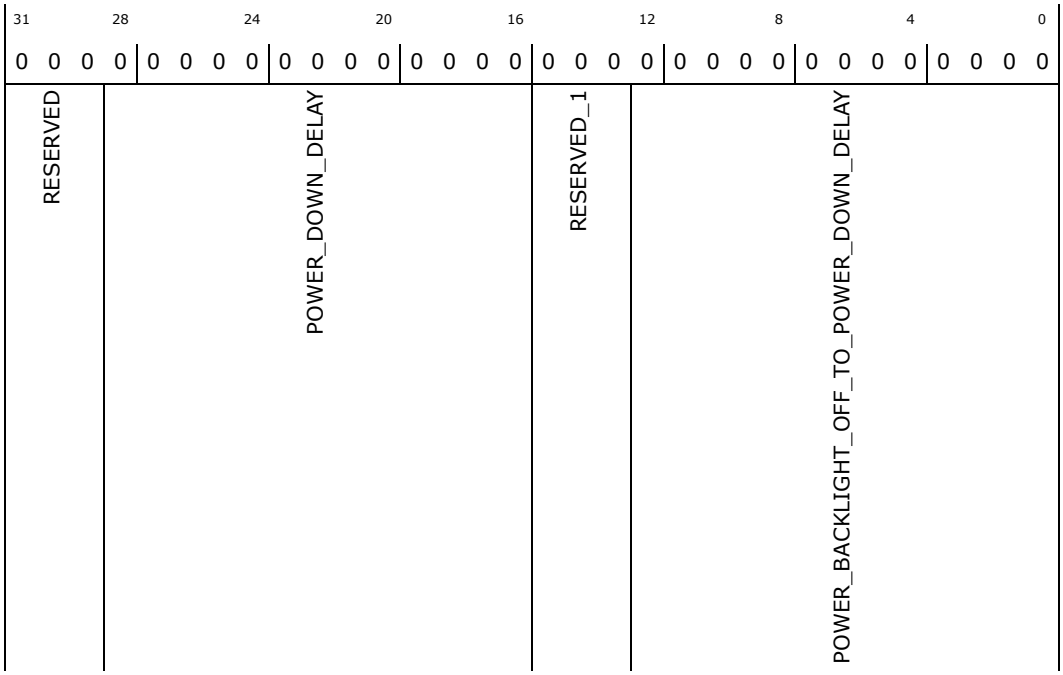
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_PP_OFF_DELAYS: [GTTMMADR_LSB + 2BF20h] + 6120Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Reserved.
28:16	0b RW	**POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 (T5 for DisplayPort) time sequence. The time unit used is the 100us timer.
15:13	0b RW	**RESERVED_1:** Reserved.
12:0	0b RW	**POWER_BACKLIGHT_OFF_TO_POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx (T4 for DisplayPort) time sequence. The time unit used is the 100us timer.

3.4.43 PIPEA_PP_DIVISOR—Offset 61210h

PipeA Panel Power Cycle Delay and Reference Divisor ([DevCL, DevCTG, DevCDV]) PP Divisor (dplrreg.v DPLRrefdiv_pp_cd)

Access Method

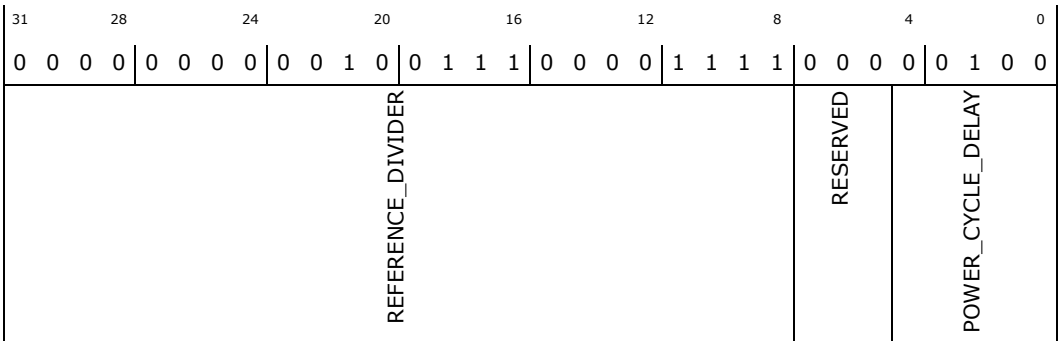
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_PP_DIVISOR: [GTTMMADR_LSB + 2BF20h] + 61210h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00270F04h



Bit Range	Default & Access	Description
31:8	000000000010011100001111b RW	**REFERENCE_DIVIDER:** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100*RefinMHz/2)-1. The default value assumes the default value for the display core clock that is for [DevCL and DevCTG] a 200MHz reference value. The following are examples for other memory speeds. Display Core Frequency Value of Field 233MHz 2D81h 200MHz 270Fh 133MHz 19F9h
7:5	0b RW	**RESERVED:** Reserved.
4:0	00100b RW	**POWER_CYCLE_DELAY:** Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the .1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a +1 value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

3.4.44 PFIT_CONTROL—Offset 61230h

Panel Fitting Controls

Access Method

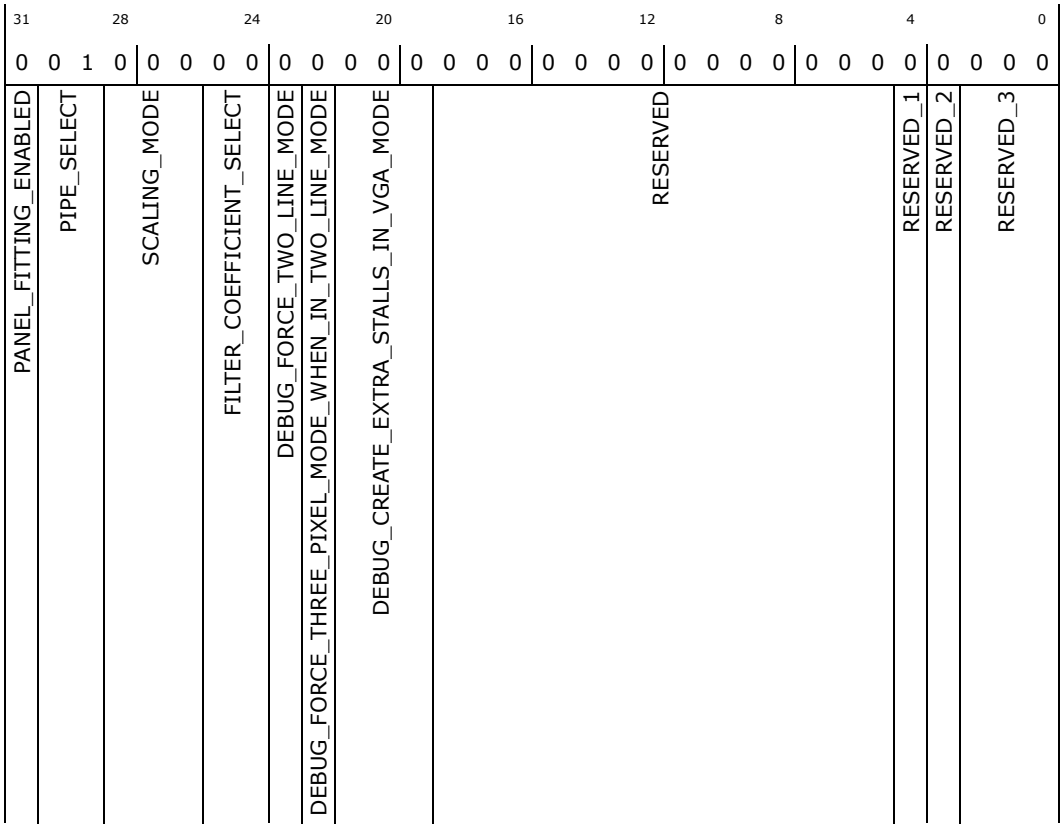
Type: Memory Mapped I/O Register (Size: 32 bits)

PFIT_CONTROL: [GTTMMADR_LSB + 2BF20h] + 61230h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 20000000h



Bit Range	Default & Access	Description
31	0b RW	**PANEL_FITTING_ENABLED:** Disables the panel fitting function by forcing pixels to bypass. Panel fitting must be disabled when running VGA native modes or interlaced modes on the same pipe. Panel fitting should be enabled or disabled before the pipe is enabled. 0 = Bypass the panel fitting (1:1 ratio) 1 = Enable panel fitting (Ratios include 1:1)
30:29	01b RW	**PIPE_SELECT:** Indicates the pipe attached to the panel fitter 00 = Panel fitter is attached to Display Pipe A. 01 = Panel fitter is attached to Display Pipe B. This is the default after reset. 10 = Reserved for pipe C 11 = Reserved for pipe D

Bit Range	Default & Access	Description
28:26	0b RW	**SCALING_MODE:** 000 = Auto-scale (source and destination should have the same aspect ratios) 001 = Programmed scaling: Values in register 61234h will be used for horizontal and vertical scaling factors 010 = Pillarbox (example: 4:3 to 16:9 auto conversion) use only when destination has wider aspect ratio than source 011 = Letterbox (example: 16:9 to 4:3 auto conversion) use only when destination has taller aspect ratio than source 1xx = Reserved
25:24	0b RW	**FILTER_COEFFICIENT_SELECT:** Selects the set of predefined filter coefficients to use for panel fitting 00 = Fuzzy filtering 01 = Crisp edge enhancing filtering 10 = Median between fuzzy and crisp filtering 11 = Reserved
23	0b RW	**DEBUG_FORCE_TWO_LINE_MODE:** debug for two line mode
22	0b RW	**DEBUG_FORCE_THREE_PIXEL_MODE_WHEN_IN_TWO_LINE_MODE:** debug force three pixel mode when in two line mode
21:19	0b RW	**DEBUG_CREATE_EXTRA_STALLS_IN_VGA_MODE:** 000 = No stall 001 = 33% stall 010 = 50% stall 011 = 66% stall 100 = 75% stall 101 = 80% stall 110 = 90% stall 111 = Reserved
18:5	0b RW	**RESERVED:** Reserved.
4	0b RW	**RESERVED_1:** (was Force One Line Mode) write as zero
3	0b RW	**RESERVED_2:** (was Dither Enable which moved to register 61180h)
2:0	0b RW	**RESERVED_3:** Reserved.

3.4.45 PFIT_PGM_RATIOS—Offset 61234h

Programmed Panel Fitting Ratios

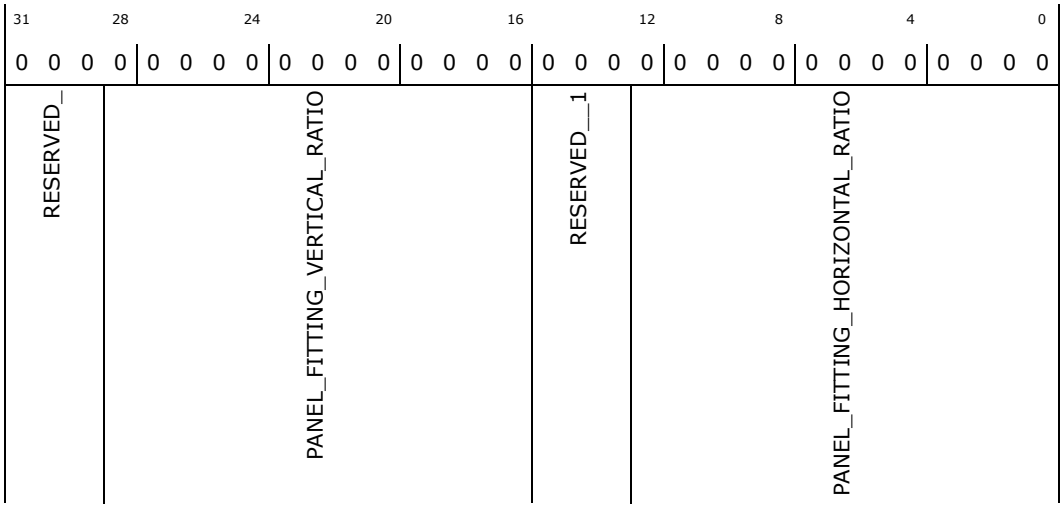
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PFIT_PGM_RATIOS: [GTTMMADR_LSB + 2BF20h] + 61234h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED_:** Reads as zeros
28:16	0b RW	**PANEL_FITTING_VERTICAL_RATIO:** Vertical scaling ratio for panel fitting.
15:13	0b RW	**RESERVED__1:** Reads as zeros
12:0	0b RW	**PANEL_FITTING_HORIZONTAL_RATIO:** Horizontal scaling ratio for panel fitting.

3.4.46 RESERVEDUSEDTOBEAUTOSCALINGRATIOSREADBACK—Offset 61238h

Reserved.

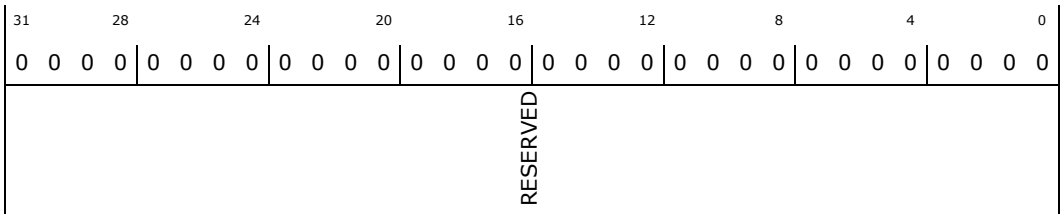
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESERVEDUSEDTOBEAUTOSCALINGRATIOSREADBACK: [GTTMMADR_LSB + 2BF20h] + 61238h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**RESERVED:** Reserved.

3.4.47 RESERVEDUSEDTOBESCALINGINITIALPHASE—Offset 6123Ch

Reserved.

Access Method

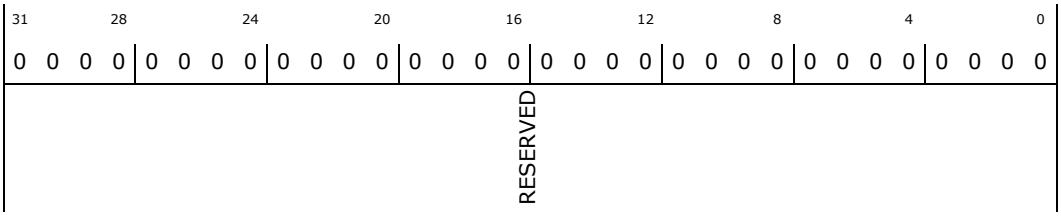
Type: Memory Mapped I/O Register (Size: 32 bits)

RESERVEDUSEDTOBESCALINGINITIALPHASE: [GTTMMADR_LSB + 2BF20h] + 6123Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED:** Reserved.

3.4.48 PIPEA_BLC_PWM_CLT2—Offset 61250h

PipeA Backlight PWM Control Register 2

Access Method

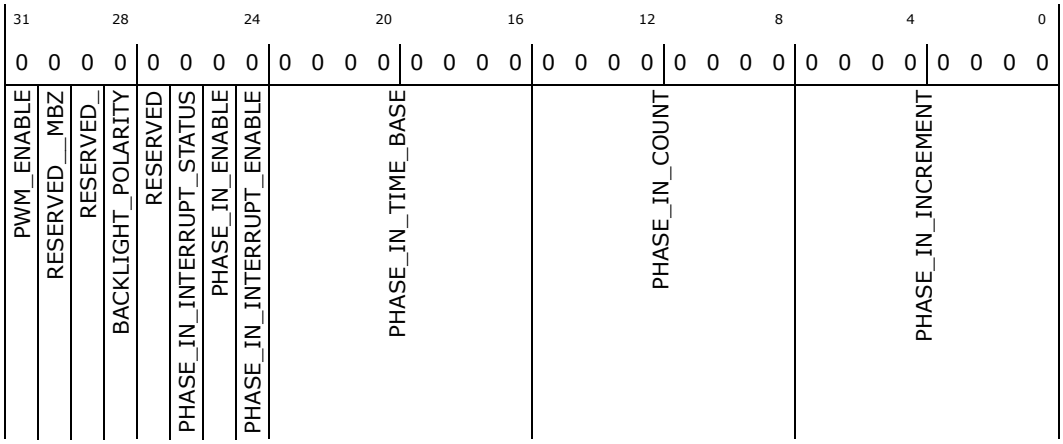
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_BLC_PWM_CLT2: [GTTMMADR_LSB + 2BF20h] + 61250h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**PWM_ENABLE:** This bit enables the PWM counter logic 0 = PWM disabled (drives 0 always) 1 = PWM enabled
30	0b RW	**RESERVED__MBZ:** Reserved.
29	0b RW	**RESERVED_:** Reserved.
28	0b RW	**BACKLIGHT_POLARITY:** This field controls the polarity of the PWM signal. 0 = Active High 1 = Active Low
27	0b RW	**RESERVED:** MBZ
26	0b RW/1C	**PHASE_IN_INTERRUPT_STATUS:** This bit will be set by hardware when a Phase-In interrupt has occurred. Software will clear this bit by writing a 1 , which will reset the interrupt generation. [DevCL-A,B] Reserved AccessType: One to Clear
25	0b RW	**PHASE_IN_ENABLE:** Setting this bit enables a PWM phase in based on the programming of the Phase In registers below. This bit clears itself when the phase in is completed.
24	0b RW	**PHASE_IN_INTERRUPT_ENABLE:** Setting this bit enables an interrupt to be generated when the PWM phase in is completed.
23:16	0b RW	**PHASE_IN_TIME_BASE:** This field determines the number of VBLANK events that pass before one increment occurs. 0 = invalid 1 = 1 vblank 2 = 2 vblanks etc.
15:8	0b RW	**PHASE_IN_COUNT:** This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware-phase-ins are disabled. Reads to this register can occur any time, where the value in this field indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. A value of 0 is invalid. In order to write the same value to this field for the second time, one must write a dummy value to this field, for example, 0 , before writing the real value for the second time.
7:0	0b RW	**PHASE_IN_INCREMENT:** This field indicates the amount to adjust the PWM duty cycle register on each increment event. This is a two s complement number.

3.4.49 PIPEA_BLC_PWM_CTL—Offset 61254h

PipeA Backlight PWM Control Register

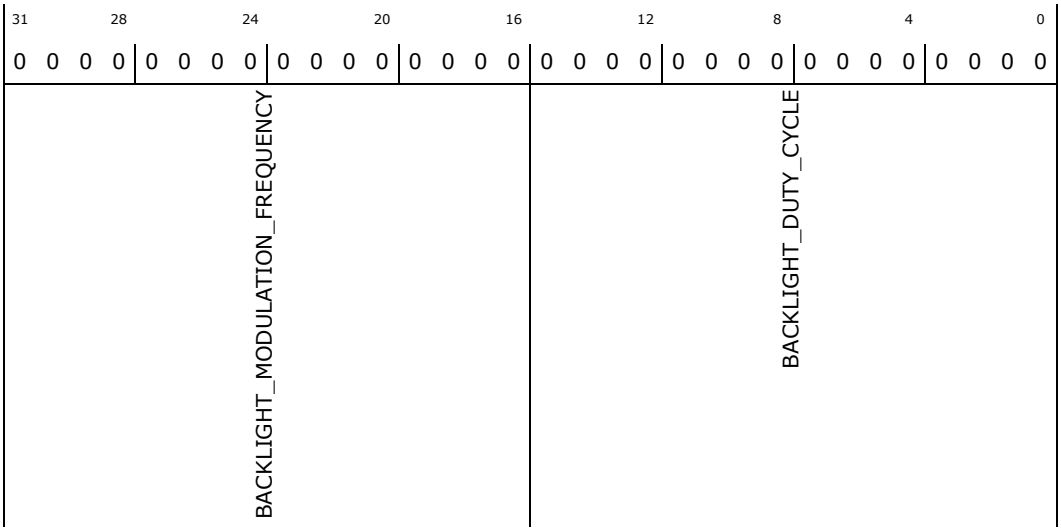
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_BLC_PWM_CTL: [GTTMMADR_LSB + 2BF20h] + 61254h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**BACKLIGHT_MODULATION_FREQUENCY:** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in display core clocks ([DevCTG] 100MHz HRAW clocks) multiplied by 128 or 25MHz S0IX clocks multiplied by 16.
15:0	0b RW	**BACKLIGHT_DUTY_CYCLE:** This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in display core clock ([DevCTG] HRAW clock) periods multiplied by 128 or 25MHz S0IX clocks multiplied by 16.

3.4.50 PIPEA_BLM_HIST_CTL—Offset 61260h

PipeA Image Enhancement Histogram Control Register

Access Method

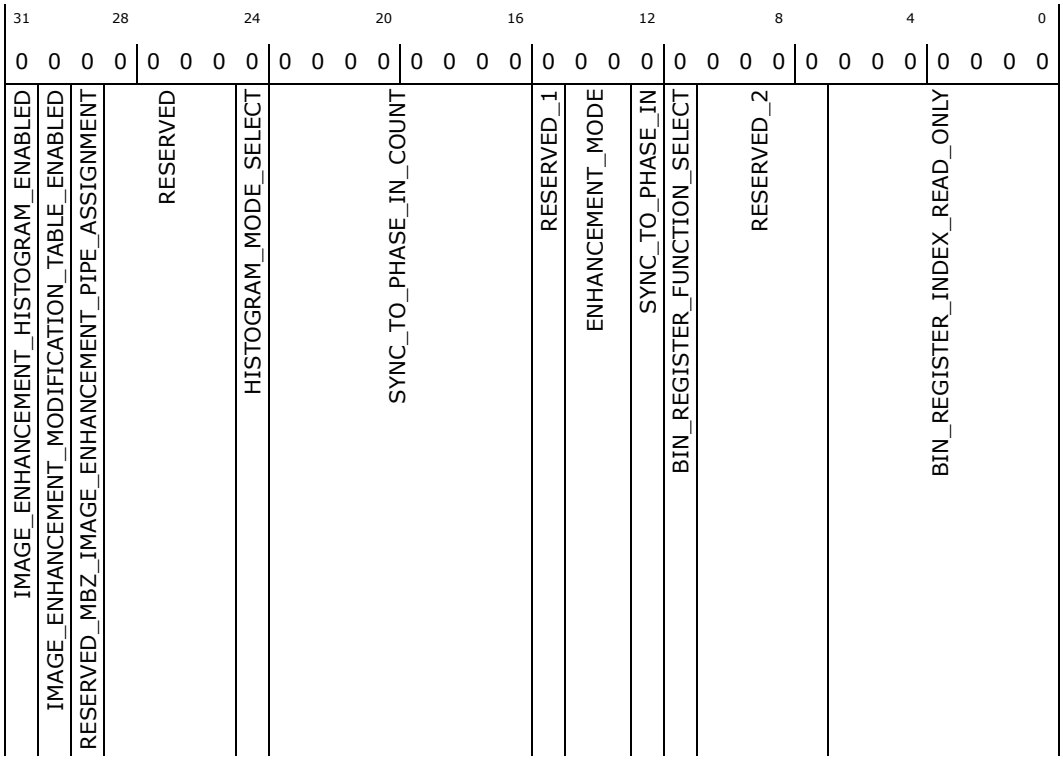
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_BLM_HIST_CTL: [GTTMMADR_LSB + 2BF20h] + 61260h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**IMAGE_ENHANCEMENT_HISTOGRAM_ENABLED:** This bit enables the Image Enhancement histogram logic to collect data. 0 = Image histogram is disabled 1 = The Image histogram is enabled. When this bit is changed from a zero to a one, histogram calculations will begin after the next VBLANK of the assigned pipe.
30	0b RW	**IMAGE_ENHANCEMENT_MODIFICATION_TABLE_ENABLED:** This bit enables the Image Enhancement modification table. 0 = disabled 1 = enabled. When this bit is changed from a zero to a one, modifications begin after the next VBLANK of the assigned pipe.
29	0b RW	**RESERVED_MBZ_IMAGE_ENHANCEMENT_PIPE_ASSIGNMENT:** Each pipe has its own IE function
28:25	0b RW	**RESERVED:** Always write as 0 s.
24	0b RW	**HISTOGRAM_MODE_SELECT:** 0: YUV Luma Mode 1: HSV Intensity Mode - Reserved on [DevCL]

Bit Range	Default & Access	Description
23:16	0b RW	**SYNC_TO_PHASE_IN_COUNT:** This field indicates the phase in count number on which the Image Enhancement table will be loaded if the Sync to Phase in is enabled.
15	0b RW	**RESERVED_1:** Always write as 0.
14:13	0b RW	**ENHANCEMENT_MODE:** 00: Direct look up mode 01: Additive mode 10: Multiplicative mode - Reserved on [DevCL] 11: Reserved
12	0b RW	**SYNC_TO_PHASE_IN:** Setting this bit enables the double buffered registers to be loaded on the phase in count value specified instead of the next vblank.
11	0b RW	**BIN_REGISTER_FUNCTION_SELECT:** This field indicates what data is being written to or read from the bin data register. 0 = Bin Threshold Count. A read from the bin data register returns that bin s threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31. 1 = Bin Image Enhancement Value. Valid range for the Bin Index is 0 to 32
10:7	0b RW	**RESERVED_2:** Always write as 0's.
6:0	0b RW	**BIN_REGISTER_INDEX_READ_ONLY:** This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set.

3.4.51 PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61264h

PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER index registers

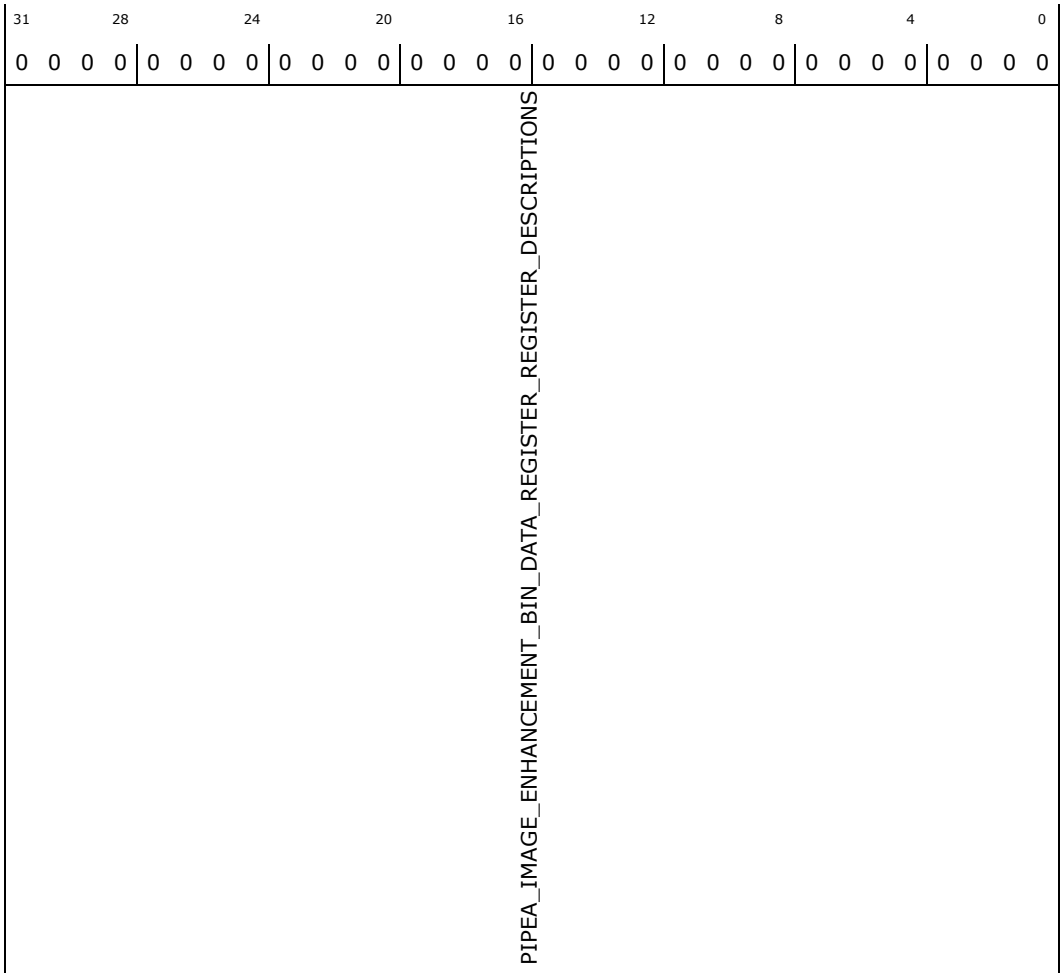
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER: [GTTMMADR_LSB + 2BF20h] + 61264h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER_REGISTER_DESCRIPTIONS:** PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER indexed register descriptions

3.4.52 PIPEAHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61268h

pipeA histrogram threshold gurband register

Access Method

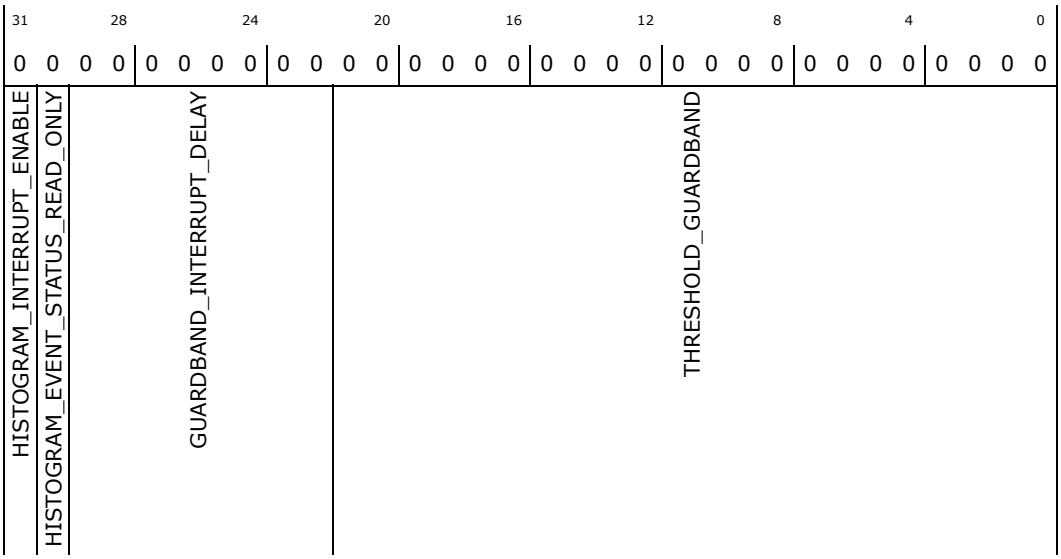
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAHISTOGRAMTHRESHOLDGUARDBANDREGISTER: [GTTMMADR_LSB + 2BF20h] + 61268h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**HISTOGRAM_INTERRUPT_ENABLE:** 0 = Disabled 1 = Enabled. This generates a histogram interrupt once a Histogram event occurs.
30	0b RO	**HISTOGRAM_EVENT_STATUS_READ_ONLY:** When a Histogram event has occurred, this will get set by the hardware. For any more Histogram events to occur, the software needs to clear this bit by writing a '1'. The default state for this bit is '0'. 0 = Histogram event has not occurred. 1 = Histogram event has occurred. AccessType: Read Only
29:22	0b RW	**GUARDBAND_INTERRUPT_DELAY:** An interrupt is generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank. A value of 0 is invalid.
21:0	0b RW	**THRESHOLD_GUARDBAND:** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank

3.4.53 PIPEB_PP_STATUS—Offset 61300h

PipeB Panel Power Status Register ([DevVLVP]) PP Status (dplrreg.v panel_pwr_sr)

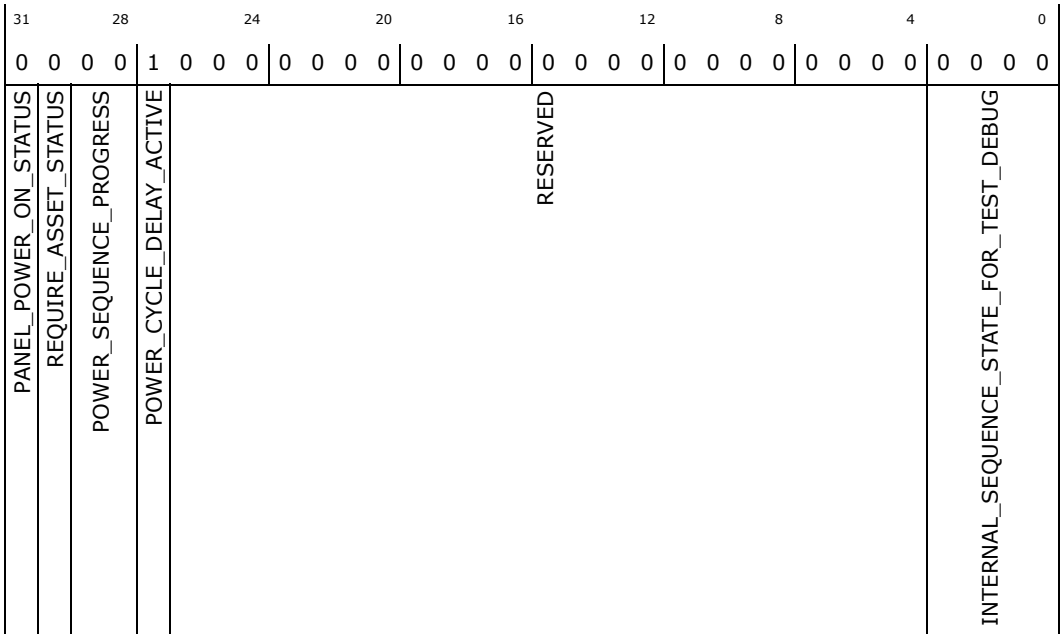
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_PP_STATUS: [GTTMMADR_LSB + 2BF20h] + 61300h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 08000000h



Bit Range	Default & Access	Description
31	0b RO	**PANEL_POWER_ON_STATUS:** 0 = Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program pipe timing and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. 1 = In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the pipe timing and DPLL registers for the pipe that is assigned to the embedded panel output. If the embedded panel port is selected as the target for the panel control, Software is responsible for enabling the LCD display by writing a 1 to the port enable bit only after all pipe timing, DPLL registers are properly programmed, and the PLL has locked to the reference signal. This bit is cleared (set to 0) only after the panel power down sequencing is completed.
30	0b RO	**REQUIRE_ASSET_STATUS:** This bit indicates the status of programming of the display PLL and the selected display port. This a power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. 0 = All required assets are not properly programmed. 1 = All required assets are ready for the driving of a panel. The following conditions determine that the assets are ready: 1) Display Pipe PLL Enabled and frequency locked (bit-31 of DPLL Control Register for the pipe attached to the embedded panel port). 2) Display Pipe Enabled (bit-31 of PIPECONF Pipe Configuration Register. For the pipe attached to the embedded panel port) 3) Embedded Panel Port is Programmed Enabled
29:28	0b RO	**POWER_SEQUENCE_PROGRESS:** 00 = Indicates that the panel is not in a power sequence 01 = Indicates that the panel is in a power up sequence (may include power cycle delay) 10 = Indicates that the panel is in a power down sequence 11 = Reserved

Bit Range	Default & Access	Description
27	1b RO	**POWER_CYCLE_DELAY_ACTIVE:** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing. 0 = A power cycle delay is not currently active 1 = A power cycle delay (T4) is currently active
26:4	0b RO	**RESERVED:** Reserved.
3:0	0b RO	**INTERNAL_SEQUENCE_STATE_FOR_TEST_DEBUG:** 0000 = Power Off Idle (S0.0) 0001 = Power Off, Wait for cycle delay (S0.1) 0010 = Power Off (S0.2) 0011 = Power Off (S0.3) 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Power On Idle (S1.0) 1001 = Power On, (S1.1) 1010 = Power On, (S1.2) 1011 = Power On, Wait for cycle delay (S1.3) 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reset

3.4.54 PIPEB_PP_CONTROL—Offset 61304h

PipeB Panel Power Control Register ([DevVLVP]) PP Control (dplrreg.v pnl_pwr_cntl)

Access Method

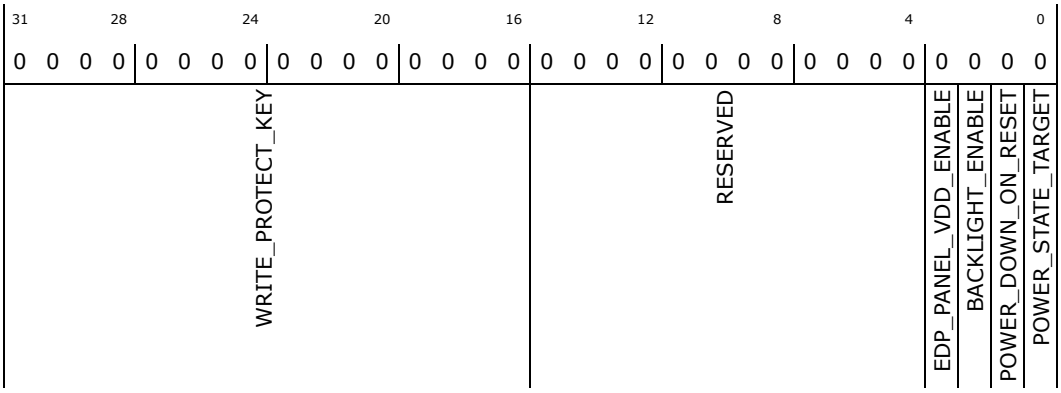
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_PP_CONTROL: [GTTMMADR_LSB + 2BF20h] + 61304h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**WRITE_PROTECT_KEY:** ABCD Write protect off When this field is programmed to anything except the write protect off setting and the panel is either powered up or in the process of a power up sequence, a set of registers involved in generation of panel timing or control become write protected. Any write cycles to those write protected registers, while they will complete as normal, will not change the value of the register when write protected. When this register field contains the write protect off key value, write protect will be unconditionally disabled. In situations where the embedded panel port is unused, the port should remain powered down and the write protect will be inactive. This field in normal operation should be left to all zeros and never programmed with the key value. It exists only to allow testing and workarounds. List of Write protected registers: (Panel sequencing Registers): Pipe B Panel power on sequencing delays - Address: 61308-6130Bh Pipe B Panel power off sequencing delays Address: 6130Ch 6130Fh Pipe B Panel power cycle delay and Reference Divisor Address: 61310h 61313 (DPLL registers): DPLL Control Registers FPA0 DPLL Divisor Register FPA1 DPLL Divisor Register 1 FPB0 DPLL Divisor Register FPB1 DPLL Divisor Register 1 (Display Pipe timing registers except source size) HTOTAL Horizontal Total Register HBLANK Horizontal Blank Register HSYNC_ Horizontal Sync Register VTOTAL_ Vertical Total Register VBLANK_ Vertical Blank Register VSYNC_ Vertical Sync Register
15:4	0b RW	**RESERVED:** Reserved.
3	0b RW	**EDP_PANEL_VDD_ENABLE:** [DevCDV]: Enabling this bit enables the panel vdd if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit for eDP link training. After eDP link training is done, software must disable it and let the normal panel power sequencing to take control. 0 = eDP panel Vdd disabled 1 = eDP panel Vdd enabled [DevCLN] Reserved
2	0b RW	**BACKLIGHT_ENABLE:** [DevCTG, DevCDV]: Enabling this bit enables the panel backlight if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit after training the link, and disable it when disabling the panel power state target. 0 = Backlight disabled 1 = Backlight enabled [DevCL] Reserved
1	0b RW	**POWER_DOWN_ON_RESET:** Enabling this bit causes the panel to power down when a reset warning comes to the GMCH from the ICH. When system reset is initiated, the embedded panel port automatically begins the panel power down sequence. If the panel is not on during a reset event, this bit is ignored. 0 = Do not run panel power down sequence when reset is detected 1 = Run panel power down sequence when system is reset
0	0b RW	**POWER_STATE_TARGET:** Writing this bit can occur any time, it will only be used at the completion of any current power cycle. 0 = The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. 1= The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.

3.4.55 PIPEB_PP_ON_DELAYS—Offset 61308h

PipeB Panel Power on Sequencing Delays ([DevVLVP]) PP On Delay values (dplrreg.v DPLRppon_sd)

Access Method

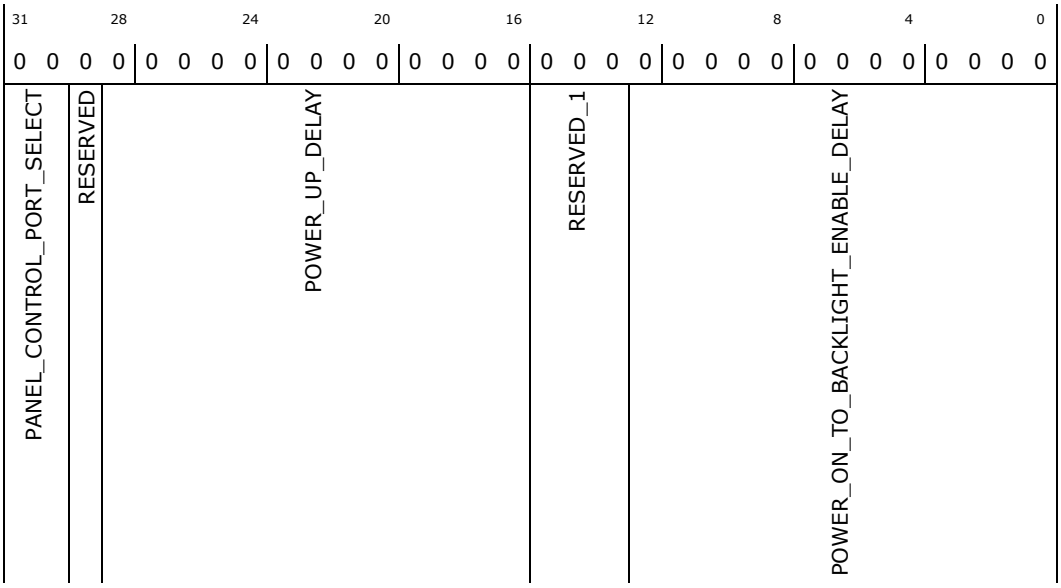
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_PP_ON_DELAYS: [GTTMMADR_LSB + 2BF20h] + 61308h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RW	**PANEL_CONTROL_PORT_SELECT:** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled or if the port is not on pipe-B, then, the power sequence will not allow a panel power up. 00 = Reserved 01 = Panel is connected to the embedded DisplayPort B 10 = Panel is connected to the embedded DisplayPort C 11 = Reserved The selection of non-existent ports are not allowed. This programming will disable panel power sequencing logic.
29	0b RW	**RESERVED:** Reserved.
28:16	0b RW	**POWER_UP_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.
15:13	0b RW	**RESERVED_1:** Reserved.

Bit Range	Default & Access	Description
12:0	0b RW	**POWER_ON_TO_BACKLIGHT_ENABLE_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 (T3 for DisplayPort) time sequence. The time unit used is the 100us timer.

3.4.56 PIPEB_PP_OFF_DELAYS—Offset 6130Ch

PipeB Panel Power off Sequencing Delays ([DevVLVP]) PP Delay Off values (dplrreg.v DPLRppoff_sd)

Access Method

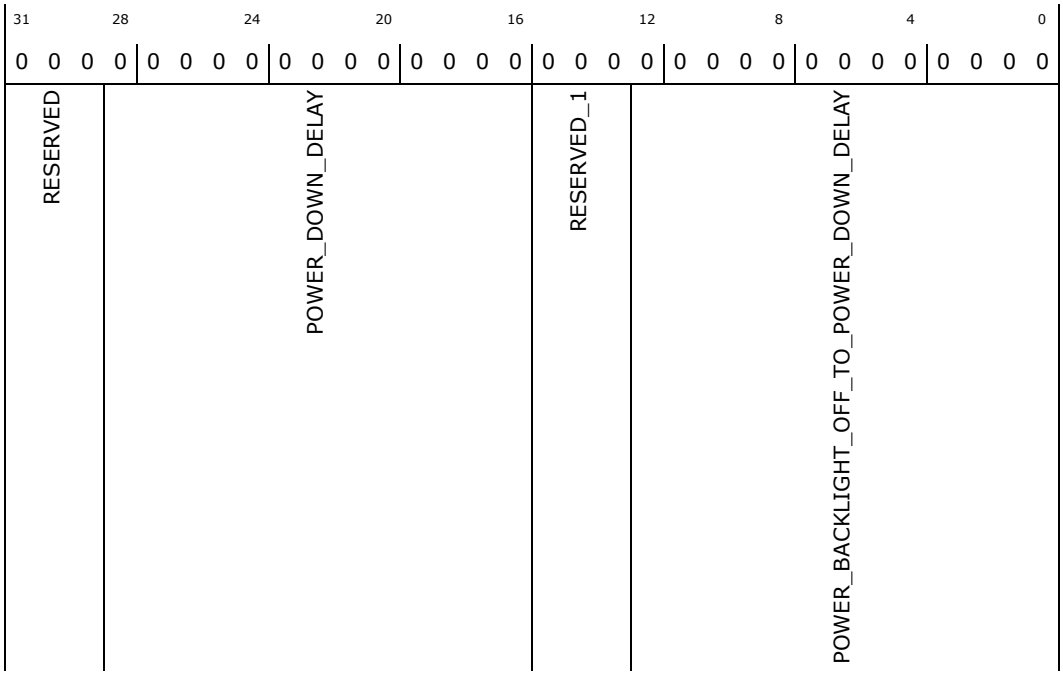
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_PP_OFF_DELAYS: [GTTMMADR_LSB + 2BF20h] + 6130Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0b RW	**RESERVED:** Reserved.
28:16	0b RW	**POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 (T5 for DisplayPort) time sequence. The time unit used is the 100us timer.

Bit Range	Default & Access	Description
15:13	0b RW	**RESERVED_1:** Reserved.
12:0	0b RW	**POWER_BACKLIGHT_OFF_TO_POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx (T4 for DisplayPort) time sequence. The time unit used is the 100us timer.

3.4.57 PIPEB_PP_DIVISOR—Offset 61310h

PipeB Panel Power Cycle Delay and Reference Divisor ([DevVLVP]) PP Divisor (dplrreg.vDPLRrefdiv_pp_cd)

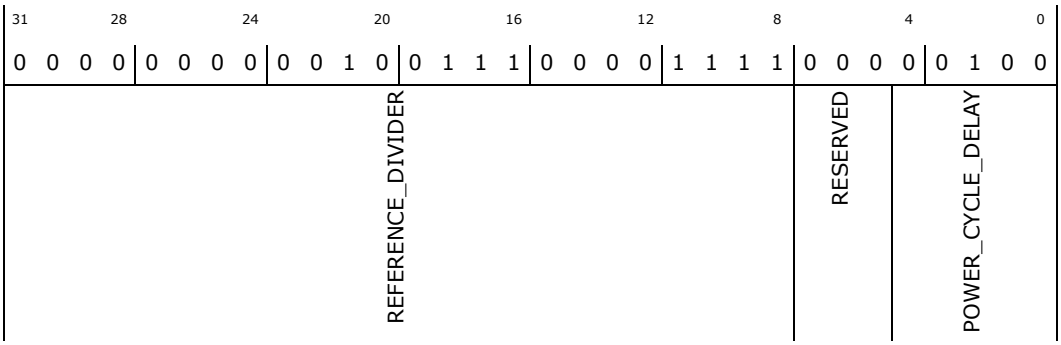
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_PP_DIVISOR: [GTTMMADR_LSB + 2BF20h] + 61310h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00270F04h



Bit Range	Default & Access	Description
31:8	000000000010011100001111b RW	**REFERENCE_DIVIDER:** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100*RefinMHz/2)-1. The default value assumes the default value for the display core clock that is for [DevCL and DevCTG] a 200MHz reference value. The following are examples for other memory speeds. Display Core Frequency Value of Field 233MHz 2D81h 200MHz 270Fh 133MHz 19F9h
7:5	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
4:0	00100b RW	**POWER_CYCLE_DELAY:** Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the .1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a +1 value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

3.4.58 PIPEB_BLC_PWM_CLT2—Offset 61350h

PipeB Backlight PWM Control Register 2

Access Method

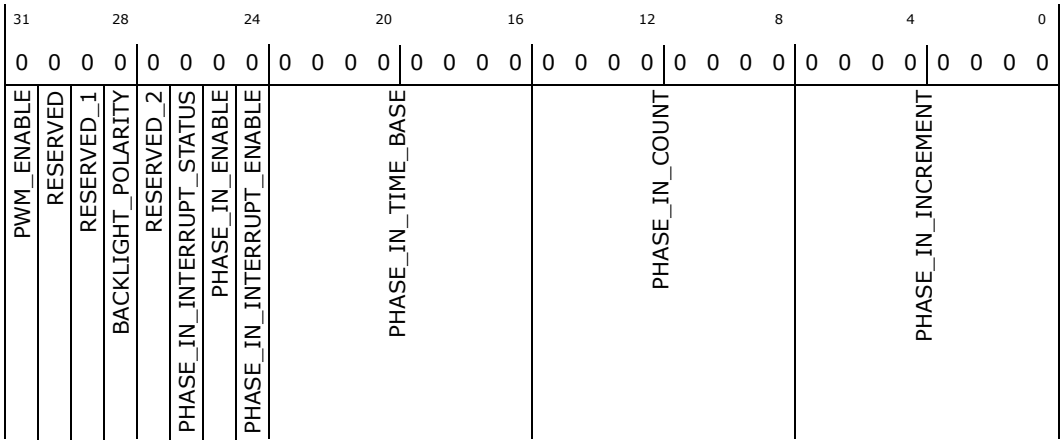
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_BLC_PWM_CLT2: [GTTMMADR_LSB + 2BF20h] + 61350h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**PWM_ENABLE:** This bit enables the PWM counter logic 0 = PWM disabled (drives 0 always) 1 = PWM enabled
30	0b RW	**RESERVED:** MBZ

Bit Range	Default & Access	Description
29	0b RW	**RESERVED_1:** Reserved.
28	0b RW	**BACKLIGHT_POLARITY:** This field controls the polarity of the PWM signal. 0 = Active High 1 = Active Low
27	0b RW	**RESERVED_2:** MBZ
26	0b RW/1C	**PHASE_IN_INTERRUPT_STATUS:** This bit will be set by hardware when a Phase-In interrupt has occurred. Software will clear this bit by writing a 1 , which will reset the interrupt generation. [DevCL-A,B] Reserved AccessType: One to Clear
25	0b RW	**PHASE_IN_ENABLE:** Setting this bit enables a PWM phase in based on the programming of the Phase In registers below. This bit clears itself when the phase in is completed.
24	0b RW	**PHASE_IN_INTERRUPT_ENABLE:** Setting this bit enables an interrupt to be generated when the PWM phase in is completed.
23:16	0b RW	**PHASE_IN_TIME_BASE:** This field determines the number of VBLANK events that pass before one increment occurs. 0 = invalid 1 = 1 vblank 2 = 2 vblanks etc.
15:8	0b RW	**PHASE_IN_COUNT:** This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware-phase-ins are disabled. Reads to this register can occur any time, where the value in this field indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. A value of 0 is invalid. In order to write the same value to this field for the second time, one must write a dummy value to this field, for example, 0 , before writing the real value for the second time.
7:0	0b RW	**PHASE_IN_INCREMENT:** This field indicates the amount to adjust the PWM duty cycle register on each increment event. This is a two s complement number.

3.4.59 PIPEB_BLC_PWM_CTL—Offset 61354h

PipeB Backlight PWM Control Register

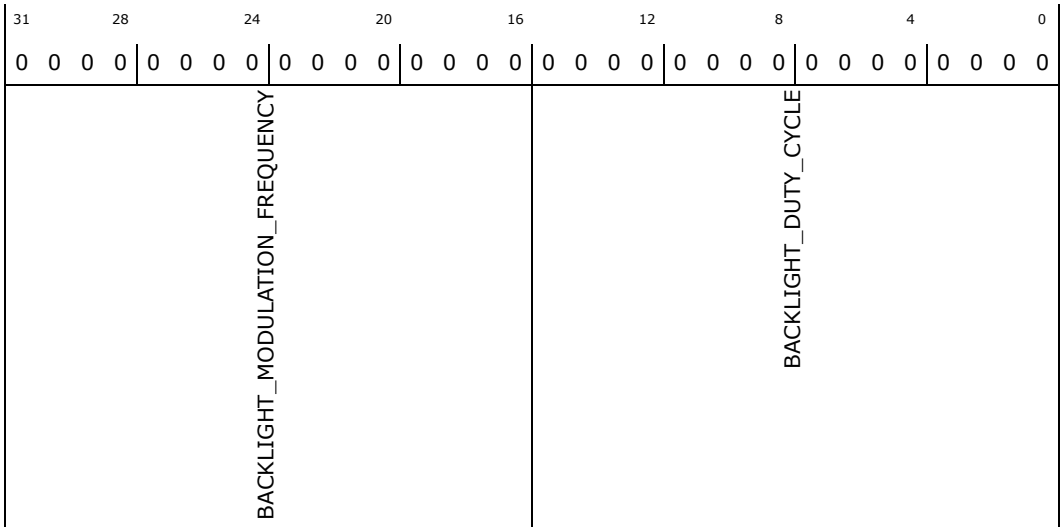
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_BLC_PWM_CTL: [GTTMMADR_LSB + 2BF20h] + 61354h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**BACKLIGHT_MODULATION_FREQUENCY:** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in display core clocks ([DevCTG] HRAW clocks) multiplied by 128 or 25MHz S0IX clocks multiplied by 16.
15:0	0b RW	**BACKLIGHT_DUTY_CYCLE:** This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in display core clock ([DevCTG] HRAW clock) periods multiplied by 128 or 25MHz S0IX clocks multiplied by 16.

3.4.60 PIPEB_BLM_HIST_CTL—Offset 61360h

PipeB Image Enhancement Histogram Control Register

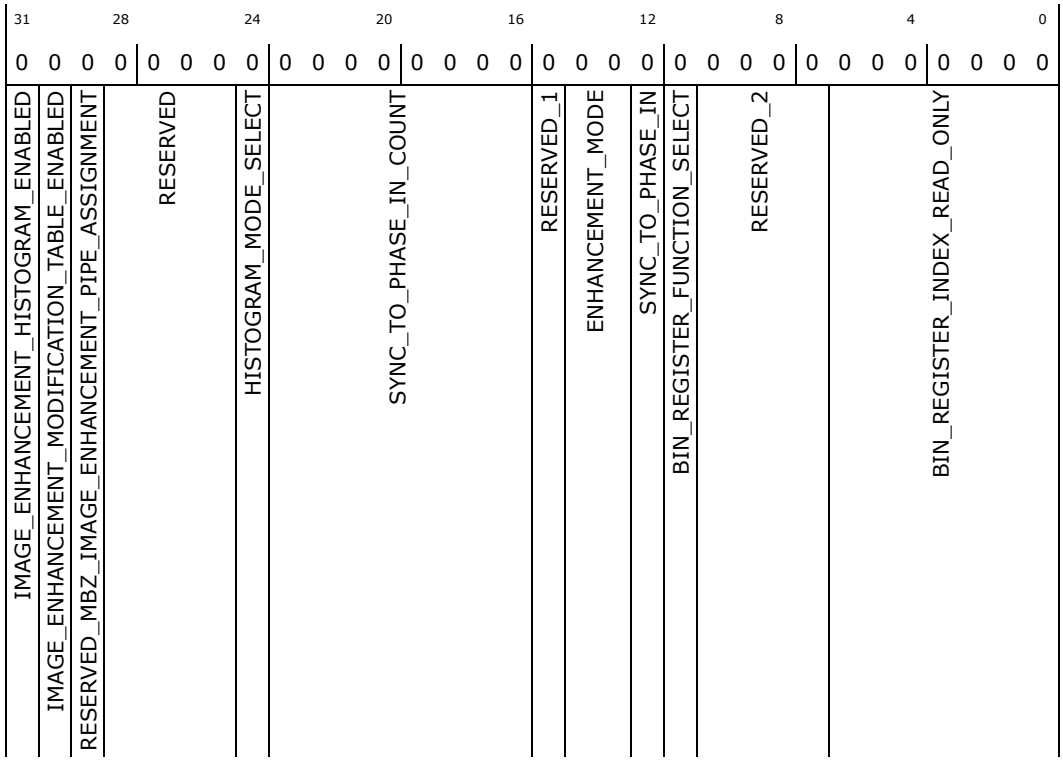
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_BLM_HIST_CTL: [GTTMMADR_LSB + 2BF20h] + 61360h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**IMAGE_ENHANCEMENT_HISTOGRAM_ENABLED:** This bit enables the Image Enhancement histogram logic to collect data. 0 = Image histogram is disabled 1 = The Image histogram is enabled. When this bit is changed from a zero to a one, histogram calculations will begin after the next VBLANK of the assigned pipe.
30	0b RW	**IMAGE_ENHANCEMENT_MODIFICATION_TABLE_ENABLED:** This bit enables the Image Enhancement modification table. 0 = disabled 1 = enabled. When this bit is changed from a zero to a one, modifications begin after the next VBLANK of the assigned pipe.
29	0b RW	**RESERVED_MBZ_IMAGE_ENHANCEMENT_PIPE_ASSIGNMENT:** Each pipe has its own dedicated IE function.
28:25	0b RW	**RESERVED:** Always write as 0 s.
24	0b RW	**HISTOGRAM_MODE_SELECT:** 0: YUV Luma Mode 1: HSV Intensity Mode - Reserved on [DevCL]
23:16	0b RW	**SYNC_TO_PHASE_IN_COUNT:** This field indicates the phase in count number on which the Image Enhancement table will be loaded if the Sync to Phase in is enabled.
15	0b RW	**RESERVED_1:** Always write as 0.
14:13	0b RW	**ENHANCEMENT_MODE:** 00: Direct look up mode 01: Additive mode 10: Multiplicative mode - Reserved on [DevCL] 11: Reserved

Bit Range	Default & Access	Description
12	0b RW	**SYNC_TO_PHASE_IN:** Setting this bit enables the double buffered registers to be loaded on the phase in count value specified instead of the next vblank.
11	0b RW	**BIN_REGISTER_FUNCTION_SELECT:** This field indicates what data is being written to or read from the bin data register. 0 = Bin Threshold Count. A read from the bin data register returns that bin s threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31. 1 = Bin Image Enhancement Value. Valid range for the Bin Index is 0 to 32
10:7	0b RW	**RESERVED_2:** Always write as 0's.
6:0	0b RO	**BIN_REGISTER_INDEX_READ_ONLY:** This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set. AccessType: Read Only

3.4.61 PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61364h

PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER index registers

Access Method

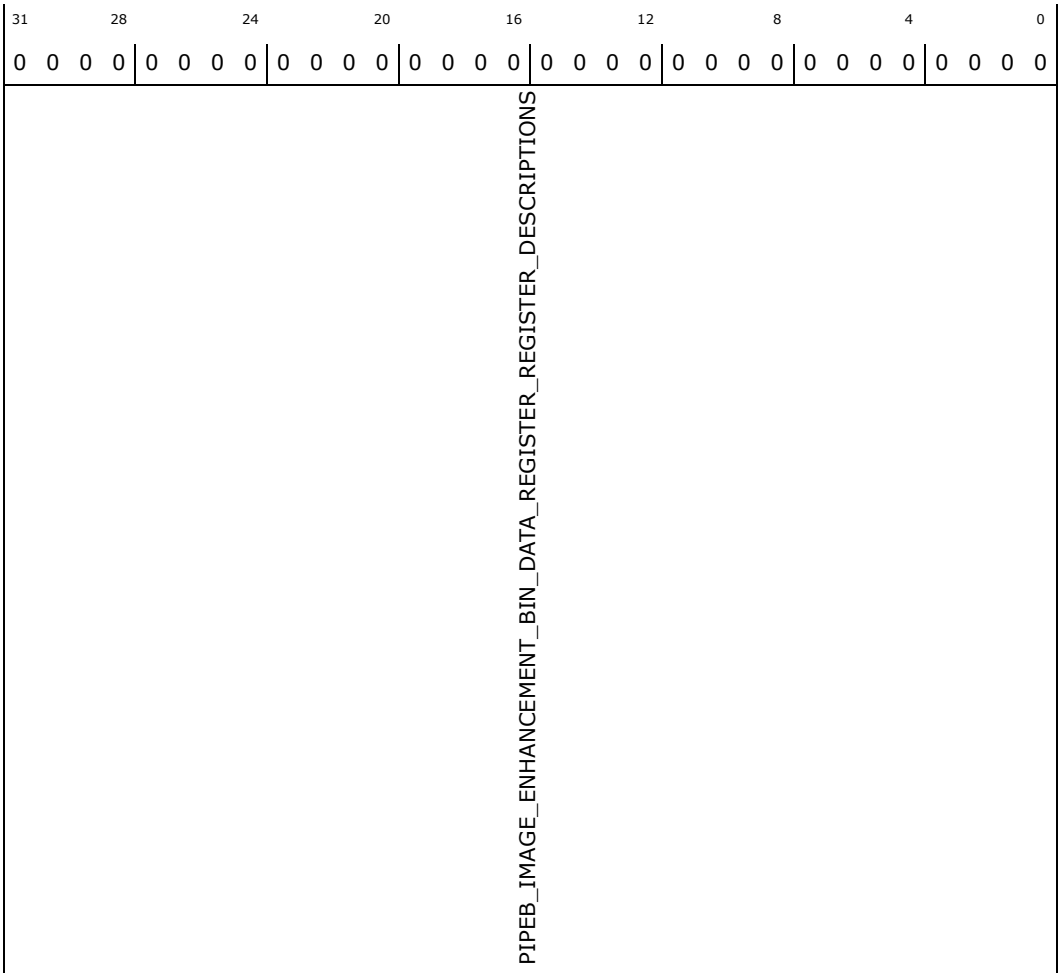
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER: [GTTMMADR_LSB + 2BF20h] + 61364h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER_REGISTER_DESCRIPTIONS:** PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER indexed register descriptions

3.4.62 PIPEBHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61368h

pipe B histogram threshold gurband register

Access Method

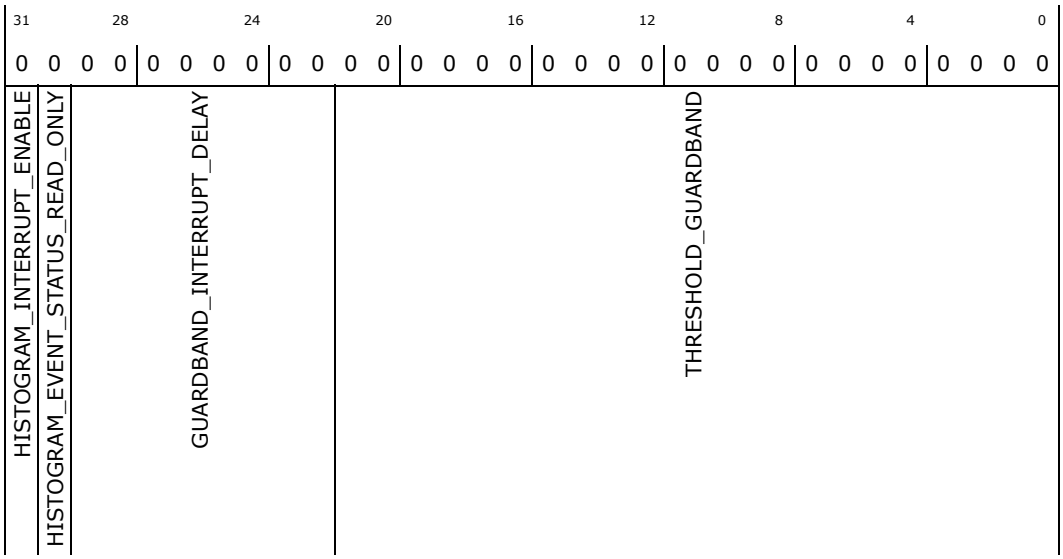
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBHISTOGRAMTHRESHOLDGUARDBANDREGISTER: [GTTMMADR_LSB + 2BF20h] + 61368h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**HISTOGRAM_INTERRUPT_ENABLE:** 0 = Disabled 1 = Enabled. This generates a histogram interrupt once a Histogram event occurs.
30	0b RO	**HISTOGRAM_EVENT_STATUS_READ_ONLY:** When a Histogram event has occurred, this will get set by the hardware. For any more Histogram events to occur, the software needs to clear this bit by writing a '1'. The default state for this bit is '0'. 0 = Histogram event has not occurred. 1 = Histogram event has occurred. AccessType: Read Only
29:22	0b RW	**GUARDBAND_INTERRUPT_DELAY:** An interrupt is generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank. A value of 0 is invalid.
21:0	0b RW	**THRESHOLD_GUARDBAND:** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank

3.4.63 MIPIC_PORT_CTRL—Offset 61700h

mipi C port ctrl

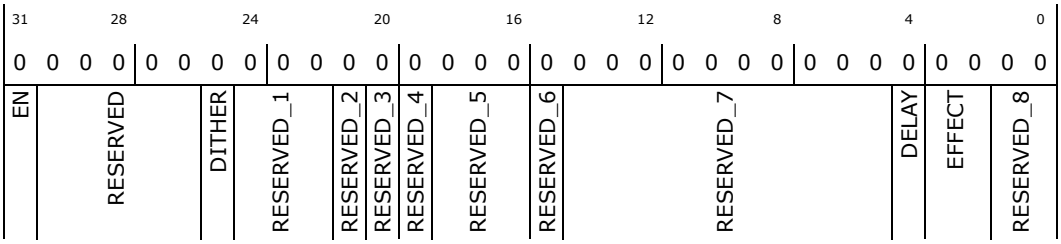
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_PORT_CTRL: [GTTMMADR_LSB + 2BF20h] + 61700h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**EN:** When this bit is disabled the MIPI DPI (video mode) is inactive and in it's low power state. When it is enable it starts to generate timing for this MIPI port 0 = The port is disabled and all MIPI DPI interface are disable (timing generator is off) 1 = The port is enabled
30:26	0b RW	**RESERVED:** Reserved.
25	0b RW	**DITHER:** This bit enables or disables (bypassing) 8-6-bit color dithering function. The usage of this bit would be on for 18-bpp panels and off for 24-bpp panels. 0 = disabled 1 = enabled
24:22	0b RW	**RESERVED_1:** Reserved.
21	0b RW	**RESERVED_2:** Reserved.
20	0b RW	**RESERVED_3:** Reserved.
19	0b RW	**RESERVED_4:** Reserved.
18:16	0b RW	**RESERVED_5:** Reserved.
15	0b RW	**RESERVED_6:** Reserved.
14:5	0b RW	**RESERVED_7:** Reserved.
4	0b RW	**DELAY:** When set, the TE counter will be count down until
3:2	0b RW	**EFFECT:** 00: No tearing effect required - memory write start as soon as write data is available 01: TE trigger by MIPI DPHY and DSI protocol 10: TE trigger by GPIO pin 11: Reserved
1:0	0b RW	**RESERVED_8:** Reserved.

3.4.64 MIPIC_TEARING_CTR—Offset 61704h

mipi C tearing ctr

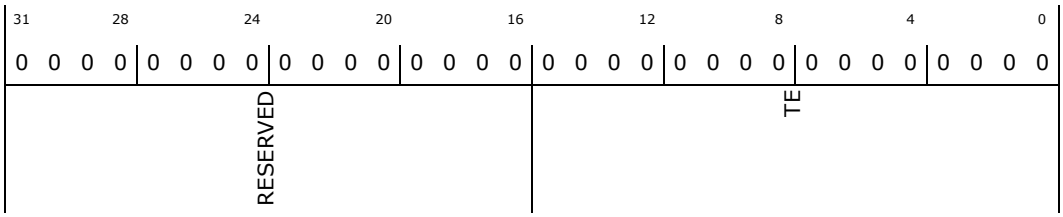
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MIPIC_TEARING_CTR: [GTTMMADR_LSB + 2BF20h] + 61704h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**TE:** Number of delay clocks from TE trigger to start sending data to DSI controller

3.4.65 AUD_CONFIG_A—Offset 62000h

Audio Configuration Pipe A

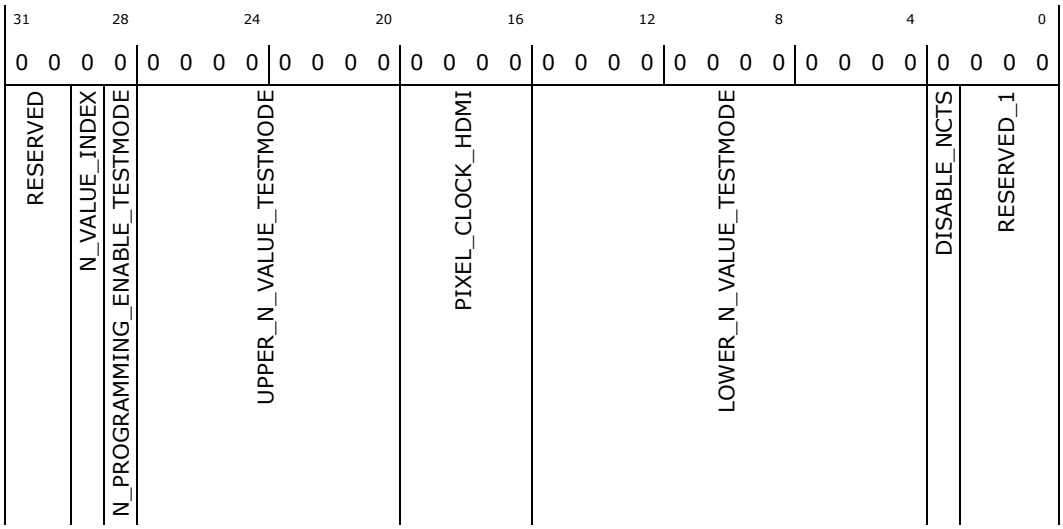
Access Method

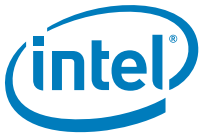
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CONFIG_A: [GTTMMADR_LSB + 2BF20h] + 62000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** Project: All Format:
29	0b RW	**N_VALUE_INDEX:** Project: All Default Value: 0b Value Name Description Project 0b HDMI N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6. All 1b DP N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value default h8000. All
28	0b RW	**N_PROGRAMMING_ENABLE_TESTMODE:** Project: All Security: Test This bit enables programming of N values for non-CEA modes. Please note that the Pipe to which audio is attached must be disabled when changing this field.
27:20	0b RW	**UPPER_N_VALUE_TESTMODE:** Project: All Security: Test These are bits [19:12] of programmable N values for non-CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the Pipe to which audio is attached must be disabled when changing this field. This register can also be used to program N value for DP for a specific Port. Default value on this register when bit 29 is set to 1 is h7FA6
19:16	0b RW	**PIXEL_CLOCK_HDMI:** Project: All Default Value: 0b This is the target frequency of the CEA/HDMI video mode to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DP Link clock. DP Link clock does not require this programming. Note: The Pipe on which audio is attached must be disabled when changing this field. Value Name Description Project 0000b 25.2 / 1.001 MHz 25.2 / 1.001 MHz All 0001b 25.2 MHz 25.2 MHz Program this value for pixel clocks not listed in this field All 0010b 27 MHz 27 MHz All 0011b 27 * 1.001 MHz 27 * 1.001 MHz All 0100b 54 MHz 54 MHz All 0101b 54 * 1.001 MHz 54 * 1.001 MHz All 0110b 74.25 / 1.001 MHz 74.25 / 1.001 MHz All 0111b 74.25 MHz 74.25 MHz All 1000b 148.5 / 1.001 MHz 148.5 / 1.001 MHz All 1001b 148.5 MHz 148.5 MHz All Others Reserved Reserved All
15:4	0b RW	**LOWER_N_VALUE_TESTMODE:** Project: All Security: Test These are bits [11:0] of programmable N values for non-CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the Pipe to which audio is attached must be disabled when changing this field. This register can also be used to program N value for DP for a specific Port. Default value on this register when bit 29 is set to 1 is h7FA6
3	0b RW	**DISABLE_NCTS:** Project: All Set this bit to disable N and CTS or M generation for CTM modes. This is to enable prediction of CRC in CTM modes.
2:0	0b RW	**RESERVED_1:** Project: All Format:

3.4.66 AUD_MISC_CTRL_A—Offset 62010h

Audio MISC Control for Pipe A

Access Method

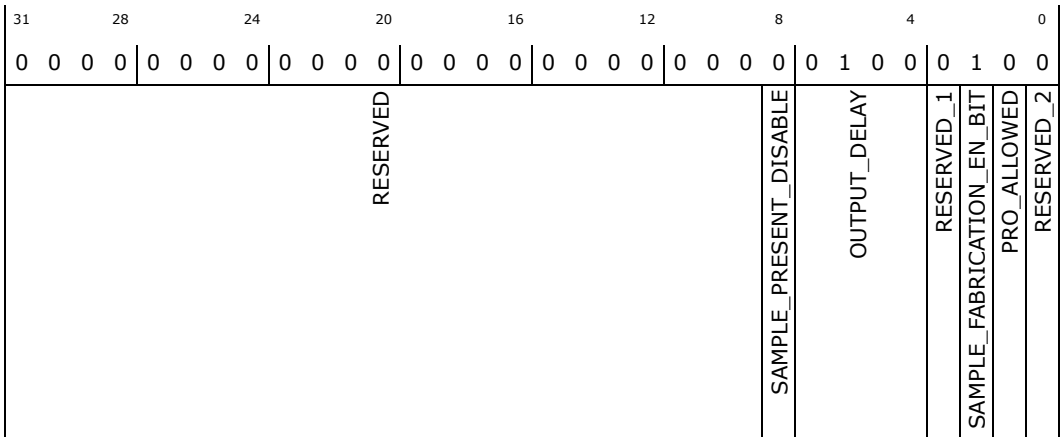
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_MISC_CTRL_A: [GTTMMADR_LSB + 2BF20h] + 62010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000044h



Bit Range	Default & Access	Description
31:9	0b RW	**RESERVED:** Project: All Format: MBZ
8	0b RW	**SAMPLE_PRESENT_DISABLE:** Project: All Security: Debug This bit is used to Disable sample present for HDMI or DP (Chicken Bit)
7:4	0100b RW	**OUTPUT_DELAY:** Project: All Default Value: 0100b The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.
3	0b RW	**RESERVED_1:** Project: All Format: MBZ
2	1b RW	**SAMPLE_FABRICATION_EN_BIT:** Project: All Access: R/W Default Value: ;1b This bit indicates whether internal fabrication of audio samples is enabled during a link underrun. Value Name Description Project 0b Disable Audio fabrication disabled All 1b Enable Audio fabrication enabled All
1	0b RW	**PRO_ALLOWED:** Project: All Access: R/W Default Value: 0b By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode. Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb. Value Name Description Project 0b Consumer Consumer use only All 1b Professional Professional use allowed All
0	0b RW	**RESERVED_2:** All Format: MBZ

3.4.67 AUD_VID_DID—Offset 62020h

Audio Vendor ID / Device ID

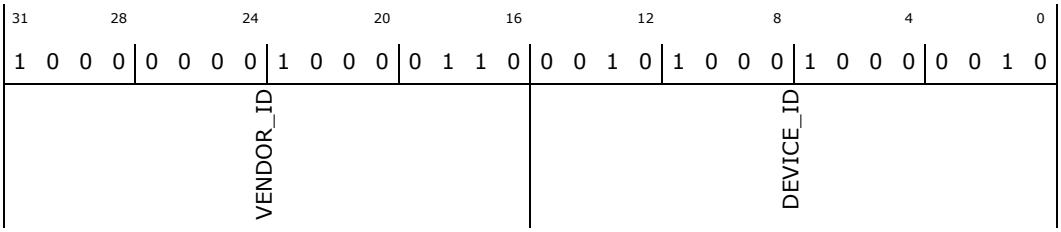
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_VID_DID: [GTTMMADR_LSB + 2BF20h] + 62020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 80862882h



Bit Range	Default & Access	Description
31:16	1000000010000110b RO	**VENDOR_ID:** Project: All Format: U16 Used to identify the codec within the PnP system. This field is hardwired within the device. Value = 0x8086
15:0	0010100010000010b RO	**DEVICE_ID:** Project: All Format: U16 Constant used to identify the codec within the PnP system. This field is set by the device hardware. Value = 0x2882.

3.4.68 AUD_RID—Offset 62024h

Audio Revision ID

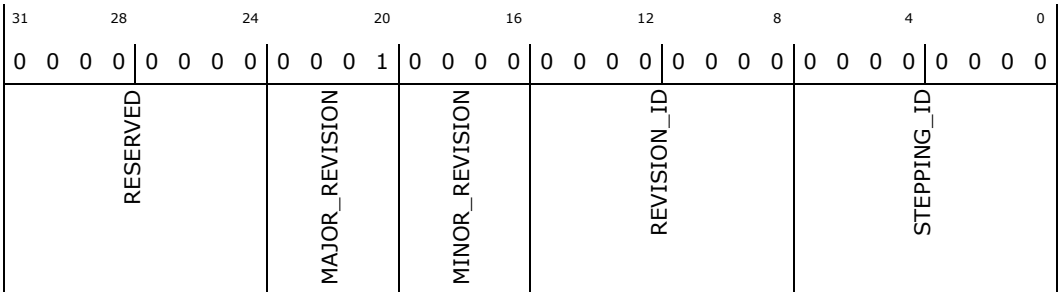
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_RID: [GTTMMADR_LSB + 2BF20h] + 62024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00100000h



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:20	0001b RO	**MAJOR_REVISION:** Project: All Default Value: 0001b The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x1
19:16	0b RO	**MINOR_REVISION:** Project: All The minor revision number (rights of the decimal) or dot number of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x0
15:8	0b RO	**REVISION_ID:** Project: All The vendors revision number for this given Device ID. This field is hardwired within the device. Value = 0x0
7:0	0b RO	**STEPPING_ID:** Project: All An optional vendor stepping number within the given Revision ID. This field is hardwired within the device. Value = 0x0

3.4.69 AUD_CTS_ENABLE_A—Offset 62028h

Audio CTS Programming Enable Pipe A

Access Method

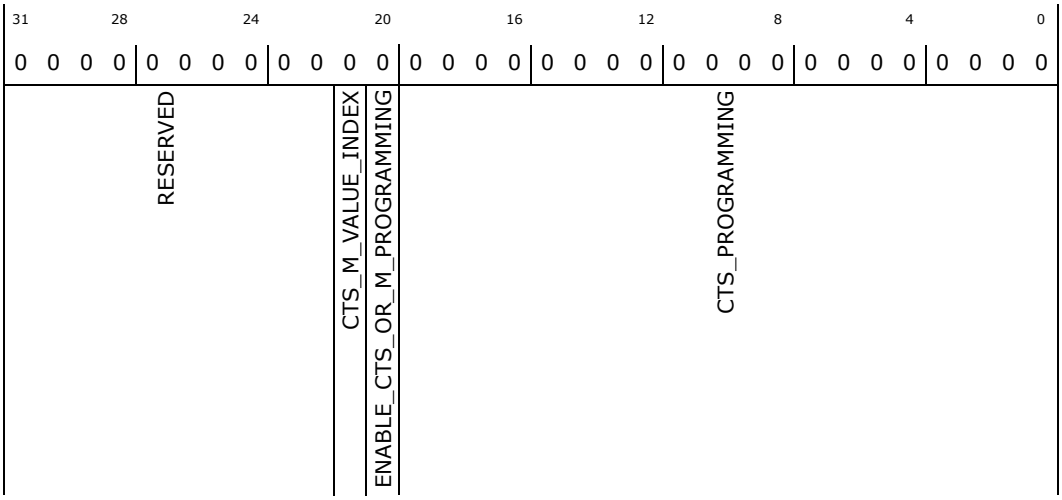
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CTS_ENABLE_A: [GTTMMADR_LSB + 2BF20h] + 62028h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0b RW	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Description
21	0b RW	**CTS_M_VALUE_INDEX:** Project: All Default Value: 0b Value Name Description Project 0b CTS CTS value read on bits 23:4 reflects CTS value. Bit 23:4 is programmable to any CTS value. default is 0 All 1b M M value read on bits 21:4 reflects DP M value. Set this bit to 1 before programming M value register. When this is set to 1 23:4 will reflect the current N value All
20	0b RW	**ENABLE_CTS_OR_M_PROGRAMMING:** Project: All When set will enable CTS or M programming.
19:0	0b RW	**CTS_PROGRAMMING:** Project: All These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the Pipe to which audio is attached must be disabled when changing this field.

3.4.70 AUD_PWRST—Offset 6204Ch

Audio Power State (Function Group, Convertor, Pin Widget)

Access Method

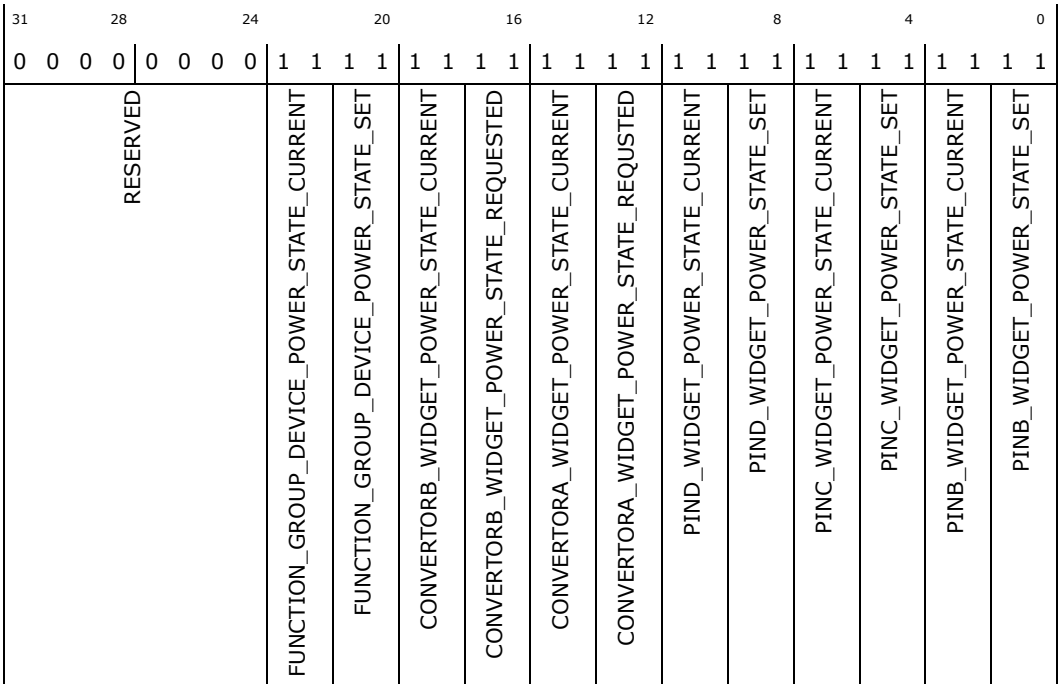
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_PWRST: [GTTMMADR_LSB + 2BF20h] + 6204Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00FFFFFFh



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:22	11b RO	**FUNCTION_GROUP_DEVICE_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
21:20	11b RO	**FUNCTION_GROUP_DEVICE_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
19:18	11b RO	**CONVERTORB_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
17:16	11b RO	**CONVERTORB_WIDGET_POWER_STATE_REQUESTED:** Project: All Format: Audio Power State Format Power state that was requested by audio software Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
15:14	11b RO	**CONVERTORA_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
13:12	11b RO	**CONVERTORA_WIDGET_POWER_STATE_REQUSTED:** Project: All Format: Audio Power State Format Power state that was requested by audio software Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
11:10	11b RO	**PIND_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
9:8	11b RO	**PIND_WIDGET_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
7:6	11b RO	**PINC_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
5:4	11b RO	**PINC_WIDGET_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
3:2	11b RO	**PINB_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Current power state
1:0	11b RO	**PINB_WIDGET_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All

3.4.71 AUD_HDMIW_HDMIEDID_A—Offset 62050h

HDMI Data EDID Block Pipe A

Access Method

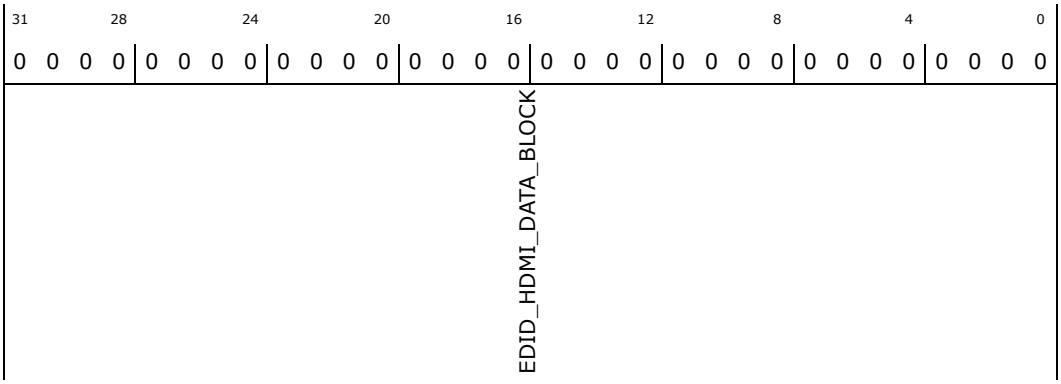
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_HDMIW_HDMIEDID_A: [GTTMMADR_LSB + 2BF20h] + 62050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**EDID_HDMI_DATA_BLOCK:** Project: All Format: Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during gfx reset

3.4.72 AUD_HDMIW_INFOFR_A—Offset 62054h

Audio Widget Data Island Packet Pipe A

Access Method

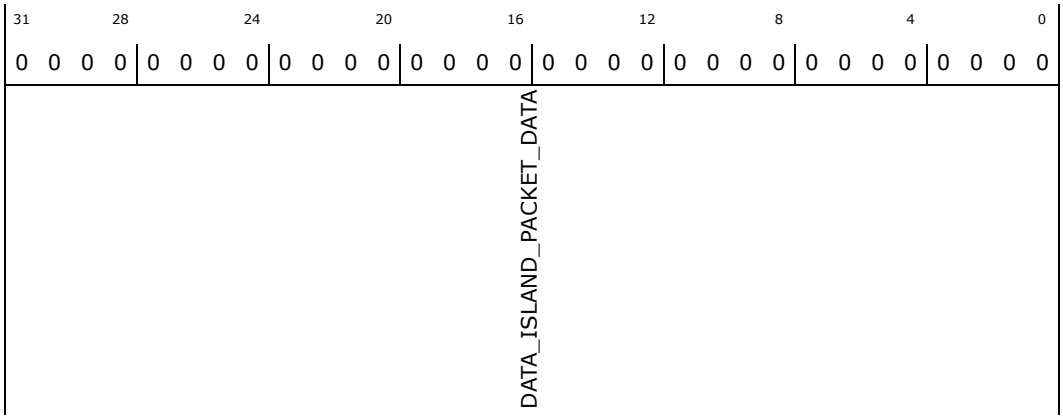
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_HDMIW_INFOFR_A: [GTTMMADR_LSB + 2BF20h] + 62054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**DATA_ISLAND_PACKET_DATA:** Project: All Format: This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

3.4.73 AUD_PORT_EN_HD_CFG—Offset 6207Ch

Audio Port Enable HDAudio Config

Access Method

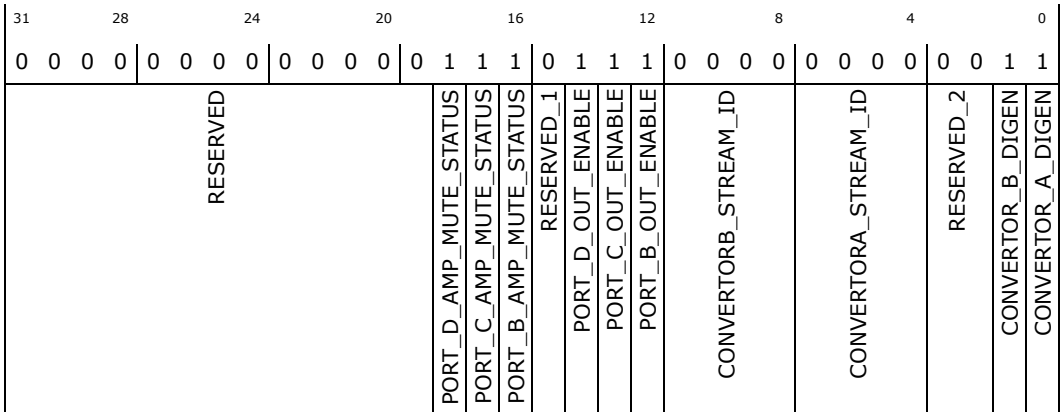
Type: Memory Mapped I/O Register (Size: 32 bits)

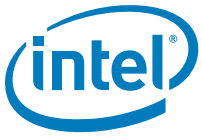
AUD_PORT_EN_HD_CFG: [GTTMMADR_LSB + 2BF20h] + 6207Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00077003h





Bit Range	Default & Access	Description
31:19	0b RO	**RESERVED:** Project: All Format:
18	1b RO	**PORT_D_AMP_MUTE_STATUS:** Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
17	1b RO	**PORT_C_AMP_MUTE_STATUS:** Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
16	1b RO	**PORT_B_AMP_MUTE_STATUS:** Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
15	0b RO	**RESERVED_1:** Project: All Format:
14	1b RO	**PORT_D_OUT_ENABLE:** Project: All Default Value: ;1b Audio is Enabled This bit reflects the state of the output path of the Pin Widget. Value Name Description Project 0b Disable Audio is Disabled All 1b Enable Audio is Enabled All
13	1b RO	**PORT_C_OUT_ENABLE:** Project: All Default Value: ;1b Audio is Enabled This bit reflects the state of the output path of the Pin Widget. Value Name Description Project 0b Disable Audio is Disabled All 1b Enable Audio is Enabled All
12	1b RO	**PORT_B_OUT_ENABLE:** Project: All Default Value: ;1b Audio is Enabled This bit reflects the state of the output path of the Pin Widget. Value Name Description Project 0b Disable Audio is Disabled All 1b Enable Audio is Enabled All
11:8	0b RO	**CONVERTORB_STREAM_ID:** Project: All Format: Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
7:4	0b RO	**CONVERTORA_STREAM_ID:** Project: All Format: Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
3:2	0b RO	**RESERVED_2:** Project: All Format:
1	1b RO	**CONVERTOR_B_DIGEN:** Project: All Default Value: ;1b Digital Transmission Enabled Enables digital transmission through this node. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Block Digital data is blocked from passing through the node, regardless of the state All 1b Pass Digital data can pass through the node (Default) All

Bit Range	Default & Access	Description
0	1b RO	**CONVERTOR_A_DIGEN:** Project: All Default Value: ;1b Digital Transmission Enabled Enables digital transmission through this node. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Block Digital data is blocked from passing through the node, regardless of the state All 1b Pass Digital data can pass through the node (Default) All

3.4.74 AUD_OUT_DIG_CNVT_A—Offset 62080h

Audio Digital Converter Conv A

Access Method

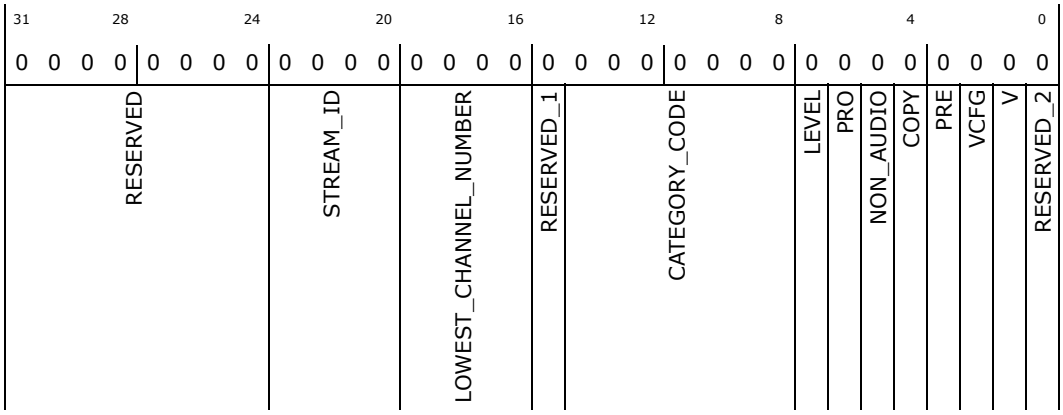
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_DIG_CNVT_A: [GTTMMADR_LSB + 2BF20h] + 62080h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:20	0b RO	**STREAM_ID:** Project: All Format: Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
19:16	0b RO	**LOWEST_CHANNEL_NUMBER:** Project: All Format: Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0
15	0b RO	**RESERVED_1:** Project: All Format:

Bit Range	Default & Access	Description
14:8	0b RO	**CATEGORY_CODE:** Project: All Format: S/PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default = 0
7	0b RO	**LEVEL:** Project: All Format: S/PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
6	0b RO	**PRO:** Project: All Default Value: 0b This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register. Value Name Description Project 0b Consumer Consumer use All 1b Professional Professional use All
5	0b RO	**NON_AUDIO:** Project: All Default Value: 0b Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b PCM Data is PCM All 1b Non PCM Data is non PCM format All
4	0b RO	**COPY:** Project: All Default Value: 0b Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0b RO	**PRE:** Project: All Default Value: 0b Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Disabled Preemphasis is disabled All 1b Enabled Filter preemphasis is enabled All
2	0b RO	**VCFG:** Project: All Format: Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
1	0b RO	**V:** Project: All Format: Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
0	0b RO	**RESERVED_2:** All Format: MBZ

3.4.75 AUD_OUT_STR_DESC_A—Offset 62084h

Audio Stream Descriptor Format Conv A

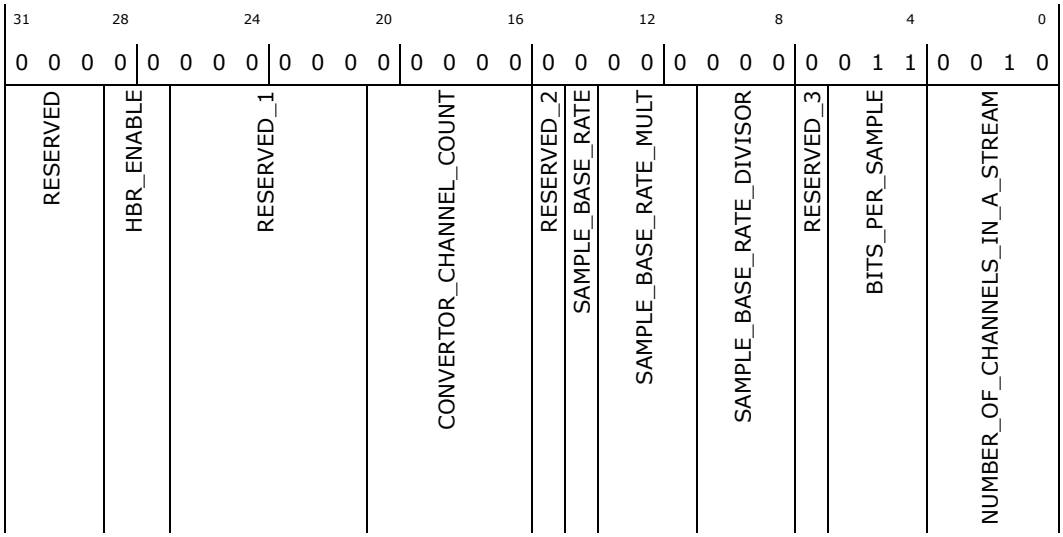
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_STR_DESC_A: [GTTMMADR_LSB + 2BF20h] + 62084h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000032h



Bit Range	Default & Access	Description
31:29	0b RO	**RESERVED:** Project: All Format:
28:27	0b RO	**HBR_ENABLE:** Project: All Format: This reflects the current HBR settings.
26:21	0b RO	**RESERVED_1:** Project: All Format:
20:16	0b RO	**CONVERTOR_CHANNEL_COUNT:** Project: All Format: This reflects the Convertor Channel Count programmed through HDAudio.
15	0b RO	**RESERVED_2:** Project: All Format:
14	0b RO	**SAMPLE_BASE_RATE:** Project: All Default Value: 0b 48 kHz Sampling base rate of audio stream. Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0b RO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: 000b 48 kHz Audio stream sample base rate multiple. Value Name Description Project 000b x1 x1 (48 kHz/44.1 kHz or less) All 001b x2 x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b x3 x3 (144 kHz) All 011b x4 x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved All
10:8	0b RO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: 000b 48 kHz Audio stream sample base rate divisor. Value Name Description Project 000b Div 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Div 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Div 3 Divide by 3 (16 kHz, 32 kHz) All 011b Div 4 Divide by 4 (11.025 kHz) All 100b Div 5 Divide by 5 (9.6 kHz) All 101b Div 6 Divide by 6 (8 kHz) All 110b Div 7 Divide by 7 All 111b Div 8 Divide by 8 (6 kHz) All
7	0b RO	**RESERVED_3:** Project: All Format: MBZ

Bit Range	Default & Access	Description
6:4	011b RO	**BITS_PER_SAMPLE:** Project: All Default Value: 011b 32 bits Value Name Description Project 000b 8 bit The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 100b 20 bits The data will be packed in memory in 20 bit containers on 32 bit boundaries All 010b 24 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All Others Reserved Reserved All
3:0	0010b RO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Default Value: 0010b 3 channels in each frame Format: U4+1 Binary value plus 1. 0000 = 1, 1111= 16 Number of channels in each frame of the stream.

3.4.76 AUD_OUT_CH_STR—Offset 62088h

Audio Channel ID and Stream ID

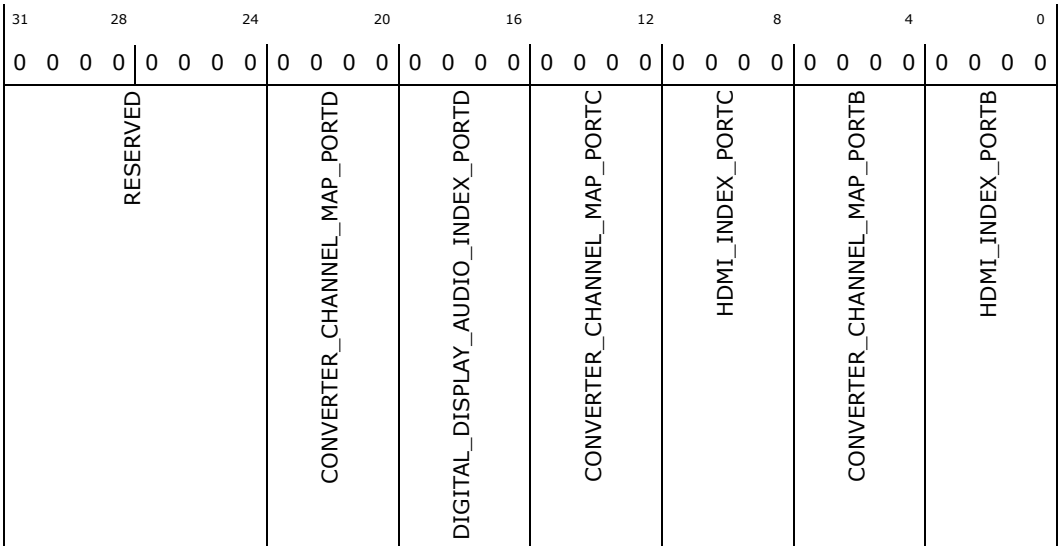
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_CH_STR: [GTTMMADR_LSB + 2BF20h] + 62088h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Description
23:20	0b RO	**CONVERTER_CHANNEL_MAP_PORTD:** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 19:16 is mapped. This field is read only
19:16	0b RO	**DIGITAL_DISPLAY_AUDIO_INDEX_PORTD:** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 20:23 of this register.
15:12	0b RO	**CONVERTER_CHANNEL_MAP_PORTC:** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 11:8 is mapped. This field is read only
11:8	0b RO	**HDMI_INDEX_PORTC:** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 12:15 of this register.
7:4	0b RO	**CONVERTER_CHANNEL_MAP_PORTB:** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 3:0 is mapped. This field is read only
3:0	0b RO	**HDMI_INDEX_PORTB:** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 4:7 of this register.

3.4.77 AUD_PINW_CONNLNG_LIST—Offset 620A8h

Audio Connection List

Access Method

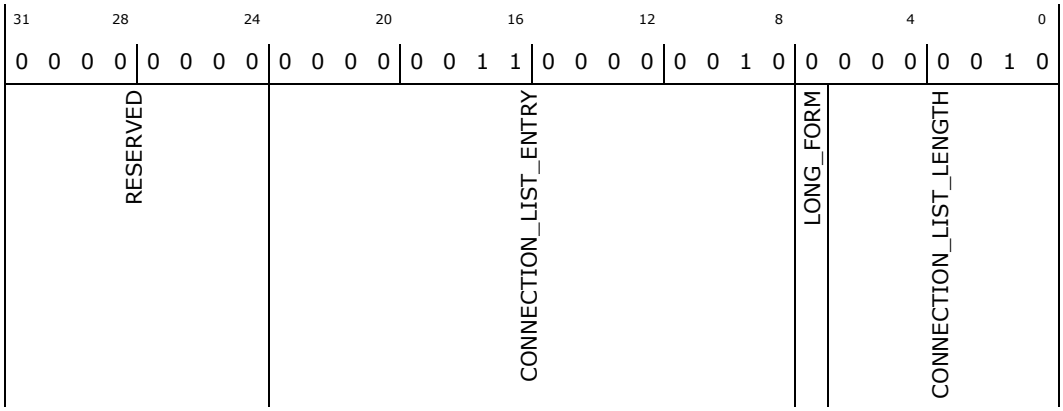
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_PINW_CONNLNG_LIST: [GTTMMADR_LSB + 2BF20h] + 620A8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00030202h



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:8	000000110 0000010b RO	**CONNECTION_LIST_ENTRY:** Project: All Default Value: 0000001100000010b Connection to Convertor Widget Node 0x0302
7	0b RO	**LONG_FORM:** Project: All Default Value: 0b This bit indicates whether the items in the connection list are long form or short form. This bit is hardwired to 0 (items in connection list are short form)
6:0	10b RO	**CONNECTION_LIST_LENGTH:** Project: All Default Value: 02h This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

3.4.78 AUD_PINW_CONNLNG_SEL—Offset 620ACh

Audio Connection Select

Access Method

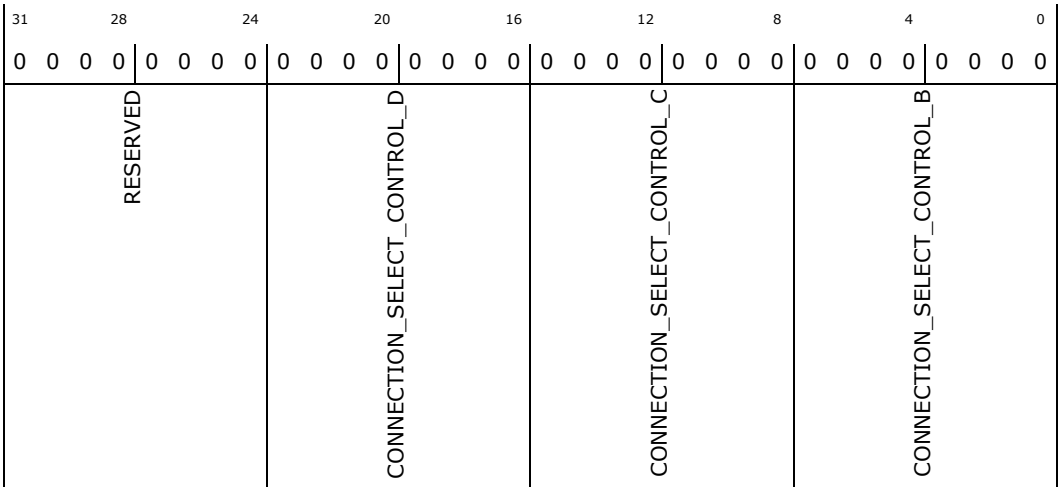
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_PINW_CONNLNG_SEL: [GTTMMADR_LSB + 2BF20h] + 620ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:16	0b RO	**CONNECTION_SELECT_CONTROL_D:** Project: All Format: Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x00

Bit Range	Default & Access	Description
15:8	0b RO	**CONNECTION_SELECT_CONTROL_C:** Project: All Format: Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x00
7:0	0b RO	**CONNECTION_SELECT_CONTROL_B:** Project: All Format: Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00

3.4.79 AUD_CNTL_ST_A—Offset 620B4h

Audio Control State Register Pipe A

Access Method

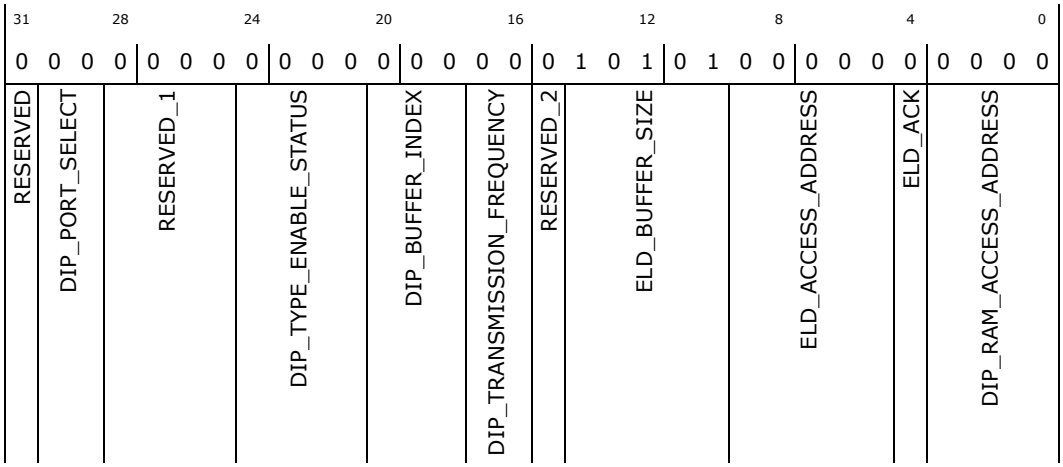
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CNTL_ST_A: [GTTMMADR_LSB + 2BF20h] + 620B4h

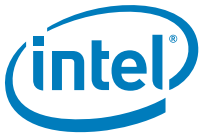
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00005400h



Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:29	0b RO	**DIP_PORT_SELECT:** Project: All AccessType: Read Only Default Value: 00b This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed. Value Name Description Project 00b Reserved Reserved All 01b Digital Port B Digital Port B All 10b Digital Port C Digital Port C All 11b Digital Port D Digital Port D All
28:25	0b RW	**RESERVED_1:** Project: All Format: MBZ



Bit Range	Default & Access	Description
24:21	0b RO	**DIP_TYPE_ENABLE_STATUS:** Project: All AccessType: Read Only Default Value: 0000b These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. Value Name Description Project XXX0b Disable Audio DIP disabled All XXX1b Enable Audio DIP enabled All XX0Xb Disable Generic 1 (ACP) DIP disabled All XX1Xb Enable Generic 1 (ACP) DIP enabled All X0XXb Disable Generic 2 DIP disabled All X1XXb Enable Generic 2 DIP enabled, can be used by ISRC1 or ISRC2 All 1XXXb Reserved Reserved All
20:18	0b RW	**DIP_BUFFER_INDEX:** Project: All Default Value: 0000b This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0s. Value Name Description Project 000b Audio Audio DIP (31 bytes of address space, 31 bytes of data) All 001b Gen 1 Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data) All 010b Gen 2 Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) All 011b Gen 3 Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) All 1XXb Reserved Reserved All
17:16	0b RO	**DIP_TRANSMISSION_FREQUENCY:** Project: All AccessType: Read Only Default Value: 00b These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written. When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. Value Name Description Project 00b Disable Disabled All 01b Reserved Reserved All 10b Send Once Send Once All 11b Best Effort Best effort (Send at least every other vsync) All
15	0b RW	**RESERVED_2:** Project: All Format: MBZ
14:10	10101b RO	**ELD_BUFFER_SIZE:** Project: All AccessType: Read only 10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)
9:5	0b RW	**ELD_ACCESS_ADDRESS:** Project: All Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.
4	0b RO	**ELD_ACK:** Project: All AccessType: Read Only Acknowledgement from the audio driver that ELD read has been completed
3:0	0b RO	**DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read Only Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

3.4.80 AUD_CNTL_ST2—Offset 620C0h

Audio Control State 2

Access Method

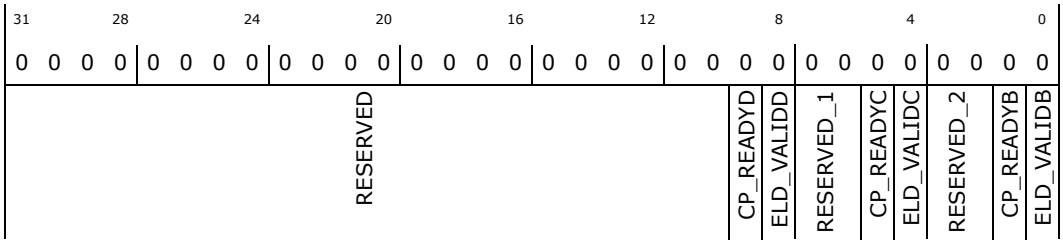
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CNTL_ST2: [GTTMMADR_LSB + 2BF20h] + 620C0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0b RW	**RESERVED:** Project: All Format:
9	0b RW	**CP_READYD:** Project: All Default Value: 0b This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. Value Name Description Project 0b Pending or Not Ready CP request pending or not ready to receive requests All 1b Ready CP request ready All
8	0b RW	**ELD_VALIDD:** Project: All Default Value: 0b This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. Value Name Description Project 0b Invalid ELD data invalid (default, when writing ELD data, set 0 by software) All 1b Valid ELD data valid (Set by video software only) All
7:6	0b RW	**RESERVED_1:** Project: All Format:
5	0b RW	**CP_READYC:** Project: All Default Value: 0b See CP_ReadyD description. Value Name Description Project 0b Not Ready CP request pending or not ready to receive requests All 1b Ready CP request ready All
4	0b RW	**ELD_VALIDC:** Project: All Default Value: 0b See ELD_validD description. Value Name Description Project 0b Invalid ELD data invalid (default, when writing ELD data, set 0 by software) All 1b Valid ELD data valid (Set by video software only) All
3:2	0b RW	**RESERVED_2:** Project: All Format:
1	0b RW	**CP_READYB:** Project: All Default Value: 0b See CP_ReadyD description. Value Name Description Project 0b Not Ready CP request pending or not ready to receive requests All 1b Ready CP request ready All
0	0b RW	**ELD_VALIDB:** Project: All Default Value: 0b See ELD_validD description. Value Name Description Project 0b Invalid ELD data invalid (default, when writing ELD data, set 0 by software) All 1b Valid ELD data valid (Set by video software only) All

3.4.81 AUD_HDMIW_STATUS—Offset 620D4h

Audio HDMI Status

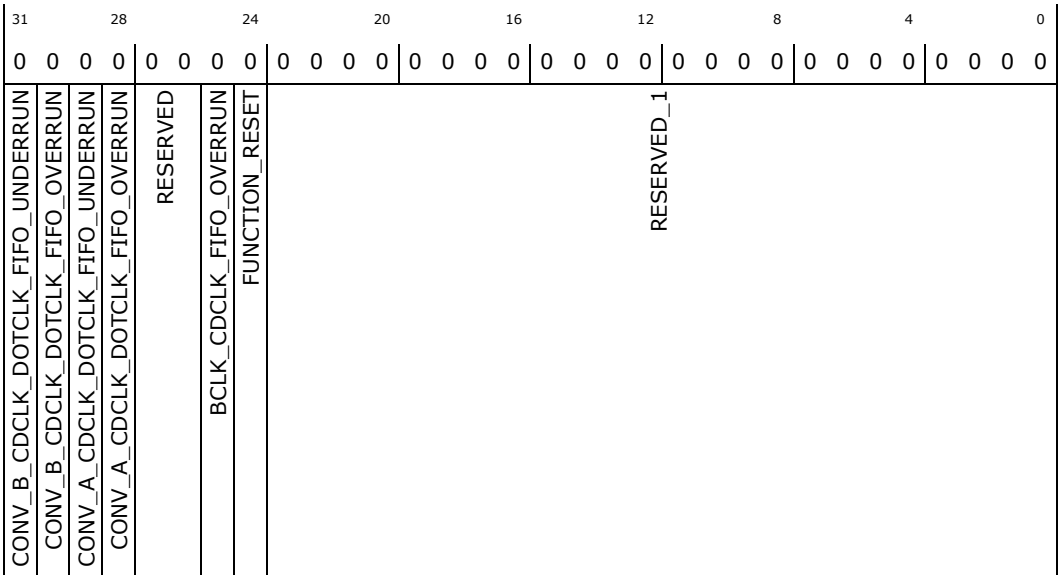
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_HDMIW_STATUS: [GTTMMADR_LSB + 2BF20h] + 620D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**CONV_B_CDCLK_DOTCLK_FIFO_UNDERRUN:** Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
30	0b RW	**CONV_B_CDCLK_DOTCLK_FIFO_OVERRUN:** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
29	0b RW	**CONV_A_CDCLK_DOTCLK_FIFO_UNDERRUN:** Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
28	0b RW	**CONV_A_CDCLK_DOTCLK_FIFO_OVERRUN:** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
27:26	0b RW	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Description
25	0b RW	**BCLK_CDCLK_FIFO_OVERRUN:** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between BCLK and CDCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
24	0b RW	**FUNCTION_RESET:** Project: All Security: Debug This bit indicates that an audio function reset occurred through the reset signal on the HD audio bus. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
23:0	0b RW	**RESERVED_1:** Project: All Format:

3.4.82 AUD_CONFIG_B—Offset 62100h

Audio Configuration Pipe B

Access Method

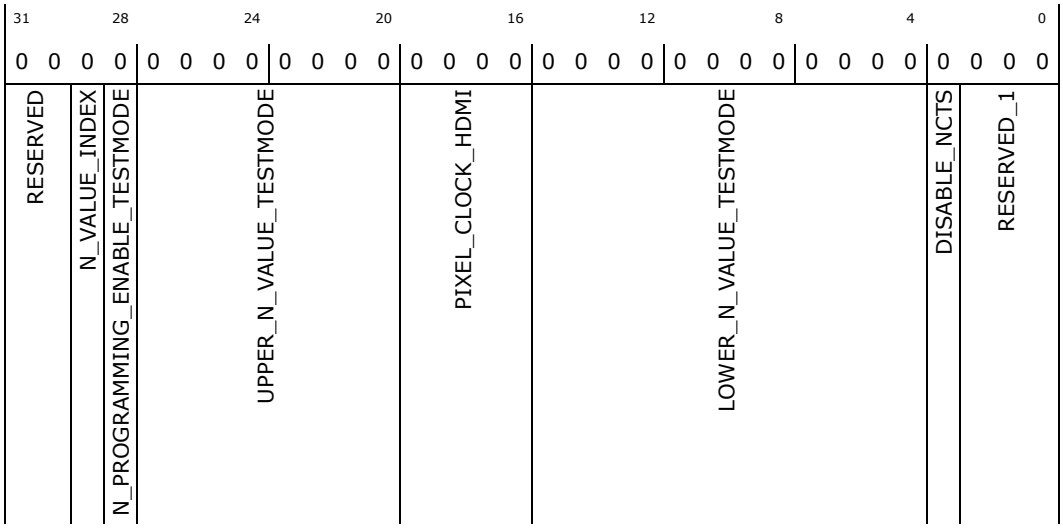
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CONFIG_B: [GTTMMADR_LSB + 2BF20h] + 62100h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Description
29	0b RW	**N_VALUE_INDEX:** Project: All Default Value: 0b Value Name Description Project 0b HDMI N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6. All 1b DP N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value default h8000. All
28	0b RW	**N_PROGRAMMING_ENABLE_TESTMODE:** Project: All Security: Test See Pipe A description.
27:20	0b RW	**UPPER_N_VALUE_TESTMODE:** Project: All Security: Test See Pipe A description
19:16	0b RW	**PIXEL_CLOCK_HDMI:** Project: All Default Value: 0b See Pipe A description. Value Name Description Project 0000b 25.2 / 1.001 MHz 25.2 / 1.001 MHz All 0001b 25.2 MHz 25.2 MHz Program this value for pixel clocks not listed in this field All 0010b 27 MHz 27 MHz All 0011b 27 * 1.001 MHz 27 * 1.001 MHz All 0100b 54 MHz 54 MHz All 0101b 54 * 1.001 MHz 54 * 1.001 MHz All 0110b 74.25 / 1.001 MHz 74.25 / 1.001 MHz All 0111b 74.25 MHz 74.25 MHz All 1000b 148.5 / 1.001 MHz 148.5 / 1.001 MHz All 1001b 148.5 MHz 148.5 MHz All others Reserved Reserved All
15:4	0b RW	**LOWER_N_VALUE_TESTMODE:** Project: All Security: Test See Pipe A description
3	0b RW	**DISABLE_NCTS:** Project: All See Pipe A description
2:0	0b RW	**RESERVED_1:** Project: All Format:

3.4.83 AUD_MISC_CTRL_B—Offset 62110h

Audio MISC Control for Pipe B

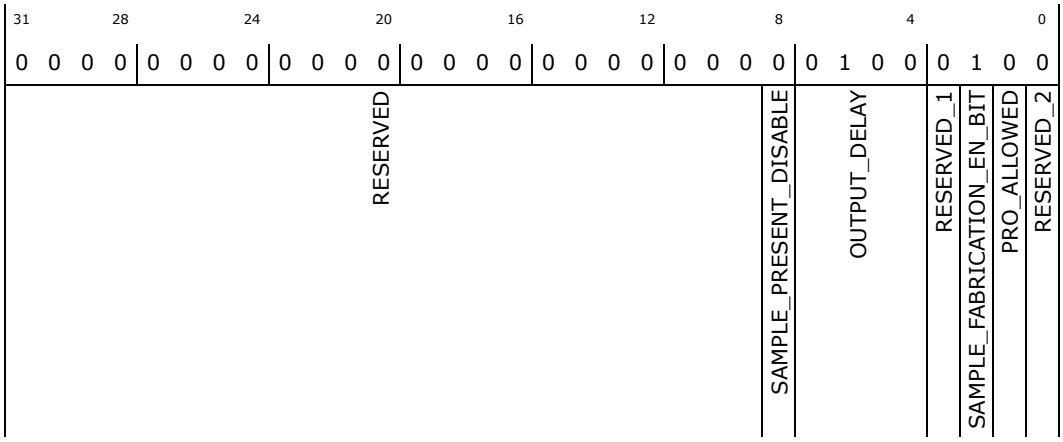
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_MISC_CTRL_B: [GTTMMADR_LSB + 2BF20h] + 62110h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000044h



Bit Range	Default & Access	Description
31:9	0b RW	**RESERVED:** Project: All Format: MBZ
8	0b RW	**SAMPLE_PRESENT_DISABLE:** Project: All Security: Debug See Pipe A description
7:4	0100b RW	**OUTPUT_DELAY:** Project: All Default Value: 0100b See Pipe A description.
3	0b RW	**RESERVED_1:** Project: All Format: MBZ
2	1b RW	**SAMPLE_FABRICATION_EN_BIT:** Project: All Access: R/W Default Value: ;1b See Pipe A description. Value Name Description Project 0b Disable Audio fabrication disabled All 1b Enable Audio fabrication enabled All
1	0b RW	**PRO_ALLOWED:** Project: All Access: R/W Default Value: 0b See Pipe A description. Value Name Description Project 0b Consumer Consumer use only All 1b Professional Professional use allowed All
0	0b RW	**RESERVED_2:** All Format: MBZ

3.4.84 AUD_CTS_ENABLE_B—Offset 62128h

Audio CTS Programming Enable Pipe B

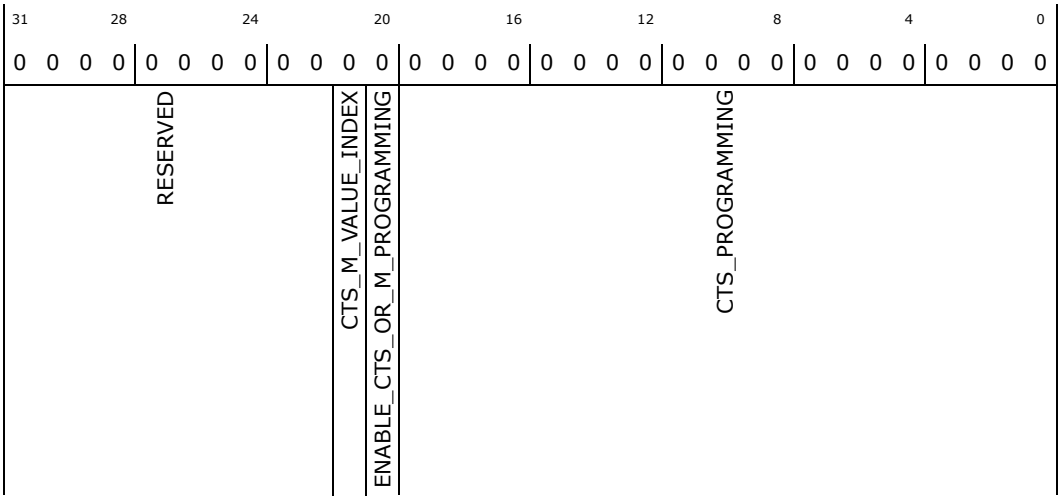
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CTS_ENABLE_B: [GTTMMADR_LSB + 2BF20h] + 62128h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0b RW	**RESERVED:** Project: All Format:
21	0b RW	**CTS_M_VALUE_INDEX:** Project: All Default Value: 0b Value Name Description Project 0b CTS CTS value read on bits 23:4 reflects CTS value. Bit 23:4 is programmable to any CTS value. default is 0 All 1b M M value read on bits 21:4 reflects DP M value. Set this bit to 1 before programming M value register. When this is set to 1 23:4 will reflect the current N value All
20	0b RW	**ENABLE_CTS_OR_M_PROGRAMMING:** Project: All See Pipe A description.
19:0	0b RW	**CTS_PROGRAMMING:** Project: All See Pipe A description.

3.4.85 AUD_HDMIW_HDMIEDID_B—Offset 62150h

HDMI Data EDID Block Pipe B

Access Method

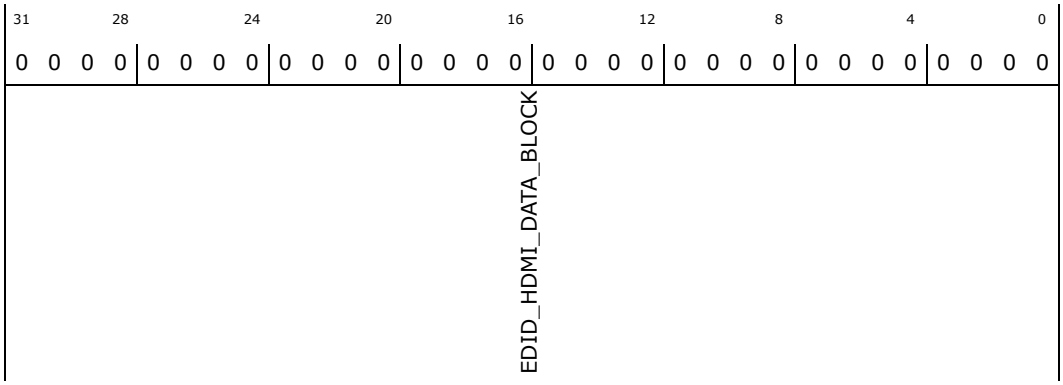
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_HDMIW_HDMIEDID_B: [GTTMMADR_LSB + 2BF20h] + 62150h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**EDID_HDMI_DATA_BLOCK:** Project: All Format: See Pipe A description

3.4.86 AUD_HDMIW_INFOFR_B—Offset 62154h

Audio Widget Data Island Packet Pipe B

Access Method

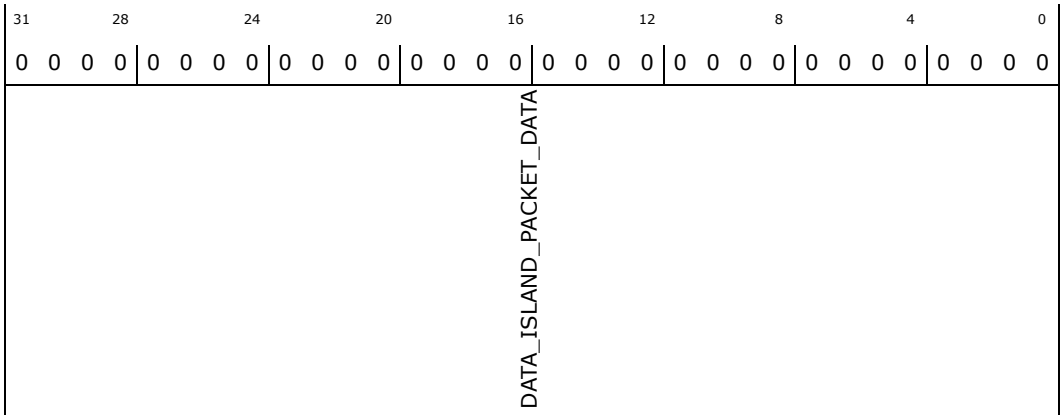
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_HDMIW_INFOFR_B: [GTTMMADR_LSB + 2BF20h] + 62154h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**DATA_ISLAND_PACKET_DATA:** Project: All Format: See Pipe A description.

3.4.87 AUD_OUT_DIG_CNVT_B—Offset 62180h

Audio Digital Converter Conv B

Access Method

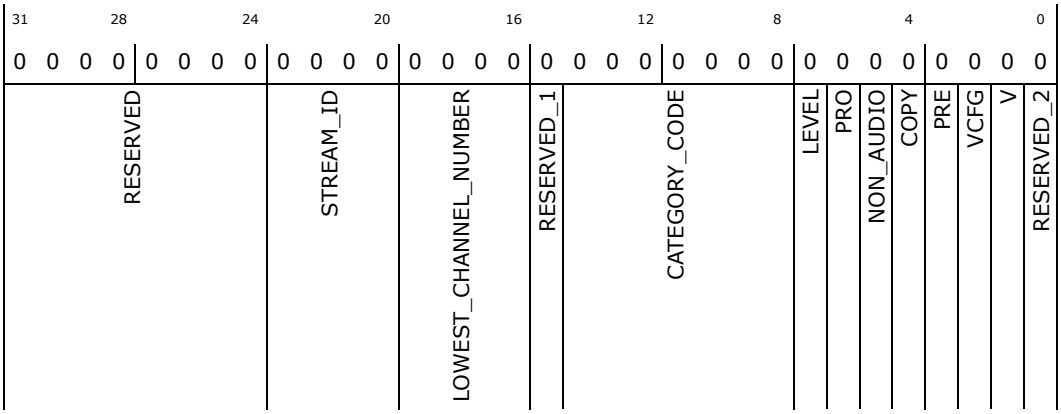
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_DIG_CNVT_B: [GTTMMADR_LSB + 2BF20h] + 62180h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:20	0b RO	**STREAM_ID:** Project: All Format: See Conv A description.
19:16	0b RO	**LOWEST_CHANNEL_NUMBER:** Project: All Format: See Conv A description
15	0b RO	**RESERVED_1:** Project: All Format:
14:8	0b RO	**CATEGORY_CODE:** Project: All Format: See Conv A description
7	0b RO	**LEVEL:** Project: All Format: See Conv A description
6	0b RO	**PRO:** Project: All Default Value: 0b See Conv A description Value Name Description Project 0b Consumer Consumer use All 1b Professional Professional use All
5	0b RO	**NON_AUDIO:** Project: All Default Value: 0b See Conv A description. Value Name Description Project 0b PCM Data is PCM All 1b Non PCM Data is non PCM format All
4	0b RO	**COPY:** Project: All Default Value: 0b See Conv A description Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All

Bit Range	Default & Access	Description
3	0b RO	**PRE:** Project: All Default Value: 0b See Conv A description Value Name Description Project 0b Disabled Preemphasis is disabled All 1b Enabled Filter preemphasis is enabled All
2	0b RO	**VCFG:** Project: All Format: See Conv A description
1	0b RO	**V:** Project: All Format: See Conv A description
0	0b RO	**RESERVED_2:** All Format: MBZ

3.4.88 AUD_OUT_STR_DESC_B—Offset 62184h

Audio Stream Descriptor Format Conv B

Access Method

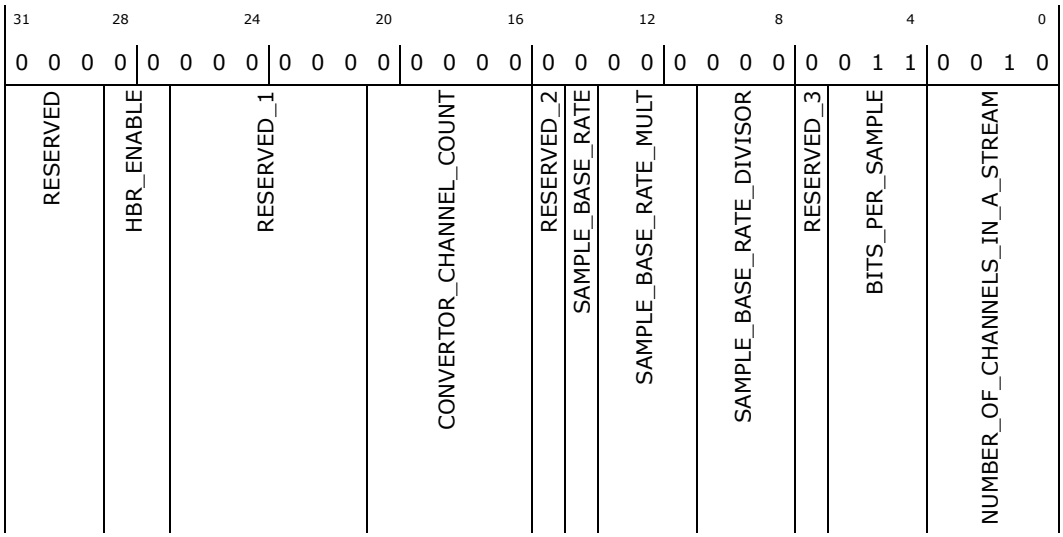
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_STR_DESC_B: [GTTMMADR_LSB + 2BF20h] + 62184h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000032h



Bit Range	Default & Access	Description
31:29	0b RO	**RESERVED:** Project: All Format:
28:27	0b RO	**HBR_ENABLE:** Project: All Format: See Conv A description.

Bit Range	Default & Access	Description
26:21	0b RO	**RESERVED_1:** Project: All Format:
20:16	0b RO	**CONVERTOR_CHANNEL_COUNT:** Project: All Format: See Conv A description.
15	0b RO	**RESERVED_2:** Project: All Format:
14	0b RO	**SAMPLE_BASE_RATE:** Project: All Default Value: 0b 48 kHz See Conv A description. Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0b RO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: 000b 48 kHz See Conv A description. Value Name Description Project 000b x1 x1 (48 kHz/44.1 kHz or less) All 001b x2 x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b x3 x3 (144 kHz) All 011b x4 x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved All
10:8	0b RO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: 000b 48 kHz See Conv A description. Value Name Description Project 000b Div 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Div 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Div 3 Divide by 3 (16 kHz, 32 kHz) All 011b Div 4 Divide by 4 (11.025 kHz) All 100b Div 5 Divide by 5 (9.6 kHz) All 101b Div 6 Divide by 6 (8 kHz) All 110b Div 7 Divide by 7 All 111b Div 8 Divide by 8 (6 kHz) All
7	0b RO	**RESERVED_3:** Project: All Format: MBZ
6:4	011b RO	**BITS_PER_SAMPLE:** Project: All Default Value: 011b 32 bits Value Name Description Project 000b 8 bit The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 100b 20 bits The data will be packed in memory in 20 bit containers on 32 bit boundaries All 010b 24 bits The data will be packed in memory in 24 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All others Res. Reserved All
3:0	0010b RO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Default Value: 0010b 3 channels in each frame Format: U4+1 Binary value plus 1. 0000 = 1, 1111= 16 See Conv A description.

3.4.89 AUD_CNTL_ST_B—Offset 621B4h

Audio Control State Register Pipe B

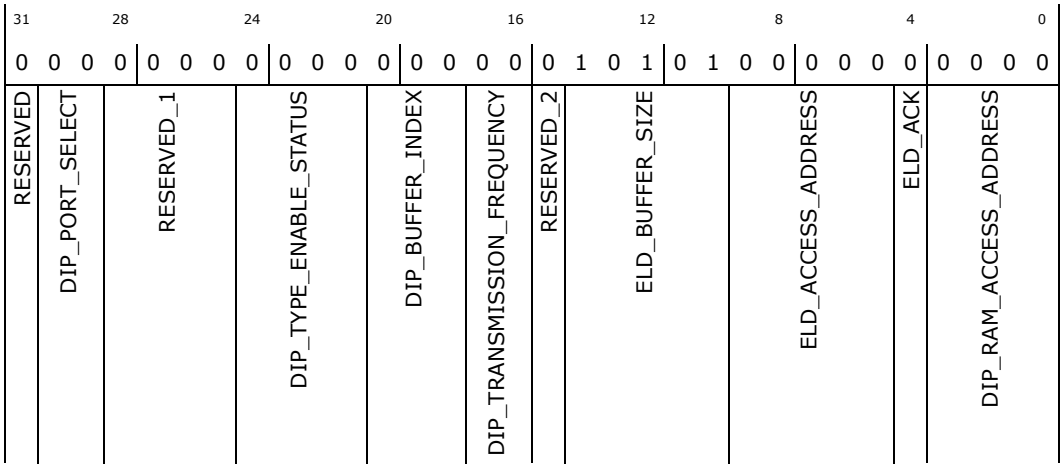
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CNTL_ST_B: [GTTMMADR_LSB + 2BF20h] + 621B4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00005400h



Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:29	0b RO	**DIP_PORT_SELECT:** Project: All AccessType: Read Only Default Value: 00b See Pipe A description. Value Name Description Project 00b Reserved Reserved All 01b Digital Port B Digital Port B All 10b Digital Port C Digital Port C All 11b Digital Port D Digital Port D All
28:25	0b RW	**RESERVED_1:** Project: All Format: MBZ
24:21	0b RO	**DIP_TYPE_ENABLE_STATUS:** Project: All AccessType: Read Only Default Value: 0000b See Pipe A description. Value Name Description Project XXX0b Disable Audio DIP disabled (Default) All XXX1b Enable Audio DIP enabled All XX0Xb Disable Generic 1 (ACP) DIP disabled All XX1Xb Enable Generic 1 (ACP) DIP enabled All X0XXb Disable Generic 2 DIP disabled All X1XXb Enable Generic 2 DIP enabled, can be used by ISRC1 or ISRC2 All 1XXXb Reserved Reserved All
20:18	0b RW	**DIP_BUFFER_INDEX:** Project: All Default Value: 000b See Pipe A description. Value Name Description Project 000b Audio Audio DIP (31 bytes of address space, 31 bytes of data) All 001b Gen 1 Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) All 010b Gen 2 Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) All 011b Gen 3 Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) All 1XXb Reserved Reserved All
17:16	0b RO	**DIP_TRANSMISSION_FREQUENCY:** Project: All AccessType: Read Only Default Value: 00b See Pipe A description Value Name Description Project 00b Disable Disabled All 01b Reserved Reserved All 10b Send Once Send Once All 11b Best Effort Best effort (Send at least every other vsync) All
15	0b RW	**RESERVED_2:** Project: All Format: MBZ
14:10	10101b RO	**ELD_BUFFER_SIZE:** Project: All AccessType: Read Only 10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)
9:5	0b RW	**ELD_ACCESS_ADDRESS:** Project: All See Pipe A description.

Bit Range	Default & Access	Description
4	0b RO	**ELD_ACK:** Project: All AccessType: Read Only See Pipe A description.
3:0	0b RO	**DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read only See Pipe A description.

3.4.90 AUD_SSID_DBG—Offset 62F00h

audio SSID debug

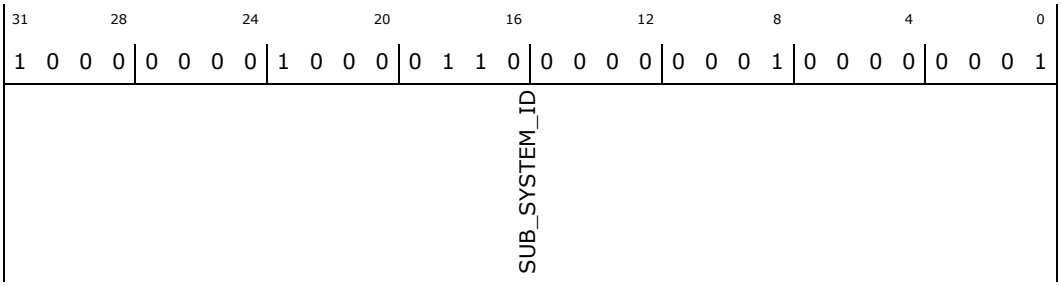
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_SSID_DBG: [GTTMMADR_LSB + 2BF20h] + 62F00h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 80860101h



Bit Range	Default & Access	Description
31:0	10000000100001100000001000000001b WO	**SUB_SYSTEM_ID:** Project: All

3.4.91 AUD_PWST1_DBG—Offset 62F04h

audio pwst1 debug

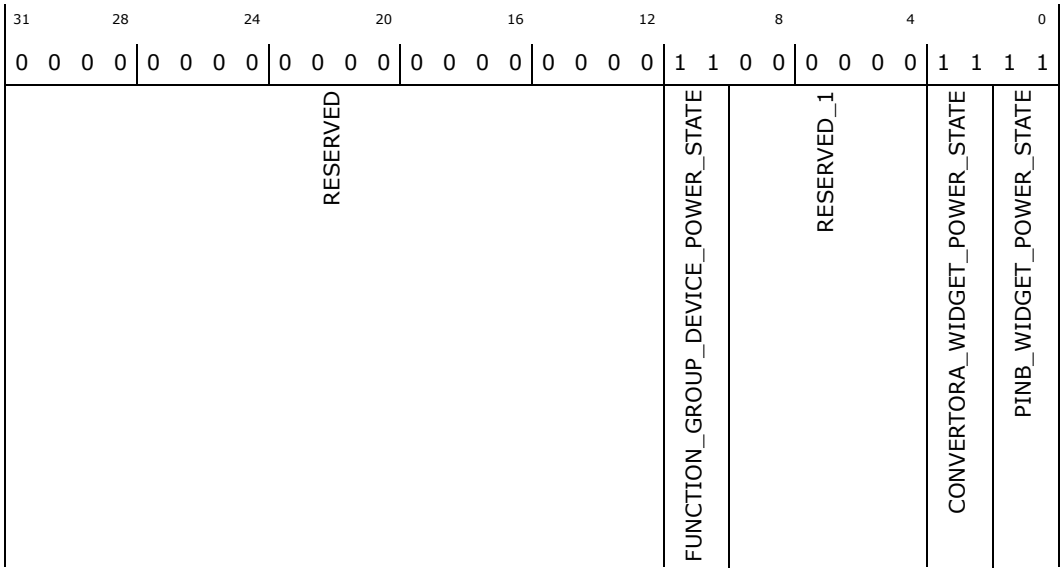
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_PWST1_DBG: [GTTMMADR_LSB + 2BF20h] + 62F04h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000C0Fh



Bit Range	Default & Access	Description
31:12	0b WO	**RESERVED:** Project: All Format: MBZ
11:10	11b WO	**FUNCTION_GROUP_DEVICE_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)
9:4	0b WO	**RESERVED_1:** Project: All Format: MBZ
3:2	11b WO	**CONVERTORA_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was requested by audio software Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)
1:0	11b WO	**PINB_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)

3.4.92 AUD_OUT_STR_DESC_A_DBG—Offset 62F08h

These values are returned from the device as the Stream Descriptor Format response to a Get Audio Output Converter Widget command.

Access Method

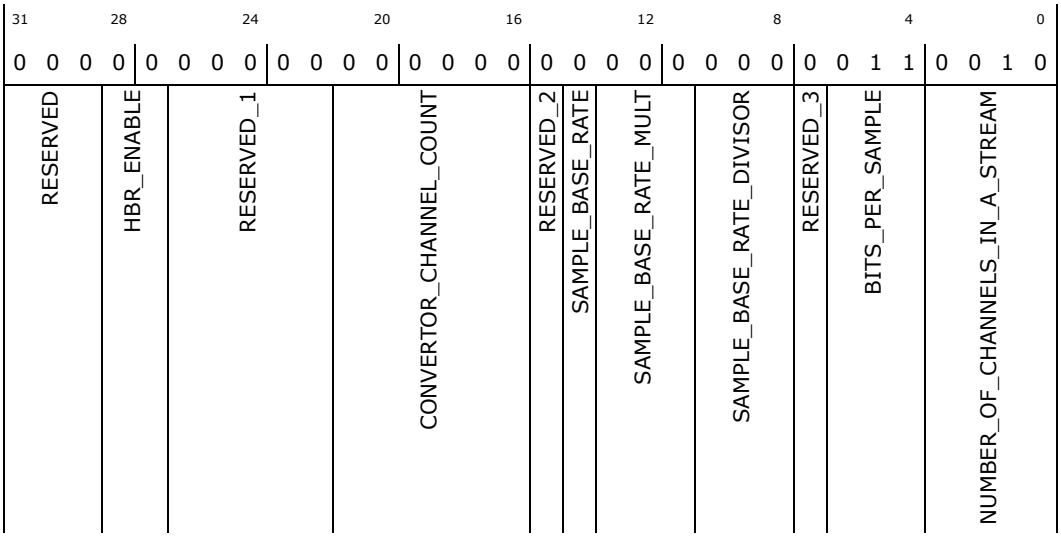
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_STR_DESC_A_DBG: [GTTMMADR_LSB + 2BF20h] + 62F08h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000032h



Bit Range	Default & Access	Description
31:29	0b WO	**RESERVED:** Project: All Format: MBZ
28:27	0b WO	**HBR_ENABLE:** Project: All This reflects the current HBR settings
26:22	0b WO	**RESERVED_1:** Project: All Format: MBZ
21:16	0b WO	**CONVERTOR_CHANNEL_COUNT:** Project: All This reflects the Convertor Channel Count programmed through HDAudio.
15	0b WO	**RESERVED_2:** Project: All Format: MBZ
14	0b WO	**SAMPLE_BASE_RATE:** Project: All Default Value: 0b (48 KHz) Sampling base rate of audio stream Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0b WO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: 000b (48 KHz) Audio stream sample base rate multiple Value Name Description Project 000b 1x 48 kHz/44.1 kHz or less All 001b 2x x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b 3x x3 (144 kHz) All 011b 4x x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved
10:8	0b WO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: 000b (indicates divide by 1 which results in 48 KHz) Audio stream sample base rate divisor Value Name Description Project 000b Divide by 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Divide by 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Divide by 3 Divide by 3 (16 kHz, 32 kHz) All 011b Divide by 4 Divide by 4 (11.025 kHz) All 100b Divide by 5 Divide by 5 (9.6 kHz) All 101b Divide by 6 Divide by 6 (8 kHz) All 110b Divide by 7 Divide by 7 All 111b Divide by Divide by 8 (6 kHz) All
7	0b WO	**RESERVED_3:** Project: All Format: MBZ

Bit Range	Default & Access	Description
6:4	011b WO	**BITS_PER_SAMPLE:** Project: All Default Value: 011b (Indicates 24 bits) Audio stream sample base rate multiple Value Name Description Project 000b 8 bits The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 010b 24 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 100b 20 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All Others Reserved Reserved
3:0	0010b WO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Format: U4+1 Default Value: 0010b (3 channels in each frame) Number of channels in each frame of the stream

3.4.93 AUD_OUT_DIG_CNVT_A_DBG—Offset 62F0Ch

These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Access Method

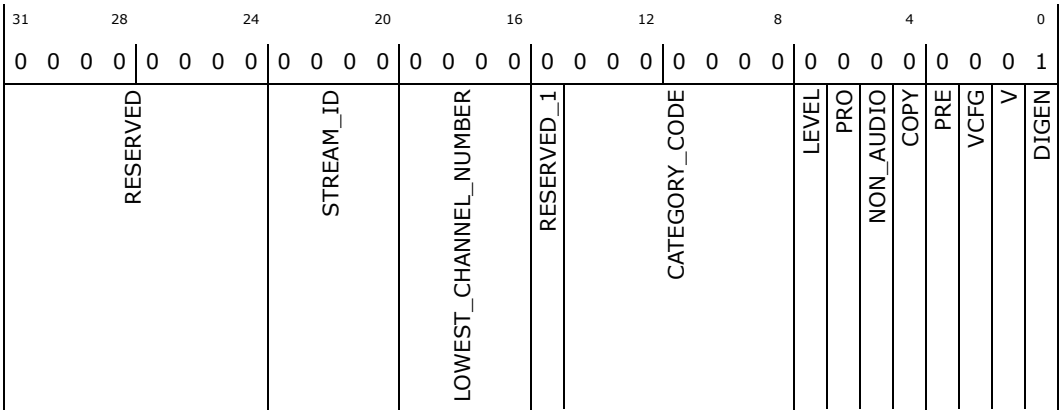
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_DIG_CNVT_A_DBG: [GTTMMADR_LSB + 2BF20h] + 62F0Ch

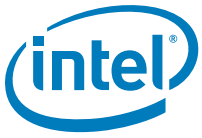
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:24	0b WO	**RESERVED:** Project: All Format: MBZ
23:20	0b WO	**STREAM_ID:** Project: All Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)



Bit Range	Default & Access	Description
19:16	0b WO	**LOWEST_CHANNEL_NUMBER:** Project: All Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0
15	0b WO	**RESERVED_1:** Project: All Format: MBZ
14:8	0b WO	**CATEGORY_CODE:** Project: All S/PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default = 0
7	0b WO	**LEVEL:** Project: All S/PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
6	0b WO	**PRO:** Project: All This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register. Value Name Description Project 0b Consumer Consumer use. Default (Consumer) All 1b Professional Professional use All
5	0b WO	**NON_AUDIO:** Project: All Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b PCM Data is PCM (Default) All 1b Non-PCM Data is non PCM format All
4	0b WO	**COPY:** Project: All Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0b WO	**PRE:** Project: All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b None Pre-emphasis is non All 1b Enabled Filter pre-emphasis is enabled All
2	0b WO	**VCFG:** Project: All Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
1	0b WO	**V:** Project: All Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
0	1b WO	**DIGEN:** All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Blocked Digital data is blocked from passing through the node, regardless of the state All 1b Passed Digital data can pass through the node (Default = 1, enabled) All

3.4.94 AUD_PWST2_DBG—Offset 62F14h

audio pwst2 debug

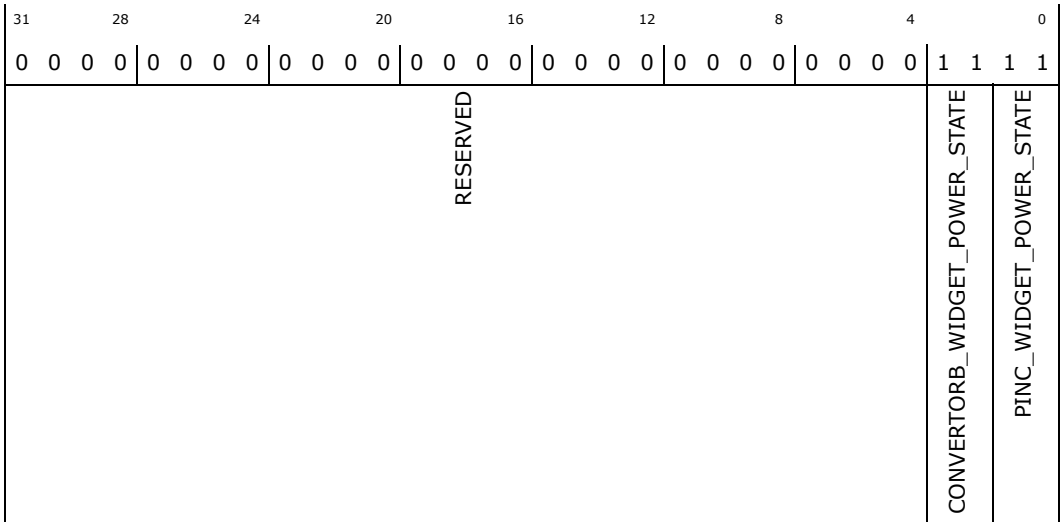
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_PWST2_DBG: [GTTMMADR_LSB + 2BF20h] + 62F14h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:4	0b WO	**RESERVED:** Project: All Format: MBZ
3:2	11b WO	**CONVERTORB_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was requested by audio software Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)
1:0	11b WO	**PINC_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)

3.4.95 AUD_OUT_STR_DESC_B_DBG—Offset 62F18h

HDAudio Verb: Converter Widget 2/72D These values are returned from the device as the Stream Descriptor Format response to a Get Audio Output Converter Widget command.

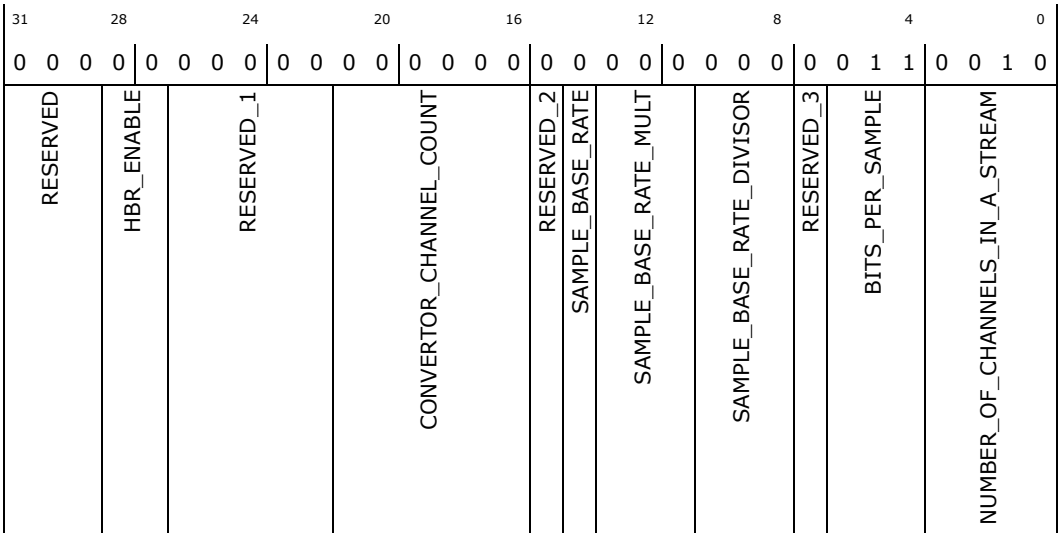
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_STR_DESC_B_DBG: [GTTMMADR_LSB + 2BF20h] + 62F18h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000032h



Bit Range	Default & Access	Description
31:29	0b WO	**RESERVED:** Project: All Format: MBZ
28:27	0b WO	**HBR_ENABLE:** Project: All This reflects the current HBR settings
26:22	0b WO	**RESERVED_1:** Project: All Format: MBZ
21:16	0b WO	**CONVERTOR_CHANNEL_COUNT:** Project: All This reflects the Convertor Channel Count programmed through HDAudio.
15	0b WO	**RESERVED_2:** Project: All Format: MBZ
14	0b WO	**SAMPLE_BASE_RATE:** Project: All Default Value: 0b (48 KHz) Sampling base rate of audio stream Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0b WO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: 000b (48 KHz) Audio stream sample base rate multiple Value Name Description Project 000b 1x 48 kHz/44.1 kHz or less All 001b 2x x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b 3x x3 (144 kHz) All 011b 4x x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved
10:8	0b WO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: 000b (indicates divide by 1 which results in 48 KHz) Audio stream sample base rate divisor Value Name Description Project 000b Divide by 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Divide by 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Divide by 3 Divide by 3 (16 kHz, 32 kHz) All 011b Divide by 4 Divide by 4 (11.025 kHz) All 100b Divide by 5 Divide by 5 (9.6 kHz) All 101b Divide by 6 Divide by 6 (8 kHz) All 110b Divide by 7 Divide by 7 All 111b Divide by Divide by 8 (6 kHz) All
7	0b WO	**RESERVED_3:** Project: All Format: MBZ

Bit Range	Default & Access	Description
6:4	011b WO	**BITS_PER_SAMPLE:** Project: All Default Value: 011b (Indicates 24 bits) Audio stream sample base rate multiple Value Name Description Project 000b 8 bits The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 010b 24 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 100b 20 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All Others Reserved Reserved
3:0	0010b WO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Format: U4+1 Default Value: 0010b (3 channels in each frame) Number of channels in each frame of the stream

3.4.96 AUD_OUT_DIG_CNVT_B_DBG—Offset 62F1Ch

HDAudio Verb: Converter Widget 70D/70E/73E/73F/706 These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Access Method

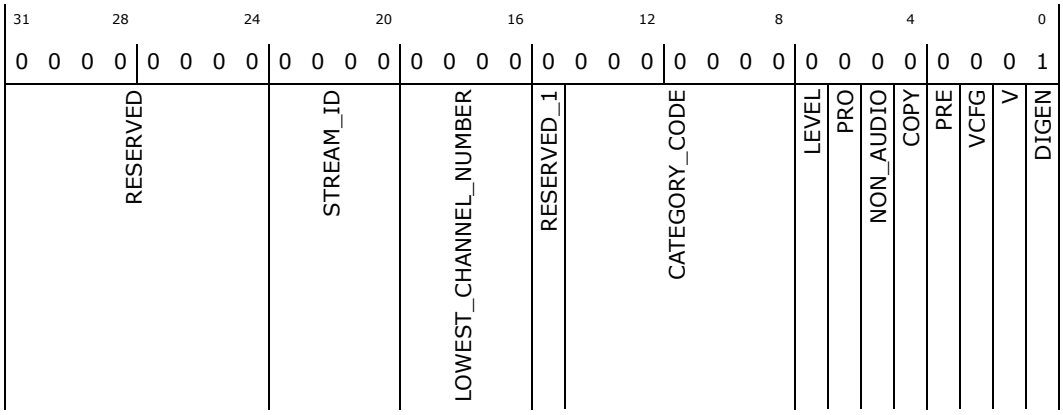
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_DIG_CNVT_B_DBG: [GTTMMADR_LSB + 2BF20h] + 62F1Ch

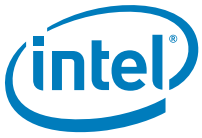
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:24	0b WO	**RESERVED:** Project: All Format: MBZ



Bit Range	Default & Access	Description
23:20	0b WO	**STREAM_ID:** Project: All Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
19:16	0b WO	**LOWEST_CHANNEL_NUMBER:** Project: All Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0
15	0b WO	**RESERVED_1:** Project: All Format: MBZ
14:8	0b WO	**CATEGORY_CODE:** Project: All S/PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default = 0
7	0b WO	**LEVEL:** Project: All S/PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
6	0b WO	**PRO:** Project: All This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register. Value Name Description Project 0b Consumer Consumer use. Default (Consumer) All 1b Professional Professional use All
5	0b WO	**NON_AUDIO:** Project: All Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b PCM Data is PCM (Default) All 1b Non-PCM Data is non PCM format All
4	0b WO	**COPY:** Project: All Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0b WO	**PRE:** Project: All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b None Pre-emphasis is non All 1b Enabled Filter pre-emphasis is enabled All
2	0b WO	**VCFG:** Project: All Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
1	0b WO	**V:** Project: All Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
0	1b WO	**DIGEN:** All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Blocked Digital data is blocked from passing through the node, regardless of the state All 1b Passed Digital data can pass through the node (Default = 1, enabled) All

3.4.97 AUD_PORT_EN_B_DBG—Offset 62F20h

HDAudio Verb: PinWidget 707/3/734/701 These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

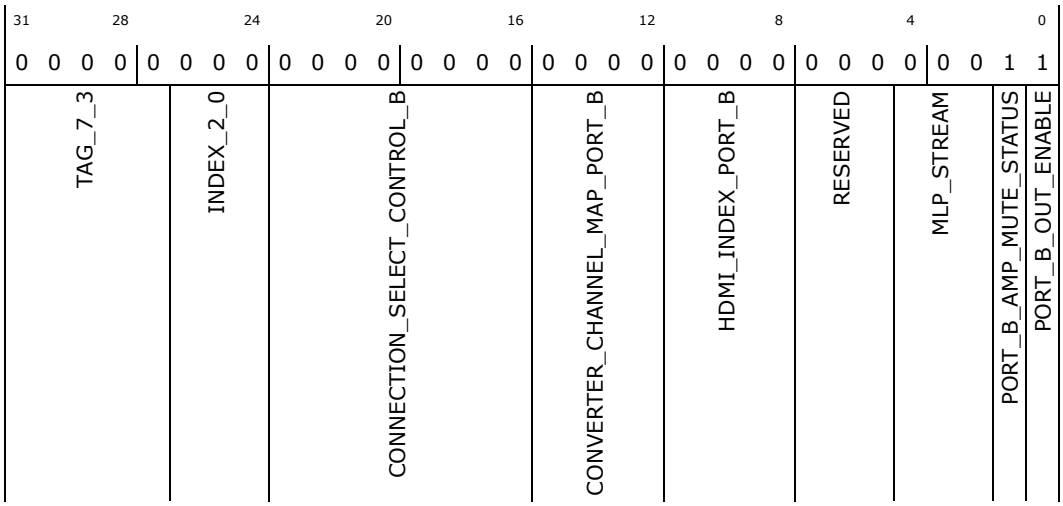
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_PORT_EN_B_DBG: [GTTMMADR_LSB + 2BF20h] + 62F20h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:27	0b WO	**TAG_7_3:** Project: All This represents the SSID that will go in the lower 5 bits of the SSID
26:24	0b WO	**INDEX_2_0:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
23:16	0b WO	**CONNECTION_SELECT_CONTROL_B:** Access Read Only Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
15:12	0b WO	**CONVERTER_CHANNEL_MAP_PORT_B:** Access Read Only Project: All The number in this field reflects the HD audio channel to which the HDMI channel is mapped. This field is read only
11:8	0b WO	**HDMI_INDEX_PORT_B:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
7:5	0b WO	**RESERVED:** Project: All Format: MBZ
4:2	0b WO	**MLP_STREAM:** Project: All Default Value: 000b Default Value Name Description Project 000b Default Default All 011b MLP Stream MLP Stream All Others Reserved Reserved All

Bit Range	Default & Access	Description
1	1b WO	**PORT_B_AMP_MUTE_STATUS:** Access Read Only Project: All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
0	1b WO	**PORT_B_OUT_ENABLE:** All This bit reflects the state of the output path of the Pin Widget. When 0, audio is disabled . Default = 1

3.4.98 AUD_PWST3_DBG—Offset 62F24h

HDAudio Verb: Pin Widget 705

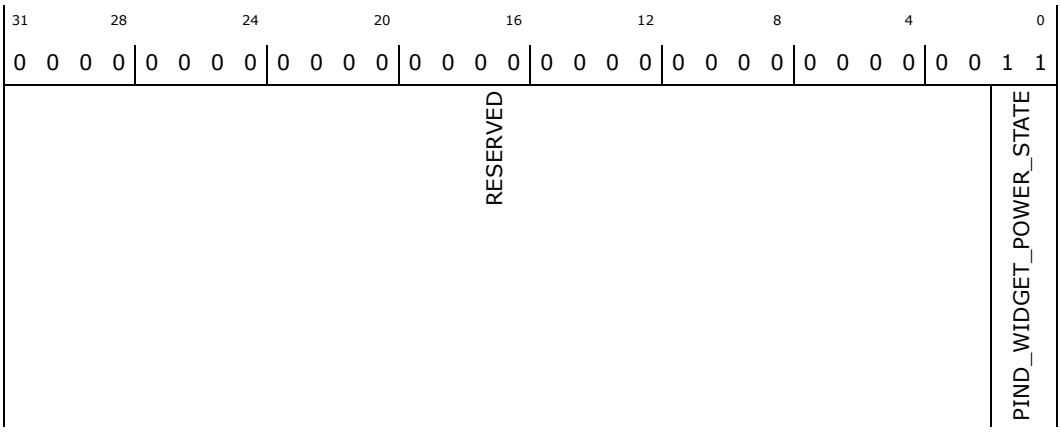
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_PWST3_DBG: [GTTMMADR_LSB + 2BF20h] + 62F24h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:2	0b WO	**RESERVED:** Project: All Format: MBZ
1:0	11b WO	**PIND_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)

3.4.99 AUD_PORT_EN_C_DBG—Offset 62F28h

HDAudio Verb: PinWidget 707/3/734/701 These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Access Method

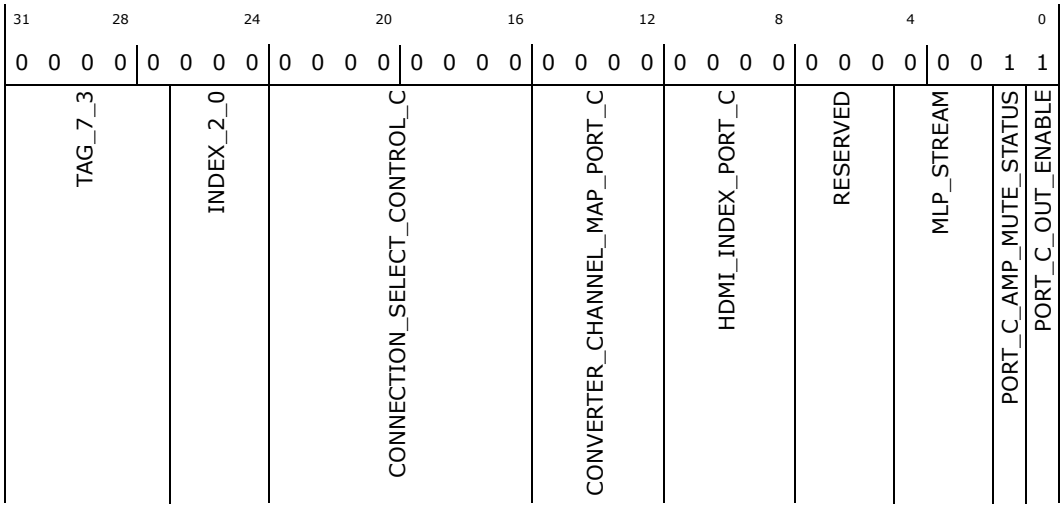
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_PORT_EN_C_DBG: [GTTMMADR_LSB + 2BF20h] + 62F28h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:27	0b WO	**TAG_7_3:** Project: All This represents the SSID that will go in the lower 5 bits of the SSID
26:24	0b WO	**INDEX_2_0:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
23:16	0b WO	**CONNECTION_SELECT_CONTROL_C:** Access Read Only Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
15:12	0b WO	**CONVERTER_CHANNEL_MAP_PORT_C:** Access Read Only Project: All The number in this field reflects the HD audio channel to which the HDMI channel is mapped. This field is read only
11:8	0b WO	**HDMI_INDEX_PORT_C:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
7:5	0b WO	**RESERVED:** Project: All Format: MBZ
4:2	0b WO	**MLP_STREAM:** Project: All Default Value: 000b Default Value Name Description Project 000b Default Default All 011b MLP Stream MLP Stream All Others Reserved Reserved All
1	1b WO	**PORT_C_AMP_MUTE_STATUS:** Access Read Only Project: All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
0	1b WO	**PORT_C_OUT_ENABLE:** All This bit reflects the state of the output path of the Pin Widget. When 0, audio is disabled . Default = 1

3.4.100 AUD_PORT_EN_D_DBG—Offset 62F2Ch

HDAudio Verb: PinWidget 707/3/734/701 These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

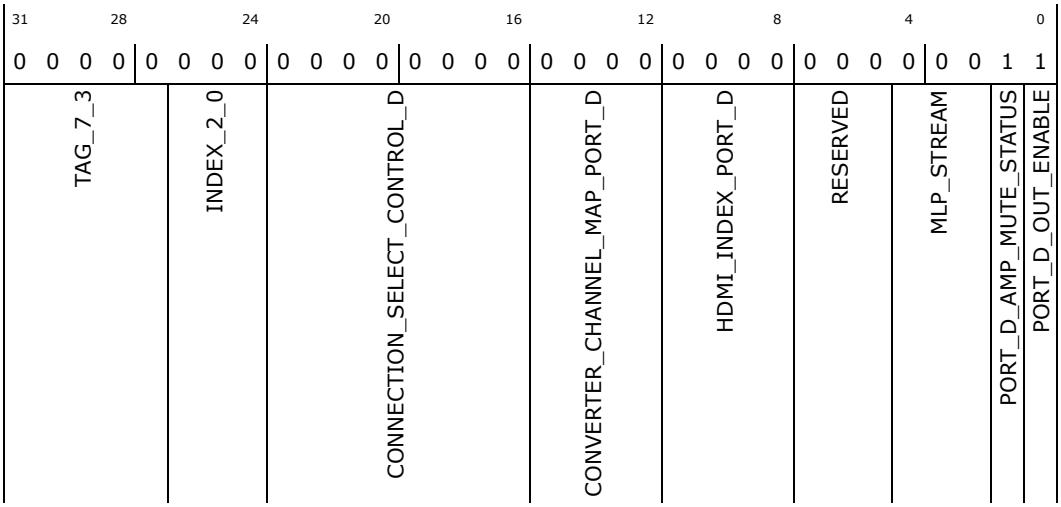
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_PORT_EN_D_DBG: [GTTMMADR_LSB + 2BF20h] + 62F2Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:27	0b WO	**TAG_7_3:** Project: All This represents the SSID that will go in the lower 5 bits of the SSID
26:24	0b WO	**INDEX_2_0:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
23:16	0b WO	**CONNECTION_SELECT_CONTROL_D:** Access Read Only Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
15:12	0b WO	**CONVERTER_CHANNEL_MAP_PORT_D:** Access Read Only Project: All The number in this field reflects the HD audio channel to which the HDMI channel is mapped. This field is read only
11:8	0b WO	**HDMI_INDEX_PORT_D:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
7:5	0b WO	**RESERVED:** Project: All Format: MBZ
4:2	0b WO	**MLP_STREAM:** Project: All Default Value: 000b Default Value Name Description Project 000b Default Default All 011b MLP Stream MLP Stream All Others Reserved Reserved All

Bit Range	Default & Access	Description
1	1b WO	**PORT_D_AMP_MUTE_STATUS:** Access Read Only Project: All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
0	1b WO	**PORT_D_OUT_ENABLE:** All This bit reflects the state of the output path of the Pin Widget. When 0, audio is disabled . Default = 1

3.4.101 AUD_CHICKENBIT_REG—Offset 62F38h

audio chickenbit register

Access Method

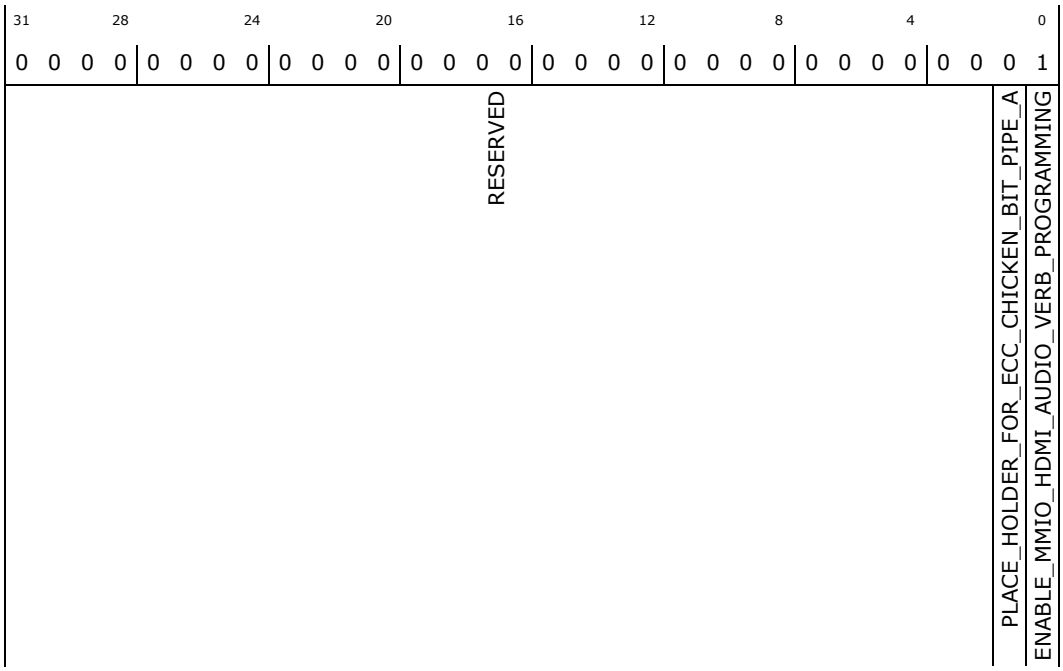
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CHICKENBIT_REG: [GTTMMADR_LSB + 2BF20h] + 62F38h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:2	0b WO	**RESERVED:** Project: All Format: MBZ
1	0b WO	**PLACE_HOLDER_FOR_ECC_CHICKEN_BIT_PIPE_A:** Project: All audr_ecc_flip_chicken_bit

Bit Range	Default & Access	Description
0	1b WO	**ENABLE_MMIO_HDMI_AUDIO_VERB_PROGRAMMING:** All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b HDAudio Programming through HDAudio Azalia All 1b MMIO Programming through MMIO Debug registers All

3.4.102 AUD_OUT_DIG_CNVTA_DBG—Offset 62F40h

HDAudio Verb: Converter Widget 70E/73E These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Access Method

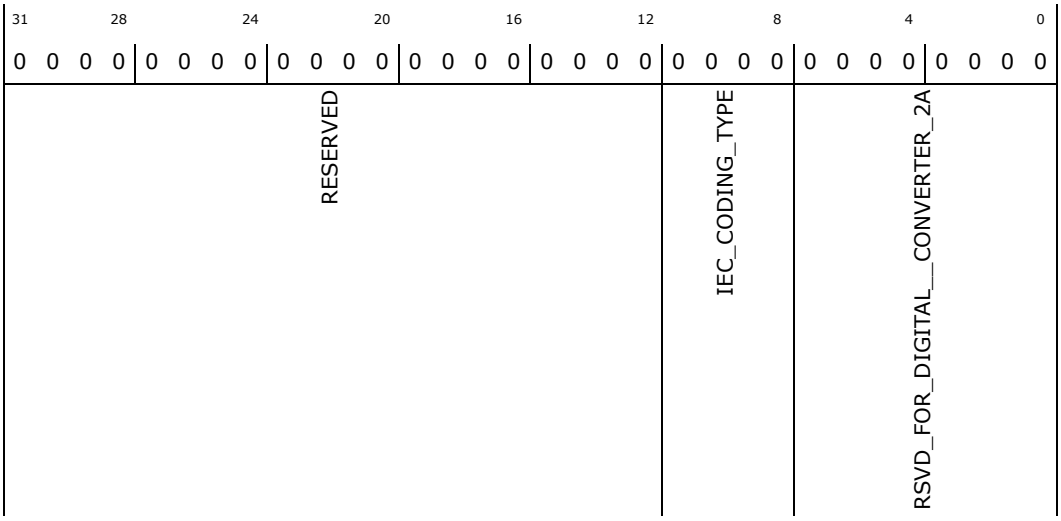
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_DIG_CNVTA_DBG: [GTTMMADR_LSB + 2BF20h] + 62F40h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b WO	**RESERVED:** Project: All Format: MBZ
11:8	0b WO	**IEC_CODING_TYPE:** Project: All
7:0	0b WO	**RSVD_FOR_DIGITAL__CONVERTER_2A:** Project: All

3.4.103 AUD_OUT_DIG_CNVTB_DBG—Offset 62F44h

HDAudio Verb: Converter Widget 70E/73E These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

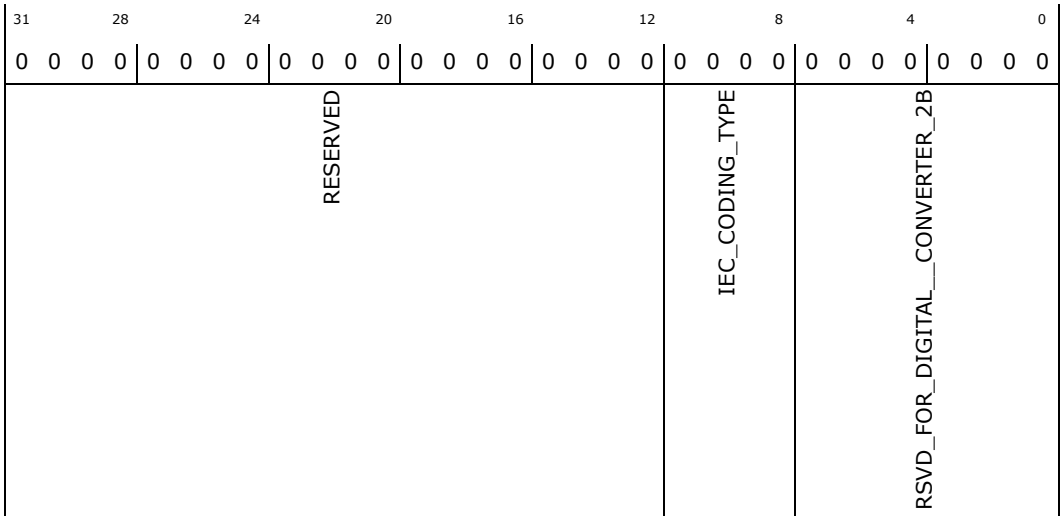
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_OUT_DIG_CNVTB_DBG: [GTTMMADR_LSB + 2BF20h] + 62F44h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b WO	**RESERVED:** Project: All Format: MBZ
11:8	0b WO	**IEC_CODING_TYPE:** Project: All
7:0	0b WO	**RSVD_FOR_DIGITAL__CONVERTER_2B:** Project: All

3.4.104 AUD_CNTL_ST_B_DBG—Offset 62F60h

HDAudio Verb: Pin Widget 730/732

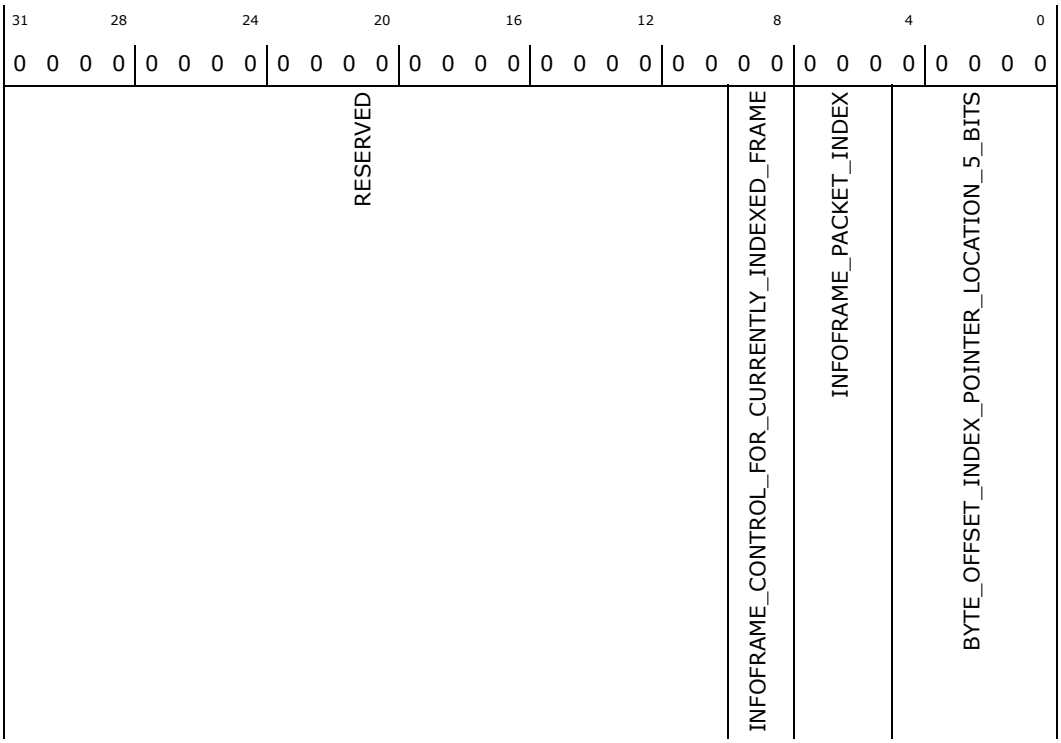
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CNTL_ST_B_DBG: [GTTMMADR_LSB + 2BF20h] + 62F60h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0b WO	**RESERVED:** Project: All Format: MBZ
9:8	0b WO	**INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME:** Project: All Default Value: 00b disable xmit Value Name Description Project 00b Disable xmit Disable xmit All 01b Reserved Reserved All 10b Xmit once Xmit once All 11b Best Effort Best Effort All
7:5	0b WO	**INFOFRAME_PACKET_INDEX:** Project: All Default Value: 00b Audio Value Name Description Project 000b Audio Audio All 001b GP GP All 010b GP2 GP2 All 011b GP3 GP3 All 100b GP4 GP4 All Others Reserved Reserved All
4:0	0b WO	**BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS:** Project: All

3.4.105 AUD_HDMIW_INFOFR_B_DBG—Offset 62F64h

HDAudio Verb: Pin Widget 731

Access Method

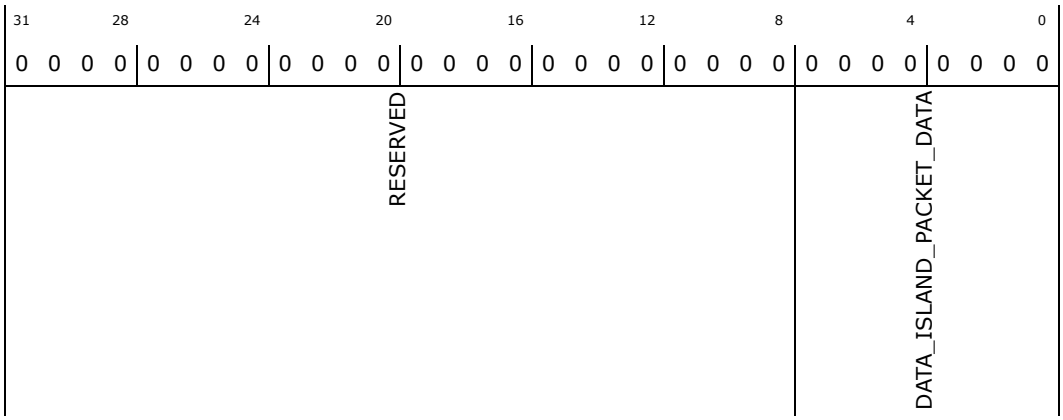
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_HDMIW_INFOFR_B_DBG: [GTTMMADR_LSB + 2BF20h] + 62F64h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b WO	**RESERVED:** Project: All Format: MBZ
7:0	0b WO	**DATA_ISLAND_PACKET_DATA:** Project: All This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

3.4.106 AUD_CNTL_ST_C_DBG—Offset 62F70h

HDAudio Verb: Pin Widget 730/732

Access Method

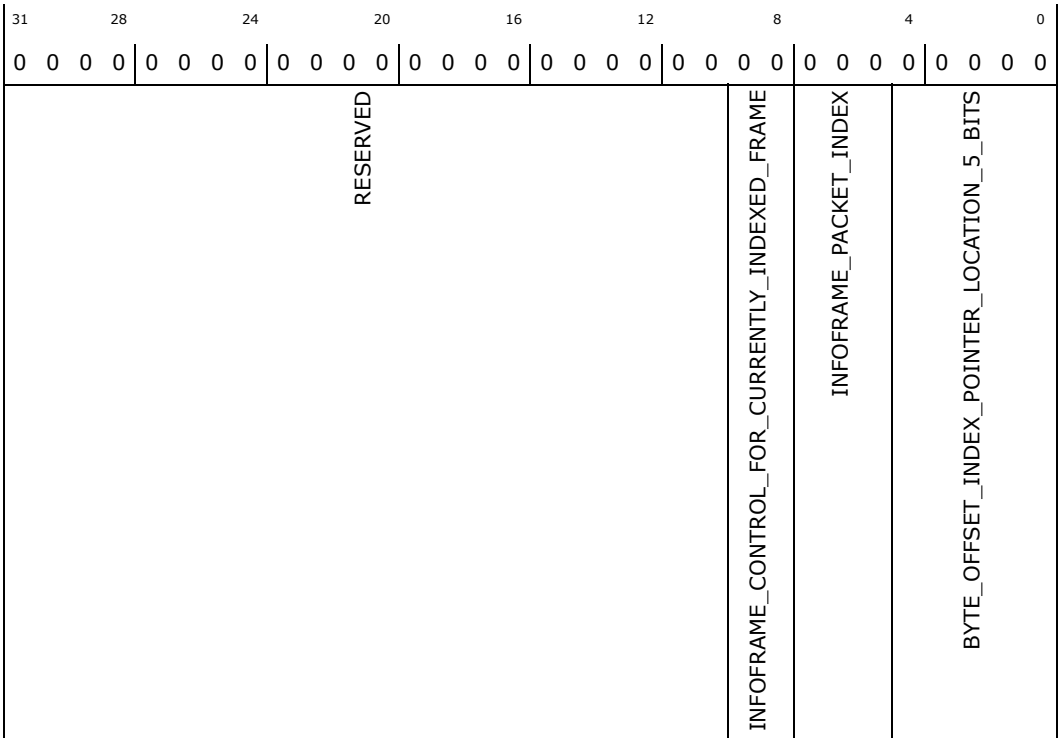
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CNTL_ST_C_DBG: [GTTMMADR_LSB + 2BF20h] + 62F70h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0b WO	**RESERVED:** Project: All Format: MBZ
9:8	0b WO	**INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME:** Project: All Default Value: 00b disable xmit Value Name Description Project 00b Disable xmit Disable xmit All 01b Reserved Reserved All 10b Xmit once Xmit once All 11b Best Effort Best Effort All
7:5	0b WO	**INFOFRAME_PACKET_INDEX:** Project: All Default Value: 00b Audio Value Name Description Project 000b Audio Audio All 001b GP GP All 010b GP2 GP2 All 011b GP3 GP3 All 100b GP4 GP4 All Others Reserved Reserved All
4:0	0b WO	**BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS:** Project: All

3.4.107 AUD_HDMIW_INFOFR_C_DBG—Offset 62F74h

HDAudio Verb: Pin Widget 731

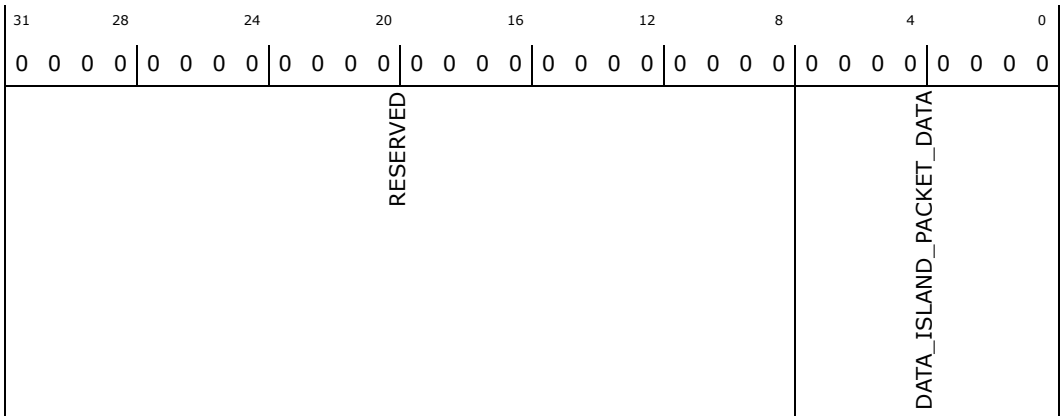
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_HDMIW_INFOFR_C_DBG: [GTTMMADR_LSB + 2BF20h] + 62F74h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b WO	**RESERVED:** Project: All Format: MBZ
7:0	0b WO	**DATA_ISLAND_PACKET_DATA:** Project: All This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

3.4.108 AUD_CNTL_ST_D_DBG—Offset 62F80h

HDAudio Verb: Pin Widget 730/732

Access Method

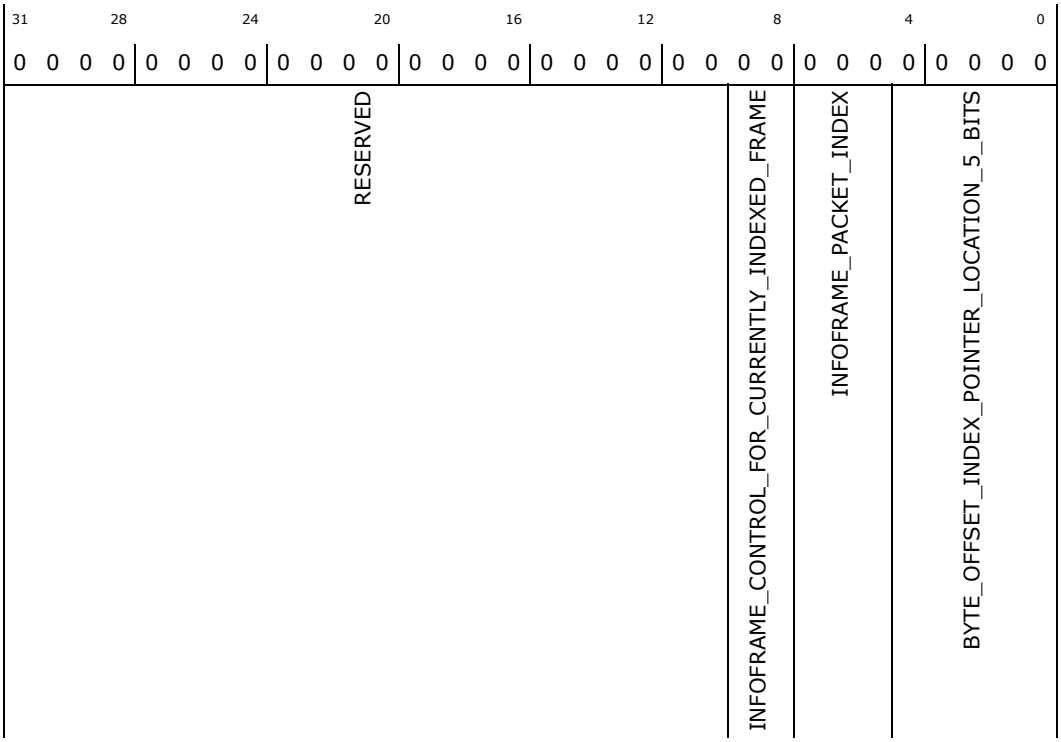
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CNTL_ST_D_DBG: [GTTMMADR_LSB + 2BF20h] + 62F80h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0b WO	**RESERVED:** Project: All Format: MBZ
9:8	0b WO	**INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME:** Project: All Default Value: 00b disable xmit Value Name Description Project 00b Disable xmit Disable xmit All 01b Reserved Reserved All 10b Xmit once Xmit once All 11b Best Effort Best Effort All
7:5	0b WO	**INFOFRAME_PACKET_INDEX:** Project: All Default Value: 00b Audio Value Name Description Project 000b Audio Audio All 001b GP GP All 010b GP2 GP2 All 011b GP3 GP3 All 100b GP4 GP4 All Others Reserved Reserved All
4:0	0b WO	**BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS:** Project: All

3.4.109 AUD_HDMIW_INFOFR_D_DBG—Offset 62F84h

HDAudio Verb: Pin Widget 731

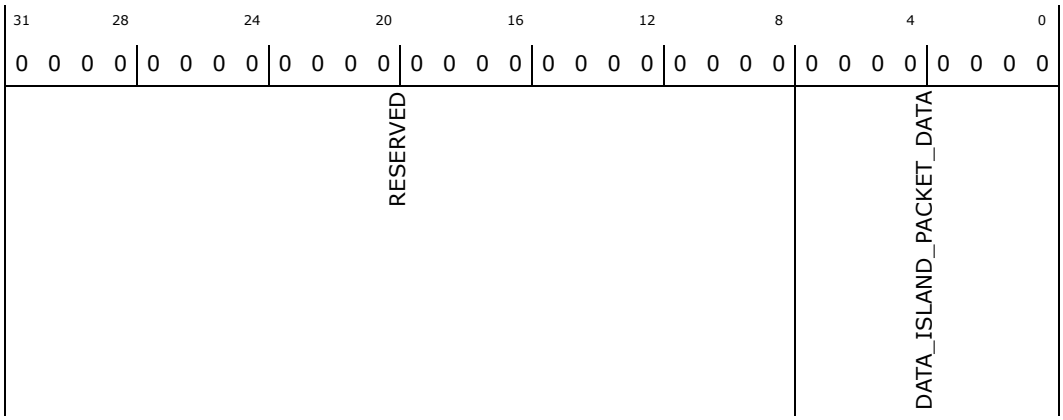
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_HDMIW_INFOFR_D_DBG: [GTTMMADR_LSB + 2BF20h] + 62F84h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b WO	**RESERVED:** Project: All Format: MBZ
7:0	0b WO	**DATA_ISLAND_PACKET_DATA:** Project: All This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

3.4.110 AUD_CONFIG_DEFAULT2_REG_PORTB—Offset 62F88h

HDAudio Verb: Pin Widget 738..73B

Access Method

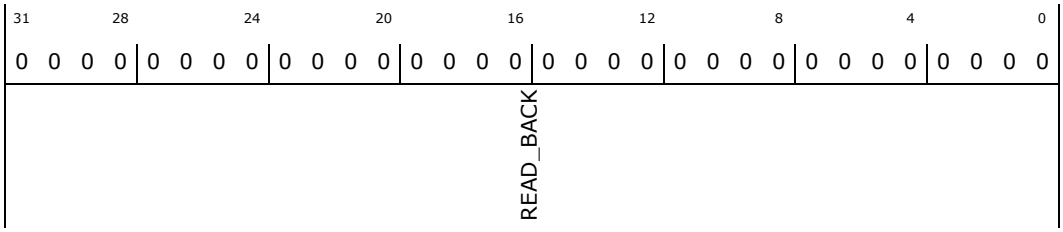
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CONFIG_DEFAULT2_REG_PORTB: [GTTMMADR_LSB + 2BF20h] + 62F88h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b WO	**READ_BACK:** Project: All Config Default 2 values of port B rgars being written using the 738/739/73A/73B

3.4.111 AUD_CONFIG_DEFAULT2_REG_PORTC—Offset 62F8Ch

HDAudio Verb: Pin Widget 738..73B

Access Method

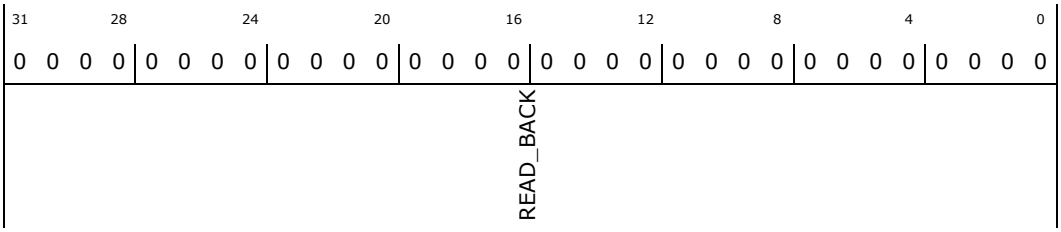
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CONFIG_DEFAULT2_REG_PORTC: [GTTMMADR_LSB + 2BF20h] + 62F8Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b WO	**READ_BACK:** Project: All Config Default 2 values of port C rgars being written using the 738/739/73A/73B

3.4.112 AUD_CONFIG_DEFAULT2_REG_PORTD—Offset 62F90h

HDAudio Verb: Pin Widget 738..73B

Access Method

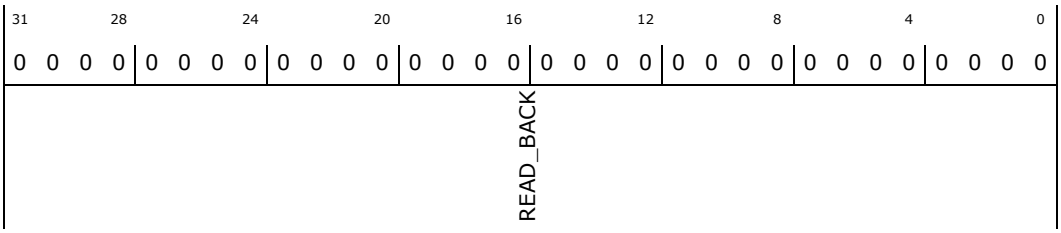
Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_CONFIG_DEFAULT2_REG_PORTD: [GTTMMADR_LSB + 2BF20h] + 62F90h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b WO	**READ_BACK:** Project: All Config Default 2 values of port D rgars being written using the 738/739/73A/73B

3.4.113 AUD_MCTSA—Offset 62F94h

Audio M or CTS Pipe A Values Readback Register

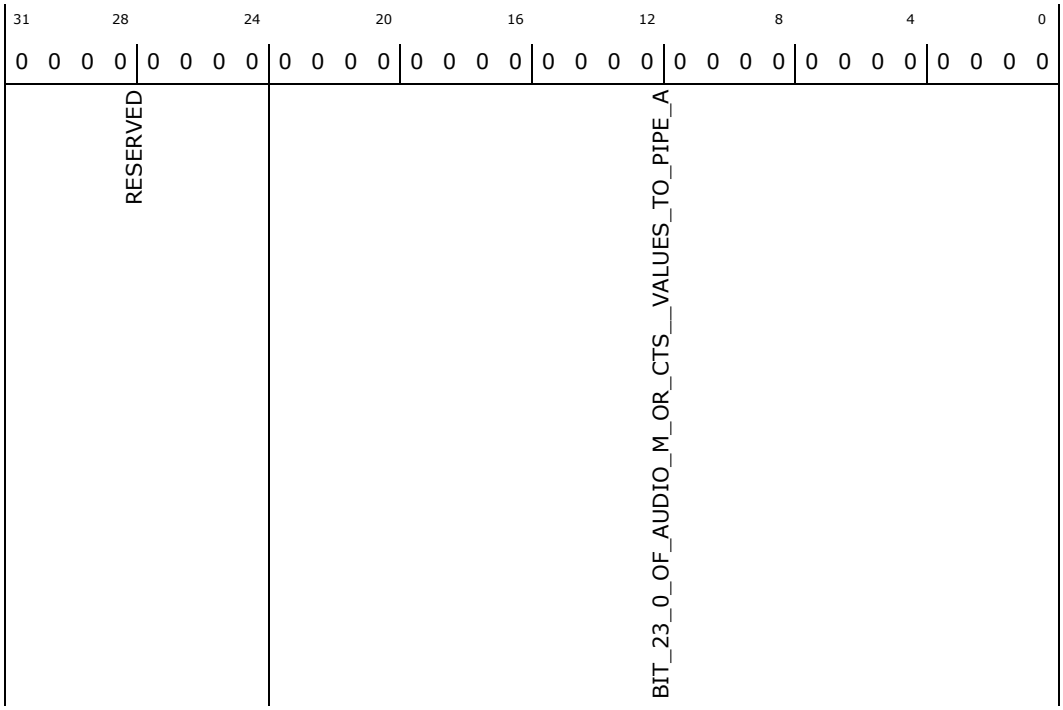
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_MCTSA: [GTTMMADR_LSB + 2BF20h] + 62F94h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Project: All Format: MBZ
23:0	0b RO	**BIT_23_0_OF_AUDIO_M_OR_CTS__VALUES_TO_PIPE_A:** Project: All

3.4.114 AUD_MCTSB—Offset 62F98h

Audio M or CTS Pipe B Values Readback Register

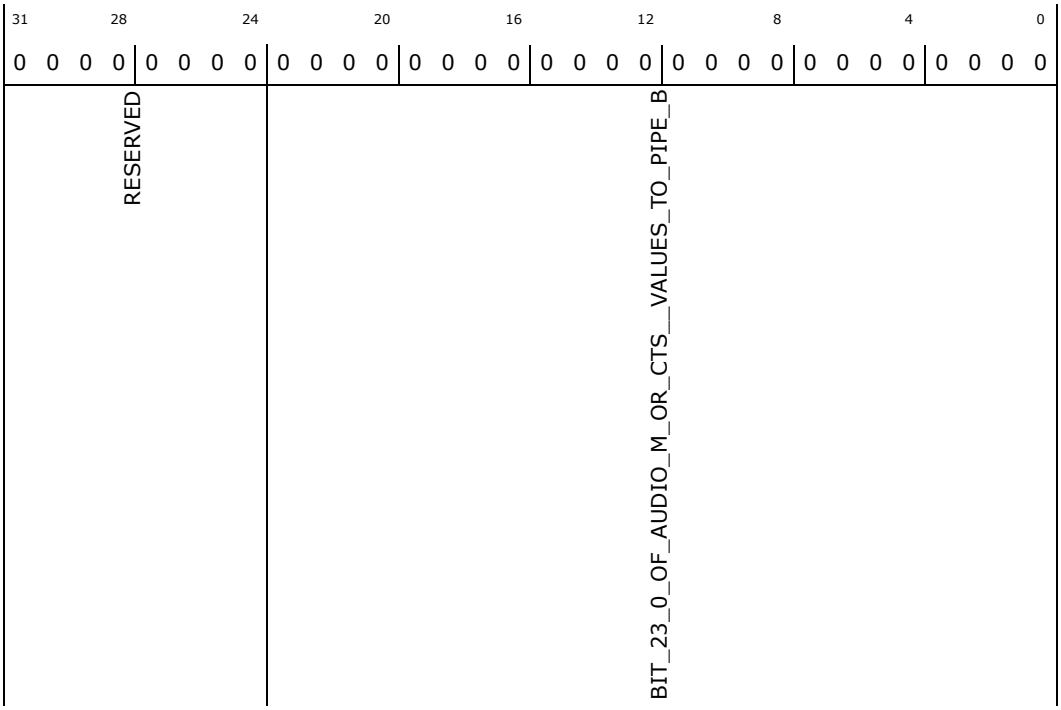
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

AUD_MCTSB: [GTTMMADR_LSB + 2BF20h] + 62F98h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Project: All Format: MBZ
23:0	0b RO	**BIT_23_0_OF_AUDIO_M_OR_CTS__VALUES_TO_PIPE_B:** Project: All

3.4.115 DP_B—Offset 64100h

DisplayPort B Control Register [DevCTG, DevCDV] Display Port B control (dprrega_b0.vql_displayb1)

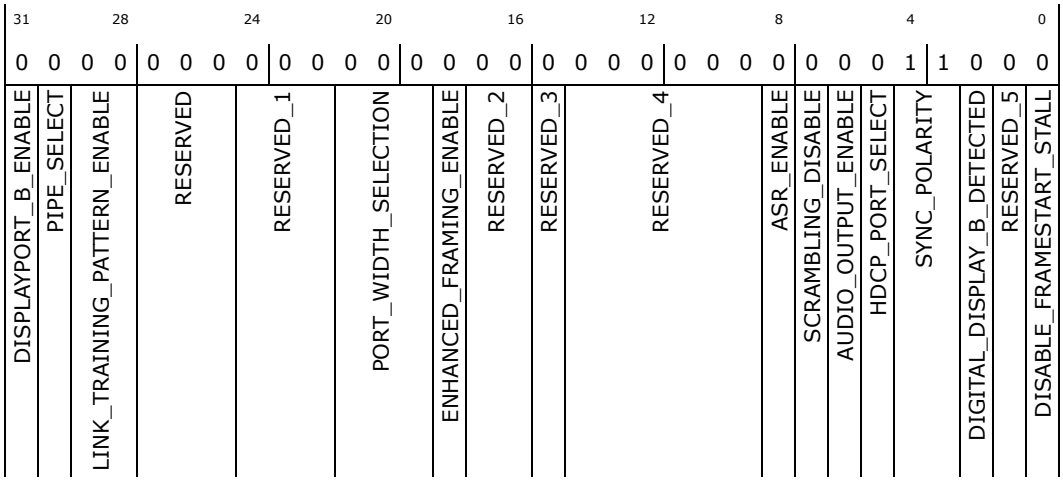
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

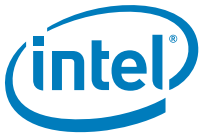
DP_B: [GTTMMADR_LSB + 2BF20h] + 64100h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000018h



Bit Range	Default & Access	Description
31	0b RW	**DISPLAYPORT_B_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. 1 = Enable. This bit enables the Display Port B interface. 0 = Disable and tristates the Display Port B interface.
30	0b RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29:28	0b RW	**LINK_TRAINING_PATTERN_ENABLE:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. 00 Pattern 1 enabled: Repetition of D10.2 characters Default. 01 Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. 10 Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times 11 Link not in training: Send normal pixels
27:25	0b RW	**RESERVED:** [DevCDV]: Voltage swing level set: [DevCTG]: These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration (At CDV moved to register at the DPIO) 000 0.4V (DEFAULT) 001 0.6V 010 0.8V 011 1.2V RESERVED 1xx RESERVED
24:22	0b RW	**RESERVED_1:** [DevCDV]: Pre-emphasis level set [DevCTG]: These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification. They mirror registers in the PCI express configuration. At CDV this field move to register in the DPIO. 000 no pre-emphasis (default) 001 3.5dB pre-emphasis (1.5x) 010 6dB pre-emphasis (2x) 011 9.5dB pre-emphasis (3x) RESERVED 1xx RESERVED
21:19	0b RW	**PORT_WIDTH_SELECTION:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 000 = x1 Mode (Default) 001 = x2 Mode. 010 = RESERVED 011 = x4 Mode. 1xx = RESERVED



Bit Range	Default & Access	Description
18	0b RW	**ENHANCED_FRAMING_ENABLE:** This bit selects enhanced framing. It must be set when HDCP will be used invoked. 0 (Default) Enhanced framing disabled 1 Enhanced framing enabled. Locked once port is enabled. Updates when the port is disabled then re-enabled
17:16	0b RW	**RESERVED_2:** MBZ
15	0b RW	**RESERVED_3:** [DevCDV]: Port reversal [DevCTG]: Locked once port is enabled. Updates when the port is disabled then re-enabled
14:9	0b RW	**RESERVED_4:** MBZ
8	0b RW	**ASR_ENABLE:** [DevVLV2]: this bit enables the Alternate Scrambler Reset capability for eDP port to use alternate scrambler reset value of FFFEh 1 - ASR enable 0 ASR disable
7	0b RW	**SCRAMBLING_DISABLE:** [DevCTG, B-step only, DevCDV]: This bit disables scrambling for this port. 0 = Scrambling enabled (Default) 1 = Scrambling disabled, no SR after initialization at loop 2 of training
6	0b RW	**AUDIO_OUTPUT_ENABLE:** This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to Normal 0 = Audio output disabled 1 = Audio output enabled
5	0b RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port
4:3	11b RW	**SYNC_POLARITY:** Indicates the polarity of Hsync and Vsync. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0b RO	**DIGITAL_DISPLAY_B_DETECTED:** Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 4 (port B) data line at boot. 0 = digital display not detected during initialization (Default) 1 = digital display detected during initialization AccessType: Read Only
1	0b RW	**RESERVED_5:** MBZ
0	0b RW	**DISABLE_FRAMESTART_STALL:** This bit, when set, will disable the framestart window to stall DP AV mixer from sending audio samples before framestart. This applies to BOTH pipes. 0 = Enable framestart window to stall audio samples. (default) 1 = Disable framestart window to stall audio samples.

3.4.116 DPB_AUX_CH_CTL—Offset 64110h

Display Port B AUX Channel Control [DevCDV] AuxB control (dprrega_b0.v auxb_ctl_rdback)

Access Method

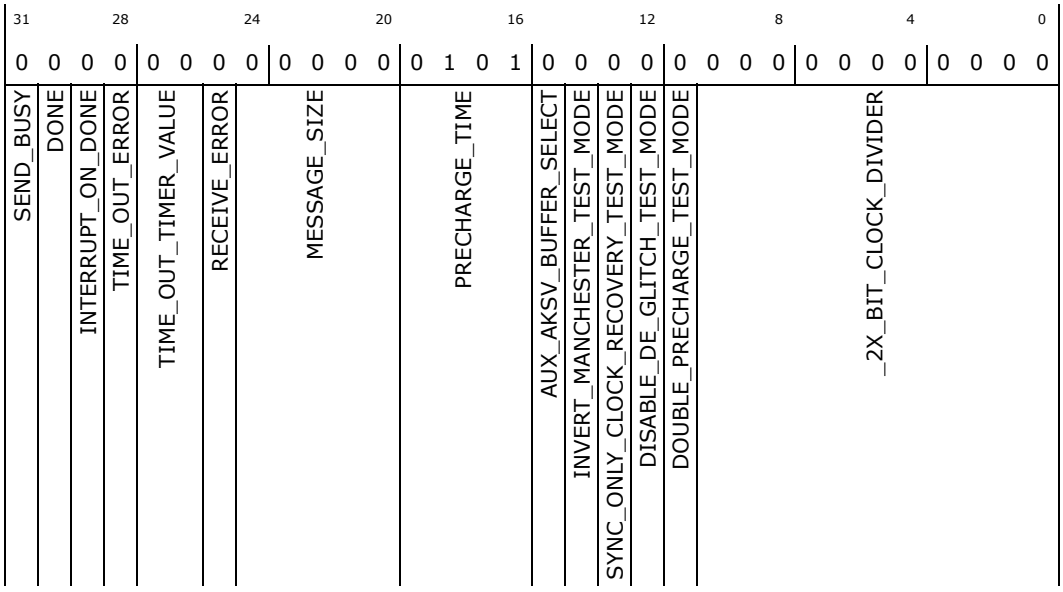
Type: Memory Mapped I/O Register (Size: 32 bits)

DPB_AUX_CH_CTL: [GTTMMADR_LSB + 2BF20h] + 64110h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00050000h



Bit Range	Default & Access	Description
31	0b RW	**SEND_BUSY:** Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a time out occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	0b RW/1C	**DONE:** A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
29	0b RW	**INTERRUPT_ON_DONE:** Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	0b RW/1C	**TIME_OUT_ERROR:** A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
27:26	0b RW	**TIME_OUT_TIMER_VALUE:** 00: 400us (default) 01: 600us 10: 800us 11: 1600us The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.
25	0b RW/1C	**RECEIVE_ERROR:** A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event. AccessType: One to Clear

Bit Range	Default & Access	Description
24:20	0b RW	**MESSAGE_SIZE:** This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only only when the done bit is set and timeout or receive error has not occurred. Sync/ Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or)20 are not allowed.
19:16	0101b RW	**PRECHARGE_TIME:** Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example: For 12us precharge, program 6 (12us/2us).
15	0b RW	**AUX_AKSV_BUFFER_SELECT:** This bit selects whether some of the data to be written over Display Port AUX comes from the Aksv buffer for HDCP authentication, or all from the AUX Data registers. Set this bit before initiating a transaction to write Aksv to the Display Port sink. All AUX protocol must be followed and Message Size set to 9 bytes. The first DWord transmitted will be from the AUX Data Register 1 for the header, then the DP_AUX_CH_AKSV_HI, then the last byte from DP_AUX_CH_AKSV_LO. The sink response is read back as usual from the AUX Data registers. More than one AUX channel can select to use the Aksv buffer simultaneously. 0 (Default) Use AUX Data registers for regular data transmission 1 Use Aksv Buffer for part of the data transmission.
14	0b RW	**INVERT_MANCHESTER_TEST_MODE:** 1 = Manchester code rising edge mid-clk signifies one (test mode) 0 = Manchester code rising edge mid-clk signifies zero (default)
13	0b RW	**SYNC_ONLY_CLOCK_RECOVERY_TEST_MODE:** 1 = Only recover clock during sync pattern (test mode) 0 = Recover clock during sync pattern and data phase (default)
12	0b RW	**DISABLE_DE_GLITCH_TEST_MODE:** 1 = Disable serial input de-glitch logic (test mode) 0 = Enable serial input de-glitch logic (default)
11	0b RW	**DOUBLE_PRECHARGE_TEST_MODE:** 1 = Precharge time is doubled 0 = Precharge time is as programmed
10:0	0b RW	**_2X_BIT_CLOCK_DIVIDER:** Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). [DevCTG-A] the input clock is cdclk. [DevCTG-B, DevCDV] the input clock is hrawclk (200MHz) Example: For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/2MHz).

3.4.117 DPB_AUX_CH_DATA1—Offset 64114h

Display Port B AUX Data Register 1 [DevCTG, DevCDV]

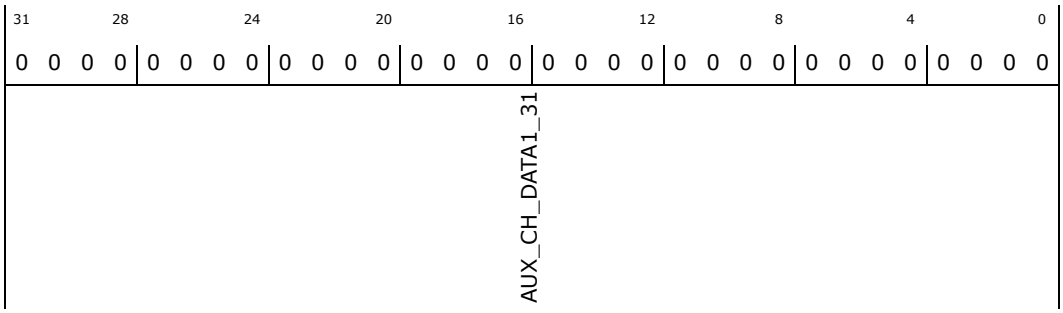
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPB_AUX_CH_DATA1: [GTTMMADR_LSB + 2BF20h] + 64114h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**AUX_CH_DATA1_31:** 0]: The first Dword of the message. The Msbyte is transmitted first. Reads will give the response data after transaction complete.

3.4.118 DPB_AUX_CH_DATA2—Offset 64118h

Display Port B AUX Data Register 2 [DevCTG, DevCDV] AuxB Data2 (dprrega_b0.v auxb_dpr_data2, ql_auxb_d2)

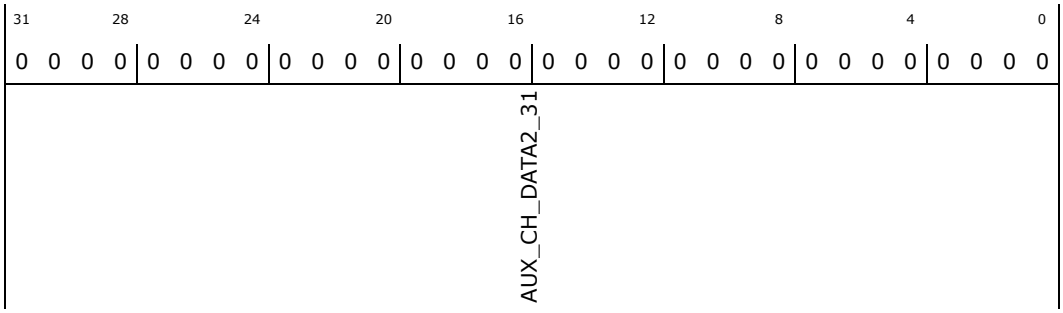
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPB_AUX_CH_DATA2: [GTTMMADR_LSB + 2BF20h] + 64118h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**AUX_CH_DATA2_31:** 0]: The second Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

3.4.119 DPB_AUX_CH_DATA3—Offset 6411Ch

Display Port B AUX Data Register 3 [DevCTG, DevCDV] AuxB Data3 (dprrega_b0.v auxb_dpr_data3, ql_auxb_d3)

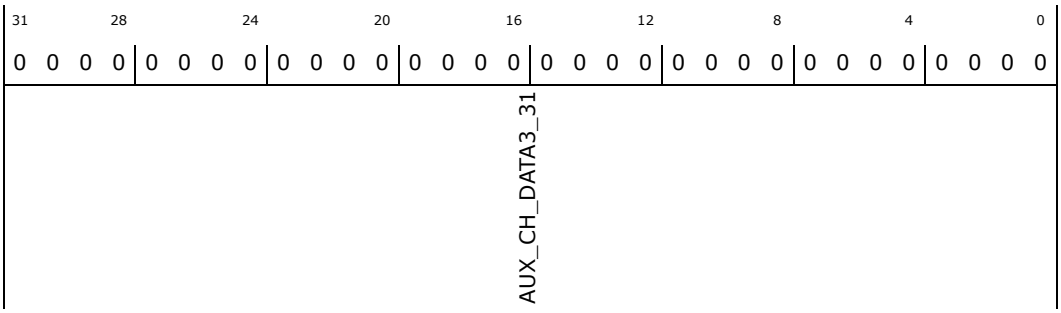
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPB_AUX_CH_DATA3: [GTTMMADR_LSB + 2BF20h] + 6411Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**AUX_CH_DATA3_31:** 0]: The third Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

3.4.120 DPB_AUX_CH_DATA4—Offset 64120h

Display Port B AUX Data Register 4 [DevCTG, DevCDV] AuxB Data4 (dprrega_b0.v auxb_dpr_data4, ql_auxb_d4)

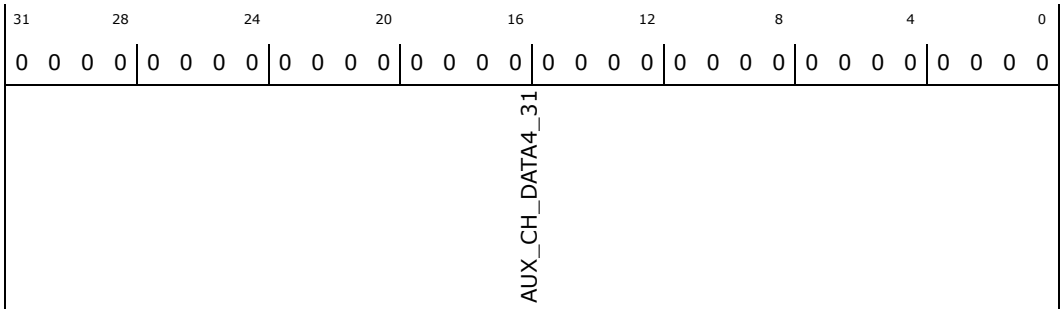
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPB_AUX_CH_DATA4: [GTTMMADR_LSB + 2BF20h] + 64120h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**AUX_CH_DATA4_31:** 0]: The fourth Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

3.4.121 DPB_AUX_CH_DATA5—Offset 64124h

Display Port B AUX Data Register 5 [DevCTG, DevCDV] AuxB Data5 (dprrega_b0.v auxb_dpr_data5, ql_auxb_d5)

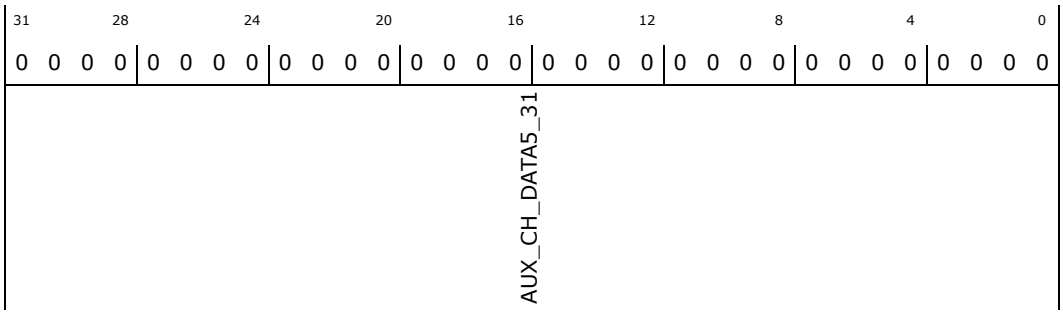
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPB_AUX_CH_DATA5: [GTTMMADR_LSB + 2BF20h] + 64124h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**AUX_CH_DATA5_31:** 0]: The fifth Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

3.4.122 DP_AUX_CH_AKSV_HI—Offset 64130h

Display Port AUX Aksv Buffer High [DevCTG-B, DevCDV] AuxB AKSV High (dprrega_b0.v dpr_aux_aksv_hi)

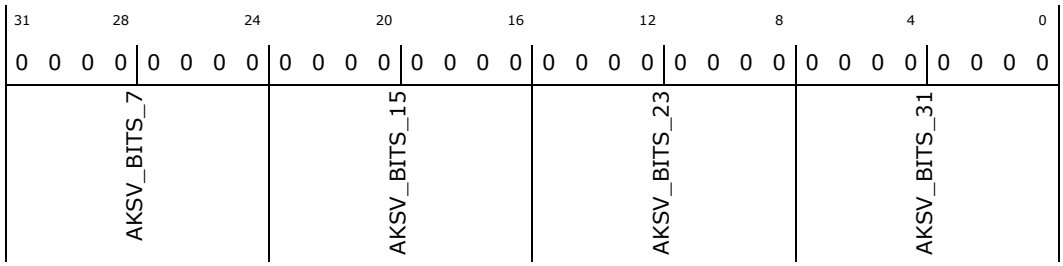
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DP_AUX_CH_AKSV_HI: [GTTMMADR_LSB + 2BF20h] + 64130h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b WO	**AKSV_BITS_7:** 0]
23:16	0b WO	**AKSV_BITS_15:** 8]
15:8	0b WO	**AKSV_BITS_23:** 16]
7:0	0b WO	**AKSV_BITS_31:** 24]

3.4.123 DP_AUX_CH_AKSV_LO—Offset 64134h

Display Port AUX Aksv Buffer Low [DevCTG-B, DevCDV] AuxB AKSV High (dprrega_b0.v dpr_aux_aksv_lo)

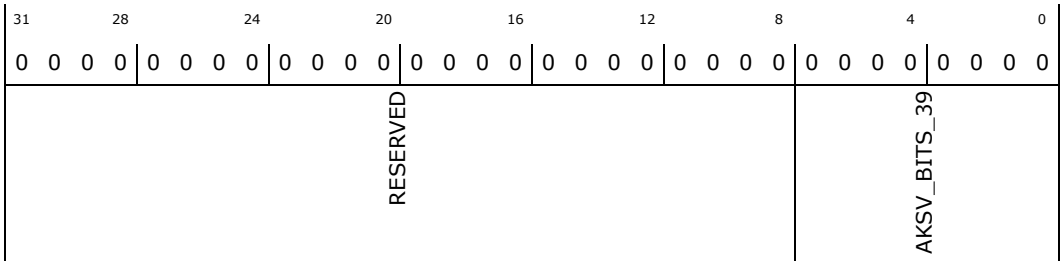
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DP_AUX_CH_AKSV_LO: [GTTMMADR_LSB + 2BF20h] + 64134h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b WO	**RESERVED:** MBZ
7:0	0b WO	**AKSV_BITS_39:** 32]

3.4.124 DPB_AUX_TST—Offset 64150h

Display Port B AUX Test Register

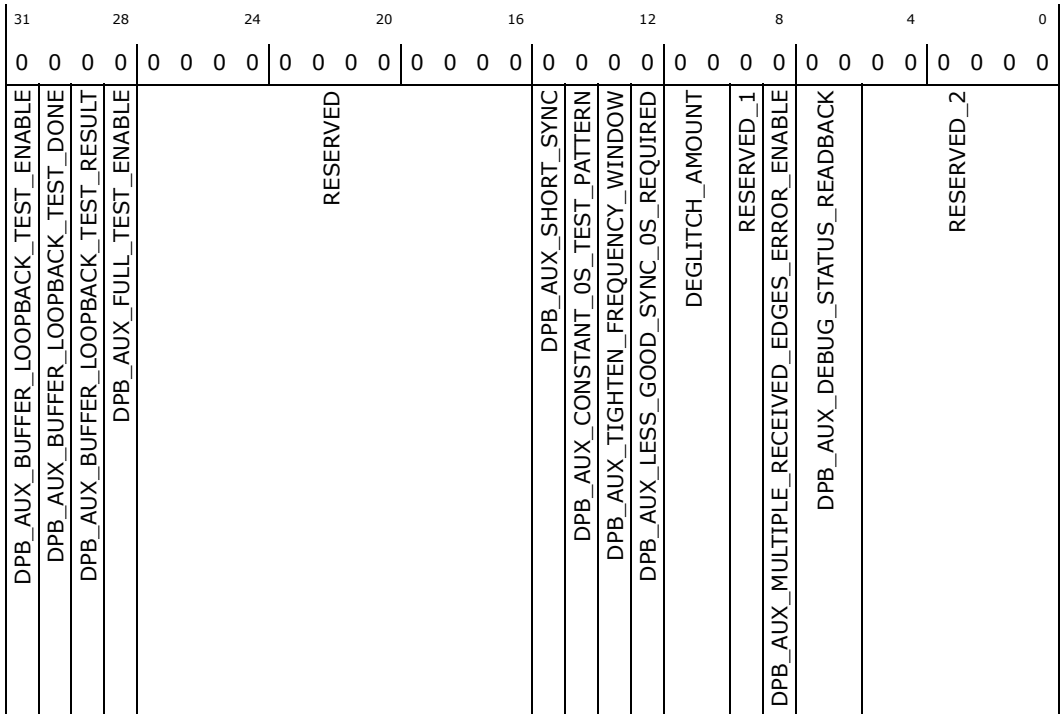
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPB_AUX_TST: [GTTMMADR_LSB + 2BF20h] + 64150h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**DPB_AUX_BUFFER_LOOPBACK_TEST_ENABLE:** Project: All Default Value: 0b Enables test for the DPB-AUX I/O buffer. A 16 cycle clock pattern is output to the I/O buffer and compared against the looped back buffer output. The input clock is cdclk. With input clock at 512MHz the pattern will bea 1 MHz clock. It scales down with lower clock frequencies. The result is found in DP-AUX Buffer Loopback Test Result after DP-AUX Buffer Loopback Test Done is set. Clear this bit to 0 after test is done to return DP-AUX to normal operation. Loopback Test can be run simultaneously on all AUX buffers. Do not enable DP-AUX Buffer Loopback Test and DP-AUX Full Test simultaneously. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test. All
30	0b RO	**DPB_AUX_BUFFER_LOOPBACK_TEST_DONE:** Project: All Default Value: 0b AccessType: Read Only DPB-AUX Buffer Loopback Test has been run and completed. This is not the done for the DP-AUX Full Test. Value Name Description Project 0b Not Done Test not done. DP-AUX Buffer Loopback Test Result is not valid All 1b Done Test done. DP-AUX Buffer Loopback Test Result is now valid All
29	0b RO	**DPB_AUX_BUFFER_LOOPBACK_TEST_RESULT:** Project: All Default Value: 0b AccessType: Read Only Result of the DPB-AUX Buffer Loopback Test. Value is only valid after a DP-AUX Loopback Test Done is 1. This is not the result of the DP-AUX Full Test. Value Name Description Project 0b Pass Pass All 1b Fail All

Bit Range	Default & Access	Description
28	0b RW	**DPB_AUX_FULL_TEST_ENABLE:** Project: All Default Value: 0b Enables test for the DPB-AUX core logic transmit and receive functions through the DPB-AUX and DPC-AUX buffers. DPB-AUX and DPC-AUX are interconnected through I/O buffer loopbacks. DPB-AUX is programmed as source to output a 20 byte test pattern. DPC-AUX is programmed as sink to receive the test pattern and reply with a different 20 byte test pattern. Test pattern 1 = 0xA55CC33E E770080C 0E0F0F8F CFEFF81C 3E77E3C8 Test pattern 2 = 0X183C7EE7 C381FF7F 3F1F0F07 030100EE 77CC33A5 Programming sequence: 1. Set DPB-AUX Full Test Enable to 1. 2. Program DPB_AUX_CH_DATA[1-5] with test pattern 1 to transmit as the source. 3. Program DPC_AUX_CH_DATA[1-5] with test pattern 2 to reply with as the sink. 4. Program all DPC_AUX_CH_CTL fields and set Send to 1. 5. Program all DPB_AUX_CH_CTL fields and set Send to 1. Then the test will start. Results checking sequence: 1. Poll DPB_AUX_CH_CTL for Done. To pass, Done must be set within 500us. 2. Read DPB_AUX_CH_CTL register. To pass, Timeout Error and Receive Error must be 0. 3. Read DPC_AUX_CH_CTL register. To pass, Receive Error must be 0. 4. Read DPB_AUX_CH_DATA[1-5] registers. To pass, they must contain test pattern 2. 5. Read DPC_AUX_CH_DATA[1-5] registers. To pass, they must contain test pattern 1. Clear this bit to 0 after test is done to return DP-AUX to normal operation. Test must be repeated with and without lane reversal to verify DPB-AUX buffer combinations. Only enable one DP-AUX Full Test at a time. To abort a test in progress, write the AUX_CH_CTL Send bits to 0 and Full Test Enable to 0. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test All
27:16	0b RW	**RESERVED:** Project: All Format:
15	0b RW	**DPB_AUX_SHORT_SYNC:** Project: All Output just 16 manchester 0s for sync (otherwise 26)
14	0b RW	**DPB_AUX_CONSTANT_0S_TEST_PATTERN:** Project: All Output never ending Manchester encoded 0s for electrical testing
13	0b RW	**DPB_AUX_TIGHTEN_FREQUENCY_WINDOW:** Project: All Tighten the window of allowable receive frequencies
12	0b RW	**DPB_AUX_LESS_GOOD_SYNC_0S_REQUIRED:** Project: All Check for only 8 good sync 0s instead of 12 when receiving
11:10	0b RW	**DEGLITCH_AMOUNT:** Project: All Default Value: 0b Select clock count for deglitch Value Name Description Project 00b 50 ns 25 clocks - GMBUS type - 50ns at 500MHz cdclk All 01b 125 ns 1/4 2X bit clock divider value - 125ns All 10b 62.5 ns 1/8 2X bit clock divider value - 62.5ns All 11b 31.125 ns 1/16 2X bit clock divider value - 31.125ns All
9	0b RW	**RESERVED_1:** Project: All Format:
8	0b RW	**DPB_AUX_MULTIPLE_RECEIVED_EDGES_ERROR_ENABLE:** Project: All Default Value: 0b Value Name Description Project 0b Okay Multiple edges in window is okay All 1b Error Multiple edges in window is an error All

Bit Range	Default & Access	Description
7:6	0b RW	**DPB_AUX_DEBUG_STATUS_READBACK:** Readback of bit clock divide field gives the error type io_aux_data_syncro and aux_io_data and sm_noa[3:0] and clkregen_baddatastop and mdec_toomuchdata and mdec_notbytealign and mdec_multiedgeinwin and Input data Output data Control state machine Error - bad STOP at end of data Error - too much data Error - data not byte aligned Error - multiple edges inside of window Error - multiple edges outside of window All
5:0	0b RW	**RESERVED_2:** Project: All Format:

3.4.125 DP_C—Offset 64200h

Display Port C Control Register [DevCTG, DevCDV,DevVLV] Display Port C control (dprrega_b0.v ql_displayc1)

Access Method

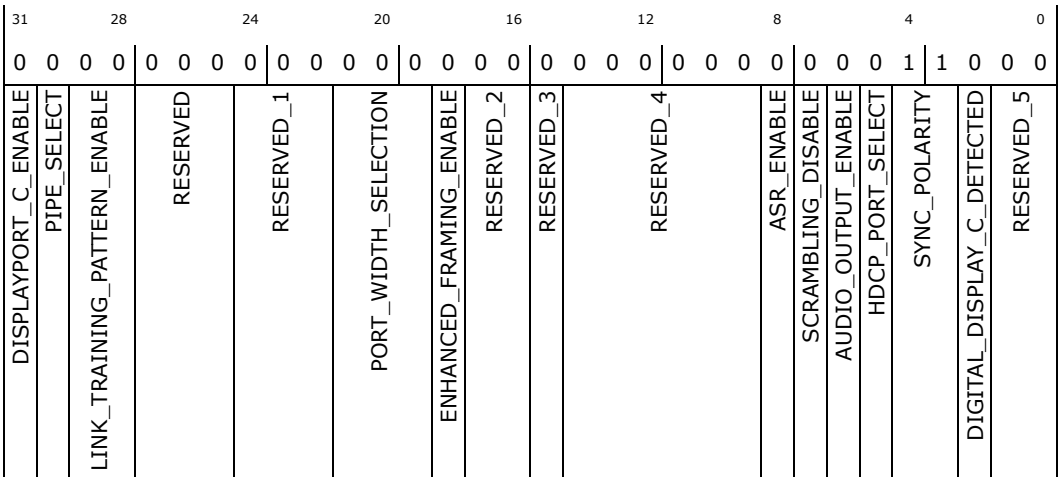
Type: Memory Mapped I/O Register (Size: 32 bits)

DP_C: [GTTMMADR_LSB + 2BF20h] + 64200h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000018h



Bit Range	Default & Access	Description
31	0b RW	**DISPLAYPORT_C_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. 1 = Enable. This bit enables the Display Port C interface. 0 = Disable and tristates the Display Port C interface.

Bit Range	Default & Access	Description
30	0b RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29:28	0b RW	**LINK_TRAINING_PATTERN_ENABLE:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. 00 Pattern 1 enabled: Repetition of D10.2 characters Default. 01 Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. 10 Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times 11 Link not in training: Send normal pixels
27:25	0b RW	**RESERVED:** [DevCDV]: Voltage swing level set [DevCTG]: These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration. 000 0.4V (DEFAULT) 001 0.6V 010 0.8V 011 1.2V RESERVED 1xx RESERVED
24:22	0b RW	**RESERVED_1:** [DevCDV]: Pre-emphasis level set [DevCTG]: These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification. They mirror registers in the PCI express configuration. 000 no pre-emphasis (default) 001 3.5dB pre-emphasis (1.5x) 010 6dB pre-emphasis (2x) 011 9.5dB pre-emphasis (3x) RESERVED 1xx RESERVED
21:19	0b RW	**PORT_WIDTH_SELECTION:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 000 = x1 Mode (Default) 001 = x2 Mode. 010 = RESERVED 011 = x4 Mode. 1xx = RESERVED
18	0b RW	**ENHANCED_FRAMING_ENABLE:** This bit selects enhanced framing. It must be set when HDCP will be used invoked. 0 (Default) Enhanced framing disabled 1 Enhanced framing enabled. Locked once port is enabled. Updates when the port is disabled then re-enabled
17:16	0b RW	**RESERVED_2:** MBZ
15	0b RW	**RESERVED_3:** [DevCDV]: Port reversal [DevCTG]: Locked once port is enabled. Updates when the port is disabled then re-enabled
14:9	0b RW	**RESERVED_4:** MBZ
8	0b RW	**ASR_ENABLE:** [DevVLV2]: this bit enables the Alternate Scrambler Reset capability for eDP port to use alternate scrambler reset value of FFFEh 1 - ASR enable 0 ASR disable
7	0b RW	**SCRAMBLING_DISABLE:** [DevCTG, B-step only, DevCDV]: This bit disables scrambling for this port. 0 = Scrambling enabled (Default) 1 = Scrambling disabled, no SR after initialization at loop 2 of training
6	0b RW	**AUDIO_OUTPUT_ENABLE:** This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to Normal 0 = Audio output disabled 1 = Audio output enabled

Bit Range	Default & Access	Description
5	0b RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port
4:3	11b RW	**SYNC_POLARITY:** Indicates the polarity of Hsync and Vsync. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0b RO	**DIGITAL_DISPLAY_C_DETECTED:** Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port (sDVO B/C) data line at boot. 0 = digital display not detected during initialization (Default) 1 = digital display detected during initialization AccessType: Read only
1:0	0b RW	**RESERVED_5:** MBZ

3.4.126 DPC_AUX_CH_CTL—Offset 64210h

Display Port C AUX Channel Control [DevCTG] AuxC Data1 (dprrega_b0.v auxc_dpr_data1, ql_auxc_d1)

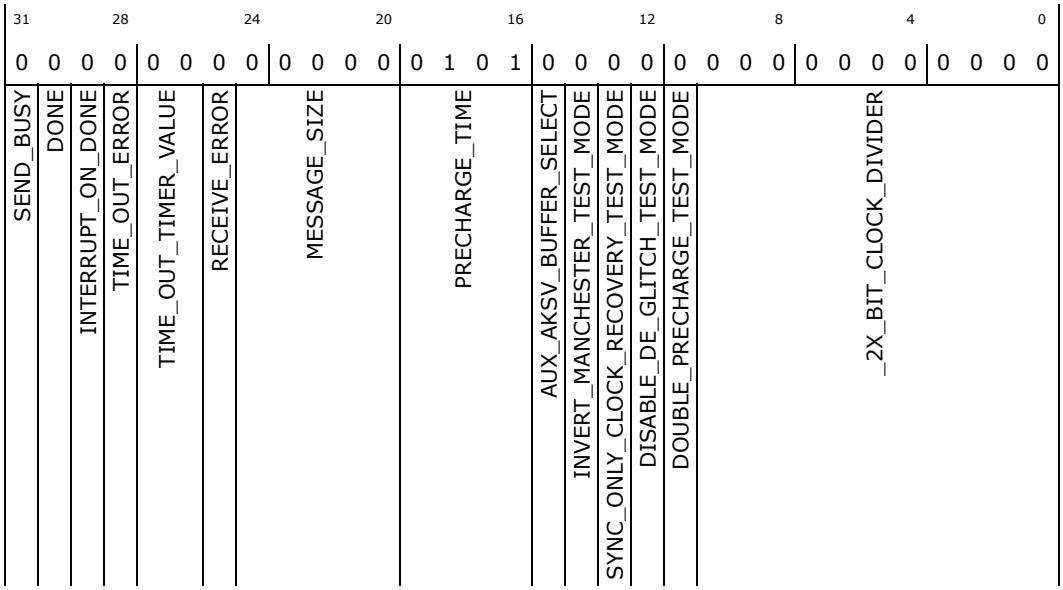
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPC_AUX_CH_CTL: [GTTMMADR_LSB + 2BF20h] + 64210h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00050000h



Bit Range	Default & Access	Description
31	0b RW	**SEND_BUSY:** Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	0b RW/1C	**DONE:** A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
29	0b RW	**INTERRUPT_ON_DONE:** Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	0b RW/1C	**TIME_OUT_ERROR:** A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
27:26	0b RW	**TIME_OUT_TIMER_VALUE:** 00: 400us (default) 01: 600us 10: 800us 11: 1600us The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.
25	0b RW/1C	**RECEIVE_ERROR:** A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
24:20	0b RW	**MESSAGE_SIZE:** This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only only when the done bit is set and timeout or receive error has not occurred. Sync/ Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or)20 are not allowed.

Bit Range	Default & Access	Description
19:16	0101b RW	**PRECHARGE_TIME:** Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example: For 12us precharge, program 6 (12us/2us).
15	0b RW	**AUX_AKSV_BUFFER_SELECT:** This bit selects whether some of the data to be written over Display Port AUX comes from the Aksv buffer for HDCP authentication, or all from the AUX Data registers. Set this bit before initiating a transaction to write Aksv to the Display Port sink. All AUX protocol must be followed and Message Size set to 9 bytes. The first DWord transmitted will be from the AUX Data Register 1 for the header, then the DP_AUX_CH_AKSV_HI, then the last byte from DP_AUX_CH_AKSV_LO. The sink response is read back as usual from the AUX Data registers. More than one AUX channel can select to use the Aksv buffer simultaneously. 0 (Default) Use AUX Data registers for regular data transmission 1 Use Aksv Buffer for part of the data transmission.
14	0b RW	**INVERT_MANCHESTER_TEST_MODE:** 1 = Manchester code rising edge mid-clk signifies one (test mode) 0 = Manchester code rising edge mid-clk signifies zero (default)
13	0b RW	**SYNC_ONLY_CLOCK_RECOVERY_TEST_MODE:** 1 = Only recover clock during sync pattern (test mode) 0 = Recover clock during sync pattern and data phase (default)
12	0b RW	**DISABLE_DE_GLITCH_TEST_MODE:** 1 = Disable serial input de-glitch logic (test mode) 0 = Enable serial input de-glitch logic (default)
11	0b RW	**DOUBLE_PRECHARGE_TEST_MODE:** 1 = Precharge time is doubled 0 = Precharge time is as programmed
10:0	0b RW	**_2X_BIT_CLOCK_DIVIDER:** Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). [DevCTG-A] the input clock is cdclk. [DevCTG-B] the input clock is hrawclk. Example: For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/ 2MHz).

3.4.127 DPC_AUX_CH_DATA1—Offset 64214h

Display Port C AUX Data Register 1 [DevCTG, DevCDV] AuxC Data1 (dprrega_b0.v auxc_dpr_data1, ql_auxc_d1)

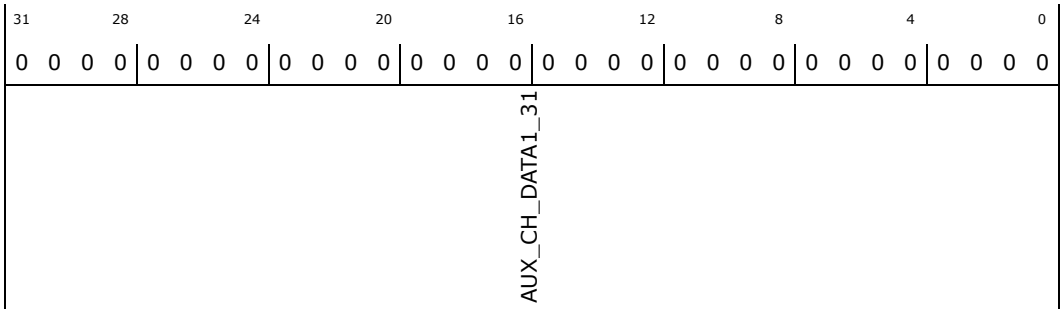
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPC_AUX_CH_DATA1: [GTTMMADR_LSB + 2BF20h] + 64214h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**AUX_CH_DATA1_31:** 0]: The first DWord of the message. The MSbyte is transmitted first. Reads will give the response data after transaction complete.

3.4.128 DPC_AUX_CH_DATA2—Offset 64218h

Display Port C AUX Data Register 2 [DevCTG, DevCDV] AuxC Data2 (dprrega_b0.v auxc_dpr_data2, ql_auxc_d2)

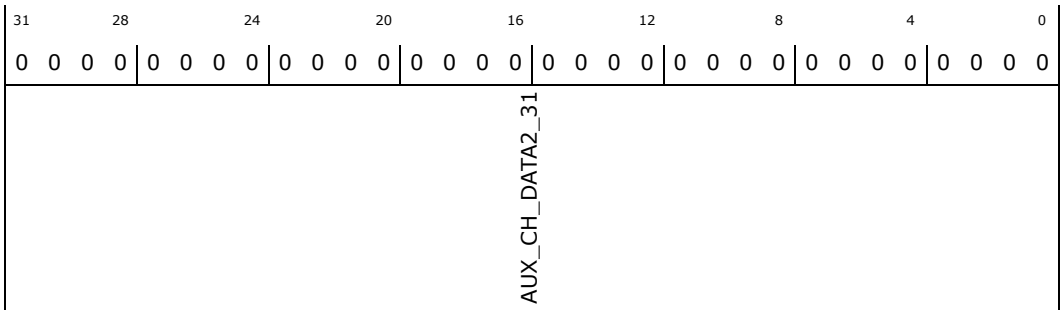
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPC_AUX_CH_DATA2: [GTTMMADR_LSB + 2BF20h] + 64218h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**AUX_CH_DATA2_31:** 0]: The second DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

3.4.129 DPC_AUX_CH_DATA3—Offset 6421Ch

Display Port C AUX Data Register 3 [DevCTG, DevCDV] AuxC Data3 (dprrega_b0.v auxc_dpr_data3, ql_auxc_d3)

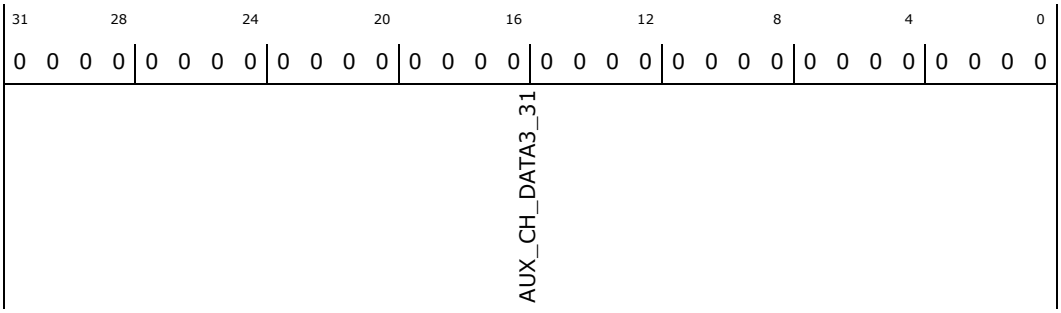
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPC_AUX_CH_DATA3: [GTTMMADR_LSB + 2BF20h] + 6421Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**AUX_CH_DATA3_31:** 0]: The third DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

3.4.130 DPC_AUX_CH_DATA4—Offset 64220h

Display Port C AUX Data Register 4 [DevCTG, DevCDV] AuxC Data4 (dprrega_b0.v auxc_dpr_data4, ql_auxc_d4)

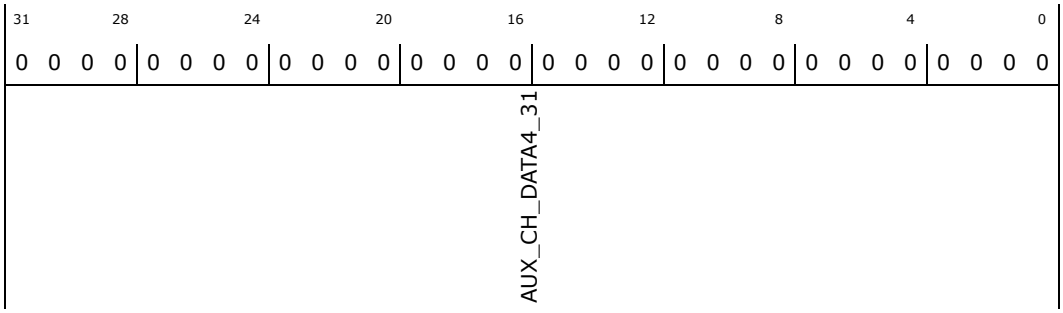
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPC_AUX_CH_DATA4: [GTTMMADR_LSB + 2BF20h] + 64220h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**AUX_CH_DATA4_31:** 0]: The fourth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

3.4.131 DPC_AUX_CH_DATA5—Offset 64224h

Display Port C AUX Data Register 5 [DevCTG, DevCDV] AuxC Data5 (dprrega_b0.v auxc_dpr_data5, ql_auxc_d5)

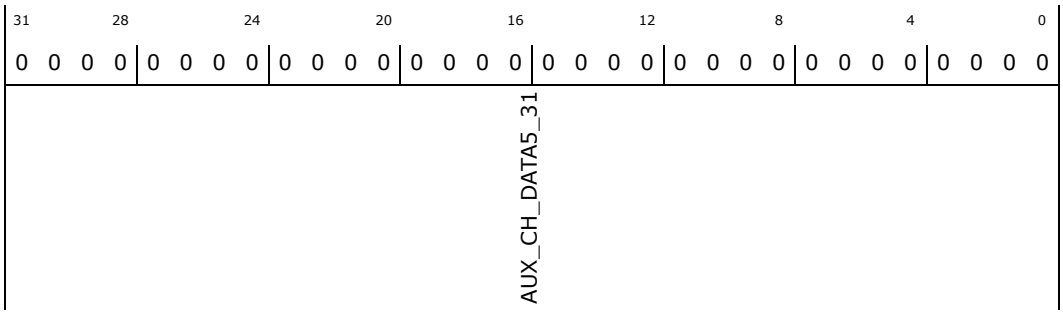
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPC_AUX_CH_DATA5: [GTTMMADR_LSB + 2BF20h] + 64224h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**AUX_CH_DATA5_31:** 0]: The fifth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

3.4.132 DPC_AUX_TST—Offset 64228h

Display Port C AUX Test Register

Access Method

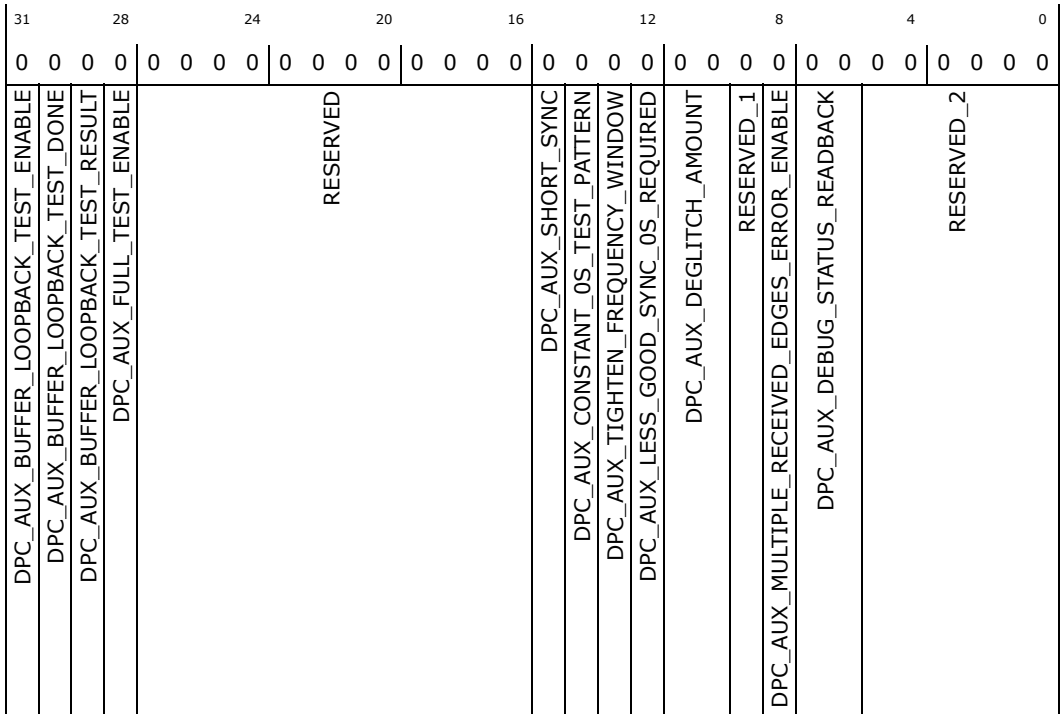
Type: Memory Mapped I/O Register (Size: 32 bits)

DPC_AUX_TST: [GTTMMADR_LSB + 2BF20h] + 64228h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**DPC_AUX_BUFFER_LOOPBACK_TEST_ENABLE:** Project: All Default Value: 0b See DPB description. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test. All
30	0b RO	**DPC_AUX_BUFFER_LOOPBACK_TEST_DONE:** Project: All Default Value: 0b AccessType: Read Only See DPB description. Value Name Description Project 0b Not Done Test not done. DP-AUX Buffer Loopback Test Result is not valid All 1b Done Test done. DP-AUX Buffer Loopback Test Result is now valid All
29	0b RO	**DPC_AUX_BUFFER_LOOPBACK_TEST_RESULT:** Project: All Default Value: 0b AccessType: Read Only See description for DPB-AUX Buffer Loopback Test Result Value Name Description Project 0b Pass Pass All 1b Fail Fail All
28	0b RW	**DPC_AUX_FULL_TEST_ENABLE:** Project: All Default Value: 0b See DPB description. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test All
27:16	0b RW	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Description
15	0b RW	**DPC_AUX_SHORT_SYNC:** Project: All See DPB description.
14	0b RW	**DPC_AUX_CONSTANT_0S_TEST_PATTERN:** Project: All See DPB description.
13	0b RW	**DPC_AUX_TIGHTEN_FREQUENCY_WINDOW:** Project: All See DPB description.
12	0b RW	**DPC_AUX_LESS_GOOD_SYNC_0S_REQUIRED:** Project: All See DPB description.
11:10	0b RW	**DPC_AUX_DEGLITCH_AMOUNT:** Project: All Default Value: 0b See DPB description. Value Name Description Project 00b 50 ns 25 clocks - GMBUS type - 50ns at 500MHz cdclk All 01b 125 ns 1/4 2X bit clock divider value - 125ns All 10b 62.5 ns 1/8 2X bit clock divider value - 62.5ns All 11b 31.125 ns 1/16 2X bit clock divider value - 31.125ns All
9	0b RW	**RESERVED_1:** Project: All Format:
8	0b RW	**DPC_AUX_MULTIPLE_RECEIVED_EDGES_ERROR_ENABLE:** Project: All Default Value: 0b Value Name Description Project 0b Okay Multiple edges in window is okay All 1b Error Multiple edges in window is an error All
7:6	0b RW	**DPC_AUX_DEBUG_STATUS_READBACK:** Project: All Default Value: 0b Value Name Description Project 00b Program Readback of bit clock divide field gives the programmed clock frequency All 01b Recover Readback of bit clock divide field gives the recovered clock frequency All 10b Error Type Readback of bit clock divide field gives the error type All
5:0	0b RW	**RESERVED_2:** Project: All Format:

3.4.133 STREAM_A_LPE_AUD_CONFIG—Offset 65000h

LPE Audio Configuration

Access Method

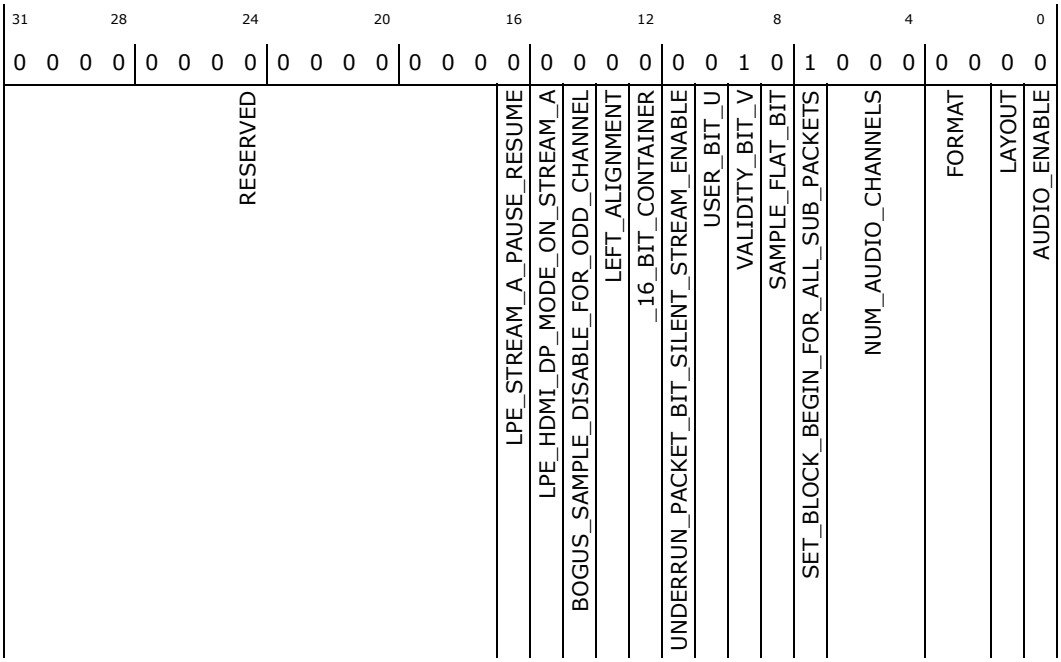
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_CONFIG: [GTTMMADR_LSB + 2BF20h] + 65000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000280h



Bit Range	Default & Access	Description
31:17	0b RW	**RESERVED:** Reserved.
16	0b RW	**LPE_STREAM_A_PAUSE_RESUME:** DMA pause fetching at the boundary of buffers when this bit is set, and resume fetching when this bit is cleared. 1- DMA stop requesting more audio sample from buffer A,B,C,D after reading and depleting all data from current buffer 0- DMA resume requesting data from the next available buffer (A,B,C,D). Programming note: this bit should not be used by SW driver. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically
15	0b RW	**LPE_HDMI_DP_MODE_ON_STREAM_A:** 1 = DP mode 0 = HDMI mode (default)
14	0b RW	**BOGUS_SAMPLE_DISABLE_FOR_ODD_CHANNEL:** When number of channels in a sample is odd (3, 5, or 7) source application may pad a bogus sample to the next even number of channels. If this bit is set there is no padding in input buffer1= No bogus sample present in buffer for odd number of channels 0= Bogus sample present in buffer for odd number of channels (default)
13	0b RW	**LEFT_ALIGNMENT:** When input buffer is in 32-bit container mode. If this bit is set the MSB of audio sample is aligned bit 31 of the container if this bit is clear MSB of audio sample is aligned with bit 23 of the container.1= MSB is bit 31 of 32-bit container 0= MSB is bit 23 of 32-bit container (default)
12	0b RW	**_16_BIT_CONTAINER:** When this bit is set 16-bit sample is stored in 16-bit container format. When it is clear container is 32-bit for each sample regardless of valid bits (default)1= 16-bit container 0= 32-bit container

Bit Range	Default & Access	Description
11	0b RW	**UNDERRUN_PACKET_BIT_SILENT_STREAM_ENABLE:** Set this bit will enable HW to send valid zero-filled packet with Sample flat bit set when no sample buffer is available, NCTS packets (or Times stamp packet) are sent to keep sink in sync even no audio sound will heard.1= send underrun packets (silent stream) 0= send null packets (default) Programming note: SW driver shall always set silent stream bit. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically.
10	0b RW	**USER_BIT_U:** HW will clear this bit in each sub-frames it sends, But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= sey U bit in sub-frame 0= clear U bit in sub-frame (default)
9	1b RW	**VALIDITY_BIT_V:** HW will set this bit in both each sub-frames it sends. But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= Set V bit in sub-frame (default) 0= clear V bit in sub-frame. For debug or testing
8	0b RW	**SAMPLE_FLAT_BIT:** When set the sample flat bit will be set in all HDMI sub-packets. 1= flat bit is set for valid sample 0= flat bit is not set for valid sample (default)
7	1b RW	**SET_BLOCK_BEGIN_FOR_ALL_SUB_PACKETS:** Controls the B bit in the header of only the first Audio Packet /frame of a 192 frame 60958 block in Layout 1 mode. This bit only applies to LPE HDMI mode. 0: The B bit will be set only for sub-packet 0 1: The B bit in the Audio sample packet header will be set for all valid sub-packets. (default)
6:4	0b RW	**NUM_AUDIO_CHANNELS:** 000: 2 channels (stereo) 001: 3 channels 010: 4 channels 011: 5 channels 100: 6 channels 101: 7 channels 110: 8 channels Note: When disable_bogus sample bit is clear HW will always treat odd number of channels similar to the next higher even number. Thus 3 is similar to 4, 5 to 6 and 7 to 8. This is because SW ensures that an even number of samples are packed in the audio buffers. Programming note: Bit 6 of of this field is a write only bit. When reads back, it always returns zero. Ensure to write bit 6 to 1?b1 when programming for 6/7/8 audio channels.
3:2	0b RW	**FORMAT:** 00: L-PCM or IEC 61937 01: High Bit Rate IEC 61937 stream packet (not supported) 10: One Bit Audio Sample packet (not supported) 11: DST Audio Sample packet (not supported)
1	0b RW	**LAYOUT:** 0: Layout 0 (2-ch) 1: Layout 1 (3-8 ch) Note: Layout bit does not matter for HBR
0	0b RW	**AUDIO_ENABLE:** Controls generation of N/CTS and transmission of audio sample packets. 0: Audio sample packets are not transmitted, CTS calculation/transmission is disabled 1: Audio sample packets are transmitted and CTS calculation is enabled When enable audio unit will wait until the next vertical blank period before sending out the audio packets. When disable, audio unit may continue to send audio packet until the end of current active video frame before stopping.

3.4.134 STREAM_A_LPE_AUD_CH_STATUS_0—Offset 65008h

Audio Channel Status Attributes 0

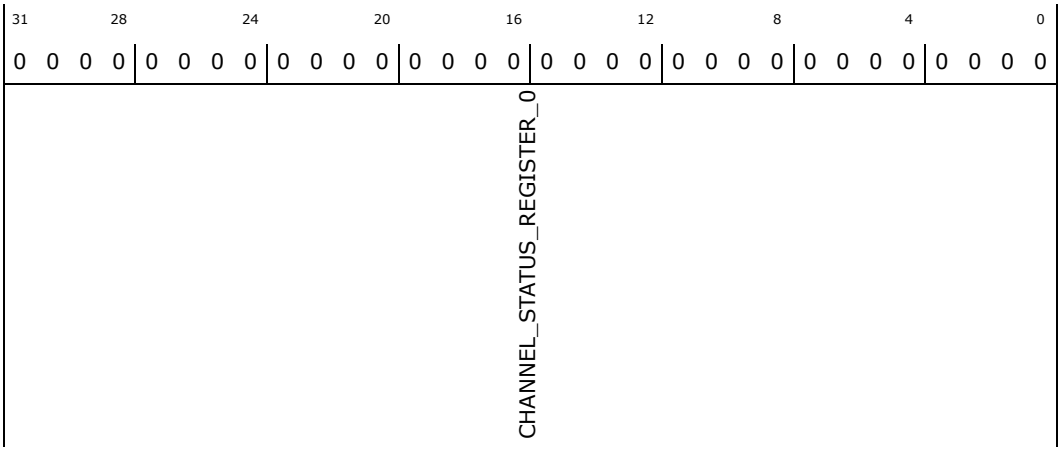
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_CH_STATUS_0: [GTTMMADR_LSB + 2BF20h] + 65008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**CHANNEL_STATUS_REGISTER_0:** . These bits are transmitted as attributes of audio packets

3.4.135 STREAM_A_LPE_AUD_CH_STATUS_1—Offset 6500Ch

Audio Channel Status Attributes 1

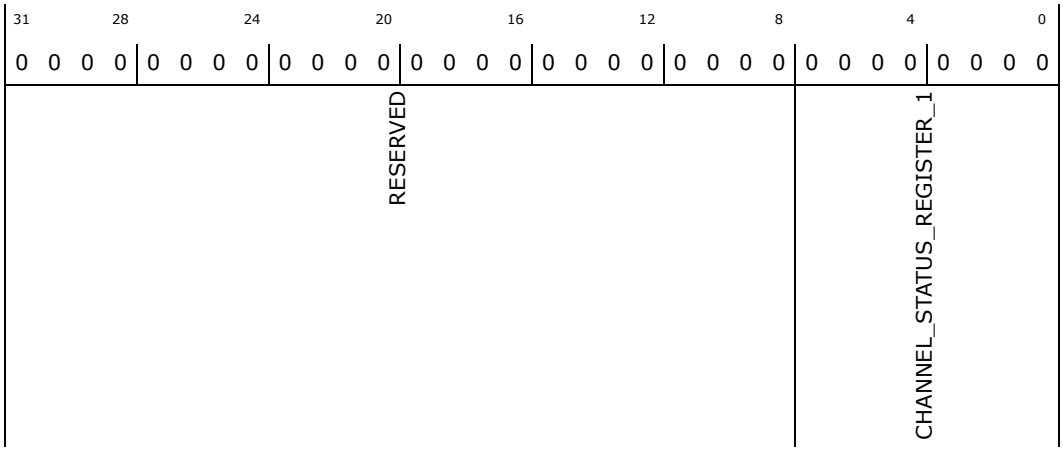
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_CH_STATUS_1: [GTTMMADR_LSB + 2BF20h] + 6500Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**RESERVED:** Reserved.
7:0	0b RW	**CHANNEL_STATUS_REGISTER_1:** . These bits are transmitted as attributes of audio packets. There is only 8 bits valid in this register.

3.4.136 STREAM_A_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65010h

Audio HDMI CTS Register (DP Maud)

Access Method

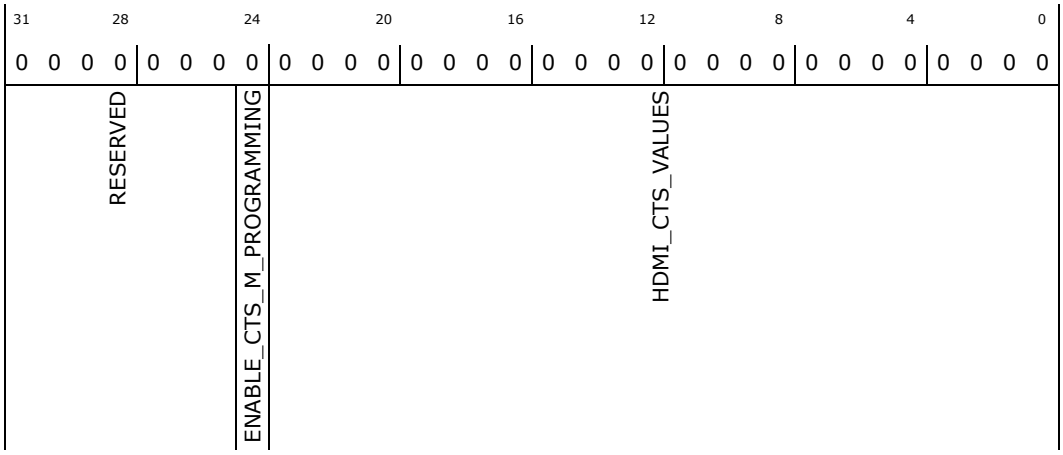
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_HDMI_CTS_DP_MAUD: [GTTMMADR_LSB + 2BF20h] + 65010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RW	**RESERVED:** Reserved.
24	0b RW	**ENABLE_CTS_M_PROGRAMMING:** 1 = Enable CTS/M programming 0 = Disable CTS/M programming
23:0	0b RW	**HDMI_CTS_VALUES:** These are bits [23:0] of programmable HDMI CTS values (or DP Maud) that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

3.4.137 STREAM_A_LPE_AUD_HDMI_N_DP_NAUD—Offset 65014h

Audio HDMI N Register (DP Naud)

Access Method

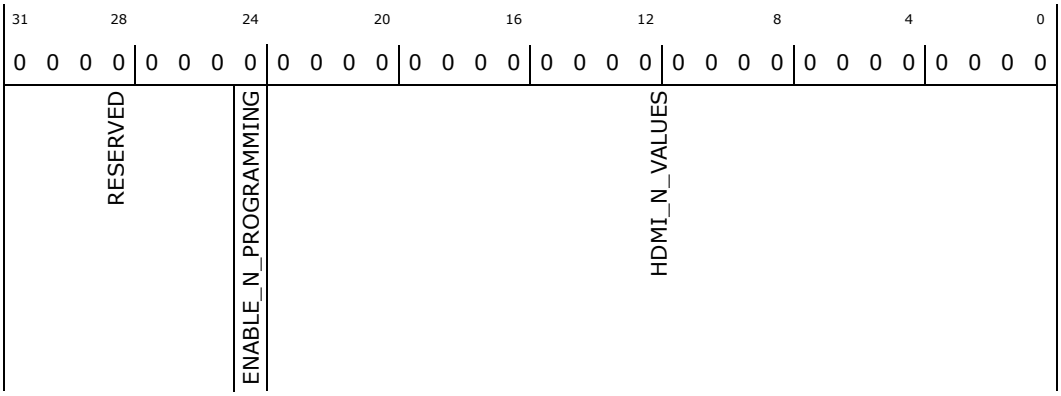
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_HDMI_N_DP_NAUD: [GTTMMADR_LSB + 2BF20h] + 65014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RW	**RESERVED:** Reserved.
24	0b RW	**ENABLE_N_PROGRAMMING:** 1 = Enable N programming 0 = Disable N programming
23:0	0b RW	**HDMI_N_VALUES:** These are bits [23:0] of programmable HDMI N (or DP Naud) values that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

3.4.138 STREAM_A_LPE_AUD_BUFFER_CONFIG—Offset 65020h

LPE Audio buffer config

Access Method

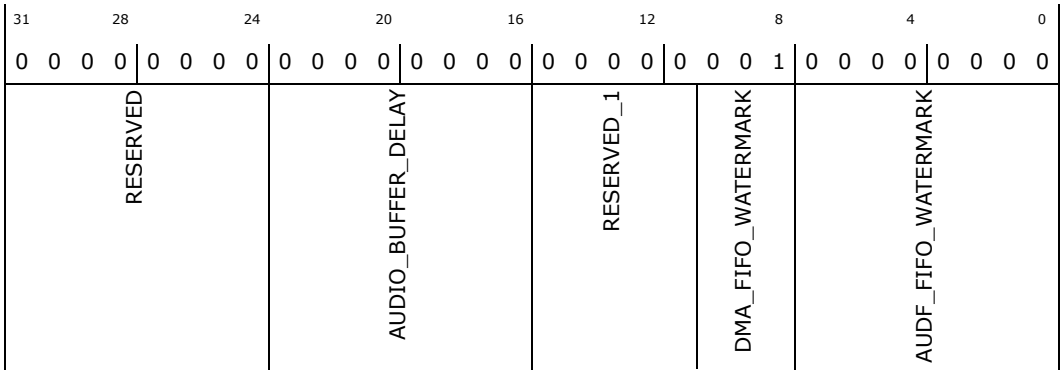
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_BUFFER_CONFIG: [GTTMMADR_LSB + 2BF20h] + 65020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000100h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**AUDIO_BUFFER_DELAY:** This field specifies a delay in number of video frames that the audio controller will count off when audio enable bit is set before start transmitting audio sample.
15:11	0b RW	**RESERVED_1:** Reserved.
10:8	001b RW	**DMA_FIFO_WATERMARK:** Audio unit has a 8x64 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in SWORDs (64B). When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI/DP packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again. Default value is 1 cacheline (SW).
7:0	0b RW	**AUDF_FIFO_WATERMARK:** Audio unit has a 96x8 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in DWORDs. When enable and sample buffer is available audio unit will fetch samples until this FIFO occupancy is above the watermark then it waits until HDMI packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again

3.4.139 STREAM_A_LPE_AUD_BUF_CH_SWP—Offset 65024h

Audio Sample Swapping

Access Method

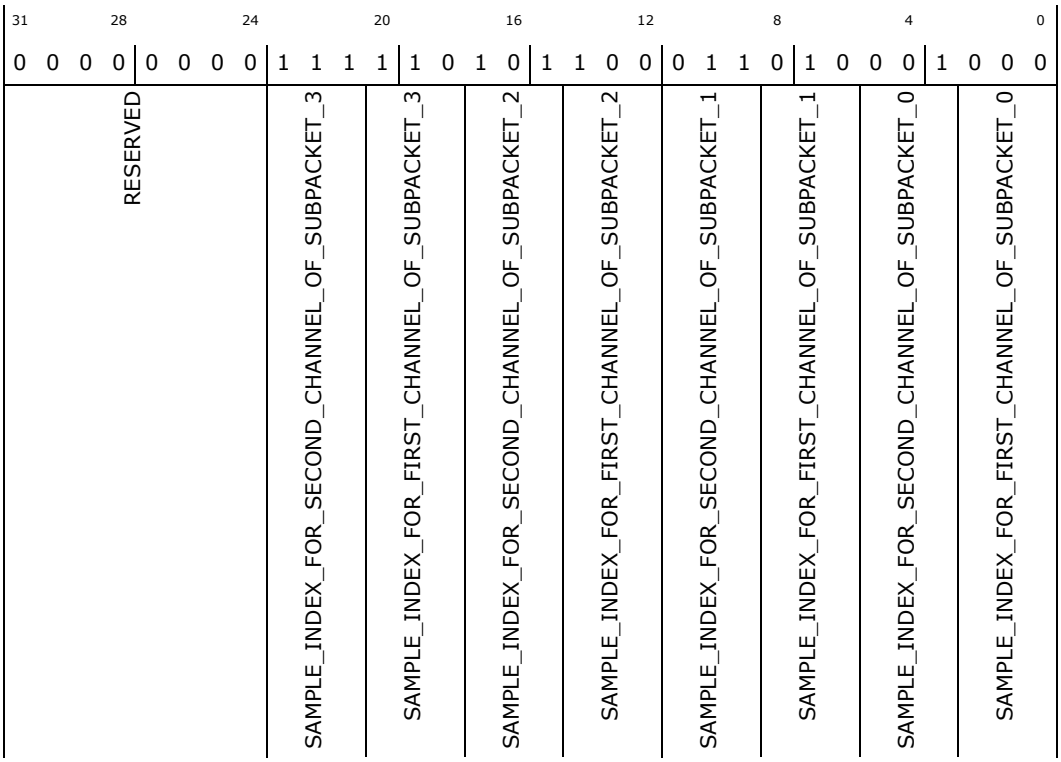
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_BUF_CH_SWP: [GTTMMADR_LSB + 2BF20h] + 65024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00FAC688h



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Reserved.
23:21	111b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 3 in a HDMI audio packet
20:18	110b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
17:15	101b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
14:12	100b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet

Bit Range	Default & Access	Description
11:9	011b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 1 in a HDMI audio packet
8:6	010b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
5:3	001b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
2:0	0b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet

3.4.140 STREAM_A_LPE_AUD_BUF_A_ADDR—Offset 65040h

Address for Audio Buffer A

Access Method

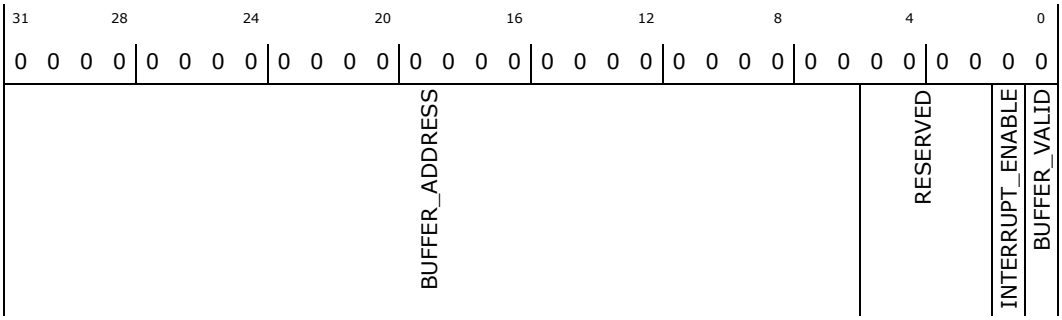
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_BUF_A_ADDR: [GTTMMADR_LSB + 2BF20h] + 65040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.4.141 STREAM_A_LPE_AUD_BUF_A_LENGTH—Offset 65044h

Length for Audio Buffer A

Access Method

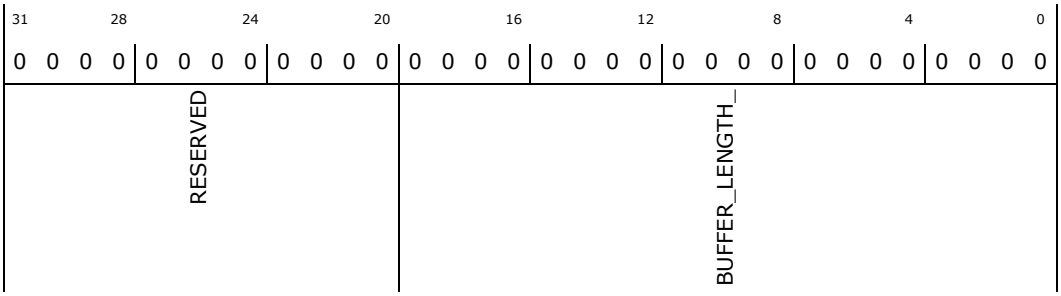
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_BUF_A_LENGTH: [GTTMMADR_LSB + 2BF20h] + 65044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

3.4.142 STREAM_A_LPE_AUD_BUF_B_ADDR—Offset 65048h

Address for Audio Buffer B

Access Method

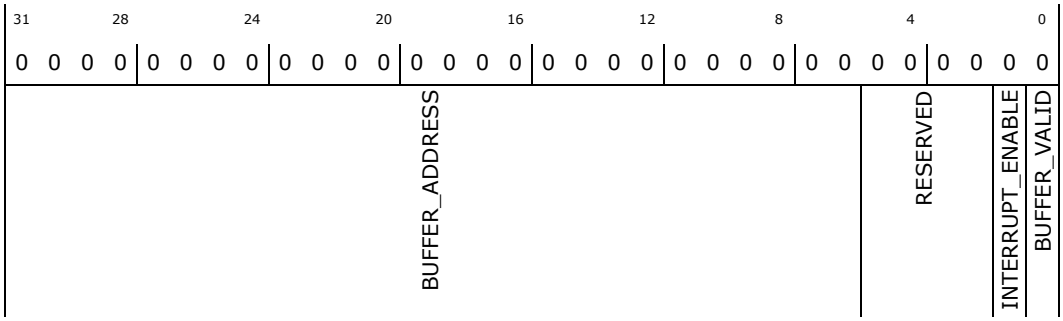
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_BUF_B_ADDR: [GTTMMADR_LSB + 2BF20h] + 65048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.4.143 STREAM_A_LPE_AUD_BUF_B_LENGTH—Offset 6504Ch

Length for Audio Buffer B

Access Method

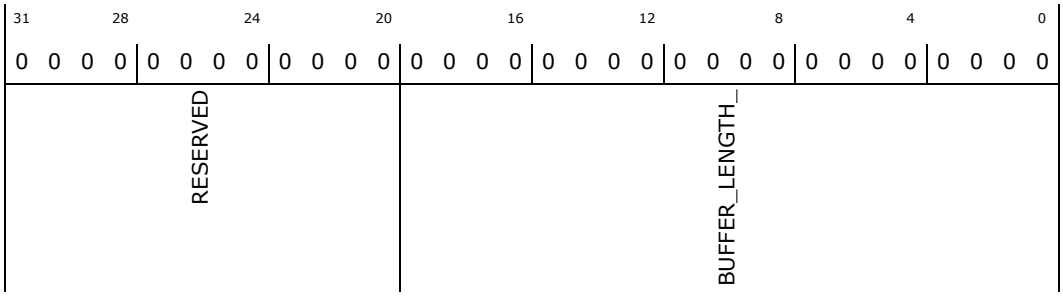
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_BUF_B_LENGTH: [GTTMMADR_LSB + 2BF20h] + 6504Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

3.4.144 STREAM_A_LPE_AUD_BUF_C_ADDR—Offset 65050h

Address for Audio Buffer C

Access Method

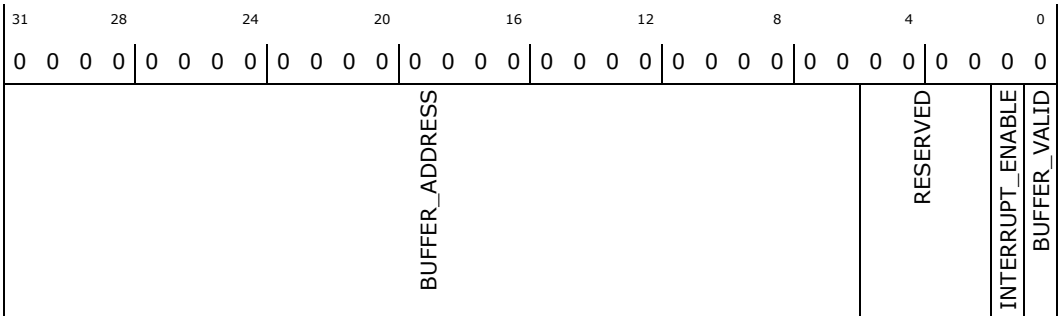
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_BUF_C_ADDR: [GTTMMADR_LSB + 2BF20h] + 65050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.4.145 STREAM_A_LPE_AUD_BUF_C_LENGTH—Offset 65054h

Length for Audio Buffer C

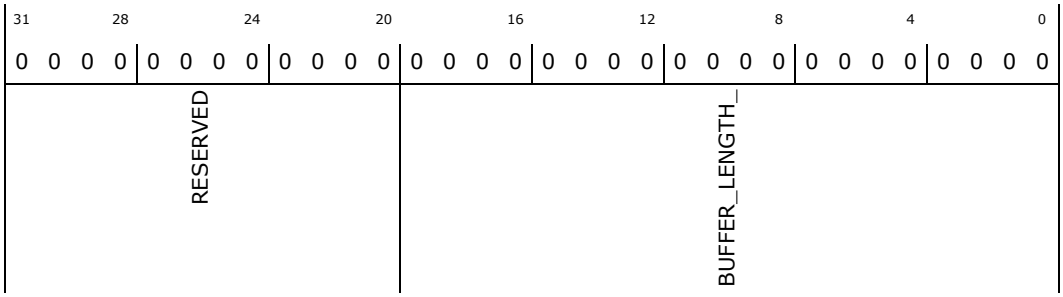
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_BUF_C_LENGTH: [GTTMMADR_LSB + 2BF20h] + 65054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

3.4.146 STREAM_A_LPE_AUD_BUF_D_ADDR—Offset 65058h

Address for Audio Buffer D

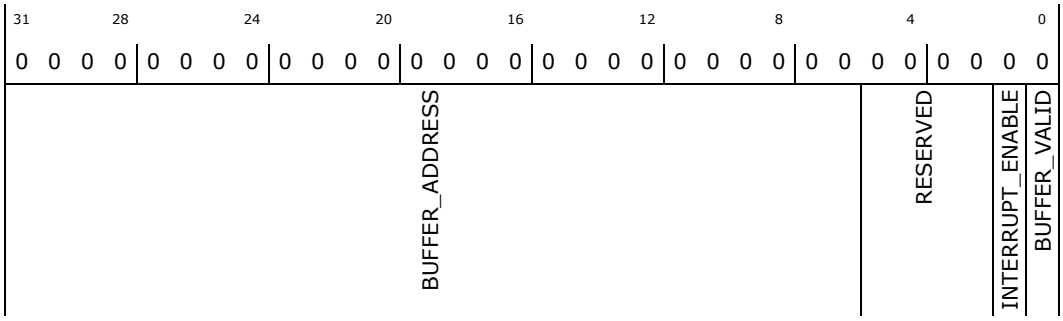
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_BUF_D_ADDR: [GTTMMADR_LSB + 2BF20h] + 65058h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.4.147 STREAM_A_LPE_AUD_BUF_D_LENGTH—Offset 6505Ch

Length for Audio Buffer D

Access Method

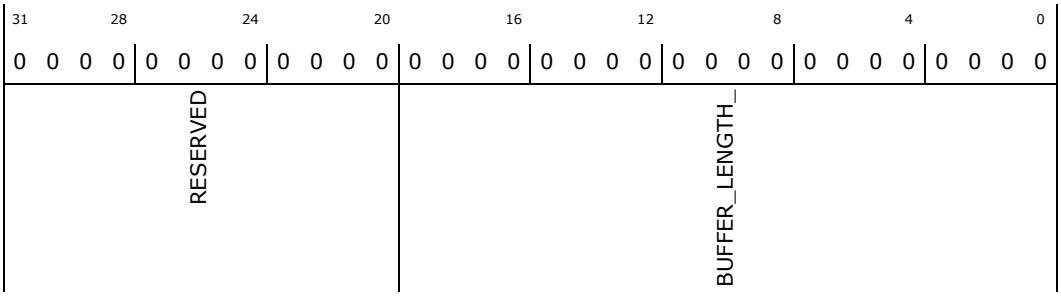
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_BUF_D_LENGTH: [GTTMMADR_LSB + 2BF20h] + 6505Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

3.4.148 STREAM_A_LPE_AUD_CNTL_ST—Offset 65060h

LPE Audio Control State Register

Access Method

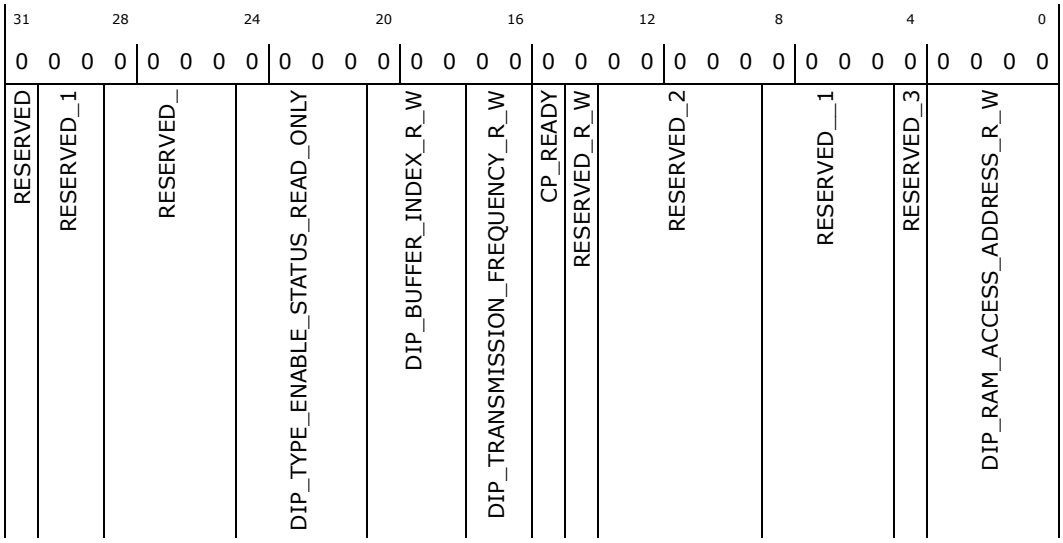
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_CNTL_ST: [GTTMMADR_LSB + 2BF20h] + 65060h

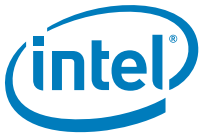
GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** Reserved.
30:29	0b RW	**RESERVED_1:** Reserved.
28:25	0b RW	**RESERVED_:** for later DIP type if needed: Must be 0.
24:21	0b RW	**DIP_TYPE_ENABLE_STATUS_READ_ONLY:** These bits reflects the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling an DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. XXX1 = Audio DIP enable status (Default = disabled) XX1X = Generic 1 (ACP) DIP enable status (Default = disabled) X1XX = Generic 2 DIP enable status, can be used by ISRC1 or ISRC2 (Default = disabled) 1XXX = Reserved
20:18	0b RW	**DIP_BUFFER_INDEX_R_W:** This field is used during read or write of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0 s. 000 = (Default) Audio DIP (31 bytes of address space, 13 bytes of data) 001 = Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) 010 = Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) 011 = Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) 1XX = reserved



Bit Range	Default & Access	Description
17:16	0b RW	**DIP_TRANSMISSION_FREQUENCY_R_W:** These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. 00 = Disabled (Default) 01 = once per frame 10 = Send once 11 = Best effort (Send at least every other vsync)
15	0b RW	**CP_READY:** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. 0 = CP request pending or not ready to receive requests (default) 1 = CP request ready CP_ready bit is programmable through Bit 14 for [DevCL, DevBLC]. CP_ready bit is programmable through Bit 15 for [DevCTG]. Bit 15 Reserved for [DevCL, DevBLC].
14	0b RW	**RESERVED_R_W:** ELD valid: This bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit.0 = ELD data invalid (default, when writing ELD data, set 0 by software) 1 = ELD data valid (Set by video software only) ELD bit is programmable through Bit 13 for [DevCL, DevBLC]. ELD bit is programmable through Bit 14 for [DevCTG].
13:9	0b RW	**RESERVED_2:** ELD buffer size (read only)10000 = This field reflects the size of the ELD buffer in DWORDs 13:9 reflects ELD buffer size for [DevCTG]. 12:9 reflects ELD buffer size for [DevCL, DevBLC].
8:5	0b RW	**RESERVED__1:** ELD access address (R/W): Selects the DWORD address for access to the ELD buffer (48 bytes). The value wraps back to zero when incremented past the max addressing value 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.
4	0b RW	**RESERVED_3:** ELD ACK: Acknowledgement from the audio driver that ELD read has been completed
3:0	0b RW	**DIP_RAM_ACCESS_ADDRESS_R_W:** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

3.4.149 STREAM_A_LPE_AUD_HDMI_STATUS—Offset 65064h

LPE Audio Status

Access Method

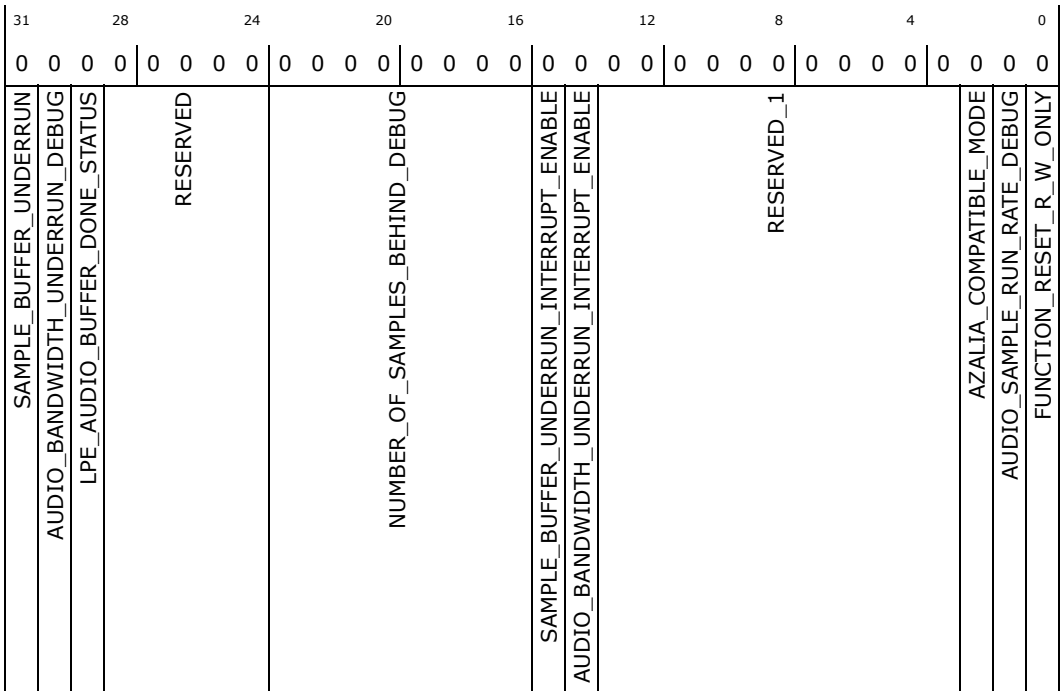
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_HDMI_STATUS: [GTTMMADR_LSB + 2BF20h] + 65064h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/1C	**SAMPLE_BUFFER_UNDERRUN:** This bit indicates an underrun in the sample buffer to HDMI controller when it needs to send. This bit is set at the last line of active video when there are no more sample in any valid buffers and HDMI audio unit has not satisfied number of audio samples intended in that video frame. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
30	0b RW/1C	**AUDIO_BANDWIDTH_UNDERRUN_DEBUG:** This bit indicates an underrun of audio samples at HDMI audio packet assembly even there is still available sample buffers. Audio bandwidth underrun should not happen in normal functionality but it may happen when audio setting is inappropriate and/or memory bus was blocked by other clients, etc... This bit is set at the last line of active video when there is valid samples in a valid buffer and HDMI audio unit has not satisfied number of audio samples intended in that video frame Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
29	0b RW/1C	**LPE_AUDIO_BUFFER_DONE_STATUS:** This bit is set when a LPE audio buffer is completed transferred all of its data to LPE audio unit. This bit is clear when write 1 to it AccessType: One to Clear
28:24	0b RW	**RESERVED:** Reserved.
23:16	0b RO	**NUMBER_OF_SAMPLES_BEHIND_DEBUG:** This field is read only to get the number of audio samples that controller needs to load and send at the time of reading. AccessType: Read Only

Bit Range	Default & Access	Description
15	0b RW	**SAMPLE_BUFFER_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line buffer underrun interrupt when sample buffer underrun status is detected 0 = LPE sample Buffer Underrun Interrupt Disabled 1 = LPE sample Buffer Underrun Interrupt Enabled
14	0b RW	**AUDIO_BANDWIDTH_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line bandwidth underrun interrupt when bandwidth underrun status is detected 0 = LPE Bandwidth Underrun Interrupt Disabled 1 = LPE Bandwidth Underrun Interrupt Enabled
13:3	0b RW	**RESERVED_1:** Reserved.
2	0b RW	**AZALIA_COMPATIBLE_MODE:** This bit is to enable the vucp, PR, ECC to be generated in the Azalia way 0 = Disable Azalia compatible mode on vucp, PR, ECC 1 = Enable Azalia compatible mode on vucp, PR, ECC
1	0b RW	**AUDIO_SAMPLE_RUN_RATE_DEBUG:** When set it allows to fetch sample 128 times than the real sample rate to allow a faster drain of sample buffers.
0	0b RW	**FUNCTION_RESET_R_W_ONLY:** Write 1 to this bit will reset hardware within audio unit without needs of reset the full display controller. The FIFO and pointers will be reset and audio registers will be reset to default values. Write 0 will put the unit back to idle and ready to be programmed again.

3.4.150 STREAM_A_LPE_AUD_HDMIW_INFOFR—Offset 65068h

Audio HDMI Data Island Packet Data

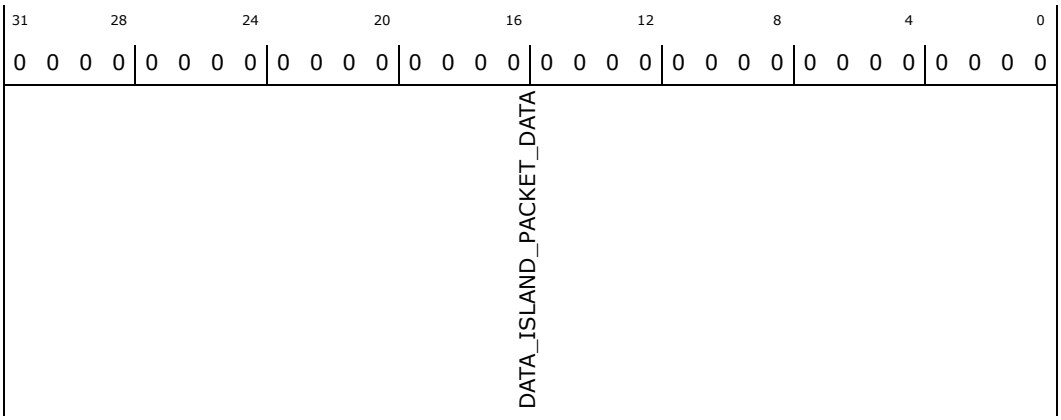
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_A_LPE_AUD_HDMIW_INFOFR: [GTTMMADR_LSB + 2BF20h] + 65068h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**DATA_ISLAND_PACKET_DATA:** When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis

3.4.151 STREAM_B_LPE_AUD_CONFIG—Offset 65800h

LPE Audio Configuration

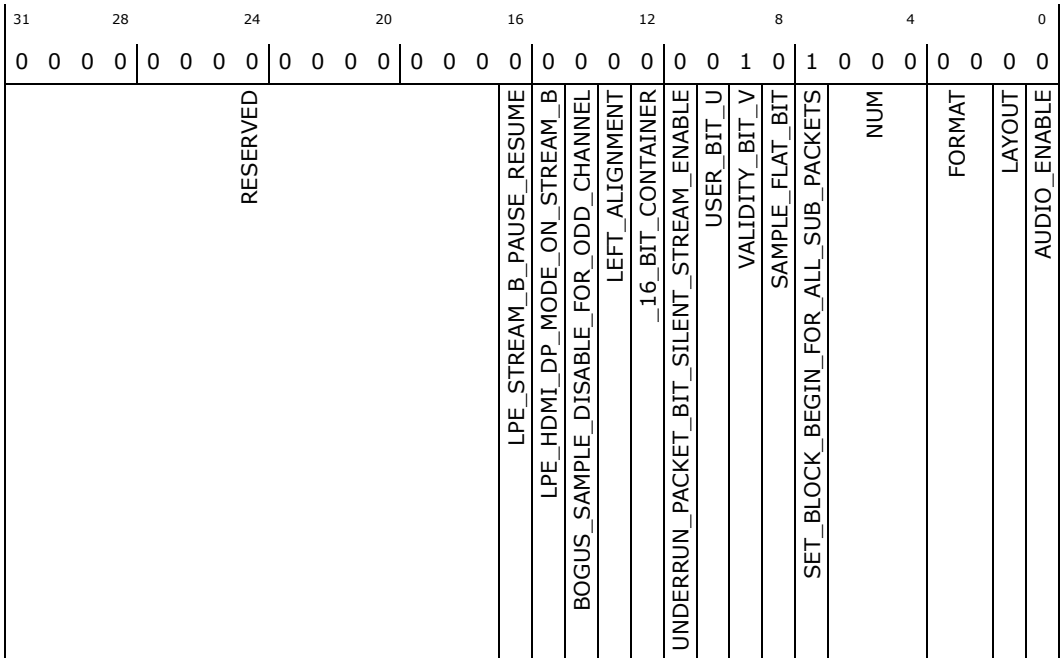
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

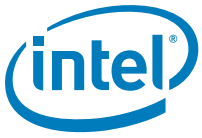
STREAM_B_LPE_AUD_CONFIG: [GTTMMADR_LSB + 2BF20h] + 65800h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000280h



Bit Range	Default & Access	Description
31:17	0b RW	**RESERVED:** Reserved.



Bit Range	Default & Access	Description
16	0b RW	**LPE_STREAM_B_PAUSE_RESUME:** DMA pause fetching at the boundary of buffers when this bit is set, and resume fetching when this bit is cleared. 1- DMA stop requesting more audio sample from buffer A,B,C,D after reading and depleting all data from current buffer 0- DMA resume requesting data from the next available buffer (A,B,C,D). Programming note: this bit should not be used by SW driver. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically.
15	0b RW	**LPE_HDMI_DP_MODE_ON_STREAM_B:** 1= DP mode 0 = HDMI mode (default)
14	0b RW	**BOGUS_SAMPLE_DISABLE_FOR_ODD_CHANNEL:** When number of channels in a sample is odd (3, 5, or 7) source application may pad a bogus sample to the next even number of channels. If this bit is set there is no padding in input buffer1= No bogus sample present in buffer for odd number of channels 0= Bogus sample present in buffer for odd number of channels (default)
13	0b RW	**LEFT_ALIGNMENT:** When input buffer is in 32-bit container mode. If this bit is set the MSB of audio sample is aligned bit 31 of the container if this bit is clear MSB of audio sample is aligned with bit 23 of the container.1= MSB is bit 31 of 32-bit container 0= MSB is bit 23 of 32-bit container (default)
12	0b RW	**_16_BIT_CONTAINER:** When this bit is set 16-bit sample is stored in 16-bit container format. When it is clear container is 32-bit for each sample regardless of valid bits (default)1= 16-bit container 0= 32-bit container
11	0b RW	**UNDERRUN_PACKET_BIT_SILENT_STREAM_ENABLE:** Set this bit will enable HW to send valid zero-filled packet with Sample flat bit set when no sample buffer is available, NCTS packets (or Timesstamp packet) are sent to keep sink in sync even no audio sound will heard.1= send underrun packets (silent stream) 0= send null packets (default) Programming note: SW driver shall always set silent stream bit. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically.
10	0b RW	**USER_BIT_U:** HW will clear this bit in each sub-frames it sends, But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= sey U bit in sub-frame 0= clear U bit in sub-frame (default)
9	1b RW	**VALIDITY_BIT_V:** HW will set this bit in both each sub-frames it sends. But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= Set V bit in sub-frame (default) 0= clear V bit in sub-frame. For debug or testing
8	0b RW	**SAMPLE_FLAT_BIT:** When set the sample flat bit will be set in all HDMI sub-packets. 1= flat bit is set for valid sample 0= flat bit is not set for valid sample (default)
7	1b RW	**SET_BLOCK_BEGIN_FOR_ALL_SUB_PACKETS:** Controls the B bit in the header of only the first Audio Packet /frame of a 192 frame 60958 block in Layout 1 mode. This bit only applies to LPE HDMI mode. 0: The B bit will be set only for sub-packet 0 1: The B bit in the Audio sample packet header will be set for all valid sub-packets. (default)

Bit Range	Default & Access	Description
6:4	0b RW	**NUM:** audio Channels 000: 2 channels (stereo) 001: 3 channels 010: 4 channels 011: 5 channels 100: 6 channels 101: 7 channels 110: 8 channels Note: When disable_bogus sample bit is clear HW will always treat odd number of channels similar to the next higher even number. Thus 3 is similar to 4, 5 to 6 and 7 to 8. This is because SW ensures that an even number of samples are packed in the audio buffers. Programming note: Bit 6 of of this field is a write only bit. When reads back, it always returns zero. Ensure to write bit 6 to 1?b1 when programming for 6/7/8 audio channels.
3:2	0b RW	**FORMAT:** 00: L-PCM or IEC 61937 01: High Bit Rate IEC 61937 stream packet (not supported) 10: One Bit Audio Sample packet (not supported) 11: DST Audio Sample packet (not supported)
1	0b RW	**LAYOUT:** 0: Layout 0 (2-ch) 1: Layout 1 (3-8 ch) Note: Layout bit does not matter for HBR
0	0b RW	**AUDIO_ENABLE:** Controls generation of N/CTS and transmission of audio sample packets. 0: Audio sample packets are not transmitted, CTS calculation/transmission is disabled 1: Audio sample packets are transmitted and CTS calculation is enabled When enable audio unit will wait until the next vertical blank period before sending out the audio packets. When disable, audio unit may continue to send audio packet until the end of current active video frame before stopping.

3.4.152 STREAM_B_LPE_AUD_CH_STATUS_0—Offset 65808h

Audio Channel Status Attributes 0

Access Method

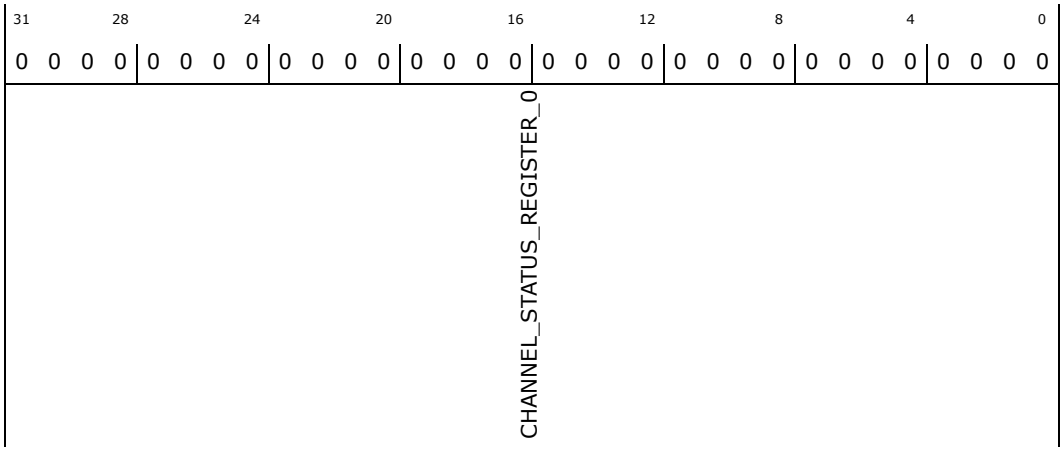
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_CH_STATUS_0: [GTTMMADR_LSB + 2BF20h] + 65808h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**CHANNEL_STATUS_REGISTER_0:** . These bits are transmitted as attributes of audio packets

3.4.153 STREAM_B_LPE_AUD_CH_STATUS_1—Offset 6580Ch

Audio Channel Status Attributes 1

Access Method

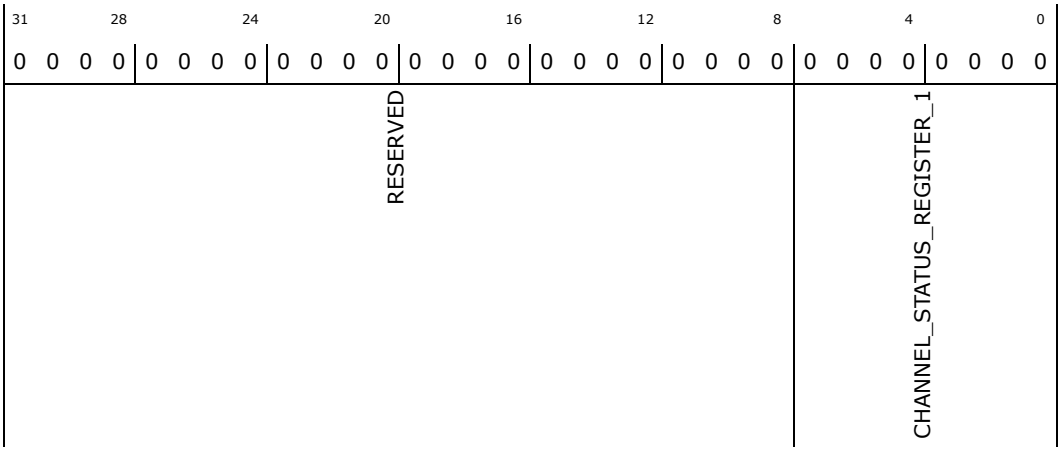
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_CH_STATUS_1: [GTTMMADR_LSB + 2BF20h] + 6580Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**RESERVED:** Reserved.
7:0	0b RW	**CHANNEL_STATUS_REGISTER_1:** . These bits are transmitted as attributes of audio packets. There is only 8 bits valid in this register.

3.4.154 STREAM_B_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65810h

Audio HDMI CTS Register (DP Maud)

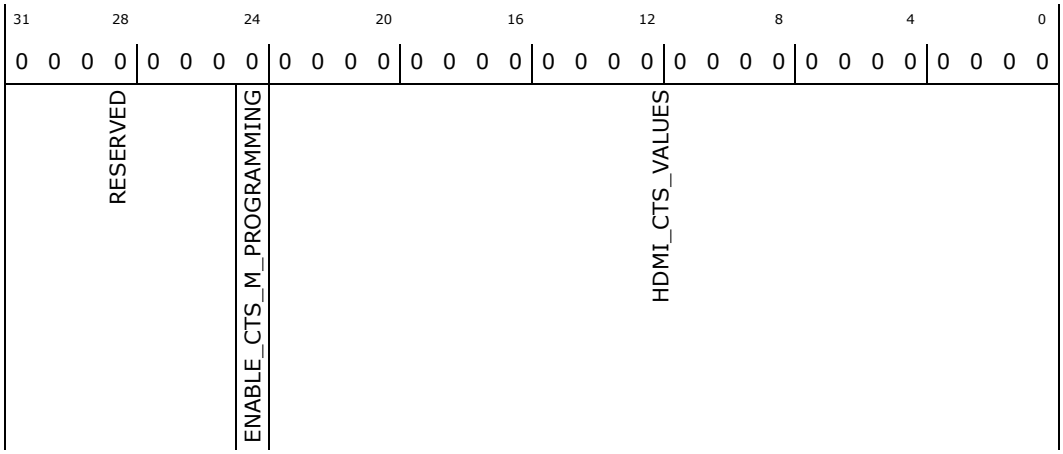
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_HDMI_CTS_DP_MAUD: [GTTMMADR_LSB + 2BF20h] + 65810h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RW	**RESERVED:** Reserved.
24	0b RW	**ENABLE_CTS_M_PROGRAMMING:** 1 = Enable CTS/M programming 0 = Disable CTS/M programming
23:0	0b RW	**HDMI_CTS_VALUES:** These are bits [23:0] of programmable HDMI CTS values (or DP Maud) that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

3.4.155 STREAM_B_LPE_AUD_HDMI_N_DP_NAUD—Offset 65814h

Audio HDMI N Register (DP Naud)

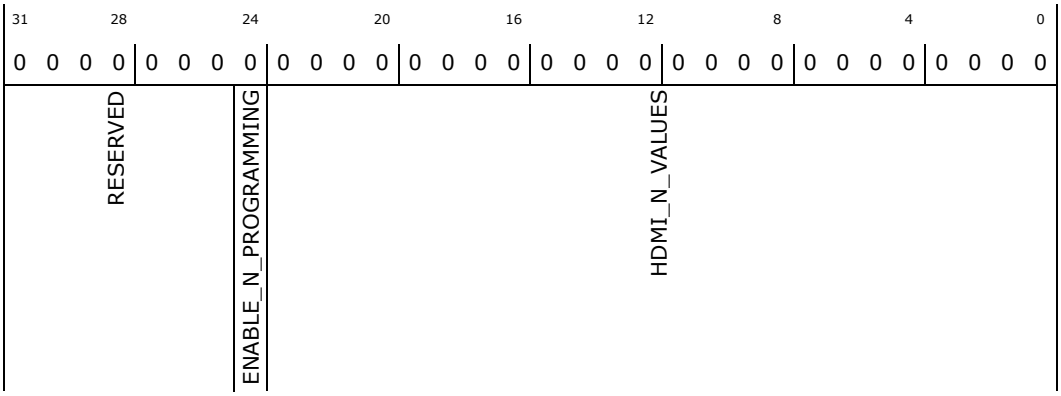
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_HDMI_N_DP_NAUD: [GTTMMADR_LSB + 2BF20h] + 65814h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RW	**RESERVED:** Reserved.
24	0b RW	**ENABLE_N_PROGRAMMING:** 1 = Enable N programming 0 = Disable N programming
23:0	0b RW	**HDMI_N_VALUES:** These are bits [23:0] of programmable HDMI N (or DP Naud) values that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

3.4.156 STREAM_B_LPE_AUD_BUFFER_CONFIG—Offset 65820h

LPE Audio buffer config

Access Method

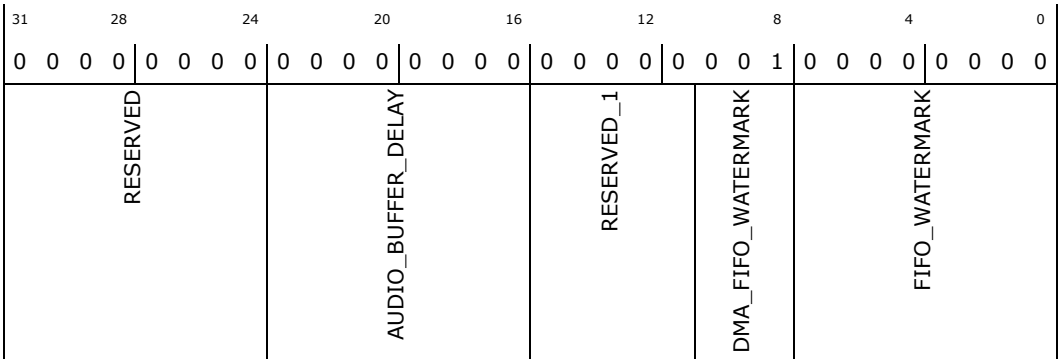
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_BUFFER_CONFIG: [GTTMMADR_LSB + 2BF20h] + 65820h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000100h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**AUDIO_BUFFER_DELAY:** This field specifies a delay in number of video frames that the audio controller will count off when audio enable bit is set before start transmitting audio sample.
15:11	0b RW	**RESERVED_1:** Reserved.
10:8	001b RW	**DMA_FIFO_WATERMARK:** Audio unit has a 8x64 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in SWORDs (64B). When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI/DP packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again. Default value is 1 cacheline (SW).
7:0	0b RW	**FIFO_WATERMARK:** Audio unit has a 96x8 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in DWORDs. When enable and sample buffer is available audio unit will fetch samples until this FIFO occupancy is above the watermark then it waits until HDMI packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again

3.4.157 STREAM_B_LPE_AUD_BUF_CH_SWP—Offset 65824h

Audio Sample Swapping

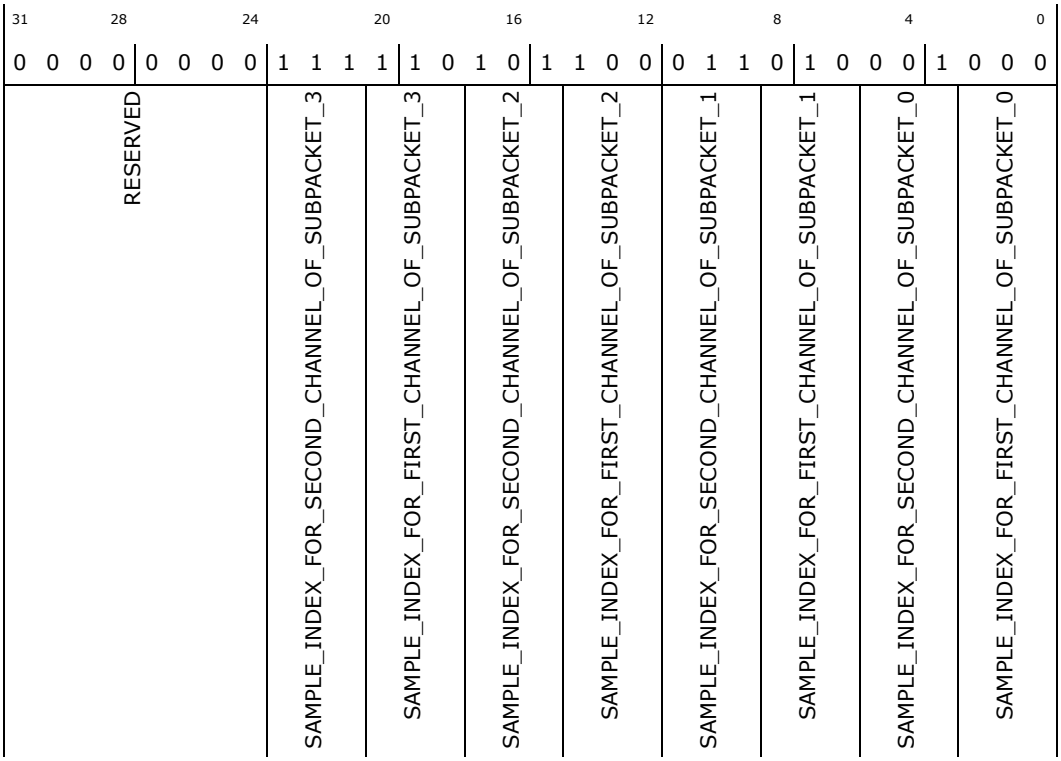
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_BUF_CH_SWP: [GTTMMADR_LSB + 2BF20h] + 65824h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00FAC688h



Bit Range	Default & Access	Description
31:24	0b RO	**RESERVED:** Reserved.
23:21	111b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 3 in a HDMI audio packet
20:18	110b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
17:15	101b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
14:12	100b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet
11:9	011b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 1 in a HDMI audio packet
8:6	010b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet

Bit Range	Default & Access	Description
5:3	001b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
2:0	0b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet

3.4.158 STREAM_B_LPE_AUD_BUF_A_ADDR—Offset 65840h

Address for Audio Buffer A

Access Method

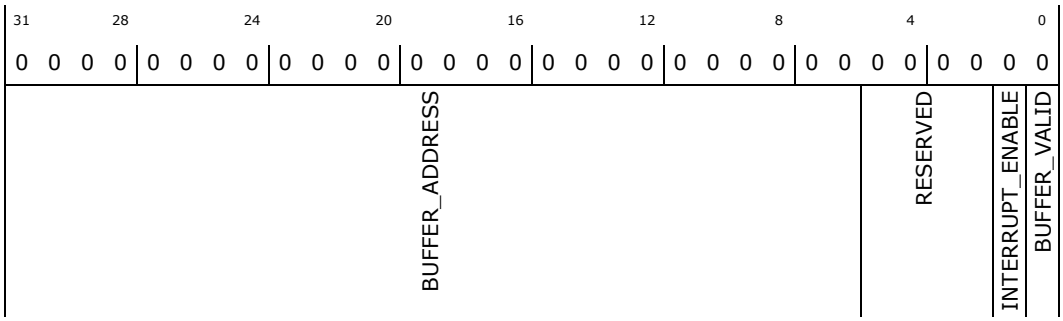
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_BUF_A_ADDR: [GTTMMADR_LSB + 2BF20h] + 65840h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.4.159 STREAM_B_LPE_AUD_BUF_A_LENGTH—Offset 65844h

Length for Audio Buffer A

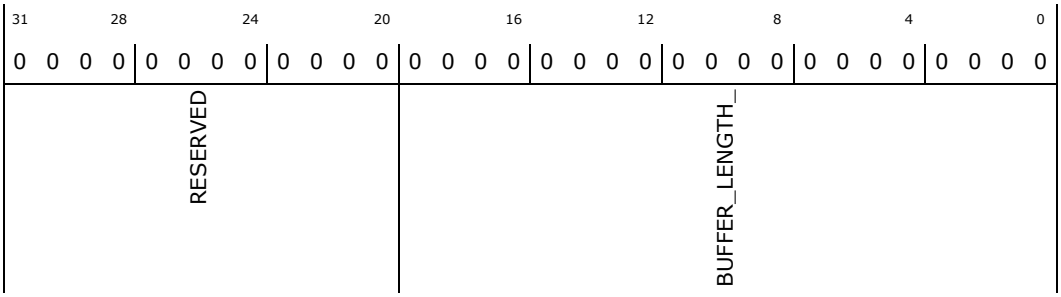
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_BUF_A_LENGTH: [GTTMMADR_LSB + 2BF20h] + 65844h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

3.4.160 STREAM_B_LPE_AUD_BUF_B_ADDR—Offset 65848h

Address for Audio Buffer B

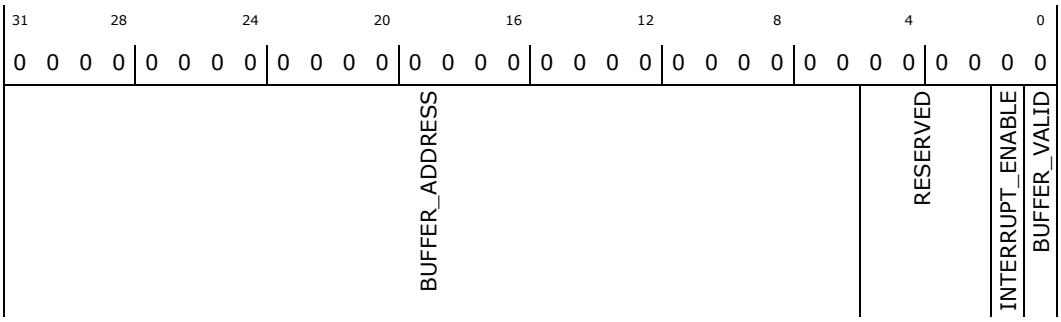
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_BUF_B_ADDR: [GTTMMADR_LSB + 2BF20h] + 65848h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.4.161 STREAM_B_LPE_AUD_BUF_B_LENGTH—Offset 6584Ch

Length for Audio Buffer B

Access Method

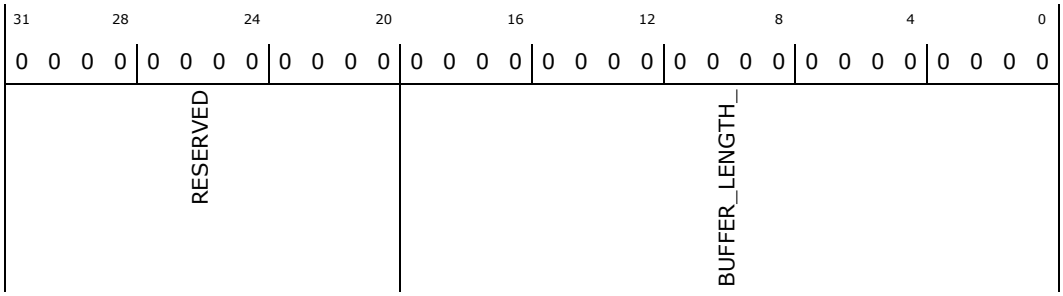
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_BUF_B_LENGTH: [GTTMMADR_LSB + 2BF20h] + 6584Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

3.4.162 STREAM_B_LPE_AUD_BUF_C_ADDR—Offset 65850h

Address for Audio Buffer C

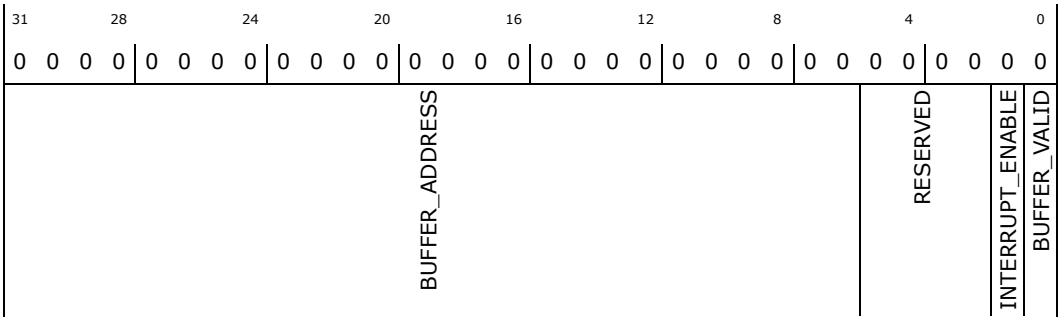
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_BUF_C_ADDR: [GTTMMADR_LSB + 2BF20h] + 65850h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.4.163 STREAM_B_LPE_AUD_BUF_C_LENGTH—Offset 65854h

Length for Audio Buffer C

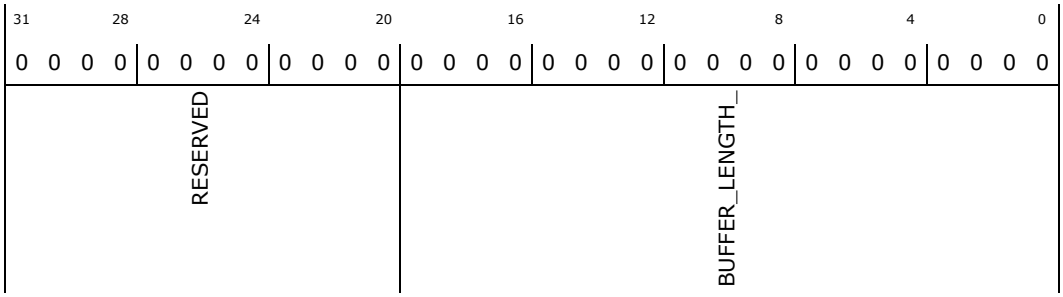
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_BUF_C_LENGTH: [GTTMMADR_LSB + 2BF20h] + 65854h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

3.4.164 STREAM_B_LPE_AUD_BUF_D_ADDR—Offset 65858h

Address for Audio Buffer D

Access Method

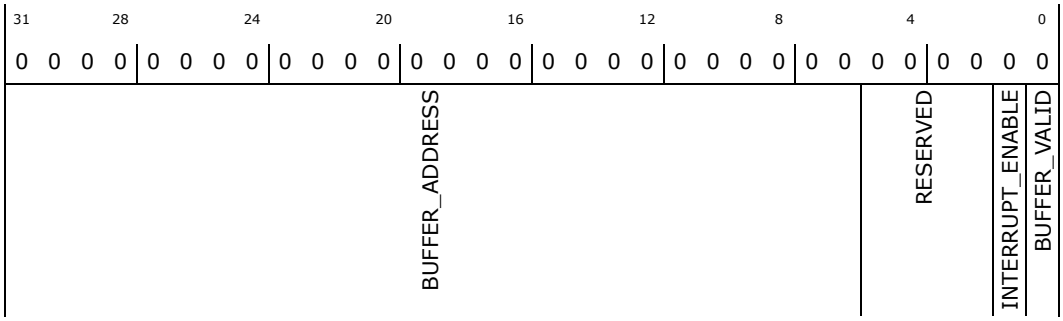
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_BUF_D_ADDR: [GTTMMADR_LSB + 2BF20h] + 65858h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

3.4.165 STREAM_B_LPE_AUD_BUF_D_LENGTH—Offset 6585Ch

Length for Audio Buffer D

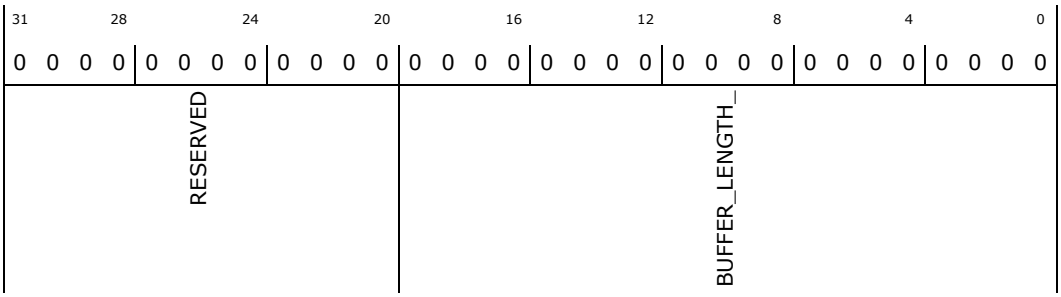
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_BUF_D_LENGTH: [GTTMMADR_LSB + 2BF20h] + 6585Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

3.4.166 STREAM_B_LPE_AUD_CNTL_ST—Offset 65860h

LPE Audio Control State Register

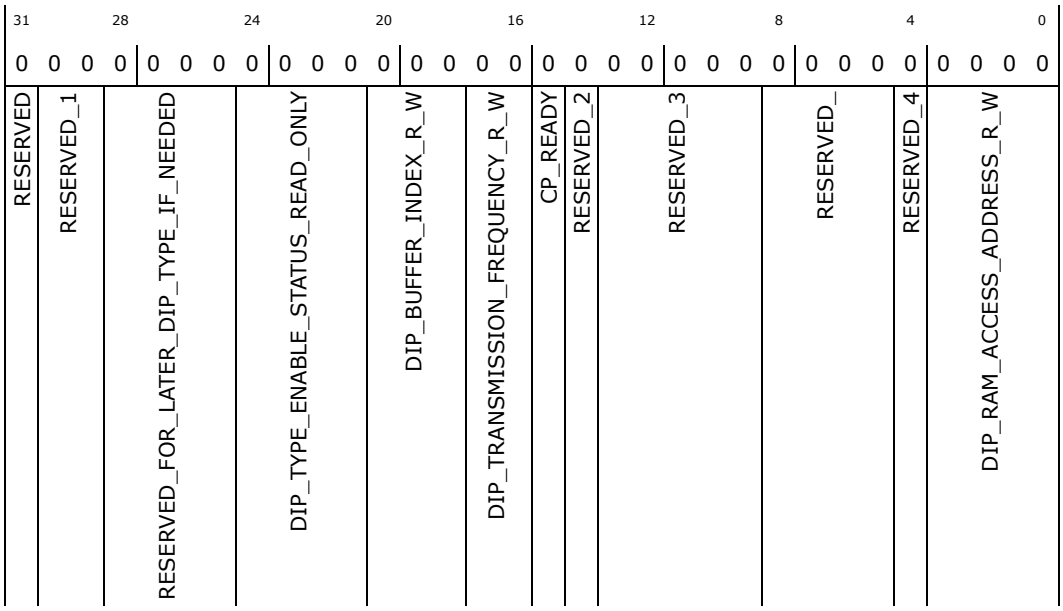
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

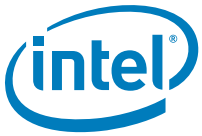
STREAM_B_LPE_AUD_CNTL_ST: [GTTMMADR_LSB + 2BF20h] + 65860h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** Reserved.
30:29	0b RW	**RESERVED_1:** Reserved.
28:25	0b RW	**RESERVED_FOR_LATER_DIP_TYPE_IF_NEEDED:** Must be 0.
24:21	0b RO	**DIP_TYPE_ENABLE_STATUS_READ_ONLY:** These bits reflects the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling an DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. XXX1 = Audio DIP enable status (Default = disabled) XX1X = Generic 1 (ACP) DIP enable status (Default = disabled) X1XX = Generic 2 DIP enable status, can be used by ISRC1 or ISRC2 (Default = disabled) 1XXX = Reserved AccessType: Read Only
20:18	0b RW	**DIP_BUFFER_INDEX_R_W:** This field is used during read or write of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0 s. 000 = (Default) Audio DIP (31 bytes of address space, 13 bytes of data) 001 = Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) 010 = Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) 011 = Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) 1XX = reserved



Bit Range	Default & Access	Description
17:16	0b RW	**DIP_TRANSMISSION_FREQUENCY_R_W:** These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. 00 = Disabled (Default) 01 = once per frame 10 = Send once 11 = Best effort (Send at least every other vsync)
15	0b RW	**CP_READY:** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. 0 = CP request pending or not ready to receive requests (default) 1 = CP request ready CP_ready bit is programmable through Bit 14 for [DevCL, DevBLC]. CP_ready bit is programmable through Bit 15 for [DevCTG]. Bit 15 Reserved for [DevCL, DevBLC].
14	0b RW	**RESERVED_2:** ELD valid: This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. 0 = ELD data invalid (default, when writing ELD data, set 0 by software) 1 = ELD data valid (Set by video software only) ELD bit is programmable through Bit 13 for [DevCL, DevBLC]. ELD bit is programmable through Bit 14 for [DevCTG].
13:9	0b RW	**RESERVED_3:** ELD buffer size (read only)10000 = This field reflects the size of the ELD buffer in DWORDs 13:9 reflects ELD buffer size for [DevCTG]. 12:9 reflects ELD buffer size for [DevCL, DevBLC].
8:5	0b RW	**RESERVED_:** ELD access address (R/W): Selects the DWORD address for access to the ELD buffer (48 bytes). The value wraps back to zero when incremented past the max addressing value 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.
4	0b RW	**RESERVED_4:** ELD ACK: Acknowledgement from the audio driver that ELD read has been completed
3:0	0b RW	**DIP_RAM_ACCESS_ADDRESS_R_W:** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

3.4.167 STREAM_B_LPE_AUD_HDMI_STATUS—Offset 65864h

LPE Audio Status

Access Method

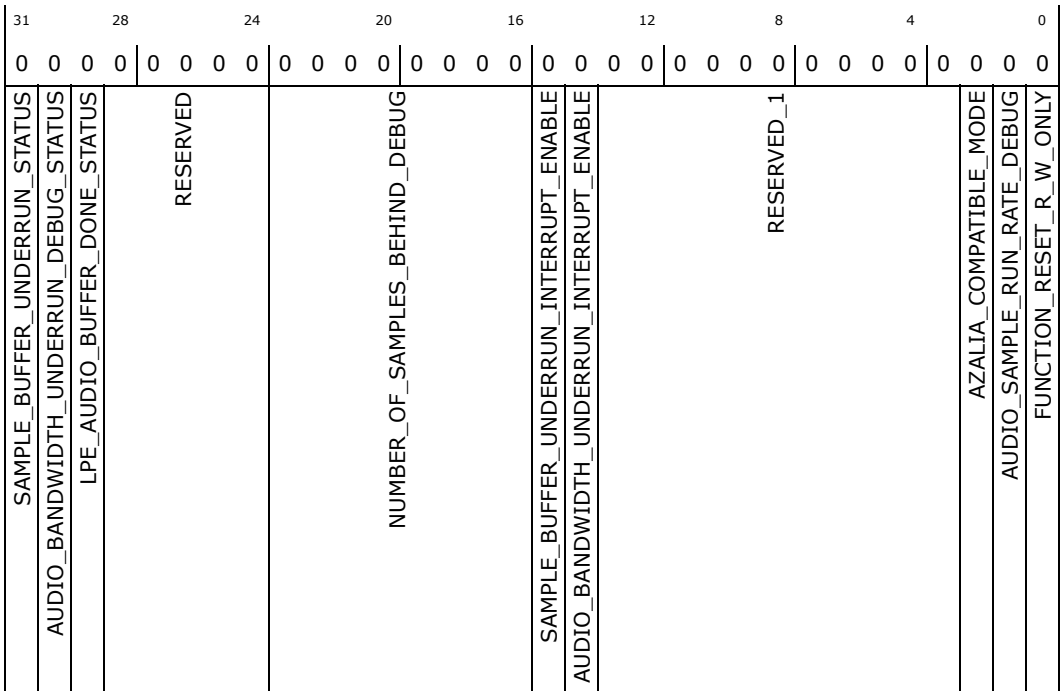
Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_HDMI_STATUS: [GTTMMADR_LSB + 2BF20h] + 65864h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/1C	**SAMPLE_BUFFER_UNDERRUN_STATUS:** This bit indicates an underrun in the sample buffer to HDMI/DP controller when it needs to send. This bit is set at the last line of active video when there are no more sample in any valid buffers and HDMI/DP audio unit has not satisfied number of audio samples intended in that video frame. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
30	0b RW/1C	**AUDIO_BANDWIDTH_UNDERRUN_DEBUG_STATUS:** This bit indicates an underrun of audio samples at HDMI audio packet assembly even there is still available sample buffers. Audio bandwidth underrun should not happen in normal functionality but it may happen when audio setting is inappropriate and/or memory bus was blocked by other clients, etc... This bit is set at the last line of active video when there is valid samples in a valid buffer and HDMI audio unit has not satisfied number of audio samples intended in that video frame Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
29	0b RW/1C	**LPE_AUDIO_BUFFER_DONE_STATUS:** This bit is set when a LPE audio buffer is completed transferred all of its data to LPE audio unit. This bit is clear when write 1 to it AccessType: One to Clear
28:24	0b RW	**RESERVED:** Reserved.
23:16	0b RO	**NUMBER_OF_SAMPLES_BEHIND_DEBUG:** This field is read only to get the number of audio samples that controller needs to load and send at the time of reading. AccessType: Read Only

Bit Range	Default & Access	Description
15	0b RW	**SAMPLE_BUFFER_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line buffer underrun interrupt when sample buffer underrun status is detected 0 = LPE sample Buffer Underrun Interrupt Disabled 1 = LPE sample Buffer Underrun Interrupt Enabled
14	0b RW	**AUDIO_BANDWIDTH_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line bandwidth underrun interrupt when bandwidth underrun status is detected 0 = LPE Bandwidth Underrun Interrupt Disabled 1 = LPE Bandwidth Underrun Interrupt Enabled
13:3	0b RW	**RESERVED_1:** Reserved.
2	0b RW	**AZALIA_COMPATIBLE_MODE:** This bit is to enable the vucp, PR, ECC to be generated in the Azalia way 0 = Disable Azalia compatible mode on vucp, PR, ECC 1 = Enable Azalia compatible mode on vucp, PR, ECC
1	0b RW	**AUDIO_SAMPLE_RUN_RATE_DEBUG:** When set it allows to fetch sample 128 times than the real sample rate to allow a faster drain of sample buffers.
0	0b RW	**FUNCTION_RESET_R_W_ONLY:** Write 1 to this bit will reset hardware within audio unit without needs of reset the full display controller. The FIFO and pointers will be reset and audio registers will be reset to default values. Write 0 will put the unit back to idle and ready to be programmed again.

3.4.168 STREAM_B_LPE_AUD_HDMIW_INFOFR—Offset 65868h

Audio HDMI Data Island Packet Data

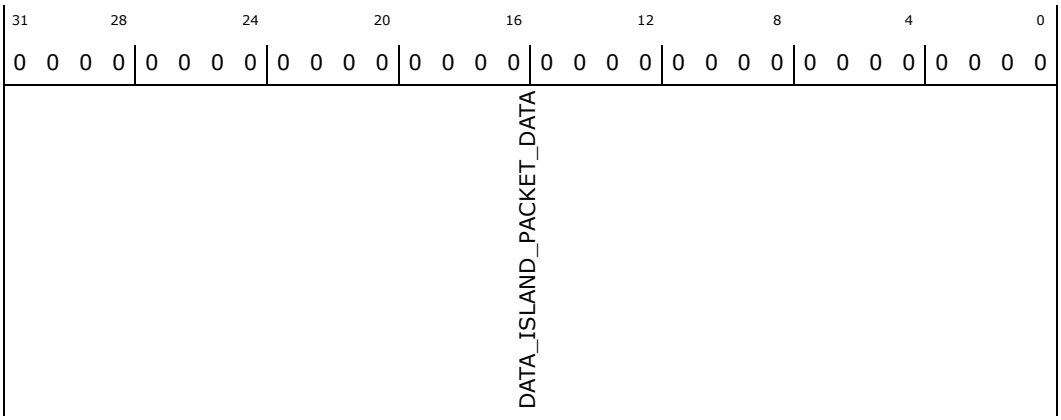
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STREAM_B_LPE_AUD_HDMIW_INFOFR: [GTTMMADR_LSB + 2BF20h] + 65868h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**DATA_ISLAND_PACKET_DATA:** When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis

3.4.169 PIPEA_DSL—Offset 70000h

Pipe A Display Scan Line

Access Method

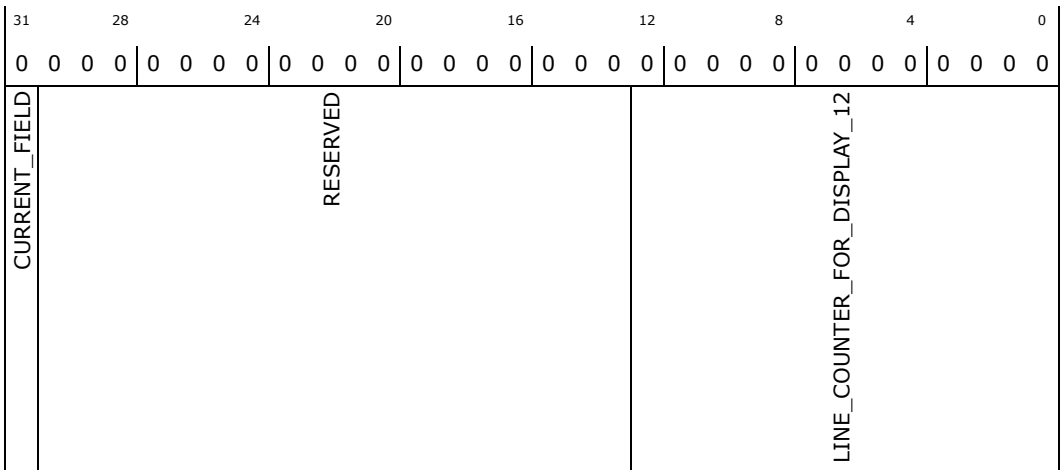
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_DSL: [GTTMMADR_LSB + 2BF20h] + 70000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**CURRENT_FIELD:** [DevBLC, DevCTG, DevCDV] Provides read back of the current field being displayed on display pipe A. Non-TV mode: 0 = first field (odd field) 1 = second field (even field) TV mode: 1 = first field (odd field) 0 = second field (even field) [DevBW] and [DevCL] Reserved: Read only.
30:13	0b RO	**RESERVED:** Read only.
12:0	0b RO	**LINE_COUNTER_FOR_DISPLAY_12:** 0]: Provides read back of the display pipe A vertical line counter. This is an indication of the current display scan line to be used by software to synchronize with the display.

3.4.170 PIPEA_SLC—Offset 70004h

Pipe A Display Scan Line Count Range Compare

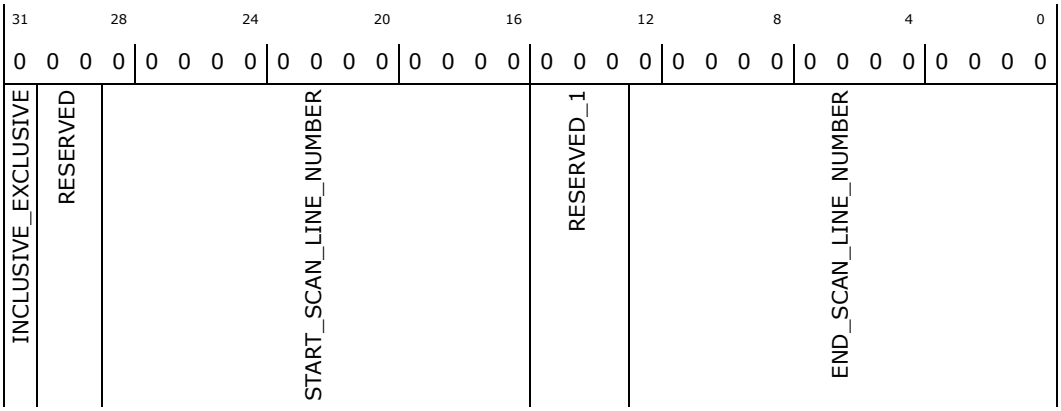
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEA_SLC: [GTTMMADR_LSB + 2BF20h] + 70004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**INCLUSIVE_EXCLUSIVE:** 1 = Inclusive: within the range. 0 = Exclusive: outside of the range.
30:29	0b RW	**RESERVED:** Read only.
28:16	0b RW	**START_SCAN_LINE_NUMBER:** [DevBLC, DevCTG, DevCDV] This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1]. [DevBW, DevCL] End Scan Line Number: This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1].
15:13	0b RW	**RESERVED_1:** Read only.
12:0	0b RW	**END_SCAN_LINE_NUMBER:** [DevBLC, DevCTG, DevCDV] This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1]. [DevBW] and [DevCL] Start Scan Line Number: This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1].

3.4.171 PIPEACONF—Offset 70008h

Pipe A Configuration Register

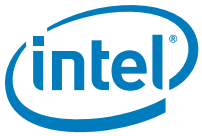
Access Method

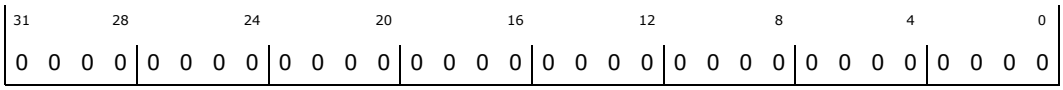
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEACONF: [GTTMMADR_LSB + 2BF20h] + 70008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h




31 28 24 20 16 12 8 4 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

PIPE_A_ENABLE
PIPE_STATE
DSI_PLL_LOCK_LOCK
FRAME_START_DELAY
DISPLAY_PORT_AUDIO_ONLY_MODE
FORCE_BORDER
PIPE_A_GAMMA_UNIT_MODE
INTERLACED_MODE
MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_A_REFRESH
DISPLAY_OVERLAY_PLANES_OFF
CURSOR_PLANES_OFF
REFRESH_RATE_CXSR_MODE_ASSOCIATION
_ON_PIPE_A_1_COLOR_CORRECTION_COEFFICIENTS_ARE_ENABLED_TO_PERFORM_COLOR_CORRECTION_0_COLOR_CORRECTION_COEFFICIENTS_ARE_DISABLED_
DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP
COLOR_RANGE_SELECT
S3D_SPRITE_ORDER
S3D_SPRITE_INTERLEAVING_FORMAT
RESERVED
BITS_PER_COLOR
DITHERING_ENABLE
DITHERING_TYPE
DDA_RESET_TEST_MODE
RESERVED_1

Bit Range	Default & Access	Description
31	0b RW	**PIPE_A_ENABLE:** Setting this bit to the value of one, turns on pipe A. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at it s lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should contain valid values before this bit is enabled. 0 = Disable 1 = Enable
30	0b RO	**PIPE_STATE:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off, this bit indicates the true current state of the pipe. 0 = Disabled 1 = Enabled AccessType: Read Only
29	0b RO	**DSI_PLL_LOCK_LOCK:** This bit indicates the clocks from DSI PLL are locked. 0 = Unlocked 1 = Locked AccessType: Read only
28:27	0b RW	**FRAME_START_DELAY:** (TEST MODE) Used to delay the frame start signal that is sent to the display planes. Normal operation uses the default 00 value and test modes can use the delayed frame start to shorten the test time. Care must be taken to insure that there are enough lines during VBLANK to support this setting. 00 = Frame Start occurs on the first HBLANK after the start of VBLANK 01 = Frame Start occurs on the second HBLANK after the start of VBLANK 10 = Frame Start occurs on the third HBLANK after the start of VBLANK 11 = Frame Start occurs on the forth HBLANK after the start of VBLANK
26	0b RW	**DISPLAY_PORT_AUDIO_ONLY_MODE:** [DevVLVP] Setting this bit to 1 indicates the DisplayPort will output audio only. 0 = DisplayPort will output Video or Video and Audio 1 = DisplayPort will output Audio only
25	0b RW	**FORCE_BORDER:** : (TEST MODE)0 = Normal Operation 1 = Color information is ignored and border color is substituted during active region
24	0b RW	**PIPE_A_GAMMA_UNIT_MODE:** This bit selects which mode the pipe gamma correction logic works in. In the palette mode, it behaves as a 3X256x8 RAM lookup. VGA and indexed mode operation should use the palette in 8-bit mode. In the 10-bit gamma mode, it will act as a piecewise linear interpolation. Other gamma units such as in the overlay or sprite are unaffected by this bit. 0 = 8-bit Palette Mode 1 = 10-bit Gamma Mode
23:21	0b RW	**INTERLACED_MODE:** These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled. 0xx = Progressive 100 = Interlaced embedded panel using programmable vertical sync shift. (2x) 101 = Interlaced using vertical sync shift. Backup option to 110 setting. (2x) 110 = Interlaced with VSYNC/HSYNC Field Indication using legacy vertical sync shift. Used for SDVO. 111 = Interlaced with Field 0 Only using legacy vertical sync shift. Not used Note: VGA display modes, sDVO line stall, and Panel fitting do not work while in interlaced modes Setting the Interlaced embedded panel mode causes hardware to automatically modify the output to match the specifications of panels that support interlaced mode.
20	0b RW	**MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_A_REFRESH:** 0 = Normal Operation, display controller generate timing and refresh display panel at refresh rate 1 = Display self-refresh mode. Display controller update frame buffer in display module on demand only

Bit Range	Default & Access	Description
19	0b RW	**DISPLAY_OVERLAY_PLANES_OFF:** This bit when set will cause all enabled Display and overlay planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the display and overlay planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
18	0b RW	**CURSOR_PLANES_OFF:** This bit when set will cause all enabled cursor planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the cursor(s) no longer appear on the screen. Setting the bit back to a zero will then allow the cursor planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
17:16	0b RW	**REFRESH_RATE_CXSR_MODE_ASSOCIATION:** These bits select how refresh rates are tied to big FIFO mode on pipe A. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 0xx. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated display panels that support corresponding mode. 00 Default no dynamic refresh rate change enabled. Software control only. 01 Progressive-to-progressive refresh rate change enabled and tied to big FIFO mode. Pixel clock values set in FPA0/FPA1 settings in the DPLLA control register and FPA0/FPA1 divider registers. FPA0 is tied to non-big-FIFO mode 10 Progressive-to-interlaced refresh rate change enabled and tied to big FIFO mode. Pixel clock value does not change in this case. Scaling must be disabled in this mode. Uses programmable VS shift 11 Reserved
15	0b RW	**COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_A_1_COLOR_CORRECTION_COEFFICIENTS_ARE_ENABLED_TO_PERFORM_COLOR_CORRECTION_0_COLOR_CORRECTION_COEFFICIENTS_ARE_DISABLED_:** • 1 = Color Correction Coefficients are enabled to perform color correction • 0 = Color Correction Coefficients are disabled
14	0b RW	**DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP:** This bit selects the software controlled progressive to progressive power saving mode (software controlled DRRS). Hardware Controlled Refresh Rate Select must be disabled when enabling this. Link and data M/N 1 values are used for normal settings, M/N 2 values are used for low power settings. 0 Normal progressive refresh rate (default) 1 Low Power progressive refresh rate
13	0b RW	**COLOR_RANGE_SELECT:** [DevVLVP]: This bit is used to select the color range of RBG outputs. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output
12	0b RW	**S3D_SPRITE_ORDER:** This bit controls the blending order of the sprite planes for S3D support: 0 = Sprite A first. The first line or pixel comes from Sprite A (default) 1 = Sprite B first. The first line or pixel comes from Sprite B
11:10	0b RW	**S3D_SPRITE_INTERLEAVING_FORMAT:** These bits control the Sprite A/B interleaving format in S3D mode 00 = No interleaving 01 = Line interleaving 10 = Pixel interleaving 11 = Reserved

Bit Range	Default & Access	Description
9:8	0b RW	**RESERVED:** [DevCDV, DevVLVP] MBZ Scrambling enable [DevCTG]: This bit enables scrambling for DisplayPort. Software must set this bit appropriately when enabling a DisplayPort output. 00 = Scrambling disabled (Default) 01 = Scrambling enabled, no SR after initialization at loop 2 of training 10 - RESERVED 11 = Scrambling and SR enabled. Scrambling is reset every 512 BS symbols.
7:5	0b RW	**BITS_PER_COLOR:** [DevCTG, DevCDV, DevVLVP]: This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change in DisplayPort. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. For further details on Display Port fixed frequency programming to accommodate these formats refer to DP Frequency Programming in DPLL section of Bspec. 000 = 8 bits per color (Default) 001 = 10 bits per color 010 = 6 bits per color 011 = RESERVED 1xx = RESERVED
4	0b RW	**DITHERING_ENABLE:** [DevCTG, DevCDV]: This bit enables dithering for DisplayPort 6bpc or 8bpc modes 0 Dithering disabled (Default) 1 Dithering enabled Programming note: Dithering should only be enabled for 8 bpc or 6 bpc.
3:2	0b RW	**DITHERING_TYPE:** [DevCTG, DevCDV]: This bit selects dithering type for DisplayPort 6bpc or 8bpc modes 00 - Spatial only (default) 01- Spatio-Temporal 1 10- Spatio-Temporal 2 (testmode) 11- Temporal only (testmode)
1	0b RW	**DDA_RESET_TEST_MODE:** [DevCTG, DevCDV]: 0 Do not reset DDA 1 Reset DDA every 8th display frame
0	0b RW	**RESERVED_1:** Write as zero

3.4.172 PIPEAGCMAXRED—Offset 70010h

Pipe A Gamma Correction Max Red

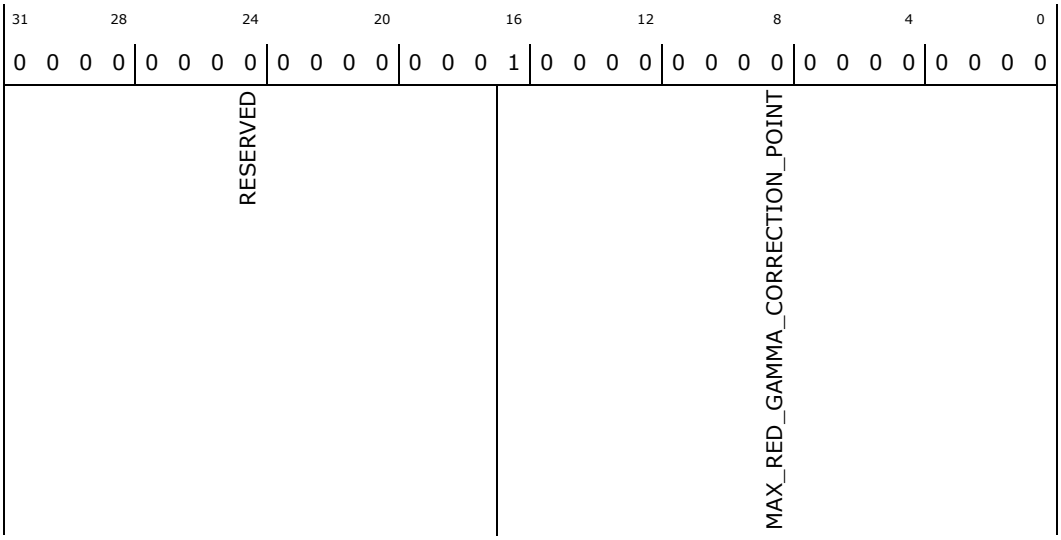
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAGCMAXRED: [GTTMMADR_LSB + 2BF20h] + 70010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	10000000000000000b RW	**MAX_RED_GAMMA_CORRECTION_POINT:** 129th reference point for red channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

3.4.173 PIPEAGCMAXGREEN—Offset 70014h

Pipe A Gamma Correction Max Green

Access Method

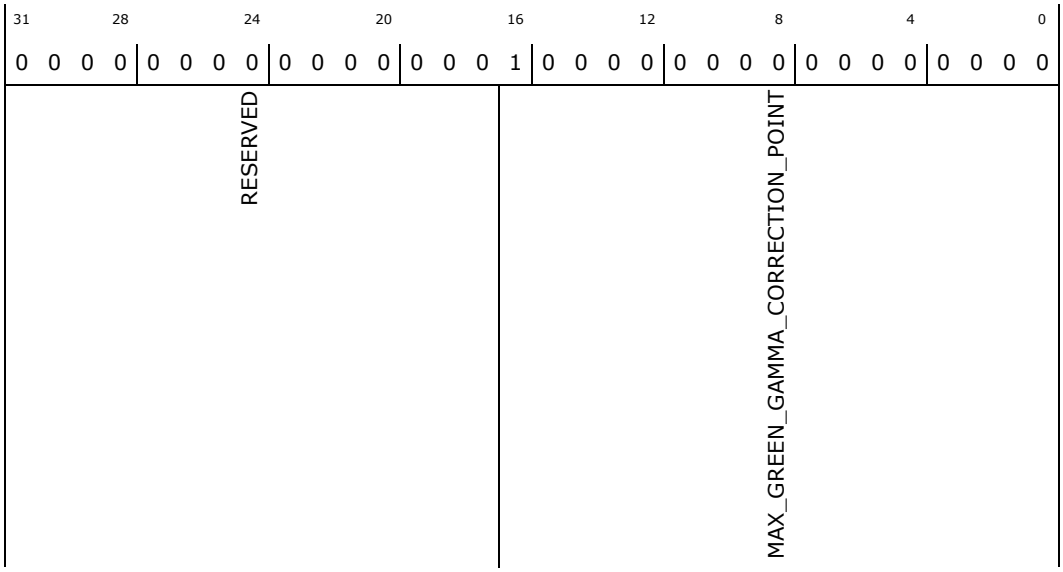
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAGCMAXGREEN: [GTTMMADR_LSB + 2BF20h] + 70014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	10000000000000000b RW	**MAX_GREEN_GAMMA_CORRECTION_POINT:** 129th reference point for green channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

3.4.174 PIPEAGCMAXBLUE—Offset 70018h

Pipe A Gamma Correction Max Blue

Access Method

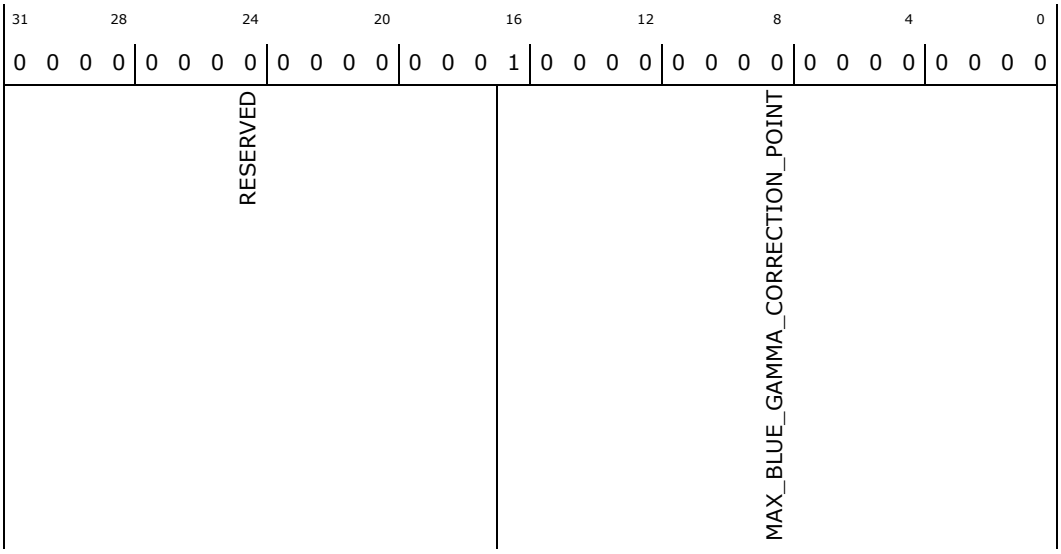
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAGCMAXBLUE: [GTTMMADR_LSB + 2BF20h] + 70018h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	10000000000000000b RW	**MAX_BLUE_GAMMA_CORRECTION_POINT:** 129th reference point for blue channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

3.4.175 PIPEASTAT—Offset 70024h

Pipe A Display Status

Access Method

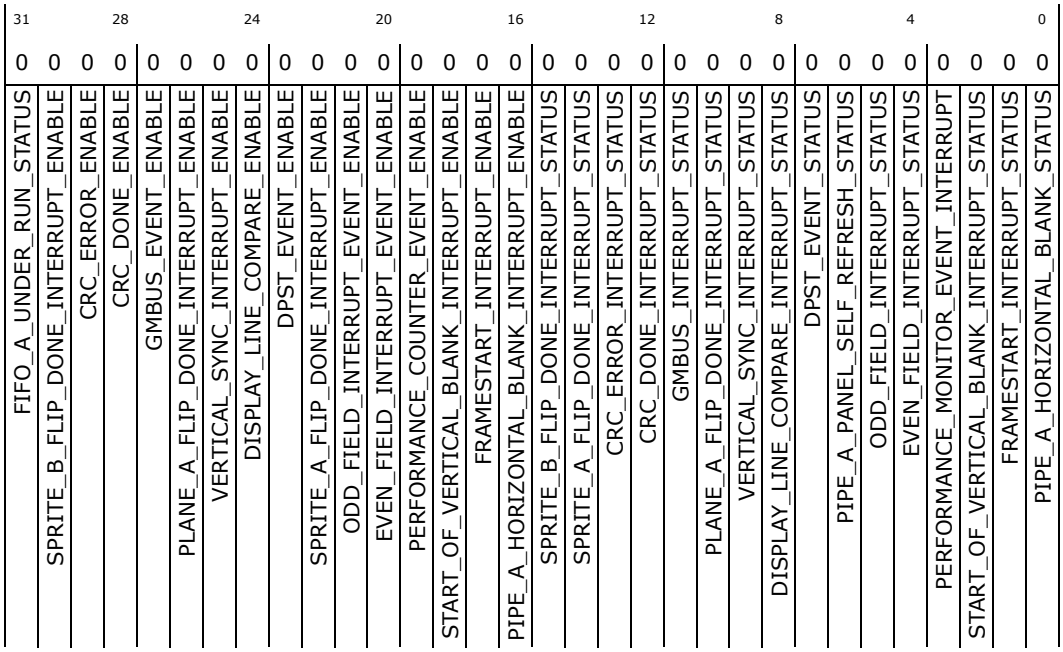
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEASTAT: [GTTMMADR_LSB + 2BF20h] + 70024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/1C	**FIFO_A_UNDER_RUN_STATUS:** Set when a pipe A FIFO under-run occurs, cleared by a write of a 1. An underrun has occurred on an attempt to pop an empty FIFO. This does not feed into the first line interrupt status register. This will occur naturally during mode changes, to be useful, it should be cleared after a mode change has occurred. This bit is only valid after Pipe A has been completely configured. 1 = FIFO A Underflow occurred 0 = FIFO A Underflow did not occur AccessType: One to Clear
30	0b RW	**SPRITE_B_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite B flip done interrupt status bit in the first line interrupt logic 0 = Sprite B Flip Done Interrupt Disabled 1 = Sprite B Flip Done Interrupt Enabled
29	0b RW	**CRC_ERROR_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt/status logic. 0 = CRC Error Detect Disabled 1 = CRC Error Detect Enabled
28	0b RW	**CRC_DONE_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt/status logic. 0 = CRC Done Detect Disabled 1 = CRC Done Detect Enabled
27	0b RW	**GMBUS_EVENT_ENABLE:** This will enable the use of the GMBUS interrupt status bit in the first line interrupt/status logic. 0 = No GMBUS event enabled 1 = GMBUS event enabled
26	0b RW	**PLANE_A_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Plane A flip done interrupt status bit in the first line interrupt logic 0 = Plane A flip done Interrupt/Status Disabled 1 = Plane A flip done Interrupt/Status Enabled

Bit Range	Default & Access	Description
25	0b RW	**VERTICAL_SYNC_INTERRUPT_ENABLE:** This will enable the consideration of the vertical sync interrupt status bit in the first line interrupt logic. 0 = Vertical Sync Interrupt/Status Disabled 1 = Vertical Sync Interrupt/Status Enabled
24	0b RW	**DISPLAY_LINE_COMPARE_ENABLE:** This will enable the consideration of the line compare interrupt status bit in the first line interrupt/status logic. 0 = Display Line Compare Interrupt/Status Disabled 1 = Display Line Compare Interrupt/Status Enabled
23	0b RW	**DPST_EVENT_ENABLE:** [DevCL, DevCTG, DevCDV]: This interrupt is generated by the DPST logic. 0 = No DPST event enabled 1 = DPST event enabled
22	0b RW	**SPRITE_A_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite A flip done interrupt status bit in the first line interrupt logic 0 = Sprite A Flip Done Interrupt Disabled 1 = Sprite A Flip Done Interrupt Enabled
21	0b RW	**ODD_FIELD_INTERRUPT_EVENT_ENABLE:** This bit should only be used when this pipe is in an interlaced display timing. 0 = Odd Field Event disable 1 = Odd Field Event enable
20	0b RW	**EVEN_FIELD_INTERRUPT_EVENT_ENABLE:** This bit should only be used when this pipe is in an interlaced display timing. 0 = Even field Event disable 1 = Even field Event enable
19	0b RW	**PERFORMANCE_COUNTER_EVENT_ENABLE:** performance counter event enable
18	0b RW	**START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Start of Vertical Blank Interrupt/Status Disabled 1 = Start of Vertical Blank Interrupt/Status Enabled
17	0b RW	**FRAMESTART_INTERRUPT_ENABLE:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Vertical Blank Interrupt/Status Disabled 1 = Vertical Blank Interrupt/ Status Enabled
16	0b RW	**PIPE_A_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** : This will enable the consideration of the start of horizontal blank interrupt status bit in the first line interrupt/status logic0 = Start of Horizontal Blank Interrupt/Status Disabled 1 = Start of Horizontal Blank Interrupt/Status Enabled
15	0b RW/1C	**SPRITE_B_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite B 0 = Sprite B Flip Not Done 1 = Sprite B Flip Done AccessType: One to Clear
14	0b RW/1C	**SPRITE_A_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite A 0 = Sprite A Flip Not Done 1 = Sprite A Flip Done AccessType: One to Clear
13	0b RW/1C	**CRC_ERROR_INTERRUPT_STATUS:** This sticky status bit is set when a Pipe A CRC error is detected. It is cleared by a write of a one. For this bit to be meaningful, the pipe and pixel clock should be enabled and running. 0 = No CRC error has occurred 1 = CRC Error Detected AccessType: One to Clear

Bit Range	Default & Access	Description
12	0b RW/1C	**CRC_DONE_INTERRUPT_STATUS:** This sticky status bit is set when Pipe A CRC calculation and compare are complete. It is cleared by a write of a one. For this bit to be meaningful, the pipe and pixel clock should be enabled and running. 0 = CRC Not Done 1 = CRC Done AccessType: One to Clear
11	0b RW/1C	**GMBUS_INTERRUPT_STATUS:** This status bit will be set on a GMBUS event. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = GMBUS event has not occurred 1 = GMBUS event has occurred AccessType: One to Clear
10	0b RW/1C	**PLANE_A_FLIP_DONE_INTERRUPT_STATUS:** Async/Sync Flip Event is completed on Display Plane A 0 = Plane A Flip Not Done 1 = Plane A Flip Done AccessType: One to Clear
9	0b RW/1C	**VERTICAL_SYNC_INTERRUPT_STATUS:** This bit provides a sticky status that is set when a pipe A vertical sync occurs, cleared by a write of a 1. For interlaced timing modes, this occurs once per field, when in progressive, it occurs once per frame. For this bit to be meaningful, the pipe and pixel clock should be enabled and running. 0 = Vertical Sync has not occurred 1 = Vertical Sync has occurred AccessType: One to Clear
8	0b RW/1C	**DISPLAY_LINE_COMPARE_INTERRUPT_STATUS:** Set when a pipe A compare match occurs, cleared by a write of a 1. 0 = Display Line Compare has not been satisfied 1 = Display Line Compare has been satisfied AccessType: One to Clear
7	0b RW/1C	**DPST_EVENT_STATUS:** [DevCL, DevCTG, DevCDV]: This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. Multiple DPST events (Histogram or Phase In) can cause this bit to be asserted, determination of which event occurred is done in the DPST registers. 0 = DPST Interrupt has not occurred on pipe A 1 = DPST Interrupt has occurred on pipe A AccessType: One to Clear
6	0b RW/1C	**PIPE_A_PANEL_SELF_REFRESH_STATUS:** This bit indicates interrupt is generated by the PSR controller and intends to send interrupt to SW driver when the PSR interrupt enable bit (70028h bit 22) is set. This is cleared when a write to this register occurs with this bit as a one. Write with this bit as a zero has no effect on the value of the bit. 0 = PSR Interrupt has not occurred on pipe A 1 = PSR interrupt has occurred on pipe A AccessType: One to Clear
5	0b RW/1C	**ODD_FIELD_INTERRUPT_STATUS:** This status bit will be set on a Odd field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Odd Field Vertical Blank has not occurred 1 = Odd Field Vertical Blank has occurred AccessType: One to Clear

Bit Range	Default & Access	Description
4	0b RW/1C	**EVEN_FIELD_INTERRUPT_STATUS:** This status bit will be set on a even field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Even Field Vertical Blank has not occurred 1 = Even Field Vertical Blank has occurred AccessType: One to Clear
3	0b RW/1C	**PERFORMANCE_MONITOR_EVENT_INTERRUPT:** AccessType: One to Clear
2	0b RW/1C	**START_OF_VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set at the beginning of a VBLANK event. At this point, the double buffered display registers flip, taking their new values. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. In MIPI DSR mode, GPIO TE trigger sets the Vblank Interrupt status 0 = Start of Vertical Blank has not occurred 1 = Start of Vertical Blank has occurred AccessType: One to Clear
1	0b RW/1C	**FRAMESTART_INTERRUPT_STATUS:** This status bit will be set on a VBLANK event, when the frame start occurs. The display registers are updated at the start of vertical blank, but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs, which is the event that triggers this bit. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = Vertical Blank has not occurred 1 = Vertical Blank has occurred AccessType: One to Clear
0	0b RW/1C	**PIPE_A_HORIZONTAL_BLANK_STATUS:** 0 = Pipe A Horizontal Blank has not occurred 1 = Pipe A Horizontal Blank has occurred AccessType: One to Clear

3.4.176 DPFLIPSTAT—Offset 70028h

Display FLIP Status Register

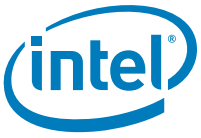
Access Method

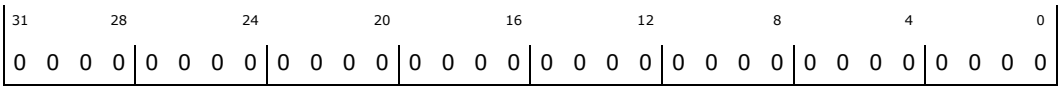
Type: Memory Mapped I/O Register (Size: 32 bits)

DPFLIPSTAT: [GTTMMADR_LSB + 2BF20h] + 70028h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

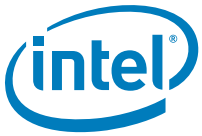
Default: 00000000h




31 28 24 20 16 12 8 4 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

RESERVED
DISPLAY_PIPE_B_LINE_COMPARE_INTERRUPT_STATUS_ENABLE
PIPE_B_HORIZONTAL_BLANK_INTERRUPT_ENABLE
PIPE_B_VERTICAL_BLANK_INTERRUPT_ENABLE
SPRITE_D_FLIP_DONE_INTERRUPT_ENABLE
SPRITE_C_FLIP_DONE_INTERRUPT_ENABLE
PLANE_B_FLIP_DONE_INTERRUPT_ENABLE
RESERVED_1
PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_A_0_PSR_INTERRUPT_DISABLED_ON_PIPE_A_1_PSR_INTERRUPT_ENABLED_ON_PIPE_A
DISPLAY_PIPE_A_LINE_COMPARE_INTERRUPT_STATUS_ENABLE
PIPE_A_HORIZONTAL_BLANK_INTERRUPT_ENABLE
PIPE_A_VERTICAL_BLANK_INTERRUPT_ENABLE
SPRITE_B_FLIP_DONE_INTERRUPT_ENABLE
SPRITE_A_FLIP_DONE_INTERRUPT_ENABLE
PLANE_A_FLIP_DONE_INTERRUPT_ENABLE

RESERVED_2



Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** MBZ
29	0b RW	**DISPLAY_PIPE_B_LINE_COMPARE_INTERRUPT_STATUS_ENABLE:** 0 = Display Pipe B Line Compare Interrupt Disabled 1 = Display Pipe B Line Compare Interrupt Enabled
28	0b RW	**PIPE_B_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe B Horizontal Blank Interrupt Disabled 1 = Pipe B Horizontal Blank Interrupt Enabled
27	0b RW	**PIPE_B_VERTICAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe B Vertical Blank Interrupt Disabled 1 = Pipe B Vertical Blank Interrupt Enabled
26	0b RW	**SPRITE_D_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite D Flip Done Interrupt Disabled 1 = Sprite D Flip Done Interrupt Enabled
25	0b RW	**SPRITE_C_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite C Flip Done Interrupt Disabled 1 = Sprite C Flip Done Interrupt Enabled
24	0b RW	**PLANE_B_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Plane B Flip Done Interrupt Disabled 1 = Plane B Flip Done Interrupt Enabled
23	0b RW	**RESERVED_1:** Reserved.
22	0b RW	**PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_A_0_PSR_INTERRUPT_DISABLED_ON_PIPE_A_1_PSR_INTERRUPT_ENABLED_ON_PIPE_A:** • 0 = PSR interrupt Disabled on Pipe A • 1 = PSR Interrupt Enabled on Pipe A
21	0b RW	**DISPLAY_PIPE_A_LINE_COMPARE_INTERRUPT_STATUS_ENABLE:** 0 = Display Pipe A Line Compare Interrupt Disabled 1 = Display Pipe A Line Compare Interrupt Enabled
20	0b RW	**PIPE_A_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe A Horizontal Blank Interrupt Disabled 1 = Pipe A Horizontal Blank Interrupt Enabled
19	0b RW	**PIPE_A_VERTICAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe A Vertical Blank Interrupt Disabled 1 = Pipe A Vertical Blank Interrupt Enabled
18	0b RW	**SPRITE_B_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite B Flip Done Interrupt Disabled 1 = Sprite B Flip Done Interrupt Enabled
17	0b RW	**SPRITE_A_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite A Flip Done Interrupt Disabled 1 = Sprite A Flip Done Interrupt Enabled
16	0b RW	**PLANE_A_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Plane A Flip Done Interrupt Disabled 1 = Plane A Flip Done Interrupt Enabled
15:0	0b RW	**RESERVED_2:** MBZ

3.4.177 DPINVGTT—Offset 7002Ch

Display Invalid GTT PTE Status Register

Access Method

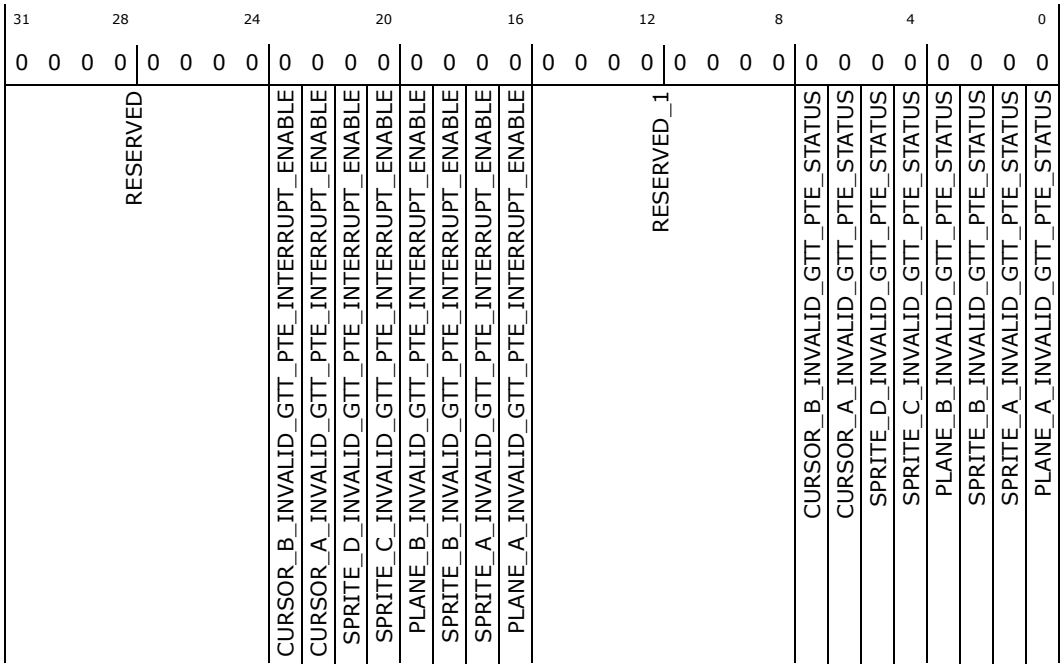
Type: Memory Mapped I/O Register (Size: 32 bits)

DPINVGTT: [GTTMMADR_LSB + 2BF20h] + 7002Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** MBZ
23	0b RW	**CURSOR_B_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Cursor B Invalid GTT PTE Interrupt Disabled 1 = Cursor B Invalid GTT PTE Interrupt Enabled
22	0b RW	**CURSOR_A_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Cursor A Invalid GTT PTE Interrupt Disabled 1 = Cursor A Invalid GTT PTE Interrupt Enabled
21	0b RW	**SPRITE_D_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite D Invalid GTT PTE Interrupt Disabled 1 = Sprite D Invalid GTT PTE Interrupt Enabled
20	0b RW	**SPRITE_C_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite C Invalid GTT PTE Interrupt Disabled 1 = Sprite C Invalid GTT PTE Interrupt Enabled
19	0b RW	**PLANE_B_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Plane B Invalid GTT PTE Interrupt Disabled 1 = Plane B Invalid GTT PTE Interrupt Enabled

Bit Range	Default & Access	Description
18	0b RW	**SPRITE_B_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite B Invalid GTT PTE Interrupt Disabled 1 = Sprite B Invalid GTT PTE Interrupt Enabled
17	0b RW	**SPRITE_A_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite A Invalid GTT PTE Interrupt Disabled 1 = Sprite A Invalid GTT PTE Interrupt Enabled
16	0b RW	**PLANE_A_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Plane A Invalid GTT PTE Interrupt Disabled 1 = Plane A Invalid GTT PTE Interrupt Enabled
15:8	0b RW	**RESERVED_1:** MBZ
7	0b RW/1C	**CURSOR_B_INVALID_GTT_PTE_STATUS:** 0 = Cursor B encountered an invalid GTT PTE has not occurred 1 = Cursor B encountered an invalid GTT PTE has occurred AccessType: One to Clear
6	0b RW/1C	**CURSOR_A_INVALID_GTT_PTE_STATUS:** 0 = Cursor A encountered an invalid GTT PTE has not occurred 1 = Cursor A encountered an invalid GTT PTE has occurred AccessType: One to Clear
5	0b RW/1C	**SPRITE_D_INVALID_GTT_PTE_STATUS:** 0 = Sprite D encountered an invalid GTT PTE has not occurred 1 = Sprite D encountered an invalid GTT PTE has occurred. AccessType: One to Clear
4	0b RW/1C	**SPRITE_C_INVALID_GTT_PTE_STATUS:** 0 = Sprite C encountered an invalid GTT PTE has not occurred 1 = Sprite C encountered an invalid GTT PTE has occurred. AccessType: One to Clear
3	0b RW/1C	**PLANE_B_INVALID_GTT_PTE_STATUS:** 0 = Plane B encountered an invalid GTT PTE has not occurred 1 = Plane B encountered an invalid GTT PTE has occurred. AccessType: One to Clear
2	0b RW/1C	**SPRITE_B_INVALID_GTT_PTE_STATUS:** 0 = Sprite B encountered an invalid GTT PTE has not occurred 1 = Sprite B encountered an invalid GTT PTE has occurred. AccessType: One to Clear
1	0b RW/1C	**SPRITE_A_INVALID_GTT_PTE_STATUS:** 0 = Sprite A encountered an invalid GTT PTE has not occurred 1 = Sprite A encountered an invalid GTT PTE has occurred. AccessType: One to Clear
0	0b RW/1C	**PLANE_A_INVALID_GTT_PTE_STATUS:** 0 = Plane A encountered an invalid GTT PTE has not occurred 1 = Plane A encountered an invalid GTT PTE has occurred. AccessType: One to Clear

3.4.178 DSPARB—Offset 70030h

Display Arbitration Control

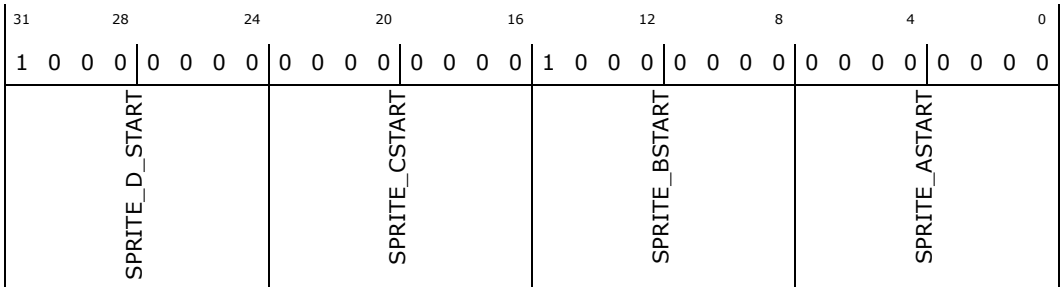
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPARB: [GTTMMADR_LSB + 2BF20h] + 70030h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 80008000h



Bit Range	Default & Access	Description
31:24	10000000b RW	**SPRITE_D_START:** This field selects the end of the ram used for Sprite C and the start of the RAM for Sprite D. If sprite C is unused, this field can be set to the same value as Sprite C START. If Sprite D is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite C START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite C FIFO will be (Sprite D START-Sprite C START)*64. The size of the Sprite D FIFO will be (TOTALSIZE-Sprite D START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
23:16	0b RW	**SPRITE_CSTART:** This field selects the end of the ram used for display B and the start of the RAM for Sprite C. If display B is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display B FIFO will be (Sprite C START)*64 bytes.
15:8	10000000b RW	**SPRITE_BSTART:** This field selects the end of the ram used for Sprite A and the start of the RAM for Sprite B. If sprite A is unused, this field can be set to the same value as Sprite A START. If Sprite B is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite A START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite A FIFO will be (Sprite B START-Sprite A START)*64. The size of the Sprite B FIFO will be (TOTALSIZE-Sprite B START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
7:0	0b RW	**SPRITE_ASTART:** This field selects the end of the ram used for display A and the start of the RAM for Sprite A. If display A is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display A FIFO will be (Sprite A START)*64 bytes.

3.4.179 FW1—Offset 70034h

Display FIFO Watermark Control 1

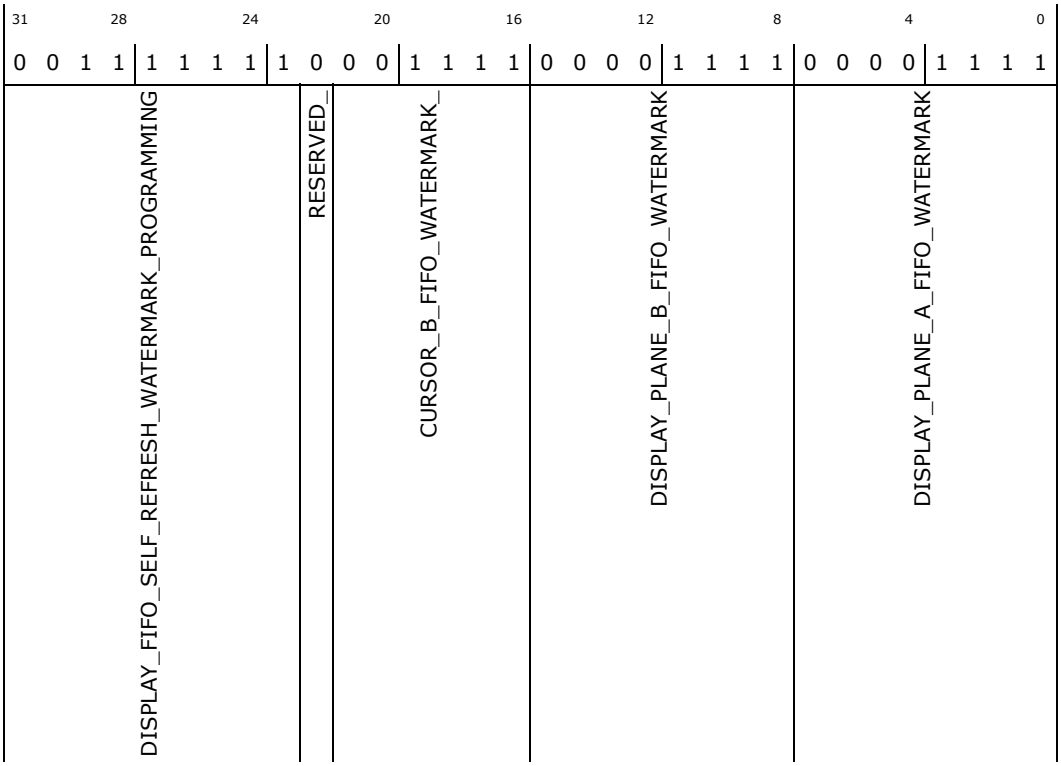
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FW1: [GTTMMADR_LSB + 2BF20h] + 70034h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 3F8F0F0Fh



Bit Range	Default & Access	Description
31:23	001111111b RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK_PROGRAMMING:** This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).Note [DevCL, DevCTG, DevCDV]: When calculating watermark values for 15/16bpp display formats, assume 32bpp for purposes of calculation using the high priority bandwidth analysis spreadsheet.
22	0b RW	**RESERVED_:** MBZ
21:16	001111b RW	**CURSOR_B_FIFO_WATERMARK_:** Number in 64Bs of space in the Cursor B FIFO above which the Cursor B Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). DevBW, DevCL, DevCDV] Always program to 8.
15:8	00001111b RW	**DISPLAY_PLANE_B_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display B Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). [DevBW, DevCL, DevCDV] Always program to 8.
7:0	00001111b RW	**DISPLAY_PLANE_A_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). [DevBW, DevCL, DevCDV] Always program to 8.

3.4.180 FW2—Offset 70038h

Display FIFO Watermark Control 2

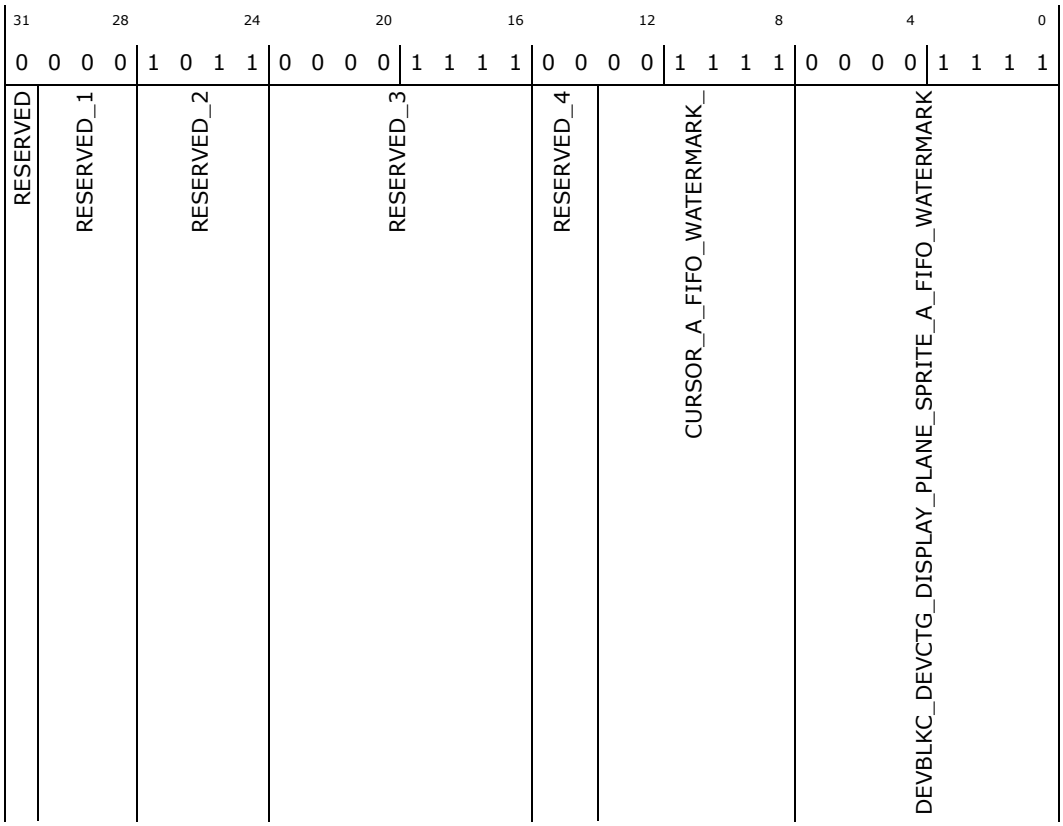
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FW2: [GTTMMADR_LSB + 2BF20h] + 70038h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 0B0F0F0Fh



Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** [DevCDV]: [DevCTG] FBC SR Watermark Enable: Enables the FBC watermarks to be used in the fetch calculation 0: disabled 1: enabled
30:28	0b RW	**RESERVED_1:** [DevCDV]: [DevCTG] FBC SR Watermark: Number of equivalent lines of the primary display SR watermark
27:24	1011b RW	**RESERVED_2:** [DevCDV] [DevCTG] FBC SR HPLL Watermark: Number of equivalent lines of the primary display SR HPLL watermark.

Bit Range	Default & Access	Description
23:16	00001111b RW	**RESERVED_3:** [DevCDV]: [DevBLKC, DevCTG] Display Plane Sprite B FIFO Watermark Number in 64Bs of space in FIFO above which the Display Sprite B Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
15:14	0b RW	**RESERVED_4:** : MBZ
13:8	001111b RW	**CURSOR_A_FIFO_WATERMARK_:** Number in 64Bs of space in the Cursor A FIFO above which the Cursor A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). DevBW, DevCL, DevCDV] Always program to 8.
7:0	00001111b RW	**DEVBLKC_DEVCTG_DISPLAY_PLANE_SPRITE_A_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display Sprite A Stream will generate requests to Memory DevBW, DevCL] Display Plane C FIFO Watermark. Number in 64Bs of space in FIFO above which the Display C Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). [DevBW, DevCL, DevCDV] Always program to 8.

3.4.181 FW3—Offset 7003Ch

Display FIFO Watermark Control 3

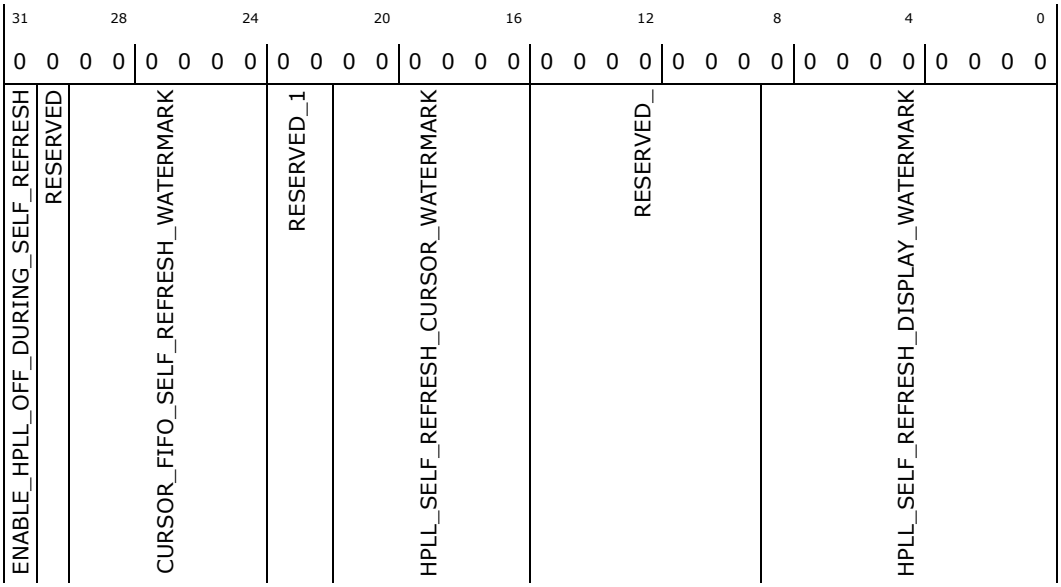
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FW3: [GTTMMADR_LSB + 2BF20h] + 7003Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**ENABLE_HPLL_OFF_DURING_SELF_REFRESH:** . 0 = Disabled 1 = Enabled [DevCL] This bit may be enabled only if the BLC_PWM_CTL duty cycle register offset (0x61254) is programmed to 100% and non-legacy backlight is enabled. This restriction does not apply when I2C is used for back light modulation. [DevCL] When one or more display pipes are enabled, this bit should be disabled before accessing the 6XXXh MMIO register address space. Software must follow these steps: disable this bit (if enabled and one display pipe is enabled) wait for next vblank (switch from hrawclk back to cdclk will occur) access the 6XXXh address space as needed re-enable this bit Note that the wait on next vblank step requires an enabled display pipe.
30	0b RW	**RESERVED:** : MBZ
29:24	0b RW	**CURSOR_FIFO_SELF_REFRESH_WATERMARK:** . Number in 64Bs of space in the Cursor FIFO above which the Cursor Stream will generate requests to Memory during self -refresh. (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
23:22	0b RW	**RESERVED_1:** : MBZ
21:16	0b RW	**HPLL_SELF_REFRESH_CURSOR_WATERMARK:** . Number in 64Bs of space in the Cursor FIFO above which the Cursor Stream will generate requests to Memory during HPLL self -refresh. (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
15:9	0b RW	**RESERVED_:** MBZ
8:0	0b RW	**HPLL_SELF_REFRESH_DISPLAY_WATERMARK:** . Number in 64Bs of space in the FIFO above which the Display Stream will generate requests to Memory during HPLL self -refresh. (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

3.4.182 PIPEAFRAMECOUNT—Offset 70040h

Pipe A Frame Counter

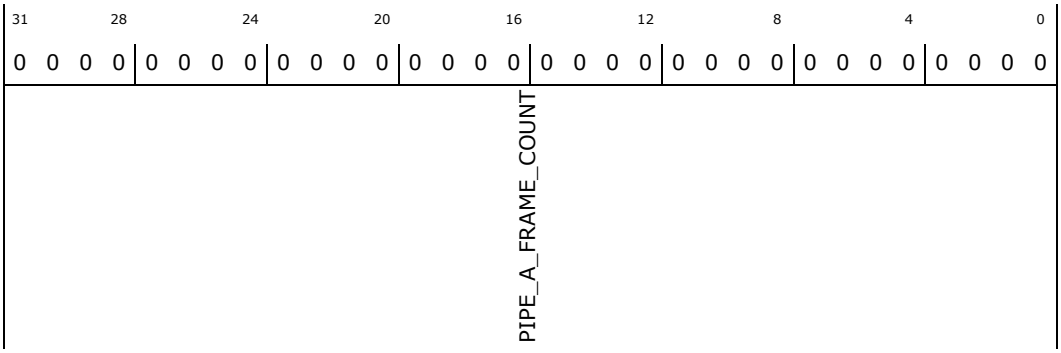
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAFRAMECOUNT: [GTTMMADR_LSB + 2BF20h] + 70040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**PIPE_A_FRAME_COUNT:** Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after 2^32 frames

3.4.183 PIPEAFLIPCOUNT—Offset 70044h

Pipe A Flip Counter

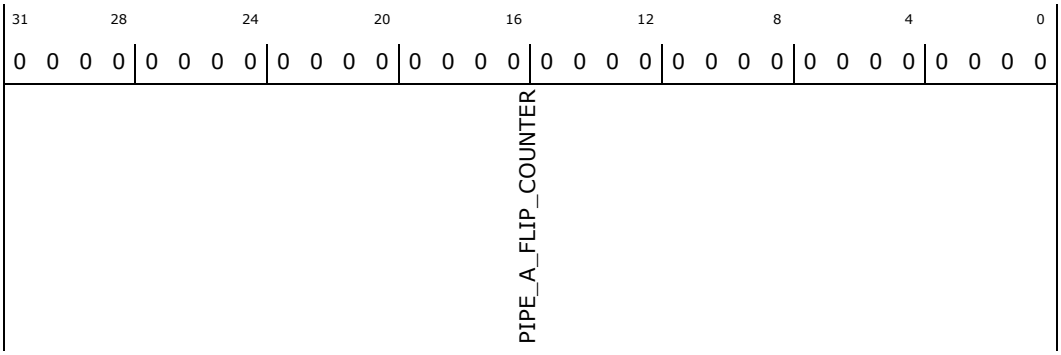
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAFLIPCOUNT: [GTTMMADR_LSB + 2BF20h] + 70044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**PIPE_A_FLIP_COUNTER:** Provides read back of the display pipe flip counter. This counter increments on each flip of the surface of the primary plane on this pipe. This includes command streamer asynchronous and synchronous flips and any MMIO writes to the primary plane surface address. It rolls over back to 0 after 2^32 flips

3.4.184 PIPEAMSAMISC—Offset 70048h

Pipe A MSA MISC

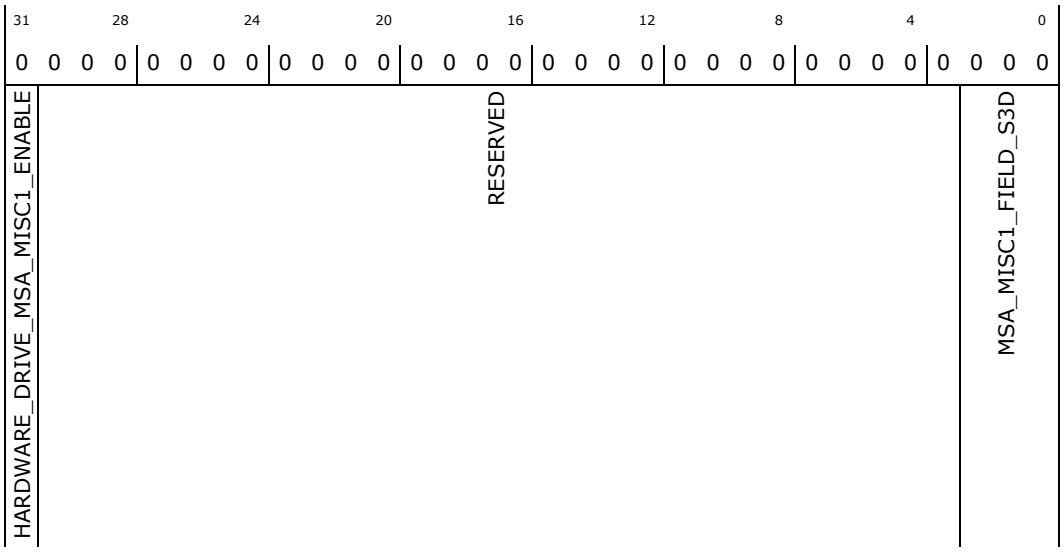
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEAMSAMISC: [GTTMMADR_LSB + 2BF20h] + 70048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**HARDWARE_DRIVE_MSA_MISC1_ENABLE:** This bit enables hardware to drive MSA MISC1 bit3:1 with the stereo 3D left/right eye field indication. Hardware will drive 000 when S3D mode is disabled, 001 when enabled and the upcoming video frame is right eye, 011 when enabled and the upcoming video frame is left eye. When this bit is disabled, software may manually program the MSA MISC1 Field S3D field in bit 2:0 in this register to set MISC1 bit 3:1 0 = Disable hardware driving MSA MISC1 bit 3:1. Allow software to manually program MSA MISC1 bit3:1 through MSA_MISC1_FIELD_S3D (default) 1 = Enable hardware to drive MSA MISC1 bit3:1 for S3D
30:3	0b RW	**RESERVED:** Reserved.
2:0	0b RW	**MSA_MISC1_FIELD_S3D:** This field provides software to manually program MSC1 stereo video attribute for DisplayPort: 000 = No stereo video transported 001 = For progressive video, the next (upcoming) video frame is RIGHT eye 010 = Reserved 011 = For progressive video, the next (upcoming) video frame is LEFT eye 100 = Stacked top and bottom top half represents left-eye view and bottom half represents right-eye view 101 = Stacked top and bottom top half represents right-eye view and bottom half represents left-eye view

3.4.185 DDL1—Offset 70050h

Display FIFO Drain Latency 1

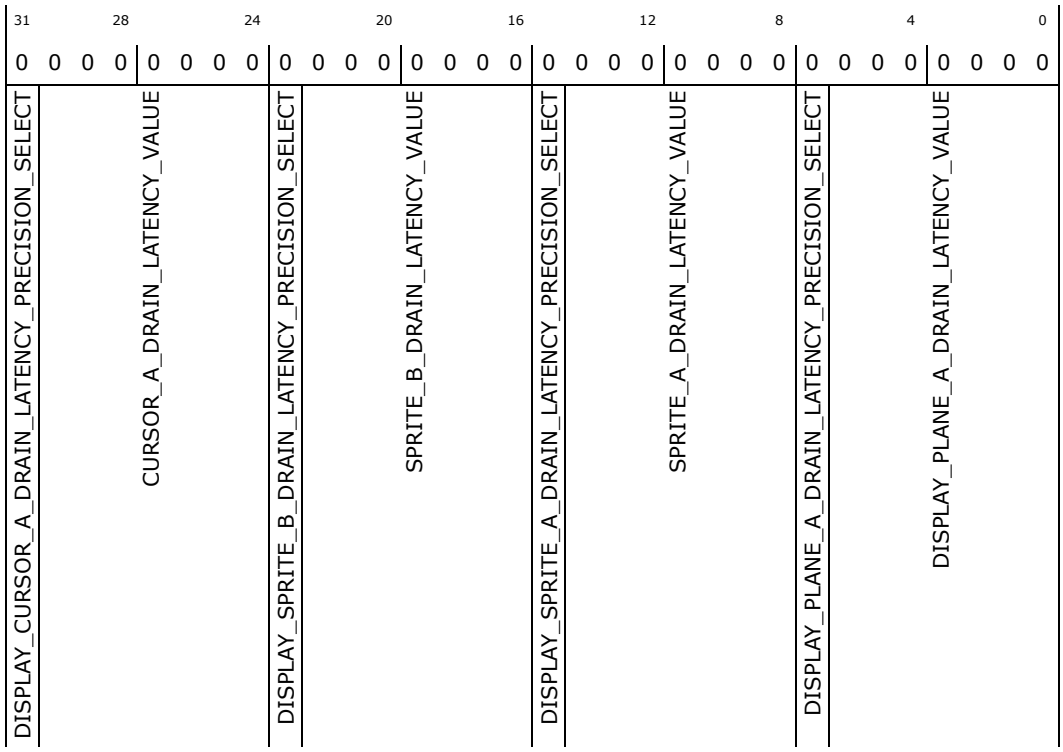
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DDL1: [GTTMMADR_LSB + 2BF20h] + 70050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**DISPLAY_CURSOR_A_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multiplier to increase precision to be stored in 7-bit Cursor A drain latency value 0 use 32 as precision multiplier to increase precision to be stored in 7-bit Cursor A drain latency value
30:24	0b RW	**CURSOR_A_DRAIN_LATENCY_VALUE:** [DevVLVP] For cursor latency, 4 BPP is assumed for all cursor formats. : Programmable drain latency value in time ticks per 64B FIFO entry
23	0b RW	**DISPLAY_SPRITE_B_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multiplier to increase precision to be stored in 7-bit Sprite B drain latency value 0 use 32 as precision multiplier to increase precision to be stored in 7-bit Sprite B drain latency value

Bit Range	Default & Access	Description
22:16	0b RW	**SPRITE_B_DRAIN_LATENCY_VALUE:** [DevVLVP] Programmable drain latency value in time ticks per 64B FIFO entry
15	0b RW	**DISPLAY_SPRITE_A_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multiplier to increase precision to be stored in 7-bit Sprite A drain latency value 0 use 32 as precision multiplier to increase precision to be stored in 7-bit Sprite A drain latency value
14:8	0b RW	**SPRITE_A_DRAIN_LATENCY_VALUE:** [DevVLVP] Programmable drain latency value in time ticks per 64B FIFO entry
7	0b RW	**DISPLAY_PLANE_A_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multiplier to increase precision to be stored in 7-bit Plane A drain latency value 0 use 32 as precision multiplier to increase precision to be stored in 7-bit Plane A drain latency value
6:0	0b RW	**DISPLAY_PLANE_A_DRAIN_LATENCY_VALUE:** [DevVLVP] Programmable drain latency value in time ticks per 64B FIFO entry

3.4.186 DDL2—Offset 70054h

Display FIFO Drain Latency 2

Access Method

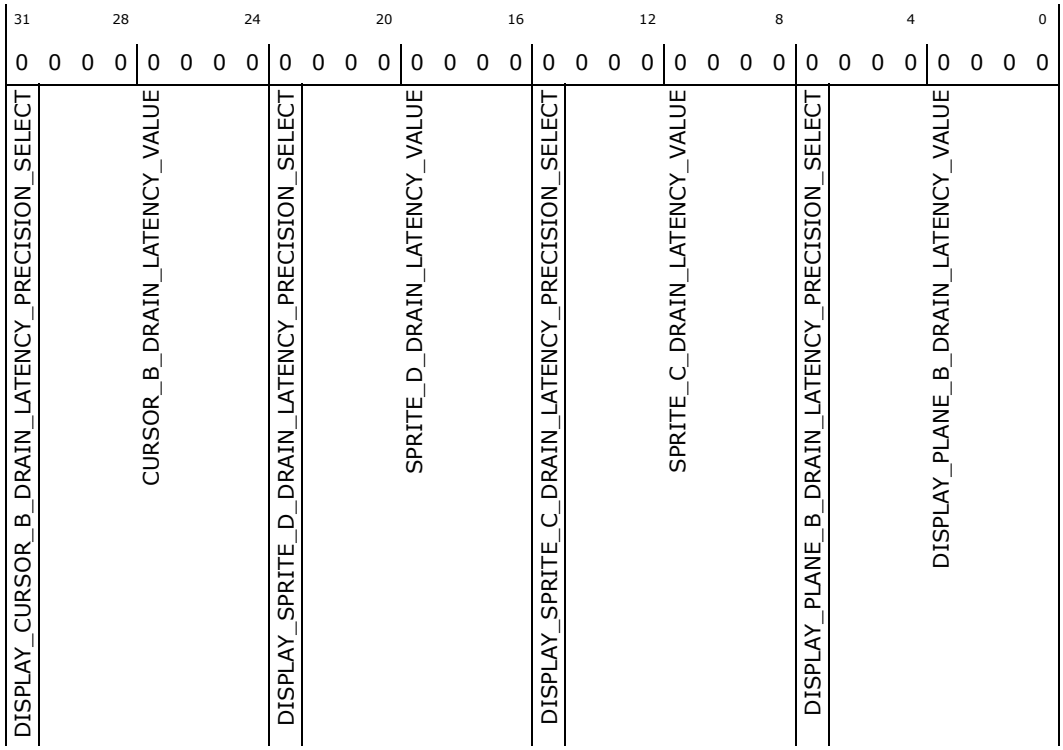
Type: Memory Mapped I/O Register (Size: 32 bits)

DDL2: [GTTMMADR_LSB + 2BF20h] + 70054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**DISPLAY_CURSOR_B_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multiplier to increase precision to be stored in 7-bit Cursor B drain latency value 0 use 32 as precision multiplier to increase precision to be stored in 7-bit Cursor B drain latency value
30:24	0b RW	**CURSOR_B_DRAIN_LATENCY_VALUE:** [DevVLVP] For cursor latency, 4 BPP is assumed for all cursor formats
23	0b RW	**DISPLAY_SPRITE_D_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multiplier to increase precision to be stored in 7-bit Sprite D drain latency value 0 use 32 as precision multiplier to increase precision to be stored in 7-bit Sprite D drain latency value
22:16	0b RW	**SPRITE_D_DRAIN_LATENCY_VALUE:** [DevVLVP]
15	0b RW	**DISPLAY_SPRITE_C_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multiplier to increase precision to be stored in 7-bit Sprite C drain latency value 0 use 32 as precision multiplier to increase precision to be stored in 7-bit Sprite C drain latency value
14:8	0b RW	**SPRITE_C_DRAIN_LATENCY_VALUE:** [DevVLVP]
7	0b RW	**DISPLAY_PLANE_B_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multiplier to increase precision to be stored in 7-bit Plane B drain latency value 0 use 32 as precision multiplier to increase precision to be stored in 7-bit Plane B drain latency value

Bit Range	Default & Access	Description
6:0	0b RW	**DISPLAY_PLANE_B_DRAIN_LATENCY_VALUE:** [DevVLVP]

3.4.187 DSPARB2—Offset 70060h

Display Arbitration Control 2

Access Method

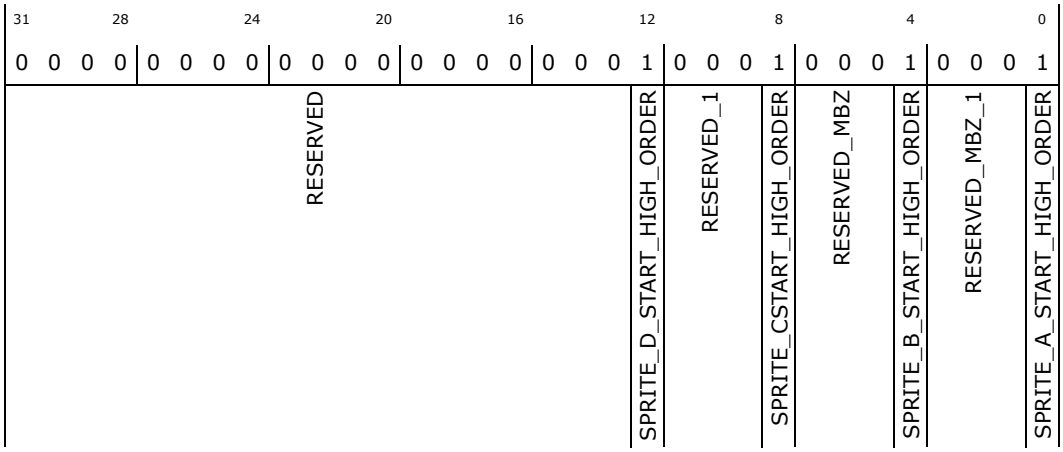
Type: Memory Mapped I/O Register (Size: 32 bits)

DSPARB2: [GTTMMADR_LSB + 2BF20h] + 70060h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00001111h



Bit Range	Default & Access	Description
31:13	0b RW	**RESERVED:** Reserved.
12	1b RW	**SPRITE_D_START_HIGH_ORDER:** This field is the high order bits for Sprite D Start pointer. Combined with lower order 8-bit Sprite D Start pointer, this field selects the end of the ram used for Sprite C and the start of the RAM for Sprite D. If sprite C is unused, this field can be set to the same value as Sprite C START. If Sprite D is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite C START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite C FIFO will be (Sprite D START-Sprite C START)*64. The size of the Sprite D FIFO will be (TOTALSIZE-Sprite D START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
11:9	0b RW	**RESERVED_1:** Reserved.

Bit Range	Default & Access	Description
8	1b RW	**SPRITE_CSTART_HIGH_ORDER:** This field is the high order bits for Sprite C Start pointer. Combined with lower order 8-bit Sprite C Start pointer, this field selects the end of the ram used for display B and the start of the RAM for Sprite C. If display B is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display B FIFO will be (Sprite C START)*64 bytes.
7:5	0b RW	**RESERVED_MBZ:** Reserved.
4	1b RW	**SPRITE_B_START_HIGH_ORDER:** This field is the high order bits for Sprite B Start pointer. Combined with lower order 8-bit Sprite B Start pointer, this field selects the end of the ram used for Sprite A and the start of the RAM for Sprite B. If sprite A is unused, this field can be set to the same value as Sprite A START. If Sprite B is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite A START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite A FIFO will be (Sprite B START-Sprite A START)*64. The size of the Sprite B FIFO will be (TOTALSIZE-Sprite B START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
3:1	0b RW	**RESERVED_MBZ_1:** Reserved.
0	1b RW	**SPRITE_A_START_HIGH_ORDER:** This field is the high order bits for Sprite A Start pointer. Combined with lower order 8-bit Sprite A Start pointer, this field selects the end of the ram used for display A and the start of the RAM for Sprite A. If display A is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display A FIFO will be (Sprite A START)*64 bytes.

3.4.188 DSPHOWM—Offset 70064h

Display FIFO WM High Order

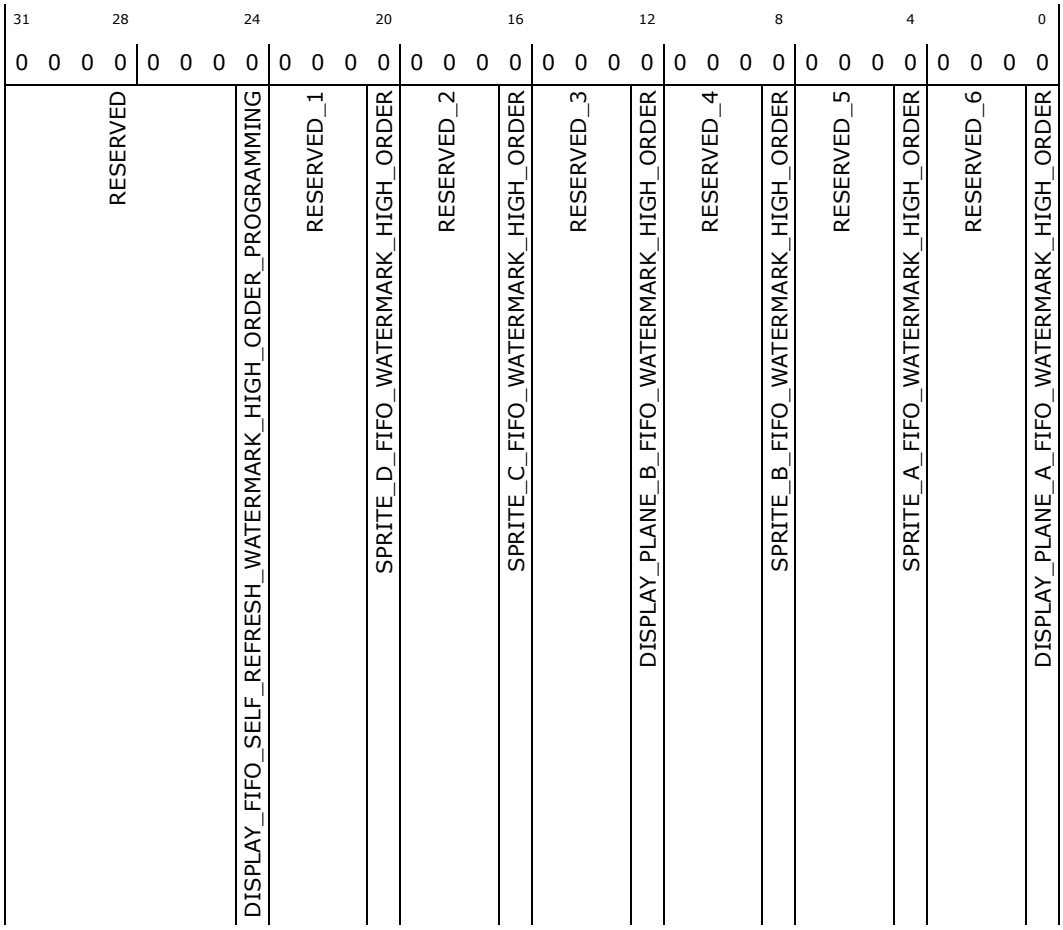
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPHOWM: [GTTMMADR_LSB + 2BF20h] + 70064h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RW	**RESERVED:** Reserved.
24	0b RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK_HIGH_ORDER_PROGRAMMING:** This field is the high order bit for the SR WM pointer . Combined with the lower order 9-bit SR FIFO WM pointer, it forms a 10-bit SR FIFO WM pointer. This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).Note [DevCL, DevCTG, DevCDV]: When calculating watermark values for 15/16bpp display formats, assume 32bpp for purposes of calculation using the high priority bandwidth analysis spreadsheet.
23:21	0b RW	**RESERVED_1:** Reserved.

Bit Range	Default & Access	Description
20	0b RW	**SPRITE_D_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite D FIFO WM. Combined with lower order 8-bit Sprite D FIFO WM, it forms a 9-bit Sprite D FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
19:17	0b RW	**RESERVED_2:** Reserved.
16	0b RW	**SPRITE_C_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite C FIFO WM. Combined with lower order 8-bit Sprite C FIFO WM, it forms a 9-bit Sprite C FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
15:13	0b RW	**RESERVED_3:** Reserved.
12	0b RW	**DISPLAY_PLANE_B_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Display B FIFO WM. Combined with lower order 8-bit Display B FIFO WM, it forms a 9-bit Display B FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
11:9	0b RW	**RESERVED_4:** Reserved.
8	0b RW	**SPRITE_B_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite B FIFO WM. Combined with lower order 8-bit Sprite B FIFO WM, it forms a 9-bit Sprite B FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:5	0b RW	**RESERVED_5:** MBZ
4	0b RW	**SPRITE_A_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite A FIFO WM. Combined with lower order 8-bit Sprite A FIFO WM, it forms a 9-bit Sprite A FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
3:1	0b RW	**RESERVED_6:** MBZ
0	0b RW	**DISPLAY_PLANE_A_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Display A FIFO WM. Combined with lower order 8-bit Display A FIFO WM, it forms a 9-bit Display A FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

3.4.189 DSPHOWM1—Offset 70068h

Display FIFO WM1 High Order

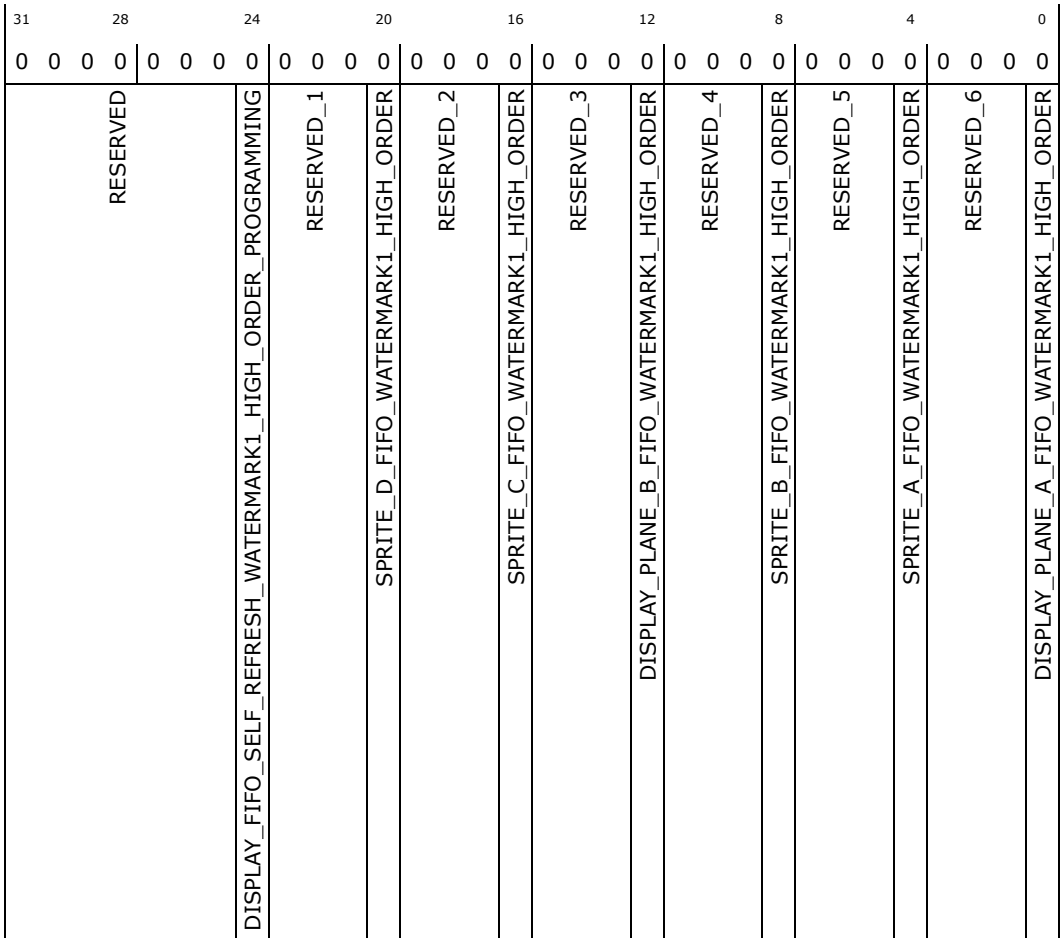
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPHOWM1: [GTTMMADR_LSB + 2BF20h] + 70068h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
24	0b RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK1_HIGH_ORDER_PROGRAMMING:** This field is the high order bit for the SR WM1 pointer . Combined with the lower order 9-bit SR FIFO WM1 pointer, it forms a 10-bit SR FIFO WM1 pointer. This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).Note [DevCL, DevCTG, DevCDV]: When calculating watermark values for 15/16bpp display formats, assume 32bpp for purposes of calculation using the high priority bandwidth analysis spreadsheet.
23:21	0b RW	**RESERVED_1:** Reserved.
20	0b RW	**SPRITE_D_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite D FIFO WM1. Combined with lower order 8-bit Sprite D FIFO WM1, it forms a 9-bit Sprite D FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
19:17	0b RW	**RESERVED_2:** Reserved.
16	0b RW	**SPRITE_C_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite C FIFO WM1. Combined with lower order 8-bit Sprite C FIFO WM1, it forms a 9-bit Sprite C FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
15:13	0b RW	**RESERVED_3:** Reserved.
12	0b RW	**DISPLAY_PLANE_B_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Display B FIFO WM1. Combined with lower order 8-bit Display B FIFO WM1, it forms a 9-bit Display B FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
11:9	0b RW	**RESERVED_4:** Reserved.
8	0b RW	**SPRITE_B_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite B FIFO WM1. Combined with lower order 8-bit Sprite B FIFO WM1, it forms a 9-bit Sprite B FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:5	0b RW	**RESERVED_5:** MBZ

Bit Range	Default & Access	Description
4	0b RW	**SPRITE_A_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite A FIFO WM1. Combined with lower order 8-bit Sprite A FIFO WM1, it forms a 9-bit Sprite A FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
3:1	0b RW	**RESERVED_6:** MBZ
0	0b RW	**DISPLAY_PLANE_A_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Display A FIFO WM1. Combined with lower order 8-bit Display A FIFO WM1, it forms a 9-bit Display A FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

3.4.190 FW4—Offset 70070h

Display FIFO Watermark1 Control 4

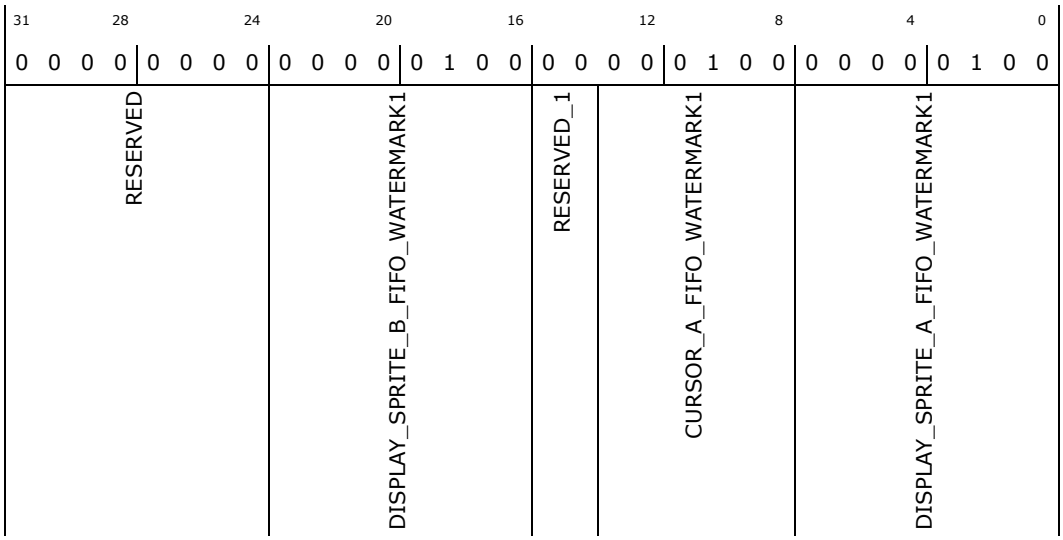
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FW4: [GTTMMADR_LSB + 2BF20h] + 70070h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00040404h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** : MBZ
23:16	00000100b RW	**DISPLAY_SPRITE_B_FIFO_WATERMARK1:** [DevCDV] Number in 64Bs of space in FIFO above which the Display Sprite B Stream will generate request with status 2
15:14	0b RW	**RESERVED_1:** : MBZ
13:8	000100b RW	**CURSOR_A_FIFO_WATERMARK1:** DevCDV] Number in 64Bs of space in the Cursor A FIFO above which the Cursor A Stream will generate requests with status 2 to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:0	00000100b RW	**DISPLAY_SPRITE_A_FIFO_WATERMARK1:** DevCDV] Number in 64Bs of space in FIFO above which the Display Sprite A Stream will generate request with status 2 (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

3.4.191 FW5—Offset 70074h

Display FIFO Watermark1 Control 5

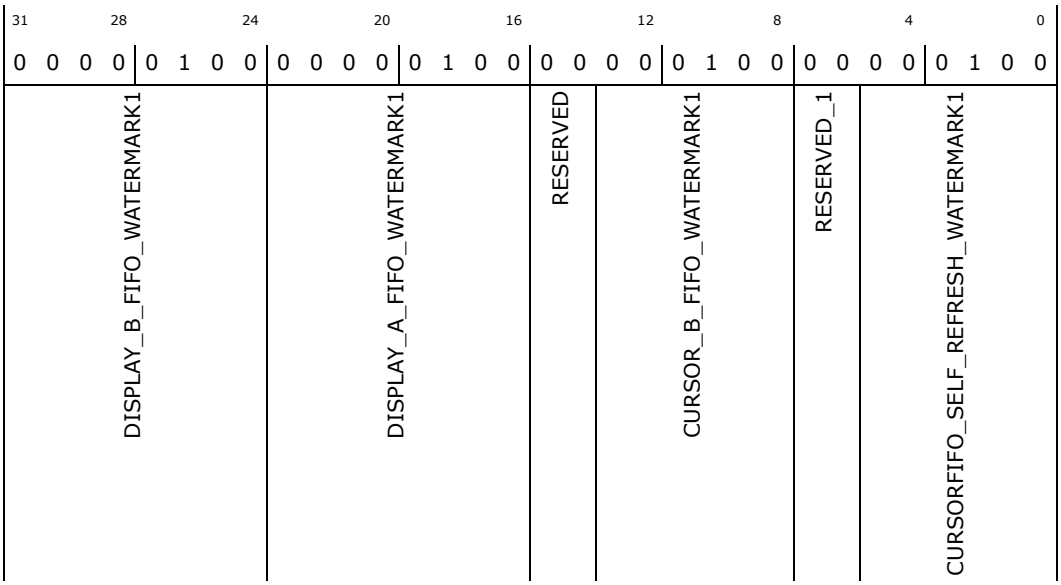
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FW5: [GTTMMADR_LSB + 2BF20h] + 70074h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 04040404h



Bit Range	Default & Access	Description
31:24	00000100b RW	**DISPLAY_B_FIFO_WATERMARK1:** [DevCDV] Number in 64Bs of space in FIFO above which the Display B Stream will generate request with status 2
23:16	00000100b RW	**DISPLAY_A_FIFO_WATERMARK1:** [DevCDV] Number in 64Bs of space in FIFO above which the Display A Stream will generate request with status 2
15:14	0b RW	**RESERVED:** : MBZ
13:8	000100b RW	**CURSOR_B_FIFO_WATERMARK1:** DevCDV] Number in 64Bs of space in the Cursor B FIFO above which the Cursor B Stream will generate requests with status 2 to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:6	0b RW	**RESERVED_1:** : MBZ
5:0	000100b RW	**CURSORFIFO_SELF_REFRESH_WATERMARK1:** DevCDV] Number in 64Bs of space in FIFO above which the Display Cursor Stream will generate request with status 2 during memory SR (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

3.4.192 FW6—Offset 70078h

Display FIFO Watermark1 Control 6

Access Method

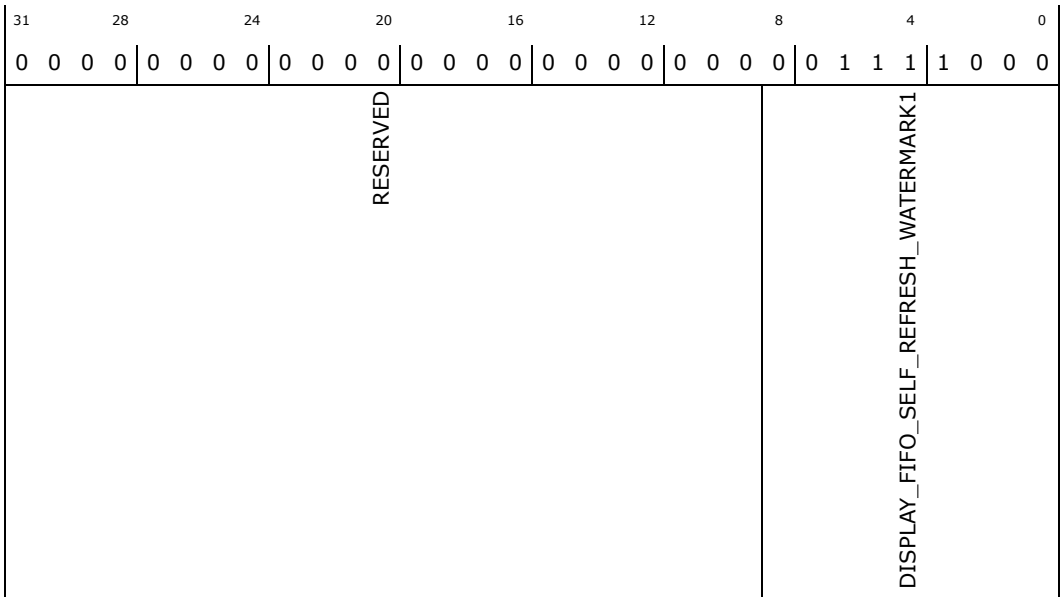
Type: Memory Mapped I/O Register (Size: 32 bits)

FW6: [GTTMMADR_LSB + 2BF20h] + 70078h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000078h



Bit Range	Default & Access	Description
31:9	0b RW	**RESERVED:** : MBZ
8:0	001111000b RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK1:** DevCDV] Number in 64Bs of space in FIFO above which the Display A/B Streamer will generate request with status 2 during max fifo mode (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

3.4.193 FW7—Offset 7007Ch

Display FIFO Watermark Control 7

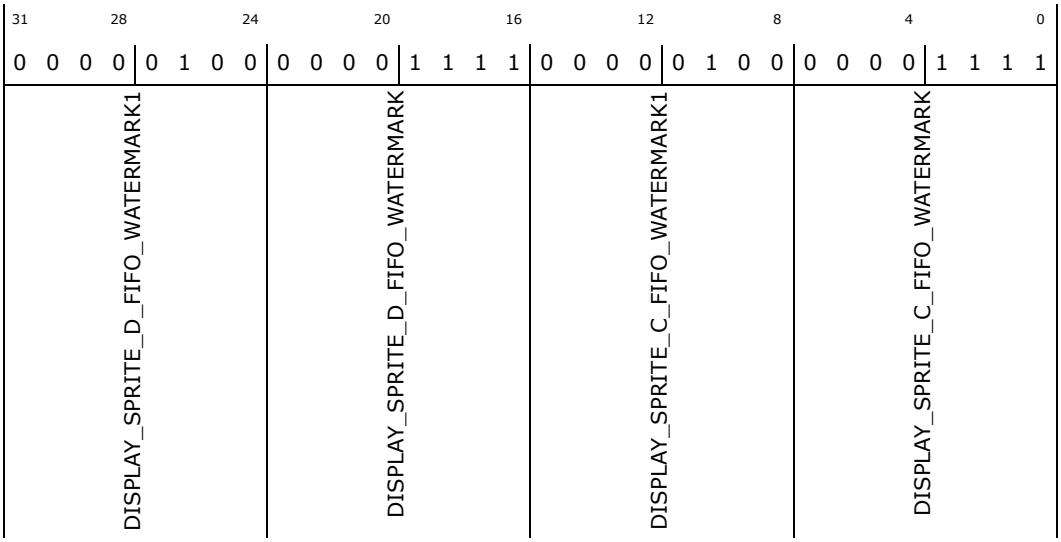
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FW7: [GTTMMADR_LSB + 2BF20h] + 7007Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 040F040Fh



Bit Range	Default & Access	Description
31:24	00000100b RW	**DISPLAY_SPRITE_D_FIFO_WATERMARK1:** [DevVLVP] Number in 64Bs of space in FIFO above which the Display Sprite D Stream will generate request with status 2
23:16	00001111b RW	**DISPLAY_SPRITE_D_FIFO_WATERMARK:** [DevVLVP] Number in 64Bs of space in FIFO above which the Display Sprite D Stream will generate request with status 2

Bit Range	Default & Access	Description
15:8	00000100b RW	**DISPLAY_SPRITE_C_FIFO_WATERMARK1:** DevVLVP] Number in 64Bs of space in FIFO above which the Display Sprite C Stream will generate request with status 2
7:0	00001111b RW	**DISPLAY_SPRITE_C_FIFO_WATERMARK:** DevVLVP] Number in 64Bs of space in FIFO above which the Display Sprite C Stream will generate request with status 2

3.4.194 CURACNTR—Offset 70080h

Cursor A Control Register

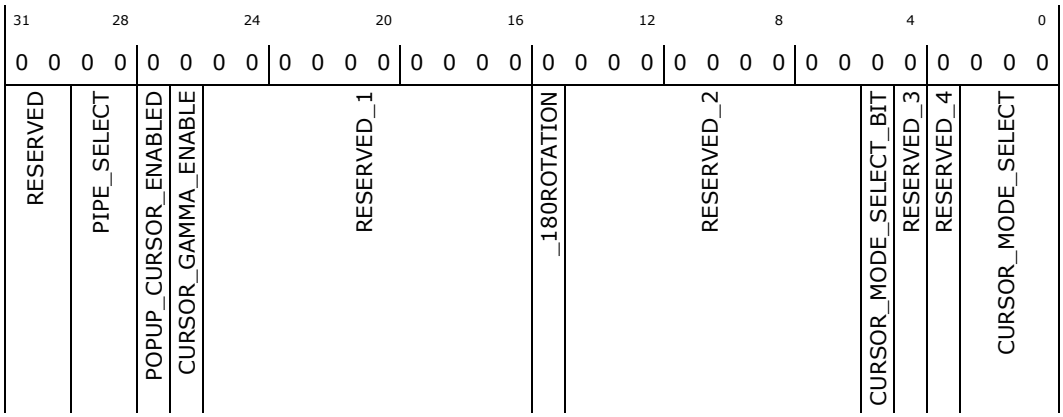
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CURACNTR: [GTTMMADR_LSB + 2BF20h] + 70080h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** Write as zero.
29:28	0b RW	**PIPE_SELECT:** [DevBW, DevCL, DevCDV] A state machine handles the synchronization of the switch to both vertical blank signals. So as far as the software is concerned, when both display pipes are being used, it can be switched at any time; the hardware will synchronize the switch. 00 = HW cursor is attached to Display Pipe A. This is the default after reset. 01 = HW cursor is attached to Display Pipe B. 10 = Reserved for pipe C 11 = Reserved for pipe D [DevBLC] and [DevCTG] Reserved: Write as zero.
27	0b RW	**POPUP_CURSOR_ENABLED:** . This bit should be turned on when using Cursor A as a popup cursor. When in popup mode, hardware interprets the cursor base address as a physical address instead of a graphics address.0 = Cursor A is hi-res 1 = Cursor A is popup

Bit Range	Default & Access	Description
26	0b RW	**CURSOR_GAMMA_ENABLE:** This bit only has an effect when using the cursor in a non-VGA mode. In VGA pop-up operation, the cursor data will always bypass the gamma (palette) unit. 0 = Cursor pixel data bypasses gamma correction or palette (default). 1 = Cursor pixel data is gamma to be corrected in the pipe.
25:16	0b RW	**RESERVED_1:** Write as zero
15	0b RW	**_180ROTATION:** This mode causes the cursor to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 = No rotation 1 = 180 Rotation of 32 bit per pixel cursors
14:6	0b RW	**RESERVED_2:** Reserved.
5	0b RW	**CURSOR_MODE_SELECT_BIT:** See following table.
4	0b RW	**RESERVED_3:** Reserved.
3	0b RW	**RESERVED_4:** Reserved.
2:0	0b RW	**CURSOR_MODE_SELECT:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

3.4.195 CURABASE—Offset 70084h

Cursor A Base Address Register

Access Method

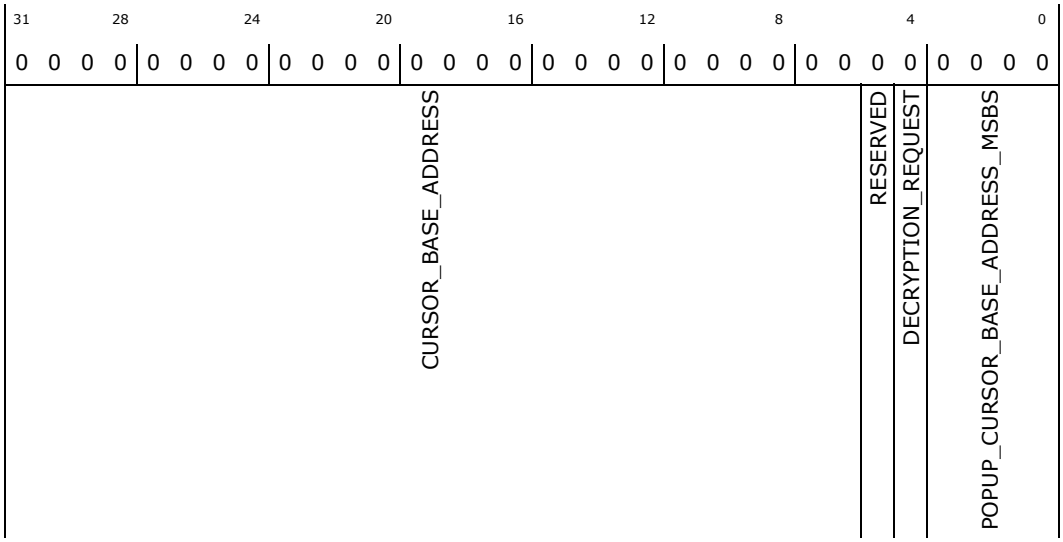
Type: Memory Mapped I/O Register (Size: 32 bits)

CURABASE: [GTTMMADR_LSB + 2BF20h] + 70084h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**CURSOR_BASE_ADDRESS:** . This field specifies bits 31:6 of the graphics address of the base of the cursor. On [DevBW] and [DevCL] if the cursor is a popup, this field specifies bits 31:6 of the physical address of the base of the cursor, and bits 35:32 of the address are specified in the LSBs of this register. Popup cursor mode is selected within the CURACNTR register.The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the cursor data in its unrotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double-buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update is also postponed if a write sequence is in progress. It is assumed that if the cursor mode is changed, the cursor image will also be changed. To prevent the cursor from appearing when it is only partially programmed, the active registers will not be updated until both the cursor control and base address registers have been programmed. If the cursor control register is written, the cursor base address must also be written before the change will be effective. However, the base address register may be changed (e.g., to change the shape of the cursor) without also writing to the control register. If both are to be written, the control register must be written first.
5	0b RW	**RESERVED:** MBZ

Bit Range	Default & Access	Description
4	0b RW	**DECRYPTION_REQUEST:** This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0b RW	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

3.4.196 CURAPOS—Offset 70088h

Cursor A Position Register

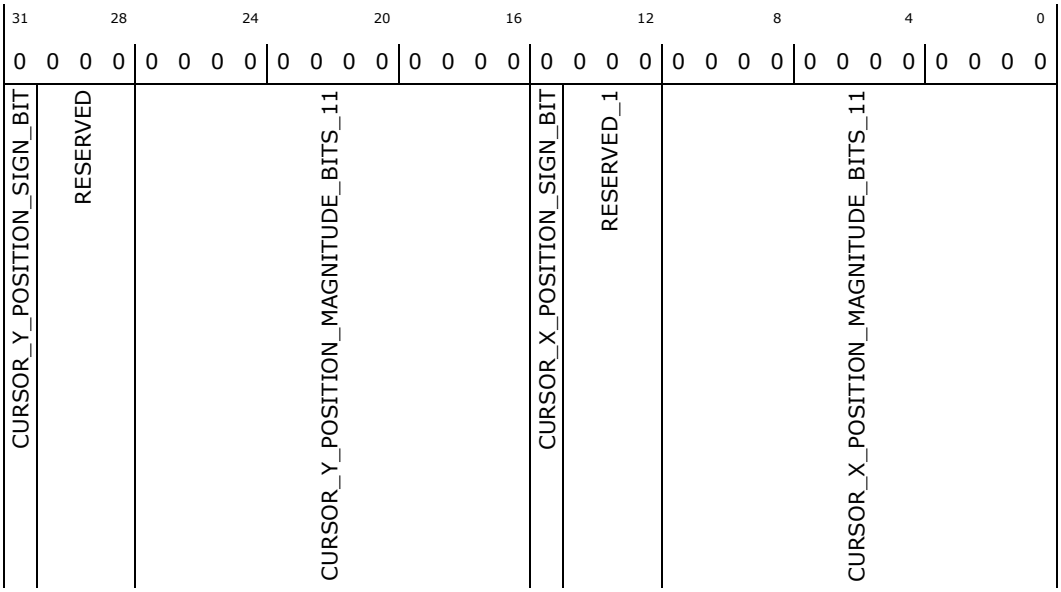
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CURAPOS: [GTTMMADR_LSB + 2BF20h] + 70088h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**CURSOR_Y_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen. For use as a VGA Popup, the entire cursor must be positioned over the active area of the VGA image.
30:28	0b RW	**RESERVED:** Write as zero.
27:16	0b RW	**CURSOR_Y_POSITION_MAGNITUDE_BITS_11:** 0: This register provides the magnitude bits of a signed 12-bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. (default is 0). For use as a VGA Popup, the entire cursor must be positioned over the active area of the VGA image. Enabling the border in VGA (VGA Border Enable bit in the VGA Config register) includes the border in what is considered the active area . For HDMI modes where the vertical zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.
15	0b RW	**CURSOR_X_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen. For use as a VGA Popup, the entire cursor must be positioned over the active area of the VGA image. Enabling the border in VGA (VGA Border Enable bit in the VGA Config register) includes the border in what is considered the active area .
14:12	0b RW	**RESERVED_1:** Write as zero.
11:0	0b RW	**CURSOR_X_POSITION_MAGNITUDE_BITS_11:** 0: These 12 bits provide the signed 13-bit value that specifies the horizontal position of cursor. The sign bit is provided by bit 15 of this register. (default is 0) For HDMI modes where the horizontal zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the end of the active video area in the unrotated orientation.

3.4.197 CURAPALET_0—Offset 70090h

Cursor A Palette registers (4 Registers)

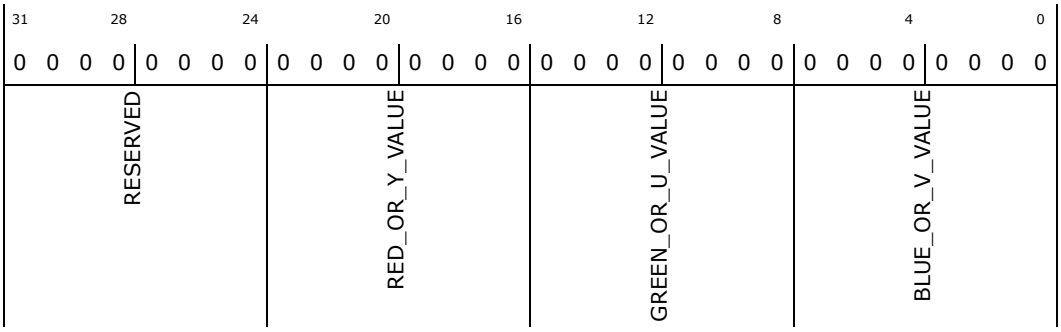
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CURAPALET_0: [GTTMMADR_LSB + 2BF20h] + 70090h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

3.4.198 CURAPALET_1—Offset 70094h

Cursor A Palette registers (4 Registers)

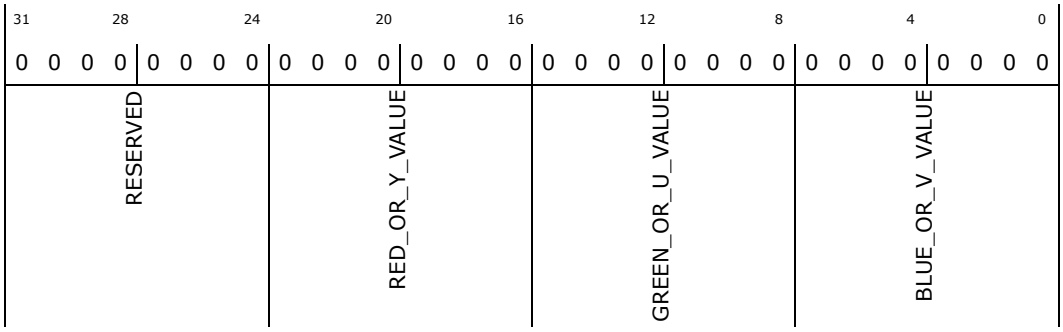
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CURAPALET_1: [GTTMMADR_LSB + 2BF20h] + 70094h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

3.4.199 CURAPALET_2—Offset 70098h

Cursor A Palette registers (4 Registers)

Access Method

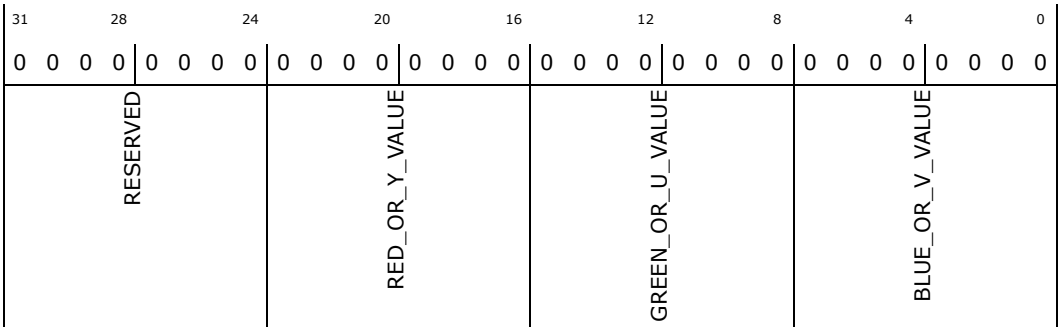
Type: Memory Mapped I/O Register (Size: 32 bits)

CURAPALET_2: [GTTMMADR_LSB + 2BF20h] + 70098h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

3.4.200 CURAPALET_3—Offset 7009Ch

Cursor A Palette registers (4 Registers)

Access Method

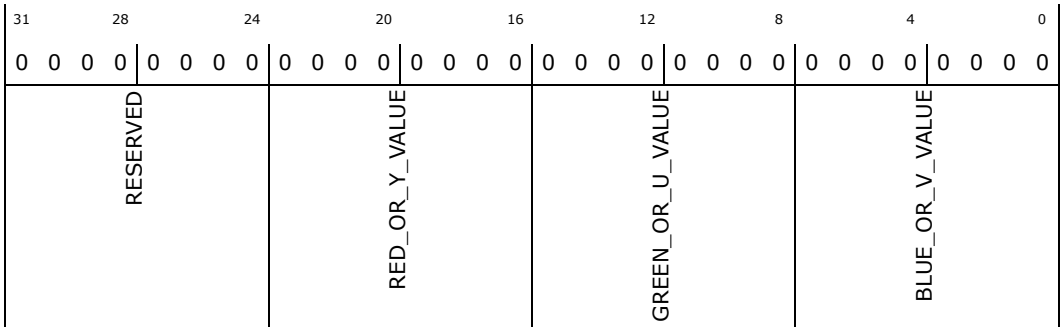
Type: Memory Mapped I/O Register (Size: 32 bits)

CURAPALET_3: [GTTMMADR_LSB + 2BF20h] + 7009Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

3.4.201 CURALIVEBASE—Offset 700ACh

Cursor A Live Base Address Register

Access Method

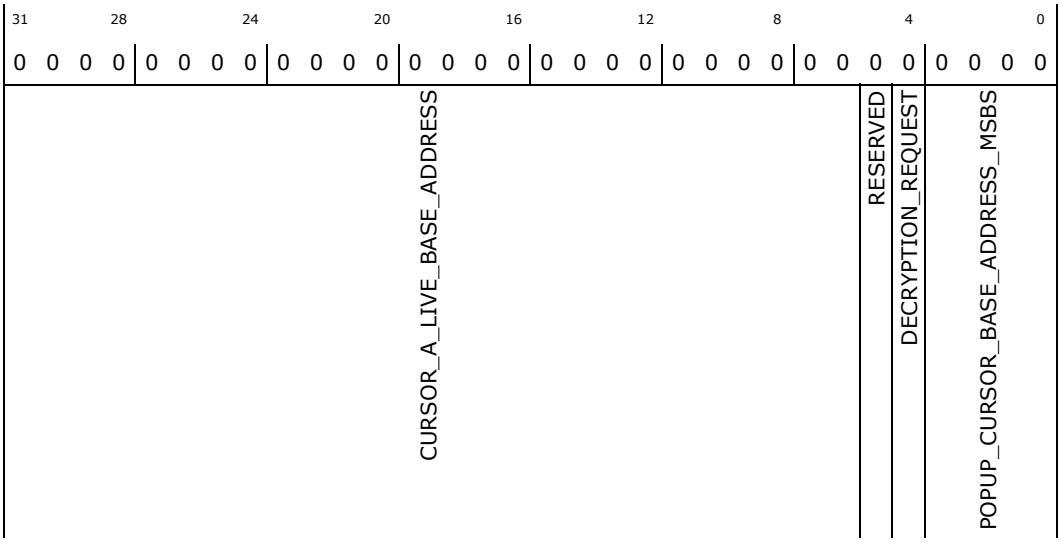
Type: Memory Mapped I/O Register (Size: 32 bits)

CURALIVEBASE: [GTTMMADR_LSB + 2BF20h] + 700ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RO	**CURSOR_A_LIVE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for the plane.
5	0b RO	**RESERVED:** MBZ
4	0b RO	**DECRYPTION_REQUEST:** This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0b RO	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

3.4.202 CURBCNTR—Offset 700C0h

Cursor B Control Register

Access Method

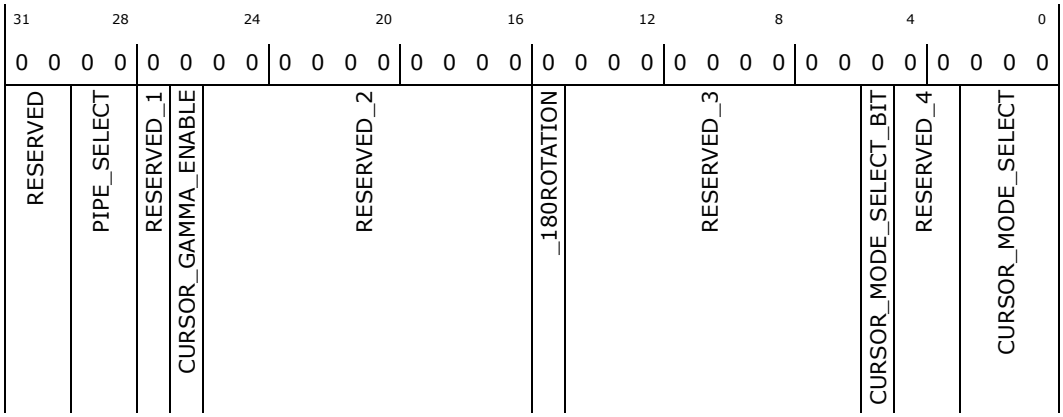
Type: Memory Mapped I/O Register (Size: 32 bits)

CURBCNTR: [GTTMMADR_LSB + 2BF20h] + 700C0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RW	**RESERVED:** Write as zero.
29:28	0b RW	**PIPE_SELECT:** [DevBW, DevCL, DevCDV]: A state machine handles the synchronization of the switch to both vertical blank signals. So as far as the software is concerned, when both display pipes are being used, it can be switched at any time; the hardware will synchronize the switch. 00 = HW cursor is attached to Display Pipe A. This is the default after reset. 01 = HW cursor is attached to Display Pipe B. 10 = Reserved for to Display Pipe C. 11 = Reserved for to Display Pipe D. Reserved [DevBLC] and [DevCTG]: Write as zero.
27	0b RW	**RESERVED_1:** Write as zero.
26	0b RW	**CURSOR_GAMMA_ENABLE:** 0 = Cursor pixel data bypasses gamma correction (default). 1 = Cursor pixel data is gamma to be corrected.
25:16	0b RW	**RESERVED_2:** Reserved.
15	0b RW	**_180ROTATION:** This mode causes the cursor to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 = No rotation 1 = 180 Rotation of 32 bit per pixel cursors
14:6	0b RW	**RESERVED_3:** Write as zero
5	0b RW	**CURSOR_MODE_SELECT_BIT:** See following table.
4:3	0b RW	**RESERVED_4:** reserved
2:0	0b RW	**CURSOR_MODE_SELECT:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

3.4.203 CURBBASE—Offset 700C4h

Cursor B Base Address Register

Access Method

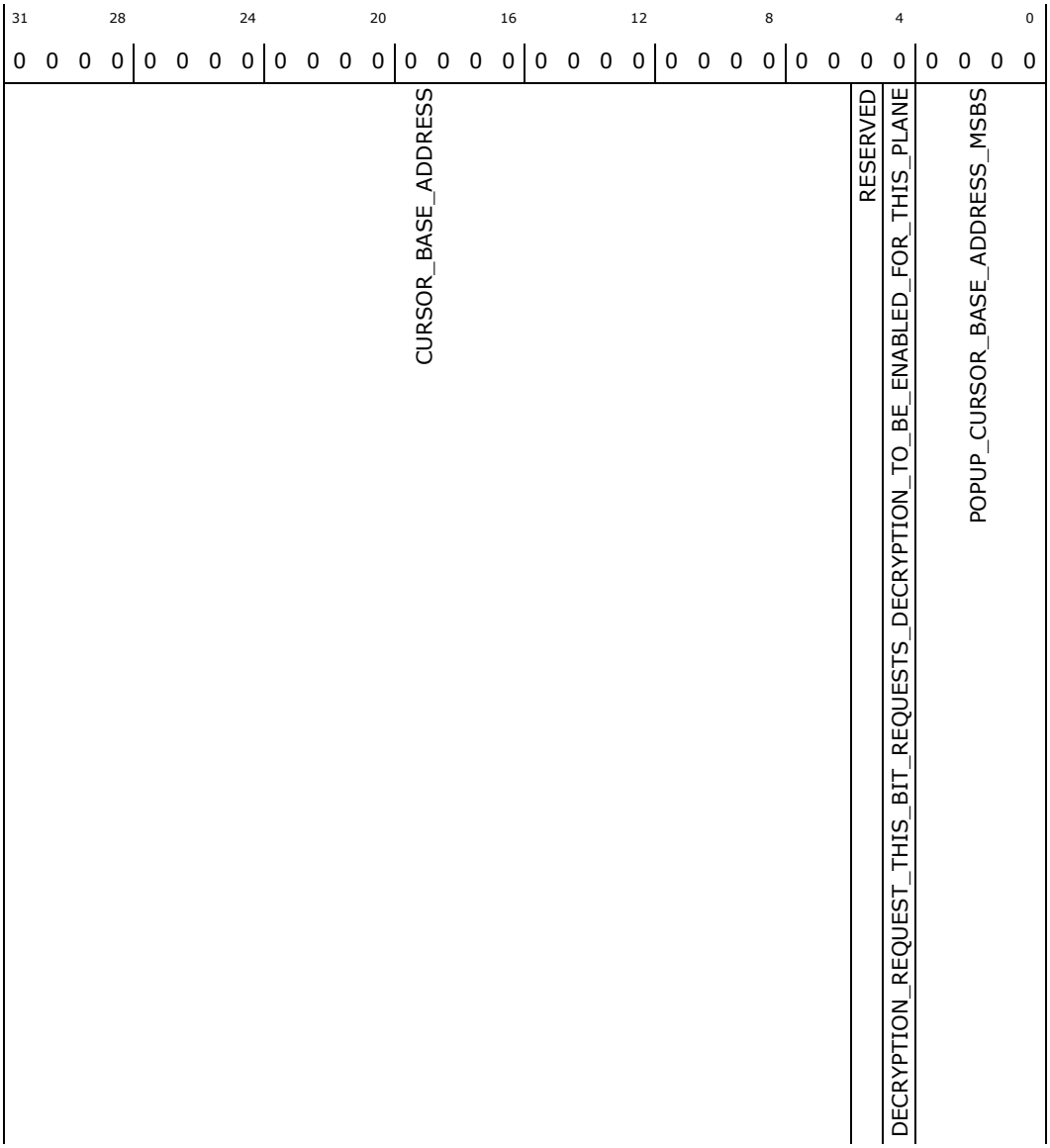
Type: Memory Mapped I/O Register (Size: 32 bits)

CURBBASE: [GTTMMADR_LSB + 2BF20h] + 700C4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**CURSOR_BASE_ADDRESS:** This register specifies the graphics address of the entire cursor. It also acts as a trigger event to force the update of active registers on the next display event. The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the cursor data in its unrotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double-buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update is also postponed if a write sequence is in progress. It is assumed that if the cursor mode is changed, the cursor image will also be changed. To prevent the cursor from appearing when it is only partially programmed, the active registers will not be updated until both the cursor control and base address registers have been programmed. If the cursor control register is written, the cursor base address must also be written before the change will be effective. However, the base address register may be changed (e.g., to change the shape of the cursor) without also writing to the control register. If both are to be written, the control register must be written first.
5	0b RW	**RESERVED:** MBZ
4	0b RW	**DECRYPTION_REQUEST_THIS_BIT_REQUESTS_DECRYPTION_TO_BE_ENABLED_FOR_THIS_PLANE:** This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0b RW	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

3.4.204 CURBPOS—Offset 700C8h

Cursor B Position Register

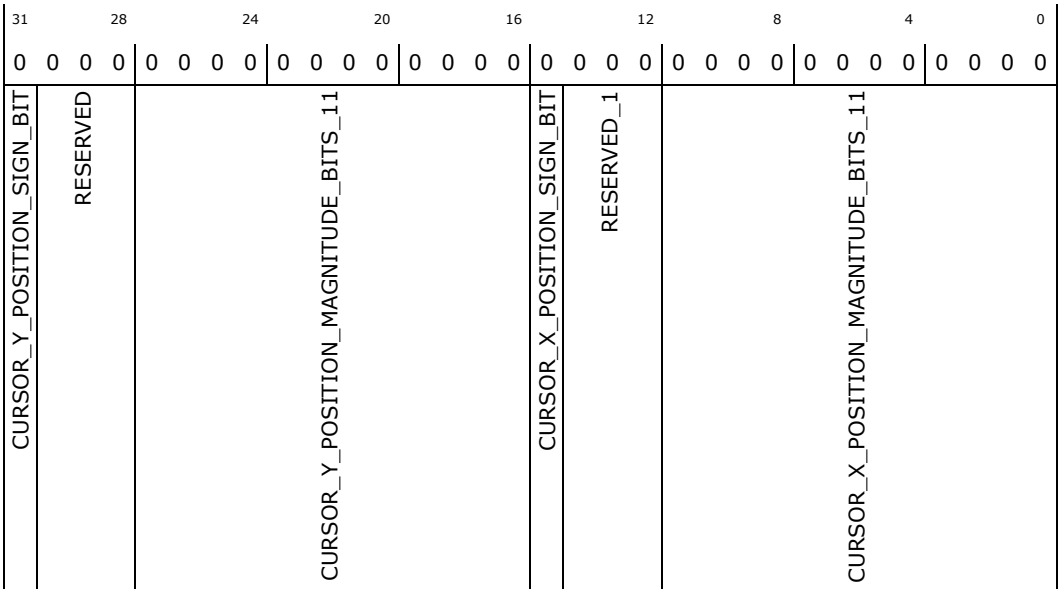
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CURBPOS: [GTTMMADR_LSB + 2BF20h] + 700C8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**CURSOR_Y_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen.
30:28	0b RW	**RESERVED:** Write as zero.
27:16	0b RW	**CURSOR_Y_POSITION_MAGNITUDE_BITS_11:** 0: This register provides the magnitude bits of a signed 13-bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. (default is 0) When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.
15	0b RW	**CURSOR_X_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen. For HDMI modes where the vertical zoom is greater than 1x, the position is specified using the zoomed grid.
14:12	0b RW	**RESERVED_1:** Write as zero.
11:0	0b RW	**CURSOR_X_POSITION_MAGNITUDE_BITS_11:** 0: These 12 bits provide the signed 13-bit value that specifies the horizontal position of cursor. The sign bit is provided by bit 15 of this register. (default is 0) For HDMI modes where the horizontal zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.

3.4.205 CURBPALET_0—Offset 700D0h

Cursor B Palette registers (4 Registers)

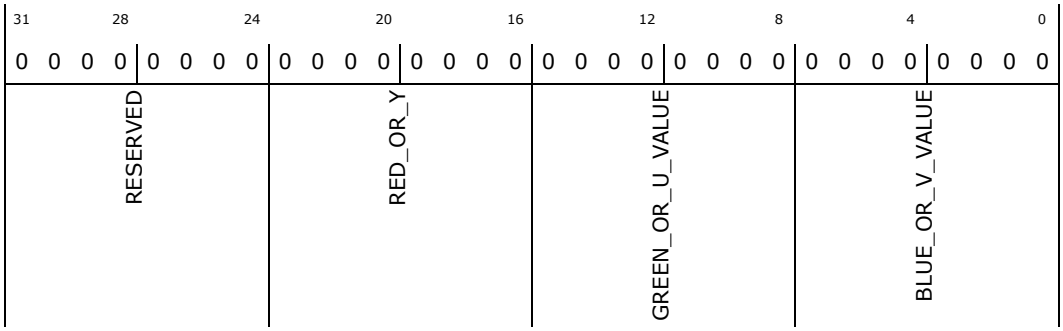
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CURBPALET_0: [GTTMMADR_LSB + 2BF20h] + 700D0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y:** RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

3.4.206 CURBPALET_1—Offset 700D4h

Cursor B Palette registers (4 Registers)

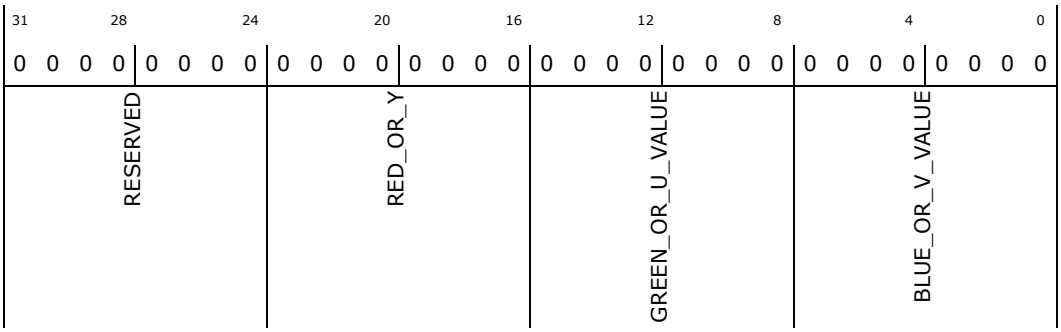
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CURBPALET_1: [GTTMMADR_LSB + 2BF20h] + 700D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y:** RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

3.4.207 CURBPALET_2—Offset 700D8h

Cursor B Palette registers (4 Registers)

Access Method

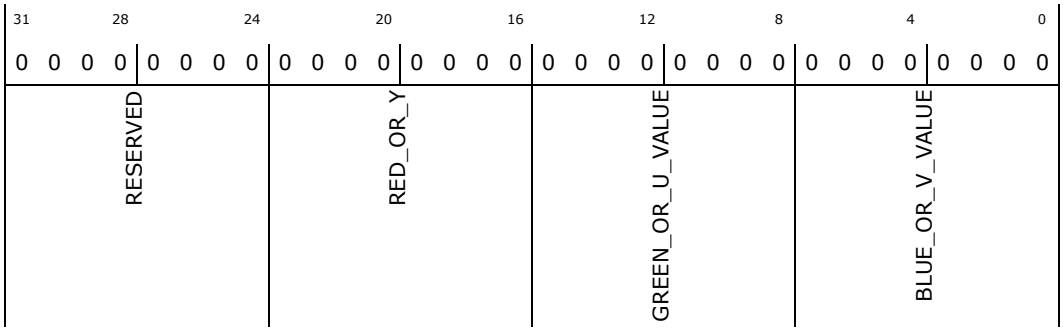
Type: Memory Mapped I/O Register (Size: 32 bits)

CURBPALET_2: [GTTMMADR_LSB + 2BF20h] + 700D8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y:** RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

3.4.208 CURBPALET_3—Offset 700DCh

Cursor B Palette registers (4 Registers)

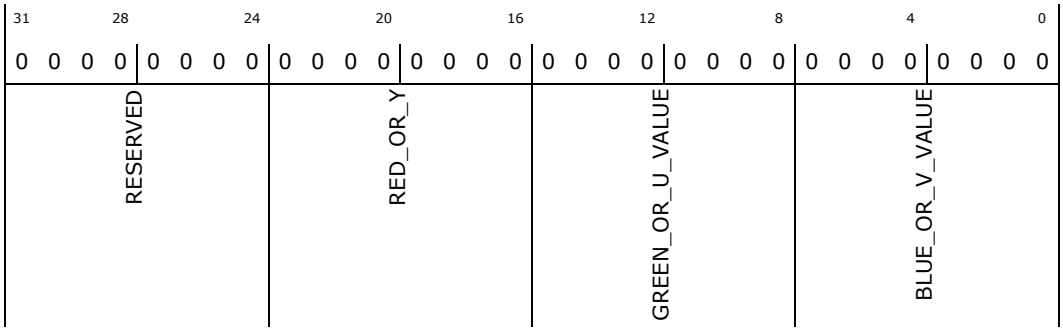
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CURBPALET_3: [GTTMMADR_LSB + 2BF20h] + 700DCh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y:** RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

3.4.209 CURBLIVEBASE—Offset 700ECh

Cursor B Live Base Address Register

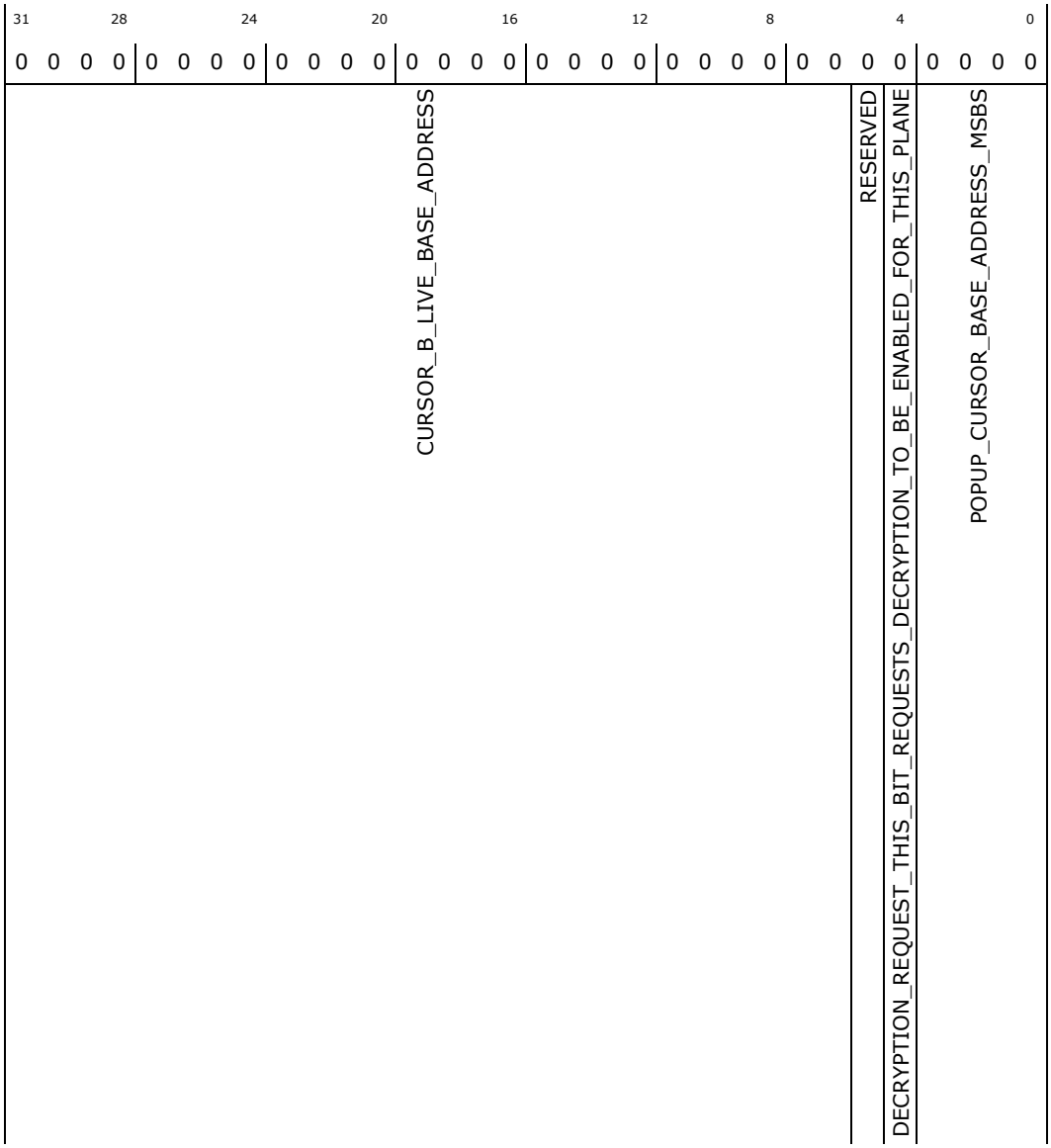
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CURBLIVEBASE: [GTTMMADR_LSB + 2BF20h] + 700ECh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RO	**CURSOR_B_LIVE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Cursor B plane.
5	0b RO	**RESERVED:** MBZ

Bit Range	Default & Access	Description
4	0b RO	**DECRYPTION_REQUEST_THIS_BIT_REQUESTS_DECRYPTION_TO_BE_ENABLED_FOR_THIS_PLANE:** This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0b RO	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

3.4.210 DSPAADDR—Offset 7017Ch

Display A Async flip Start Address Register

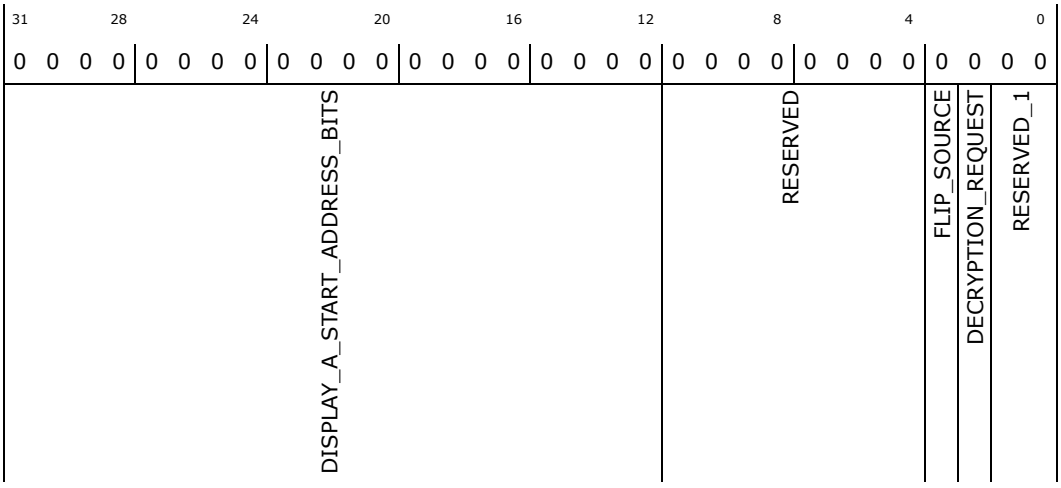
Access Method

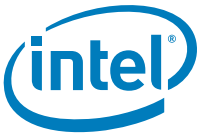
Type: Memory Mapped I/O Register (Size: 32 bits)

DSPAADDR: [GTTMMADR_LSB + 2BF20h] + 7017Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31:12	0b RW	**DISPLAY_A_START_ADDRESS_BITS:** This register provides the start address of the display A plane or the first eye when running in stereo mode. This address must be at least pixel aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . Write to this register triggers async flip. The async flip address is written into the Display A Base Address register 0x7019C
11:4	0b RW	**RESERVED:** MBZ
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0b RW	**RESERVED_1:** MBZ

3.4.211 DSPACNTR—Offset 70180h

Display A Plane Control Register

Access Method

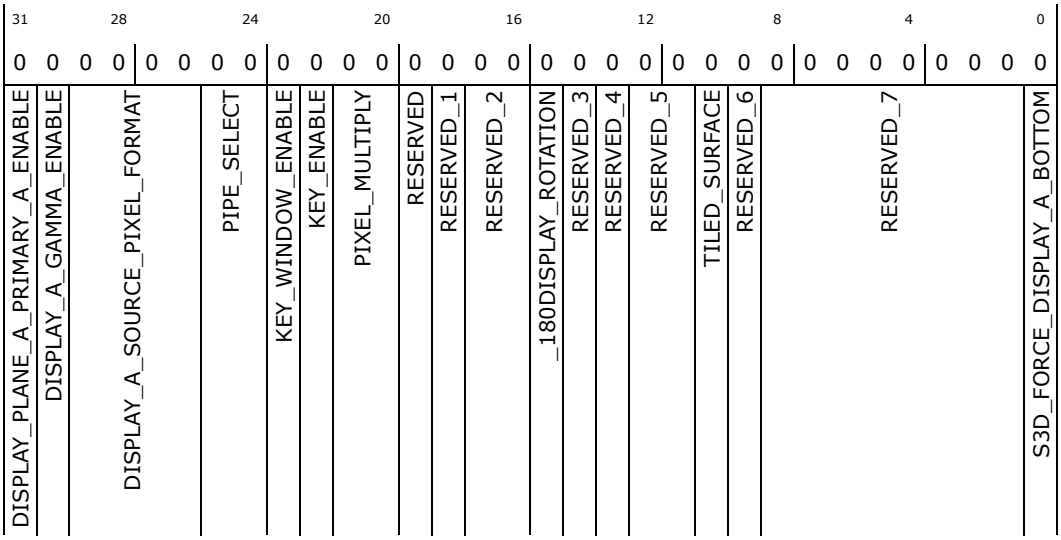
Type: Memory Mapped I/O Register (Size: 32 bits)

DSPACNTR: [GTTMMADR_LSB + 2BF20h] + 70180h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**DISPLAY_PLANE_A_PRIMARY_A_ENABLE:** When this bit is set, the primary plane will generate pixels for display. When set to zero, display plane A memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that display A is assigned. The display pipe must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. 1 = Enable 0 = Disable
30	0b RW	**DISPLAY_A_GAMMA_ENABLE:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane s pixel data only. For 8-bit indexed display data, this bit should be set to a one. 0 = Display A pixel data bypasses the display pipe gamma correction logic (default). 1 = Display A pixel data is gamma corrected in the display pipe gamma correction logic.
29:26	0b RW	**DISPLAY_A_SOURCE_PIXEL_FORMAT:** These bits should only be changed after the plane has been disabled. Pixel formats with an alpha channel (8:8:8:8) should not use source keying. Pixel format of 8-bit indexed uses the palette. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 000x = Reserved. 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format. (with pre-multiplied alpha color format) 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format. (with pre-multiplied alpha color format) 1010 = 32-bit BGRX (10:10:10:2) pixel format Ignore alpha 1011 = 32-bit BGRA (10:10:10:2) pixel format (with pre-multiplied alpha color format) 1100 = 64-bit RGBX (16:16:16:16) 16 bit floating point pixel format. Ignore alpha. 1101 = 64-bit RGBA (16:16:16:16) 16-bit floating point pixel format (with pre-multiplied color format) 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8) pixel format (with pre-multiplied color format)
25:24	0b RO	**PIPE_SELECT:** Plane A always ties to Pipe A. AccessType: Read Only Reserved

Bit Range	Default & Access	Description
23	0b RW	**KEY_WINDOW_ENABLE:** . This bit applies only to devices with a display plane C. This bit is set to one when the color key is used as a destination key for display C. Display plane C must be enabled on the same pipe and it s Z-order should be programmed to be behind display A for this to be set to a one.0 = Source Key applies to entire display plane A 1 = Source Key applies to only pixels within the intersection between Display A and Display C [DevBLC] and [DevCTG]: Reserved
22	0b RW	**KEY_ENABLE:** . This bit enables source keying for display A. Source keying allows a plane that is behind (below) this plane to show through where the display A key matches the display A data. This function is overloaded to provide display C destination keying when combined with the key window enable bit. Setting this bit is not allowed when the display pixel format includes an alpha channel.0 = Source key is disabled 1 = Source key is enabled [DevBLC] and [DevCTG]: Reserved In destination keying, primary plane pixel will be made transparent when blending with sprite pixel as the destination if the primary src key matches with the primary pixel value.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the pixel multiply mode, the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes: Asynchronous flips are not permitted when pixel multiply is enabled. 00 = No duplication 01 = Line/pixel Doubling 10 = Reserved 11 = Pixel Doubling only
19	0b RW	**RESERVED:** Software must preserve the contents of this bit.
18	0b RW	**RESERVED_1:** Write as zero
17:16	0b RW	**RESERVED_2:** Software must preserve the contents of this bit.
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. [DevCL] Do not enable 180 rotation together with Frame Buffer Compression0 = No rotation 1 = 180 rotation
14	0b RW	**RESERVED_3:** [DevBW, DevCL, DevCDV]: [DevBLC] and [DevCTG] Display A Trickle Feed Enable: 0 = Trickle Feed Enabled - Display A data requests are sent whenever there is space in the Display Data Buffer. 1 = Trickle Feed Disabled - Display A data requests are sent in bursts. Note: On mobile products this bit will be ignored such that Trickle Feed is always disabled. [DevELK] Must always be programmed disabled
13	0b RW	**RESERVED_4:** [DevBW, DevCL, DevCDV]: [DevBLC] and [DevCTG] Display A Data Buffer Partitioning Control: 0 = Display A Data Buffer will encompass Sprite A buffer space when Sprite A is disabled. 1 = Display A Data Buffer will not use Sprite A buffer space when Sprite A is disabled. Note: When in C3xR Max FIFO mode, this bit will be ignored.
12:11	0b RW	**RESERVED_5:** Reserved.

Bit Range	Default & Access	Description
10	0b RW	**TILED_SURFACE:** . This bit indicates that the display A surface data is in tiled memory. The tile pitch is specified in bytes in the DSPASTRIDE register. Only X tiling is supported for display surfaces.When this bit is set, it affects the hardware interpretation of the DSPATILEOFF, DSPALINOFF, and DSPASURF registers. 0 = Display A surface uses linear memory 1 = Display A surface uses X-tiled memory
9	0b RW	**RESERVED_6:** [DevBW, DevCL, DevCDV] Write as zero [DevBLC, DevCTG] Asynchronous Surface Address Update Enable: This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions: No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 = DSPASURF MMIO writes will update synchronous to start of vertical blank (default) 1 = DSPASURF MMIO writes will update asynchronously
8:1	0b RW	**RESERVED_7:** Write as zero
0	0b RW	**S3D_FORCE_DISPLAY_A_BOTTOM:** This bit will force the display A plane to be on the bottom of any sprite planes in the Z order. 0 = Display A Z-order is determined by the other control bits in pipe A 1 = Display A is forced to be on the bottom of any sprite planes in Z-order in pipe A

3.4.212 DSPALINOFF—Offset 70184h

Display A Linear Offset Register

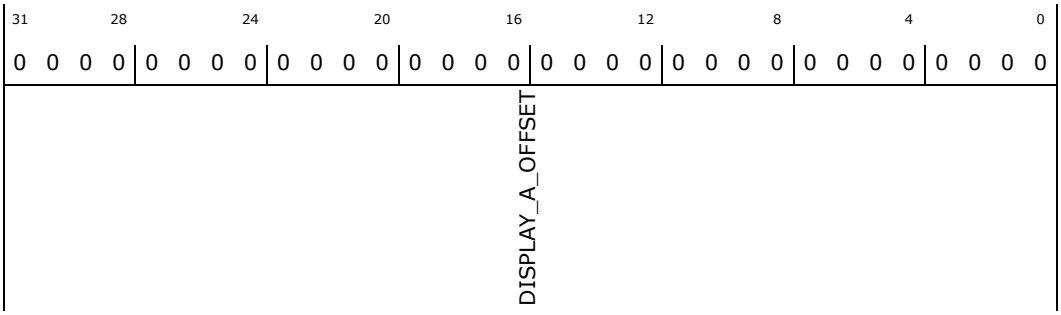
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPALINOFF: [GTTMMADR_LSB + 2BF20h] + 70184h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**DISPLAY_A_OFFSET:** This register provides the panning offset into the display A plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

3.4.213 DSPASTRIDE—Offset 70188h

Display A Stride Register

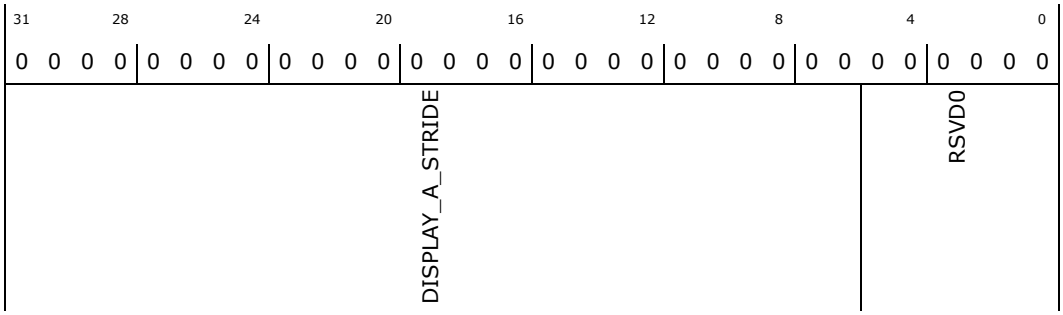
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPASTRIDE: [GTTMMADR_LSB + 2BF20h] + 70188h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**DISPLAY_A_STRIDE:** This is the stride for display A in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. This value is used to determine the line to line increment for the display. This register is updated either through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes. [DevBW, DevCL, DevCDV] The display stride must be power of 2 when doing Asynch Flips. [DevBW, DevCL, DevCDV] The display stride must be 8KB or greater when doing Asynch Flips together with 180 rotation. The value in this register is updated through the command streamer during a synchronous flip.
5:0	0b RO	**RSVD0:** Reserved

3.4.214 DSPAKEYVAL—Offset 70194h

Sprite Color Key Value Register

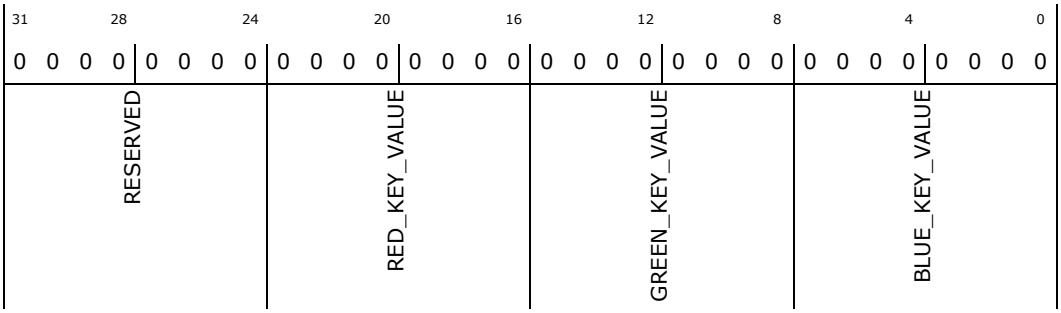
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPAKEYVAL: [GTTMMADR_LSB + 2BF20h] + 70194h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**RED_KEY_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

3.4.215 DSPAKEYMSK—Offset 70198h

Sprite Color Key Mask Register

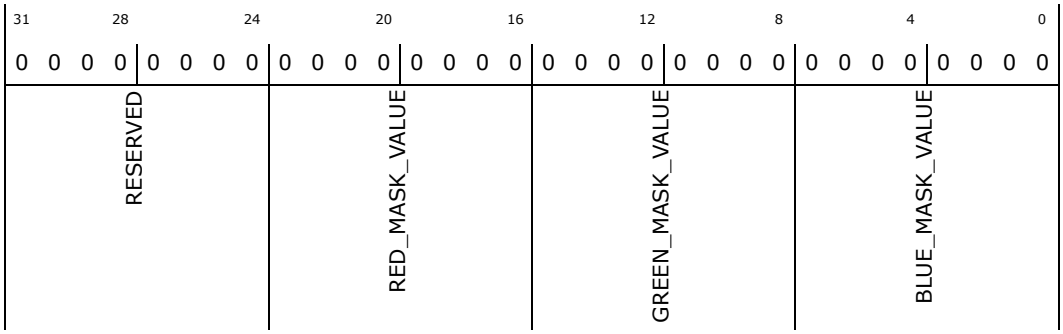
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPAKEYMSK: [GTTMMADR_LSB + 2BF20h] + 70198h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	0b RW	**RED_MASK_VALUE:** Specifies the color key mask for the sprite red/Cr channel.
15:8	0b RW	**GREEN_MASK_VALUE:** Specifies the color key mask for the sprite green/Y channel.
7:0	0b RW	**BLUE_MASK_VALUE:** Specifies the color key mask for the sprite blue/Cb channel.

3.4.216 DSPASURF—Offset 7019Ch

Display A Surface Base Address Register

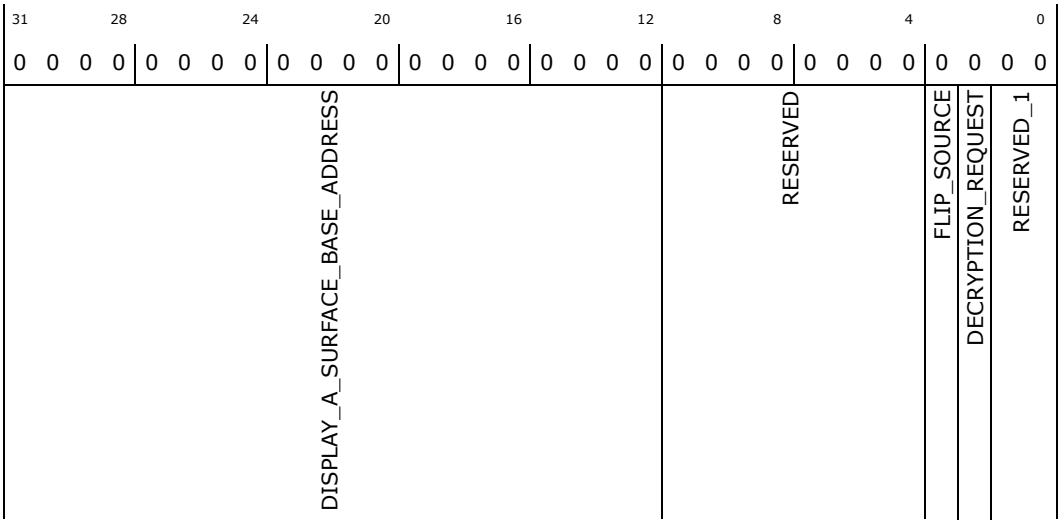
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPASURF: [GTTMMADR_LSB + 2BF20h] + 7019Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**DISPLAY_A_SURFACE_BASE_ADDRESS:** . This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPATILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPALINOFF register.This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED:** Reserved.
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0b RW	**RESERVED_1:** MBZ

3.4.217 DSPATILEOFF—Offset 701A4h

Display A Tiled Offset Register

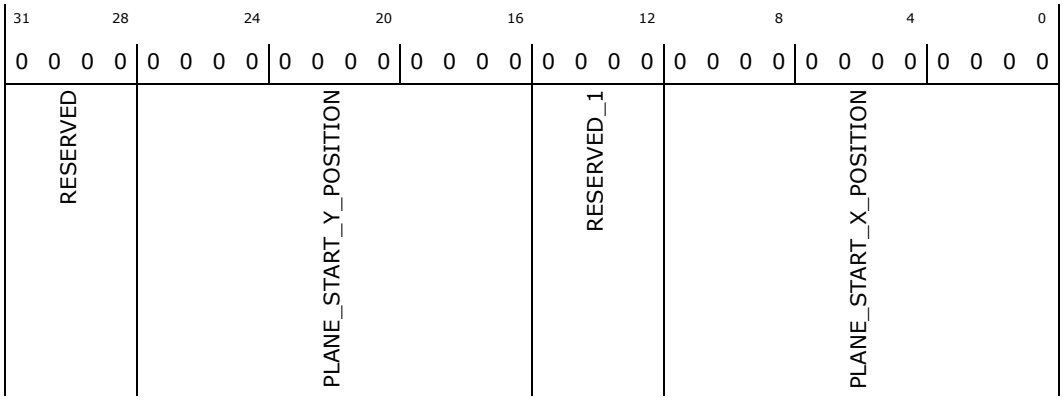
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPATILEOFF: [GTTMMADR_LSB + 2BF20h] + 701A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation. [DevBW, DevCL, DevCDV] When display stride is 16KB and doing Asynch Flips, do not program the offset to give pans of 7680 to 8191 bytes.

3.4.218 DSPASURFLIVE—Offset 701ACh

Display A Live Surface Base Address Register [DevCTG-B, DevCDV]

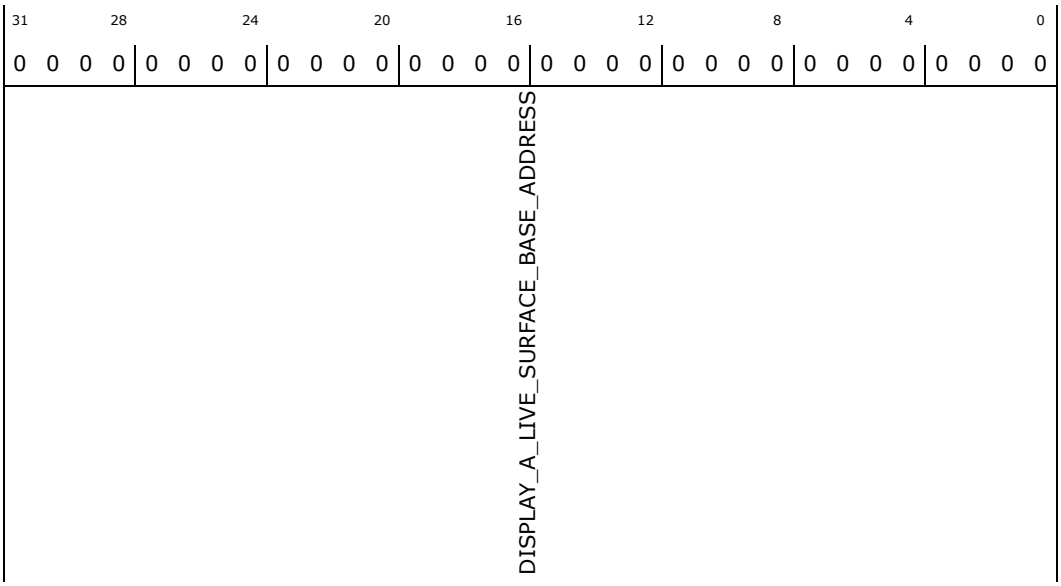
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPASURFLIVE: [GTTMMADR_LSB + 2BF20h] + 701ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**DISPLAY_A_LIVE_SURFACE_BASE_ADDRESS:** . This gives the live value of the surface base address as being currently used for the plane.

3.4.219 CBR1—Offset 70400h

Chicken Bit Register

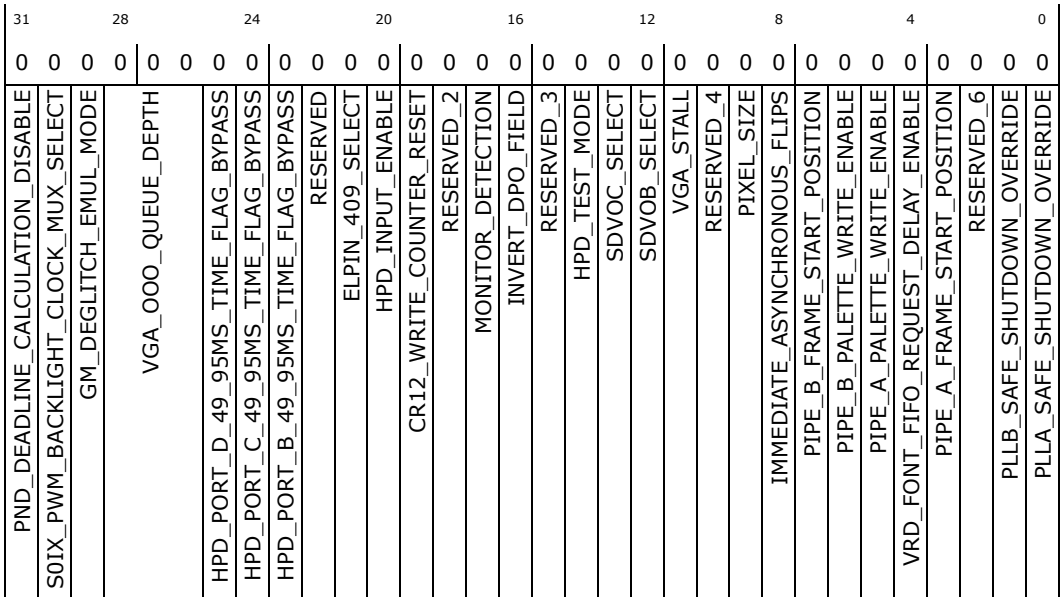
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

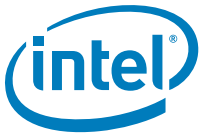
CBR1: [GTTMMADR_LSB + 2BF20h] + 70400h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**PND_DEADLINE_CALCULATION_DISABLE:** 1 = PND deadline scheme is disabled. Latency deadline calculation is based on the pre-programmed watermark level and the 2-bit FIFO status region. 0 = PND deadline scheme is enabled. Latency deadline calculation is based on actual FIFO level
30	0b RW	**S0IX_PWM_BACKLIGHT_CLOCK_MUX_SELECT:** This bit is used to select the new pwm backlight control during s0ix mode 0 = select s0ix pwm backlight control based on 25 MHz oscillator clock (default) 1 = select normal pwm backlight control based on hrawclk Programming note: This bit is programmed to select either 200MHz refclk from CCK or 25MHz refclk from XTAL. This bit cannot be changed on the fly.
29	0b RW	**GM_DEGLITCH_EMUL_MODE:** GM deglitch emulation mode
28:26	0b RW	**VGA_OOO_QUEUE_DEPTH:** 0xx = Disable out-of-order stall logic for VGA 100 = Enable out-of-order VGA stall depth of 64 101 = Enable out-of-order VGA stall depth of 48 110 = Enable out-of-order VGA stall depth of 32 111 = Enable out-of-order VGA stall depth of 16
25	0b RW	**HPD_PORT_D_49_95MS_TIME_FLAG_BYPASS:** bypass 49_95ms time flag in Port D Not Used
24	0b RW	**HPD_PORT_C_49_95MS_TIME_FLAG_BYPASS:** bypass 49_95ms time flag in Port C Programming note: VLV uses HPD deglitch time as 50us. For glitches between 50us and 250us during hot plug event, driver may see multiple hpd interrupts, driver shall either service them or ignore them.
23	0b RW	**HPD_PORT_B_49_95MS_TIME_FLAG_BYPASS:** bypass 49_95ms time flag in Port B Programming note: VLV uses HPD deglitch time as 50us. For glitches between 50us and 250us during hot plug event, driver may see multiple hpd interrupts, driver shall either service them or ignore them.
22	0b RW	**RESERVED:** Reserved.



Bit Range	Default & Access	Description
21	0b RW	**ELPIN_409_SELECT:** This bit is used to select one of the elpin 409 bug fixes 0 = vrd_ci_rreq 1 = count comparator
20	0b RW	**HPD_INPUT_PIN_DISABLE (HPD_INPUT_ENABLE):** [DevVLVP]: this bit is used to disable HPD detection in the Display core from using HPD input pin pin 0 = HPD Input pin is enabled to detect HPD detection by Display core (default) 1 = HPD input is pin is disabled to detect HPD detection by Display core
19	0b RW	**CR12_WRITE_COUNTER_RESET:** 0 = Disable CR12 write counter reset 1 = Enable CR12 write counter reset
18	0b RW	**RESERVED_2:** Reserved.
17	0b RW	**MONITOR_DETECTION:** This bit is used to test the monitor detection. Do not program unless directed.
16	0b RW	**INVERT_DPO_FIELD:** Invert DPO interlaced field output. This bit is used to invert the field sense input to the planes from DPO.
15	0b RW	**RESERVED_3:** Reserved.
14	0b RW	**HPD_TEST_MODE:** load programmable value for filter and long pulse value of HPD register 0x70408.
13	0b RW	**SDVOC_SELECT:** sdvoc deglitch logic output select
12	0b RW	**SDVOB_SELECT:** sdvob deglitch logic output select
11	0b RW	**VGA_STALL:** Stall native mode VGA when frequency is over 50 MHz. This bit is only used during VGA native mode.
10	0b RW	**RESERVED_4:** to prevent async flip failures.
9	0b RW	**PIXEL_SIZE:** This bit changes the VGA pixel width and height calculations.
8	0b RW	**IMMEDIATE_ASYNCHRONOUS_FLIPS:** This bit causes asynchronous flips to complete immediately upon the start of the vertical blank period. When enabling this feature, frame start should also be moved to the end of the vertical blank period by setting the frame start position bit.
7	0b RW	**PIPE_B_FRAME_START_POSITION:** This bit changes the position of frame start on pipe B. This feature is used in conjunction with the immediate asynchronous flips bit to enable fast asynchronous flips during vertical blanking. 0 = frame start occurs at start of the vertical blank period 1 = frame start occurs at end of the vertical blank period Default: 1, causing frame start to occur at the end of vertical blank
6	0b RW	**PIPE_B_PALETTE_WRITE_ENABLE:** Disables anti-collision logic in the palette during non-blanking periods on pipe B.
5	0b RW	**PIPE_A_PALETTE_WRITE_ENABLE:** Disables anti-collision logic in the palette during non-blanking periods on pipe A
4	0b RW	**VRD_FONT_FIFO_REQUEST_DELAY_ENABLE:** This bit enable VRD font read request delay in VGA mode

Bit Range	Default & Access	Description
3	0b RW	**PIPE_A_FRAME_START_POSITION:** This bit changes the position of frame start on pipe A. This feature is used in conjunction with the immediate asynchronous flips bit to enable fast asynchronous flips during vertical blanking. 0 = frame start occurs at start of the vertical blank period 1 = frame start occurs at end of the vertical blank period Default: 1, causing frame start to occur at the end of vertical blank
2	0b RW	**RESERVED_6:** Reserved.
1	0b RW	**PLLB_SAFE_SHUTDOWN_OVERRIDE:** This bit disables the dependency for pipe B to be disabled before the PLL is shut down
0	0b RW	**PLLA_SAFE_SHUTDOWN_OVERRIDE:** This bit disables the dependency for pipe A to be disabled before the PLL is shut down

3.4.220 CBR2—Offset 70404h

Chicken2 Bit Register

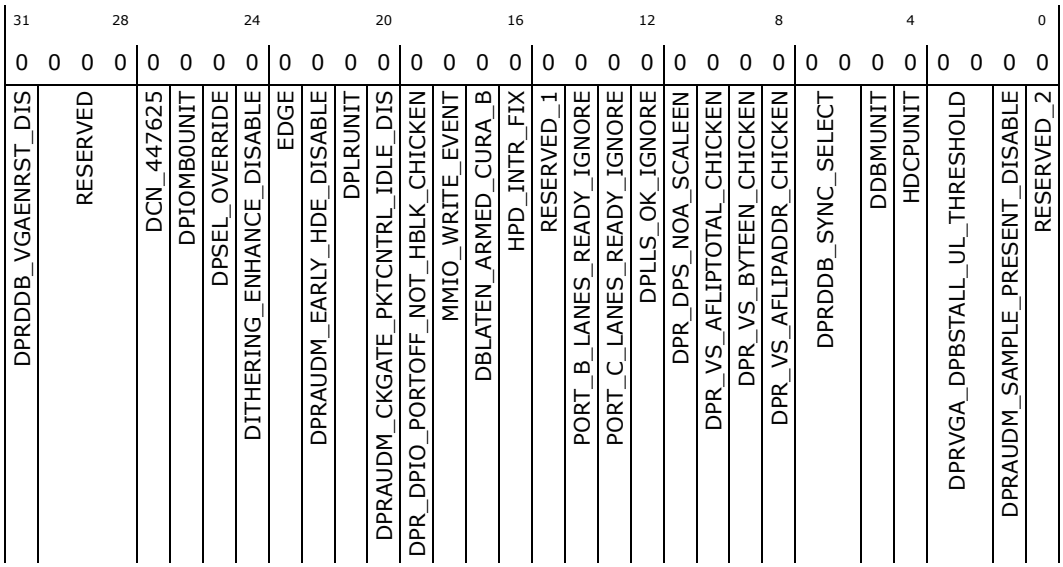
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CBR2: [GTTMMADR_LSB + 2BF20h] + 70404h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**DPRDDB_VGAENRST_DIS:** Enable rise and fall detection of DPRvgadis for DDB reset (dprddb_vgaenrst_dis)

Bit Range	Default & Access	Description
30:28	0b RW	**RESERVED:** Reserved.
27	0b RW	**DCN_447625:** : - x8 support for hybrid gfx, Kwasi requested (dpr_dpio_x8_conc_sel)
26	0b RW	**DPIOMB0UNIT:** ignoring EDP logic when enabling Lanes by the dptc_otxoenb [DevVLVP]: Reserved
25	0b RW	**DPSEL_OVERRIDE:** when this chicken bit is set override the selects to 0 (dpsel_override) timeslice_sync_rst_b = DPRVGAdis | mrchicken2_Q[25]
24	0b RW	**DITHERING_ENHANCE_DISABLE:** Anh need for dithering enhance (dithering_enhance_disable)
23	0b RW	**EDGE:** edgeA/Bvblank, edgeDPSA/Bvblank, curA/Bedgevblank,
22	0b RW	**DPRAUDM_EARLY_HDE_DISABLE:** Chicken bit to Audio unit to disable early RAM FIFO read in 2-channel mode (DPRAUDM_early_hde_disable)
21	0b RW	**DPLRUNIT:** Selects cdclk for pwm logic, pwm logic, uses hrawclk by default (select cdclk in scan mode or by setting a chicken bit) [DevVLVP]: Reserved
20	0b RW	**DPRAUDM_CKGATE_PKTCNTRL_IDLE_DIS:** Chicken bit to disable audclk gating when pktcontrol FSM is idle (DPRAUDM_ckgate_pktcntrl_idle_dis)
19	0b RW	**DPR_DPIO_PORTOFF_NOT_HBLK_CHICKEN:** This bit is needed to qualify the port off with hblank to take care of fragmented audio packet sent off. When chicken bit is enabled, the port off is dependent upon state of hblank, else the legacy behavior rules (dpr_dpio_portoff_not_hblk_chicken)
18	0b RW	**MMIO_WRITE_EVENT:** 0: mmio_write_event = RMDecPipeSLC_pre 1: mmio_write_event = 1'b0
17	0b RW	**DBLATEN_ARMED_CURA_B:** Dblaten_armed_curA/B
16	0b RW	**HPD_INTR_FIX:** Freezes hpdb_intr_fix, hpdc_intr_fix, hpdd_intr_fix
15	0b RW	**RESERVED_1:** Reserved.
14	0b RW	**PORT_B_LANES_READY_IGNORE:** 1: Lanes considered as ready for normal operation 0: usual operation: Lanes readiness indications arrived from DPIO SEG outputs [DevVLVP]: Reserved
13	0b RW	**PORT_C_LANES_READY_IGNORE:** 1: Lanes considered as ready for normal operation 0: usual operation: Lanes readiness indications arrived from DPIO SEG outputs [DevVLVP]: Reserved
12	0b RW	**DPLLS_OK_IGNORE:** 1: Both mPHY DPLLs considered as OK ('1'). Lanes can be enabled. 0: usual operation: DPLL readiness indications arrived from DPIO SEG outputs [DevVLVP]: Reserved
11	0b RW	**DPR_DPS_NOA_SCALEEN:** This bit is to enable viewing critical control signals that were added as a result of Cantiga B0 Overlay changes. Default = 0. (dpr_dps_noa_scaleen) 0: Non-scaling signals are sent to NOA bus 1: Scaling signals are sent to the NOA bus

Bit Range	Default & Access	Description
10	0b RW	**DPR_VS_AFLIPTOTAL_CHICKEN:** This chicken bit bypasses the current logic used for calculating the number of requests to make for an asynchronous flip. It will be helpful because the current logic is very difficult to validate. (dpr_vs_afliptotal_chicken)
9	0b RW	**DPR_VS_BYTEEN_CHICKEN:** This chicken bit bypasses the current logic used for selecting the proper byte enables. It is intended to address byte enables during asynchronous flips, but it was easier to bypass the entire byte-enable circuit instead. HSD bug #1932963. (dpr_vs_byteen_chicken)
8	0b RW	**DPR_VS_AFLIPADDR_CHICKEN:** This chicken bit bypasses the current logic used for selecting the starting fetch address of an asynchronous flip. HSD bug #1932964. (dpr_vs_aflipaddr_chicken)
7:6	0b RW	**DPRDDB_SYNC_SELECT:** When set vsync reset is asserted and when clear no reset is asserted. (dprddb_novsyncreset) This selects between VRVSYNC and hi-res VSYCN when set with dprvrd_novsyncreset also set sync_select novsyncreset. (dprddb_sync_select) X0 = No Vsync reset 01 = VGA vsync or hi-res between Nat and UL mode 11 = VGA vsync reset in both UL and native
5	0b RW	**DDBMUNIT:** C0 ECO1 chicken bit defaulted to fix enable
4	0b RW	**HDCPUNIT:** EGLK A5 ECO1 Fix. Read Data Fix For RMBus Protocol. vsmunit: Lock Up Issue.
3:2	0b RW	**DPRVGA_DPBSTALL_UL_THRESHOLD:** VGATEST2 issue fix, Stall throttling done during horiz_blank and UL mode is asserted. (DPRVGA_dpbstall_ul_threshold). 01: DPB to VGA stall during UL mode
1	0b RW	**DPRAUDM_SAMPLE_PRESENT_DISABLE:** When set this bit will disable the sample present bits being set in layout 1 mode of Audio. Default is to enable sample present on Audio. (DPRAUDM_sample_present_disable) vsmunit: FBC/SR Power Fix
0	0b RW	**RESERVED_2:** [DevVLVP] MBZ. This bit si the same as bit 31 in 70450h rega_loadcount_crtdetect

3.4.221 CCBR—Offset 70408h

ChickenCount Bit Register

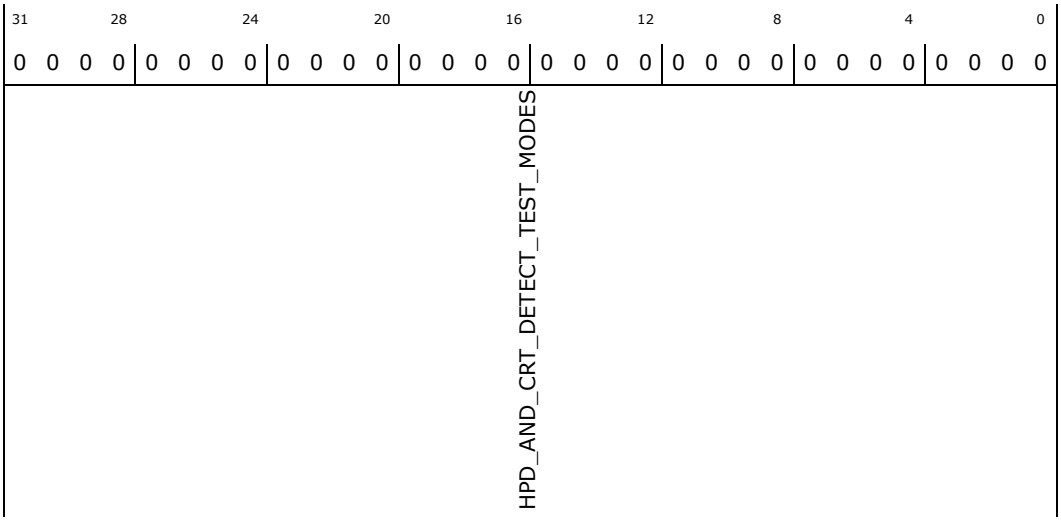
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CCBR: [GTTMMADR_LSB + 2BF20h] + 70408h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**HPD_AND_CRT_DETECT_TEST_MODES:** HPD and CRT detect test mode

3.4.222 CBR3—Offset 7040Ch

Chicken3 Bit Register

Access Method

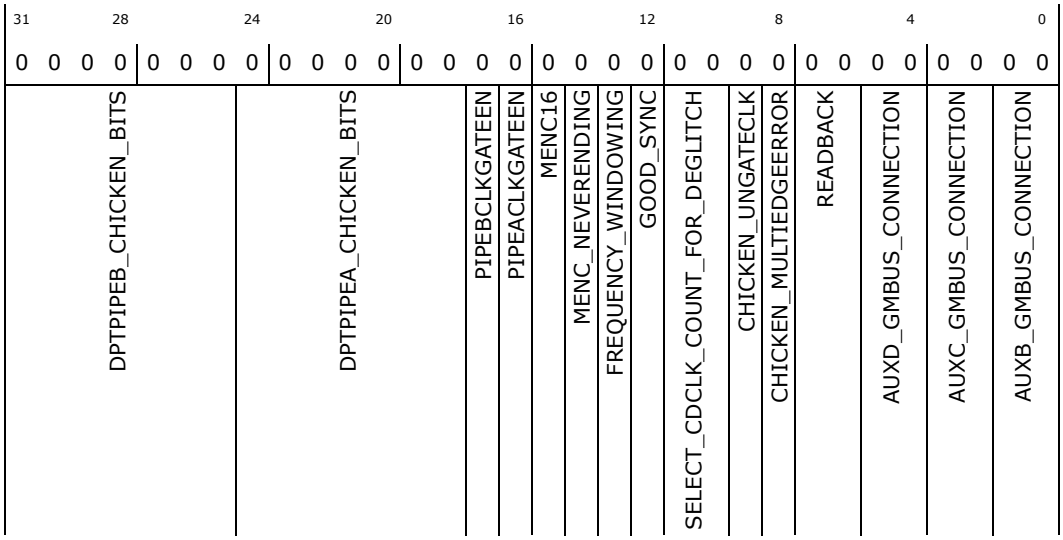
Type: Memory Mapped I/O Register (Size: 32 bits)

CBR3: [GTTMMADR_LSB + 2BF20h] + 7040Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RW	**DPTPIPEB_CHICKEN_BITS:** not used [DevVLVP]: Reserved
24:18	0b RW	**DPTPIPEA_CHICKEN_BITS:** not used [DevVLVP]: Reserved
17	0b RW	**PIPEBCLKGATEEN:** Enables reg_pipeBclkgateen_cd reg_pipeBclkgateen_db [DevVLVP]: Reserved
16	0b RW	**PIPEACLKGATEEN:** Enables reg_pipeAclkgateen_cd reg_pipeAclkgateen_da [DevVLVP]: Reserved
15	0b RW	**MENC16:** Chicken to cause MENC to output just 16 manchester 0s for sync (otherwise 26) [DevVLVP]: Reserved
14	0b RW	**MENC_NEVERENDING:** Chicken to cause MENC to output never ending sync 0s for electrical testing [DevVLVP]: Reserved
13	0b RW	**FREQUENCY_WINDOWING:** Chicken to tighten the frequency windowing [DevVLVP]: Reserved
12	0b RW	**GOOD_SYNC:** Chicken to check for only 8 good sync 0s instead of 12 [DevVLVP]: Reserved
11:10	0b RW	**SELECT_CDCLK_COUNT_FOR_DEGLITCH:** 11 = 1/16 2X bit clock divider value - 31.125ns 10 = 1/8 2X bit clock divider value - 62.5ns 01 = 1/4 2X bit clock divider value - 125ns 00 = 25 - GMBUS type 50ns at 500MHz cdclk [DevVLVP]: Reserved
9	0b RW	**CHICKEN_UNGATECLK:** 1 = Ungate clock 0 = Automatic clock gating [DevVLVP]: Reserved
8	0b RW	**CHICKEN_MULTIEDGEERROR:** 1 = Multiple edges in window is an error 0 = Multiple edges in window is okay [DevVLVP]: Reserved
7:6	0b RW	**READBACK:** 11 = Readback of bit clock divide field gives the error type 01 = Readback gives the recovered clock frequency 00 = Readback gives the programmed clock frequency [DevVLVP]: Reserved

Bit Range	Default & Access	Description
5:4	0b RW	**AUXD_GMBUS_CONNECTION:** Selects gmbus connection for AUXD [DevVLVP]: Reserved
3:2	0b RW	**AUXC_GMBUS_CONNECTION:** Selects gmbus connection for AUXC [DevVLVP]: Reserved
1:0	0b RW	**AUXB_GMBUS_CONNECTION:** Selects gmbus connection for AUXB [DevVLVP]: Reserved

3.4.223 SWF00—Offset 70410h

Software Flag Registers

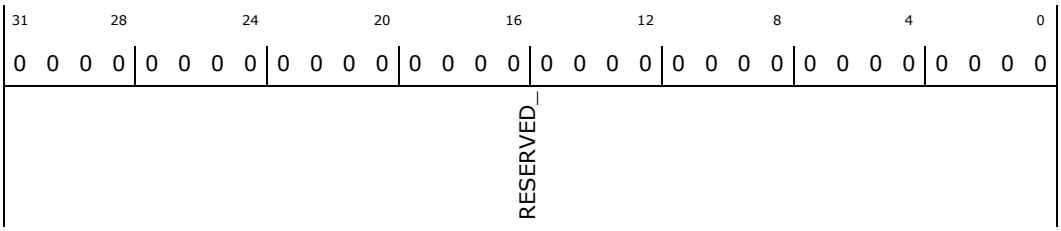
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF00: [GTTMMADR_LSB + 2BF20h] + 70410h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.224 SWF01—Offset 70414h

Software Flag Registers

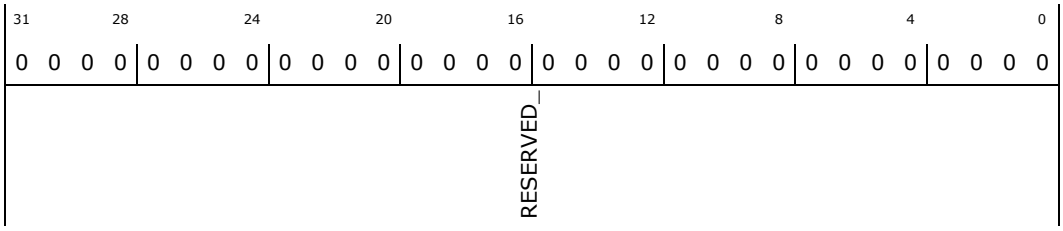
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF01: [GTTMMADR_LSB + 2BF20h] + 70414h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.225 SWF02—Offset 70418h

Software Flag Registers

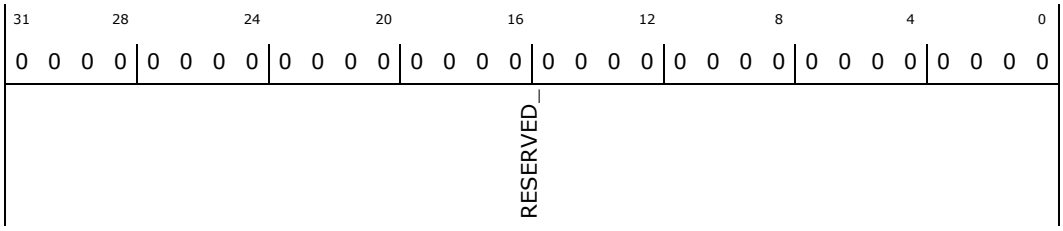
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF02: [GTTMMADR_LSB + 2BF20h] + 70418h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.226 SWF03—Offset 7041Ch

Software Flag Registers

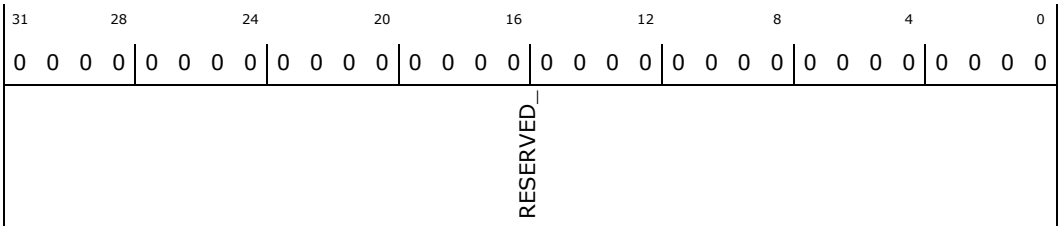
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF03: [GTTMMADR_LSB + 2BF20h] + 7041Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.227 SWF04—Offset 70420h

Software Flag Registers

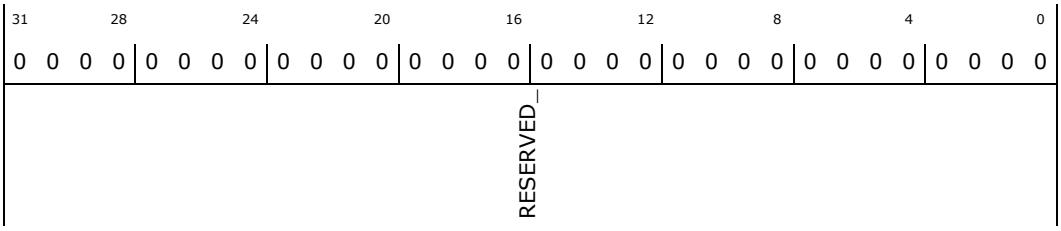
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF04: [GTTMMADR_LSB + 2BF20h] + 70420h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.228 SWF05—Offset 70424h

Software Flag Registers

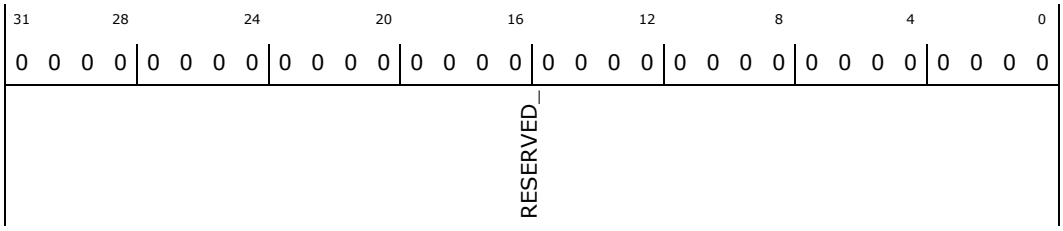
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF05: [GTTMMADR_LSB + 2BF20h] + 70424h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.229 SWF06—Offset 70428h

Software Flag Registers

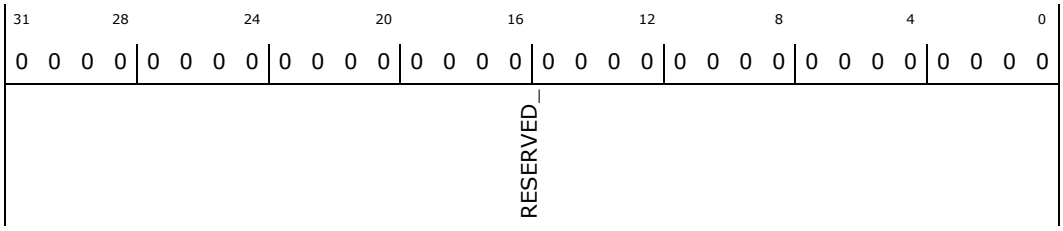
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF06: [GTTMMADR_LSB + 2BF20h] + 70428h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.230 SWF07—Offset 7042Ch

Software Flag Registers

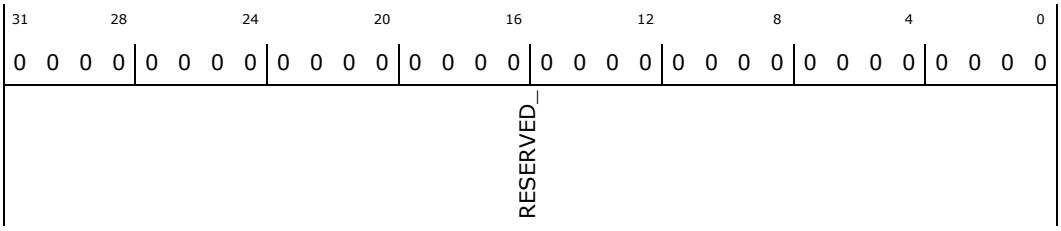
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF07: [GTTMMADR_LSB + 2BF20h] + 7042Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.231 SWF08—Offset 70430h

Software Flag Registers

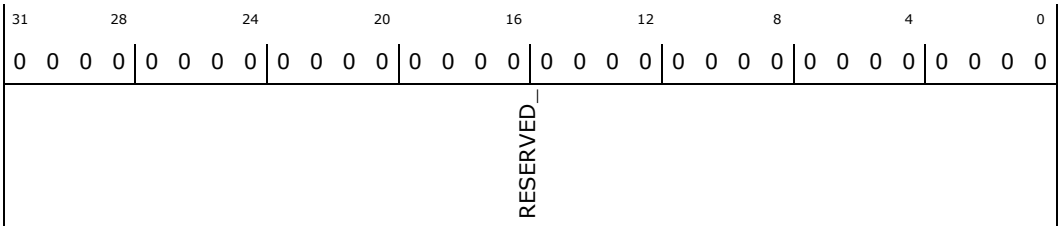
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF08: [GTTMMADR_LSB + 2BF20h] + 70430h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.232 SWF09—Offset 70434h

Software Flag Registers

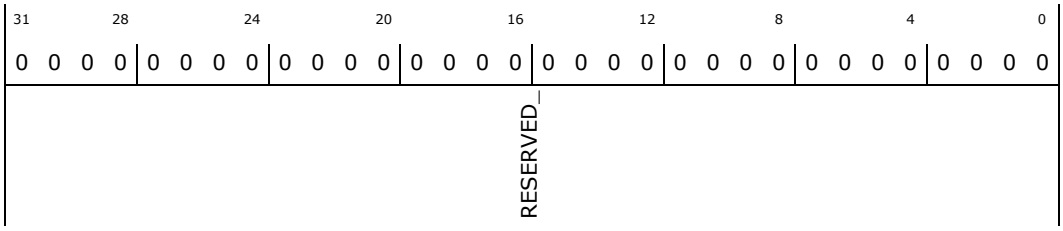
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF09: [GTTMMADR_LSB + 2BF20h] + 70434h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.233 SWF0A—Offset 70438h

Software Flag Registers

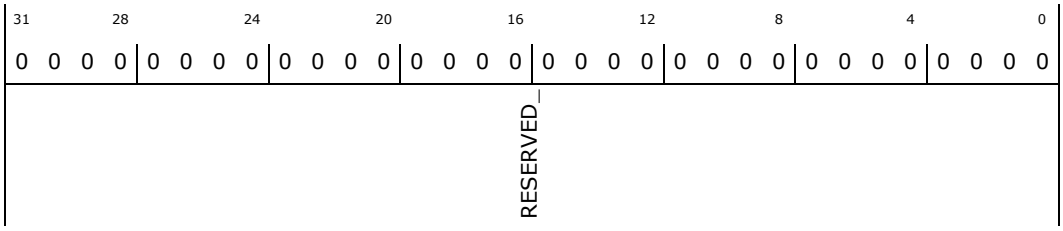
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF0A: [GTTMMADR_LSB + 2BF20h] + 70438h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.234 SWF0B—Offset 7043Ch

Software Flag Registers

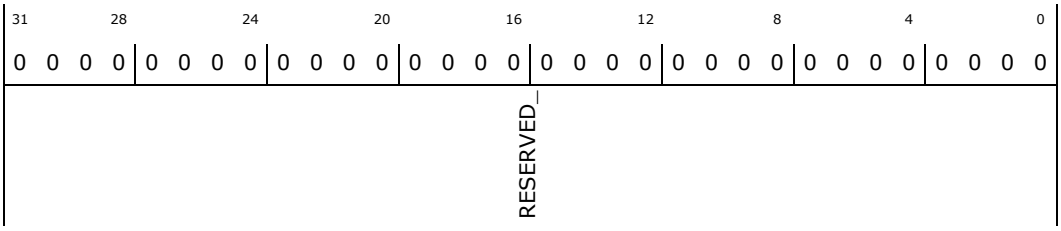
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF0B: [GTTMMADR_LSB + 2BF20h] + 7043Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.235 SWF0C—Offset 70440h

Software Flag Registers

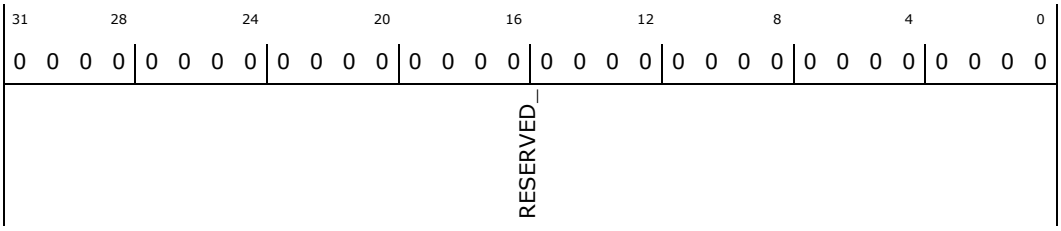
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF0C: [GTTMMADR_LSB + 2BF20h] + 70440h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.236 SWF0D—Offset 70444h

Software Flag Registers

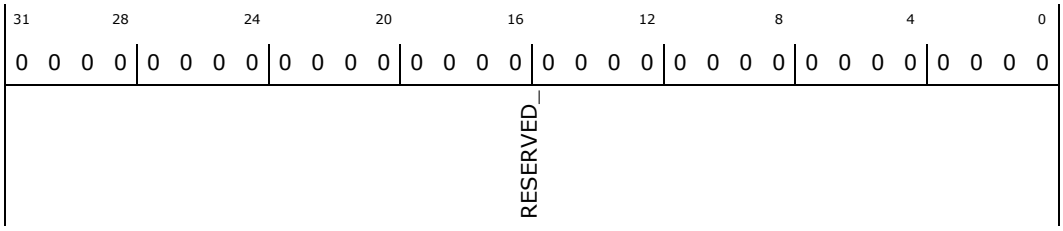
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF0D: [GTTMMADR_LSB + 2BF20h] + 70444h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.237 SWF0E—Offset 70448h

Software Flag Registers

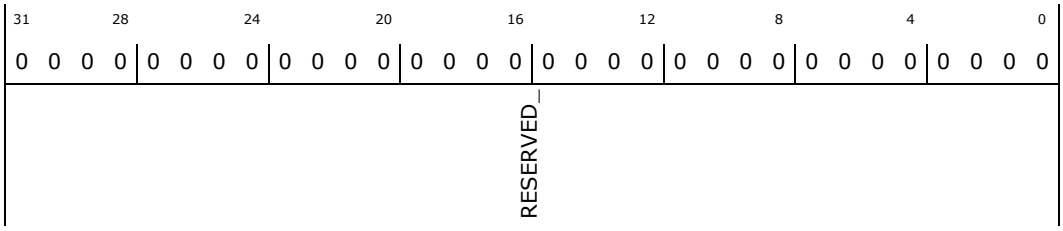
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF0E: [GTTMMADR_LSB + 2BF20h] + 70448h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.238 SWF0F—Offset 7044Ch

Software Flag Registers

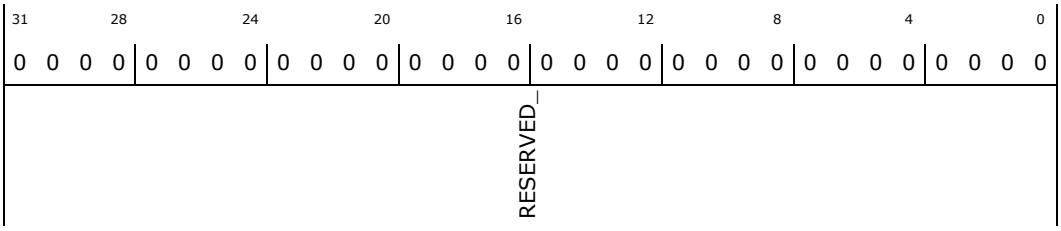
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF0F: [GTTMMADR_LSB + 2BF20h] + 7044Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.239 CBR4—Offset 70450h

Display Chicken Bits 4 ;

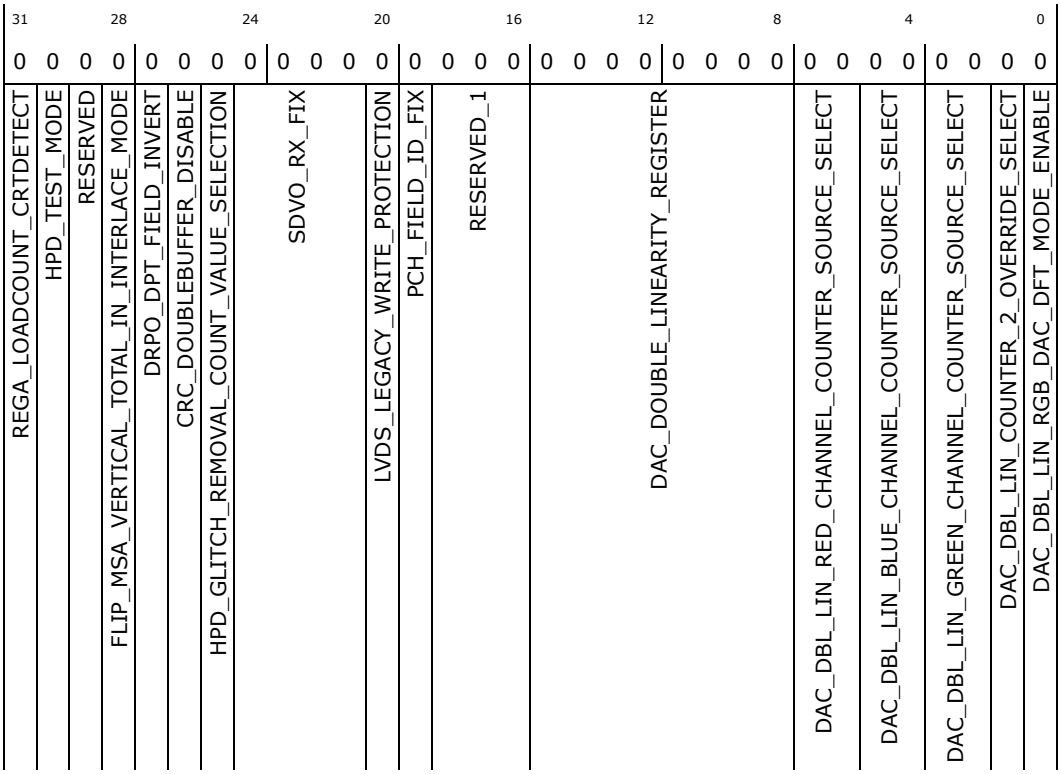
Access Method

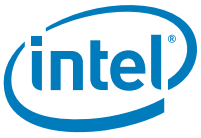
Type: Memory Mapped I/O Register (Size: 32 bits)

CBR4: [GTTMMADR_LSB + 2BF20h] + 70450h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31	0b RW	**REGA_LOADCOUNT_CRTDETECT:** Project: All Format: Load initial value to crtdetect counter
30	0b RW	**HPD_TEST_MODE:** Project: All Default Value: 0b Load programmable value for filter and long pulse value of HPD Value Name Description Project 0b Short Pulse Short Pulse All 1b Long Pulse Long Pulse All
29	0b RW	**RESERVED:** Project: All Format: PBC
28	0b RW	**FLIP_MSA_VERTICAL_TOTAL_IN_INTERLACE_MODE:** Project: All Format: Set to 1 to flip MSA vtotal
27	0b RW	**DRPO_DPT_FIELD_INVERT:** Project: All Format: Invert interlaced field ID output from dptunit.
26	0b RW	**CRC_DOUBLEBUFFER_DISABLE:** Project: All Format: Disable doublebuffering on CRCs so enable/disable and source select will happen immediately.
25	0b RW	**HPD_GLITCH_REMOVAL_COUNT_VALUE_SELECTION:** Project: All Default Value: 0b Value Name Description Project 0b 500us 500us glitch removal All 1b 50us 50us glitch removal All
24:21	0b RW	**SDVO_RX_FIX:** Project: All Format: Program SDVO receiver fix values [DevVLVP]: Reserved
20	0b RW	**LVDS_LEGACY_WRITE_PROTECTION:** Project: All Format: [DevVLVP]: Reserved
19	0b RW	**PCH_FIELD_ID_FIX:** Project: All Format: 1: CPU and PCH field IDs are independent 0: CPU field ID is tied to PCH field ID [DevVLVP]: Reserved
18:16	0b RW	**RESERVED_1:** Project: All Format: MBZ
15:8	0b RW	**DAC_DOUBLE_LINEARITY_REGISTER:** Project: All Format: Project: DevIBX-B Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of counter 1 All 11b Counter 2 Counter 2 All
7:6	0b RW	**DAC_DBL_LIN_RED_CHANNEL_COUNTER_SOURCE_SELECT:** Project: DevIBX-B Default Value: 00b DefaultVaueDesc BitFieldDesc Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of Counter 1 All 11b Counter 2 Counter 2 All Programming Notes Notes Errata Description Project # Desc All
5:4	0b RW	**DAC_DBL_LIN_BLUE_CHANNEL_COUNTER_SOURCE_SELECT:** Project: DevIBX-B Default Value: 00b Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of counter 1 All 11b Counter 2 Counter 2 All
3:2	0b RW	**DAC_DBL_LIN_GREEN_CHANNEL_COUNTER_SOURCE_SELECT:** Project: DevIBX-B Default Value: 00b Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of counter 1 All 11b Counter 2 Counter 2 All

Bit Range	Default & Access	Description
1	0b RW	**DAC_DBL_LIN_COUNTER_2_OVERRIDE_SELECT:** Project: DevIBX-B Default Value: 0b Value Name Description Project 0b No override No override, count value is from counter 2 All 1b Override Override mode enabled, count value is from 8-bit override value All
0	0b RW	**DAC_DBL_LIN_RGB_DAC_DFT_MODE_ENABLE:** Project: DevIBX-B Default Value: 0b Value Name Description Project 0b Disable Normal operation, no test mode enabled All 1b Enable RGB DAC DFT mode enabled All

3.4.240 PIPEB_DSL—Offset 71000h

Display Scan Line

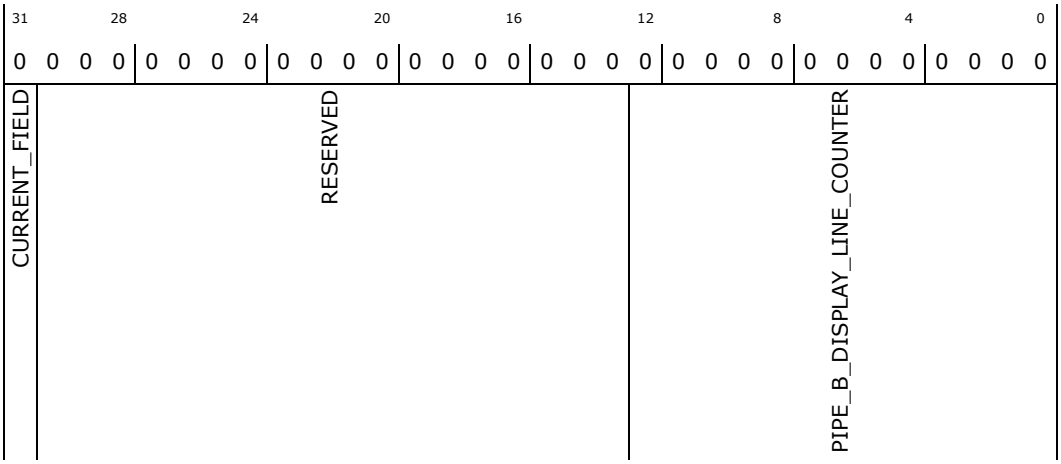
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_DSL: [GTTMMADR_LSB + 2BF20h] + 71000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**CURRENT_FIELD:** [DevBLC, DevCTG, DevCDV] Provides read back of the current field being displayed on display pipe B. Non-TV mode: 0 = first field (odd field) 1 = second field (even field) TV mode: 1 = first field (odd field) 0 = second field (even field) [DevBW and DevCL] Reserved: Read only.
30:13	0b RO	**RESERVED:** Read only.

Bit Range	Default & Access	Description
12:0	0b RO	**PIPE_B_DISPLAY_LINE_COUNTER:** This register enables the read back of the display vertical line counter . The display line values are from the pipe B timing generator. They change at the leading edge of HSYNC, and can be safely read at any time.

3.4.241 PIPEB_SLC—Offset 71004h

Pipe B Display Scan Line Range Compare Register

Access Method

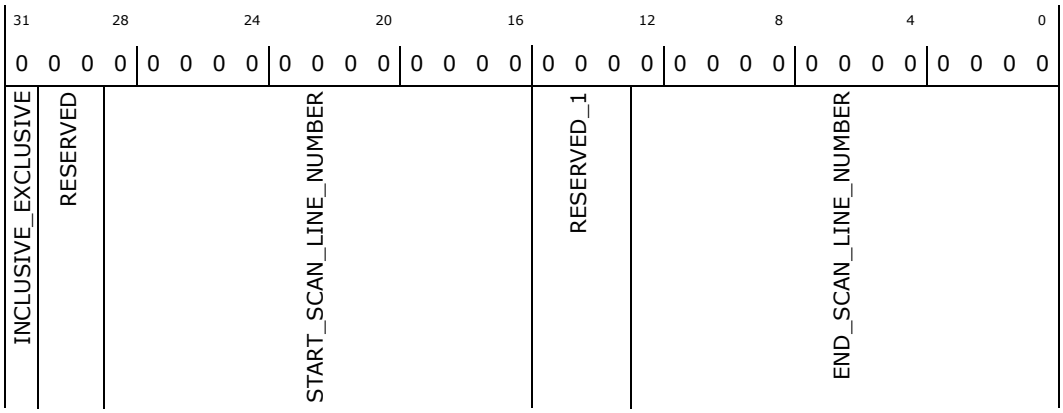
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEB_SLC: [GTTMMADR_LSB + 2BF20h] + 71004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**INCLUSIVE_EXCLUSIVE:** 1 = Inclusive Within Range, 0 = Exclusive Out of Range
30:29	0b RW	**RESERVED:** Read only.
28:16	0b RW	**START_SCAN_LINE_NUMBER:** [DevBLC, DevCTG, DevCDV] This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1]. [DevBW] and [DevCL] End Scan Line Number: This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1].
15:13	0b RW	**RESERVED_1:** Read only.

Bit Range	Default & Access	Description
12:0	0b RW	**END_SCAN_LINE_NUMBER:** [DevBLC, DevCTG, DevCDV] This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1]. [DevBW] and [DevCL] Start Scan Line Number: This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1].

3.4.242 PIPEBCONF—Offset 71008h

Pipe B Configuration Register

Access Method

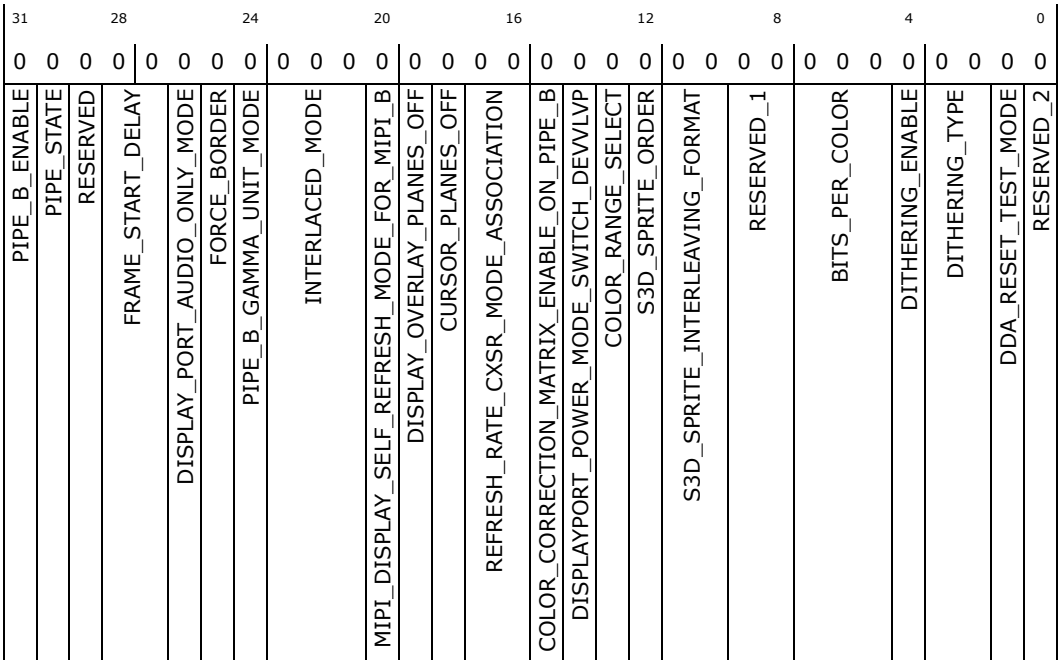
Type: Memory Mapped I/O Register (Size: 32 bits)

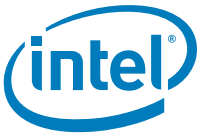
PIPEBCONF: [GTTMMADR_LSB + 2BF20h] + 71008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

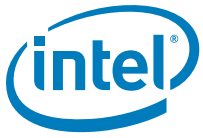
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31	0b RW	**PIPE_B_ENABLE:** Setting this bit to the value of one, turns on pipe B. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at its lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should contain valid values before this bit is enabled. Disabling the Pipe and changing the timing registers and re-enabling the pipe before the next VBLANK will cause the mode change to occur at the end of the current frame. This requires no wait on the software s part. On the other hand, if this is the disabling of the pipe, that does require a software wait for VBLANK to occur. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption is at it s lowest state. 1 = Enable 0 = Disable
30	0b RO	**PIPE_STATE:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off, this bit indicates the true current state of the pipe. 0 = Disabled 1 = Enabled AccessType: Read Only
29	0b RW	**RESERVED:** Write as zero.
28:27	0b RW	**FRAME_START_DELAY:** Used to delay the frame start signal that is sent to the display planes. Normal operation uses the default 00 value and test modes can use the delayed frame start to shorten the test time. This would be set to 00 for normal operation. 00 = Frame Start occurs on the first HBLANK after the start of VBLANK 01 = Frame Start occurs on the second HBLANK after the start of VBLANK 10 = Frame Start occurs on the third HBLANK after the start of VBLANK 11 = Frame Start occurs on the forth HBLANK after the start of VBLANK
26	0b RW	**DISPLAY_PORT_AUDIO_ONLY_MODE:** [DevVLVP] Setting this bit to 1 indicates the DisplayPort will output audio only. 0 = DisplayPort will output Video or Video and Audio 1 = DisplayPort will output Audio only
25	0b RW	**FORCE_BORDER:** : (TEST MODE)0 = Normal Operation 1 = Color information is ignored and border color is substituted during active region
24	0b RW	**PIPE_B_GAMMA_UNIT_MODE:** . This bit selects which mode the pipe gamma correction logic works in. In the palette mode, it behaves as a 3X256x8 RAM lookup. VGA and indexed mode operation should use the palette in 8-bit mode. In the 10-bit gamma mode, it will act as a piecewise linear interpolation. Other gamma units such as in the overlay and sprite are unaffected by this bit.0 = 8-bit Palette Mode 1 = 10-bit Gamma Mode



Bit Range	Default & Access	Description
23:21	0b RW	**INTERLACED_MODE:** These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled. 0xx = Progressive 100 = Interlaced embedded panel using programmable vertical sync shift (2x) 101 = Interlaced using vertical sync shift. Backup option to setting 110. (2x) 110 = Interlaced with VSYNC/HSYNC Field Indication using legacy vertical sync shift. Used for SDVO. 111 = Interlaced with Field 0 Only using legacy vertical sync shift. Not used. Note: VGA display modes, sDVO line stall, and Panel fitting do not work while in interlaced modes Setting the Interlaced embedded panel mode causes hardware to automatically modify the output to match the specifications of panels that support interlaced mode.
20	0b RW	**MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_B:** .0 = Normal Operation, display controller generate timing and refresh display panel at refresh rate 1 = Display self-refresh mode. Display controller update frame buffer in display module on demand only
19	0b RW	**DISPLAY_OVERLAY_PLANES_OFF:** . This bit when set will cause all enabled Display and overlay planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the display and overlay planes to resume on the following VBLANK.0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
18	0b RW	**CURSOR_PLANES_OFF:** . This bit when set will cause all enabled cursor planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the cursor planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
17:16	0b RW	**REFRESH_RATE_CXSR_MODE_ASSOCIATION:** These bits select how refresh rates are tied to CxSR on pipe B. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 0xx. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated dispay panels that support corresponding mode. 00 Default no dynamic refresh rate change enabled. Software control only. 01 Progressive-to-progressive refresh rate change enabled and tied to CxSR. Pixel clock values set in FPB0/FPB1 settings in the DPLLB control register and FPB0/FPB1 divider registers. 10 Progressive-to-interlaced refresh rate change enabled and tied to CxSR. Pixel clock value does not change in this case. Scaling must be disabled in this mode. Uses programmable VS shift 11 Reserved
15	0b RW	**COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_B:** 1 = Color Correction Coefficients are enabled to perform color correction 0 = Color Correction Coefficients are disabled
14	0b RW	**DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP:** This bit selects the software controlled progressive to progressive power saving mode (software controlled DRRS). Hardware Controlled Refresh Rate Select must be disabled when enabling this. Link and data M/N 1 values are used for normal settings, M/N 2 values are used for low power settings. 0 Normal progressive refresh rate (default) 1 Low Power progressive refresh rate

Bit Range	Default & Access	Description
13	0b RW	**COLOR_RANGE_SELECT:** [DevVLVP]: This bit is used to select the color range of RBG outputs. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output
12	0b RW	**S3D_SPRITE_ORDER:** This bit controls the blending order of the sprite planes for S3D support: 0 = Sprite C first. The first line or pixel comes from Sprite C (default) 1 = Sprite D first. The first line or pixel comes from Sprite D
11:10	0b RW	**S3D_SPRITE_INTERLEAVING_FORMAT:** These bits control the Sprite C/D interleaving format in S3D mode 00 = No interleaving 01 = Line interleaving 10 = Pixel interleaving 11 = Reserved
9:8	0b RW	**RESERVED_1:** [DevCDV, DevVLVP] MBZ Scrambling enable [DevCTG]: This bit enables scrambling for DisplayPort. Software must set this bit appropriately when enabling a DisplayPort output. 00 = Scrambling disabled (Default) 01 = Scrambling enabled, no SR after initialization at loop 2 of training 10 - RESERVED 11 = Scrambling and SR enabled. Scrambling is reset every 512 BS symbols.
7:5	0b RW	**BITS_PER_COLOR:** [DevCTG, DevCDV, DevVLVP]: This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. For further details on Display Port fixed frequency programming to accommodate these formats refer to DP Frequency Programming in DPLL section of Bspec. 000 = 8 bits per color (Default) 001 = 10 bits per color 010 = 6 bits per color 011 = RESERVED 1xx = RESERVED
4	0b RW	**DITHERING_ENABLE:** [DevCTG, DevCDV]: This bit enables dithering for DisplayPort 6bpc or 8bpc modes 0 Dithering disabled (Default) 1 Dithering enabled Programming Note: Dithering should only be enabled for 8bpc or 6bpc.
3:2	0b RW	**DITHERING_TYPE:** [DevCTG, DevCDV]: This bit selects dithering type for DisplayPort 6bpc or 8bpc modes 00 - Spatial only (default) 01- Spatio-Temporal 1 10- Spatio-Temporal 2 (testmode) 11- Temporal only (testmode)
1	0b RW	**DDA_RESET_TEST_MODE:** [DevCTG, DevCDV]: 0 Do not reset DDA 1 Reset DDA every 8th display frame
0	0b RW	**RESERVED_2:** Write as zero

3.4.243 PIPEBGCMAXRED—Offset 71010h

Pipe B Gamma Correction Max Red

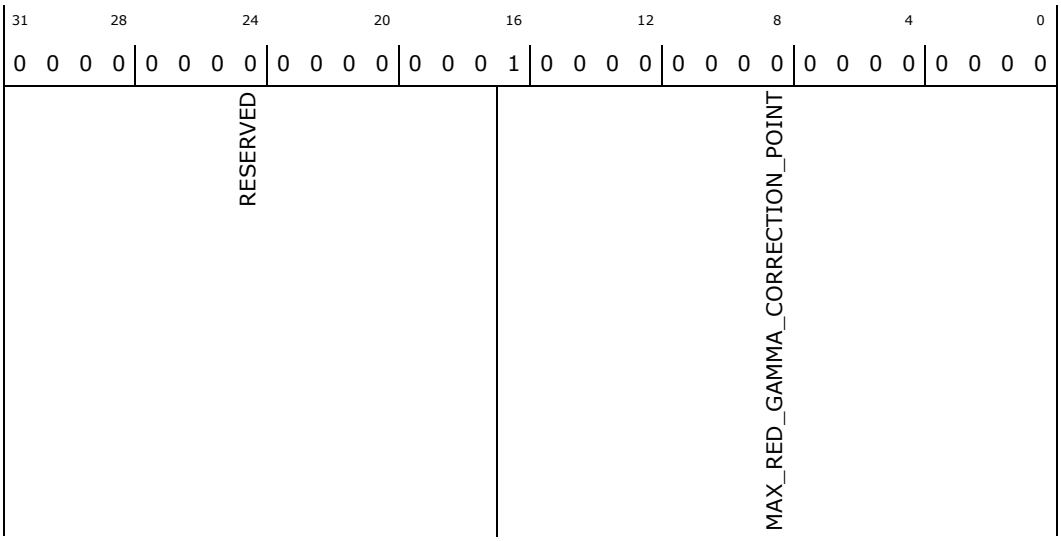
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBGCMAXRED: [GTTMMADR_LSB + 2BF20h] + 71010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	10000000000000000b RW	**MAX_RED_GAMMA_CORRECTION_POINT:** . 129th reference point for red channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

3.4.244 PIPEBGCMAXGREEN—Offset 71014h

Pipe B Gamma Correction Max Green

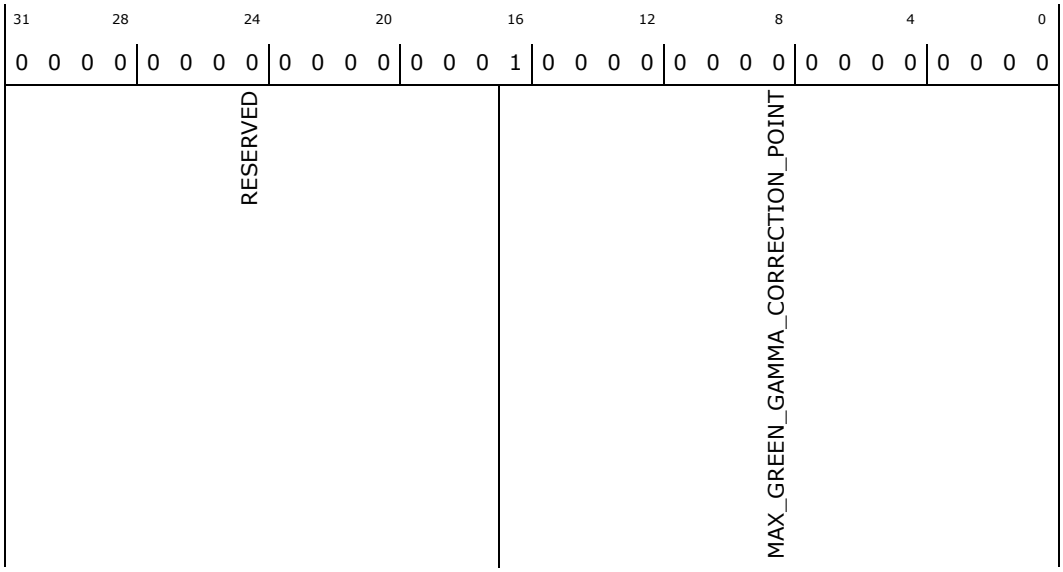
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBGCMAXGREEN: [GTTMMADR_LSB + 2BF20h] + 71014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	10000000000000000b RW	**MAX_GREEN_GAMMA_CORRECTION_POINT:** . 129th reference point for green channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

3.4.245 PIPEBGCMAXBLUE—Offset 71018h

Pipe B Gamma Correction Max Blue

Access Method

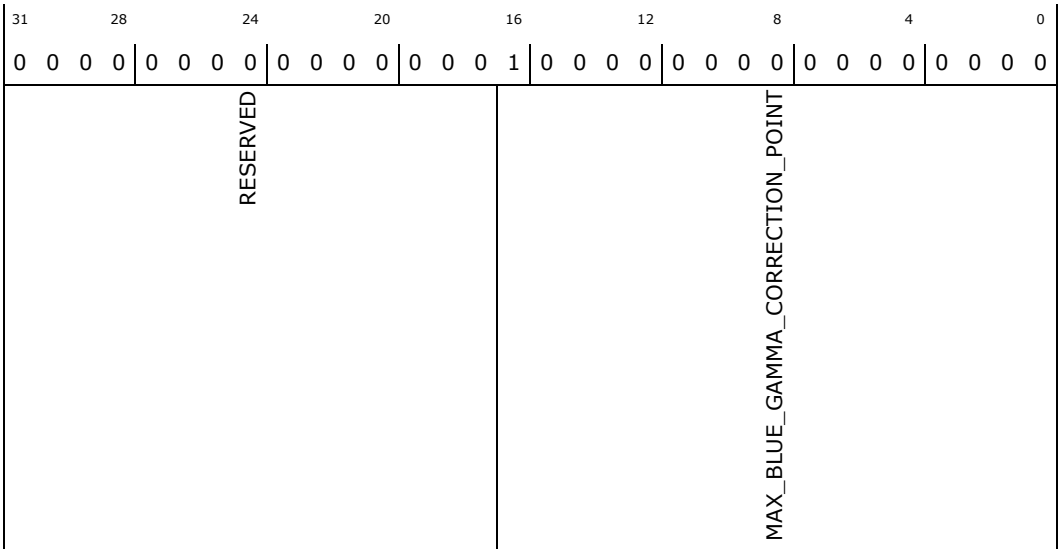
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBGCMAXBLUE: [GTTMMADR_LSB + 2BF20h] + 71018h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	10000000000000000b RW	**MAX_BLUE_GAMMA_CORRECTION_POINT:** . 129th reference point for blue channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

3.4.246 PIPEBSTAT—Offset 71024h

Pipe B Status

Access Method

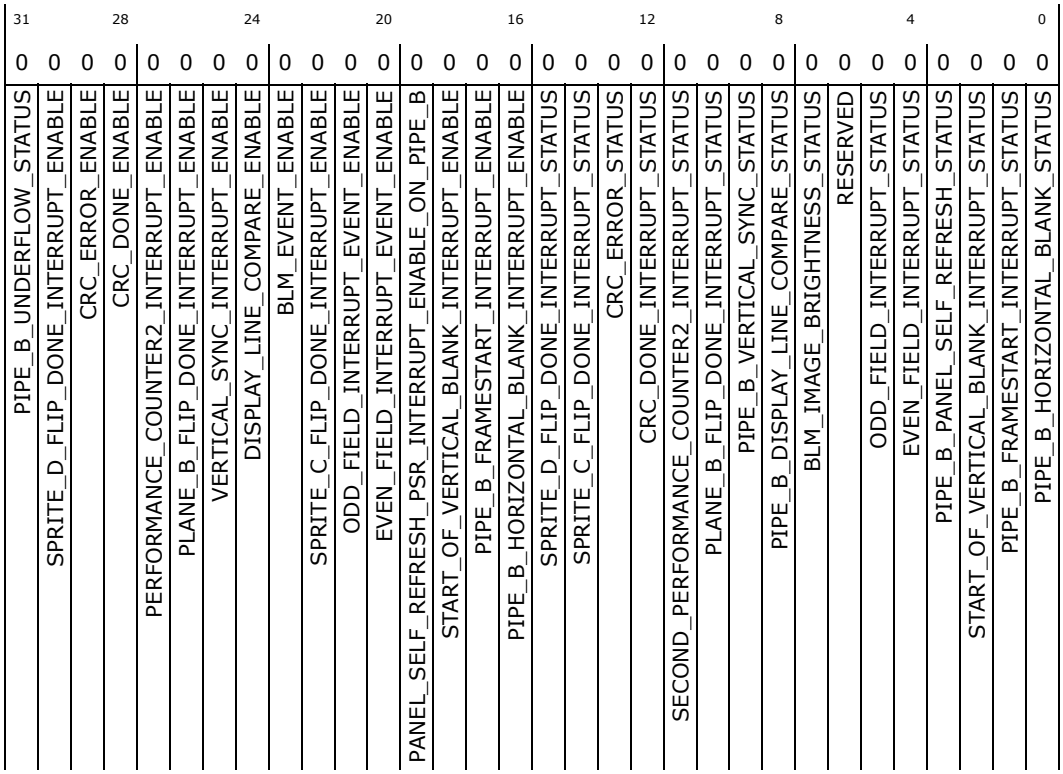
Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBSTAT: [GTTMMADR_LSB + 2BF20h] + 71024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/1C	**PIPE_B_UNDERFLOW_STATUS:** This bit is set when an underflow occurs at the display pipe B. It is cleared by writing a one to this bit. This event will occur naturally during mode changes, to be effective, it should be cleared after a mode change. This bit is only valid after Pipe B has been completely configured. 1 = FIFO B Underflow occurred 0 = FIFO B Underflow did not occur AccessType: One to Clear
30	0b RW	**SPRITE_D_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite D flip done interrupt status bit in the first line interrupt logic 0 = Sprite D Flip Done Interrupt Disabled 1 = Sprite D Flip Done Interrupt Enabled
29	0b RW	**CRC_ERROR_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt/status logic. 0 = CRC Error Detect Disabled 1 = CRC Error Detect Enabled
28	0b RW	**CRC_DONE_ENABLE:** This will enable the consideration of the CRC done status bit in the first line interrupt/status logic. 0 = CRC Done Detect Disabled 1 = CRC Done Detect Enabled
27	0b RW	**PERFORMANCE_COUNTER2_INTERRUPT_ENABLE:** This bit enables the second performance counter interrupt. 0 = Second Performance Counter2 Interrupt Status Disabled 1 = Second Performance Counter2 interrupt Status Enabled

Bit Range	Default & Access	Description
26	0b RW	**PLANE_B_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Plane B flip done interrupt status bit in the first line interrupt logic 0 = Plane B flip done Interrupt/Status Disabled 1 = Plane B flip done Interrupt/Status Enabled
25	0b RW	**VERTICAL_SYNC_INTERRUPT_ENABLE:** 0 = Vertical Sync Interrupt/ Status Disabled 1 = Vertical Sync Interrupt/Status Enabled
24	0b RW	**DISPLAY_LINE_COMPARE_ENABLE:** 0 = Pipe B Display Line Compare Status Report Disabled 1 = Pipe B Display Line Compare Status report Enabled
23	0b RW	**BLM_EVENT_ENABLE:** [DevCL, DevCTG, DevCDV]: This interrupt is generated by the image brightness segment comparators. Which segment cause an interrupt are controlled by the BLM Histogram control register. 0 = No BLM event enabled 1 = BLM event enabled
22	0b RW	**SPRITE_C_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite C flip done interrupt status bit in the first line interrupt logic 0 = Sprite C Flip Done Interrupt Disabled 1 = Sprite C Flip Done Interrupt Enabled
21	0b RW	**ODD_FIELD_INTERRUPT_EVENT_ENABLE:** . This bit should only be used when this pipe is in an interlaced display timing.0 = Odd Field Event disable 1 = Odd Field Event enable
20	0b RW	**EVEN_FIELD_INTERRUPT_EVENT_ENABLE:** . This bit should only be used when this pipe is in an interlaced display timing.0 = Even field Event disable 1 = Even field Event enable
19	0b RW	**PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_B:** 0 = PSR interrupt Disabled on Pipe B 1 = PSR Interrupt Enabled on Pipe B
18	0b RW	**START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Start of Vertical Blank Interrupt/Status Disabled 1 = Start of Vertical Blank Interrupt/Status Enabled
17	0b RW	**PIPE_B_FRAMESTART_INTERRUPT_ENABLE:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Pipe B Framestart Interrupt/Status Disabled 1 = Pipe B Framestart Interrupt/Status Enabled
16	0b RW	**PIPE_B_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** : This will enable the consideration of the start of horizontal blank interrupt status bit in the first line interrupt/status logic0 = Start of Horizontal Blank Interrupt/Status Disabled 1 = Start of Horizontal Blank Interrupt/Status Enabled
15	0b RW/1C	**SPRITE_D_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite D 0 = Sprite D Flip Not Done 1 = Sprite D Flip Done AccessType: One to Clear
14	0b RW/1C	**SPRITE_C_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite C 0 = Sprite C Flip Not Done 1 = Sprite C Flip Done AccessType: One to Clear
13	0b RW/1C	**CRC_ERROR_STATUS:** This bit is set when a Pipe B CRC error is detected. It is cleared by a write of a one. 0 = No CRC Error 1 = CRC Error detected AccessType: One to Clear

Bit Range	Default & Access	Description
12	0b RW/1C	**CRC_DONE_INTERRUPT_STATUS:** This bit is set when Pipe B CRC calculation and compare are complete. It is cleared by a write of a one. 0 = CRC Not Done 1 = CRC Done AccessType: One to Clear
11	0b RW/1C	**SECOND_PERFORMANCE_COUNTER2_INTERRUPT_STATUS:** This bit is set when the second performance counter2 generates an interrupt. It is cleared by a write of a one. 0 = Second performance counter interrupt event not asserted 1 = Second performance counter interrupt event asserted AccessType: One to Clear
10	0b RW/1C	**PLANE_B_FLIP_DONE_INTERRUPT_STATUS:** Async/Sync Flip Event is completed on Display Plane B 0 = Plane B Flip Not Done 1 = Plane B Flip Done AccessType: One to Clear
9	0b RW/1C	**PIPE_B_VERTICAL_SYNC_STATUS:** 0 = Vertical Sync not asserted 1 = Vertical Sync asserted AccessType: One to Clear
8	0b RW/1C	**PIPE_B_DISPLAY_LINE_COMPARE_STATUS:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 = Display Line Compare Status not asserted 1 = Display Line Compare Status asserted AccessType: One to Clear
7	0b RW/1C	**BLM_IMAGE_BRIGHTNESS_STATUS:** [DevCL, DevCTG, DevCDV]: This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 =DPST Interrupt has not occurred on pipe B 1 = DPST Interrupt has occurred on pipe B AccessType: One to Clear
6	0b RW	**RESERVED:** MBZ
5	0b RW/1C	**ODD_FIELD_INTERRUPT_STATUS:** . This status bit will be set on a Odd field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set.Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Odd Field Vertical Blank has not occurred 1 = Odd Field Vertical Blank has occurred AccessType: One to Clear
4	0b RW/1C	**EVEN_FIELD_INTERRUPT_STATUS:** . This status bit will be set on a even filed VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set.Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Even Field Vertical Blank has not occurred 1 = Even Field Vertical Blank has occurred AccessType: One to Clear
3	0b RW/1C	**PIPE_B_PANEL_SELF_REFRESH_STATUS:** This bit indicates interrupt is generated by the PSR controller and intends to send interrupt to SW driver when the PSR interrupt enable bit (70028h bit 22) is set. This is cleared when a write to this register occurs with this bit as a one. Write with this bit as a zero has no effect on the value of the bit. 0 = PSR Interrupt has not occurred on pipe B 1 = PSR interrupt has occurred on pipe B AccessType: One to Clear

Bit Range	Default & Access	Description
2	0b RW/1C	**START_OF_VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set at the beginning of a VBLANK event. At this point, the double buffered display registers flip, taking their new values. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. In MIPI DSR mode, GPIO TE trigger sets the Vblank Interrupt status 0 = Start of Vertical Blank has not occurred 1 = Start of Vertical Blank has occurred AccessType: One to Clear
1	0b RW/1C	**PIPE_B_FRAMESTART_INTERRUPT_STATUS:** This status bit will be set on a VBLANK event, when the frame start occurs. The display registers are updated at the start of vertical blank, but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs, which is the event that triggers this bit. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = Pipe B Framestart Status has not occurred 1 = Pipe B Framestart Status has occurred AccessType: One to Clear
0	0b RW/1C	**PIPE_B_HORIZONTAL_BLANK_STATUS:** 0 = Pipe B Horizontal Blank has not occurred 1 = Pipe B Horizontal Blank has occurred AccessType: One to Clear

3.4.247 PIPEBFRAMECOUNT—Offset 71040h

Pipe B Frame Counter

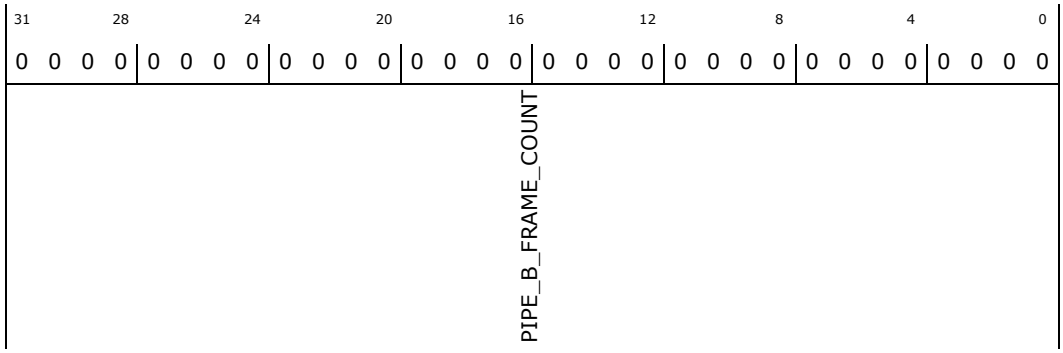
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBFRAMECOUNT: [GTTMMADR_LSB + 2BF20h] + 71040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**PIPE_B_FRAME_COUNT:** Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after 2^32 frames

3.4.248 PIPEBFLIPCOUNT—Offset 71044h

Pipe B Flip Counter

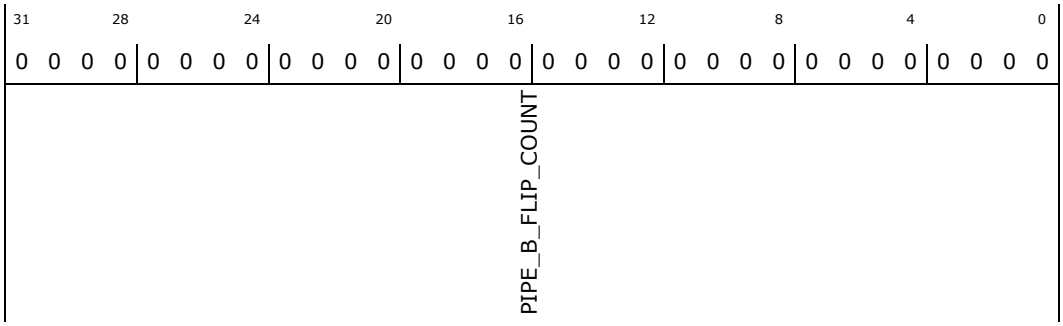
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBFLIPCOUNT: [GTTMMADR_LSB + 2BF20h] + 71044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**PIPE_B_FLIP_COUNT:** Provides read back of the display pipe flip counter. This counter increments on each flip of the surface of the primary plane on this pipe. This includes command streamer asynchronous and synchronous flips and any MMIO writes to the primary plane surface address. It rolls over back to 0 after 2^32 flips.

3.4.249 PIPEBMSAMISC—Offset 71048h

Pipe B MSA MISC

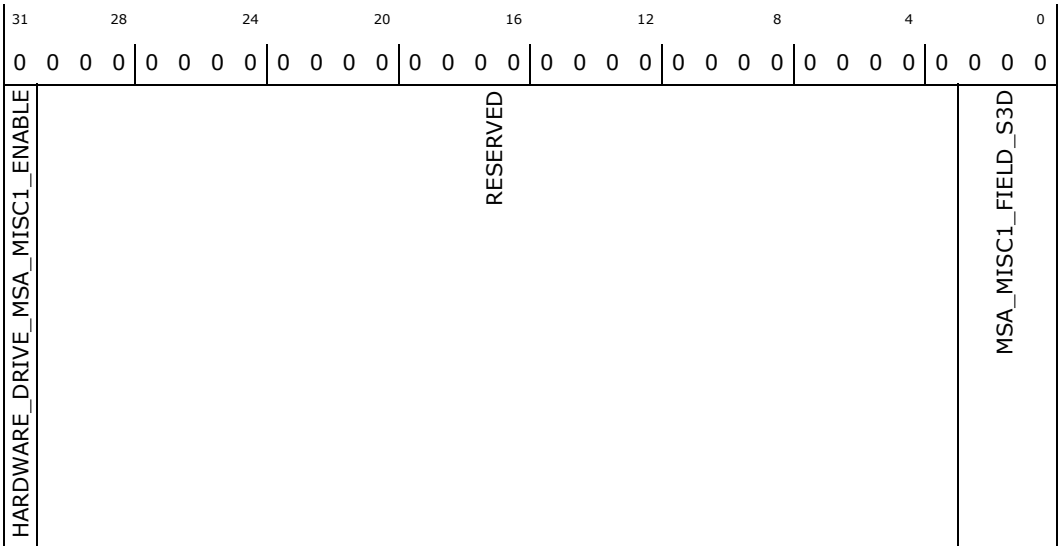
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PIPEBMSAMISC: [GTTMMADR_LSB + 2BF20h] + 71048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**HARDWARE_DRIVE_MSA_MISC1_ENABLE:** This bit enables hardware to drive MSA MISC1 bit3:1 with the stereo 3D left/right eye field indication. Hardware will drive 000 when S3D mode is disabled, 001 when enabled and the upcoming video frame is right eye, 011 when enabled and the upcoming video frame is left eye. When this bit is disabled, software may manually program the MSA MISC1 Field S3D field in bit 2:0 in this register to set MISC1 bit 3:1 0 = Disable hardware driving MSA MISC1 bit 3:1. Allow software to manually program MSA MISC1 bit3:1 through MSA_MISC1_FIELD_S3D (default) 1 = Enable hardware to drive MSA MISC1 bit3:1 for S3D
30:3	0b RW	**RESERVED:** Reserved.
2:0	0b RW	**MSA_MISC1_FIELD_S3D:** This field provides software to manually program MSC1 stereo video attribute for DisplayPort: 000 = No stereo video transported 001 = For progressive video, the next (upcoming) video frame is RIGHT eye 010 = Reserved 011 = For progressive video, the next (upcoming) video frame is LEFT eye 100 = Stacked top and bottom top half represents left-eye view and bottom half represents right-eye view 101 = Stacked top and bottom top half represents right-eye view and bottom half represents left-eye view

3.4.250 DSPBADDR—Offset 7117Ch

Display B Async flip Start Address Register

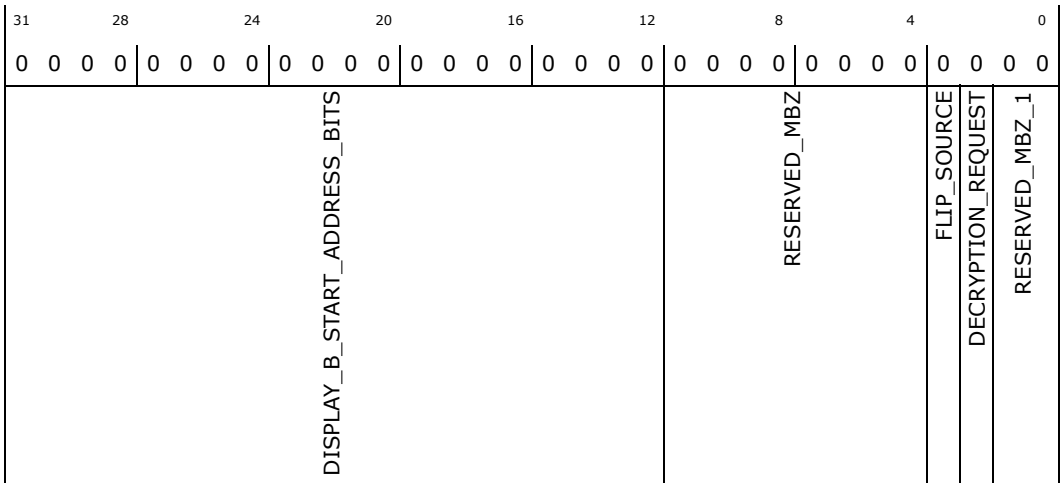
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPBADDR: [GTTMMADR_LSB + 2BF20h] + 7117Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**DISPLAY_B_START_ADDRESS_BITS:** This register provides the start address of the display B plane or the first eye when running in stereo mode. This address must be at least pixel aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . Write to this register triggers async flip The async flip address is written into the Display B Base Address register 0x7119C
11:4	0b RW	**RESERVED_MBZ:** Reserved.
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0b RW	**RESERVED_MBZ_1:** Reserved.

3.4.251 DSPBCNTR—Offset 71180h

Display B/Sprite Plane Control Register

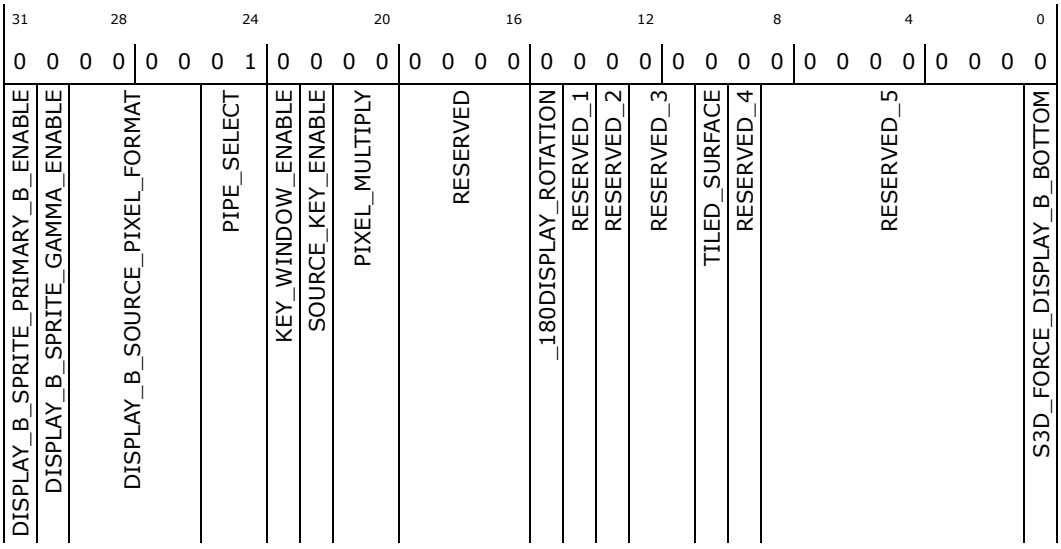
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPBCNTR: [GTTMMADR_LSB + 2BF20h] + 71180h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 01000000h



Bit Range	Default & Access	Description
31	0b RW	**DISPLAY_B_SPRITE_PRIMARY_B_ENABLE:** This bit will enable or disable the display B/sprite. When this bit is set, the plane will generate pixels for display. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. 1 = Enable 0 = Disable
30	0b RW	**DISPLAY_B_SPRITE_GAMMA_ENABLE:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane pixel data only. For 8-bit indexed display data, this bit should be set to a one. 0 = Display B pixel data bypasses the pipe gamma correction logic (default). 1 = Display B pixel data is gamma corrected in the pipe gamma correction logic

Bit Range	Default & Access	Description
29:26	0b RW	**DISPLAY_B_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/display B. Pixel formats with an alpha channel (8:8:8:8) should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 000x = Reserved. 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format. (with pre-multiplied alpha color format) 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format. (with pre-multiplied alpha color format) 1010 = 32-bit BGRX (10:10:10:2) pixel format Ignore alpha 1011 = 32-bit BGRA (10:10:10:2) pixel format (with pre-multiplied alpha color format) 1100 = 64-bit RGBX (16:16:16:16) 16 bit floating point pixel format. Ignore alpha. 1101 = 64-bit RGBA (16:16:16:16) 16-bit floating point pixel format (with pre-multiplied color format) 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8) pixel format (with pre-multiplied color format)
25:24	01b RO	**PIPE_SELECT:** Plane B always ties to Pipe B. Reserved AccessType: Read Only
23	0b RW	**KEY_WINDOW_ENABLE:** This applies only to devices with a Display Plane C. It determines what area of the screen the source key compare should be applied. This bit is set to one when the color key is used as a destination key for display C. Display plane C must be enabled on the same pipe and display A should not be enabled on this pipe for this to be used. The function is only effective when display C is enabled and defined by Z-order to be behind display B. 0 = If keying is enabled, it applies to the entire display B plane 1 = If keying is enabled, it applies only to the intersection between display B and display C [DevBLC] and [DevCTG]: Reserved
22	0b RW	**SOURCE_KEY_ENABLE:** When used as a sprite or a secondary this enables source color keying. Sprite pixel values that match the key will become transparent. Source keying allows a plane that is behind (below) this plane to show through where the display B data matches the display B key. This function is overloaded to provide display C destination keying when combined with the key window enable bit.. Setting this bit is not allowed when the display pixel format includes an alpha channel. 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled. [DevBLC] and [DevCTG]: Reserved In destination keying, primary plane pixel will be made transparent when blending with sprite pixel as the destination if the primary src key matches with the primary pixel value.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes: Asynchronous flips are not permitted when pixel multiply is enabled. 00 = No duplication 01 = Line/pixel Doubling 10 = Reserved 11 = Pixel Doubling only
19:16	0b RW	**RESERVED:** Write as zero
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. [DevCL] Do not enable 180 rotation together with Frame Buffer Compression 0 = No rotation 1 = 180 rotation

Bit Range	Default & Access	Description
14	0b RW	**RESERVED_1:** [DevBW, DevCL, DevCDV] [DevBLC, DevCTG] Display B Trickle Feed Enable: 0 = Trickle Feed Enabled - Display B data requests are sent whenever there is space in the Display Data Buffer. 1 = Trickle Feed Disabled - Display B data requests are sent in bursts. Note: On mobile products this bit will be ignored such that Trickle Feed is always disabled. [DevELK] Must always be programmed disabled
13	0b RW	**RESERVED_2:** [DevBW, DevCL, DevCDV] [DevBLC, DevCTG] Display B Data Buffer Partitioning Control: 0 = Display B Data Buffer will encompass Sprite B buffer space when Sprite B is disabled. 1 = Display B Data Buffer will not use Sprite B buffer space when Sprite B is disabled. Note: When in C3xR Max FIFO mode, this bit will be ignored.
12:11	0b RW	**RESERVED_3:** Reserved.
10	0b RW	**TILED_SURFACE:** This bit indicates that the display B surface data is in tiled memory. The tile pitch is specified in bytes in the DSPBSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPBLINOFF, DSPBTILEOFF, and DSPBSURF registers. 0 = Display B surface uses linear memory 1 = Display B surface uses X-tiled memory
9	0b RW	**RESERVED_4:** [DevBW, DevCL, DevCDV] Write as zero [DevBLC, DevCTG] Asynchronous Surface Address Update Enable: This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions: No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 = DSPBSURF MMIO writes will update synchronous to start of vertical blank (default) 1 = DSPBSURF MMIO writes will update asynchronously
8:1	0b RW	**RESERVED_5:** Write as zero
0	0b RW	**S3D_FORCE_DISPLAY_B_BOTTOM:** This bit will force the display B plane to be on the bottom of any sprite planes in the Z order. 0 = Display B Z-order is determined by the other control bits in pipe B 1 = Display B is forced to be on the bottom of any sprite planes in Z-order in pipe B

3.4.252 DSPBLINOFFSET—Offset 71184h

Display B/Sprite Linear Offset Register

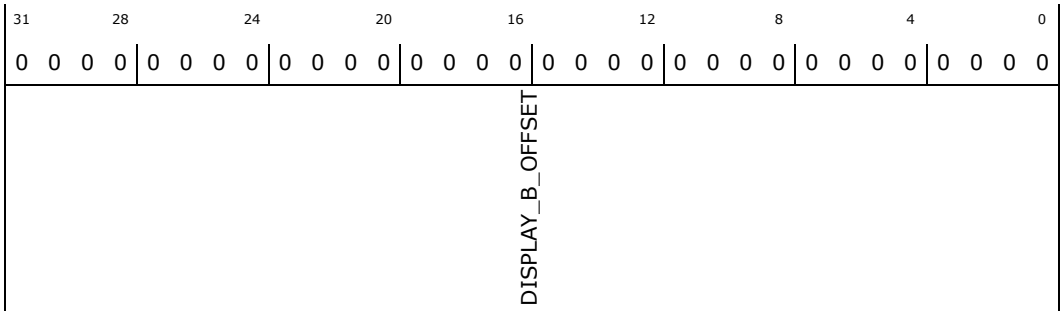
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPBLINOFFSET: [GTTMMADR_LSB + 2BF20h] + 71184h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**DISPLAY_B_OFFSET:** This register provides the panning offset into the display B plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

3.4.253 DSPBSTRIDE—Offset 71188h

Display B/Sprite Stride Register

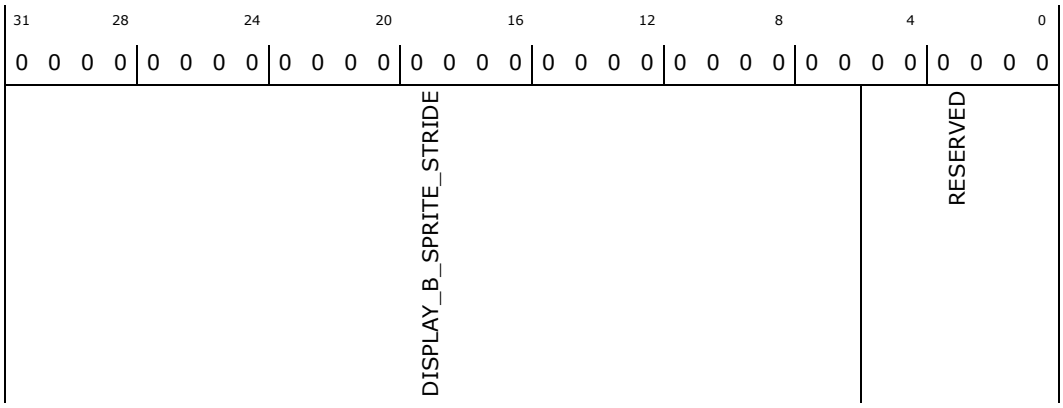
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPBSTRIDE: [GTTMMADR_LSB + 2BF20h] + 71188h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**DISPLAY_B_SPRITE_STRIDE:** This is the stride for display B/Sprite in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. The maximum value for this register is fixed. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes. [DevBW, DevCL, DevCDV] The display stride must be power of 2 when doing Asynch Flips. [DevBW, DevCL, DevCDV] The display stride must be 8KB or greater when doing Asynch Flips together with 180 rotation. The value in this register is updated through the command streamer during a synchronous flip.
5:0	0b RW	**RESERVED:** Reserved.

3.4.254 DSPBKEYVAL—Offset 71194h

Sprite Color Key Value Register

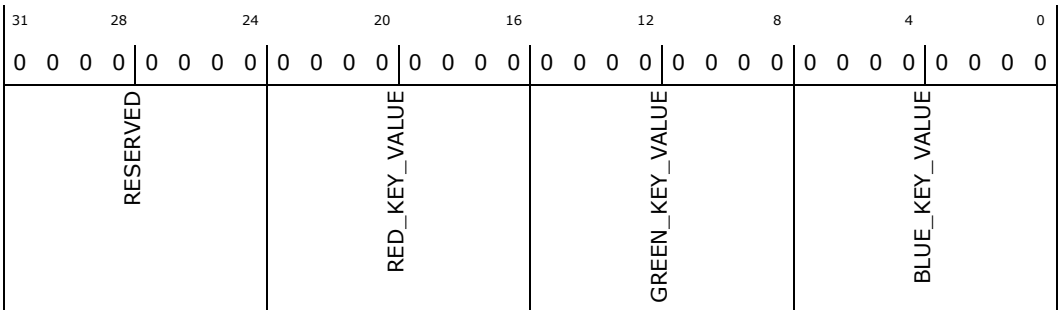
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPBKEYVAL: [GTTMMADR_LSB + 2BF20h] + 71194h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	0b RW	**RED_KEY_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_VALUE:** Specifies the color key value for the sprite green/Y channel.

Bit Range	Default & Access	Description
7:0	0b RW	**BLUE_KEY_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

3.4.255 DSPBKEYMSK—Offset 71198h

Sprite Color Key Mask Register

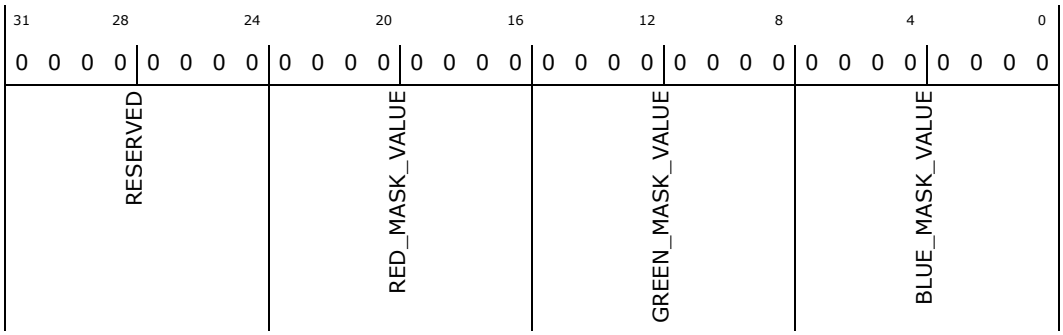
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPBKEYMSK: [GTTMMADR_LSB + 2BF20h] + 71198h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	0b RW	**RED_MASK_VALUE:** Specifies the color key mask for the sprite red/Cr channel.
15:8	0b RW	**GREEN_MASK_VALUE:** Specifies the color key mask for the sprite green/Y channel.
7:0	0b RW	**BLUE_MASK_VALUE:** Specifies the color key mask for the sprite blue/Cb channel.

3.4.256 DSPBSURF—Offset 7119Ch

Display B Surface Address Register

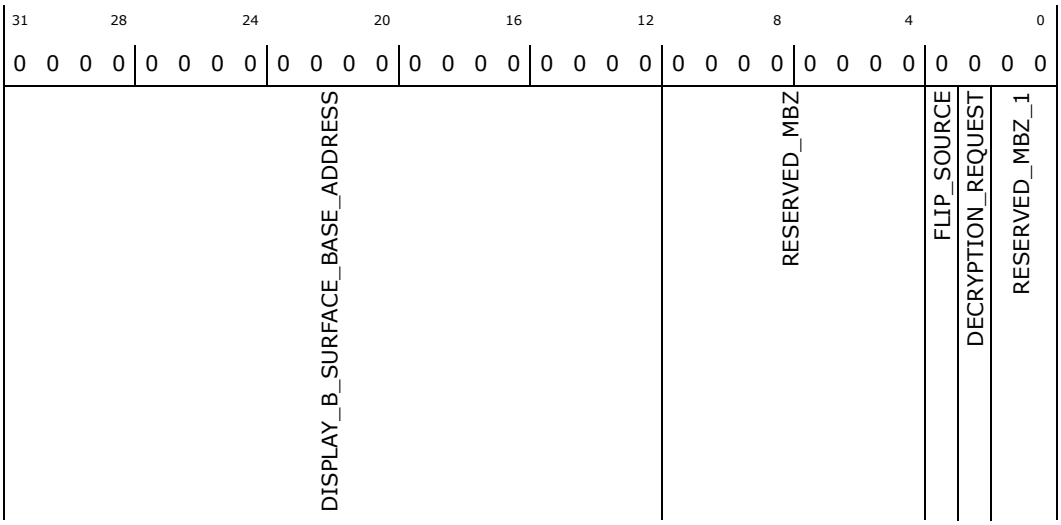
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPBSURF: [GTTMMADR_LSB + 2BF20h] + 7119Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**DISPLAY_B_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPBTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPBLINOFF register. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED_MBZ:** Reserved.
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0b RW	**RESERVED_MBZ_1:** Reserved.

3.4.257 DSPBTILEOFF—Offset 711A4h

Display B Tiled Offset Register

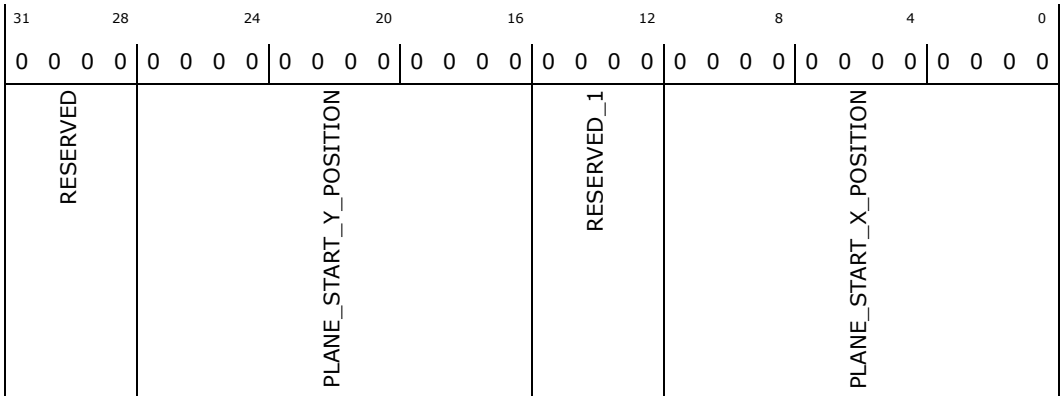
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPBTILEOFF: [GTTMMADR_LSB + 2BF20h] + 711A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation. [DevBW, DevCL, DevCDV] When display stride is 16KB and doing Asynch Flips, do not program the offset to give pans of 7680 to 8191 bytes.

3.4.258 DSPBSURFLIVE—Offset 711ACh

Display B Live Surface Base Address Register [DevCTG-B, DevCDV]

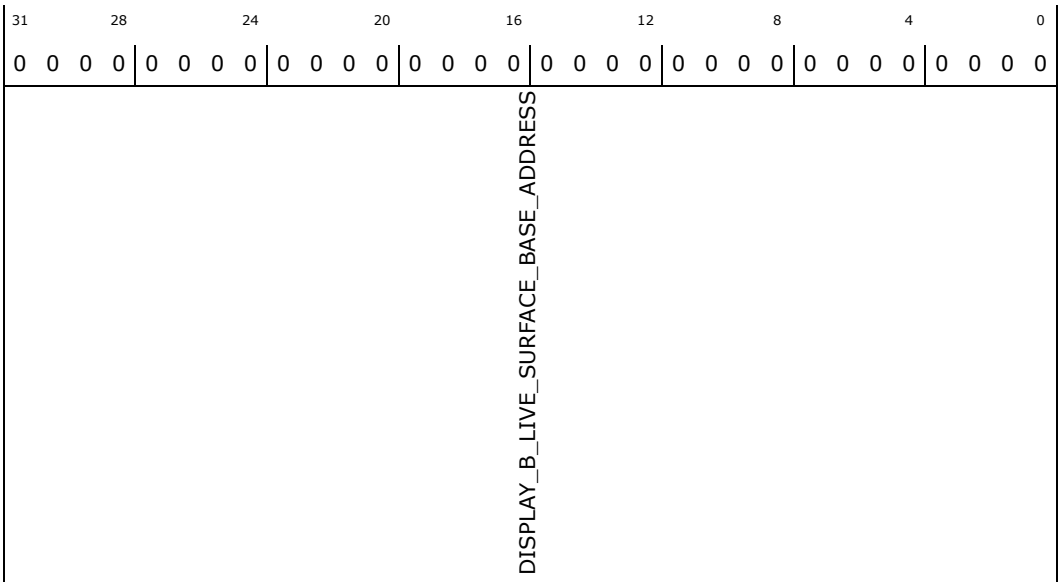
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPBSURFLIVE: [GTTMMADR_LSB + 2BF20h] + 711ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**DISPLAY_B_LIVE_SURFACE_BASE_ADDRESS:** . This gives the live value of the surface base address as being currently used for the plane.

3.4.259 DSPBFLPQSTAT—Offset 71200h

Flip Queue Status Register

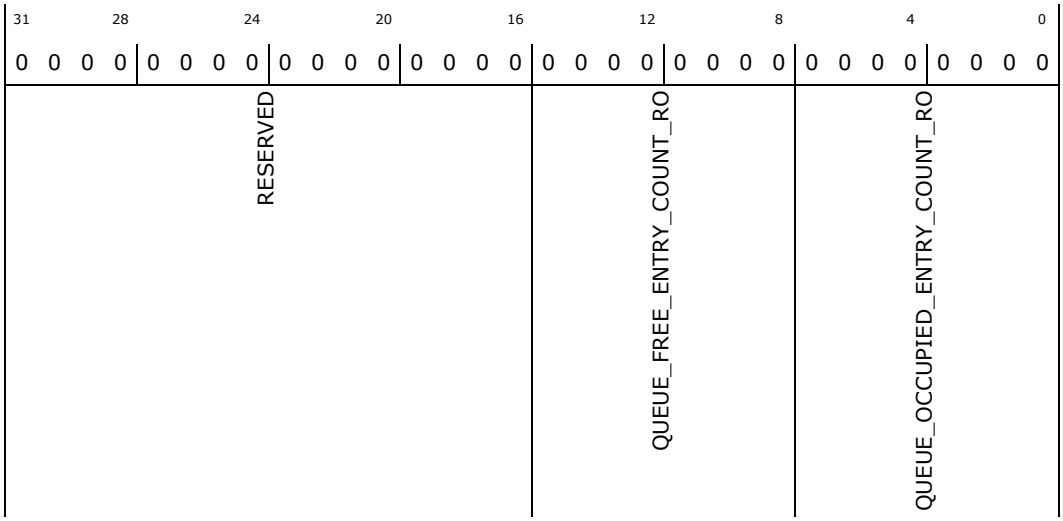
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSPBFLPQSTAT: [GTTMMADR_LSB + 2BF20h] + 71200h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RESERVED:** Write as zero (RO)
15:8	0b RO	**QUEUE_FREE_ENTRY_COUNT_RO:** This value indicates the number of free entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.
7:0	0b RO	**QUEUE_OCCUPIED_ENTRY_COUNT_RO:** This value indicates the number of occupied entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.

3.4.260 VGACNTRL—Offset 71400h

VGA Display Plane Control Register

Access Method

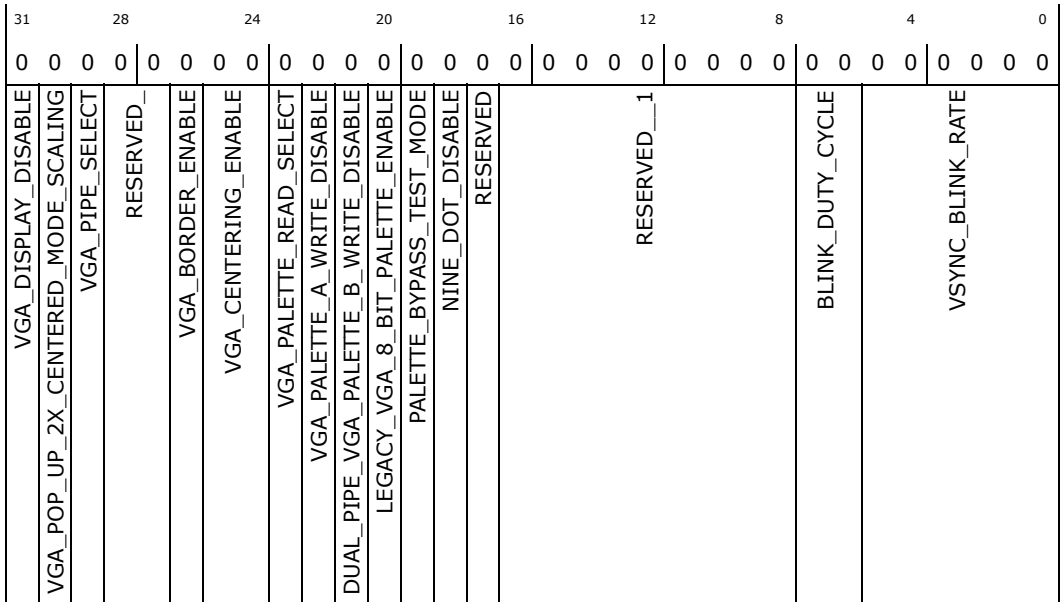
Type: Memory Mapped I/O Register (Size: 32 bits)

VGACNTRL: [GTTMMADR_LSB + 2BF20h] + 71400h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

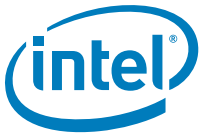
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**VGA_DISPLAY_DISABLE:** This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000-BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA register settings. VGA display should only be enabled if all display planes other than VGA are disabled. After enabling the VGA, most display planes need to stay disabled, only the VGA popup (cursor A) can be enabled. The VGA display is never trusted. No secrets are allowed in the pre-allocated memory and VGA is limited to access only that memory. During trusted operation (when registers are locked via Lock), this bit will always act as if it was set to a one (disabled VGA display). VGA 132 Column text mode is not supported. 0 = VGA Display Enabled 1 = VGA Display Disabled
30	0b RW	**VGA_POP_UP_2X_CENTERED_MODE_SCALING:** When this bit is set to a one, the VGA and pop-up data is scaled using pixel doubling in both the horizontal and vertical direction for use on un-scaled flat panel displays. Setting this bit allows the VGA to run at higher dot clock frequencies and creates a larger (4x the size) image for better quality on larger displays. It is intended for use in one of the centering modes when not using the internal panel fitting. Do not use it for native VGA modes or when internal panel fitting is used to scale VGA. In the situations where it is used, for 1280 wide or larger panels this bit should be set. For exactly 1280 wide panels, the Nine-dot disable bit should also be set. This operation is in addition to the VGA functions that double the pixels and lines. 0 = VGA display is normal size 1 = VGA and VGA popup data is doubled in the horizontal and vertical direction.

Bit Range	Default & Access	Description
29	0b RW	**VGA_PIPE_SELECT:** This bit only applies to devices with dual pipe support. For devices with a single display pipe, this bit will be ignored. For dual pipe devices, this bit determines which pipe is to receive the VGA display data. This must be changed only when the VGA display is in the disabled state via the VGA display disable bit or during the write to enable VGA display. 0 = Selects Assigns the VGA display to Pipe A 1 = Selects Assigns the VGA display to Pipe B
28:27	0b RW	**RESERVED_:** Software must preserve the contents of these bits.
26	0b RW	**VGA_BORDER_ENABLE:** This bit determines if the VGA border areas during VGA centering modes are included in the active display area and do or do not appear on integrated TV encoder output and devices that use centering such as on DVO connected flat panel, TV displays, or integrated panels. For use with the internal panel fitting logic, the border if enabled will be scaled along with the pixel data. Setting this bit allows the popup to be positioned overlapping the border area of the image. 0 = VGA Border areas are not included in the image size calculations for centering only active area. 1 = VGA Border areas are enabled and is passed to the display pipe for display and used in the image size calculation for centering modes
25:24	0b RW	**VGA_CENTERING_ENABLE:** VGA centering modes use the pipe timing generators to determine the actual display timings. This would normally correspond to the display panel size and timings. The VGA registers determine the centered VGA image height and width. The VGA border may or may not be considered in the calculation selected by the VGA Border Enable bit. For a proper image, the VGA image size should not exceed the pipe timing generator active rectangle. When using the internal panel fitting logic, the horizontal image size needs to be less than or equal to 2048 pixels to generate a proper image. The VGA image will either be centered within the pipe timing rectangle or appear in the upper left corner. Upper left corner centered mode is generally used for external panel scaling where the DVO stall signal is used and is always used for internal panel fitting operation. When panel fitter is enabled on the same pipe as VGA this register setting is ignored and upper left corner centered mode is always selected. When centering is disabled, the VGA CRTC registers determine the display timing compatible with legacy VGA devices for driving CRT like devices. 00 = VGA centering is disabled, VGA operates in Native VGA mode or when driving integrated TV 01 = VGA centering is enabled, VGA image appears in the center of the larger rectangle 10 = VGA centering is enabled, VGA image appears in the upper left corner of the larger rectangle 11 = VGA centering is enabled, VGA image appears in the upper left corner of the larger rectangle
23	0b RW	**VGA_PALETTE_READ_SELECT:** This bit only applies to dual display pipe devices and determines which palette VGA palette read accesses will occur from. 0 = VGA palette reads will access Palette A (default). 1 = VGA palette reads will access Palette B VGA palette reads are reads from I/O address 0x3c9.
22	0b RW	**VGA_PALETTE_A_WRITE_DISABLE:** This determines which palette the VGA palette writes will have as a destination. One or both palettes can be the destination. If both are disabled, writes will not affect the palette RAM contents. 0 = VGA palette writes will update Palette A (default). 1 = VGA palette writes will not update Palette A VGA palette writes are writes to I/O address 0x3C9h.



Bit Range	Default & Access	Description
21	0b RW	**DUAL_PIPE_VGA_PALETTE_B_WRITE_DISABLE:** This determines which palette the VGA palette writes will have as a destination. One or both palettes can be the destination. If both are disabled, writes will not affect the palette RAM contents. 0 = VGA palette writes will update Palette B (default). 1 = VGA palette writes will not update Palette B VGA palette writes are writes to I/O address 0x3C9h.
20	0b RW	**LEGACY_VGA_8_BIT_PALETTE_ENABLE:** This bit only affects reads and writes to the palette through VGA I/O addresses. In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read. It provides backward compatibility for original VGA programs (in it s default state) as well as VESA VBE support for 8-bit palette. It does not affect palette accesses through the palette register MMIO path. 0 = 6-bit DAC (default). 1 = 8-bit DAC.
19	0b RW	**PALETTE_BYPASS_TEST_MODE:** 0 = Pass VGA data through the palette for translation (Normal Operation) 1 = Bypass the palette for allowing testing without loading palette both VGA and popup data will bypass the palette in this mode.
18	0b RW	**NINE_DOT_DISABLE:** Prevents DOS applications from setting the VGA display into a real 9-dot per character operation mode, instead the device emulates that using 8-dots per character. This is intended to provide VGA compatibility on DVI type connectors and integrated panels where there would otherwise not be room for the 720 horizontal pixels or 1440 pixels when horizontally doubled. The VGA register bit SR01(0) functionality is disabled. VGA panning control handles the pseudo 9-dot mode when both this bit is set and SR01(0) is clear. 0 = Enable use of 9-dot enable bit in VGA registers 1 = Ignore the 9-dot per character bit and always use 8
17	0b RW	**RESERVED:** Reserved.
16:8	0b RW	**RESERVED__1:** Software must preserve the contents of these bits.
7:6	0b RW	**BLINK_DUTY_CYCLE:** Controls the VGA text mode blink duty cycle relative to the cursor blink duty cycle. 00 = 100% Duty Cycle, Full Cursor Rate (Default) 01 = 25% Duty Cycle, Cursor Rate 10 = 50% Duty Cycle, Cursor Rate 11 = 75% Duty Cycle, Cursor Rate
5:0	0b RW	**VSYNC_BLINK_RATE:** Controls the VGA blink rate in terms of the number of VSYNCs per on/off cycle. These bits are programmed with the (VSYNCs/cycle)/2-1. The proper programming of this register is determined by the VSYNC rate that the display requires when in a VGA display mode.

3.4.261 SWF10—Offset 71410h

Software Flag Registers

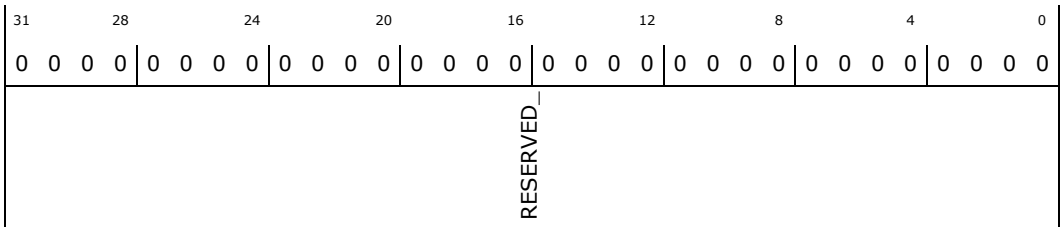
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF10: [GTTMMADR_LSB + 2BF20h] + 71410h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.262 SWF11—Offset 71414h

Software Flag Registers

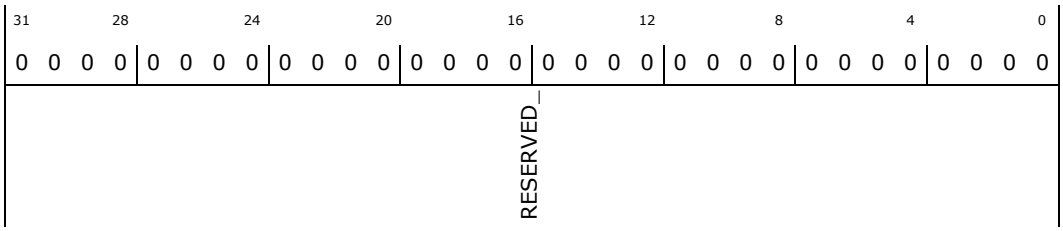
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF11: [GTTMMADR_LSB + 2BF20h] + 71414h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.263 SWF12—Offset 71418h

Software Flag Registers

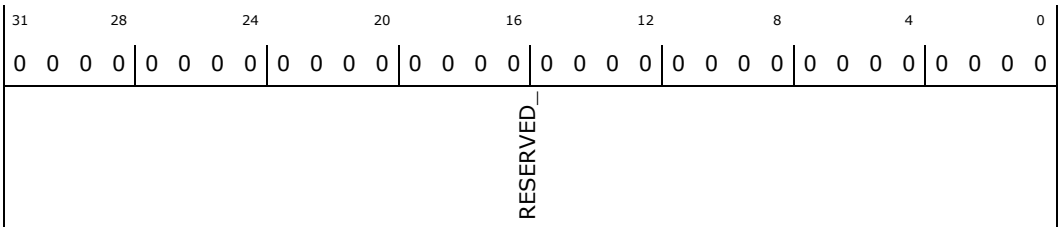
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF12: [GTTMMADR_LSB + 2BF20h] + 71418h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.264 SWF13—Offset 7141Ch

Software Flag Registers

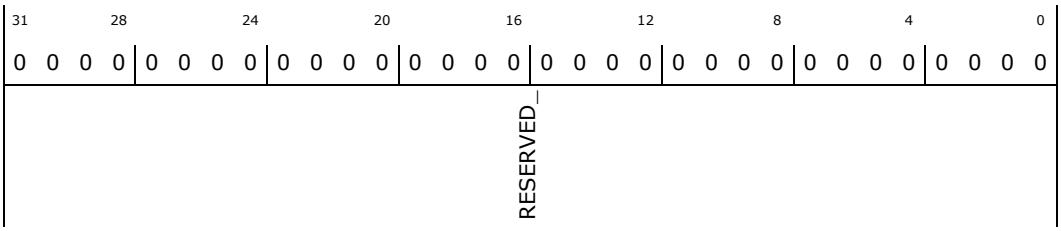
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF13: [GTTMMADR_LSB + 2BF20h] + 7141Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.265 SWF14—Offset 71420h

Software Flag Registers

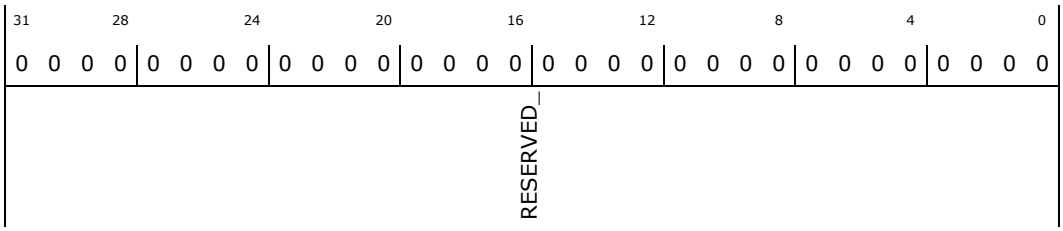
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF14: [GTTMMADR_LSB + 2BF20h] + 71420h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.266 SWF15—Offset 71424h

Software Flag Registers

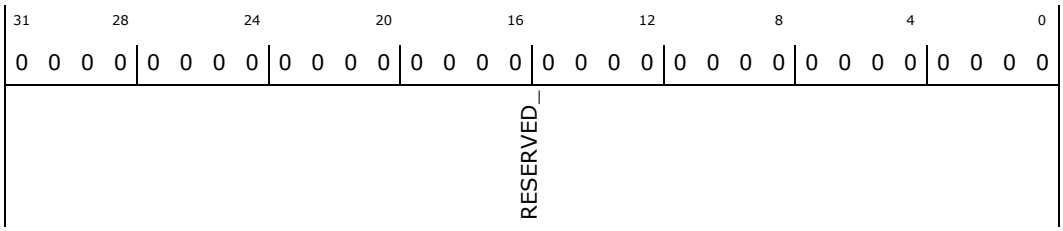
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF15: [GTTMMADR_LSB + 2BF20h] + 71424h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.267 SWF16—Offset 71428h

Software Flag Registers

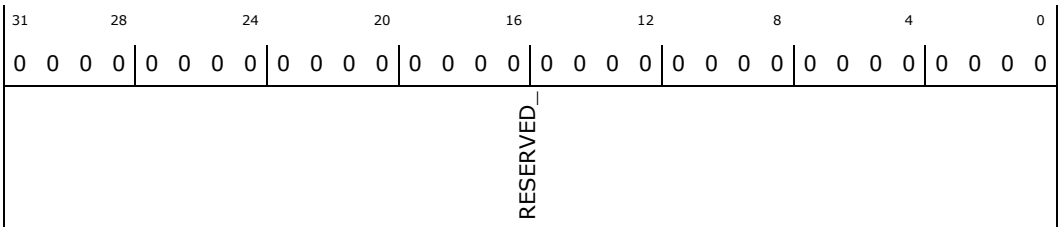
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF16: [GTTMMADR_LSB + 2BF20h] + 71428h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.268 SWF17—Offset 7142Ch

Software Flag Registers

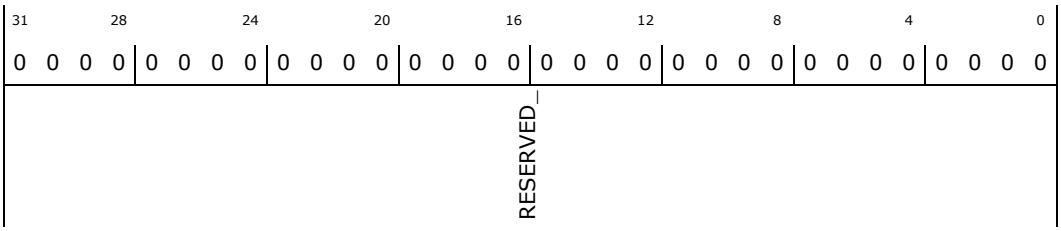
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF17: [GTTMMADR_LSB + 2BF20h] + 7142Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.269 SWF18—Offset 71430h

Software Flag Registers

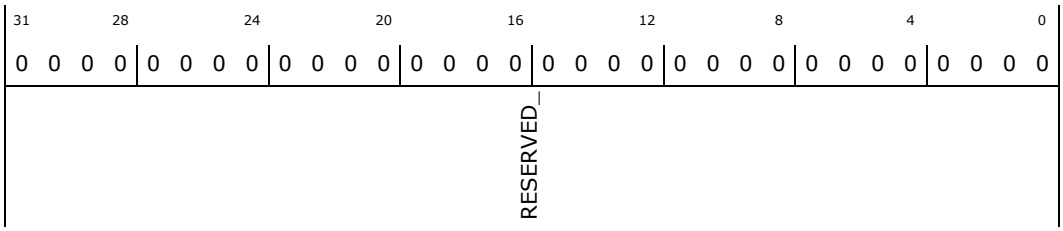
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF18: [GTTMMADR_LSB + 2BF20h] + 71430h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.270 SWF19—Offset 71434h

Software Flag Registers

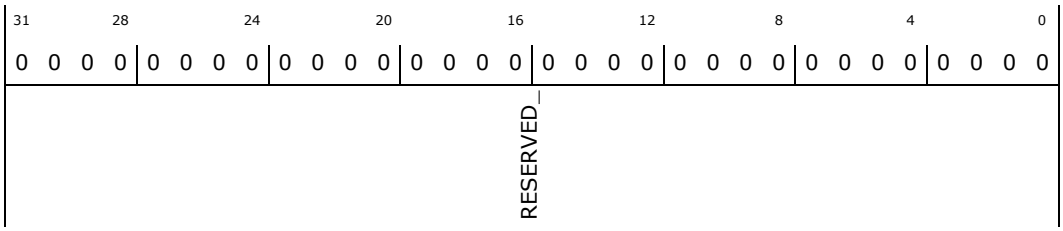
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF19: [GTTMMADR_LSB + 2BF20h] + 71434h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.271 SWF1A—Offset 71438h

Software Flag Registers

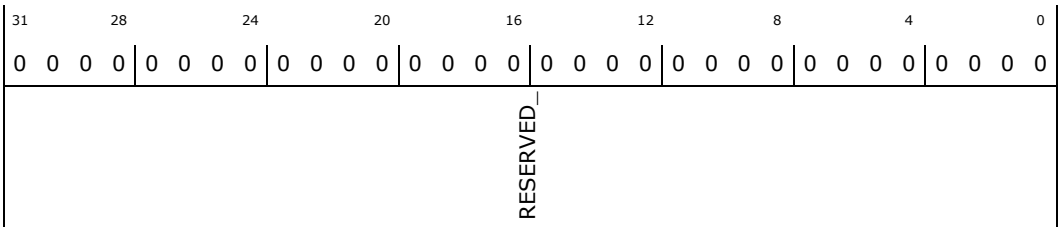
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF1A: [GTTMMADR_LSB + 2BF20h] + 71438h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.272 SWF1B—Offset 7143Ch

Software Flag Registers

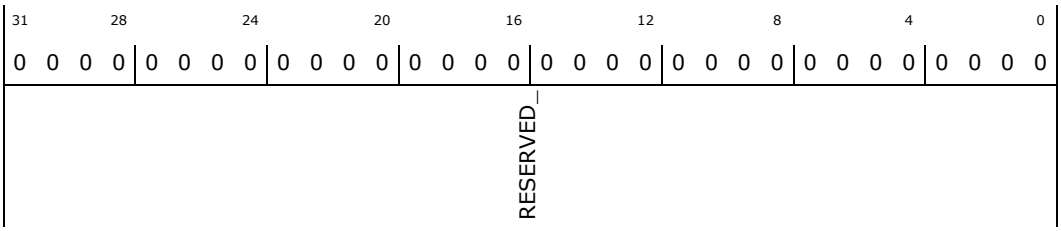
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF1B: [GTTMMADR_LSB + 2BF20h] + 7143Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.273 SWF1C—Offset 71440h

Software Flag Registers

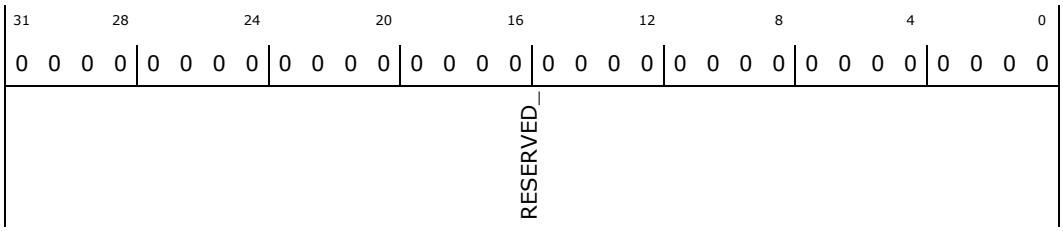
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF1C: [GTTMMADR_LSB + 2BF20h] + 71440h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.274 SWF1D—Offset 71444h

Software Flag Registers

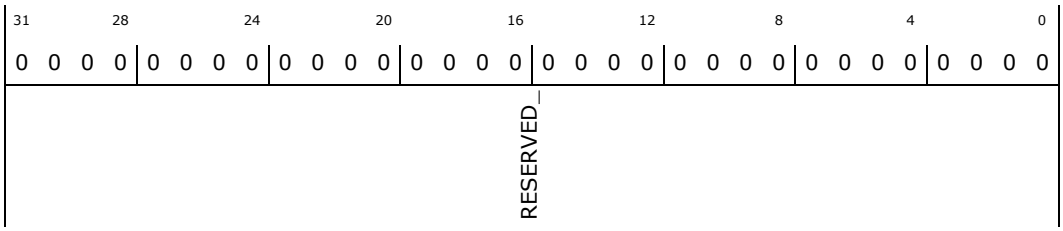
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF1D: [GTTMMADR_LSB + 2BF20h] + 71444h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.275 SWF1E—Offset 71448h

Software Flag Registers

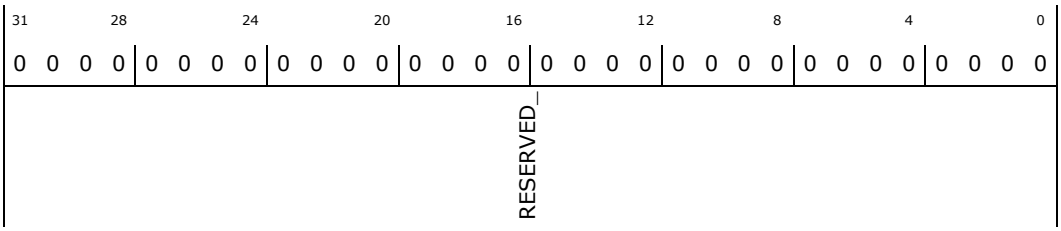
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF1E: [GTTMMADR_LSB + 2BF20h] + 71448h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.276 SWF1F—Offset 7144Ch

Software Flag Registers

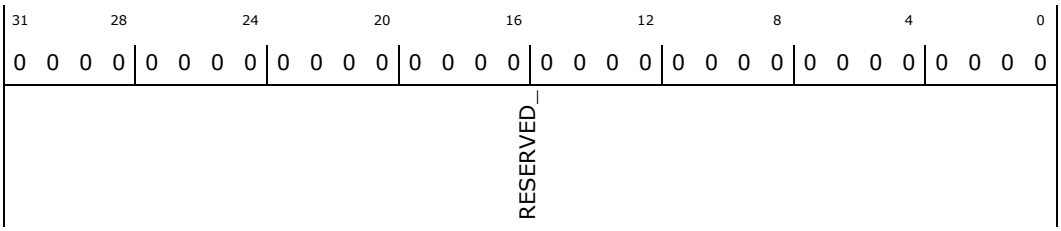
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF1F: [GTTMMADR_LSB + 2BF20h] + 7144Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.277 SPACNTR—Offset 72180h

Sprite A Control Register

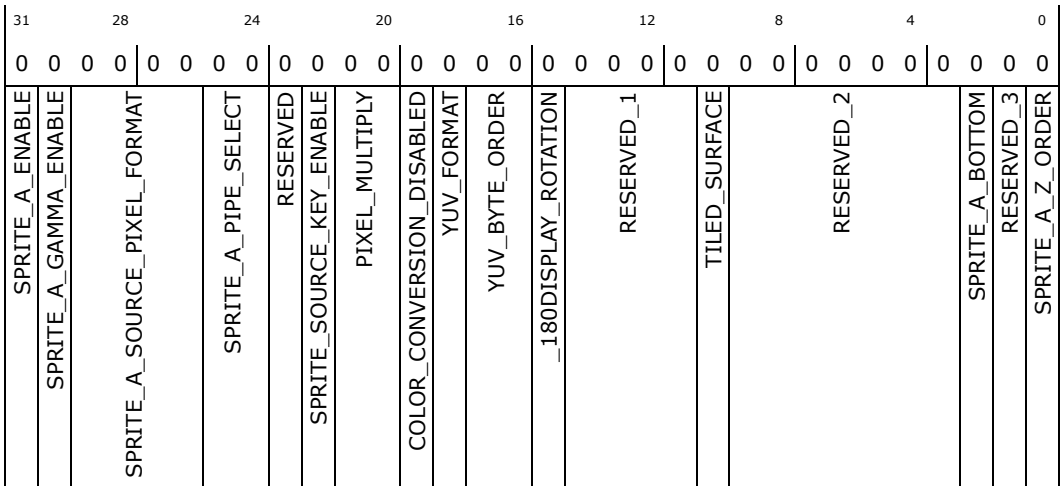
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPACNTR: [GTTMMADR_LSB + 2BF20h] + 72180h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**SPRITE_A_ENABLE:** This bit will enable or disable the Sprite A. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0b RW	**SPRITE_A_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite A data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite A logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite A pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite A pixel data is gamma corrected in the pipe gamma correction logic
29:26	0b RW	**SPRITE_A_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite A. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)

Bit Range	Default & Access	Description
25:24	0b RW	**SPRITE_A_PIPE_SELECT:** Sprite A always ties to pipe A. Reserved.
23	0b RW	**RESERVED:** Reserved.
22	0b RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite A pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite A pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled. Each sprite has built in source keying enabled/disabled. If the source keying is disabled and no alpha blending is enabled, the pixels are tagged as opaque. If sprite source keying is enabled and no alpha blending is enabled, it works as follows: For YUV sprite data, each yuv channel data is compared with the corresponding channel s key color Low and High (each channel in range can be masked out). If all three channels are in range between the low and high key values, it is considered source compared. For RGB sprite data, each 24-bit RGB pixel data is compared with the 24-bit key value (note it only uses the 24-bit Low key value for comparison). Each 24-bit has to be equal (each bit comparison can also be masked out) for the source compared. If the sprite source data compare and matches, then the sprite data will be tagged as transparent when blending with its destination pixel. If the sprite source data does not compare, then the sprite data will be tagged as opaque when blending with its destination pixel.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	0b RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0b RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0b RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0b RW	**RESERVED_1:** Reserved.

Bit Range	Default & Access	Description
10	0b RW	**TILED_SURFACE:** This bit indicates that the Sprite A surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite A surface uses linear memory 1 = Sprite A surface uses X-tiled memory
9:3	0b RW	**RESERVED_2:** Write as zero
2	0b RW	**SPRITE_A_BOTTOM:** This bit will force the Sprite A plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite A Z order is determined by the other control bits 1 = Sprite A is forced to be on the bottom of the Z order.
1	0b RW	**RESERVED_3:** Reserved.
0	0b RW	**SPRITE_A_Z_ORDER:** With Sprite A and B z-order, bottom control bits, Sprite A plane is placed in a specific z-order among other planes. Display Pipe A Z-orders SA zorderSA bottomSB zorderSB bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PA SA SB CAPA in Black 1000PA SB SA CAPA in Black 0001SB PA SA CAuse src keying on SB 0011SB PA SA CAuse src keying on SB 1001SB SA PA CAuse src keying on SA 1011SB SA PA CAuse src keying on SA 0100SA PA SB CAuse src keying on SA 1100SA PA SB CAuse src keying on SA 0110SA SB PA CAuse src keying on SB 1110SA SB PA CAuse src keying on SB 0: Sprite A z-order is disabled 1: Sprite A z-order is enabled

3.4.278 SPALINOFF—Offset 72184h

Sprite A Linear Offset Register

Access Method

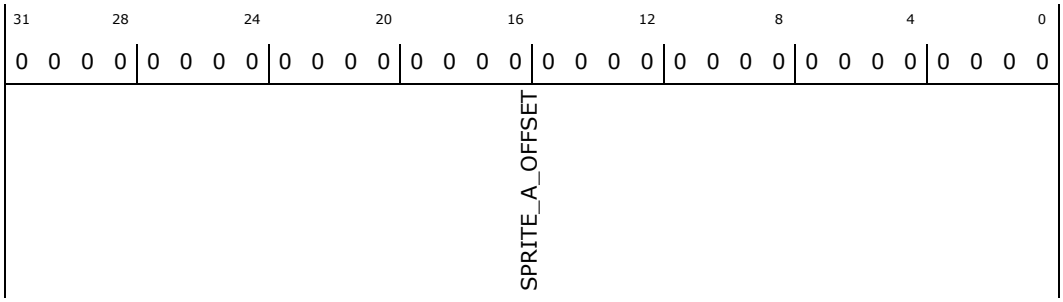
Type: Memory Mapped I/O Register (Size: 32 bits)

SPALINOFF: [GTTMMADR_LSB + 2BF20h] + 72184h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**SPRITE_A_OFFSET:** This register provides the panning offset into the Sprite A plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

3.4.279 SPASTRIDE—Offset 72188h

Sprite A Stride Register

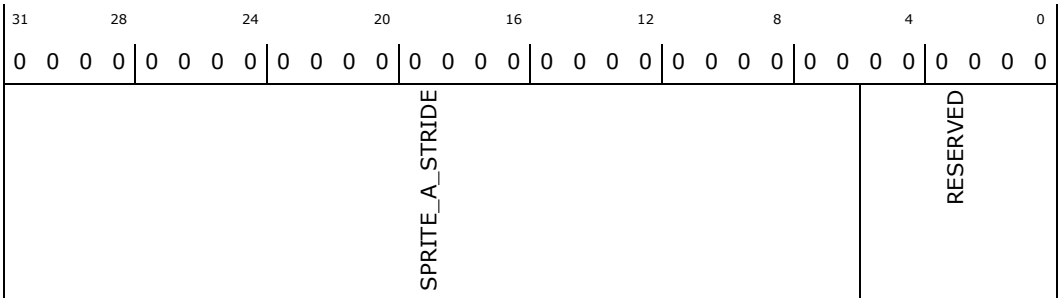
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPASTRIDE: [GTTMMADR_LSB + 2BF20h] + 72188h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**SPRITE_A_STRIDE:** This is the stride for Sprite A in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0b RW	**RESERVED:** Reserved.

3.4.280 SPAPOS—Offset 7218Ch

Sprite A Position Register

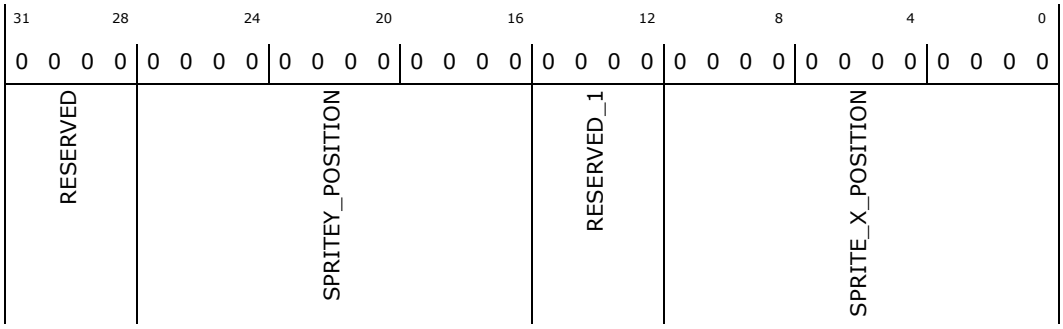
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPAPOS: [GTTMMADR_LSB + 2BF20h] + 7218Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

3.4.281 SPASIZE—Offset 72190h

Sprite A Height and Width Register

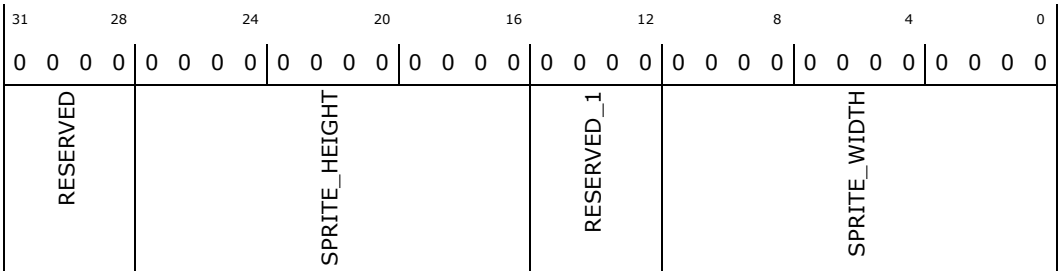
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPASIZE: [GTTMMADR_LSB + 2BF20h] + 72190h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

3.4.282 SPAKEYMINVAL—Offset 72194h

Sprite A Color Key Min Value Register

Access Method

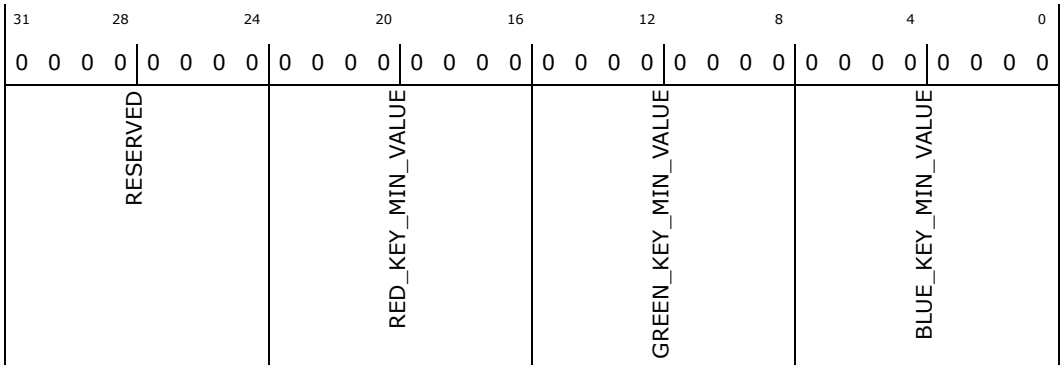
Type: Memory Mapped I/O Register (Size: 32 bits)

SPAKEYMINVAL: [GTTMMADR_LSB + 2BF20h] + 72194h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

3.4.283 SPAKEYMSK—Offset 72198h

Sprite A Color Key Mask Register

Access Method

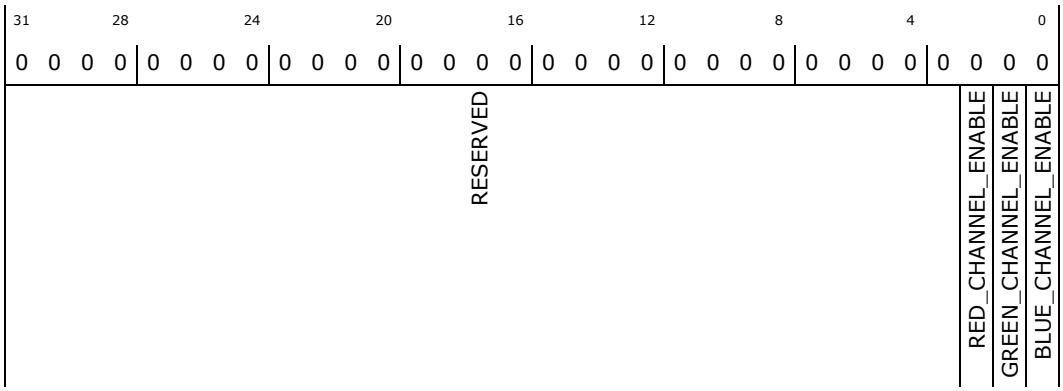
Type: Memory Mapped I/O Register (Size: 32 bits)

SPAKEYMSK: [GTTMMADR_LSB + 2BF20h] + 72198h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**RESERVED:** Write as zero
2	0b RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0b RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0b RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

3.4.284 SPASURF—Offset 7219Ch

Sprite A Surface Address Register

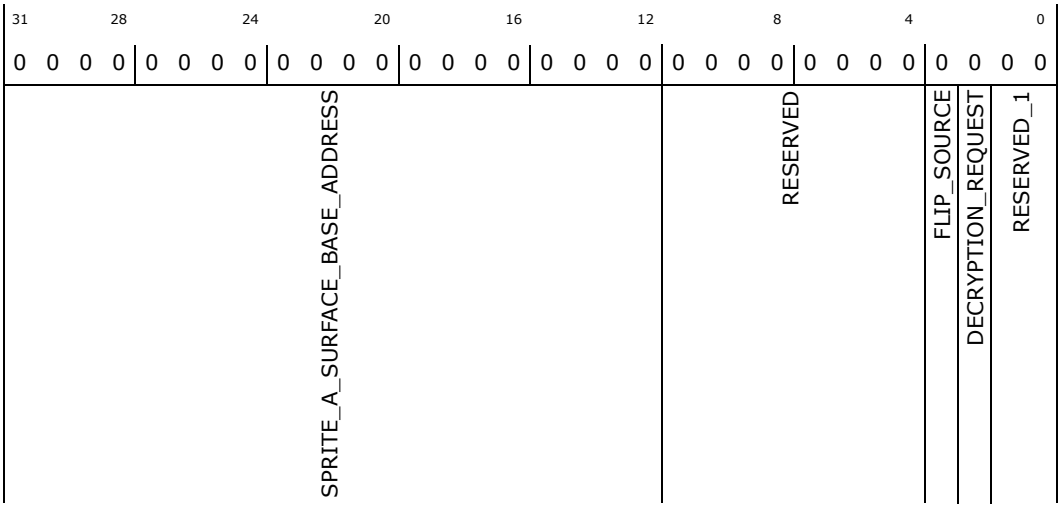
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPASURF: [GTTMMADR_LSB + 2BF20h] + 7219Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**SPRITE_A_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED:** : MBZ
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decryption not requested All 1b Requested Decryption requested All
1:0	0b RW	**RESERVED_1:** : MBZ

3.4.285 SPAKEYMAXVAL—Offset 721A0h

Sprite A Color Key Max Value Register

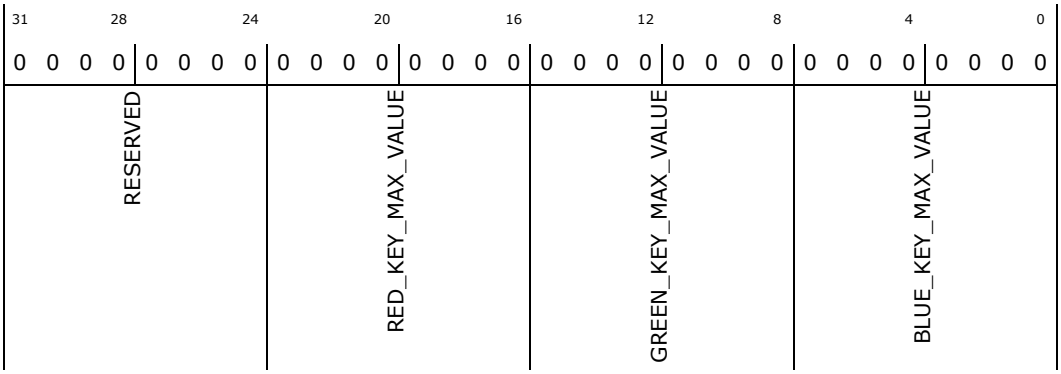
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPAKEYMAXVAL: [GTTMMADR_LSB + 2BF20h] + 721A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

3.4.286 SPATILEOFF—Offset 721A4h

Sprite A Tiled Offset Register

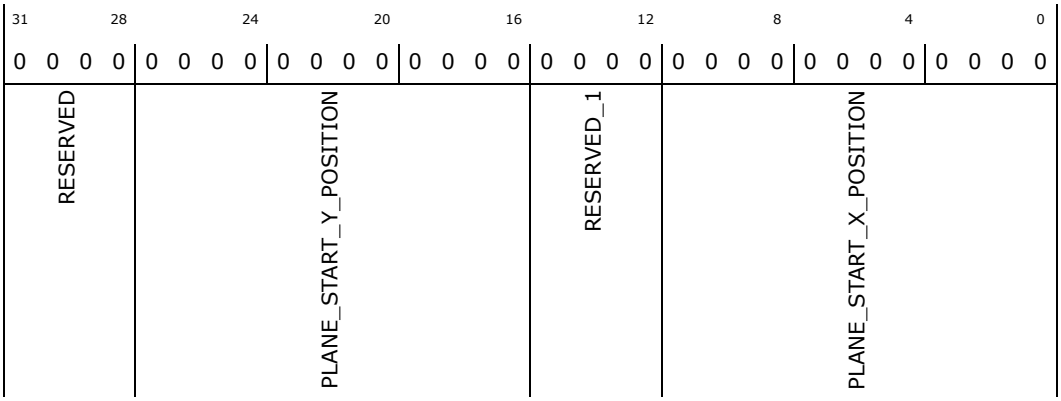
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPATILEOFF: [GTTMMADR_LSB + 2BF20h] + 721A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

3.4.287 SPACONTALPHA—Offset 721A8h

Sprite A Constant Alpha Register

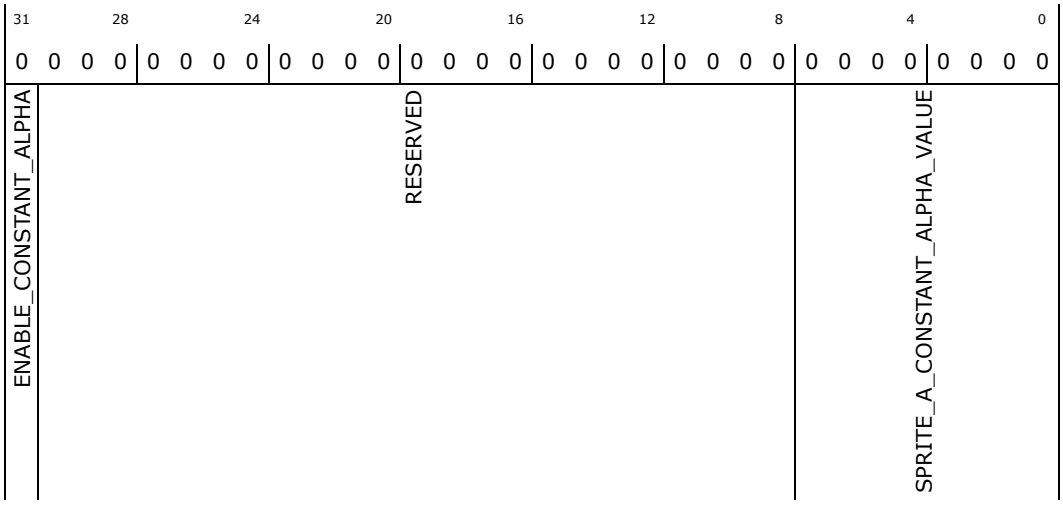
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPACONTALPHA: [GTTMMADR_LSB + 2BF20h] + 721A8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**ENABLE_CONSTANT_ALPHA:** Sprite A Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite A Sprite Constant Alpha is disabled 1 Sprite A Sprite Constant Alpha is enabled
30:8	0b RW	**RESERVED:** : MBZ
7:0	0b RW	**SPRITE_A_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

3.4.288 SPALIVESURF—Offset 721ACh

Sprite A Live Surface Address Register

Access Method

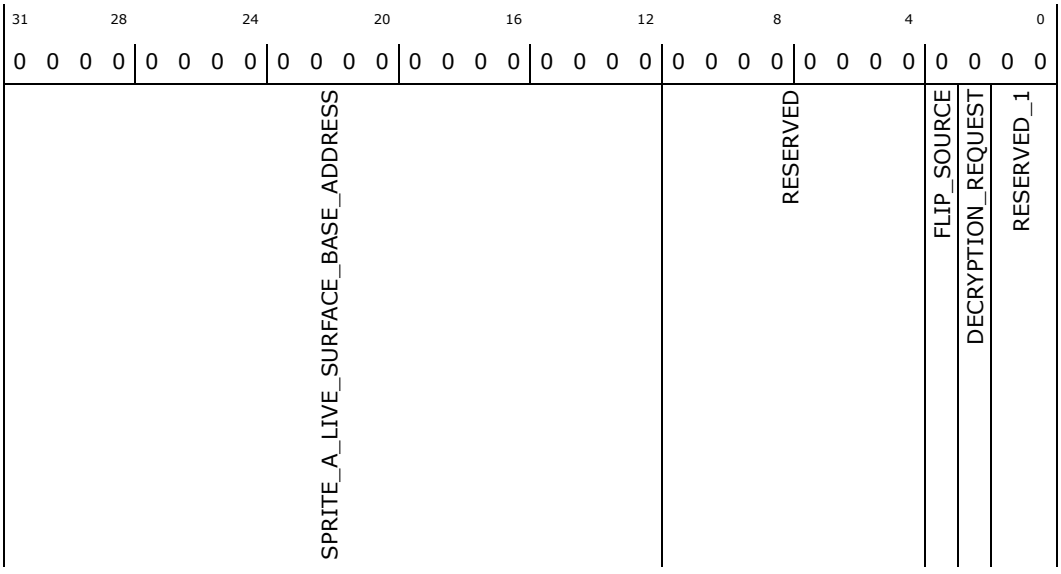
Type: Memory Mapped I/O Register (Size: 32 bits)

SPALIVESURF: [GTTMMADR_LSB + 2BF20h] + 721ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**SPRITE_A_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for the Sprite A plane.

Bit Range	Default & Access	Description
11:4	0b RO	**RESERVED:** : MBZ
3	0b RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decryption not requested All 1b Requested Decryption requested All
1:0	0b RO	**RESERVED_1:** : MBZ

3.4.289 SPACLRC0—Offset 721D0h

Sprite A Color Correction 0 Register

Access Method

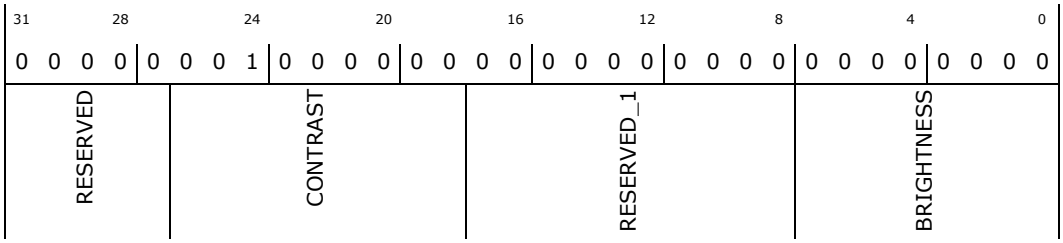
Type: Memory Mapped I/O Register (Size: 32 bits)

SPACLRC0: [GTTMMADR_LSB + 2BF20h] + 721D0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 01000000h



Bit Range	Default & Access	Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
26:18	001000000b RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0b RW	**RESERVED_1:** Reserved.
7:0	0b RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

3.4.290 SPACLRC1—Offset 721D4h

Sprite A Color Correction 1 Register

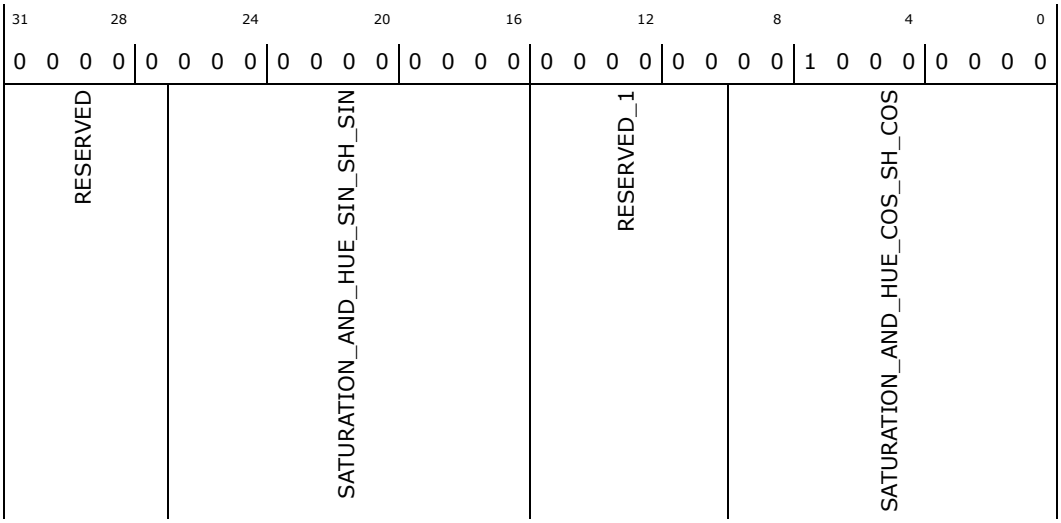
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPACLRC1: [GTTMMADR_LSB + 2BF20h] + 721D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:27	0b RW	**RESERVED:** Reserved.
26:16	0b RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0b RW	**RESERVED_1:** Reserved.
9:0	0010000000b RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

3.4.291 SPAGAMC5—Offset 721E0h

Sprite A Gamma Correction Registers

Access Method

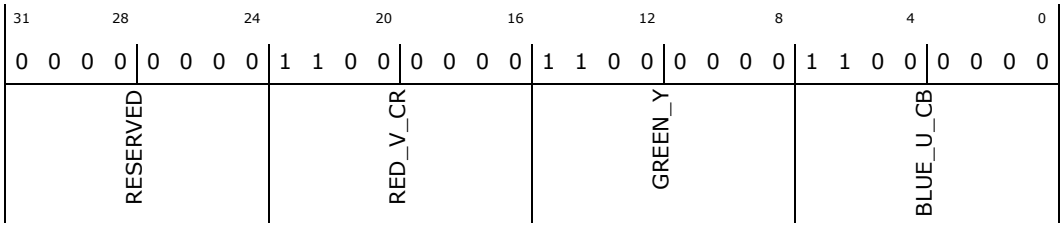
Type: Memory Mapped I/O Register (Size: 32 bits)

SPAGAMC5: [GTTMMADR_LSB + 2BF20h] + 721E0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00C0C0C0h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved
23:16	11000000b RW	**RED_V_CR:** gamma correction mapping Red to cr
15:8	11000000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	11000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.292 SPAGAMC4—Offset 721E4h

Sprite A Gamma Correction Registers

Access Method

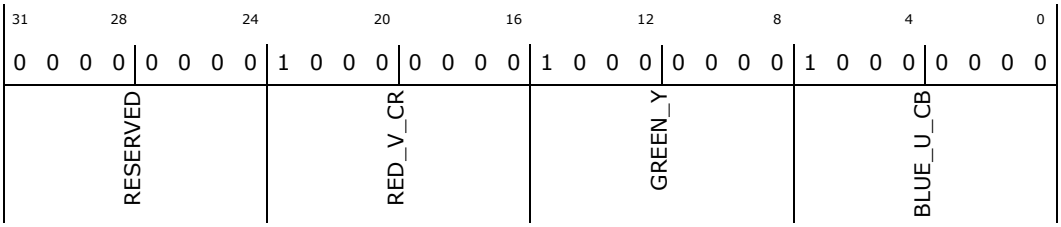
Type: Memory Mapped I/O Register (Size: 32 bits)

SPAGAMC4: [GTTMMADR_LSB + 2BF20h] + 721E4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00808080h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	10000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	10000000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	10000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.293 SPAGAMC3—Offset 721E8h

Sprite A Gamma Correction Registers

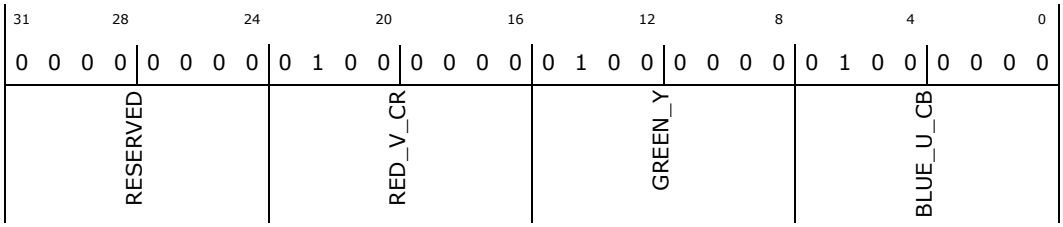
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPAGAMC3: [GTTMMADR_LSB + 2BF20h] + 721E8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00404040h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	01000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	01000000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	01000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.294 SPAGAMC2—Offset 721ECh

Sprite A Gamma Correction Registers

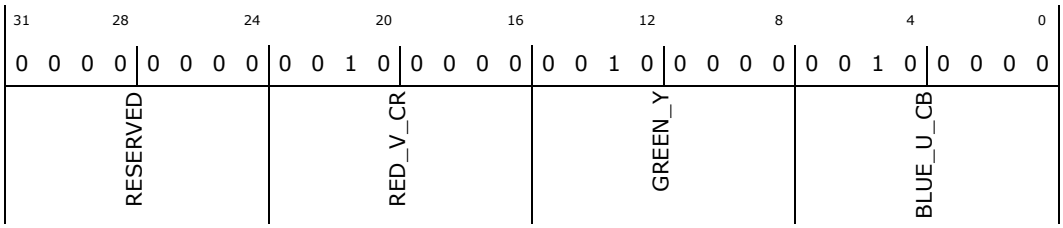
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPAGAMC2: [GTTMMADR_LSB + 2BF20h] + 721ECh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00202020h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
23:16	00100000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00100000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00100000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.295 SPAGAMC1—Offset 721F0h

Sprite A Gamma Correction Registers

Access Method

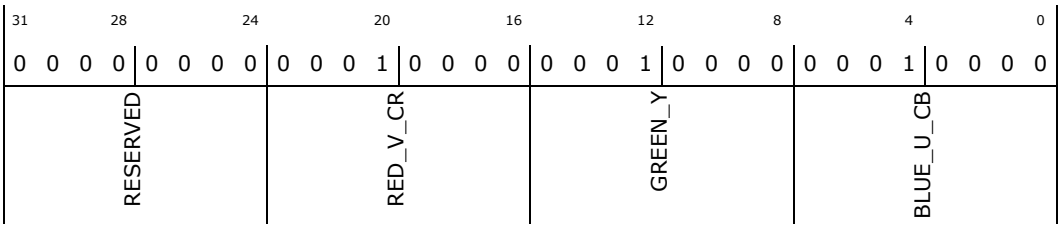
Type: Memory Mapped I/O Register (Size: 32 bits)

SPAGAMC1: [GTTMMADR_LSB + 2BF20h] + 721F0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00101010h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	00010000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00010000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00010000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.296 SPAGAMC0—Offset 721F4h

Sprite A Gamma Correction Registers

Access Method

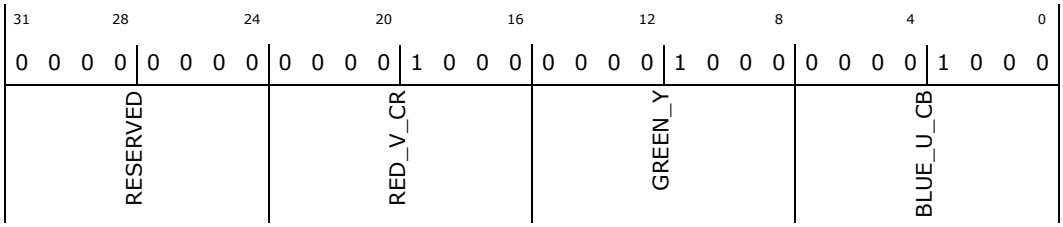
Type: Memory Mapped I/O Register (Size: 32 bits)

SPAGAMC0: [GTTMMADR_LSB + 2BF20h] + 721F4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00080808h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	00001000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00001000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00001000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.297 SPBCNTR—Offset 72280h

Sprite B Control Register

Access Method

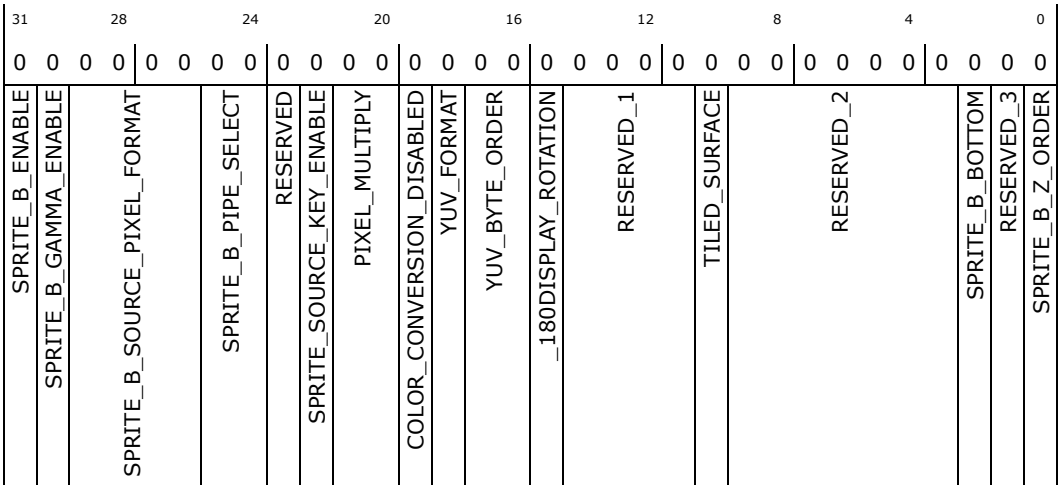
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBCNTR: [GTTMMADR_LSB + 2BF20h] + 72280h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**SPRITE_B_ENABLE:** This bit will enable or disable the Sprite B. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0b RW	**SPRITE_B_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite B data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite B logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite B pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite B pixel data is gamma corrected in the pipe gamma correction logic
29:26	0b RW	**SPRITE_B_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite B. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0b RW	**SPRITE_B_PIPE_SELECT:** Sprite B always ties to Pipe A. Reserved

Bit Range	Default & Access	Description
23	0b RW	**RESERVED:** Reserved.
22	0b RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite B pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite B pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	0b RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0b RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0b RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0b RW	**RESERVED_1:** Reserved.
10	0b RW	**TILED_SURFACE:** This bit indicates that the Sprite B surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite B surface uses linear memory 1 = Sprite B surface uses X-tiled memory
9:3	0b RW	**RESERVED_2:** Write as zero
2	0b RW	**SPRITE_B_BOTTOM:** This bit will force the Sprite B plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite B Z order is determined by the other control bits 1 = Sprite B is forced to be on the bottom of the Z order.
1	0b RW	**RESERVED_3:** Reserved.

Bit Range	Default & Access	Description
0	0b RW	**SPRITE_B_Z_ORDER:** With Sprite A and B z-order, bottom control bits, Sprite B plane is placed in a specific z-order among other planes in pipe A. Display Pipe A Z-orders SA zorderSA bottomSB zorderSB bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PA SA SB CAPA in Black 1000PA SB SA CAPA in Black 0001SB PA SA CAuse src keying on SB 0011SB PA SA CAuse src keying on SB 1001SB SA PA CAuse src keying on SA 1011SB SA PA CAuse src keying on SA 0100SA PA SB CAuse src keying on SA 1100SA PA SB CAuse src keying on SA 0110SA SB PA CAuse src keying on SB 1110SA SB PA CAuse src keying on SB 0: Sprite B z-order is disabled 1: Sprite B z-order is enabled

3.4.298 SPBLINOFF—Offset 72284h

Sprite B Linear Offset Register

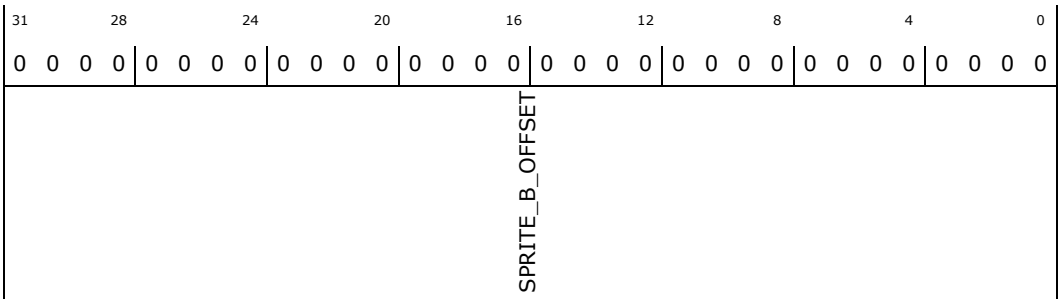
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPBLINOFF: [GTTMMADR_LSB + 2BF20h] + 72284h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**SPRITE_B_OFFSET:** This register provides the panning offset into the Sprite B plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

3.4.299 SPBSTRIDE—Offset 72288h

Sprite B Stride Register

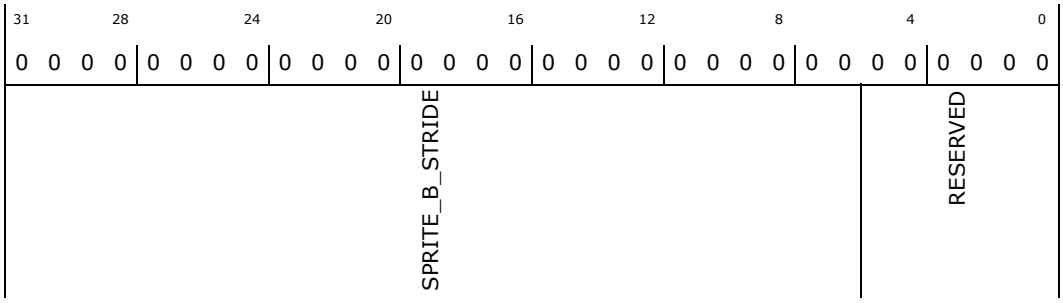
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPBSTRIDE: [GTTMMADR_LSB + 2BF20h] + 72288h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**SPRITE_B_STRIDE:** This is the stride for Sprite B in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0b RW	**RESERVED:** Reserved.

3.4.300 SPBPOS—Offset 7228Ch

Sprite B Position Register

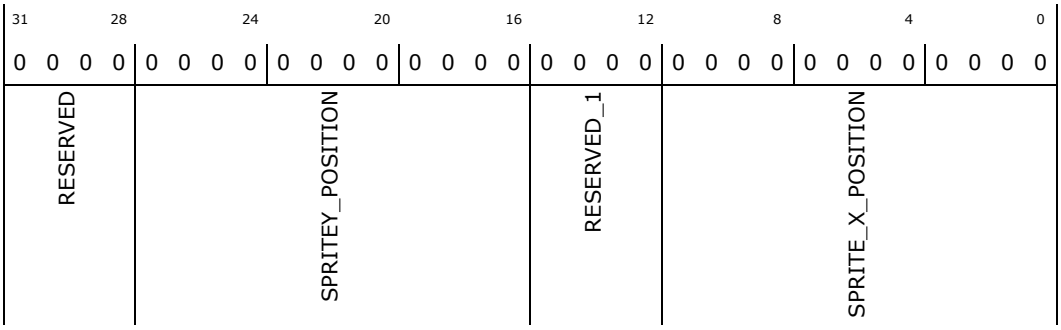
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPBPOS: [GTTMMADR_LSB + 2BF20h] + 7228Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

3.4.301 SPBSIZE—Offset 72290h

Sprite B Height and Width Register

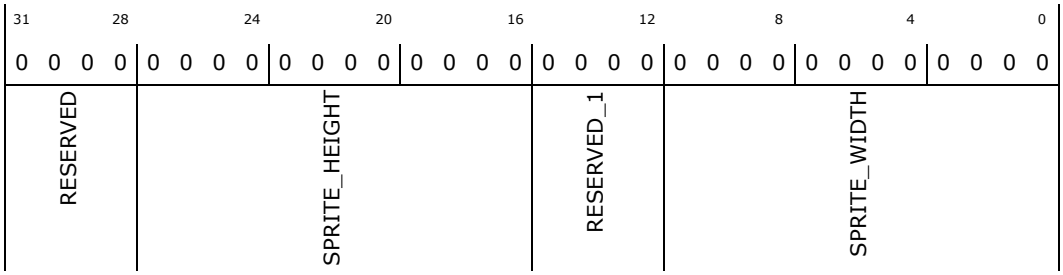
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPBSIZE: [GTTMMADR_LSB + 2BF20h] + 72290h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

3.4.302 SPBKEYMINVAL—Offset 72294h

Sprite B Color Key Min Value Register

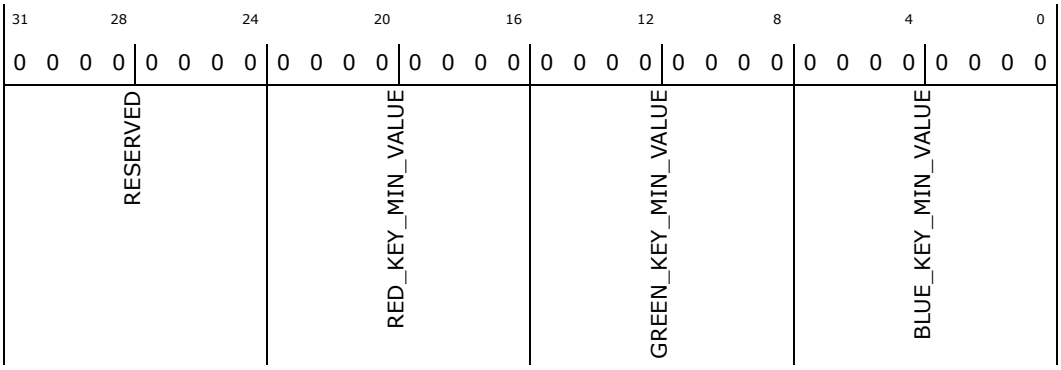
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPBKEYMINVAL: [GTTMMADR_LSB + 2BF20h] + 72294h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

3.4.303 SPBKEYMSK—Offset 72298h

Sprite B Color Key Mask Register

Access Method

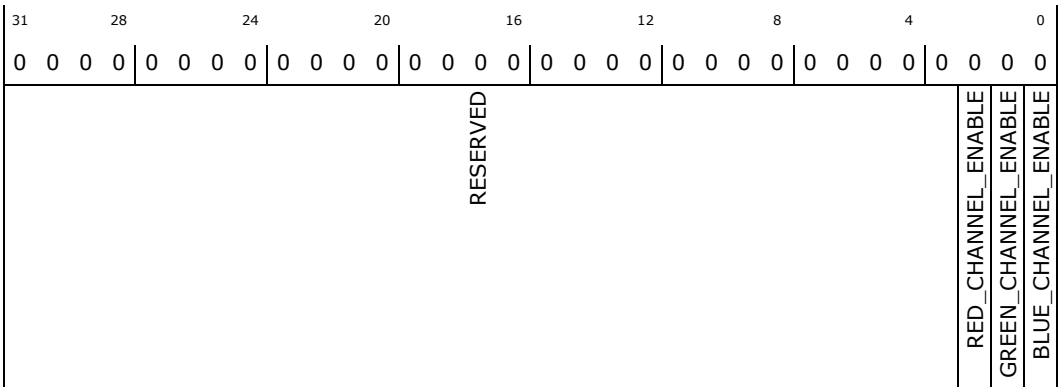
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBKEYMSK: [GTTMMADR_LSB + 2BF20h] + 72298h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**RESERVED:** Write as zero
2	0b RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0b RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0b RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

3.4.304 SPBSURF—Offset 7229Ch

Sprite B Surface Address Register

Access Method

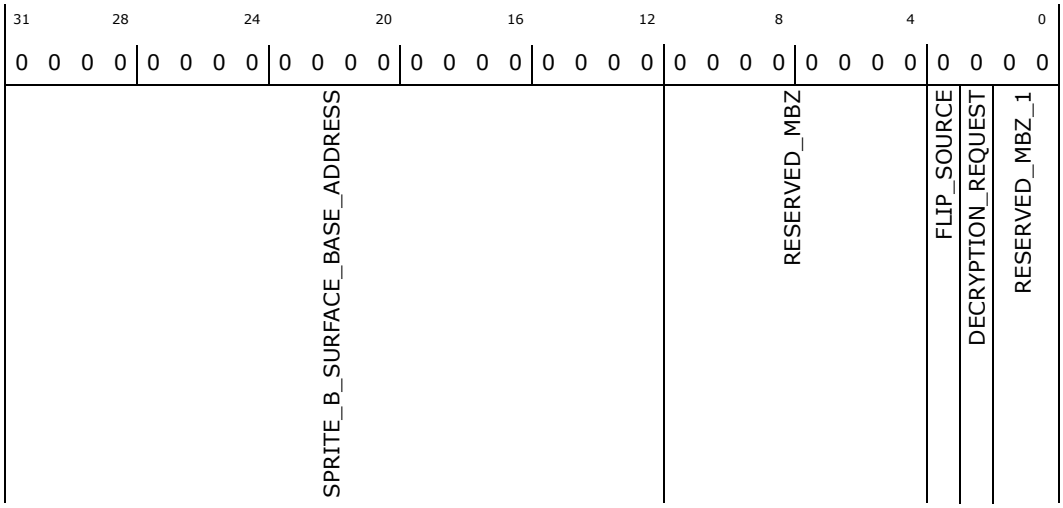
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBSURF: [GTTMMADR_LSB + 2BF20h] + 7229Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**SPRITE_B_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED_MBZ:** Reserved.
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decryption not requested All 1b Requested Decryption requested All
1:0	0b RW	**RESERVED_MBZ_1:** Reserved.

3.4.305 SPBKEYMAXVAL—Offset 722A0h

Sprite B Color Key Max Value Register

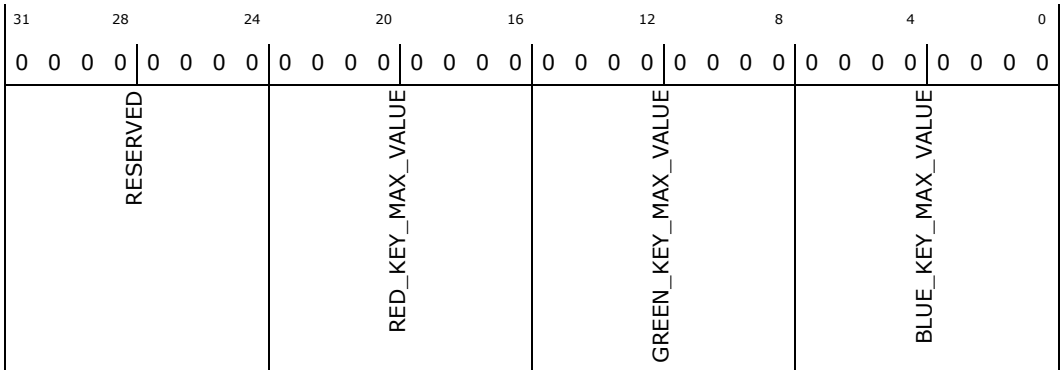
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPBKEYMAXVAL: [GTTMMADR_LSB + 2BF20h] + 722A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

3.4.306 SPBTILEOFF—Offset 722A4h

Sprite B Tiled Offset Register

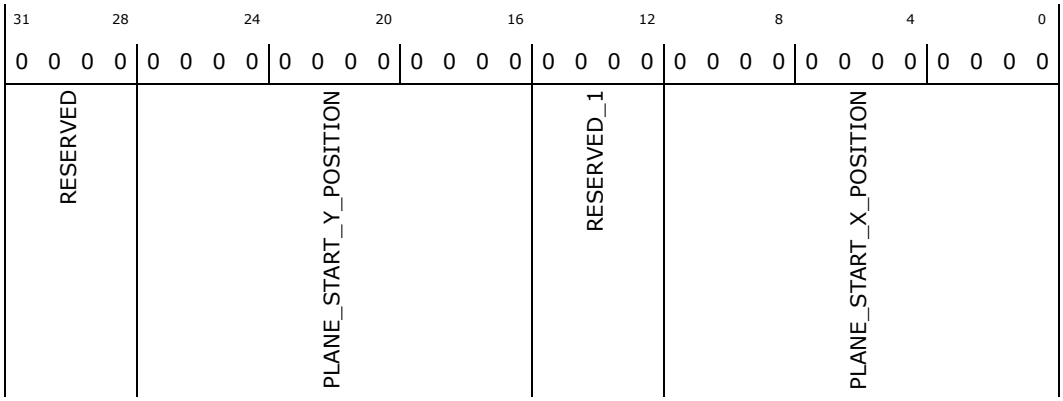
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPBTILEOFF: [GTTMMADR_LSB + 2BF20h] + 722A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

3.4.307 SPBCONTALPHA—Offset 722A8h

Sprite B Constant Alpha Register

Access Method

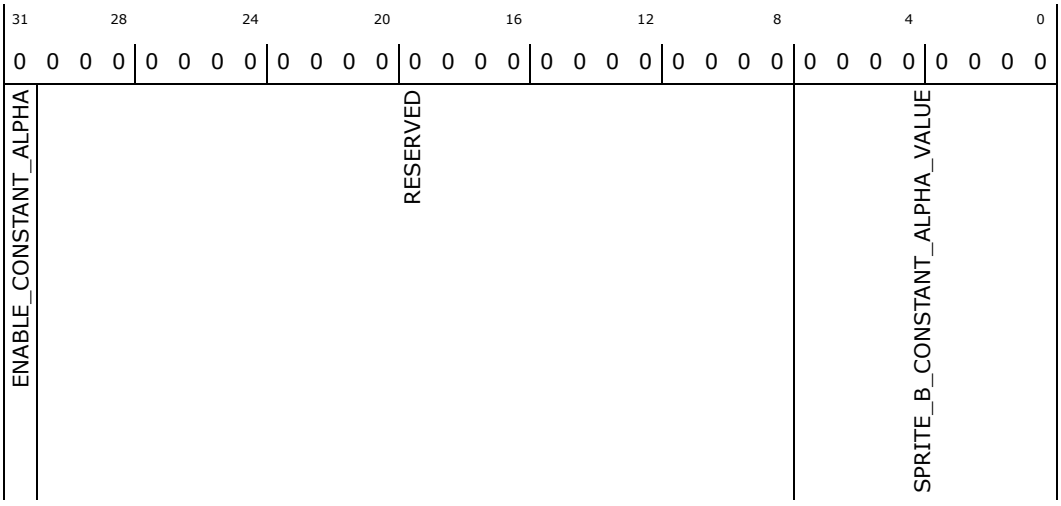
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBCONTALPHA: [GTTMMADR_LSB + 2BF20h] + 722A8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**ENABLE_CONSTANT_ALPHA:** Sprite B Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite B Sprite Constant Alpha is disabled 1 Sprite B Sprite Constant Alpha is enabled
30:8	0b RW	**RESERVED:** : MBZ
7:0	0b RW	**SPRITE_B_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

3.4.308 SPBLIVESURF—Offset 722ACh

Sprite B Live Surface Address Register

Access Method

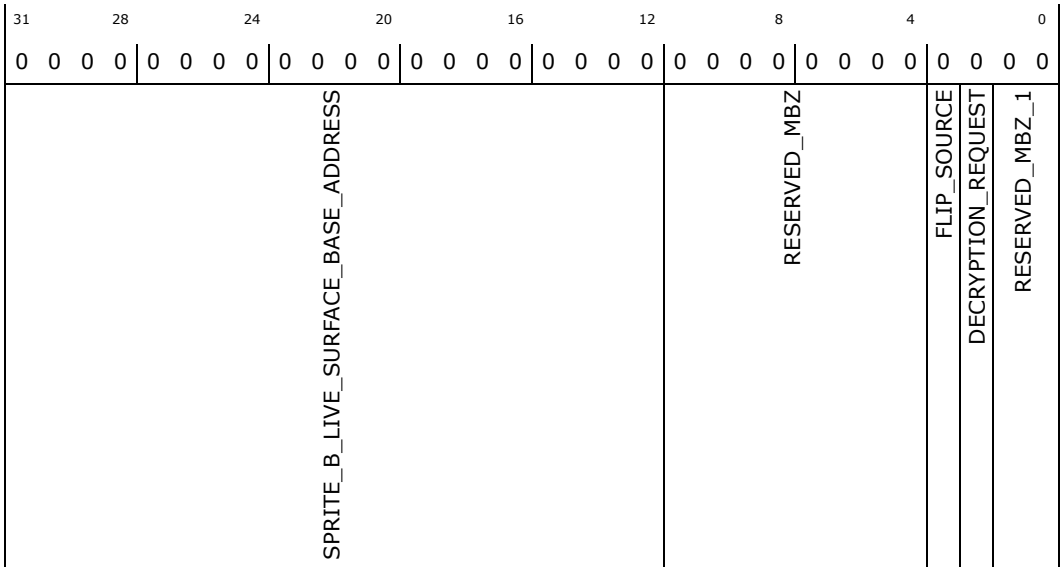
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBLIVESURF: [GTTMMADR_LSB + 2BF20h] + 722ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**SPRITE_B_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite B plane.

Bit Range	Default & Access	Description
11:4	0b RO	**RESERVED_MBZ:** Reserved.
3	0b RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decryption not requested All 1b Requested Decryption requested All
1:0	0b RO	**RESERVED_MBZ_1:** Reserved.

3.4.309 SPBCLRC0—Offset 722D0h

Sprite B Color Correction 0 Register

Access Method

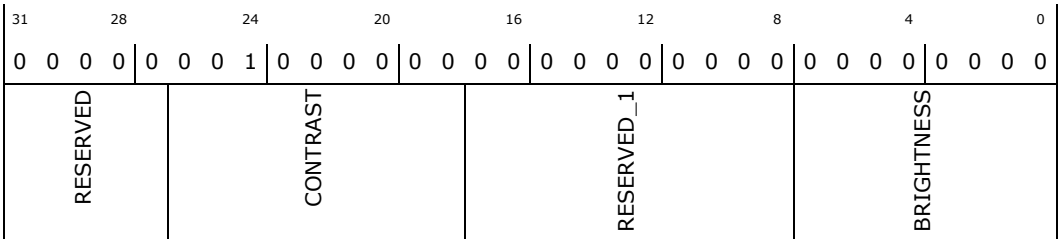
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBCLRC0: [GTTMMADR_LSB + 2BF20h] + 722D0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 01000000h



Bit Range	Default & Access	Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
26:18	001000000b RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0b RW	**RESERVED_1:** Reserved.
7:0	0b RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

3.4.310 SPBCLRC1—Offset 722D4h

Sprite B Color Correction 1 Register

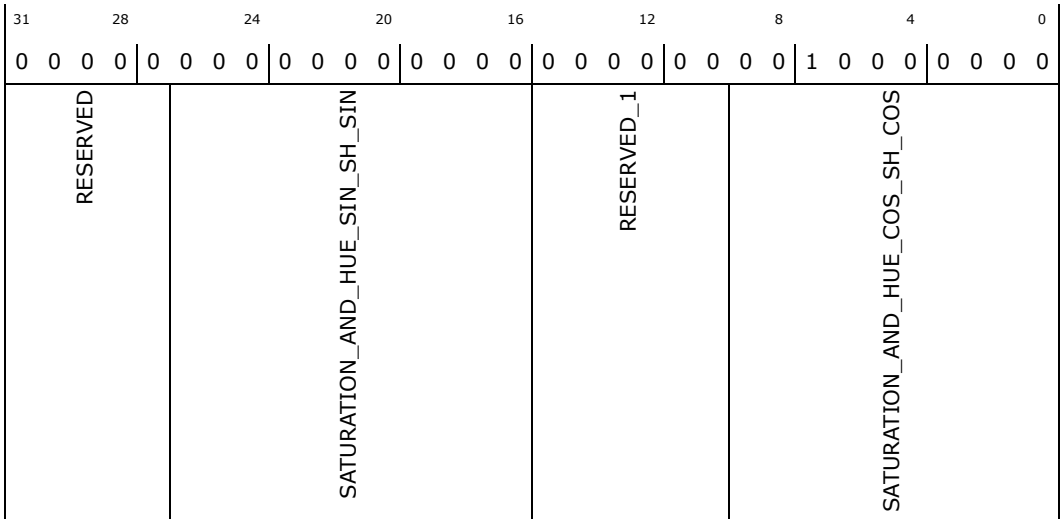
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPBCLRC1: [GTTMMADR_LSB + 2BF20h] + 722D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:27	0b RW	**RESERVED:** Reserved.
26:16	0b RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0b RW	**RESERVED_1:** Reserved.
9:0	0010000000b RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

3.4.311 SPBGAMC5—Offset 722E0h

Sprite B Gamma Correction Registers

Access Method

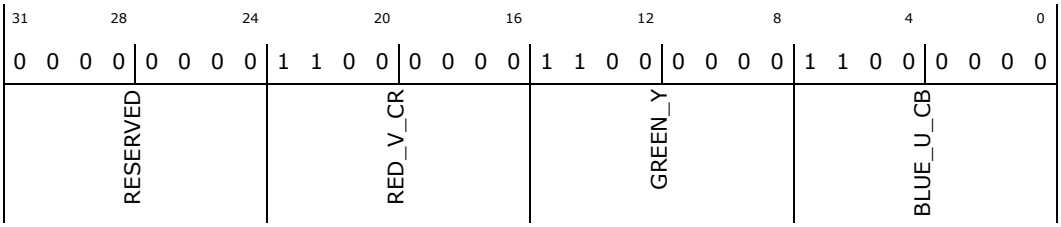
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBGAMC5: [GTTMMADR_LSB + 2BF20h] + 722E0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00C0C0C0h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	11000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	11000000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	11000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.312 SPBGAMC4—Offset 722E4h

Sprite B Gamma Correction Registers

Access Method

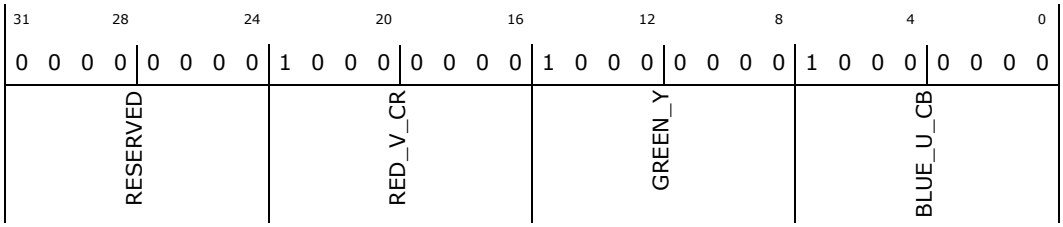
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBGAMC4: [GTTMMADR_LSB + 2BF20h] + 722E4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00808080h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	10000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	10000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	10000000b RW	**BLUE_U_CB:** gamma correction mapping CB

3.4.313 SPBGAMC3—Offset 722E8h

Sprite B Gamma Correction Registers

Access Method

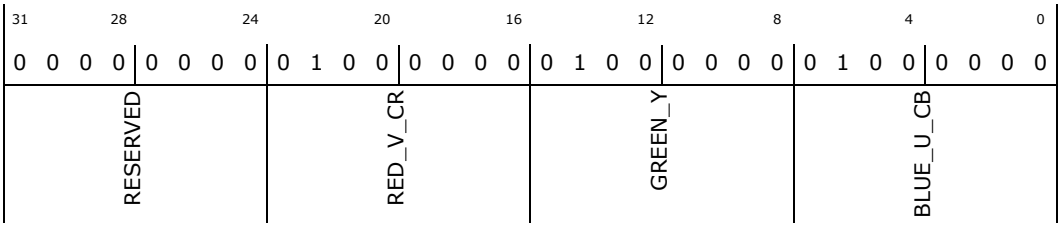
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBGAMC3: [GTTMMADR_LSB + 2BF20h] + 722E8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00404040h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	01000000b RW	**RED_V_CR:** gamma correction mapping red to CR
15:8	01000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	01000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.314 SPBGAMC2—Offset 722ECh

Sprite B Gamma Correction Registers

Access Method

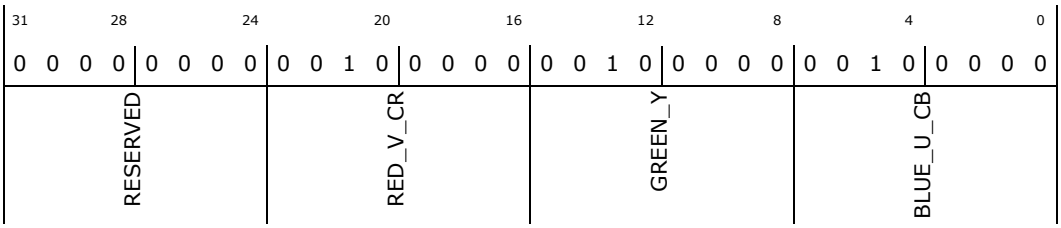
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBGAMC2: [GTTMMADR_LSB + 2BF20h] + 722ECh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00202020h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved

Bit Range	Default & Access	Description
23:16	00100000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00100000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00100000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

3.4.315 SPBGAMC1—Offset 722F0h

Sprite B Gamma Correction Registers

Access Method

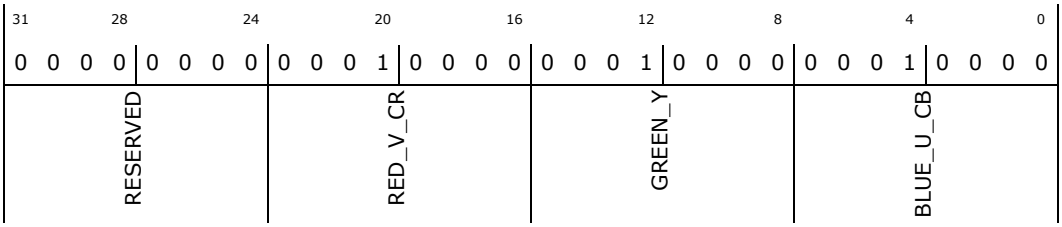
Type: Memory Mapped I/O Register (Size: 32 bits)

SPBGAMC1: [GTTMMADR_LSB + 2BF20h] + 722F0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00101010h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	00010000b RW	**RED_V_CR:** gamma correction mapping red to CR
15:8	00010000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00010000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

3.4.316 SPBGAMC0—Offset 722F4h

Sprite B Gamma Correction Registers

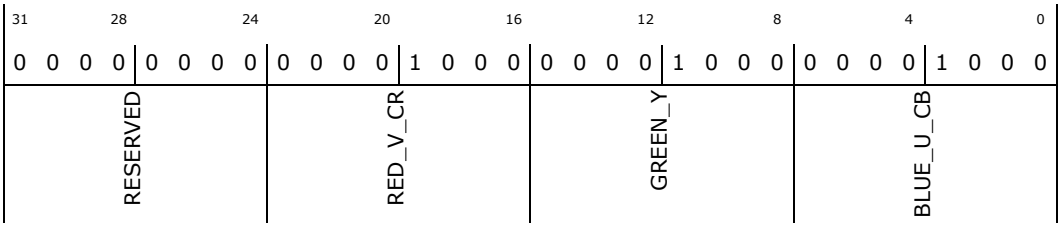
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPBGAMC0: [GTTMMADR_LSB + 2BF20h] + 722F4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00080808h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	00001000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00001000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00001000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

3.4.317 SPCCNTR—Offset 72380h

Sprite C Control Register

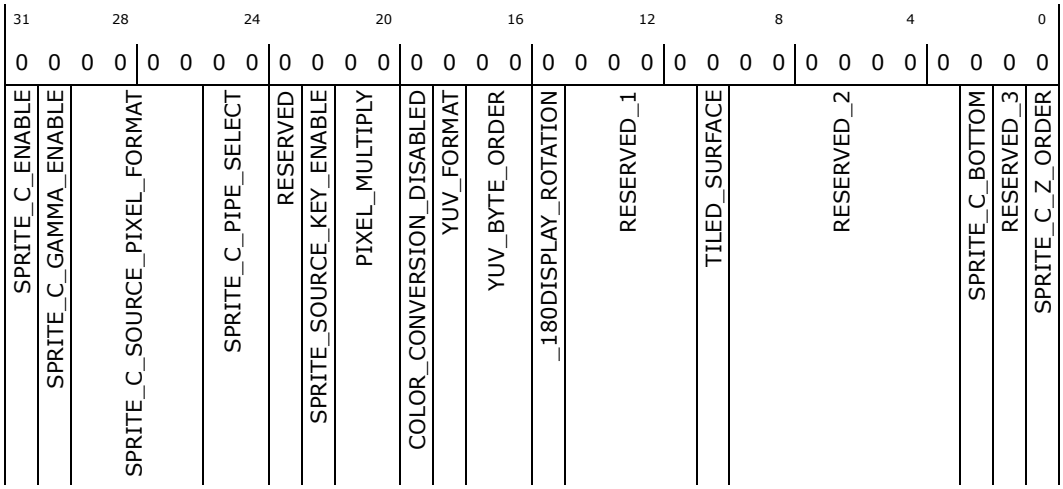
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

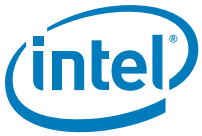
SPCCNTR: [GTTMMADR_LSB + 2BF20h] + 72380h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**SPRITE_C_ENABLE:** This bit will enable or disable the Sprite C. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0b RW	**SPRITE_C_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite C data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite C logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite C pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite C pixel data is gamma corrected in the pipe gamma correction logic
29:26	0b RW	**SPRITE_C_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite C. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0b RW	**SPRITE_C_PIPE_SELECT:** Sprite C always ties to Pipe B Reserved.



Bit Range	Default & Access	Description
23	0b RW	**RESERVED:** Reserved.
22	0b RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite C pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite C pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	0b RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0b RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0b RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0b RW	**RESERVED_1:** Reserved.
10	0b RW	**TILED_SURFACE:** This bit indicates that the Sprite C surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite C surface uses linear memory 1 = Sprite C surface uses X-tiled memory
9:3	0b RW	**RESERVED_2:** Write as zero
2	0b RW	**SPRITE_C_BOTTOM:** This bit will force the Sprite C plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite C Z order is determined by the other control bits 1 = Sprite C is forced to be on the bottom of the Z order.
1	0b RW	**RESERVED_3:** Reserved.

Bit Range	Default & Access	Description
0	0b RW	**SPRITE_C_Z_ORDER:** With Sprite C and D z-order, bottom control bits, Sprite C plane is placed in a specific z-order among other planes in pipe B. Display Pipe B Z-orders SC zorderSC bottomSD zorderSD bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PB SC SD CBPB in Black 1000PB SD SC CBPB in Black 0001SD PB SC CBuse src keying on SD 0011SD PB SC CBuse src keying on SD 1001SD SC PB CBuse src keying on SC 1011SD SC PB CBuse src keying on SC 0100SC PB SD CBuse src keying on SC 1100SC PB SD CBuse src keying on SC 0110SC SD PB CBuse src keying on SD 1110SC SD PB CBuse src keying on SD 0101Not Allowed 0111Not Allowed 1101Not Allowed 1111Not Allowed 1010Not Allowed 1011Not Allowed 0: Sprite C z-order is disabled 1: Sprite C z-order is enabled

3.4.318 SPCLINOFF—Offset 72384h

Sprite C Linear Offset Register

Access Method

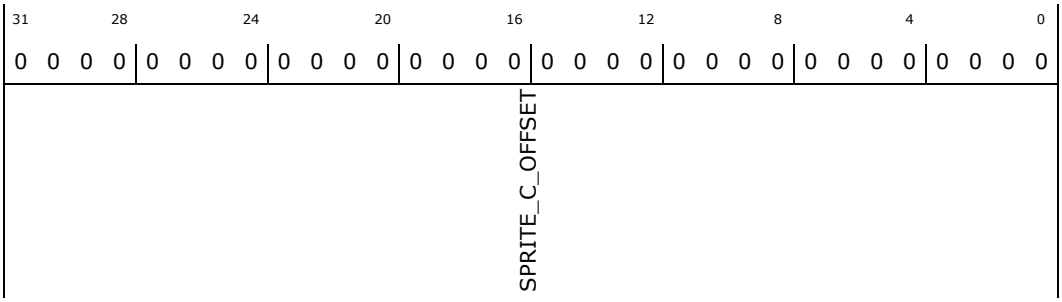
Type: Memory Mapped I/O Register (Size: 32 bits)

SPCLINOFF: [GTTMMADR_LSB + 2BF20h] + 72384h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**SPRITE_C_OFFSET:** This register provides the panning offset into the Sprite C plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

3.4.319 SPCSTRIDE—Offset 72388h

Sprite C Stride Register

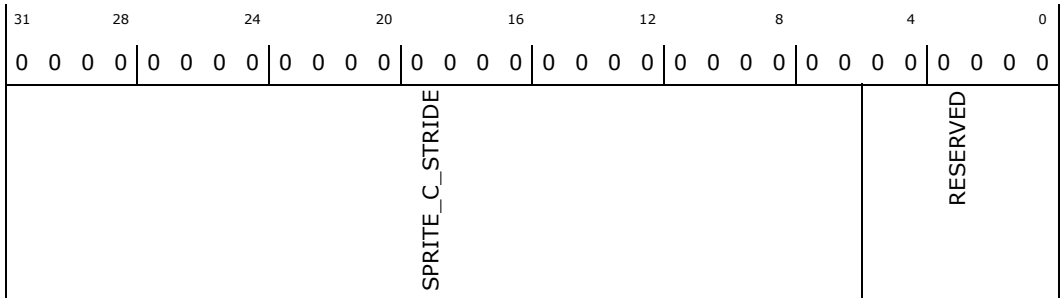
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCSTRIDE: [GTTMMADR_LSB + 2BF20h] + 72388h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**SPRITE_C_STRIDE:** This is the stride for Sprite C in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0b RW	**RESERVED:** Reserved.

3.4.320 SPCPOS—Offset 7238Ch

Sprite C Position Register

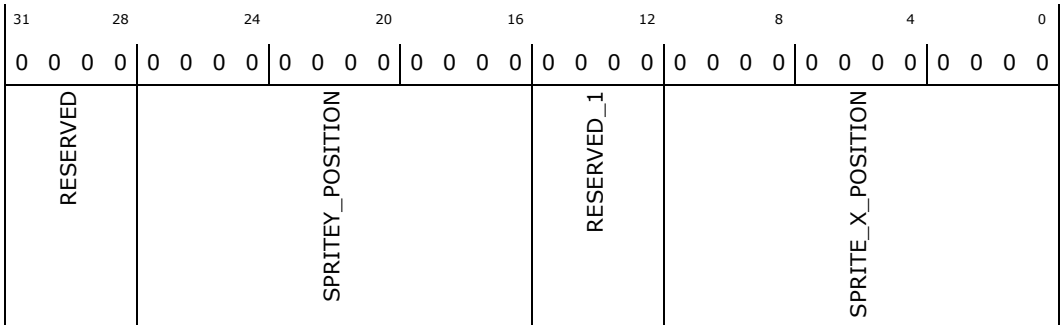
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCPOS: [GTTMMADR_LSB + 2BF20h] + 7238Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

3.4.321 SPCSIZE—Offset 72390h

Sprite C Height and Width Register

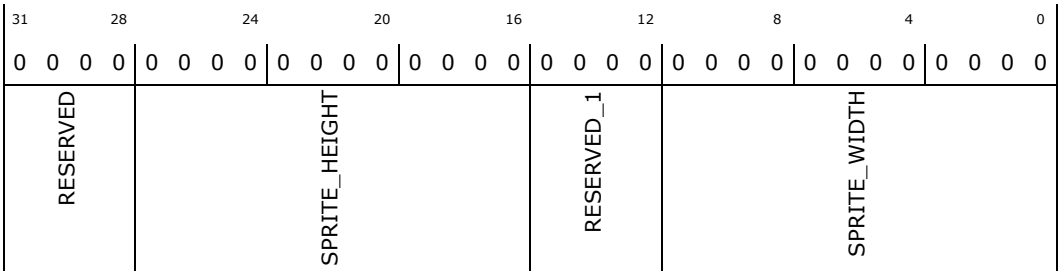
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCSIZE: [GTTMMADR_LSB + 2BF20h] + 72390h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

3.4.322 SPCKEYMINVAL—Offset 72394h

Sprite C Color Key Min Value Register

Access Method

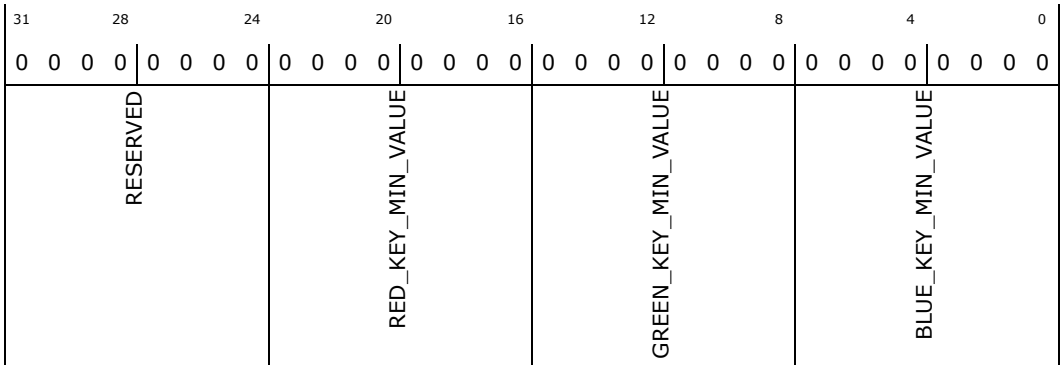
Type: Memory Mapped I/O Register (Size: 32 bits)

SPCKEYMINVAL: [GTTMMADR_LSB + 2BF20h] + 72394h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

3.4.323 SPCKEYMSK—Offset 72398h

Sprite C Color Key Mask Register

Access Method

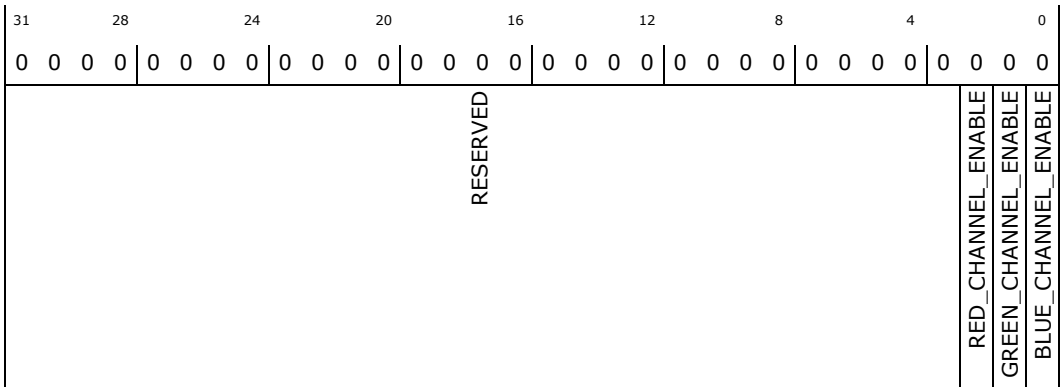
Type: Memory Mapped I/O Register (Size: 32 bits)

SPCKEYMSK: [GTTMMADR_LSB + 2BF20h] + 72398h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**RESERVED:** Write as zero
2	0b RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0b RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0b RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

3.4.324 SPCSURF—Offset 7239Ch

Sprite C Surface Address Register

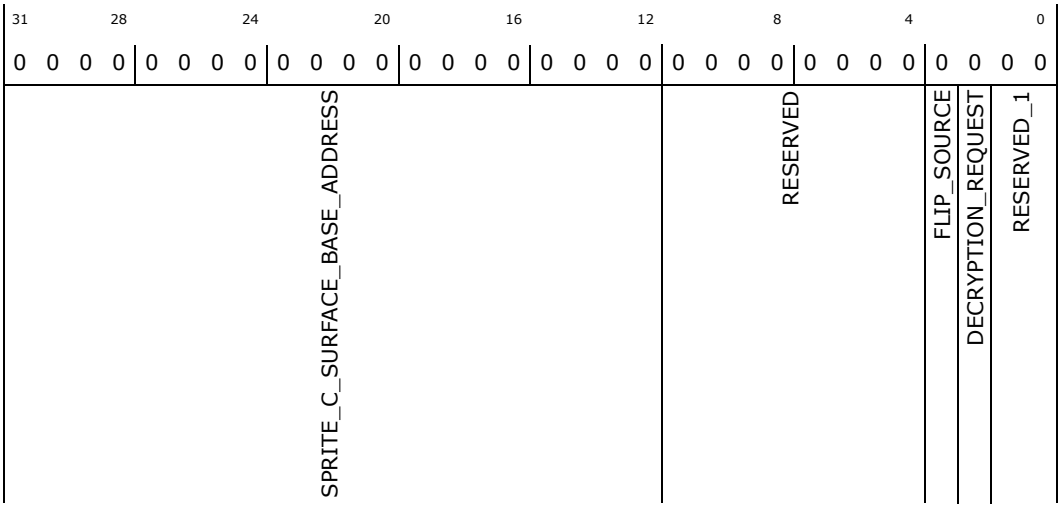
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCSURF: [GTTMMADR_LSB + 2BF20h] + 7239Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**SPRITE_C_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED:** : MBZ
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decryption not requested All 1b Requested Decryption requested All
1:0	0b RW	**RESERVED_1:** : MBZ

3.4.325 SPCKEYMAXVAL—Offset 723A0h

Sprite C Color Key Max Value Register

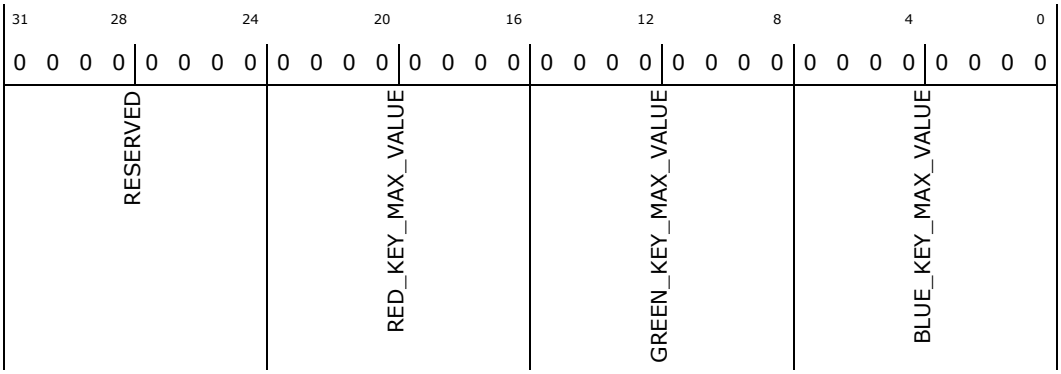
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCKEYMAXVAL: [GTTMMADR_LSB + 2BF20h] + 723A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the Sprite Clue/Cb channel.

3.4.326 SPCTILEOFF—Offset 723A4h

Sprite C Tiled Offset Register

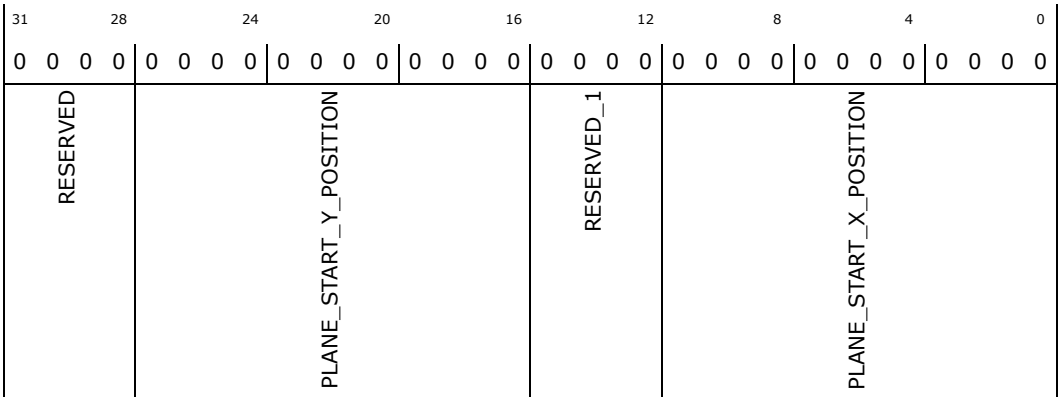
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCTILEOFF: [GTTMMADR_LSB + 2BF20h] + 723A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

3.4.327 SPCCONTALPHA—Offset 723A8h

Sprite C Constant Alpha Register

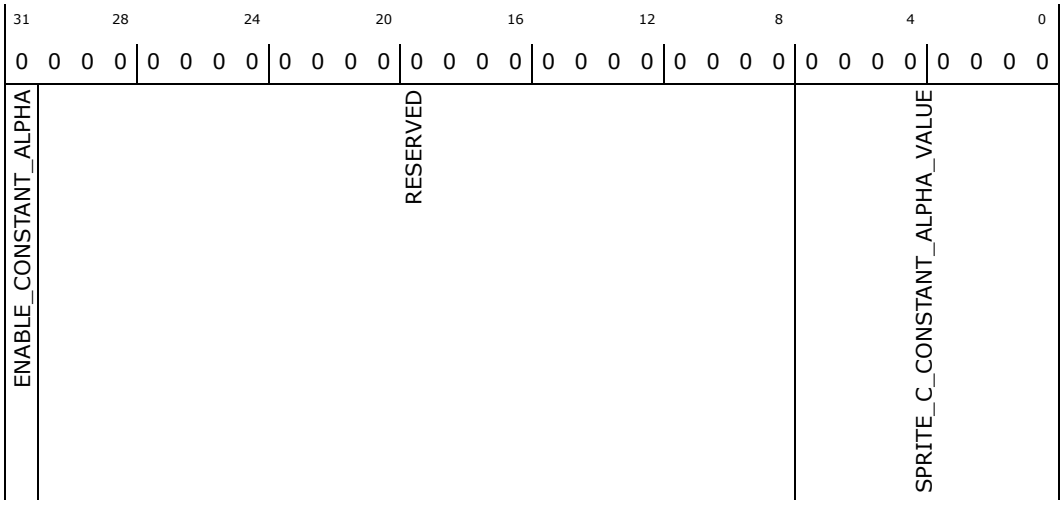
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCCONTALPHA: [GTTMMADR_LSB + 2BF20h] + 723A8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**ENABLE_CONSTANT_ALPHA:** Sprite C Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite C Sprite Constant Alpha is disabled 1 Sprite C Sprite Constant Alpha is enabled
30:8	0b RW	**RESERVED:** : MBZ
7:0	0b RW	**SPRITE_C_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

3.4.328 SPCLIVESURF—Offset 723ACh

Sprite C Live Surface Address Register

Access Method

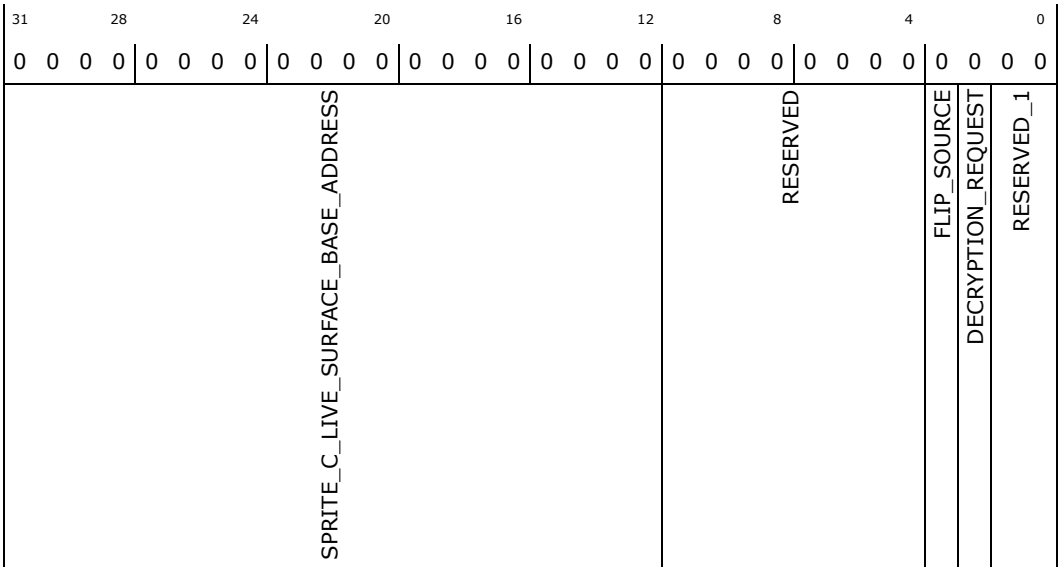
Type: Memory Mapped I/O Register (Size: 32 bits)

SPCLIVESURF: [GTTMMADR_LSB + 2BF20h] + 723ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**SPRITE_C_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite C.

Bit Range	Default & Access	Description
11:4	0b RO	**RESERVED:** : MBZ
3	0b RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decryption not requested All 1b Requested Decryption requested All
1:0	0b RO	**RESERVED_1:** : MBZ

3.4.329 SPCCLRC0—Offset 723D0h

Sprite C Color Correction 0 Register

Access Method

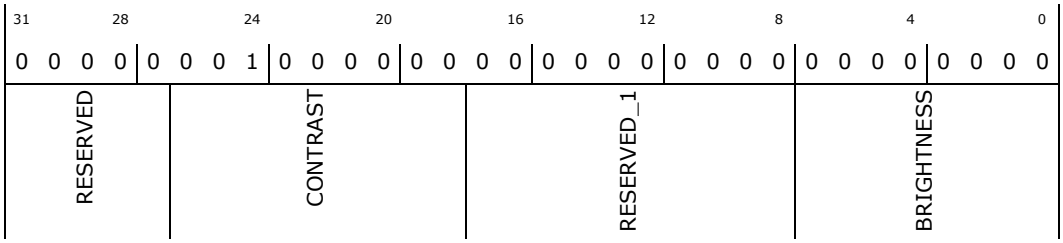
Type: Memory Mapped I/O Register (Size: 32 bits)

SPCCLRC0: [GTTMMADR_LSB + 2BF20h] + 723D0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 01000000h



Bit Range	Default & Access	Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
26:18	001000000b RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0b RW	**RESERVED_1:** Reserved.
7:0	0b RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

3.4.330 SPCCLRC1—Offset 723D4h

Sprite C Color Correction 1 Register

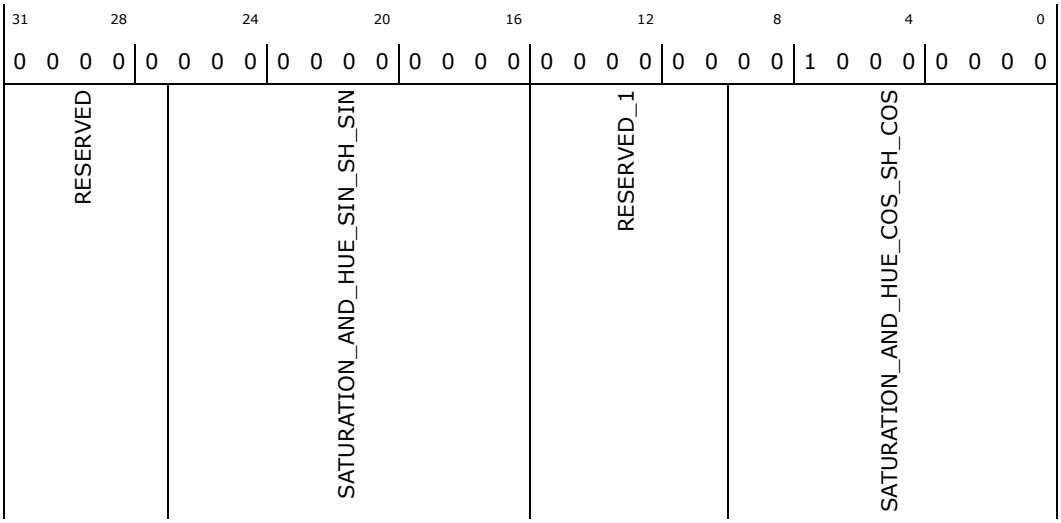
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCCLRC1: [GTTMMADR_LSB + 2BF20h] + 723D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:27	0b RW	**RESERVED:** Reserved.
26:16	0b RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0b RW	**RESERVED_1:** Reserved.
9:0	0010000000b RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

3.4.331 SPCGAMC5—Offset 723E0h

Sprite C Gamma Correction Registers

Access Method

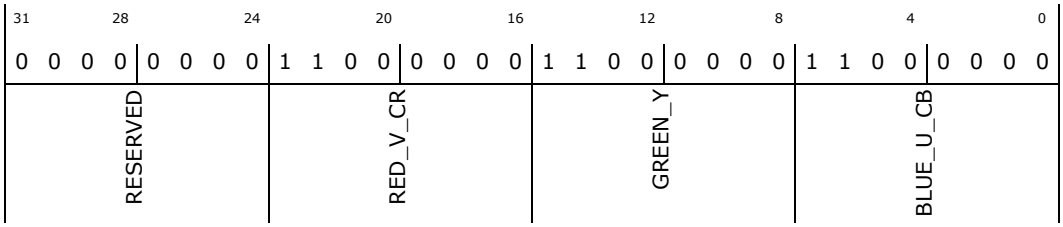
Type: Memory Mapped I/O Register (Size: 32 bits)

SPCGAMC5: [GTTMMADR_LSB + 2BF20h] + 723E0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00C0C0C0h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	11000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	11000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	11000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.332 SPCGAMC4—Offset 723E4h

Sprite C Gamma Correction Registers

Access Method

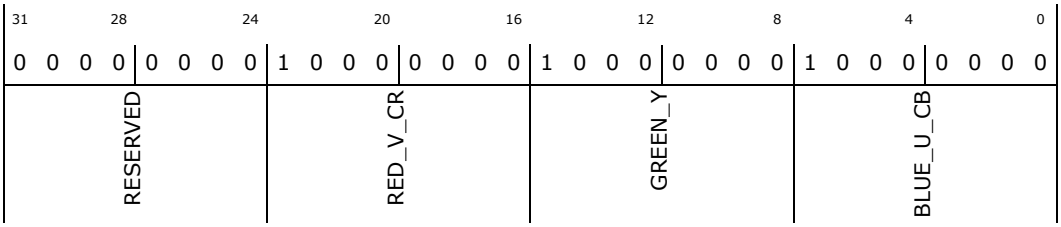
Type: Memory Mapped I/O Register (Size: 32 bits)

SPCGAMC4: [GTTMMADR_LSB + 2BF20h] + 723E4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00808080h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	10000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	10000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	10000000b RW	**BLUE_U_CB:** gamma correction mapping CB

3.4.333 SPCGAMC3—Offset 723E8h

Sprite C Gamma Correction Registers

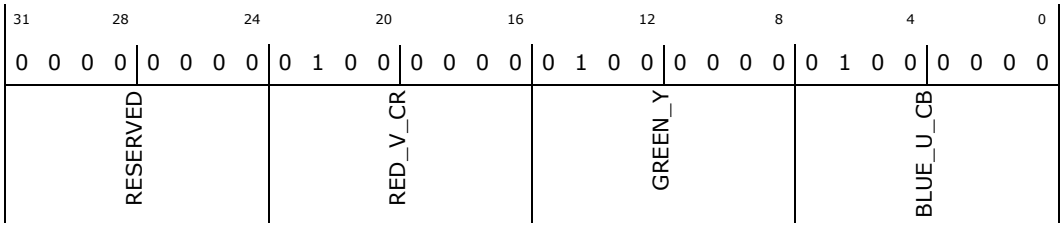
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCGAMC3: [GTTMMADR_LSB + 2BF20h] + 723E8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00404040h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	01000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	01000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	01000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.334 SPCGAMC2—Offset 723ECh

Sprite C Gamma Correction Registers

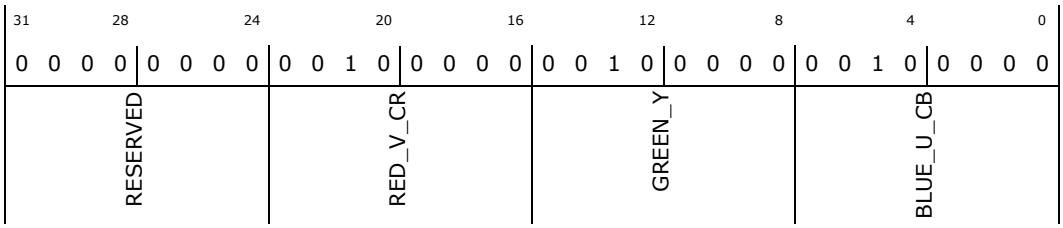
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCGAMC2: [GTTMMADR_LSB + 2BF20h] + 723ECh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00202020h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved

Bit Range	Default & Access	Description
23:16	00100000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00100000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00100000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.335 SPCGAMC1—Offset 723F0h

Sprite C Gamma Correction Registers

Access Method

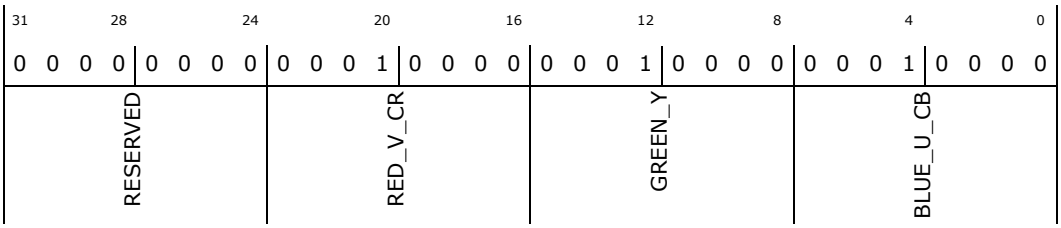
Type: Memory Mapped I/O Register (Size: 32 bits)

SPCGAMC1: [GTTMMADR_LSB + 2BF20h] + 723F0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00101010h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	00010000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00010000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	00010000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.336 SPCGAMC0—Offset 723F4h

Sprite C Gamma Correction Registers

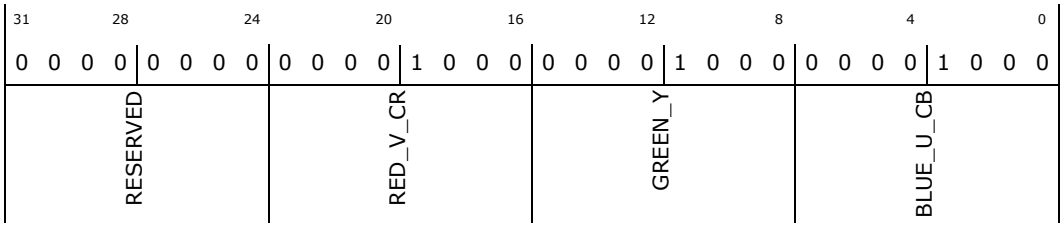
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPCGAMC0: [GTTMMADR_LSB + 2BF20h] + 723F4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00080808h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	00001000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00001000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	00001000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.337 SWF30—Offset 72414h

Software Flag Registers

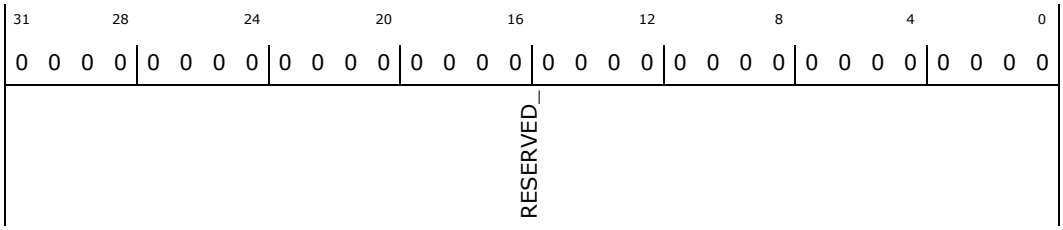
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF30: [GTTMMADR_LSB + 2BF20h] + 72414h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.338 SWF31—Offset 72418h

Software Flag Registers

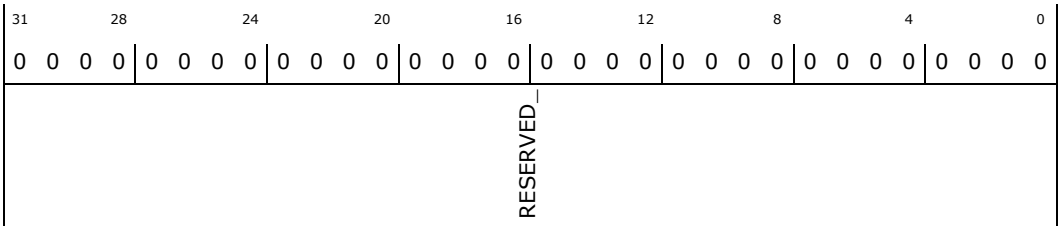
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF31: [GTTMMADR_LSB + 2BF20h] + 72418h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.339 SWF32—Offset 7241Ch

Software Flag Registers

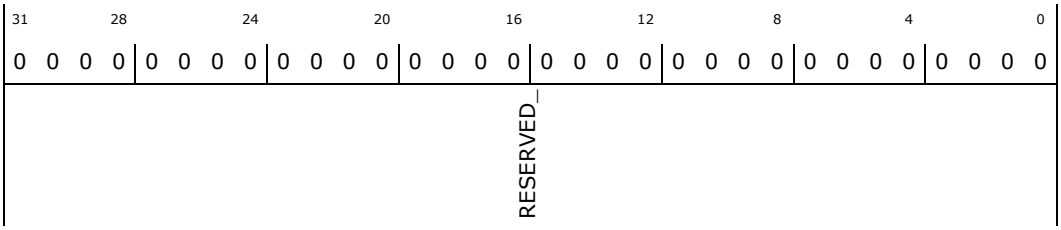
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SWF32: [GTTMMADR_LSB + 2BF20h] + 7241Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

3.4.340 SPDCNTR—Offset 72480h

Sprite D Control Register

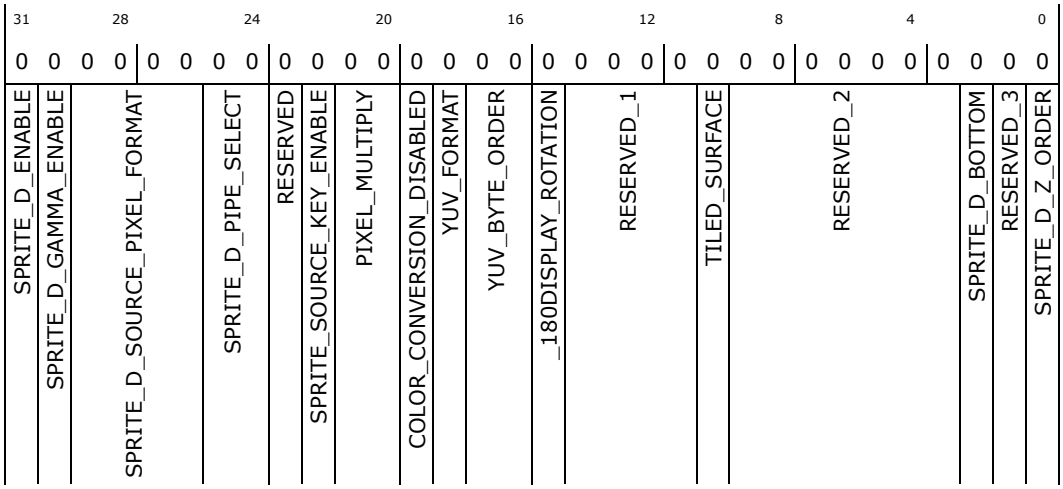
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDCNTR: [GTTMMADR_LSB + 2BF20h] + 72480h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**SPRITE_D_ENABLE:** This bit will enable or disable the Sprite D. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0b RW	**SPRITE_D_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite D data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite D logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite D pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite D pixel data is gamma corrected in the pipe gamma correction logic

Bit Range	Default & Access	Description
29:26	0b RW	**SPRITE_D_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite D. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0b RW	**SPRITE_D_PIPE_SELECT:** Sprite D always ties to Pipe B. Reserved.
23	0b RW	**RESERVED:** Reserved.
22	0b RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite D pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite D pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	0b RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0b RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0b RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0b RW	**RESERVED_1:** Reserved.

Bit Range	Default & Access	Description
10	0b RW	**TILED_SURFACE:** This bit indicates that the Sprite D surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite D surface uses linear memory 1 = Sprite D surface uses X-tiled memory
9:3	0b RW	**RESERVED_2:** Write as zero
2	0b RW	**SPRITE_D_BOTTOM:** This bit will force the Sprite D plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite D Z order is determined by the other control bits 1 = Sprite D is forced to be on the bottom of the Z order.
1	0b RW	**RESERVED_3:** Reserved.
0	0b RW	**SPRITE_D_Z_ORDER:** With Sprite C and D z-order, bottom control bits, Sprite D plane is placed in a specific z-order among other planes in pipe B. Display Pipe B Z-orders SC zorderSC bottomSD zorderSD bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PB SC SD CBPB in Black 1000PB SD SC CBPB in Black 0001SD PB SC CBuse src keying on SD 0011SD PB SC CBuse src keying on SD 1001SD SC PB CBuse src keying on SC 1011SD SC PB CBuse src keying on SC 0100SC PB SD CBuse src keying on SC 1100SC PB SD CBuse src keying on SC 0110SC SD PB CBuse src keying on SD 1110SC SD PB CBuse src keying on SD 0101Not Allowed 0111Not Allowed 1101Not Allowed 1111Not Allowed 1010Not Allowed 1011Not Allowed 0: Sprite D z-order is disabled 1: Sprite D z-order is enabled

3.4.341 SPDLINOFF—Offset 72484h

Sprite D Linear Offset Register

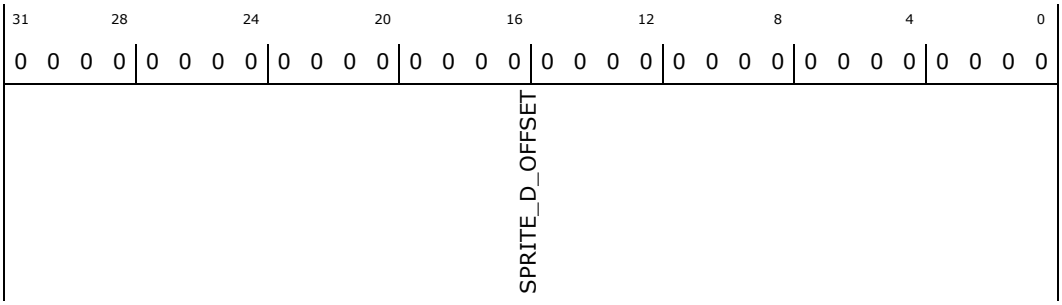
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDLINOFF: [GTTMMADR_LSB + 2BF20h] + 72484h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**SPRITE_D_OFFSET:** This register provides the panning offset into the Sprite D plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

3.4.342 SPDSTRIDE—Offset 72488h

Sprite D Stride Register

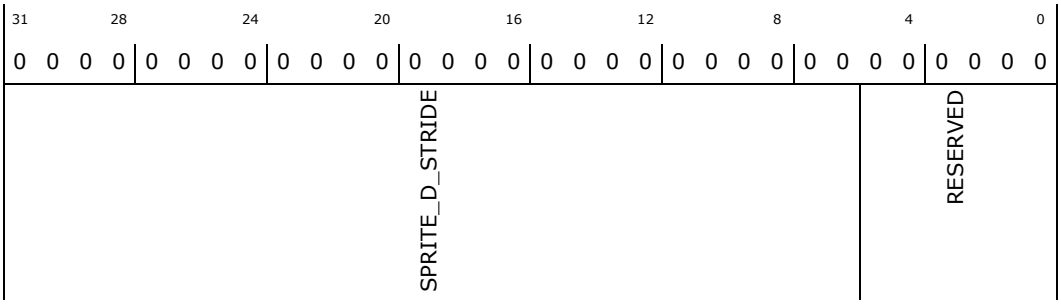
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDSTRIDE: [GTTMMADR_LSB + 2BF20h] + 72488h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RW	**SPRITE_D_STRIDE:** This is the stride for Sprite D in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0b RW	**RESERVED:** Reserved.

3.4.343 SPDPOS—Offset 7248Ch

Sprite D Position Register

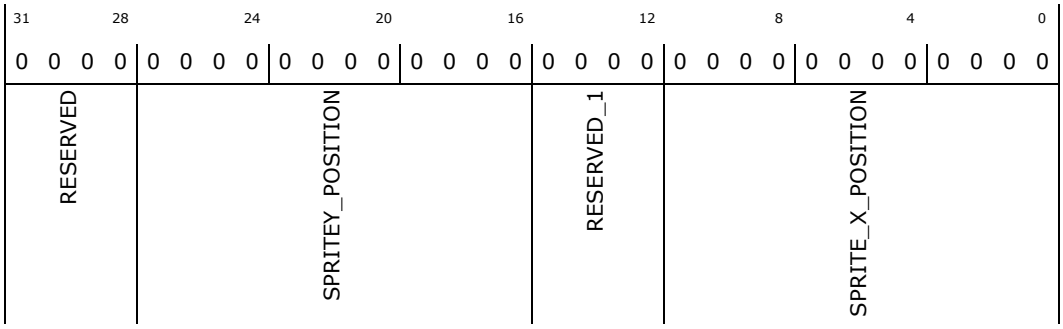
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDPOS: [GTTMMADR_LSB + 2BF20h] + 7248Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

3.4.344 SPDSIZE—Offset 72490h

Sprite D Height and Width Register

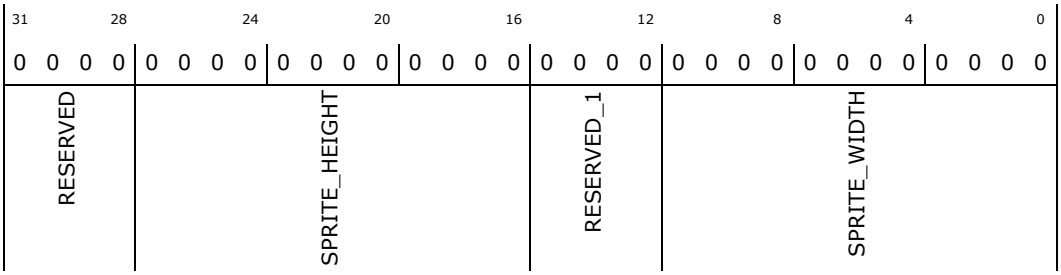
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDSIZE: [GTTMMADR_LSB + 2BF20h] + 72490h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

3.4.345 SPDKEYMINVAL—Offset 72494h

Sprite D Color Key Min Value Register

Access Method

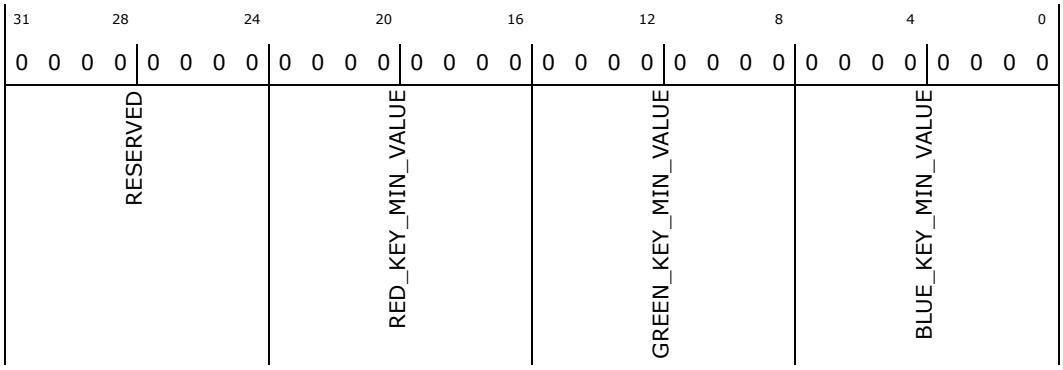
Type: Memory Mapped I/O Register (Size: 32 bits)

SPDKEYMINVAL: [GTTMMADR_LSB + 2BF20h] + 72494h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

3.4.346 SPDKEYMSK—Offset 72498h

Sprite D Color Key Mask Register

Access Method

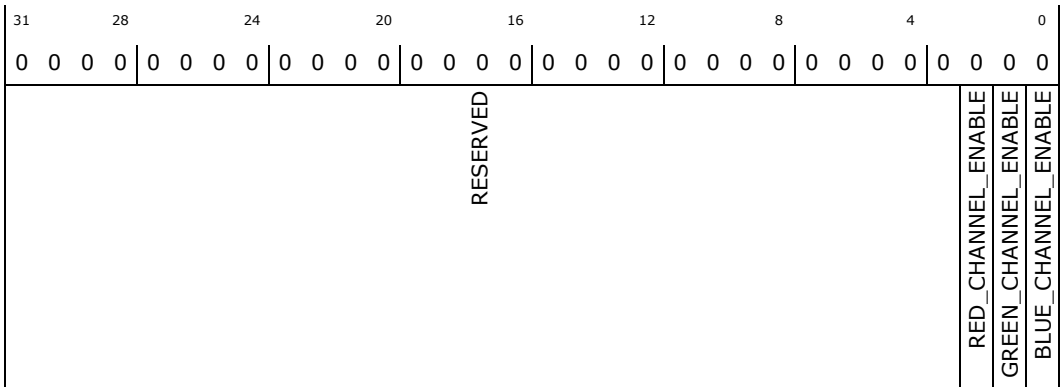
Type: Memory Mapped I/O Register (Size: 32 bits)

SPDKEYMSK: [GTTMMADR_LSB + 2BF20h] + 72498h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**RESERVED:** Write as zero
2	0b RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0b RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0b RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

3.4.347 SPDSURF—Offset 7249Ch

Sprite D Surface Address Register

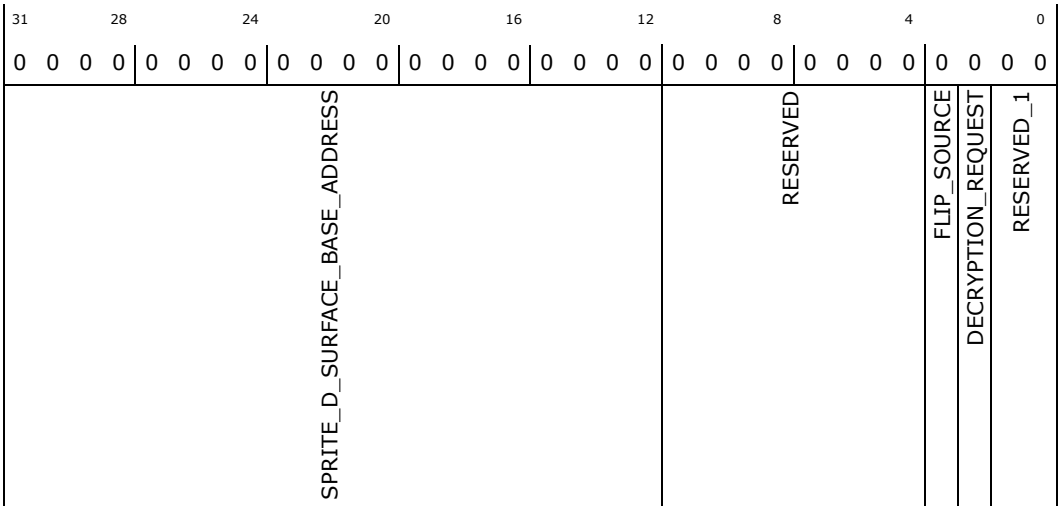
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDSURF: [GTTMMADR_LSB + 2BF20h] + 7249Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**SPRITE_D_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED:** : MBZ
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decryption not requested All 1b Requested Decryption requested All
1:0	0b RW	**RESERVED_1:** : MBZ

3.4.348 SPDKEYMAXVAL—Offset 724A0h

Sprite D Color Key Max Value Register

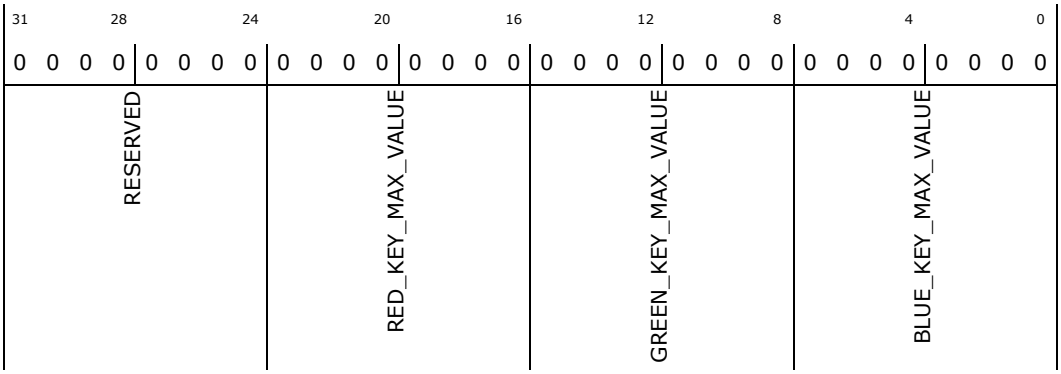
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDKEYMAXVAL: [GTTMMADR_LSB + 2BF20h] + 724A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the Sprite blue/Cb channel.

3.4.349 SPDTILEOFF—Offset 724A4h

Sprite D Tiled Offset Register

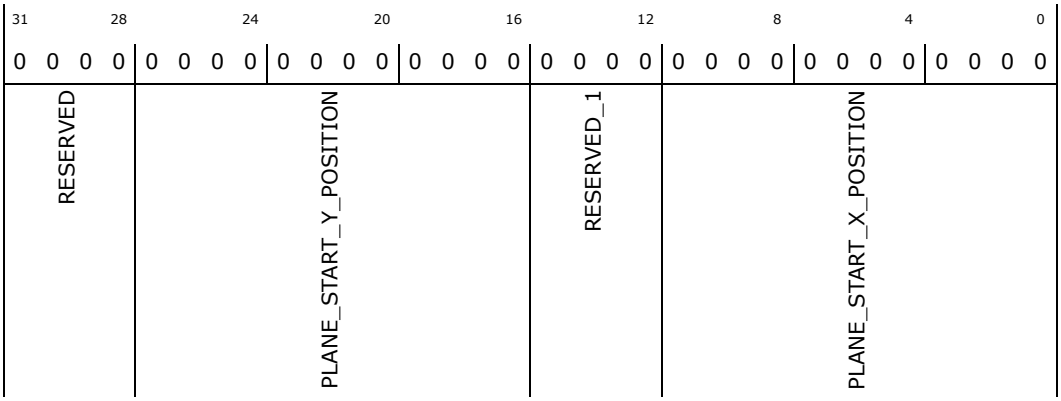
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDTILEOFF: [GTTMMADR_LSB + 2BF20h] + 724A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

3.4.350 SPDCONTALPHA—Offset 724A8h

Sprite D Constant Alpha Register

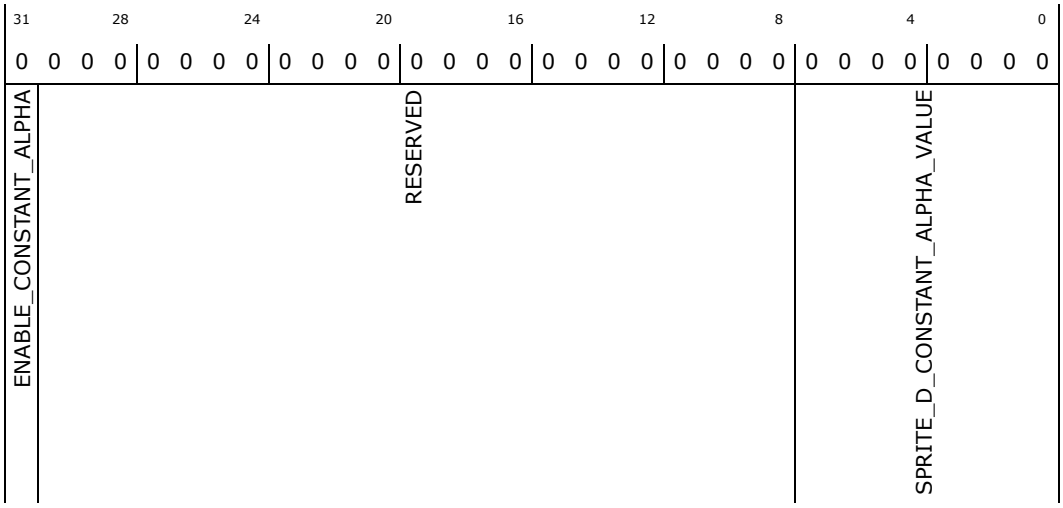
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDCONTALPHA: [GTTMMADR_LSB + 2BF20h] + 724A8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**ENABLE_CONSTANT_ALPHA:** Sprite D Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite D Constant Alpha is disabled 1 Sprite D Constant Alpha is enabled
30:8	0b RW	**RESERVED:** : MBZ
7:0	0b RW	**SPRITE_D_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

3.4.351 SPDLIVESURF—Offset 724ACh

Sprite D Live Surface Address Register

Access Method

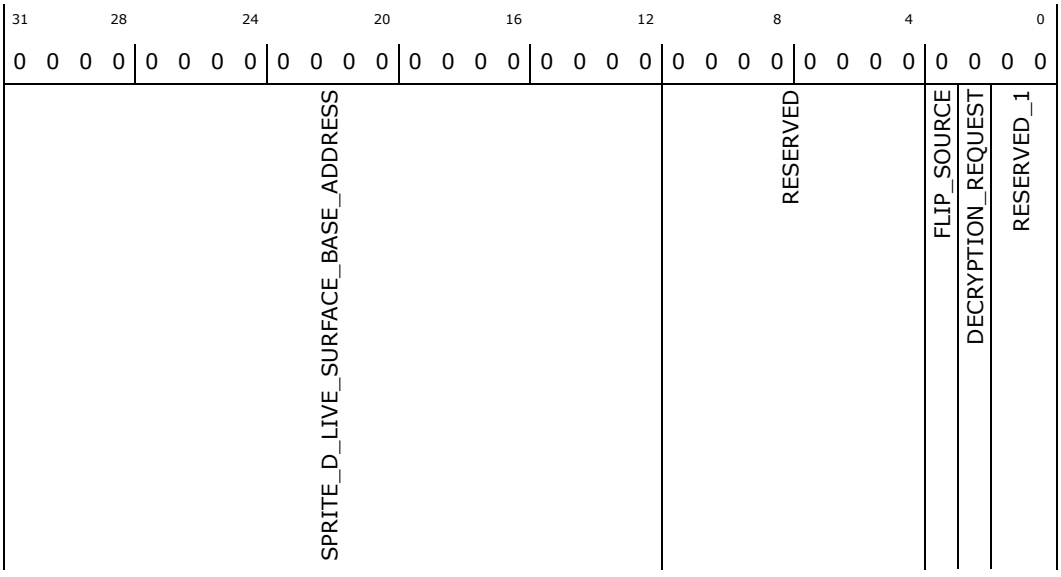
Type: Memory Mapped I/O Register (Size: 32 bits)

SPDLIVESURF: [GTTMMADR_LSB + 2BF20h] + 724ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**SPRITE_D_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite D

Bit Range	Default & Access	Description
11:4	0b RO	**RESERVED:** : MBZ
3	0b RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decryption not requested All 1b Requested Decryption requested All
1:0	0b RO	**RESERVED_1:** : MBZ

3.4.352 SPDCLRC0—Offset 724D0h

Sprite D Color Correction 0 Register

Access Method

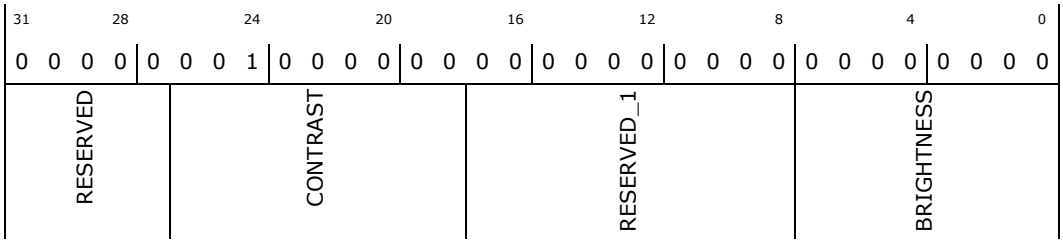
Type: Memory Mapped I/O Register (Size: 32 bits)

SPDCLRC0: [GTTMMADR_LSB + 2BF20h] + 724D0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 01000000h



Bit Range	Default & Access	Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
26:18	001000000b RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0b RW	**RESERVED_1:** Reserved.
7:0	0b RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

3.4.353 SPDCLRC1—Offset 724D4h

Sprite D Color Correction 1 Register

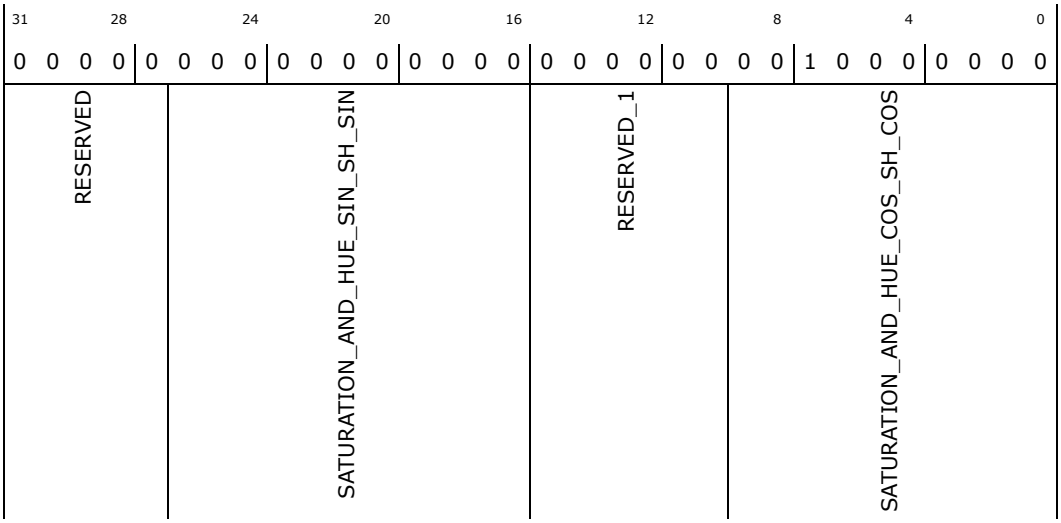
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDCLRC1: [GTTMMADR_LSB + 2BF20h] + 724D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:27	0b RW	**RESERVED:** Reserved.
26:16	0b RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0b RW	**RESERVED_1:** Reserved.
9:0	0010000000b RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

3.4.354 SPDGAMC5—Offset 724E0h

Sprite D Gamma Correction Registers

Access Method

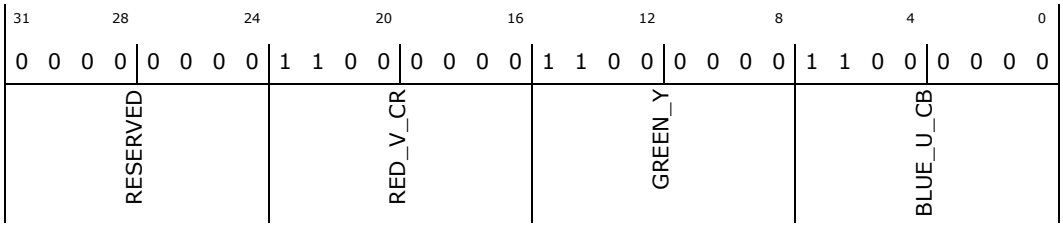
Type: Memory Mapped I/O Register (Size: 32 bits)

SPDGAMC5: [GTTMMADR_LSB + 2BF20h] + 724E0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00C0C0C0h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	11000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	11000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	11000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.355 SPDGAMC4—Offset 724E4h

Sprite D Gamma Correction Registers

Access Method

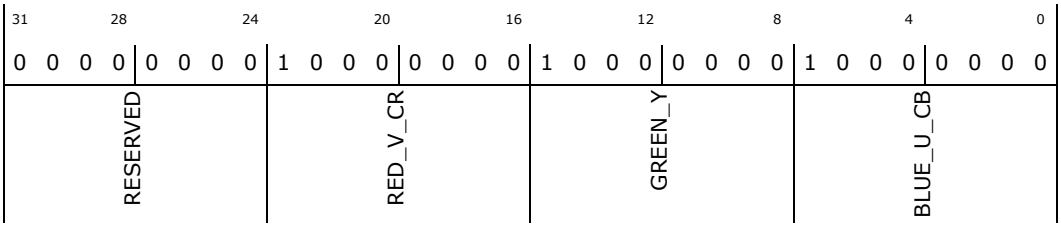
Type: Memory Mapped I/O Register (Size: 32 bits)

SPDGAMC4: [GTTMMADR_LSB + 2BF20h] + 724E4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00808080h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	10000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	10000000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	10000000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

3.4.356 SPDGAMC3—Offset 724E8h

Sprite D Gamma Correction Registers

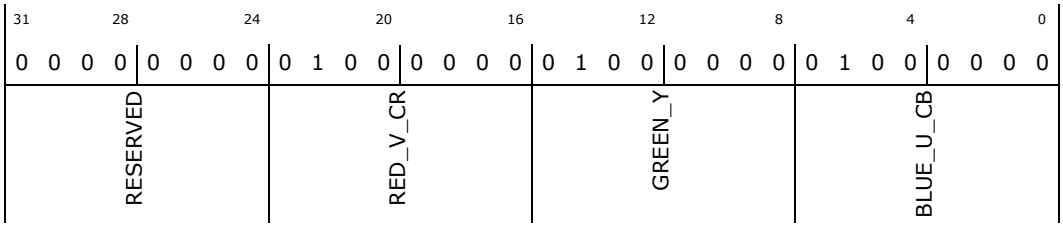
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDGAMC3: [GTTMMADR_LSB + 2BF20h] + 724E8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00404040h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	01000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	01000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	01000000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

3.4.357 SPDGAMC2—Offset 724ECh

Sprite D Gamma Correction Registers

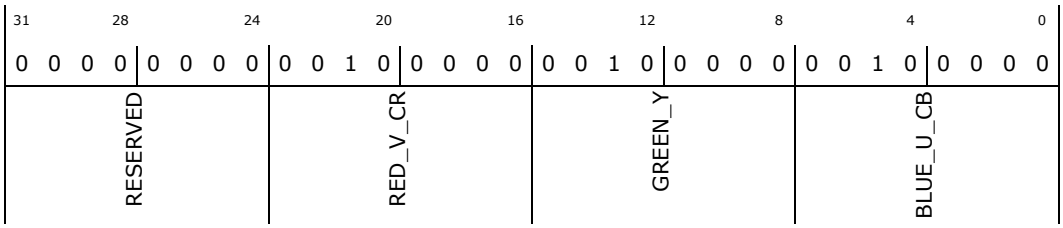
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDGAMC2: [GTTMMADR_LSB + 2BF20h] + 724ECh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00202020h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved

Bit Range	Default & Access	Description
23:16	00100000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00100000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00100000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

3.4.358 SPDGAMC1—Offset 724F0h

Sprite D Gamma Correction Registers

Access Method

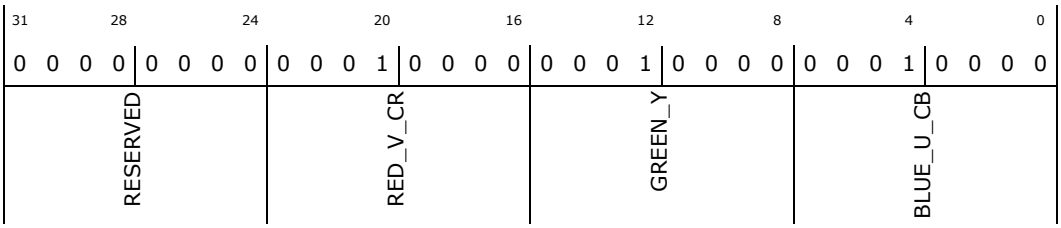
Type: Memory Mapped I/O Register (Size: 32 bits)

SPDGAMC1: [GTTMMADR_LSB + 2BF20h] + 724F0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00101010h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	00010000b RW	**RED_V_CR:** gamma correction mapping red to CR
15:8	00010000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00010000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

3.4.359 SPDGAMC0—Offset 724F4h

Sprite D Gamma Correction Registers

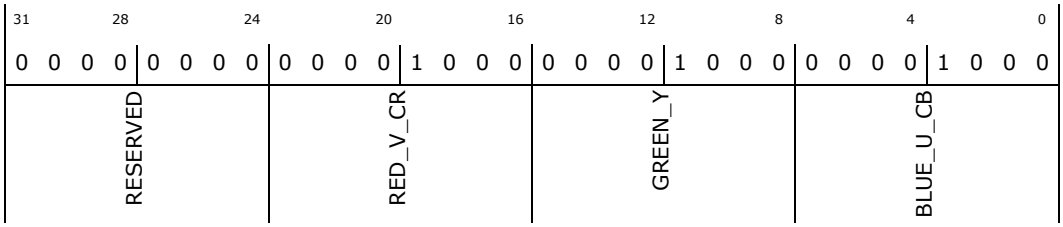
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SPDGAMC0: [GTTMMADR_LSB + 2BF20h] + 724F4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00080808h



Bit Range	Default & Access	Description
31:24	0b RW	**RESERVED:** reserved
23:16	00001000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00001000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	00001000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

3.4.360 PCSRC—Offset 73000h

Performance Counter Source Register

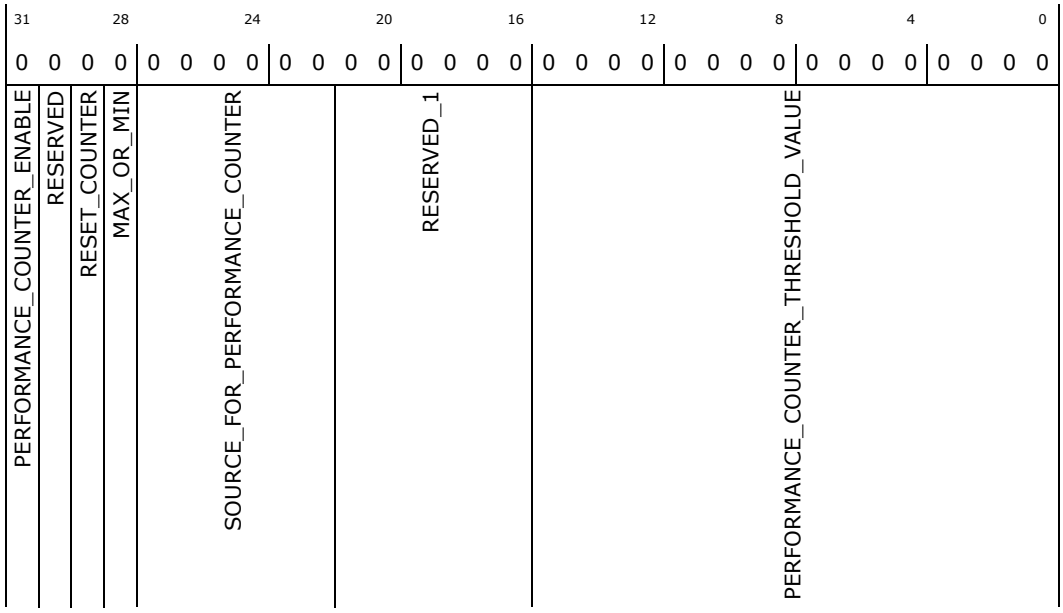
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PCSRC: [GTTMMADR_LSB + 2BF20h] + 73000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**PERFORMANCE_COUNTER_ENABLE:** This bit enables the performance counter. 0 = Performance counter is disabled 1 = Performance counter is enabled.
30	0b RW	**RESERVED:** Reserved.
29	0b RW	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, summing all events in the frame 0 = Reset after each event within the frame
28	0b RW	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value. The previous value is used to do the compare. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Description
27:22	0b RW	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = VGA Font Request Latency 000010 = VGA Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Steamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Steamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 100111 = Sprite D Command Request Latency 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA)
21:16	0b RW	**RESERVED_1:** Write as zero.
15:0	0b RW	**PERFORMANCE_COUNTER_THRESHOLD_VALUE:** This value is used to compare against the performance counter. If the performance counter matches this value, an interrupt is generated if the interrupt bit is enabled. When the source selected is DDB FIFO status, the threshold value is used to program the value needed to monitor in the DDB FIFO. No interrupt is generated in this condition.

3.4.361 PCSTAT—Offset 73004h

Performance Counter Status Register

Access Method

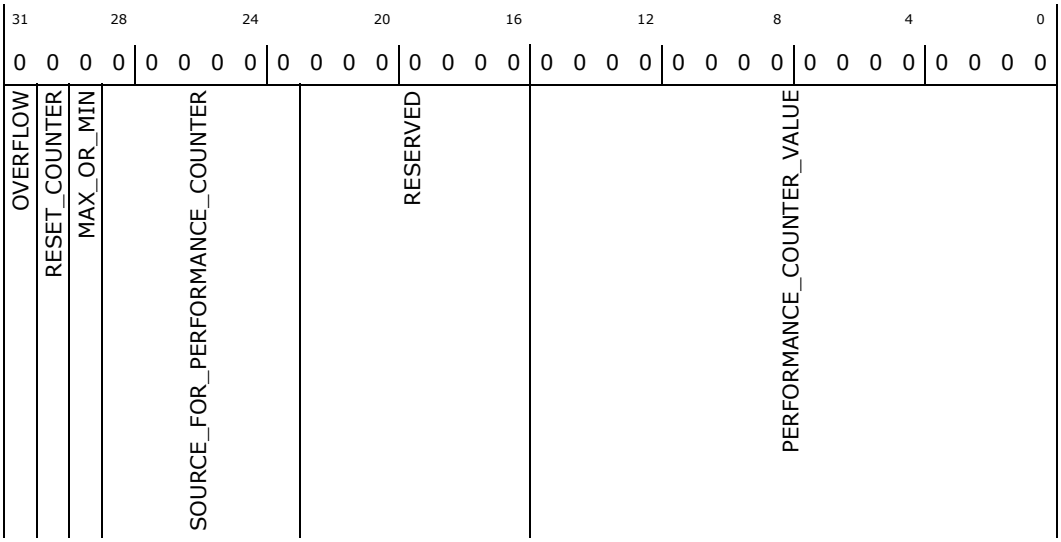
Type: Memory Mapped I/O Register (Size: 32 bits)

PCSTAT: [GTTMMADR_LSB + 2BF20h] + 73004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**OVERFLOW:** This bit indicates weather the 16 bit counter overflowed or not. 0 = Counter is valid 1 = Counter is invalid since it overflowed
30	0b RO	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, sum of all event in the frame 0 = Reset after each event within the frame
29	0b RO	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value of the previous event. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Description
28:23	0b RO	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = VGA Font Request Latency 000010 = VGA Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Steamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Steamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 100111 = Sprite D Command Request Latency 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA)
22:16	0b RO	**RESERVED:** Write as zero.
15:0	0b RO	**PERFORMANCE_COUNTER_VALUE:** This is the value of the performance counter for the source indicated in the source field.

3.4.362 PCSRC2—Offset 73008h

Performance Counter Source2 Register

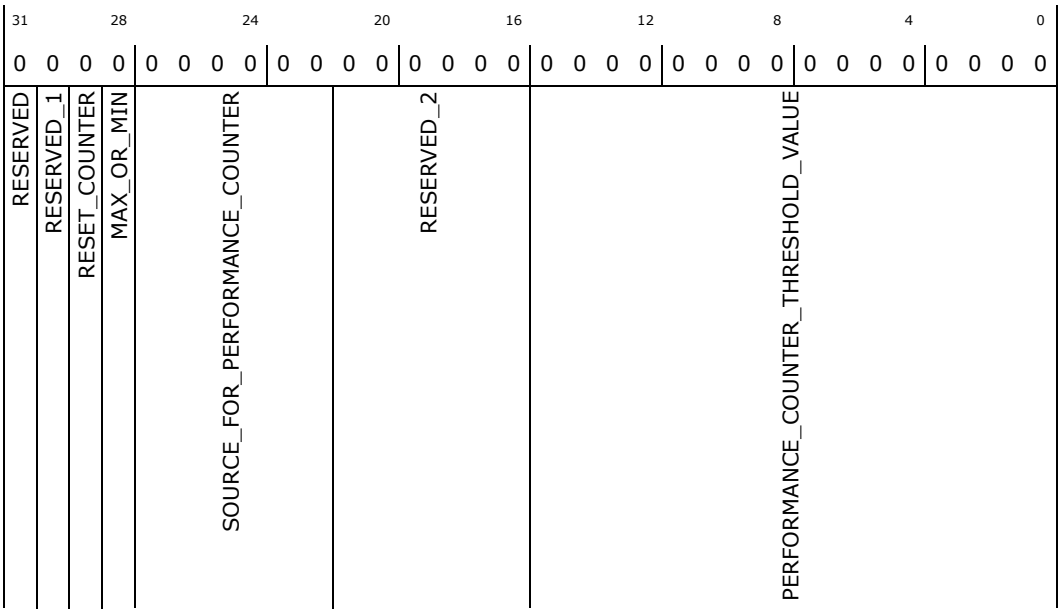
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PCSRC2: [GTTMMADR_LSB + 2BF20h] + 73008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**RESERVED:** Programming note: This second performance counter is enabled by the enable bit in the PCSRC1 bit 31.
30	0b RW	**RESERVED_1:** Reserved.
29	0b RW	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, summing all events in the frame 0 = Reset after each event within the frame
28	0b RW	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value. The previous value is used to do the compare. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Description
27:22	0b RW	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = VGA Font Request Latency 000010 = VGA Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Streamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Streamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 100111 = Sprite D Command Request Latency 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB)
21:16	0b RW	**RESERVED_2:** Write as zero.
15:0	0b RW	**PERFORMANCE_COUNTER_THRESHOLD_VALUE:** This value is used to compare against the performance counter. If the performance counter matches this value, an interrupt is generated if the interrupt bit is enabled. When the source selected is DDB FIFO status, the threshold value is used to program the value needed to monitor in the DDB FIFO. No interrupt is generated in this condition.

3.4.363 PCSTAT2—Offset 7300Ch

Performance Counter Status2 Register

Access Method

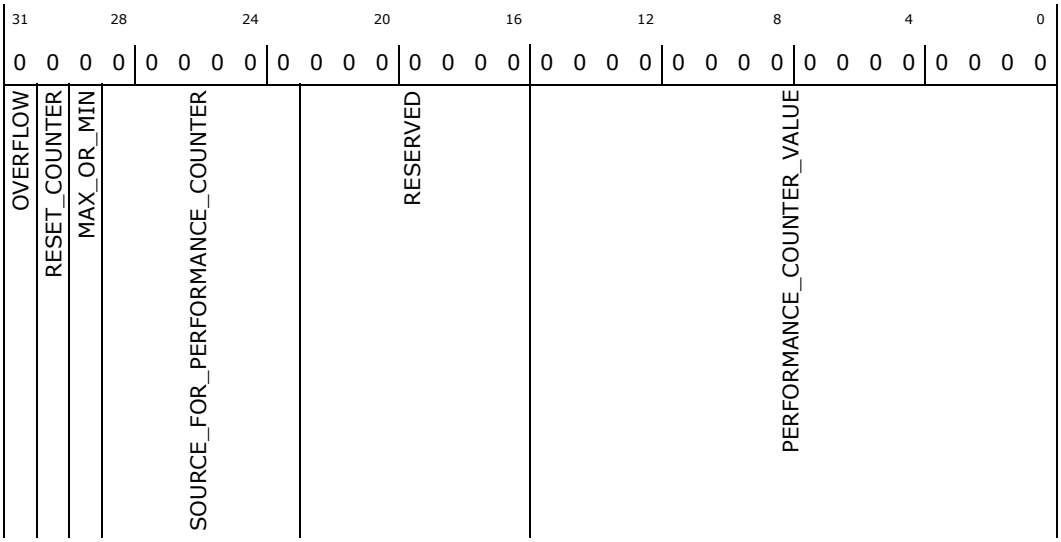
Type: Memory Mapped I/O Register (Size: 32 bits)

PCSTAT2: [GTTMMADR_LSB + 2BF20h] + 7300Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**OVERFLOW:** This bit indicates weather the 16 bit counter overflowed or not. 0 = Counter is valid 1 = Counter is invalid since it overflowed
30	0b RO	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, sum of all event in the frame 0 = Reset after each event within the frame
29	0b RO	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value of the previous event. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Description
28:23	0b RO	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = VGA Font Request Latency 000010 = VGA Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Steamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Steamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 101001 = InSR to HP Put (first put after inSR failing edge) 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB)
22:16	0b RO	**RESERVED:** Write as zero.
15:0	0b RO	**PERFORMANCE_COUNTER_VALUE:** This is the value of the performance counter for the source indicated in the source field.

3.5 Display Memory Mapped Registers (Write Only)

Table 13. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size	Register ID—Description	Default Value
3BAh	1	"FCR (FCR_MDA_Write)—Offset 3BAh" on page 683	00h
3C2h	1	"MSR (MSR_Write)—Offset 3C2h" on page 684	00h
3C7h	1	"DACRX—Offset 3C7h" on page 685	00h
3DAh	1	"FCR (FCR_CGA_Write)—Offset 3DAh" on page 686	00h

3.5.1 FCR (FCR_MDA_Write)—Offset 3BAh

Feature Control

Access Method

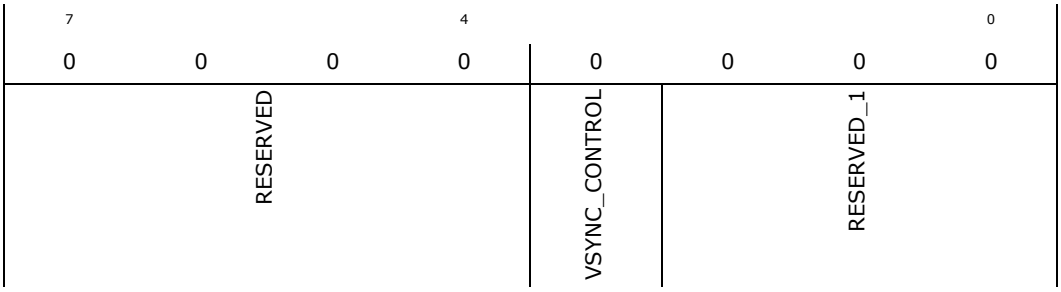
Type: Memory Mapped I/O Register (Size: 8 bits)

FCR_MDA_Write: [GTTMMADR_LSB + 2BF20h] + 3BAh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:4	0b RW	**RESERVED:** Read as 0.
3	0b RW	**VSYNC_CONTROL:** This bit is provided for compatibility only and has no other function. Reads and writes to this bit have no effect other than to change the value of this bit. The previous definition of this bit selected the output on the VSYNC pin. 0 = Was used to set VSYNC out put on the VSYNC pin (default). 1 = Was used to set the log i cal 'OR' of VSYNC and Display Enable output on the VSYNC pin. This capability was not typically very useful..
2:0	0b RW	**RESERVED_1:** Read as 0.

3.5.2 MSR (MSR_Write)—Offset 3C2h

Miscellaneous Output

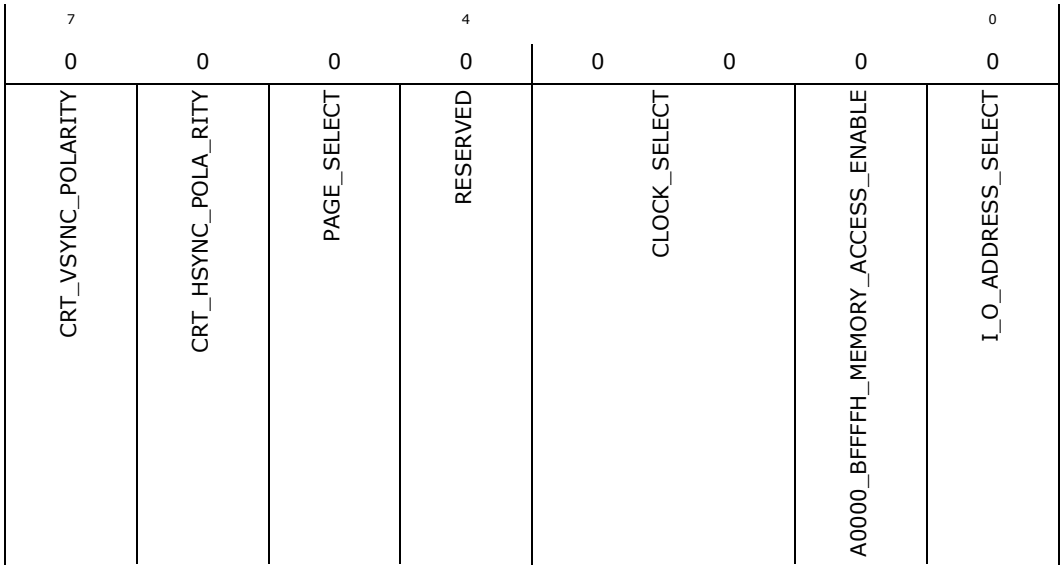
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

MSR_Write: [GTTMMADR_LSB + 2BF20h] + 3C2h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RW	**CRT_VSYNC_POLARITY:** This is a legacy function that is used in native VGA modes. For most cases, sync polarity will be controlled by the port control bits. The VGA settings can be optionally selected for compatibility with the original VGA when used in the VGA native mode. Sync polarity was used in VGA to signal the monitor how many lines of active display are being generated. 0 = Positive Polarity (default). 1 = Negative Polarity.
6	0b RW	**CRT_HSYNC_POLA_RITY:** This is a legacy function that is used in native VGA modes. For most cases, sync polarity will be controlled by the port control bits. The VGA settings can be optionally selected for compatibility with the original VGA when used in the VGA native mode. 0 = Positive Polarity (default). 1 = Negative Polarity
5	0b RW	**PAGE_SELECT:** In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KB page in dis play memory for CPU access: 0 = Upper page (default) 1 = Lower page. Selects between two 64KB pages of frame buffer memory during standard VGA odd/even modes (modes 0h through 5h). Bit 1 of register GR06 can also program this bit in other modes. Note that this bit is would normally set to 1 by the software.
4	0b RW	**RESERVED:** Read as 0.

Bit Range	Default & Access	Description
3:2	0b RW	**CLOCK_SELECT:** These bits can select the dot clock source for the CRT interface. The bits should be used to select the dot clock in standard native VGA modes only. When in the centering or upper left corner modes, these bits should be set to have no effect on the clock rate. The actual frequencies that these bits select, if they have any affect at all, is programmable through the DPLL registers that default to the standard values used for VGA. 00 = CLK0, 25.175 MHz (for standard VGA modes with 640 pixel (8-dot) horizontal resolution) (default) 01 = CLK1, 28.322 MHz. (for standard VGA modes with 720 pixel (9-dot) horizontal resolution) 10 = Was used to select an external clock (now unused) 11 = Reserved
1	0b RW	**A0000_BFFFFH_MEMORY_ACCESS_ENABLE:** VGA Compatibility bit enables access to local video memory (frame buffer) at A0000(BFFFFh. When disabled, accesses to VGA memory are blocked in this region. This bit is independent of and does not block CPU access to the video linear frame buffer at other addresses. Note that it is typical for AGP chipsets to shadow this register to allow proper steering of memory accesses to the proper bus. 0 = Prevent CPU access to memory/registers/ROM through the A0000-BFFFF VGA memory aperture (default). 1 = Allow CPU access to memory/registers/ROM through the A0000-BFFFF VGA memory aperture. This memory must be mapped as UC by the CPU; see VGA Host Access Memory Munging in Display and Overlay Functions.
0	0b RW	**I_O_ADDRESS_SELECT:** This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01). Presently ignored (whole range is claimed), but will ignore 3Bx for color configuration or 3Dx for monochrome. Note that it is typical in AGP chipsets to shadow this bit and properly steer I/O cycles to the proper bus for operation where a MDA exists on another bus such as ISA. 0 = Select 3Bxh I/O address (MDA emulation) (default). 1 = Select 3Dxh I/O address (CGA emulation).

3.5.3 DACRX—Offset 3C7h

Palette Read Index Register

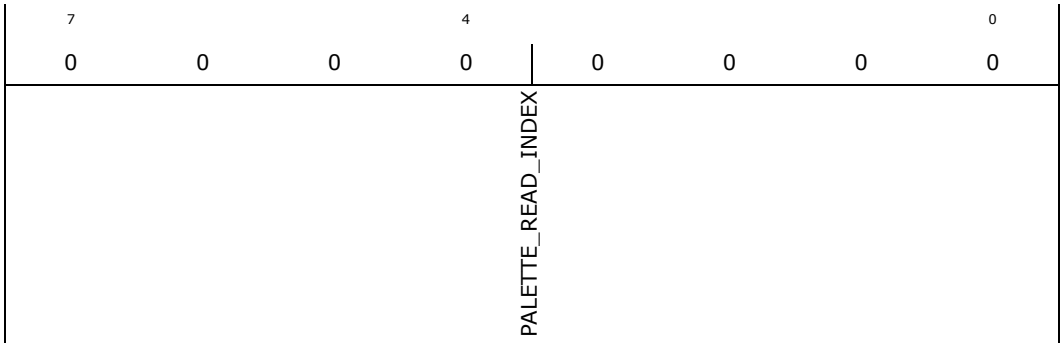
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

DACRX: [GTTMMADR_LSB + 2BF20h] + 3C7h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b WO	**PALETTE_READ_INDEX:** The 8-bit index value programmed into this register chooses which of 256 standard color data positions within the palette are to be made accessible for being read from via the Palette Data Register (DACDATA). The index value held in this register is automatically incremented when all three bytes of the color data position selected by the current index have been read. A write to this register will abort a uncompleted palette write sequence. This register allows access to the palette even when running non-VGA display modes.

3.5.4 FCR (FCR_CGA_Write)—Offset 3DAh

Feature Control

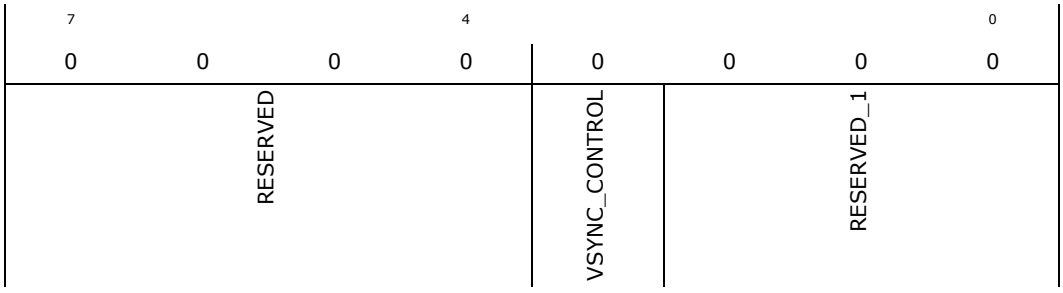
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

FCR_CGA_Write: [GTTMMADR_LSB + 2BF20h] + 3DAh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:4	0b RW	**RESERVED:** Read as 0.

Bit Range	Default & Access	Description
3	0b RW	**VSYNC_CONTROL:** This bit is provided for compatibility only and has no other function. Reads and writes to this bit have no effect other than to change the value of this bit. The previous definition of this bit selected the output on the VSYNC pin. 0 = Was used to set VSYNC out put on the VSYNC pin (default). 1 = Was used to set the log i cal 'OR' of VSYNC and Display Enable output on the VSYNC pin. This capability was not typically very useful..
2:0	0b RW	**RESERVED_1:** Read as 0.

3.6 Image Signal Processor PCI Configuration Registers

Table 14. Summary of Image Signal Processor PCI Configuration Registers—0/2/0

Offset	Size	Register ID—Description	Default Value
0h	4	"iunit_ID_type (ID)—Offset 0h" on page 689	0F388086h
4h	4	"iunit_PCICMDSTS_type (PCICMDSTS)—Offset 4h" on page 689	00100000h
8h	4	"iunit_RIDCC_type (RIDCC)—Offset 8h" on page 690	04800001h
Ch	4	"iunit_HDR_type (HDR)—Offset Ch" on page 691	00000000h
10h	4	"iunit_ISPMMADR_type (ISPMMADR)—Offset 10h" on page 692	00000000h
2Ch	4	"iunit_SSID_type (SSID)—Offset 2Ch" on page 692	00000000h
34h	4	"iunit_CAPPOINT_type (CAPPOINT)—Offset 34h" on page 693	00000080h
3Ch	4	"iunit_INTR_type (INTR)—Offset 3Ch" on page 693	00000000h
80h	4	"iunit_PMCAP_type (PMCAP)—Offset 80h" on page 694	00229001h
84h	4	"iunit_PMCS_type (PMCS)—Offset 84h" on page 694	00000000h
90h	4	"iunit_MSI_CAPID_type (MSI_CAPID)—Offset 90h" on page 695	00000005h
94h	4	"iunit_MSI_ADDRESS_type (MSI_ADDRESS)—Offset 94h" on page 696	00000000h
98h	4	"iunit_MSI_DATA_type (MSI_DATA)—Offset 98h" on page 696	00000000h
9Ch	4	"iunit_INTERRUPT_CONTROL_type (INTERRUPT_CONTROL)—Offset 9Ch" on page 697	00000100h
B0h	4	"iunit_PERF0_type (PERF0)—Offset B0h" on page 698	00000000h
B4h	4	"iunit_PERF1_type (PERF1)—Offset B4h" on page 699	00000000h
B8h	4	"iunit_PERF2_type (PERF2)—Offset B8h" on page 699	00000000h
BCh	4	"iunit_PERF3_type (PERF3)—Offset BCh" on page 700	00000000h
C0h	4	"iunit_MISR0_type (MISR0)—Offset C0h" on page 701	FFFFFFFFh
C4h	4	"iunit_MISR1_type (MISR1)—Offset C4h" on page 702	FFFFFFFFh
C8h	4	"iunit_MISR2_type (MISR2)—Offset C8h" on page 702	FFFFFFFFh
CCh	4	"iunit_MISR3_type (MISR3)—Offset CCh" on page 702	FFFFFFFFh
D0h	4	"iunit_MANUFACTURING_ID_type (MANUFACTURING_ID)—Offset D0h" on page 703	00000000h
D4h	4	"iunit_IUNIT_ACCESS_CTRL_VIOL_type (IUNIT_ACCESS_CTRL_VIOL)—Offset D4h" on page 703	00000000h
D8h	4	"iunit_IUNIT_DEADLINE_STATUS_type (IUNIT_DEADLINE_STATUS)—Offset D8h" on page 704	00000000h
DCh	4	"iunit_IUNIT_AFE_HS_CONTROL_type (IUNIT_AFE_HS_CONTROL)—Offset DCh" on page 705	64000A00h
E0h	4	"iunit_IUNIT_AFE_RCOMP_CONTROL_type (IUNIT_AFE_RCOMP_CONTROL)—Offset E0h" on page 706	00000000h
E4h	4	"iunit_IUNIT_AFE_TRIM_CONTROL_type (IUNIT_AFE_TRIM_CONTROL)—Offset E4h" on page 707	00000000h

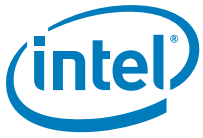


Table 14. Summary of Image Signal Processor PCI Configuration Registers—0/2/0

Offset	Size	Register ID—Description	Default Value
E8h	4	"iunit_IUNIT_CSI_CONTROL_type (IUNIT_CSI_CONTROL)—Offset E8h" on page 708	000003F8h
ECh	4	"iunit_IUNIT_DEADLINE_CONTROL_type (IUNIT_DEADLINE_CONTROL)—Offset ECh" on page 709	040A0100h
F0h	4	"iunit_IUNIT_RCOMP_STATUS_type (IUNIT_RCOMP_STATUS)—Offset F0h" on page 710	16161616h
F4h	4	"iunit_IUNIT_RCOMP_CONTROL_type (IUNIT_RCOMP_CONTROL)—Offset F4h" on page 711	00200001h
F8h	4	"iunit_IUNIT_STATUS_type (IUNIT_STATUS)—Offset F8h" on page 713	0000EB01h
FCh	4	"iunit_IUNIT_CONTROL_type (IUNIT_CONTROL)—Offset FCh" on page 714	00000103h

3.6.1 iunit_ID_type (ID)—Offset 0h

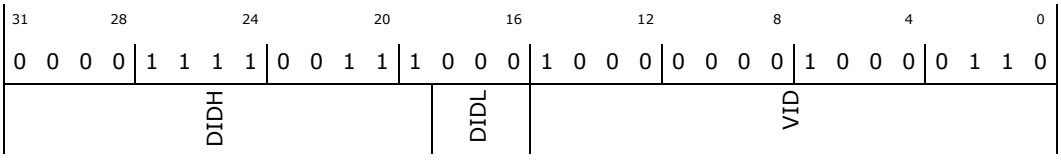
PCI Device and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ID: [B:0, D:3, F:0] + 0h

Default: 0F388086h



Bit Range	Default & Access	Description
31:19	01E7h RO	**DIDH:** DEVICE_IDENTIFICATION_NUMBER_HIGH: Upper bits of ISP Device ID. Connected to straps at IUNIT top level. (Tangier IUNIT Device IDs range from 16'h1178 through 16'h117F. IUNIT Device IDs range from 16'h0F38 through 16'h0F3F.)
18:16	000b RO	**DIDL:** DEVICE_IDENTIFICATION_NUMBER_LOW: Lower bits of ISP Device ID. Connected to fuse FB_isp_device_id. (Tangier IUNIT Device IDs range from 16'h1178 through 16'h117F. IUNIT Device IDs range from 16'h0F38 through 16'h0F3F.)
15:0	8086h RO	**VID:** VENDOR_IDENTIFICATION_NUMBER: PCI standard identification for Intel.

3.6.2 iunit_PCICMDSTS_type (PCICMDSTS)—Offset 4h

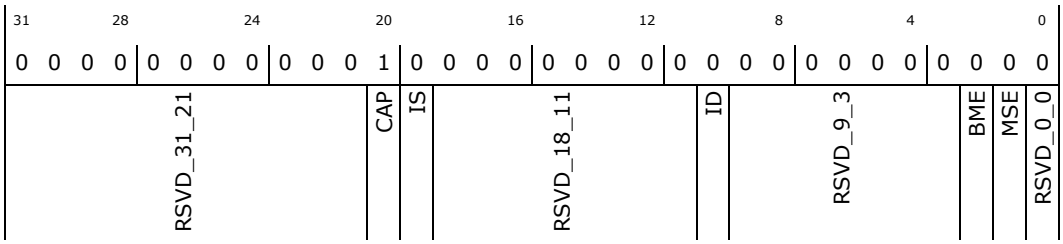
PCI Command and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCICMDSTS: [B:0, D:3, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31:21	0h RO	**RSVD_31_21:** Reserved
20	1b RO	**CAP:** CAPABILITY_LIST: Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list.
19	0b RO	**IS:** INTERRUPT_STATUS: Reflects the state of the interrupt in the camera device. Is set to 1 if IER and IIR are both set. Otherwise is set to 0.
18:11	0h RO	**RSVD_18_11:** Reserved
10	0b RW	**ID:** INTERRUPT_DISABLE: When 1, blocks the sending of ASSERT_INTA and DEASSERT_INTA messages to the Intel Legacy Block (ILB). The interrupt status is not blocked from being reflected in PCICMDSTS.IS. When 0, permits the sending of ASSERT_INTA and DEASSERT_INTA messages to the ILB.
9:3	0h RO	**RSVD_9_3:** Reserved
2	0h RW	**BME:** BUS_MASTER_ENABLE: Enables ISP to function as a PCI compliant master. When 0, blocks the sending of MSI interrupts. When 1, permits the sending of MSI interrupts.
1	0h RW	**MSE:** MEMORY_SPACE_ENABLE: When set, accesses to this device's memory space is enabled. When 1, the ISP will compare the incoming address on the IOSF bus with ISPMMADR(31:22). If there is a match and if the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and present it on the AHB bus. When 0, the ISP will not claim MEMRD or MEMWR IOSF commands.
0	0h RO	**RSVD_0_0:** Reserved

3.6.3 iunit_RIDCC_type (RIDCC)—Offset 8h

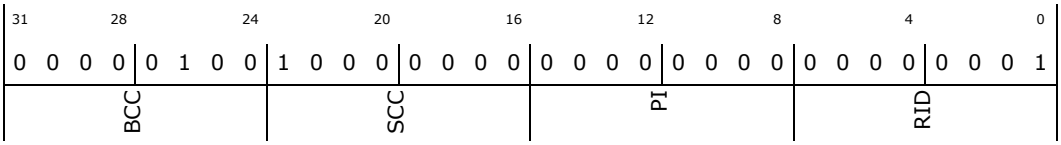
Revision Identification and Class Codes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RIDCC: [B:0, D:3, F:0] + 8h

Default: 04800001h



Bit Range	Default & Access	Description
31:24	04h RO	**BCC:** BASE_CLASS_CODE: Indicates a multimedia device.
23:16	80h RO	**SCC:** SUB_CLASS_CODE: Indicates other multimedia device.
15:8	0h RO	**PI:** PROGRAMMING_INTERFACE: Default programming interface.
7:0	01h RO	**RID:** REVISION_ID: The value in this field reflects the value of strapRID(7:0) (which is an input pin of ISP) and can be changed with each stepping of the silicon.

3.6.4 iunit_HDR_type (HDR)—Offset Ch

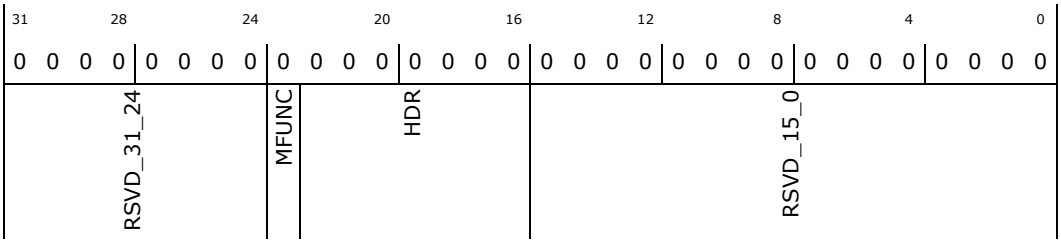
Header Type

Access Method

Type: PCI Configuration Register (Size: 32 bits)

HDR: [B:0, D:3, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**RSVD_31_24:** Reserved
23	0h RO	**MFUNC:** MULTI_FUNCTION_STATUS: IUNIT is a single function.
22:16	0h RO	**HDR:** HEADER_CODE: Indicates a type 0 header format.
15:0	0h RO	**RSVD_15_0:** Reserved

3.6.5 iunit_ISPMMADR_type (ISPMMADR)—Offset 10h

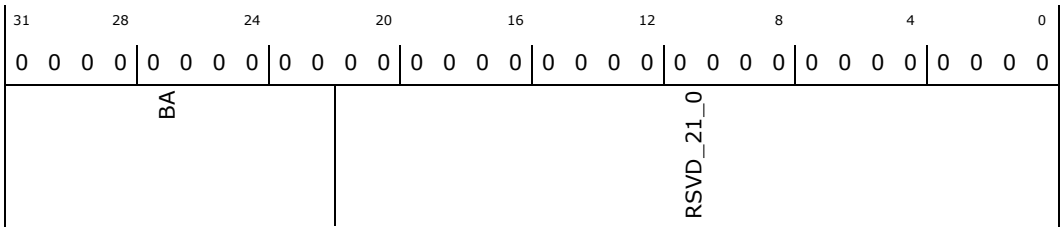
Memory Mapped Address Range. This is the base address for all memory mapped registers.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**BA:** BASE_ADDRESS: Set by the OS, these bits correspond to address signals (31:22). The ISP will compare the IOSF address (31:22) with ISPMMADR(31:22). If there is a match, and PCICMDSTS(1) = MSE = 1 and the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and present it on the AHB bus to the vendor IP.
21:0	0h RO	**RSVD_21_0:** Reserved

3.6.6 iunit_SSID_type (SSID)—Offset 2Ch

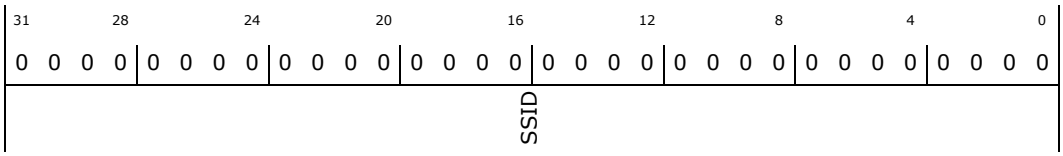
Subsystem Identifiers

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SSID: [B:0, D:3, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**SSID:** SUBSYSTEM_IDENTIFIERS: The value in this field is a copy of the SSID register programmed by the graphics device driver or BIOS in the Device 0/2/0 PCI header. To change the subsystem ID, write to Device 0/2/0 SSID instead of to this SSID.

3.6.7 iunit_CAPPOINT_type (CAPPOINT)—Offset 34h

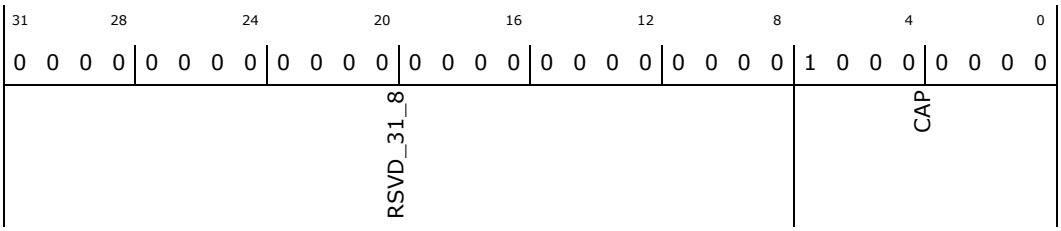
Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPPOINT: [B:0, D:3, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD_31_8:** Reserved
7:0	80h RO	**CAP:** CAPABILITIES_POINTER: The first item in the capabilities list is at address 80h.

3.6.8 iunit_INTR_type (INTR)—Offset 3Ch

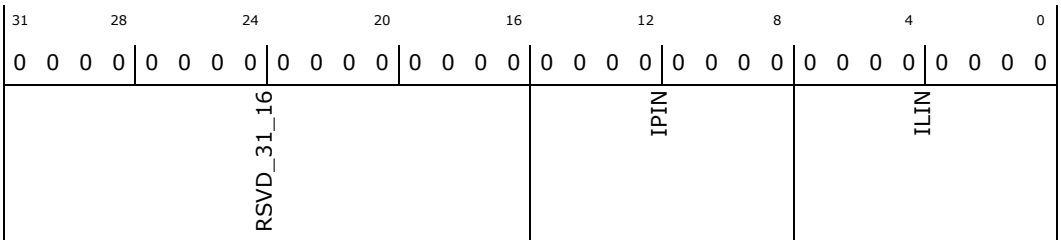
Interrupt. This register is programmed by SBIOS.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTR: [B:0, D:3, F:0] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD_31_16:** Reserved
15:8	0h RO	**IPIN:** INTERRUPT_PIN: PCI Device 0/3/0 (IUNIT) is a single function device. If INTx is used, the PCI spec requires that it use INTA#. If INTx is used (FB_intx_supported fuse is 1), then this field is hard coded to 01h. If INTx is not used (FB_intx_supported fuse is 0), this field is hard coded to 00h.

Bit Range	Default & Access	Description
7:0	0h RW	**ILIN:** INTERRUPT_LINE: BIOS written value to communicate interrupt line routing information to the ISP device driver.

3.6.9 iunit_PMCAP_type (PMCAP)—Offset 80h

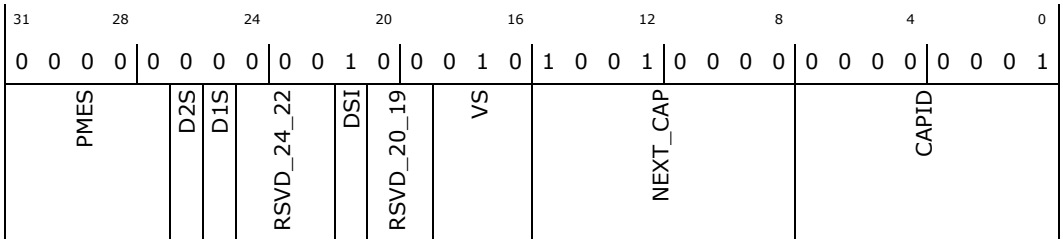
Power Management Capabilities

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMCAP: [B:0, D:3, F:0] + 80h

Default: 00229001h



Bit Range	Default & Access	Description
31:27	0h RO	**PMES:** PME_SUPPORT: The camera controller does not generate PME#.
26	0h RO	**D2S:** D2_SUPPORT: The D2 power management state is not supported.
25	0h RO	**D1S:** D1_SUPPORT: The D1 power management state is not supported.
24:22	0h RO	**RSVD_24_22:** Reserved
21	01h RO	**DSI:** DEVICE_SPECIFIC_INITIALIZATION: Hardwired to 1 to indicate that special initialization of the camera controller is required before generic class device driver is to use it.
20:19	0h RO	**RSVD_20_19:** Reserved
18:16	2h RO	**VS:** VERSION: Indicates compliance with revision 1.1 of the PCI Power Management Specification.
15:8	90h RO	**NEXT_CAP:** POINTER_TO_NEXT_CAPABILITY: Indicates the next item in the capabilities list.
7:0	01h RO	**CAPID:** CAPABILITIES: SIG defines this ID is 01h for power management.

3.6.10 iunit_PMCS_type (PMCS)—Offset 84h

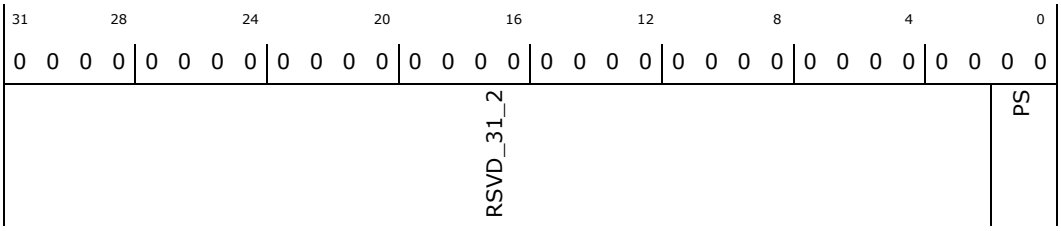
Power Management Control/Status.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMCS: [B:0, D:3, F:0] + 84h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**RSVD_31_2:** Reserved
1:0	0h RW	**PS:** POWER_STATE: Power management is implemented by writing to control registers in the PUNIT. This field may be programmed by the software driver, but no action is taken based on writing to this field.

3.6.11 iunit_MSI_CAPID_type (MSI_CAPID)—Offset 90h

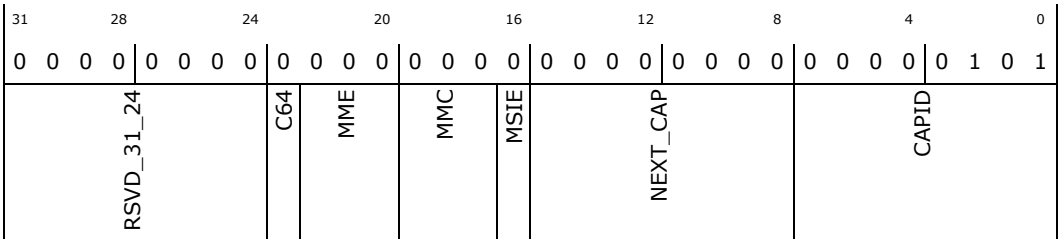
Message Signaled Interrupts Capability ID and Control Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MSI_CAPID: [B:0, D:3, F:0] + 90h

Default: 00000005h



Bit Range	Default & Access	Description
31:24	0h RO	**RSVD_31_24:** Reserved
23	0h RO	**C64:** 64_BIT_ADDRESS_CAPABLE: 32-bit capable only.
22:20	0h RW	**MME:** MULTIPLE_MESSAGE_ENABLE: This field is RW for software compatibility, but only a single message is ever generated.
19:17	0h RO	**MMC:** MULTIPLE_MESSAGE_CAPABLE: This device is only single message capable.

Bit Range	Default & Access	Description
16	0h RW	**MSIE:** MSI_ENABLE: If set, MSI is enabled. PCICMDSTS.BME must be set for an MSI to be generated.When 0, blocks the sending of a MSI interrupt. The interrupt status is not blocked from being reflected in the PCICMDSTS.IS bit. When 1, permits sending of a MSI interrupt.
15:8	0h RO	**NEXT_CAP:** POINTER_TO_NEXT_CAPABILITY: Indicates this is the last item in the list.
7:0	05h RO	**CAPID:** CAPABILITY_ID: Indicates an MSI capability.

3.6.12 iunit_MSI_ADDRESS_type (MSI_ADDRESS)—Offset 94h

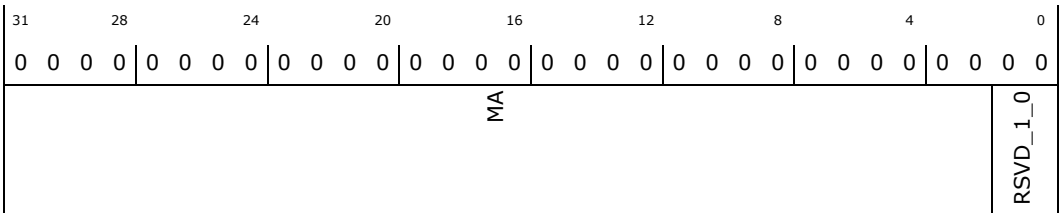
MSI Message Address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MSI_ADDRESS: [B:0, D:3, F:0] + 94h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**MA:** MSI_ADDRESS: System specified message address, always DW aligned. When the ISP issues an MSI interrupt as a MEMWR on the IOSF, the memory address used is 12xFEE, MSI_ADDRESS[19:0].
1:0	0h RO	**RSVD_1_0:** Reserved

3.6.13 iunit_MSI_DATA_type (MSI_DATA)—Offset 98h

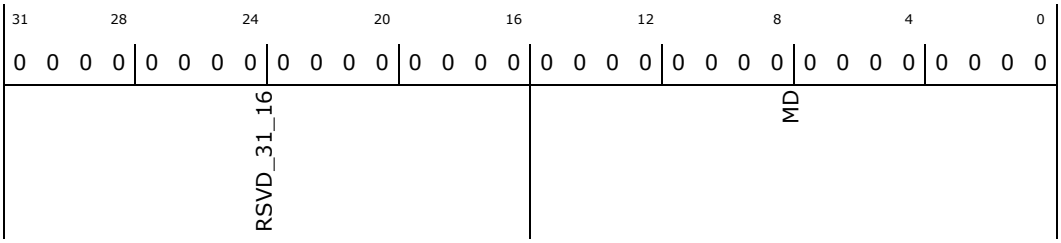
MSI Message Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MSI_DATA: [B:0, D:3, F:0] + 98h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD_31_16:** Reserved
15:0	0h RW	**MD:** MSI_DATA: This 16-bit field is programmed by system software and is driven onto the lower word of data during the data phase of the MSI write transaction. When the ISP issues an MSI interrupt as a MEMWR on the IOSF, the write data corresponds to the value of this field.

3.6.14 iunit_INTERRUPT_CONTROL_type (INTERRUPT_CONTROL)—Offset 9Ch

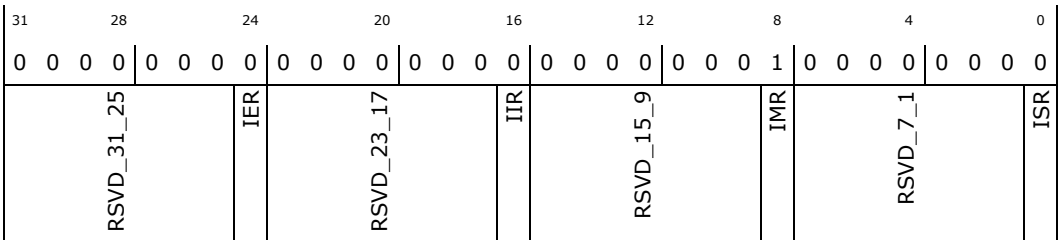
INTERRUPT_CONTROL

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPT_CONTROL: [B:0, D:3, F:0] + 9Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:25	0h RO	**RSVD_31_25:** Reserved

Bit Range	Default & Access	Description
24	0h RW	**IER:** IER: This is an enable bit that allows the sending of an interrupt to the CPU using either MSI or INTR mechanisms. The interrupt is sent immediately to the CPU. The firmware running on the ISP guarantees ordering by reading the last data write from memory before raising the interrupt. 1 = If MSI_ENABLE is set, then an MSI is sent to the CPU when the IIR bit is set, or if the IIR bit remains set after software writes to this register. If INTERRUPT_DISABLE is not set, then an ASSERT_INTA message is sent to the Intel Legacy Block (ILB) when the IIR bit is set by hardware, or if the IIR bit remains set after software writes to this register. If software clears the IIR bit, and INTERRUPT_DISABLE is not set then a DEASSERT_INTA message is sent to the ILB. 0 = Do not generate an MSI even if the MSI_ENABLE bit is set. Do not send ASSERT_INTA or DEASSERT_INTA messages to the ILB even if the INTERRUPT_DISABLE bit is not set.
23:17	0h RO	**RSVD_23_17:** Reserved
16	0h RW/1C	**IIR:** IIR: This is the persistent value of the interrupt bit. It is set by hardware, and cleared by software. Software must write a 1 to clear this bit. Writing a 0 is a NOP. If both software and hardware attempt to write to this field in the same clock cycle, hardware wins. 1 = An interrupt was received from the vendor IP when the IMR bit was not set, and software has not yet cleared it. 0 = There is no pending interrupt.
15:9	0h RO	**RSVD_15_9:** Reserved
8	1b RW	**IMR:** IMR: Interrupt Mask bit. 1 = IIR bit will not be set when the ISR bit is set. 0 = IIR bit will be set when the ISR bit is set.
7:1	0h RO	**RSVD_7_1:** Reserved
0	0h RO	**ISR:** ISR: Reflects the state of the interrupt line from the vendor IP, after it is synchronized to the czclk domain.

3.6.15 iunit_PERF0_type (PERF0)—Offset B0h

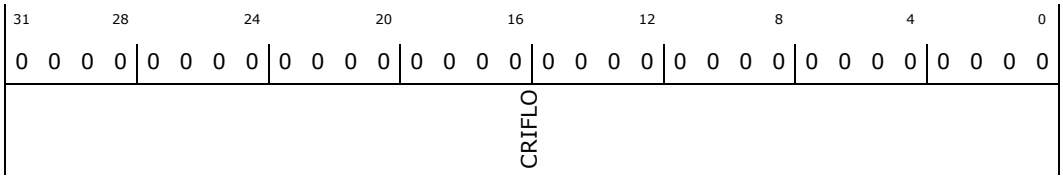
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PERF0: [B:0, D:3, F:0] + B0h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW/SE	**CRIFLO:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 31:0 of the cumulative_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will enable all four counters.

3.6.16 iunit_PERF1_type (PERF1)—Offset B4h

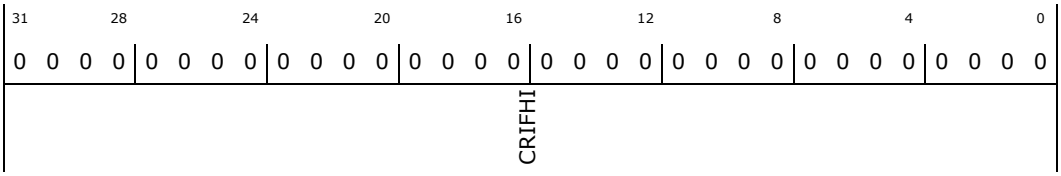
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PERF1: [B:0, D:3, F:0] + B4h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW/SE	**CRIFHI:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 63:32 of the cumulative_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will disable all four counters.

3.6.17 iunit_PERF2_type (PERF2)—Offset B8h

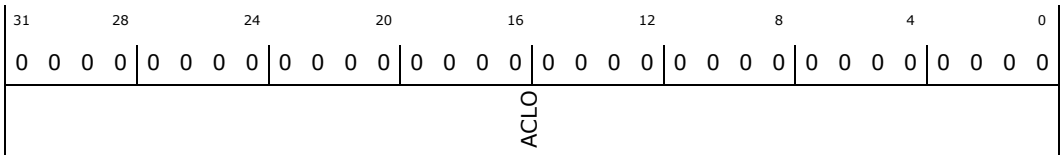
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PERF2: [B:0, D:3, F:0] + B8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW/SE	**ACLO:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 31:0 of the active_cycles counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear all four counters. The counters should only be cleared after they are disabled.

3.6.18 iunit_PERF3_type (PERF3)—Offset BCh

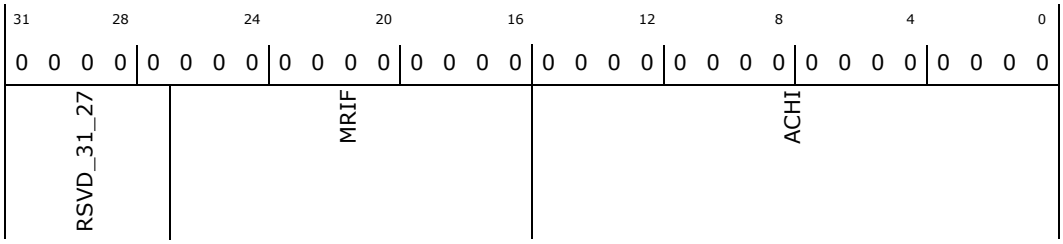
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PERF3: [B:0, D:3, F:0] + BCh

Default: 00000000h



Bit Range	Default & Access	Description
31:27	0h RO	**RSVD_31_27:** Reserved

Bit Range	Default & Access	Description
26:16	0h RW/SE	**MRIF:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 11:0 of the max_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear the max_reads_in_flight counters only. The counters should only be cleared after they are disabled.
15:0	0h RW/SE	**ACHI:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 47:32 of the active_cycles counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear the max_reads_in_flight counters only. The counters should only be cleared after they are disabled.

3.6.19 iunit_MISR0_type (MISR0)—Offset C0h

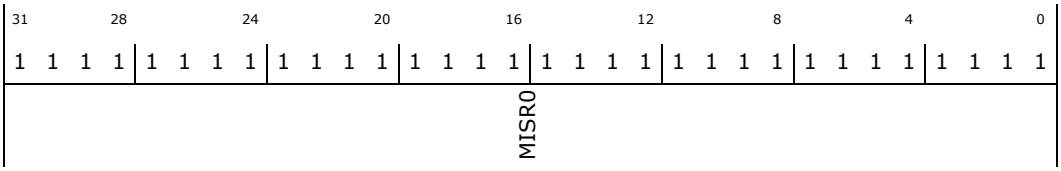
OCP Master Write Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MISR0: [B:0, D:3, F:0] + C0h

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW/C	**MISR0:** MISR0: Write to this register address clears this MISR. This is a 8:1 compression MISR capturing the 256-bit write data on the OCP interface between ISP_CSS and Iunit wrapper.

3.6.20 iunit_MISR1_type (MISR1)—Offset C4h

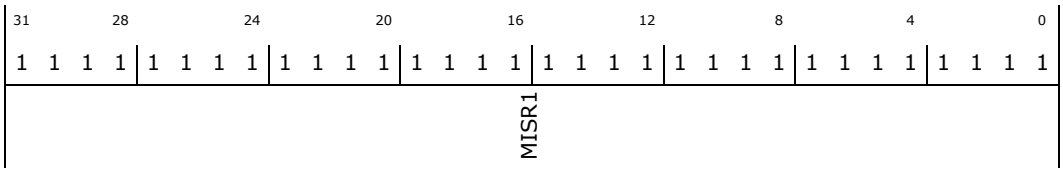
OCP Master Read Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MISR1: [B:0, D:3, F:0] + C4h

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW/C	**MISR1:** MISR1: Write to this register address clears this MISR. This is a 8:1 compression MISR capturing the 256-bit read return data on the OCP interface between ISP_CSS and Iunit wrapper.

3.6.21 iunit_MISR2_type (MISR2)—Offset C8h

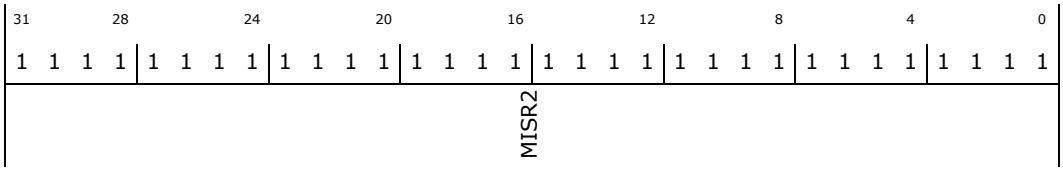
OCP Master Address and Control

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MISR2: [B:0, D:3, F:0] + C8h

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW/C	**MISR2:** MISR2: Write to this register address clears this MISR. This is a 4:1 compression MISR capturing the control signals on the OCP Master port in the Iunit.

3.6.22 iunit_MISR3_type (MISR3)—Offset CCh

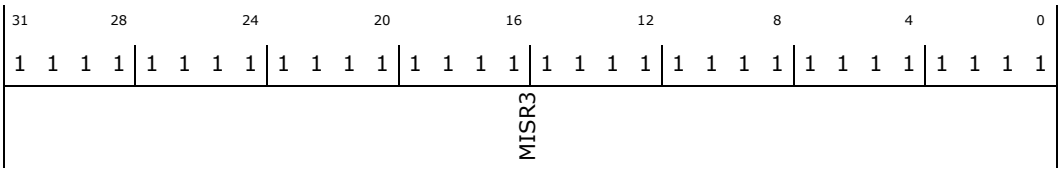
Scalar Processor output

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MISR3: [B:0, D:3, F:0] + CCh

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW/C	**MISR3:** MISR3: Write to this register address clears this MISR. This is a 4:1 compression MISR capturing the output signals of the Scalar Processor.

3.6.23 iunit_MANUFACTURING_ID_type (MANUFACTURING_ID)—Offset D0h

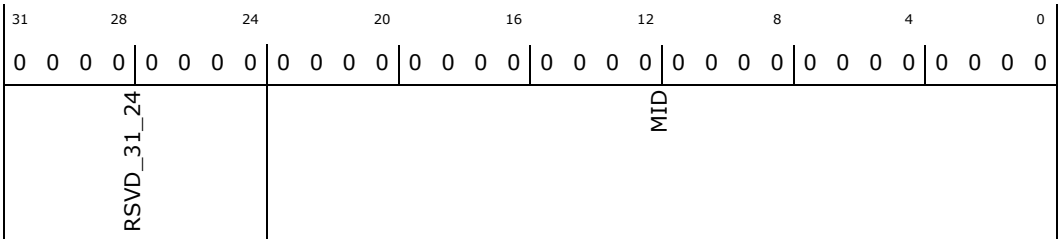
Manufacturing ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANUFACTURING_ID: [B:0, D:3, F:0] + D0h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**RSVD_31_24:** Reserved
23:0	0h RO	**MID:** MANUFACTURING_ID: Hardwired to strapMANID(23:0).

3.6.24 iunit_IUNIT_ACCESS_CTRL_VIOL_type (IUNIT_ACCESS_CTRL_VIOL)—Offset D4h

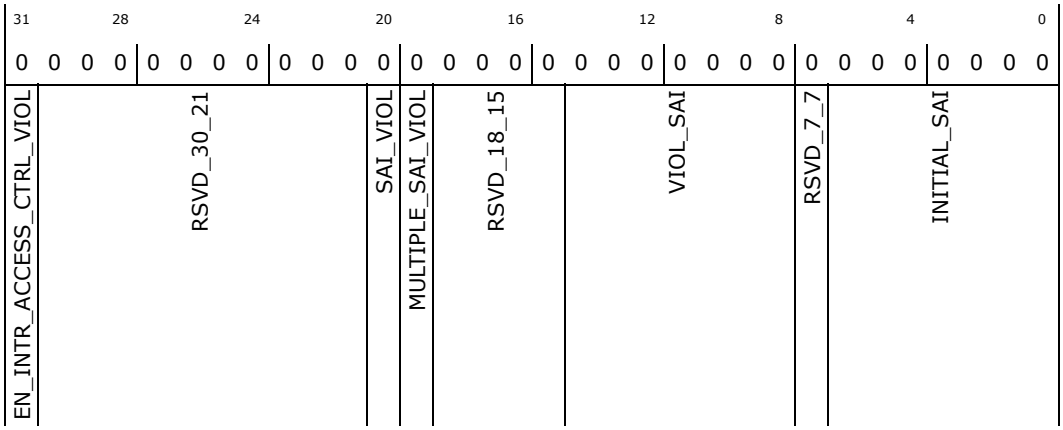
IUNIT Access control violation register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_ACCESS_CTRL_VIOL: [B:0, D:3, F:0] + D4h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**EN_INTR_ACCESS_CTRL_VIOL:** Enable Interrupt on access control violation: When set, the IUNIT will latch violation information into this register and send an interrupt request (opcode 0XEE) and (port 0x04) to the PUNIT.
30:21	00h RO	**RSVD_30_21:** Reserved
20	0b RW	**SAI_VIOL:** SAI_VIOL: If set, the IUNIT has detected an SAI violation and has captured the status in this register. This bit must be cleared by software in order for IUNIT to capture the next violation.
19	0b RW	**MULTIPLE_SAI_VIOL:** If set, more than one SAI violation has been detected in the IUNIT. Status for the 1st violation has been captured in this register. It is recommend that software clear this bit whenever it clears bit[20] of this register.
18:15	0h RO	**RSVD_18_15:** Reserved
14:8	00h RW	**VIOL_SAI:** VIOL_SAI: SAI bits that triggered the violation: This 7-bit value indicates the SAI of the subsequent transaction which caused the violation.
7	0b RO	**RSVD_7_7:** Reserved
6:0	00h RW	**INITIAL_SAI:** INITIAL_SAI: This 7-bit value indicates the SAI of the initial transaction for SAI mismatch error codes.

3.6.25 iunit_IUNIT_DEADLINE_STATUS_type (IUNIT_DEADLINE_STATUS)—Offset D8h

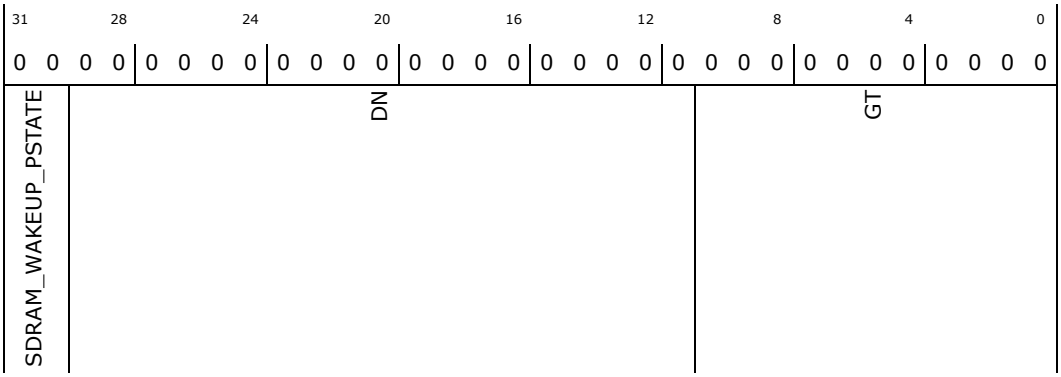
IUNIT Deadline Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_DEADLINE_STATUS: [B:0, D:3, F:0] + D8h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**SDRAM_WAKEUP_PSTATE:** SDRAM_WAKEUP_PSTATE: State of the SDRAM_WAKEUP state machine. 00b = State machine is idle; 01b = sdram_wakeup seen, waiting for all memory transactions in flight to complete; 10b = All memory transactions are completed, waiting for acknowledgement from czclk domain before returning to idle state;
29:11	0h RO	**DN:** DN: Computed deadline value to be send with the next request on IB PFI bus. This is the internal deadline value. The actual deadline that is sent on the IB PFI bus is the maximum of GT+MDD or DN.
10:0	0h RO	**GT:** GT: Current value of Global Timer

3.6.26 iunit_IUNIT_AFE_HS_CONTROL_type (IUNIT_AFE_HS_CONTROL)—Offset DCh

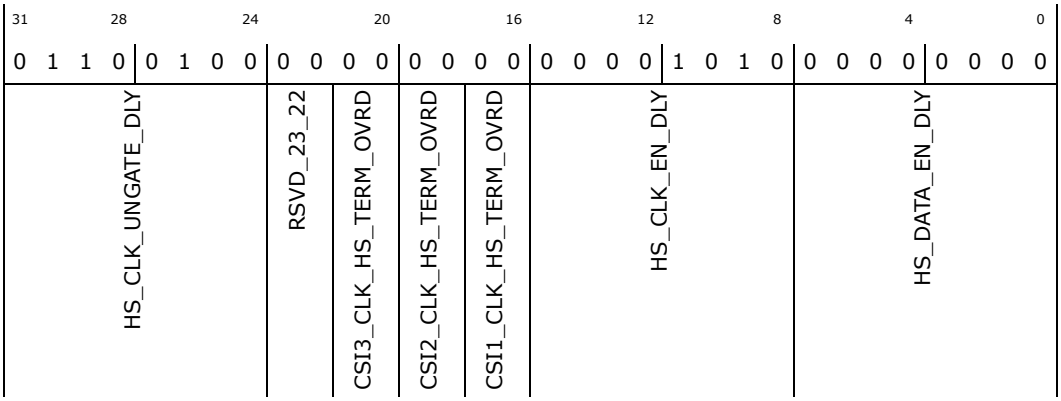
High-speed termination control MIPI CSI DPHY

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_AFE_HS_CONTROL: [B:0, D:3, F:0] + DCh

Default: 64000A00h



Bit Range	Default & Access	Description
31:24	64h RW	**HS_CLK_UNGATE_DLY:** HS_CLK_UNGATE_DLY: Delay between the assertion of HS enable and the ungating of the HS clocks going to the DPHY logic for all clock lanes. HS clocks are gated by default and are ungated after Tclk-settle time. The range of this field is 0 nsec to 510 nsec in increments of 2 nsec, with reset value 0x64 indicating 200 nsec. Note that we use czclk to increment the counter, hence the actual delay can be as much as 10 nsec larger than the programmed value.
23:22	0h RW	**RSVD_23_22:** Reserved
21:20	00b RW	**CSI3_CLK_HS_TERM_OVRD:** CSI3_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI3 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;
19:18	00b RW	**CSI2_CLK_HS_TERM_OVRD:** CSI2_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI2 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;
17:16	00b RW	**CSI1_CLK_HS_TERM_OVRD:** CSI1_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI1 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;
15:8	0Ah RW	**HS_CLK_EN_DLY:** HS_CLK_EN_DLY: Delay between the assertion of HS termination enable and the assertion of HS enable for all clock lanes. The range of this field is 0 nsec to 510 nsec in increments of 2 nsec, with reset value 0x0A indicating 20 nsec. Note that we use czclk to increment the counter, hence the actual delay can be as much as 10 nsec larger than the programmed value.
7:0	0h RW	**HS_DATA_EN_DLY:** HS_DATA_EN_DLY: Delay between the assertion of HS termination enable and the assertion of HS enable for all data lanes. The range of this field is 0 nsec to 510 nsec in increments of 2 nsec, with reset value 0x0 indicating 0 nsec. Note that we use czclk to increment the counter, hence the actual delay can be as much as 10 nsec larger than the programmed value.

3.6.27 iunit_IUNIT_AFE_RCOMP_CONTROL_type (IUNIT_AFE_RCOMP_CONTROL)—Offset E0h

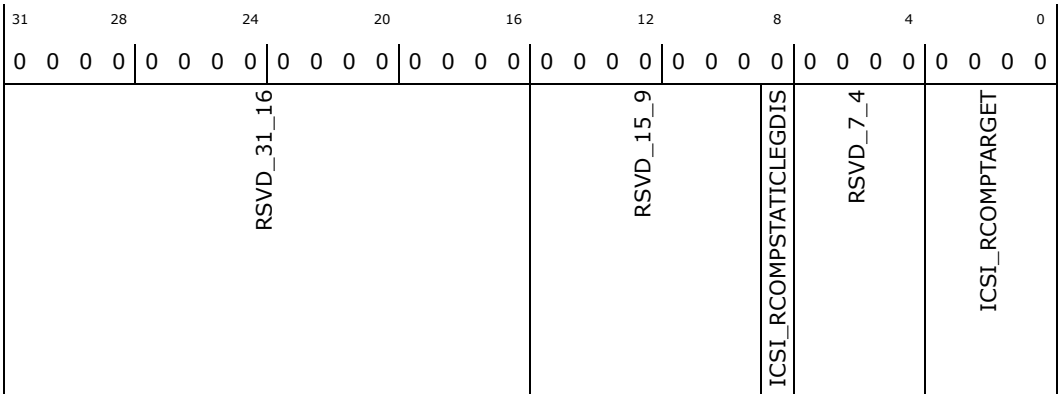
AFE RCOMP control

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_AFE_RCOMP_CONTROL: [B:0, D:3, F:0] + E0h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD_31_16:** Reserved
15:9	0h RW	**RSVD_15_9:** Reserved
8	0b RW	**ICSI_RCOMPSTATICLEGDIS:** ICSI_RCOMPSTATICLEGDIS: Disable RCOMP static leg in AFE
7:4	0h RW	**RSVD_7_4:** Reserved
3:0	0h RW	**ICSI_RCOMPTARGET:** ICSI_RCOMPTARGET: RCOMP target level range is 70ohm to 130ohm differential impedance. 0000b = 50ohms; 0001b = 30ohms; 0010b = 35ohms; 0011b = 40ohms; 0100b = 45ohms; 0101b = 55ohms; 0110b = 60ohms; 0111b = 65ohms;

3.6.28 iunit_IUNIT_AFE_TRIM_CONTROL_type (IUNIT_AFE_TRIM_CONTROL)—Offset E4h

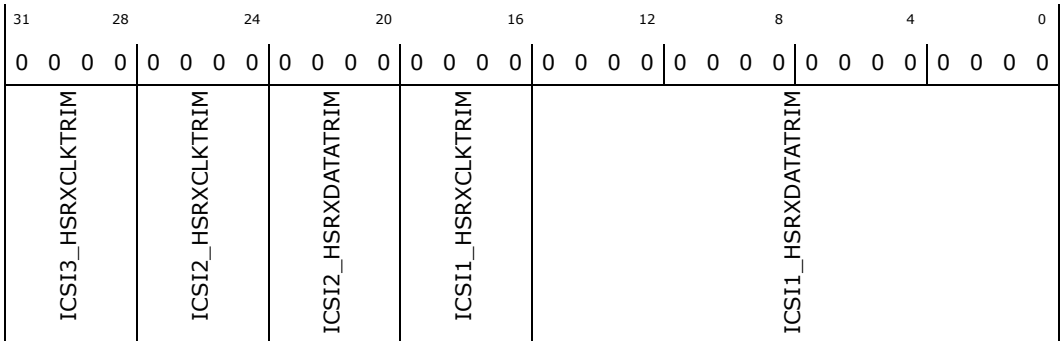
Configurable delay for CSI AFE data/clk lanes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_AFE_TRIM_CONTROL: [B:0, D:3, F:0] + E4h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**ICSI3_HSRXCLKTRIM:** ICSI3_HSRXCLKTRIM: Delay for CSI3 clock lane. Refer to the CSI AFE Circuit Architecture Spec (CAS) for the actual delays for each trim value setting.
27:24	0h RW	**ICSI2_HSRXCLKTRIM:** ICSI2_HSRXCLKTRIM: Delay for CSI2 clock lane. Refer to the CSI AFE Circuit Architecture Spec (CAS) for the actual delays for each trim value setting.
23:20	0h RW	**ICSI2_HSRXDATATRIM:** ICSI2_HSRXDATATRIM: Delay for CSI2 data lane. Refer to the CSI AFE Circuit Architecture Spec (CAS) for the actual delays for each trim value setting.
19:16	0h RW	**ICSI1_HSRXCLKTRIM:** ICSI1_HSRXCLKTRIM: Delay for CSI1 clock lane. Refer to the CSI AFE Circuit Architecture Spec (CAS) for the actual delays for each trim value setting.
15:0	0h RW	**ICSI1_HSRXDATATRIM:** ICSI1_HSRXDATATRIM: Delay for CSI1 data lanes. Refer to the CSI AFE Circuit Architecture Spec (CAS) for the actual delays for each trim value setting.

3.6.29 iunit_IUNIT_CSI_CONTROL_type (IUNIT_CSI_CONTROL)—Offset E8h

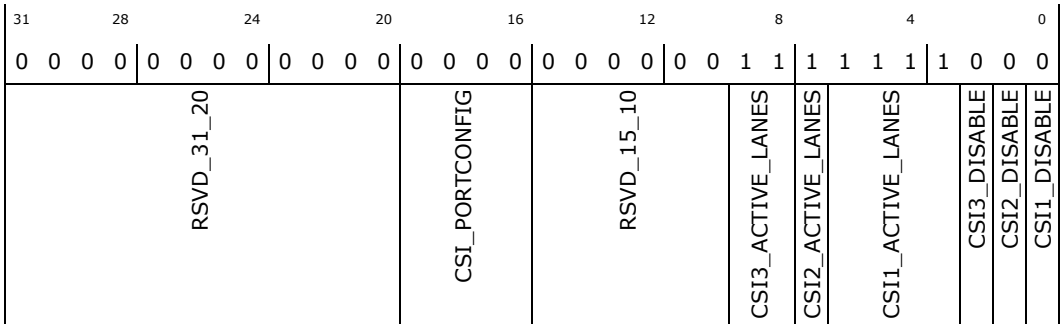
Control register for MIPI-CSI

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_CSI_CONTROL: [B:0, D:3, F:0] + E8h

Default: 000003F8h



Bit Range	Default & Access	Description
31:20	0h RW	**RSVD_31_20:** Reserved
19:16	0h RW	**CSI_PORTCONFIG:** CSI_PORTCONFIG: Used to enable the CSI data lanes to CSI ports if FB_csi_portconfig_override fuse is set. This field is ignored if FB_csi_portconfig_override fuse is clear.
15:10	0h RW	**RSVD_15_10:** Reserved
9:8	11b RW	**CSI3_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI CSI3 interface. 1=active, 0=inactive.
7	1b RW	**CSI2_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI CSI2 interface. 1=active, 0=inactive.
6:3	1111b RW	**CSI1_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI CSI1 interface. 1=active, 0=inactive.
2	0b RW	**CSI3_DISABLE:** 1 = Disable MIPI CSI3 interface. 0 = Enable MIPI CSI3 interface if FB_csi_portdisable[2] fuse is cleared
1	0b RW	**CSI2_DISABLE:** 1 = Disable MIPI CSI2 interface. 0 = Enable MIPI CSI2 interface if FB_csi_portdisable[1] fuse is cleared
0	0b RW	**CSI1_DISABLE:** 1 = Disable MIPI CSI1 interface. 0 = Enable MIPI CSI1 interface if FB_csi_portdisable[0] fuse is cleared

3.6.30 iunit_IUNIT_DEADLINE_CONTROL_type (IUNIT_DEADLINE_CONTROL)—Offset ECh

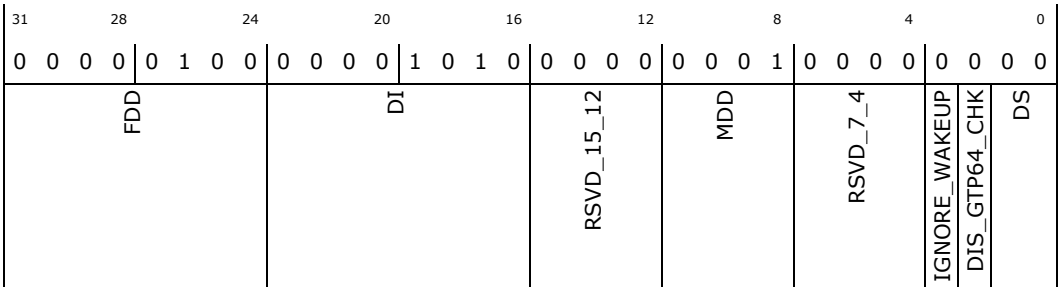
IUNIT Deadline Control Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_DEADLINE_CONTROL: [B:0, D:3, F:0] + ECh

Default: 040A0100h



Bit Range	Default & Access	Description
31:24	04h RW	**FDD:** FIRST_DEADLINE_DELAY: Delay between the rising edge of WAKEUP signal and the fake deadline that will be specified for the first request of that line. Unit in 250 nsec. Reset value of 8'h04 indicates FDD = 1 usec.
23:16	0Ah RW	**DI:** DEADLINE_INCREMENT: Difference in deadline times between adjacent requests. If the current request is for 32B, the next deadline will be DI more than the current deadline. If the current request is for 64B, the next deadline will be 2*DI more than the current deadline. Unit in 1/1024 usec. Reset value of 8'h0A indicates DI = 9.765625 nsec.
15:12	0h RW	**RSVD_15_12:** Reserved
11:8	1h RW	**MDD:** MINIMUM_DEADLINE_DELAY: Minimum separation between current Global Timer value and the deadline specified with any request on the PFI interface. Unit is 250 nsec. Reset value of 4'h1 indicates MDD = 250 nsec.
7:4	0h RW	**RSVD_7_4:** Reserved
3	0b RW	**IGNORE_WAKEUP:** If clear, then after each rising edge of sdram_wakeup, the OCP master interface is stalled until all reads in flight and all FIFOs are empty and then the next deadline is set to GT + FDD. If set, the sdram_wakeup signal from ISP_CSS is ignored.
2	0b RW	**DIS_GTP64_CHK:** If clear, then the PFI interface is stalled whenever the next deadline value exceeds GT + 64 usec. This check is a safety measure to make sure that deadline does not drift too far into the future. If set, this check is not performed.
1:0	0h RW	**DS:** DEADLINE_SCHEME: 11b = Reserved; 10b = Reserved; 01b = When WAKEUP is asserted, FDD is added to the current global timer to compute DN. With each request, the deadline sent to Pondicherry is either DN, or the sum of the global timer and MDD, whichever is larger. After each request is sent, DN is computed by adding DI for each 32Byte request sent to either DN or the sum of the global timer and MDD, whichever is larger. Each clock cycle, DN is checked to make sure it is greater than the current global timer, else it is set to the global timer.; 00b = When WAKEUP is asserted, FDD is added to the current global timer to compute DN. With each request, the deadline sent to Pondicherry is either DN, or the sum of the global timer and MDD, whichever is larger. After each request is sent, DN is computed by adding DI for each 32Byte request sent to DN. Each cycle, DN is checked to make sure that it is either greater than the current global timer, or is less than the global timer by no more than 64 usec, else it is set to the global timer minus 64 usec.

3.6.31 iunit_IUNIT_RCOMP_STATUS_type (IUNIT_RCOMP_STATUS)—Offset F0h

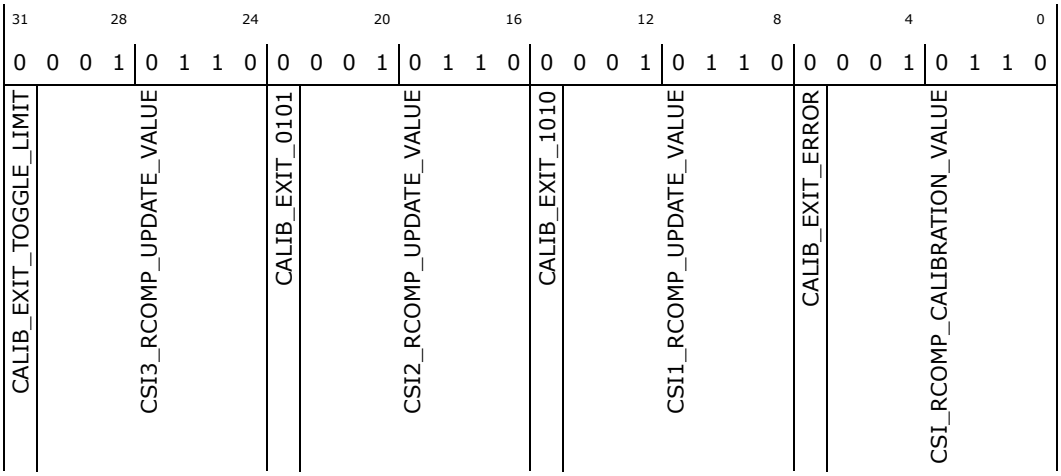
IUNIT RCOMP Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_RCOMP_STATUS: [B:0, D:3, F:0] + F0h

Default: 16161616h



Bit Range	Default & Access	Description
31	0b RO	**CALIB_EXIT_TOGGLE_LIMIT:** CALIB_EXIT_TOGGLE_LIMIT: If set, indicates that the last calibration cycle exited because the number of toggles matched the value specified by the CSI_HS_ROGGLE_LIMIT_CREG_ENC field of the IUNIT_RCOMP_CONTROL register.
30:24	16h RO	**CSI3_RCOMP_UPDATE_VALUE:** MIPI CSI3 RCOMP value: Current RCOMP value on MIPI CSI3 port
23	0b RO	**CALIB_EXIT_0101:** CALIB_EXIT_0101: If set, indicates that the last calibration cycle exited because the last four states of rcompcountup were 0101
22:16	16h RO	**CSI2_RCOMP_UPDATE_VALUE:** MIPI CSI2 RCOMP value: Current RCOMP value on MIPI CSI2 port
15	0b RO	**CALIB_EXIT_1010:** CALIB_EXIT_1010: If set, indicates that the last calibration cycle exited because the last four states of rcompcountup were 1010
14:8	16h RO	**CSI1_RCOMP_UPDATE_VALUE:** MIPI CSI1 RCOMP value: Current RCOMP value on MIPI CSI1 port
7	0b RO	**CALIB_EXIT_ERROR:** CALIB_EXIT_ERROR: If set, indicates that the last calibration cycle exited due to an error condition.
6:0	16h RO	**CSI_RCOMP_CALIBRATION_VALUE:** MIPI CSI RCOMP value from last calibration cycle

3.6.32 iunit_IUNIT_RCOMP_CONTROL_type (IUNIT_RCOMP_CONTROL)—Offset F4h

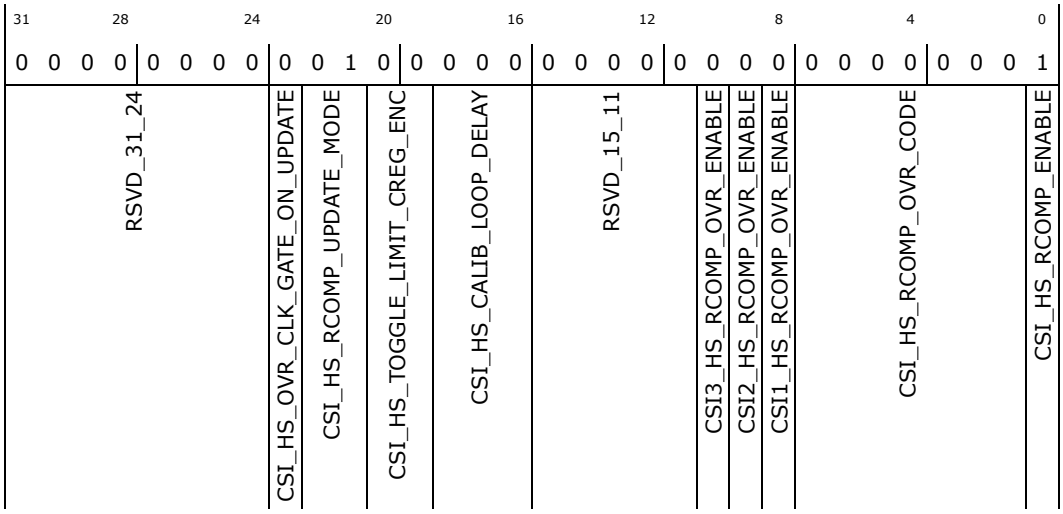
MIPI CSI RCOMP control register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_RCOMP_CONTROL: [B:0, D:3, F:0] + F4h

Default: 00200001h



Bit Range	Default & Access	Description
31:24	0h RW	**RSVD_31_24:** Reserved
23	0b RW	**CSI_HS_OVR_CLK_GATE_ON_UPDATE:** CSI_HS_OVR_CLK_GATE_ON_UPDATE: If cleared, the high speed clock going to the digital logic is gated when RCOMP update is happening. The clock is gated for a minimum of 100 nsec. If this bit is set, then the high speed clock is not gated during the update cycle.
22:21	01b RW	**CSI_HS_RCOMP_UPDATE_MODE:** CSI_HS_RCOMP_UPDATE_MODE: 00b = RCOMP is updated if the clock lane is in LP11 state. 01b = RCOMP is updated if all the data lanes are in LP11 state. 10b = RCOMP is updated immediately after calibration is completed, or the CSI[1-3]_HS_RCOMP_OVR_ENABLE bits are written to 1 by software. 11b = Reserved.
20:19	0h RW	**CSI_HS_TOGGLE_LIMIT_CREG_ENC:** CSI_HS_TOGGLE_LIMIT_CREG_ENC: HS state machine toggle limit. Number of times RCOMP state machine will toggle before exiting. 2'b00: 6 toggles; 2'b01: 4 toggles; 2'b10: 8 toggles; 2'b11: 10 toggles;
18:16	0h RW	**CSI_HS_CALIB_LOOP_DELAY:** CSI_HS_CALIB_LOOP_DELAY: Delay after applying a new RCOMP value to the AFE, before sampling the count up/down input from the AFE. 0h=)50-53ns; 1h=)60ns; 2h=)70-72ns; 3h=)80-83ns; 4h=)90ns; 5h=)100-102ns; 6h=)125-128ns; 7h=)150ns. At the start of each RCOMP calibration cycle, the state machine waits for 8x this delay before starting to sample the count up/down signal.
15:11	0h RW	**RSVD_15_11:** Reserved
10	0b RW	**CSI3_HS_RCOMP_OVR_ENABLE:** CSI3_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 3. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 3.

Bit Range	Default & Access	Description
9	0b RW	**CSI2_HS_RCOMP_OVR_ENABLE:** CSI2_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 2. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 2.
8	0b RW	**CSI1_HS_RCOMP_OVR_ENABLE:** CSI1_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 1. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 1.
7:1	0h RW	**CSI_HS_RCOMP_OVR_CODE:** CSI_HS_RCOMP_OVR_CODE: Software defined value to use as the RCOMP value for CSI[1-3] ports if the CSI[1-3]_HS_RCOMP_OVR_ENABLE fields are set.
0	1b RW	**CSI_HS_RCOMP_ENABLE:** CSI_HS_RCOMP_ENABLE: Enable CSI HS RCOMP. (Note: This bit does not affect the initial RCOMP at the de-assertion of reset which is controlled by the fuse FB_disable_initial_RCOMP.)

3.6.33 iunit_IUNIT_STATUS_type (IUNIT_STATUS)—Offset F8h

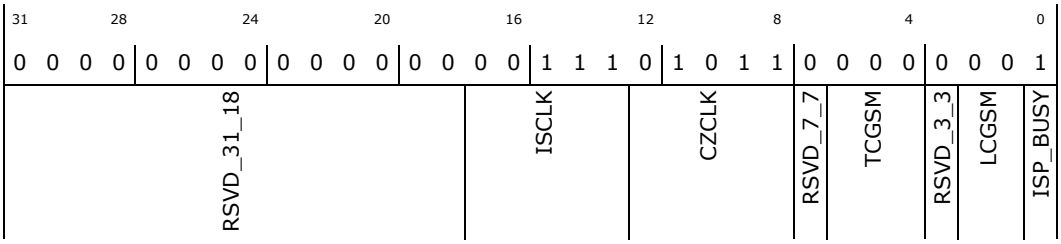
IUNIT Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_STATUS: [B:0, D:3, F:0] + F8h

Default: 0000EB01h



Bit Range	Default & Access	Description
31:18	0h RO	**RSVD_31_18:** Reserved
17:13	07h RO	**ISCLK:** Reflects the value of cck_isp_isclk_ratio_zcznfwh input pin.
12:8	0Bh RO	**CZCLK:** Reflects the value of cck_xxx_czclk_ratio_zcznfwh input pin.
7	0b RO	**RSVD_7_7:** Reserved

Bit Range	Default & Access	Description
6:4	0h RO	**TCGSM:** ISP trunk clock gating state machine. 0h = RUN_TRUNK_CLK; 1h = STOP_TRUNK_CLK; 2h = WAIT_FOR_RESUME; 3h = START_TRUNK_CLK; 4h = WAIT_FOR_LOCAL_CLK_TO_START. The reset value will be RUN_TRUNK_CLK. If the FB_override_initial_clock_gating fuse is not set, then shortly after reset, the value of this register will automatically change to STOP_TRUNK_CLK.
3	0b RO	**RSVD_3_3:** Reserved
2:1	0h RO	**LCGSM:** ISP local clock gating state machine. 0h = RUN_LOCAL_CLK; 1h = WAIT_FOR_FIFO_EMPTY; 2h = STOP_LOCAL_CLK. The reset value will be RUN_LOCAL_CLK. If the FB_override_initial_clock_gating fuse is not set, then shortly after reset, the value of this register will automatically change to STOP_LOCAL_CLK.
0	1b RO	**ISP_BUSY:** ISP_BUSY: 1 = ISP is busy; 0 = ISP is idle.

3.6.34 iunit_IUNIT_CONTROL_type (IUNIT_CONTROL)—Offset FCh

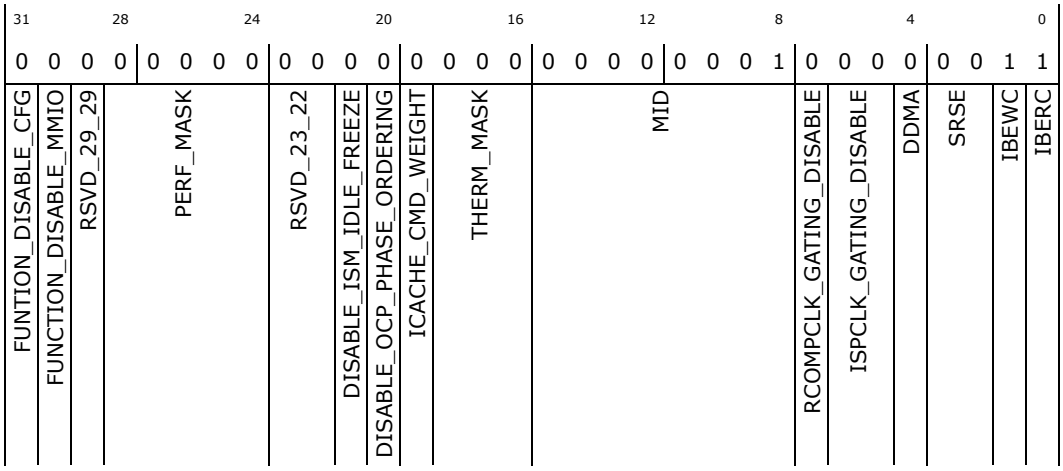
IUNIT Control Register

Access Method

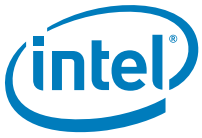
Type: PCI Configuration Register (Size: 32 bits)

IUNIT_CONTROL: [B:0, D:3, F:0] + FCh

Default: 00000103h

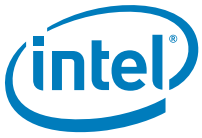


Bit Range	Default & Access	Description
31	0b RW	**FUNTION_DISABLE_CFG:** FUNCTION_DISABLE_CFG: When set, the IUNIT stops accepting any new Configuration cycle requests on the IOSF Primary bus including any new configuration cycle requests to clear this bit. Both legacy and MSI interrupts are disabled as well.



Bit Range	Default & Access	Description
30	0b RW	**FUNCTION_DISABLE_MMIO:** FUNCTION_DISABLE_MMIO: When set, the IUNIT stops accepting any new MMIO access requests on the IOSF Primary bus.
29	0b RW	**RSVD_29_29:** Reserved
28:24	0h RW	**PERF_MASK:** PERF_MASK: This field determines the amount of performance throttling applied to ispclk. The value of this field determines how many beat periods of ispclk are killed, where a beat period is defined as 16 ispclk cycles. A 16 cycle period was chosen to make the throttling independent of the actual clock ratio between ispclk and coreclk. Note that clock gating should be enabled when thermal throttling is enabled.
23:22	0h RW	**RSVD_23_22:** Reserved
21	0h RW	**DISABLE_ISM_IDLE_FREEZE:** DISABLE_ISM_IDLE_FREEZE: When IUNIT receive a RESET_WARN message from PUNIT, it will freeze the IOSF primary Idle State Machine (among other things), before sending an OK_TO_RESET message to PUNIT. If the DISABLE_ISM_IDLE_FREEZE bit is set, IUNIT will not freeze the ISM in the IDLE state as part of this reset sequence.
20	0h RW	**DISABLE_OCP_PHASE_ORDERING:** DISABLE_OCP_PHASE_ORDERING: By default, IUNIT will follow the OCP phase ordering protocol and wait until a write command is accepted before accepting the write data corresponding to that command. If the DISABLE_OCP_PHASE_ORDERING bit is set, the IUNIT wrapper will accept the write data independent of the write command.
19	0h RW	**ICACHE_CMD_WEIGHT:** ICACHE_CMD_WEIGHT: 0b = Requests from the OCP master port sending Icache miss traffic will win arbitration over requests from the OCP master port that sends pixel data traffic. 1b = Requests from the two OCP master interfaces will be accepted in a round robin fashion.
18:16	0h RW	**THERM_MASK:** THERM_MASK: This field determines the amount of thermal throttling applied to ispclk. The value of this field determines how many beat periods of ispclk are killed, where a beat period is defined as 16 ispclk cycles. A 16 cycle period was chosen to make the throttling independent of the actual clock ratio between ispclk and coreclk. 000 = No throttling; 001 = 12.5% throttling; 010 = 25% throttling; 011 = 37.5% throttling; 100 = 50% throttling; 101 = 62.5% throttling; 110 = 75% throttling; 111 = 87.5% throttling;
15:8	01h RW	**MID:** MIN_IDLE_DELAY: Minimum wait time after the rising edge of idle, before the clock gating state machine will start the sequence to gate ispclk. Range is 0 to 130 usec. Unit is 0.512 usec. Reset value of 8'h1 indicates MID = 0.512 usec.
7	0b RW	**RCOMPCLK_GATING_DISABLE:** 1 = Disable clock gating for rcompclk. 0 = Enable clock gating for rcompclk. Note: All clock gating is disabled by hardware while reset is asserted, regardless of the state of this field.
6:5	00b RW	**ISPCLK_GATING_DISABLE:** ISPCLK_GATING_DISABLE: 11 = Disable local clock gating and trunk clock gating for ispclk.; 10 = Enable local clock gating for ispclk, but disable trunk clock gating.; 01 = Reserved; 00 = Enable local clock gating and trunk clock gating for ispclk. Note: All clock gating is disabled by hardware while reset is asserted, regardless of the state of this field.

Bit Range	Default & Access	Description
4	0b RW	**DDMA:** 1 = Disable DMA. Stop sending any requests on the IB PFI port. 0 = Enable DMA. IB PFI port operates normally.
3:2	0h RW	**SRSE:** SOFT_RESET_SEQUENCE_ENABLE: If SRSE=2b00: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will a) stop accepting requests on the IOSF primary interface, b) stop accepting new requests from the OCP master interface, c) wait until read data from all earlier read requests received from the OCP master interface have been returned by SSA, d) wait until SSA reads data for all earlier PFI write requests, and e) wait for all DPHY lanes to enter stop state (LP11), and then f) send an IUNIT_OK_TO_RESET posted message to PUNIT. If SRSE=2b01: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will a) stop accepting requests on the IOSF primary interface, b) stop accepting new requests from the OCP master interface, c) wait until read data from all earlier read requests received from the OCP master interface have been returned by SSA, d) wait until SSA reads data for all earlier PFI write requests, and then e) send an IUNIT_OK_TO_RESET posted message to PUNIT. If SRSE=2b10: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will wait for all DPHY lanes to enter stop state (LP11), and then send an IUNIT_OK_TO_RESET posted message to PUNIT. If SRSE=2b11: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will immediately send an IUINT_OK_TO_RESET posted message to PUNIT.
1	1b RW	**IBEWC:** IB_ENABLE_WRITE_COMBINING: When set, enables the combining of adjacent 32-byte write requests to the same cache line. When cleared, each 32-byte write request is sent as a separate request on the IB interface.
0	1b RW	**IBERC:** IB_ENABLE_READ_COMBINING: When set, enables the combining of adjacent 32-byte read requests to the same cache line. When cleared, each 32-byte read request is sent as a separate request on the IB interface.



3.7 Image Signal Processor Memory Mapped IO Registers

Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_gpd_gp_reg_reg_gp_sdram_wakeup_type (gpd_gp_reg_reg_gp_sdram_wakeup)—Offset 0h" on page 773	00000000h
4h	4	"reg_gpd_gp_reg_reg_gp_idle_type (gpd_gp_reg_reg_gp_idle)—Offset 4h" on page 774	00000000h
8h	4	"reg_gpd_gp_reg_reg_gp_irq_req0_type (gpd_gp_reg_reg_gp_irq_req0)—Offset 8h" on page 774	00000000h
Ch	4	"reg_gpd_gp_reg_reg_gp_irq_req1_type (gpd_gp_reg_reg_gp_irq_req1)—Offset Ch" on page 775	00000000h
10h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_type (gpd_gp_reg_reg_gp_sp_stream_stat)—Offset 10h" on page 775	00022022h
14h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_type (gpd_gp_reg_reg_gp_sp_stream_stat_b)—Offset 14h" on page 779	00000000h
18h	4	"reg_gpd_gp_reg_reg_gp_isp_stream_stat_type (gpd_gp_reg_reg_gp_isp_stream_stat)—Offset 18h" on page 780	02200000h
1Ch	4	"reg_gpd_gp_reg_reg_gp_mod_stream_stat_type (gpd_gp_reg_reg_gp_mod_stream_stat)—Offset 1Ch" on page 783	AA88A222h
20h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond)—Offset 20h" on page 786	00000000h
24h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond_type (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond)—Offset 24h" on page 787	00000000h
28h	4	"reg_gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond)—Offset 28h" on page 787	00000000h
2Ch	4	"reg_gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond)—Offset 2Ch" on page 788	00000000h
30h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable)—Offset 30h" on page 789	00000000h
34h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable_type (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable)—Offset 34h" on page 790	00000000h
38h	4	"reg_gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable)—Offset 38h" on page 791	00000000h

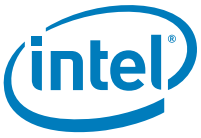


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
3Ch	4	"reg_gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable)—Offset 3Ch" on page 792	00000000h
40h	4	"reg_gpd_gp_reg_reg_gp_switch_if_type (gpd_gp_reg_reg_gp_switch_if)—Offset 40h" on page 793	00000000h
44h	4	"reg_gpd_gp_reg_reg_gp_switch_gdc1_type (gpd_gp_reg_reg_gp_switch_gdc1)—Offset 44h" on page 794	00000000h
48h	4	"reg_gpd_gp_reg_reg_gp_switch_gdc2_type (gpd_gp_reg_reg_gp_switch_gdc2)—Offset 48h" on page 794	00000000h
4Ch	4	"reg_gpd_gp_reg_reg_gp_srst_type (gpd_gp_reg_reg_gp_srst)—Offset 4Ch" on page 795	00000000h
50h	4	"reg_gpd_gp_reg_reg_gp_slv_reg_srst_type (gpd_gp_reg_reg_gp_slv_reg_srst)—Offset 50h" on page 797	00000000h
100h	4	"reg_gpd_tc_FifoWriteCmd_type (gpd_tc_FifoWriteCmd)—Offset 100h" on page 798	00000000h
400h	4	"reg_gpd_c_gpio_reg_gpio_doe_type (gpd_c_gpio_reg_gpio_doe)—Offset 400h" on page 798	00000000h
404h	4	"reg_gpd_c_gpio_reg_gpio_do_select_type (gpd_c_gpio_reg_gpio_do_select)—Offset 404h" on page 799	00000000h
408h	4	"reg_gpd_c_gpio_reg_gpio_do_0_type (gpd_c_gpio_reg_gpio_do_0)—Offset 408h" on page 800	00000000h
40Ch	4	"reg_gpd_c_gpio_reg_gpio_do_1_type (gpd_c_gpio_reg_gpio_do_1)—Offset 40Ch" on page 800	00000000h
410h	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_0_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_0)—Offset 410h" on page 801	00000000h
414h	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_1_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_1)—Offset 414h" on page 801	00000000h
418h	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_2_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_2)—Offset 418h" on page 802	00000000h
41Ch	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_3_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_3)—Offset 41Ch" on page 803	00000000h
420h	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_main_cnt_type (gpd_c_gpio_reg_gpio_do_pwm_main_cnt)—Offset 420h" on page 803	00000000h
424h	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_enable_type (gpd_c_gpio_reg_gpio_do_pwm_enable)—Offset 424h" on page 804	00000000h
428h	4	"reg_gpd_c_gpio_reg_gpio_di_debouncemethod_type (gpd_c_gpio_reg_gpio_di_debouncemethod)—Offset 428h" on page 805	00000000h

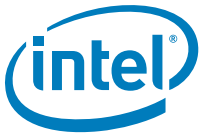


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
42Ch	4	"reg_gpd_c_gpio_reg_gpio_di_debounce_cnt0_type (gpd_c_gpio_reg_gpio_di_debounce_cnt0)—Offset 42Ch" on page 806	00000000h
430h	4	"reg_gpd_c_gpio_reg_gpio_di_debounce_cnt1_type (gpd_c_gpio_reg_gpio_di_debounce_cnt1)—Offset 430h" on page 807	00000000h
434h	4	"reg_gpd_c_gpio_reg_gpio_di_debounce_cnt2_type (gpd_c_gpio_reg_gpio_di_debounce_cnt2)—Offset 434h" on page 807	00000000h
438h	4	"reg_gpd_c_gpio_reg_gpio_di_debounce_cnt3_type (gpd_c_gpio_reg_gpio_di_debounce_cnt3)—Offset 438h" on page 808	00000000h
43Ch	4	"reg_gpd_c_gpio_reg_gpio_di_activelevel_type (gpd_c_gpio_reg_gpio_di_activelevel)—Offset 43Ch" on page 809	00000FFFh
440h	4	"reg_gpd_c_gpio_reg_gpio_di_debouncemethod_type (gpd_c_gpio_reg_gpio_di_debouncemethod)—Offset 428h" on page 805	00000FFFh
500h	4	"reg_gpd_irq_ctrl_reg_irq_edge_type (gpd_irq_ctrl_reg_irq_edge)—Offset 500h" on page 810	00000000h
504h	4	"reg_gpd_irq_ctrl_reg_irq_mask_type (gpd_irq_ctrl_reg_irq_mask)—Offset 504h" on page 810	00000000h
508h	4	"reg_gpd_irq_ctrl_reg_irq_status_type (gpd_irq_ctrl_reg_irq_status)—Offset 508h" on page 811	00000000h
50Ch	4	"reg_gpd_irq_ctrl_reg_irq_clear_type (gpd_irq_ctrl_reg_irq_clear)—Offset 50Ch" on page 813	00000000h
510h	4	"reg_gpd_irq_ctrl_reg_irq_enable_type (gpd_irq_ctrl_reg_irq_enable)—Offset 510h" on page 813	00000000h
514h	4	"reg_gpd_irq_ctrl_reg_irq_level_not_pulse_type (gpd_irq_ctrl_reg_irq_level_not_pulse)—Offset 514h" on page 814	00000000h
518h	4	"reg_gpd_irq_ctrl_reg_irq_str_out_enable_type (gpd_irq_ctrl_reg_irq_str_out_enable)—Offset 518h" on page 814	00000000h
600h	4	"reg_gpd_gptimer_reg_reset_type (gpd_gptimer_reg_reset)—Offset 600h" on page 815	00000000h
604h	4	"reg_gpd_gptimer_overall_enable_type (gpd_gptimer_overall_enable)—Offset 604h" on page 815	00000000h
608h	4	"reg_gpd_gptimer_enable_timer_0_type (gpd_gptimer_enable_timer_0)—Offset 608h" on page 816	00000000h
60Ch	4	"reg_gpd_gptimer_enable_timer_1_type (gpd_gptimer_enable_timer_1)—Offset 60Ch" on page 817	00000000h
610h	4	"reg_gpd_gptimer_enable_timer_2_type (gpd_gptimer_enable_timer_2)—Offset 610h" on page 817	00000000h

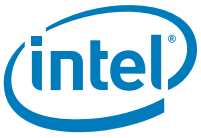


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
614h	4	"reg_gpd_gptimer_enable_timer_3_type (gpd_gptimer_enable_timer_3)—Offset 614h" on page 818	00000000h
618h	4	"reg_gpd_gptimer_enable_timer_4_type (gpd_gptimer_enable_timer_4)—Offset 618h" on page 819	00000000h
61Ch	4	"reg_gpd_gptimer_enable_timer_5_type (gpd_gptimer_enable_timer_5)—Offset 61Ch" on page 819	00000000h
620h	4	"reg_gpd_gptimer_enable_timer_6_type (gpd_gptimer_enable_timer_6)—Offset 620h" on page 820	00000000h
624h	4	"reg_gpd_gptimer_enable_timer_7_type (gpd_gptimer_enable_timer_7)—Offset 624h" on page 821	00000000h
628h	4	"reg_gpd_gptimer_value_timer_0_type (gpd_gptimer_value_timer_0)—Offset 628h" on page 821	00000000h
62Ch	4	"reg_gpd_gptimer_value_timer_1_type (gpd_gptimer_value_timer_1)—Offset 62Ch" on page 822	00000000h
630h	4	"reg_gpd_gptimer_value_timer_2_type (gpd_gptimer_value_timer_2)—Offset 630h" on page 822	00000000h
634h	4	"reg_gpd_gptimer_value_timer_3_type (gpd_gptimer_value_timer_3)—Offset 634h" on page 823	00000000h
638h	4	"reg_gpd_gptimer_value_timer_4_type (gpd_gptimer_value_timer_4)—Offset 638h" on page 823	00000000h
63Ch	4	"reg_gpd_gptimer_value_timer_5_type (gpd_gptimer_value_timer_5)—Offset 63Ch" on page 824	00000000h
640h	4	"reg_gpd_gptimer_value_timer_6_type (gpd_gptimer_value_timer_6)—Offset 640h" on page 824	00000000h
644h	4	"reg_gpd_gptimer_value_timer_7_type (gpd_gptimer_value_timer_7)—Offset 644h" on page 825	00000000h
648h	4	"reg_gpd_gptimer_count_type_timer_0_type (gpd_gptimer_count_type_timer_0)—Offset 648h" on page 825	00000000h
64Ch	4	"reg_gpd_gptimer_count_type_timer_1_type (gpd_gptimer_count_type_timer_1)—Offset 64Ch" on page 826	00000000h
650h	4	"reg_gpd_gptimer_count_type_timer_2_type (gpd_gptimer_count_type_timer_2)—Offset 650h" on page 827	00000000h
654h	4	"reg_gpd_gptimer_count_type_timer_3_type (gpd_gptimer_count_type_timer_3)—Offset 654h" on page 827	00000000h
658h	4	"reg_gpd_gptimer_count_type_timer_4_type (gpd_gptimer_count_type_timer_4)—Offset 658h" on page 828	00000000h
65Ch	4	"reg_gpd_gptimer_count_type_timer_5_type (gpd_gptimer_count_type_timer_5)—Offset 65Ch" on page 829	00000000h
660h	4	"reg_gpd_gptimer_count_type_timer_6_type (gpd_gptimer_count_type_timer_6)—Offset 660h" on page 829	00000000h
664h	4	"reg_gpd_gptimer_count_type_timer_7_type (gpd_gptimer_count_type_timer_7)—Offset 664h" on page 830	00000000h

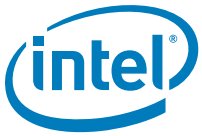


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
668h	4	"reg_gpd_gptimer_signal_select_timer_0_type (gpd_gptimer_signal_select_timer_0)—Offset 668h" on page 831	00000000h
66Ch	4	"reg_gpd_gptimer_signal_select_timer_1_type (gpd_gptimer_signal_select_timer_1)—Offset 66Ch" on page 831	00000000h
670h	4	"reg_gpd_gptimer_signal_select_timer_2_type (gpd_gptimer_signal_select_timer_2)—Offset 670h" on page 832	00000000h
674h	4	"reg_gpd_gptimer_signal_select_timer_3_type (gpd_gptimer_signal_select_timer_3)—Offset 674h" on page 833	00000000h
678h	4	"reg_gpd_gptimer_signal_select_timer_4_type (gpd_gptimer_signal_select_timer_4)—Offset 678h" on page 833	00000000h
67Ch	4	"reg_gpd_gptimer_signal_select_timer_5_type (gpd_gptimer_signal_select_timer_5)—Offset 67Ch" on page 834	00000000h
680h	4	"reg_gpd_gptimer_signal_select_timer_6_type (gpd_gptimer_signal_select_timer_6)—Offset 680h" on page 835	00000000h
684h	4	"reg_gpd_gptimer_signal_select_timer_7_type (gpd_gptimer_signal_select_timer_7)—Offset 684h" on page 835	00000000h
688h	4	"reg_gpd_gptimer_irq_trigger_value_0_type (gpd_gptimer_irq_trigger_value_0)—Offset 688h" on page 836	00000000h
68Ch	4	"reg_gpd_gptimer_irq_trigger_value_1_type (gpd_gptimer_irq_trigger_value_1)—Offset 68Ch" on page 837	00000000h
690h	4	"reg_gpd_gptimer_irq_timer_select_0_type (gpd_gptimer_irq_timer_select_0)—Offset 690h" on page 837	00000000h
694h	4	"reg_gpd_gptimer_irq_timer_select_1_type (gpd_gptimer_irq_timer_select_1)—Offset 694h" on page 838	00000000h
698h	4	"reg_gpd_gptimer_irq_enable_0_type (gpd_gptimer_irq_enable_0)—Offset 698h" on page 838	00000000h
69Ch	4	"reg_gpd_gptimer_irq_enable_1_type (gpd_gptimer_irq_enable_1)—Offset 69Ch" on page 839	00000000h
10000h	4	"reg_scp_stat_and_ctrl_type (scp_stat_and_ctrl)—Offset 10000h" on page 840	000000A0h
10004h	4	"reg_scp_base_address_type (scp_base_address)—Offset 10004h" on page 841	00000000h
10008h	4	"reg_scp_unused_2_type (scp_unused_2)—Offset 10008h" on page 841	00000000h
10010h	4	"reg_scp_base_addr_seg_0_MI_xmem_master_int_type (scp_base_addr_seg_0_MI_xmem_master_int)—Offset 10010h" on page 842	00000000h

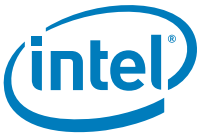


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
10014h	4	"reg_scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master_type (scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master)—Offset 10014h" on page 843	00000000h
10018h	4	"reg_scp_unused_6_type (scp_unused_6)—Offset 10018h" on page 843	00000000h
1001Ch	4	"reg_scp_unused_7_type (scp_unused_7)—Offset 1001Ch" on page 844	00000000h
10024h	4	"reg_scp_debug_pc_type (scp_debug_pc)—Offset 10024h" on page 844	00000000h
10028h	4	"reg_scp_stall_stat_fifo_loc_mt_am_inst_0_op0_type (scp_stall_stat_fifo_loc_mt_am_inst_0_op0)—Offset 10028h" on page 845	00000000h
1002Ch	4	"reg_scp_unused_11_type (scp_unused_11)—Offset 1002Ch" on page 846	00000000h
10030h	4	"reg_scp_pmem_slave_access_type (scp_pmem_slave_access)—Offset 10030h" on page 847	00000000h
20000h	4	"reg_isp_stat_and_ctrl_type (isp_stat_and_ctrl)—Offset 20000h" on page 847	000000A0h
20004h	4	"reg_isp_base_address_type (isp_base_address)—Offset 20004h" on page 849	00000000h
20008h	4	"reg_isp_unused_2_type (isp_unused_2)—Offset 20008h" on page 849	00000000h
20010h	4	"reg_isp_base_addr_seg_0_MI_base_config_mem_master_type (isp_base_addr_seg_0_MI_base_config_mem_master)—Offset 20010h" on page 850	00000000h
20014h	4	"reg_isp_unused_5_type (isp_unused_5)—Offset 20014h" on page 851	00000000h
2001Ch	4	"reg_isp_debug_pc_type (isp_debug_pc)—Offset 2001Ch" on page 851	00000000h
20020h	4	"reg_isp_stall_stat_base_config_mem_iam_op0_type (isp_stall_stat_base_config_mem_iam_op0)—Offset 20020h" on page 852	00000000h
20024h	4	"reg_isp_unused_9_type (isp_unused_9)—Offset 20024h" on page 853	00000000h
20028h	4	"reg_isp_pmem_slave_access_type (isp_pmem_slave_access)—Offset 20028h" on page 853	00000000h
30000h	4	"reg_ifmt_ift_prim_IF_sw_rst_type (ifmt_ift_prim_IF_sw_rst)—Offset 30000h" on page 854	00000000h
30004h	4	"reg_ifmt_ift_prim_IF_start_line_type (ifmt_ift_prim_IF_start_line)—Offset 30004h" on page 855	00000000h
30008h	4	"reg_ifmt_ift_prim_IF_start_column_type (ifmt_ift_prim_IF_start_column)—Offset 30008h" on page 855	00000000h

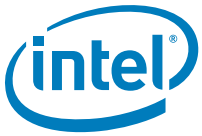


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
3000Ch	4	"reg_ifmt_ift_prim_IF_Cropped_height_type (ifmt_ift_prim_IF_Cropped_height)—Offset 3000Ch" on page 856	00000000h
30010h	4	"reg_ifmt_ift_prim_IF_Cropped_width_type (ifmt_ift_prim_IF_Cropped_width)—Offset 30010h" on page 856	00000000h
30014h	4	"reg_ifmt_ift_prim_IF_Vert_Decim_type (ifmt_ift_prim_IF_Vert_Decim)—Offset 30014h" on page 857	00000000h
30018h	4	"reg_ifmt_ift_prim_IF_Horiz_Decim_type (ifmt_ift_prim_IF_Horiz_Decim)—Offset 30018h" on page 858	00000000h
3001Ch	4	"reg_ifmt_ift_prim_IF_Horiz_Deinter_type (ifmt_ift_prim_IF_Horiz_Deinter)—Offset 3001Ch" on page 858	00000000h
30020h	4	"reg_ifmt_ift_prim_IF_Left_Pad_type (ifmt_ift_prim_IF_Left_Pad)—Offset 30020h" on page 859	00000000h
30024h	4	"reg_ifmt_ift_prim_IF_EOF_Offset_type (ifmt_ift_prim_IF_EOF_Offset)—Offset 30024h" on page 860	00000000h
30028h	4	"reg_ifmt_ift_prim_IF_Start_addr_type (ifmt_ift_prim_IF_Start_addr)—Offset 30028h" on page 860	00000000h
3002Ch	4	"reg_ifmt_ift_prim_IF_End_addr_type (ifmt_ift_prim_IF_End_addr)—Offset 3002Ch" on page 861	00000000h
30030h	4	"reg_ifmt_ift_prim_IF_incr_type (ifmt_ift_prim_IF_incr)—Offset 30030h" on page 861	00000000h
30034h	4	"reg_ifmt_ift_prim_IF_YUV_420_format_type (ifmt_ift_prim_IF_YUV_420_format)—Offset 30034h" on page 862	00000000h
30038h	4	"reg_ifmt_ift_prim_IF_Vsynch_active_low_type (ifmt_ift_prim_IF_Vsynch_active_low)—Offset 30038h" on page 863	00000000h
3003Ch	4	"reg_ifmt_ift_prim_IF_Hsynch_active_low_type (ifmt_ift_prim_IF_Hsynch_active_low)—Offset 3003Ch" on page 863	00000000h
30040h	4	"reg_ifmt_ift_prim_IF_ReEnable_type (ifmt_ift_prim_IF_ReEnable)—Offset 30040h" on page 864	00000000h
30044h	4	"reg_ifmt_ift_prim_IF_block_input_type (ifmt_ift_prim_IF_block_input)—Offset 30044h" on page 865	00000000h
30048h	4	"reg_ifmt_ift_prim_IF_Vert_Deinter_type (ifmt_ift_prim_IF_Vert_Deinter)—Offset 30048h" on page 865	00000000h
30100h	4	"reg_ifmt_ift_prim_IF_FSM_Sync_status_type (ifmt_ift_prim_IF_FSM_Sync_status)—Offset 30100h" on page 866	00000000h
30104h	4	"reg_ifmt_ift_prim_FSM_Sync_counter_type (ifmt_ift_prim_FSM_Sync_counter)—Offset 30104h" on page 867	00000000h
30108h	4	"reg_ifmt_ift_prim_FSM_Crop_status_type (ifmt_ift_prim_FSM_Crop_status)—Offset 30108h" on page 867	00000000h

Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
3010Ch	4	"reg_ifmt_ift_prim_FSM_Crop_line_counter_type (ifmt_ift_prim_FSM_Crop_line_counter)—Offset 3010Ch" on page 868	00000000h
30110h	4	"reg_ifmt_ift_prim_FSM_Crop_pixel_counter_type (ifmt_ift_prim_FSM_Crop_pixel_counter)—Offset 30110h" on page 869	00000000h
30114h	4	"reg_ifmt_ift_prim_FSM_Deinterl_idx_buffer_type (ifmt_ift_prim_FSM_Deinterl_idx_buffer)—Offset 30114h" on page 870	00000000h
30118h	4	"reg_ifmt_ift_prim_FSM_Horiz_Decim_cnt_type (ifmt_ift_prim_FSM_Horiz_Decim_cnt)—Offset 30118h" on page 870	00000000h
3011Ch	4	"reg_ifmt_ift_prim_FSM_Vertic_Decim_cnt_type (ifmt_ift_prim_FSM_Vertic_Decim_cnt)—Offset 3011Ch" on page 871	00000000h
30120h	4	"reg_ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt)—Offset 30120h" on page 872	00000000h
30124h	4	"reg_ifmt_ift_prim_IF_FSM_Padding_status_type (ifmt_ift_prim_IF_FSM_Padding_status)—Offset 30124h" on page 872	00000000h
30128h	4	"reg_ifmt_ift_prim_IF_FSM_Padding_elem_idx_type (ifmt_ift_prim_IF_FSM_Padding_elem_idx)—Offset 30128h" on page 873	00000000h
3012Ch	4	"reg_ifmt_ift_prim_IF_FSM_Vec_Sup_type (ifmt_ift_prim_IF_FSM_Vec_Sup)—Offset 3012Ch" on page 874	00000000h
30130h	4	"reg_ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full)—Offset 30130h" on page 875	00000000h
30134h	4	"reg_ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept)—Offset 30134h" on page 875	00000001h
30138h	4	"reg_ifmt_ift_prim_IF_Pixel_Fifo_status_type (ifmt_ift_prim_IF_Pixel_Fifo_status)—Offset 30138h" on page 876	00000001h
30200h	4	"reg_ifmt_ift_prim_b_IF_sw_rst_type (ifmt_ift_prim_b_IF_sw_rst)—Offset 30200h" on page 877	00000000h
30204h	4	"reg_ifmt_ift_prim_b_IF_start_line_type (ifmt_ift_prim_b_IF_start_line)—Offset 30204h" on page 878	00000000h
30208h	4	"reg_ifmt_ift_prim_b_IF_start_column_type (ifmt_ift_prim_b_IF_start_column)—Offset 30208h" on page 878	00000000h
3020Ch	4	"reg_ifmt_ift_prim_b_IF_Cropped_height_type (ifmt_ift_prim_b_IF_Cropped_height)—Offset 3020Ch" on page 879	00000000h

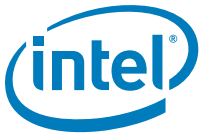


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
30210h	4	"reg_ifmt_ift_prim_b_IF_Cropped_width_type (ifmt_ift_prim_b_IF_Cropped_width)—Offset 30210h" on page 880	00000000h
30214h	4	"reg_ifmt_ift_prim_b_IF_Vert_Decim_type (ifmt_ift_prim_b_IF_Vert_Decim)—Offset 30214h" on page 880	00000000h
30218h	4	"reg_ifmt_ift_prim_b_IF_Horiz_Decim_type (ifmt_ift_prim_b_IF_Horiz_Decim)—Offset 30218h" on page 881	00000000h
3021Ch	4	"reg_ifmt_ift_prim_b_IF_Horiz_Deinter_type (ifmt_ift_prim_b_IF_Horiz_Deinter)—Offset 3021Ch" on page 882	00000000h
30220h	4	"reg_ifmt_ift_prim_b_IF_Left_Pad_type (ifmt_ift_prim_b_IF_Left_Pad)—Offset 30220h" on page 882	00000000h
30224h	4	"reg_ifmt_ift_prim_b_IF_EOF_Offset_type (ifmt_ift_prim_b_IF_EOF_Offset)—Offset 30224h" on page 883	00000000h
30228h	4	"reg_ifmt_ift_prim_b_IF_Start_addr_type (ifmt_ift_prim_b_IF_Start_addr)—Offset 30228h" on page 883	00000000h
3022Ch	4	"reg_ifmt_ift_prim_b_IF_End_addr_type (ifmt_ift_prim_b_IF_End_addr)—Offset 3022Ch" on page 884	00000000h
30230h	4	"reg_ifmt_ift_prim_b_IF_incr_type (ifmt_ift_prim_b_IF_incr)—Offset 30230h" on page 885	00000000h
30234h	4	"reg_ifmt_ift_prim_b_IF_YUV_420_format_type (ifmt_ift_prim_b_IF_YUV_420_format)—Offset 30234h" on page 885	00000000h
30238h	4	"reg_ifmt_ift_prim_b_IF_Vsynch_active_low_type (ifmt_ift_prim_b_IF_Vsynch_active_low)—Offset 30238h" on page 886	00000000h
3023Ch	4	"reg_ifmt_ift_prim_b_IF_Hsynch_active_low_type (ifmt_ift_prim_b_IF_Hsynch_active_low)—Offset 3023Ch" on page 886	00000000h
30240h	4	"reg_ifmt_ift_prim_b_IF_ReEnable_type (ifmt_ift_prim_b_IF_ReEnable)—Offset 30240h" on page 887	00000000h
30244h	4	"reg_ifmt_ift_prim_b_IF_block_input_type (ifmt_ift_prim_b_IF_block_input)—Offset 30244h" on page 888	00000000h
30248h	4	"reg_ifmt_ift_prim_b_IF_Vert_Deinter_type (ifmt_ift_prim_b_IF_Vert_Deinter)—Offset 30248h" on page 888	00000000h
30300h	4	"reg_ifmt_ift_prim_b_IF_FSM_Sync_status_type (ifmt_ift_prim_b_IF_FSM_Sync_status)—Offset 30300h" on page 889	00000000h
30304h	4	"reg_ifmt_ift_prim_b_FSM_Sync_counter_type (ifmt_ift_prim_b_FSM_Sync_counter)—Offset 30304h" on page 890	00000000h
30308h	4	"reg_ifmt_ift_prim_b_FSM_Crop_status_type (ifmt_ift_prim_b_FSM_Crop_status)—Offset 30308h" on page 890	00000000h

Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
3030Ch	4	"reg_ifmt_ift_prim_b_FSM_Crop_line_counter_type (ifmt_ift_prim_b_FSM_Crop_line_counter)—Offset 3030Ch" on page 891	00000000h
30310h	4	"reg_ifmt_ift_prim_b_FSM_Crop_pixel_counter_type (ifmt_ift_prim_b_FSM_Crop_pixel_counter)—Offset 30310h" on page 892	00000000h
30314h	4	"reg_ifmt_ift_prim_b_FSM_Deinterl_idx_buffer_type (ifmt_ift_prim_b_FSM_Deinterl_idx_buffer)—Offset 30314h" on page 893	00000000h
30318h	4	"reg_ifmt_ift_prim_b_FSM_Horiz_Decim_cnt_type (ifmt_ift_prim_b_FSM_Horiz_Decim_cnt)—Offset 30318h" on page 893	00000000h
3031Ch	4	"reg_ifmt_ift_prim_b_FSM_Vertic_Decim_cnt_type (ifmt_ift_prim_b_FSM_Vertic_Decim_cnt)—Offset 3031Ch" on page 894	00000000h
30320h	4	"reg_ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt)—Offset 30320h" on page 895	00000000h
30324h	4	"reg_ifmt_ift_prim_b_IF_FSM_Padding_status_type (ifmt_ift_prim_b_IF_FSM_Padding_status)—Offset 30324h" on page 896	00000000h
30328h	4	"reg_ifmt_ift_prim_b_IF_FSM_Padding_elem_idx_type (ifmt_ift_prim_b_IF_FSM_Padding_elem_idx)—Offset 30328h" on page 897	00000000h
3032Ch	4	"reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup)—Offset 3032Ch" on page 897	00000000h
30330h	4	"reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full)—Offset 30330h" on page 898	00000000h
30334h	4	"reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept)—Offset 30334h" on page 899	00000001h
30338h	4	"reg_ifmt_ift_prim_b_IF_Pixel_Fifo_status_type (ifmt_ift_prim_b_IF_Pixel_Fifo_status)—Offset 30338h" on page 899	00000001h
30400h	4	"reg_ifmt_ift_sec_IF_sw_rst_type (ifmt_ift_sec_IF_sw_rst)—Offset 30400h" on page 900	00000000h
30404h	4	"reg_ifmt_ift_sec_IF_start_line_type (ifmt_ift_sec_IF_start_line)—Offset 30404h" on page 901	00000000h
30408h	4	"reg_ifmt_ift_sec_IF_start_column_type (ifmt_ift_sec_IF_start_column)—Offset 30408h" on page 902	00000000h
3040Ch	4	"reg_ifmt_ift_sec_IF_Cropped_height_type (ifmt_ift_sec_IF_Cropped_height)—Offset 3040Ch" on page 902	00000000h

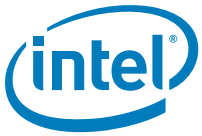


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
30410h	4	"reg_ifmt_ift_sec_IF_Cropped_width_type (ifmt_ift_sec_IF_Cropped_width)—Offset 30410h" on page 903	00000000h
30414h	4	"reg_ifmt_ift_sec_IF_Vert_Decim_type (ifmt_ift_sec_IF_Vert_Decim)—Offset 30414h" on page 904	00000000h
30418h	4	"reg_ifmt_ift_sec_IF_Horiz_Decim_type (ifmt_ift_sec_IF_Horiz_Decim)—Offset 30418h" on page 904	00000000h
3041Ch	4	"reg_ifmt_ift_sec_IF_Horiz_Deinter_type (ifmt_ift_sec_IF_Horiz_Deinter)—Offset 3041Ch" on page 905	00000000h
30420h	4	"reg_ifmt_ift_sec_IF_Left_Pad_type (ifmt_ift_sec_IF_Left_Pad)—Offset 30420h" on page 906	00000000h
30424h	4	"reg_ifmt_ift_sec_IF_EOF_Offset_type (ifmt_ift_sec_IF_EOF_Offset)—Offset 30424h" on page 906	00000000h
30428h	4	"reg_ifmt_ift_sec_IF_Start_addr_type (ifmt_ift_sec_IF_Start_addr)—Offset 30428h" on page 907	00000000h
3042Ch	4	"reg_ifmt_ift_sec_IF_End_addr_type (ifmt_ift_sec_IF_End_addr)—Offset 3042Ch" on page 907	00000000h
30430h	4	"reg_ifmt_ift_sec_IF_incr_type (ifmt_ift_sec_IF_incr)—Offset 30430h" on page 908	00000000h
30434h	4	"reg_ifmt_ift_sec_IF_YUV_420_format_type (ifmt_ift_sec_IF_YUV_420_format)—Offset 30434h" on page 908	00000000h
30438h	4	"reg_ifmt_ift_sec_IF_Vsynch_active_low_type (ifmt_ift_sec_IF_Vsynch_active_low)—Offset 30438h" on page 909	00000000h
3043Ch	4	"reg_ifmt_ift_sec_IF_Hsynch_active_low_type (ifmt_ift_sec_IF_Hsynch_active_low)—Offset 3043Ch" on page 910	00000000h
30440h	4	"reg_ifmt_ift_sec_IF_ReEnable_type (ifmt_ift_sec_IF_ReEnable)—Offset 30440h" on page 911	00000000h
30444h	4	"reg_ifmt_ift_sec_IF_block_input_type (ifmt_ift_sec_IF_block_input)—Offset 30444h" on page 911	00000000h
30448h	4	"reg_ifmt_ift_sec_IF_Vert_Deinter_type (ifmt_ift_sec_IF_Vert_Deinter)—Offset 30448h" on page 912	00000000h
30500h	4	"reg_ifmt_ift_sec_IF_FSM_Sync_status_type (ifmt_ift_sec_IF_FSM_Sync_status)—Offset 30500h" on page 913	00000000h
30504h	4	"reg_ifmt_ift_sec_FSM_Sync_counter_type (ifmt_ift_sec_FSM_Sync_counter)—Offset 30504h" on page 913	00000000h
30508h	4	"reg_ifmt_ift_sec_FSM_Crop_status_type (ifmt_ift_sec_FSM_Crop_status)—Offset 30508h" on page 914	00000000h
3050Ch	4	"reg_ifmt_ift_sec_FSM_Crop_line_counter_type (ifmt_ift_sec_FSM_Crop_line_counter)—Offset 3050Ch" on page 915	00000000h

Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
30510h	4	"reg_ifmt_ift_sec_FSM_Crop_pixel_counter_type (ifmt_ift_sec_FSM_Crop_pixel_counter)—Offset 30510h" on page 915	00000000h
30514h	4	"reg_ifmt_ift_sec_FSM_Deinterl_idx_buffer_type (ifmt_ift_sec_FSM_Deinterl_idx_buffer)—Offset 30514h" on page 916	00000000h
30518h	4	"reg_ifmt_ift_sec_FSM_Horiz_Decim_cnt_type (ifmt_ift_sec_FSM_Horiz_Decim_cnt)—Offset 30518h" on page 917	00000000h
3051Ch	4	"reg_ifmt_ift_sec_FSM_Vertic_Decim_cnt_type (ifmt_ift_sec_FSM_Vertic_Decim_cnt)—Offset 3051Ch" on page 918	00000000h
30520h	4	"reg_ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt)—Offset 30520h" on page 918	00000000h
30524h	4	"reg_ifmt_ift_sec_IF_FSM_Padding_status_type (ifmt_ift_sec_IF_FSM_Padding_status)—Offset 30524h" on page 919	00000000h
30528h	4	"reg_ifmt_ift_sec_IF_FSM_Padding_elem_idx_type (ifmt_ift_sec_IF_FSM_Padding_elem_idx)—Offset 30528h" on page 920	00000000h
3052Ch	4	"reg_ifmt_ift_sec_IF_FSM_Vec_Sup_type (ifmt_ift_sec_IF_FSM_Vec_Sup)—Offset 3052Ch" on page 921	00000000h
30530h	4	"reg_ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full)—Offset 30530h" on page 922	00000000h
30534h	4	"reg_ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept)—Offset 30534h" on page 922	00000001h
30538h	4	"reg_ifmt_ift_sec_IF_Pixel_Fifo_status_type (ifmt_ift_sec_IF_Pixel_Fifo_status)—Offset 30538h" on page 923	00000001h
30600h	4	"reg_ifmt_mem_cpy_MemCopy_sw_rst_type (ifmt_mem_cpy_MemCopy_sw_rst)—Offset 30600h" on page 924	00000000h
30604h	4	"reg_ifmt_mem_cpy_MemCopy_in_endian_type (ifmt_mem_cpy_MemCopy_in_endian)—Offset 30604h" on page 925	00000000h
30608h	4	"reg_ifmt_mem_cpy_MemCopy_out_endian_type (ifmt_mem_cpy_MemCopy_out_endian)—Offset 30608h" on page 925	00000000h
3060Ch	4	"reg_ifmt_mem_cpy_MemCopy_bit_swap_type (ifmt_mem_cpy_MemCopy_bit_swap)—Offset 3060Ch" on page 926	00000000h
30610h	4	"reg_ifmt_mem_cpy_MemCopy_block_synch_type (ifmt_mem_cpy_MemCopy_block_synch)—Offset 30610h" on page 927	00000000h

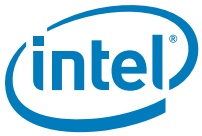


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
30614h	4	"reg_ifmt_mem_cpy_MemCopy_packet_synch_type (ifmt_mem_cpy_MemCopy_packet_synch)—Offset 30614h" on page 927	00000000h
30618h	4	"reg_ifmt_mem_cpy_MemCopy_rd_post_wr_sync_type (ifmt_mem_cpy_MemCopy_rd_post_wr_sync)—Offset 30618h" on page 928	00000000h
3061Ch	4	"reg_ifmt_mem_cpy_MemCopy_dual_input_type (ifmt_mem_cpy_MemCopy_dual_input)—Offset 3061Ch" on page 929	00000000h
30620h	4	"reg_ifmt_mem_cpy_MemCopy_ReEnable_type (ifmt_mem_cpy_MemCopy_ReEnable)—Offset 30620h" on page 929	00000000h
30700h	4	"reg_ifmt_mem_cpy_MemCopy_token_data_type (ifmt_mem_cpy_MemCopy_token_data)—Offset 30700h" on page 930	00000000h
30704h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Sync_status_type (ifmt_mem_cpy_MemCopy_FSM_Sync_status)—Offset 30704h" on page 931	00000000h
30708h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt)—Offset 30708h" on page 931	00000000h
3070Ch	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt)—Offset 3070Ch" on page 932	00000000h
30710h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt)—Offset 30710h" on page 933	00000000h
30714h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status_type (ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status)—Offset 30714h" on page 934	00000000h
30718h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt)—Offset 30718h" on page 935	00000000h
3071Ch	4	"reg_ifmt_mem_cpy_MemCopy_FSM_CioWr_status_type (ifmt_mem_cpy_MemCopy_FSM_CioWr_status)—Offset 3071Ch" on page 936	00000004h
30720h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_CioWr_addr_type (ifmt_mem_cpy_MemCopy_FSM_CioWr_addr)—Offset 30720h" on page 937	00000000h
30800h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg0_type (ifmt_gp_reg_IFMT_input_switch_lut_reg0)—Offset 30800h" on page 938	00000000h
30804h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg1_type (ifmt_gp_reg_IFMT_input_switch_lut_reg1)—Offset 30804h" on page 939	00000000h

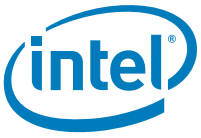


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
30808h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg2_type (ifmt_gp_reg_IFMT_input_switch_lut_reg2)—Offset 30808h" on page 939	00000000h
3080Ch	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg3_type (ifmt_gp_reg_IFMT_input_switch_lut_reg3)—Offset 3080Ch" on page 940	00000000h
30810h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg4_type (ifmt_gp_reg_IFMT_input_switch_lut_reg4)—Offset 30810h" on page 941	00000000h
30814h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg5_type (ifmt_gp_reg_IFMT_input_switch_lut_reg5)—Offset 30814h" on page 941	00000000h
30818h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg6_type (ifmt_gp_reg_IFMT_input_switch_lut_reg6)—Offset 30818h" on page 942	00000000h
3081Ch	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg7_type (ifmt_gp_reg_IFMT_input_switch_lut_reg7)—Offset 3081Ch" on page 943	00000000h
30820h	4	"reg_ifmt_gp_reg_IFMT_input_switch_fsync_lut_type (ifmt_gp_reg_IFMT_input_switch_fsync_lut)—Offset 30820h" on page 943	00000000h
30824h	4	"reg_ifmt_gp_reg_IFMT_srst_type (ifmt_gp_reg_IFMT_srst)—Offset 30824h" on page 944	00000000h
30828h	4	"reg_ifmt_gp_reg_IFMT_slv_reg_srst_type (ifmt_gp_reg_IFMT_slv_reg_srst)—Offset 30828h" on page 945	00000000h
3082Ch	4	"reg_ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type_type (ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type)—Offset 3082Ch" on page 946	00000000h
30A00h	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge)—Offset 30A00h" on page 947	00000000h
30A04h	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask)—Offset 30A04h" on page 947	00000000h
30A08h	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_status_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_status)—Offset 30A08h" on page 948	00000000h
30A0Ch	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear)—Offset 30A0Ch" on page 949	00000000h
30A10h	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable)—Offset 30A10h" on page 950	00000000h
30A14h	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse)—Offset 30A14h" on page 950	00000000h

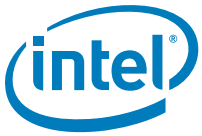


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
40000h	4	"reg_isp_dma_DMA_FSM_Command_type (isp_dma_DMA_FSM_Command)—Offset 40000h" on page 951	00000001h
41000h	4	"reg_isp_dma_DMA_CH0_Packing_setup_type (isp_dma_DMA_CH0_Packing_setup)—Offset 41000h" on page 952	00000000h
41004h	4	"reg_isp_dma_DMA_CH1_Packing_setup_type (isp_dma_DMA_CH1_Packing_setup)—Offset 41004h" on page 953	00000000h
41008h	4	"reg_isp_dma_DMA_CH2_Packing_setup_type (isp_dma_DMA_CH2_Packing_setup)—Offset 41008h" on page 953	00000000h
4100Ch	4	"reg_isp_dma_DMA_CH3_Packing_setup_type (isp_dma_DMA_CH3_Packing_setup)—Offset 4100Ch" on page 954	00000000h
41010h	4	"reg_isp_dma_DMA_CH4_Packing_setup_type (isp_dma_DMA_CH4_Packing_setup)—Offset 41010h" on page 955	00000000h
41014h	4	"reg_isp_dma_DMA_CH5_Packing_setup_type (isp_dma_DMA_CH5_Packing_setup)—Offset 41014h" on page 956	00000000h
41018h	4	"reg_isp_dma_DMA_CH6_Packing_setup_type (isp_dma_DMA_CH6_Packing_setup)—Offset 41018h" on page 957	00000000h
4101Ch	4	"reg_isp_dma_DMA_CH7_Packing_setup_type (isp_dma_DMA_CH7_Packing_setup)—Offset 4101Ch" on page 958	00000000h
41020h	4	"reg_isp_dma_DMA_CH8_Packing_setup_type (isp_dma_DMA_CH8_Packing_setup)—Offset 41020h" on page 959	00000000h
41024h	4	"reg_isp_dma_DMA_CH9_Packing_setup_type (isp_dma_DMA_CH9_Packing_setup)—Offset 41024h" on page 960	00000000h
41028h	4	"reg_isp_dma_DMA_CH10_Packing_setup_type (isp_dma_DMA_CH10_Packing_setup)—Offset 41028h" on page 961	00000000h
4102Ch	4	"reg_isp_dma_DMA_CH11_Packing_setup_type (isp_dma_DMA_CH11_Packing_setup)—Offset 4102Ch" on page 962	00000000h
41030h	4	"reg_isp_dma_DMA_CH12_Packing_setup_type (isp_dma_DMA_CH12_Packing_setup)—Offset 41030h" on page 963	00000000h
41034h	4	"reg_isp_dma_DMA_CH13_Packing_setup_type (isp_dma_DMA_CH13_Packing_setup)—Offset 41034h" on page 964	00000000h

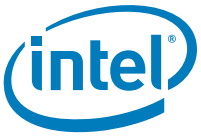


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41038h	4	"reg_isp_dma_DMA_CH14_Packing_setup_type (isp_dma_DMA_CH14_Packing_setup)—Offset 41038h" on page 965	00000000h
4103Ch	4	"reg_isp_dma_DMA_CH15_Packing_setup_type (isp_dma_DMA_CH15_Packing_setup)—Offset 4103Ch" on page 966	00000000h
41040h	4	"reg_isp_dma_DMA_CH16_Packing_setup_type (isp_dma_DMA_CH16_Packing_setup)—Offset 41040h" on page 967	00000000h
41044h	4	"reg_isp_dma_DMA_CH17_Packing_setup_type (isp_dma_DMA_CH17_Packing_setup)—Offset 41044h" on page 968	00000000h
41048h	4	"reg_isp_dma_DMA_CH18_Packing_setup_type (isp_dma_DMA_CH18_Packing_setup)—Offset 41048h" on page 969	00000000h
4104Ch	4	"reg_isp_dma_DMA_CH19_Packing_setup_type (isp_dma_DMA_CH19_Packing_setup)—Offset 4104Ch" on page 970	00000000h
41050h	4	"reg_isp_dma_DMA_CH20_Packing_setup_type (isp_dma_DMA_CH20_Packing_setup)—Offset 41050h" on page 971	00000000h
41054h	4	"reg_isp_dma_DMA_CH21_Packing_setup_type (isp_dma_DMA_CH21_Packing_setup)—Offset 41054h" on page 972	00000000h
41058h	4	"reg_isp_dma_DMA_CH22_Packing_setup_type (isp_dma_DMA_CH22_Packing_setup)—Offset 41058h" on page 973	00000000h
4105Ch	4	"reg_isp_dma_DMA_CH23_Packing_setup_type (isp_dma_DMA_CH23_Packing_setup)—Offset 4105Ch" on page 974	00000000h
41060h	4	"reg_isp_dma_DMA_CH24_Packing_setup_type (isp_dma_DMA_CH24_Packing_setup)—Offset 41060h" on page 975	00000000h
41064h	4	"reg_isp_dma_DMA_CH25_Packing_setup_type (isp_dma_DMA_CH25_Packing_setup)—Offset 41064h" on page 976	00000000h
41068h	4	"reg_isp_dma_DMA_CH26_Packing_setup_type (isp_dma_DMA_CH26_Packing_setup)—Offset 41068h" on page 977	00000000h
41070h	4	"reg_isp_dma_DMA_CH28_Packing_setup_type (isp_dma_DMA_CH28_Packing_setup)—Offset 41070h" on page 978	00000000h
41074h	4	"reg_isp_dma_DMA_CH29_Packing_setup_type (isp_dma_DMA_CH29_Packing_setup)—Offset 41074h" on page 979	00000000h

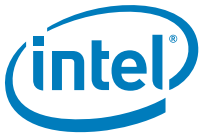


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41078h	4	"reg_isp_dma_DMA_CH30_Packing_setup_type (isp_dma_DMA_CH30_Packing_setup)—Offset 41078h" on page 980	00000000h
4107Ch	4	"reg_isp_dma_DMA_CH31_Packing_setup_type (isp_dma_DMA_CH31_Packing_setup)—Offset 4107Ch" on page 981	00000000h
41100h	4	"reg_isp_dma_DMA_CH0_dev_stride_A_type (isp_dma_DMA_CH0_dev_stride_A)—Offset 41100h" on page 982	00000000h
41104h	4	"reg_isp_dma_DMA_CH1_dev_stride_A_type (isp_dma_DMA_CH1_dev_stride_A)—Offset 41104h" on page 983	00000000h
41108h	4	"reg_isp_dma_DMA_CH2_dev_stride_A_type (isp_dma_DMA_CH2_dev_stride_A)—Offset 41108h" on page 983	00000000h
4110Ch	4	"reg_isp_dma_DMA_CH3_dev_stride_A_type (isp_dma_DMA_CH3_dev_stride_A)—Offset 4110Ch" on page 984	00000000h
41110h	4	"reg_isp_dma_DMA_CH4_dev_stride_A_type (isp_dma_DMA_CH4_dev_stride_A)—Offset 41110h" on page 984	00000000h
41114h	4	"reg_isp_dma_DMA_CH5_dev_stride_A_type (isp_dma_DMA_CH5_dev_stride_A)—Offset 41114h" on page 985	00000000h
41118h	4	"reg_isp_dma_DMA_CH6_dev_stride_A_type (isp_dma_DMA_CH6_dev_stride_A)—Offset 41118h" on page 986	00000000h
4111Ch	4	"reg_isp_dma_DMA_CH7_dev_stride_A_type (isp_dma_DMA_CH7_dev_stride_A)—Offset 4111Ch" on page 986	00000000h
41120h	4	"reg_isp_dma_DMA_CH8_dev_stride_A_type (isp_dma_DMA_CH8_dev_stride_A)—Offset 41120h" on page 987	00000000h
41124h	4	"reg_isp_dma_DMA_CH9_dev_stride_A_type (isp_dma_DMA_CH9_dev_stride_A)—Offset 41124h" on page 987	00000000h
41128h	4	"reg_isp_dma_DMA_CH10_dev_stride_A_type (isp_dma_DMA_CH10_dev_stride_A)—Offset 41128h" on page 988	00000000h
4112Ch	4	"reg_isp_dma_DMA_CH11_dev_stride_A_type (isp_dma_DMA_CH11_dev_stride_A)—Offset 4112Ch" on page 988	00000000h
41130h	4	"reg_isp_dma_DMA_CH12_dev_stride_A_type (isp_dma_DMA_CH12_dev_stride_A)—Offset 41130h" on page 989	00000000h

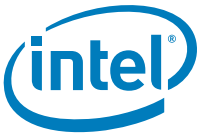


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41134h	4	"reg_isp_dma_DMA_CH13_dev_stride_A_type (isp_dma_DMA_CH13_dev_stride_A)—Offset 41134h" on page 990	00000000h
41138h	4	"reg_isp_dma_DMA_CH14_dev_stride_A_type (isp_dma_DMA_CH14_dev_stride_A)—Offset 41138h" on page 990	00000000h
4113Ch	4	"reg_isp_dma_DMA_CH15_dev_stride_A_type (isp_dma_DMA_CH15_dev_stride_A)—Offset 4113Ch" on page 991	00000000h
41140h	4	"reg_isp_dma_DMA_CH16_dev_stride_A_type (isp_dma_DMA_CH16_dev_stride_A)—Offset 41140h" on page 992	00000000h
41144h	4	"reg_isp_dma_DMA_CH17_dev_stride_A_type (isp_dma_DMA_CH17_dev_stride_A)—Offset 41144h" on page 992	00000000h
41148h	4	"reg_isp_dma_DMA_CH18_dev_stride_A_type (isp_dma_DMA_CH18_dev_stride_A)—Offset 41148h" on page 993	00000000h
4114Ch	4	"reg_isp_dma_DMA_CH19_dev_stride_A_type (isp_dma_DMA_CH19_dev_stride_A)—Offset 4114Ch" on page 993	00000000h
41150h	4	"reg_isp_dma_DMA_CH20_dev_stride_A_type (isp_dma_DMA_CH20_dev_stride_A)—Offset 41150h" on page 994	00000000h
41154h	4	"reg_isp_dma_DMA_CH21_dev_stride_A_type (isp_dma_DMA_CH21_dev_stride_A)—Offset 41154h" on page 995	00000000h
41200h	4	"reg_isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A)—Offset 41200h" on page 995	00000000h
41204h	4	"reg_isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_A)—Offset 41204h" on page 996	00000000h
41208h	4	"reg_isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_A)—Offset 41208h" on page 997	00000000h
4120Ch	4	"reg_isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_A)—Offset 4120Ch" on page 998	00000000h
41210h	4	"reg_isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_A)—Offset 41210h" on page 999	00000000h
41214h	4	"reg_isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_A)—Offset 41214h" on page 1000	00000000h

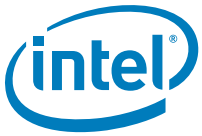


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41218h	4	"reg_isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_A)—Offset 41218h" on page 1001	00000000h
4121Ch	4	"reg_isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_A)—Offset 4121Ch" on page 1002	00000000h
41220h	4	"reg_isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_A)—Offset 41220h" on page 1003	00000000h
41224h	4	"reg_isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_A)—Offset 41224h" on page 1004	00000000h
41228h	4	"reg_isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_A)—Offset 41228h" on page 1005	00000000h
4122Ch	4	"reg_isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_A)—Offset 4122Ch" on page 1006	00000000h
41230h	4	"reg_isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_A)—Offset 41230h" on page 1007	00000000h
41234h	4	"reg_isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_A)—Offset 41234h" on page 1008	00000000h
41238h	4	"reg_isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_A)—Offset 41238h" on page 1009	00000000h
4123Ch	4	"reg_isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_A)—Offset 4123Ch" on page 1010	00000000h
41240h	4	"reg_isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_A)—Offset 41240h" on page 1011	00000000h
41244h	4	"reg_isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_A)—Offset 41244h" on page 1012	00000000h
41248h	4	"reg_isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_A)—Offset 41248h" on page 1013	00000000h
4124Ch	4	"reg_isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_A)—Offset 4124Ch" on page 1014	00000000h
41250h	4	"reg_isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_A)—Offset 41250h" on page 1015	00000000h

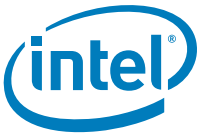


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41254h	4	"reg_isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_A)—Offset 41254h" on page 1016	00000000h
41258h	4	"reg_isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_A)—Offset 41258h" on page 1017	00000000h
4125Ch	4	"reg_isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_A)—Offset 4125Ch" on page 1018	00000000h
41260h	4	"reg_isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_A)—Offset 41260h" on page 1019	00000000h
41264h	4	"reg_isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_A)—Offset 41264h" on page 1020	00000000h
41268h	4	"reg_isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_A)—Offset 41268h" on page 1021	00000000h
4126Ch	4	"reg_isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_A)—Offset 4126Ch" on page 1022	00000000h
41270h	4	"reg_isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_A)—Offset 41270h" on page 1023	00000000h
41274h	4	"reg_isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_A)—Offset 41274h" on page 1024	00000000h
41278h	4	"reg_isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_A)—Offset 41278h" on page 1025	00000000h
4127Ch	4	"reg_isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_A)—Offset 4127Ch" on page 1026	00000000h
412C0h	4	"reg_isp_dma_DMA_CH22_dev_stride_A_type (isp_dma_DMA_CH22_dev_stride_A)—Offset 412C0h" on page 1027	00000000h
412C4h	4	"reg_isp_dma_DMA_CH23_dev_stride_A_type (isp_dma_DMA_CH23_dev_stride_A)—Offset 412C4h" on page 1028	00000000h
412C8h	4	"reg_isp_dma_DMA_CH24_dev_stride_A_type (isp_dma_DMA_CH24_dev_stride_A)—Offset 412C8h" on page 1029	00000000h
412CCh	4	"reg_isp_dma_DMA_CH25_dev_stride_A_type (isp_dma_DMA_CH25_dev_stride_A)—Offset 412CCh" on page 1029	00000000h

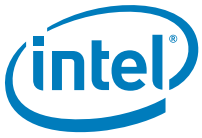


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
412D0h	4	"reg_isp_dma_DMA_CH26_dev_stride_A_type (isp_dma_DMA_CH26_dev_stride_A)—Offset 412D0h" on page 1030	00000000h
412D4h	4	"reg_isp_dma_DMA_CH27_dev_stride_A_type (isp_dma_DMA_CH27_dev_stride_A)—Offset 412D4h" on page 1030	00000000h
412D8h	4	"reg_isp_dma_DMA_CH28_dev_stride_A_type (isp_dma_DMA_CH28_dev_stride_A)—Offset 412D8h" on page 1031	00000000h
412DCh	4	"reg_isp_dma_DMA_CH29_dev_stride_A_type (isp_dma_DMA_CH29_dev_stride_A)—Offset 412DCh" on page 1032	00000000h
412E0h	4	"reg_isp_dma_DMA_CH30_dev_stride_A_type (isp_dma_DMA_CH30_dev_stride_A)—Offset 412E0h" on page 1032	00000000h
412E4h	4	"reg_isp_dma_DMA_CH31_dev_stride_A_type (isp_dma_DMA_CH31_dev_stride_A)—Offset 412E4h" on page 1033	00000000h
41300h	4	"reg_isp_dma_DMA_CH0_Device_Xb_A_type (isp_dma_DMA_CH0_Device_Xb_A)—Offset 41300h" on page 1033	00000000h
41304h	4	"reg_isp_dma_DMA_CH1_Device_Xb_A_type (isp_dma_DMA_CH1_Device_Xb_A)—Offset 41304h" on page 1034	00000000h
41308h	4	"reg_isp_dma_DMA_CH2_Device_Xb_A_type (isp_dma_DMA_CH2_Device_Xb_A)—Offset 41308h" on page 1035	00000000h
4130Ch	4	"reg_isp_dma_DMA_CH3_Device_Xb_A_type (isp_dma_DMA_CH3_Device_Xb_A)—Offset 4130Ch" on page 1035	00000000h
41310h	4	"reg_isp_dma_DMA_CH4_Device_Xb_A_type (isp_dma_DMA_CH4_Device_Xb_A)—Offset 41310h" on page 1036	00000000h
41314h	4	"reg_isp_dma_DMA_CH5_Device_Xb_A_type (isp_dma_DMA_CH5_Device_Xb_A)—Offset 41314h" on page 1037	00000000h
41318h	4	"reg_isp_dma_DMA_CH6_Device_Xb_A_type (isp_dma_DMA_CH6_Device_Xb_A)—Offset 41318h" on page 1037	00000000h
4131Ch	4	"reg_isp_dma_DMA_CH7_Device_Xb_A_type (isp_dma_DMA_CH7_Device_Xb_A)—Offset 4131Ch" on page 1038	00000000h
41320h	4	"reg_isp_dma_DMA_CH8_Device_Xb_A_type (isp_dma_DMA_CH8_Device_Xb_A)—Offset 41320h" on page 1039	00000000h

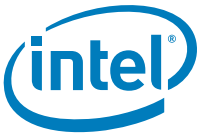


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41324h	4	"reg_isp_dma_DMA_CH9_Device_Xb_A_type (isp_dma_DMA_CH9_Device_Xb_A)—Offset 41324h" on page 1039	00000000h
41328h	4	"reg_isp_dma_DMA_CH10_Device_Xb_A_type (isp_dma_DMA_CH10_Device_Xb_A)—Offset 41328h" on page 1040	00000000h
4132Ch	4	"reg_isp_dma_DMA_CH11_Device_Xb_A_type (isp_dma_DMA_CH11_Device_Xb_A)—Offset 4132Ch" on page 1041	00000000h
41330h	4	"reg_isp_dma_DMA_CH12_Device_Xb_A_type (isp_dma_DMA_CH12_Device_Xb_A)—Offset 41330h" on page 1041	00000000h
41334h	4	"reg_isp_dma_DMA_CH13_Device_Xb_A_type (isp_dma_DMA_CH13_Device_Xb_A)—Offset 41334h" on page 1042	00000000h
41338h	4	"reg_isp_dma_DMA_CH14_Device_Xb_A_type (isp_dma_DMA_CH14_Device_Xb_A)—Offset 41338h" on page 1043	00000000h
4133Ch	4	"reg_isp_dma_DMA_CH15_Device_Xb_A_type (isp_dma_DMA_CH15_Device_Xb_A)—Offset 4133Ch" on page 1043	00000000h
41340h	4	"reg_isp_dma_DMA_CH16_Device_Xb_A_type (isp_dma_DMA_CH16_Device_Xb_A)—Offset 41340h" on page 1044	00000000h
41344h	4	"reg_isp_dma_DMA_CH17_Device_Xb_A_type (isp_dma_DMA_CH17_Device_Xb_A)—Offset 41344h" on page 1045	00000000h
41348h	4	"reg_isp_dma_DMA_CH18_Device_Xb_A_type (isp_dma_DMA_CH18_Device_Xb_A)—Offset 41348h" on page 1045	00000000h
4134Ch	4	"reg_isp_dma_DMA_CH19_Device_Xb_A_type (isp_dma_DMA_CH19_Device_Xb_A)—Offset 4134Ch" on page 1046	00000000h
41350h	4	"reg_isp_dma_DMA_CH20_Device_Xb_A_type (isp_dma_DMA_CH20_Device_Xb_A)—Offset 41350h" on page 1047	00000000h
41354h	4	"reg_isp_dma_DMA_CH21_Device_Xb_A_type (isp_dma_DMA_CH21_Device_Xb_A)—Offset 41354h" on page 1047	00000000h
41358h	4	"reg_isp_dma_DMA_CH22_Device_Xb_A_type (isp_dma_DMA_CH22_Device_Xb_A)—Offset 41358h" on page 1048	00000000h
4135Ch	4	"reg_isp_dma_DMA_CH23_Device_Xb_A_type (isp_dma_DMA_CH23_Device_Xb_A)—Offset 4135Ch" on page 1049	00000000h

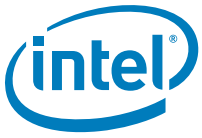


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41360h	4	"reg_isp_dma_DMA_CH24_Device_Xb_A_type (isp_dma_DMA_CH24_Device_Xb_A)—Offset 41360h" on page 1049	00000000h
41364h	4	"reg_isp_dma_DMA_CH25_Device_Xb_A_type (isp_dma_DMA_CH25_Device_Xb_A)—Offset 41364h" on page 1050	00000000h
41368h	4	"reg_isp_dma_DMA_CH26_Device_Xb_A_type (isp_dma_DMA_CH26_Device_Xb_A)—Offset 41368h" on page 1051	00000000h
4136Ch	4	"reg_isp_dma_DMA_CH27_Device_Xb_A_type (isp_dma_DMA_CH27_Device_Xb_A)—Offset 4136Ch" on page 1051	00000000h
41370h	4	"reg_isp_dma_DMA_CH28_Device_Xb_A_type (isp_dma_DMA_CH28_Device_Xb_A)—Offset 41370h" on page 1052	00000000h
41374h	4	"reg_isp_dma_DMA_CH29_Device_Xb_A_type (isp_dma_DMA_CH29_Device_Xb_A)—Offset 41374h" on page 1053	00000000h
41378h	4	"reg_isp_dma_DMA_CH30_Device_Xb_A_type (isp_dma_DMA_CH30_Device_Xb_A)—Offset 41378h" on page 1053	00000000h
4137Ch	4	"reg_isp_dma_DMA_CH31_Device_Xb_A_type (isp_dma_DMA_CH31_Device_Xb_A)—Offset 4137Ch" on page 1054	00000000h
41400h	4	"reg_isp_dma_DMA_CH0_dev_stride_B_type (isp_dma_DMA_CH0_dev_stride_B)—Offset 41400h" on page 1055	00000000h
41404h	4	"reg_isp_dma_DMA_CH1_dev_stride_B_type (isp_dma_DMA_CH1_dev_stride_B)—Offset 41404h" on page 1055	00000000h
41408h	4	"reg_isp_dma_DMA_CH2_dev_stride_B_type (isp_dma_DMA_CH2_dev_stride_B)—Offset 41408h" on page 1056	00000000h
4140Ch	4	"reg_isp_dma_DMA_CH3_dev_stride_B_type (isp_dma_DMA_CH3_dev_stride_B)—Offset 4140Ch" on page 1056	00000000h
41410h	4	"reg_isp_dma_DMA_CH4_dev_stride_B_type (isp_dma_DMA_CH4_dev_stride_B)—Offset 41410h" on page 1057	00000000h
41414h	4	"reg_isp_dma_DMA_CH5_dev_stride_B_type (isp_dma_DMA_CH5_dev_stride_B)—Offset 41414h" on page 1058	00000000h
41418h	4	"reg_isp_dma_DMA_CH6_dev_stride_B_type (isp_dma_DMA_CH6_dev_stride_B)—Offset 41418h" on page 1058	00000000h

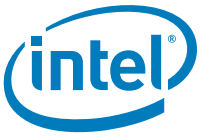


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
4141Ch	4	"reg_isp_dma_DMA_CH7_dev_stride_B_type (isp_dma_DMA_CH7_dev_stride_B)—Offset 4141Ch" on page 1059	00000000h
41420h	4	"reg_isp_dma_DMA_CH8_dev_stride_B_type (isp_dma_DMA_CH8_dev_stride_B)—Offset 41420h" on page 1059	00000000h
41424h	4	"reg_isp_dma_DMA_CH9_dev_stride_B_type (isp_dma_DMA_CH9_dev_stride_B)—Offset 41424h" on page 1060	00000000h
41428h	4	"reg_isp_dma_DMA_CH10_dev_stride_B_type (isp_dma_DMA_CH10_dev_stride_B)—Offset 41428h" on page 1060	00000000h
4142Ch	4	"reg_isp_dma_DMA_CH11_dev_stride_B_type (isp_dma_DMA_CH11_dev_stride_B)—Offset 4142Ch" on page 1061	00000000h
41430h	4	"reg_isp_dma_DMA_CH12_dev_stride_B_type (isp_dma_DMA_CH12_dev_stride_B)—Offset 41430h" on page 1062	00000000h
41434h	4	"reg_isp_dma_DMA_CH13_dev_stride_B_type (isp_dma_DMA_CH13_dev_stride_B)—Offset 41434h" on page 1062	00000000h
41438h	4	"reg_isp_dma_DMA_CH14_dev_stride_B_type (isp_dma_DMA_CH14_dev_stride_B)—Offset 41438h" on page 1063	00000000h
4143Ch	4	"reg_isp_dma_DMA_CH15_dev_stride_B_type (isp_dma_DMA_CH15_dev_stride_B)—Offset 4143Ch" on page 1064	00000000h
41440h	4	"reg_isp_dma_DMA_CH16_dev_stride_B_type (isp_dma_DMA_CH16_dev_stride_B)—Offset 41440h" on page 1064	00000000h
41444h	4	"reg_isp_dma_DMA_CH17_dev_stride_B_type (isp_dma_DMA_CH17_dev_stride_B)—Offset 41444h" on page 1065	00000000h
41448h	4	"reg_isp_dma_DMA_CH18_dev_stride_B_type (isp_dma_DMA_CH18_dev_stride_B)—Offset 41448h" on page 1065	00000000h
4144Ch	4	"reg_isp_dma_DMA_CH19_dev_stride_B_type (isp_dma_DMA_CH19_dev_stride_B)—Offset 4144Ch" on page 1066	00000000h
41450h	4	"reg_isp_dma_DMA_CH20_dev_stride_B_type (isp_dma_DMA_CH20_dev_stride_B)—Offset 41450h" on page 1067	00000000h
41454h	4	"reg_isp_dma_DMA_CH21_dev_stride_B_type (isp_dma_DMA_CH21_dev_stride_B)—Offset 41454h" on page 1067	00000000h

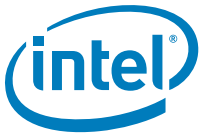


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41458h	4	"reg_isp_dma_DMA_CH22_dev_stride_B_type (isp_dma_DMA_CH22_dev_stride_B)—Offset 41458h" on page 1068	00000000h
4145Ch	4	"reg_isp_dma_DMA_CH23_dev_stride_B_type (isp_dma_DMA_CH23_dev_stride_B)—Offset 4145Ch" on page 1068	00000000h
41460h	4	"reg_isp_dma_DMA_CH24_dev_stride_B_type (isp_dma_DMA_CH24_dev_stride_B)—Offset 41460h" on page 1069	00000000h
41468h	4	"reg_isp_dma_DMA_CH26_dev_stride_B_type (isp_dma_DMA_CH26_dev_stride_B)—Offset 41468h" on page 1070	00000000h
4146Ch	4	"reg_isp_dma_DMA_CH27_dev_stride_B_type (isp_dma_DMA_CH27_dev_stride_B)—Offset 4146Ch" on page 1070	00000000h
41470h	4	"reg_isp_dma_DMA_CH28_dev_stride_B_type (isp_dma_DMA_CH28_dev_stride_B)—Offset 41470h" on page 1071	00000000h
41474h	4	"reg_isp_dma_DMA_CH29_dev_stride_B_type (isp_dma_DMA_CH29_dev_stride_B)—Offset 41474h" on page 1071	00000000h
41478h	4	"reg_isp_dma_DMA_CH30_dev_stride_B_type (isp_dma_DMA_CH30_dev_stride_B)—Offset 41478h" on page 1072	00000000h
4147Ch	4	"reg_isp_dma_DMA_CH31_dev_stride_B_type (isp_dma_DMA_CH31_dev_stride_B)—Offset 4147Ch" on page 1073	00000000h
41500h	4	"reg_isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B)—Offset 41500h" on page 1073	00000000h
41504h	4	"reg_isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_B)—Offset 41504h" on page 1074	00000000h
41508h	4	"reg_isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_B)—Offset 41508h" on page 1075	00000000h
4150Ch	4	"reg_isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_B)—Offset 4150Ch" on page 1076	00000000h
41510h	4	"reg_isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_B)—Offset 41510h" on page 1077	00000000h
41514h	4	"reg_isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_B)—Offset 41514h" on page 1078	00000000h

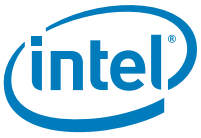


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41518h	4	"reg_isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_B)—Offset 41518h" on page 1079	00000000h
4151Ch	4	"reg_isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_B)—Offset 4151Ch" on page 1080	00000000h
41520h	4	"reg_isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_B)—Offset 41520h" on page 1081	00000000h
41524h	4	"reg_isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_B)—Offset 41524h" on page 1082	00000000h
41528h	4	"reg_isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_B)—Offset 41528h" on page 1083	00000000h
4152Ch	4	"reg_isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_B)—Offset 4152Ch" on page 1084	00000000h
41530h	4	"reg_isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_B)—Offset 41530h" on page 1085	00000000h
41534h	4	"reg_isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_B)—Offset 41534h" on page 1086	00000000h
41538h	4	"reg_isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_B)—Offset 41538h" on page 1087	00000000h
4153Ch	4	"reg_isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_B)—Offset 4153Ch" on page 1088	00000000h
41540h	4	"reg_isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_B)—Offset 41540h" on page 1089	00000000h
41544h	4	"reg_isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_B)—Offset 41544h" on page 1090	00000000h
41548h	4	"reg_isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_B)—Offset 41548h" on page 1091	00000000h
4154Ch	4	"reg_isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_B)—Offset 4154Ch" on page 1092	00000000h
41550h	4	"reg_isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_B)—Offset 41550h" on page 1093	00000000h

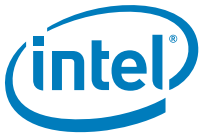


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41554h	4	"reg_isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_B)—Offset 41554h" on page 1094	00000000h
41558h	4	"reg_isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_B)—Offset 41558h" on page 1095	00000000h
4155Ch	4	"reg_isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_B)—Offset 4155Ch" on page 1096	00000000h
41560h	4	"reg_isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_B)—Offset 41560h" on page 1097	00000000h
41564h	4	"reg_isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_B)—Offset 41564h" on page 1098	00000000h
41568h	4	"reg_isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_B)—Offset 41568h" on page 1099	00000000h
4156Ch	4	"reg_isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_B)—Offset 4156Ch" on page 1100	00000000h
41570h	4	"reg_isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_B)—Offset 41570h" on page 1101	00000000h
41574h	4	"reg_isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_B)—Offset 41574h" on page 1102	00000000h
41578h	4	"reg_isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_B)—Offset 41578h" on page 1103	00000000h
4157Ch	4	"reg_isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_B)—Offset 4157Ch" on page 1104	00000000h
41600h	4	"reg_isp_dma_DMA_CH0_Device_Xb_B_type (isp_dma_DMA_CH0_Device_Xb_B)—Offset 41600h" on page 1105	00000000h
41604h	4	"reg_isp_dma_DMA_CH1_Device_Xb_B_type (isp_dma_DMA_CH1_Device_Xb_B)—Offset 41604h" on page 1106	00000000h
41608h	4	"reg_isp_dma_DMA_CH2_Device_Xb_B_type (isp_dma_DMA_CH2_Device_Xb_B)—Offset 41608h" on page 1107	00000000h
4160Ch	4	"reg_isp_dma_DMA_CH3_Device_Xb_B_type (isp_dma_DMA_CH3_Device_Xb_B)—Offset 4160Ch" on page 1107	00000000h

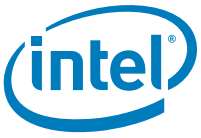


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41610h	4	"reg_isp_dma_DMA_CH4_Device_Xb_B_type (isp_dma_DMA_CH4_Device_Xb_B)—Offset 41610h" on page 1108	00000000h
41614h	4	"reg_isp_dma_DMA_CH5_Device_Xb_B_type (isp_dma_DMA_CH5_Device_Xb_B)—Offset 41614h" on page 1109	00000000h
41618h	4	"reg_isp_dma_DMA_CH6_Device_Xb_B_type (isp_dma_DMA_CH6_Device_Xb_B)—Offset 41618h" on page 1109	00000000h
4161Ch	4	"reg_isp_dma_DMA_CH7_Device_Xb_B_type (isp_dma_DMA_CH7_Device_Xb_B)—Offset 4161Ch" on page 1110	00000000h
41620h	4	"reg_isp_dma_DMA_CH8_Device_Xb_B_type (isp_dma_DMA_CH8_Device_Xb_B)—Offset 41620h" on page 1111	00000000h
41624h	4	"reg_isp_dma_DMA_CH9_Device_Xb_B_type (isp_dma_DMA_CH9_Device_Xb_B)—Offset 41624h" on page 1111	00000000h
41628h	4	"reg_isp_dma_DMA_CH10_Device_Xb_B_type (isp_dma_DMA_CH10_Device_Xb_B)—Offset 41628h" on page 1112	00000000h
4162Ch	4	"reg_isp_dma_DMA_CH11_Device_Xb_B_type (isp_dma_DMA_CH11_Device_Xb_B)—Offset 4162Ch" on page 1113	00000000h
41630h	4	"reg_isp_dma_DMA_CH12_Device_Xb_B_type (isp_dma_DMA_CH12_Device_Xb_B)—Offset 41630h" on page 1113	00000000h
41634h	4	"reg_isp_dma_DMA_CH13_Device_Xb_B_type (isp_dma_DMA_CH13_Device_Xb_B)—Offset 41634h" on page 1114	00000000h
41638h	4	"reg_isp_dma_DMA_CH14_Device_Xb_B_type (isp_dma_DMA_CH14_Device_Xb_B)—Offset 41638h" on page 1115	00000000h
4163Ch	4	"reg_isp_dma_DMA_CH15_Device_Xb_B_type (isp_dma_DMA_CH15_Device_Xb_B)—Offset 4163Ch" on page 1115	00000000h
41640h	4	"reg_isp_dma_DMA_CH16_Device_Xb_B_type (isp_dma_DMA_CH16_Device_Xb_B)—Offset 41640h" on page 1116	00000000h
41644h	4	"reg_isp_dma_DMA_CH17_Device_Xb_B_type (isp_dma_DMA_CH17_Device_Xb_B)—Offset 41644h" on page 1117	00000000h
41648h	4	"reg_isp_dma_DMA_CH18_Device_Xb_B_type (isp_dma_DMA_CH18_Device_Xb_B)—Offset 41648h" on page 1117	00000000h

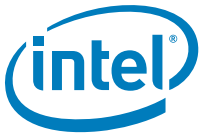


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
4164Ch	4	"reg_isp_dma_DMA_CH19_Device_Xb_B_type (isp_dma_DMA_CH19_Device_Xb_B)—Offset 4164Ch" on page 1118	00000000h
41650h	4	"reg_isp_dma_DMA_CH20_Device_Xb_B_type (isp_dma_DMA_CH20_Device_Xb_B)—Offset 41650h" on page 1119	00000000h
41654h	4	"reg_isp_dma_DMA_CH21_Device_Xb_B_type (isp_dma_DMA_CH21_Device_Xb_B)—Offset 41654h" on page 1119	00000000h
41658h	4	"reg_isp_dma_DMA_CH22_Device_Xb_B_type (isp_dma_DMA_CH22_Device_Xb_B)—Offset 41658h" on page 1120	00000000h
4165Ch	4	"reg_isp_dma_DMA_CH23_Device_Xb_B_type (isp_dma_DMA_CH23_Device_Xb_B)—Offset 4165Ch" on page 1121	00000000h
41660h	4	"reg_isp_dma_DMA_CH24_Device_Xb_B_type (isp_dma_DMA_CH24_Device_Xb_B)—Offset 41660h" on page 1121	00000000h
41664h	4	"reg_isp_dma_DMA_CH25_Device_Xb_B_type (isp_dma_DMA_CH25_Device_Xb_B)—Offset 41664h" on page 1122	00000000h
41668h	4	"reg_isp_dma_DMA_CH26_Device_Xb_B_type (isp_dma_DMA_CH26_Device_Xb_B)—Offset 41668h" on page 1123	00000000h
4166Ch	4	"reg_isp_dma_DMA_CH27_Device_Xb_B_type (isp_dma_DMA_CH27_Device_Xb_B)—Offset 4166Ch" on page 1123	00000000h
41670h	4	"reg_isp_dma_DMA_CH28_Device_Xb_B_type (isp_dma_DMA_CH28_Device_Xb_B)—Offset 41670h" on page 1124	00000000h
41674h	4	"reg_isp_dma_DMA_CH29_Device_Xb_B_type (isp_dma_DMA_CH29_Device_Xb_B)—Offset 41674h" on page 1125	00000000h
41678h	4	"reg_isp_dma_DMA_CH31_Device_Xb_B_type (isp_dma_DMA_CH31_Device_Xb_B)—Offset 41678h" on page 1125	00000000h
41700h	4	"reg_isp_dma_DMA_CH0_Yb_type (isp_dma_DMA_CH0_Yb)—Offset 41700h" on page 1126	00000000h
41704h	4	"reg_isp_dma_DMA_CH1_Yb_type (isp_dma_DMA_CH1_Yb)—Offset 41704h" on page 1127	00000000h
41708h	4	"reg_isp_dma_DMA_CH2_Yb_type (isp_dma_DMA_CH2_Yb)—Offset 41708h" on page 1127	00000000h
4170Ch	4	"reg_isp_dma_DMA_CH3_Yb_type (isp_dma_DMA_CH3_Yb)—Offset 4170Ch" on page 1128	00000000h

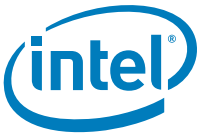


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41710h	4	"reg_isp_dma_DMA_CH4_Yb_type (isp_dma_DMA_CH4_Yb)—Offset 41710h" on page 1129	00000000h
41714h	4	"reg_isp_dma_DMA_CH5_Yb_type (isp_dma_DMA_CH5_Yb)—Offset 41714h" on page 1129	00000000h
41718h	4	"reg_isp_dma_DMA_CH6_Yb_type (isp_dma_DMA_CH6_Yb)—Offset 41718h" on page 1130	00000000h
4171Ch	4	"reg_isp_dma_DMA_CH7_Yb_type (isp_dma_DMA_CH7_Yb)—Offset 4171Ch" on page 1130	00000000h
41720h	4	"reg_isp_dma_DMA_CH8_Yb_type (isp_dma_DMA_CH8_Yb)—Offset 41720h" on page 1131	00000000h
41724h	4	"reg_isp_dma_DMA_CH9_Yb_type (isp_dma_DMA_CH9_Yb)—Offset 41724h" on page 1132	00000000h
41728h	4	"reg_isp_dma_DMA_CH10_Yb_type (isp_dma_DMA_CH10_Yb)—Offset 41728h" on page 1132	00000000h
4172Ch	4	"reg_isp_dma_DMA_CH11_Yb_type (isp_dma_DMA_CH11_Yb)—Offset 4172Ch" on page 1133	00000000h
41730h	4	"reg_isp_dma_DMA_CH12_Yb_type (isp_dma_DMA_CH12_Yb)—Offset 41730h" on page 1133	00000000h
41734h	4	"reg_isp_dma_DMA_CH13_Yb_type (isp_dma_DMA_CH13_Yb)—Offset 41734h" on page 1134	00000000h
41738h	4	"reg_isp_dma_DMA_CH14_Yb_type (isp_dma_DMA_CH14_Yb)—Offset 41738h" on page 1135	00000000h
4173Ch	4	"reg_isp_dma_DMA_CH15_Yb_type (isp_dma_DMA_CH15_Yb)—Offset 4173Ch" on page 1135	00000000h
41740h	4	"reg_isp_dma_DMA_CH16_Yb_type (isp_dma_DMA_CH16_Yb)—Offset 41740h" on page 1136	00000000h
41744h	4	"reg_isp_dma_DMA_CH17_Yb_type (isp_dma_DMA_CH17_Yb)—Offset 41744h" on page 1136	00000000h
41748h	4	"reg_isp_dma_DMA_CH18_Yb_type (isp_dma_DMA_CH18_Yb)—Offset 41748h" on page 1137	00000000h
4174Ch	4	"reg_isp_dma_DMA_CH19_Yb_type (isp_dma_DMA_CH19_Yb)—Offset 4174Ch" on page 1138	00000000h
41750h	4	"reg_isp_dma_DMA_CH20_Yb_type (isp_dma_DMA_CH20_Yb)—Offset 41750h" on page 1138	00000000h
41754h	4	"reg_isp_dma_DMA_CH21_Yb_type (isp_dma_DMA_CH21_Yb)—Offset 41754h" on page 1139	00000000h
41758h	4	"reg_isp_dma_DMA_CH22_Yb_type (isp_dma_DMA_CH22_Yb)—Offset 41758h" on page 1139	00000000h
4175Ch	4	"reg_isp_dma_DMA_CH23_Yb_type (isp_dma_DMA_CH23_Yb)—Offset 4175Ch" on page 1140	00000000h
41760h	4	"reg_isp_dma_DMA_CH24_Yb_type (isp_dma_DMA_CH24_Yb)—Offset 41760h" on page 1141	00000000h

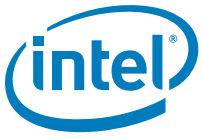


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41764h	4	"reg_isp_dma_DMA_CH25_Yb_type (isp_dma_DMA_CH25_Yb)—Offset 41764h" on page 1141	00000000h
41768h	4	"reg_isp_dma_DMA_CH26_Yb_type (isp_dma_DMA_CH26_Yb)—Offset 41768h" on page 1142	00000000h
4176Ch	4	"reg_isp_dma_DMA_CH27_Yb_type (isp_dma_DMA_CH27_Yb)—Offset 4176Ch" on page 1142	00000000h
41770h	4	"reg_isp_dma_DMA_CH28_Yb_type (isp_dma_DMA_CH28_Yb)—Offset 41770h" on page 1143	00000000h
41774h	4	"reg_isp_dma_DMA_CH29_Yb_type (isp_dma_DMA_CH29_Yb)—Offset 41774h" on page 1144	00000000h
4177Ch	4	"reg_isp_dma_DMA_CH31_Yb_type (isp_dma_DMA_CH31_Yb)—Offset 4177Ch" on page 1144	00000000h
41800h	4	"reg_isp_dma_DMA_CH0_pending_command_type (isp_dma_DMA_CH0_pending_command)—Offset 41800h" on page 1145	00000000h
41804h	4	"reg_isp_dma_DMA_CH1_pending_command_type (isp_dma_DMA_CH1_pending_command)—Offset 41804h" on page 1145	00000000h
41808h	4	"reg_isp_dma_DMA_CH2_pending_command_type (isp_dma_DMA_CH2_pending_command)—Offset 41808h" on page 1146	00000000h
4180Ch	4	"reg_isp_dma_DMA_CH3_pending_command_type (isp_dma_DMA_CH3_pending_command)—Offset 4180Ch" on page 1147	00000000h
41810h	4	"reg_isp_dma_DMA_CH4_pending_command_type (isp_dma_DMA_CH4_pending_command)—Offset 41810h" on page 1148	00000000h
41814h	4	"reg_isp_dma_DMA_CH5_pending_command_type (isp_dma_DMA_CH5_pending_command)—Offset 41814h" on page 1149	00000000h
41818h	4	"reg_isp_dma_DMA_CH6_pending_command_type (isp_dma_DMA_CH6_pending_command)—Offset 41818h" on page 1150	00000000h
4181Ch	4	"reg_isp_dma_DMA_CH7_pending_command_type (isp_dma_DMA_CH7_pending_command)—Offset 4181Ch" on page 1151	00000000h
41820h	4	"reg_isp_dma_DMA_CH8_pending_command_type (isp_dma_DMA_CH8_pending_command)—Offset 41820h" on page 1152	00000000h
41824h	4	"reg_isp_dma_DMA_CH9_pending_command_type (isp_dma_DMA_CH9_pending_command)—Offset 41824h" on page 1153	00000000h
41828h	4	"reg_isp_dma_DMA_CH10_pending_command_type (isp_dma_DMA_CH10_pending_command)—Offset 41828h" on page 1154	00000000h

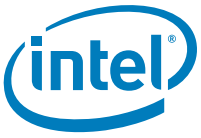


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
4182Ch	4	"reg_isp_dma_DMA_CH11_pending_command_type (isp_dma_DMA_CH11_pending_command)—Offset 4182Ch" on page 1155	00000000h
41830h	4	"reg_isp_dma_DMA_CH12_pending_command_type (isp_dma_DMA_CH12_pending_command)—Offset 41830h" on page 1156	00000000h
41834h	4	"reg_isp_dma_DMA_CH13_pending_command_type (isp_dma_DMA_CH13_pending_command)—Offset 41834h" on page 1157	00000000h
41838h	4	"reg_isp_dma_DMA_CH14_pending_command_type (isp_dma_DMA_CH14_pending_command)—Offset 41838h" on page 1158	00000000h
4183Ch	4	"reg_isp_dma_DMA_CH15_pending_command_type (isp_dma_DMA_CH15_pending_command)—Offset 4183Ch" on page 1159	00000000h
41840h	4	"reg_isp_dma_DMA_CH16_pending_command_type (isp_dma_DMA_CH16_pending_command)—Offset 41840h" on page 1160	00000000h
41844h	4	"reg_isp_dma_DMA_CH17_pending_command_type (isp_dma_DMA_CH17_pending_command)—Offset 41844h" on page 1161	00000000h
41848h	4	"reg_isp_dma_DMA_CH18_pending_command_type (isp_dma_DMA_CH18_pending_command)—Offset 41848h" on page 1162	00000000h
4184Ch	4	"reg_isp_dma_DMA_CH19_pending_command_type (isp_dma_DMA_CH19_pending_command)—Offset 4184Ch" on page 1163	00000000h
41850h	4	"reg_isp_dma_DMA_CH20_pending_command_type (isp_dma_DMA_CH20_pending_command)—Offset 41850h" on page 1164	00000000h
41854h	4	"reg_isp_dma_DMA_CH21_pending_command_type (isp_dma_DMA_CH21_pending_command)—Offset 41854h" on page 1165	00000000h
41858h	4	"reg_isp_dma_DMA_CH22_pending_command_type (isp_dma_DMA_CH22_pending_command)—Offset 41858h" on page 1166	00000000h
4185Ch	4	"reg_isp_dma_DMA_CH23_pending_command_type (isp_dma_DMA_CH23_pending_command)—Offset 4185Ch" on page 1167	00000000h
41860h	4	"reg_isp_dma_DMA_CH24_pending_command_type (isp_dma_DMA_CH24_pending_command)—Offset 41860h" on page 1168	00000000h
41864h	4	"reg_isp_dma_DMA_CH25_pending_command_type (isp_dma_DMA_CH25_pending_command)—Offset 41864h" on page 1169	00000000h

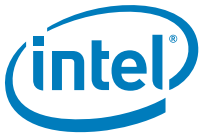


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41868h	4	"reg_isp_dma_DMA_CH26_pending_command_type (isp_dma_DMA_CH26_pending_command)—Offset 41868h" on page 1170	00000000h
4186Ch	4	"reg_isp_dma_DMA_CH27_pending_command_type (isp_dma_DMA_CH27_pending_command)—Offset 4186Ch" on page 1171	00000000h
41870h	4	"reg_isp_dma_DMA_CH28_pending_command_type (isp_dma_DMA_CH28_pending_command)—Offset 41870h" on page 1172	00000000h
41874h	4	"reg_isp_dma_DMA_CH29_pending_command_type (isp_dma_DMA_CH29_pending_command)—Offset 41874h" on page 1173	00000000h
41878h	4	"reg_isp_dma_DMA_CH30_pending_command_type (isp_dma_DMA_CH30_pending_command)—Offset 41878h" on page 1174	00000000h
4187Ch	4	"reg_isp_dma_DMA_CH31_pending_command_type (isp_dma_DMA_CH31_pending_command)—Offset 4187Ch" on page 1175	00000000h
42000h	4	"reg_isp_dma_DMA_command_token_type (isp_dma_DMA_command_token)—Offset 42000h" on page 1176	00000000h
42004h	4	"reg_isp_dma_DMA_command_src_addr_type (isp_dma_DMA_command_src_addr)—Offset 42004h" on page 1177	00000000h
42008h	4	"reg_isp_dma_DMA_command_dst_addr_type (isp_dma_DMA_command_dst_addr)—Offset 42008h" on page 1177	00000000h
4200Ch	4	"reg_isp_dma_DMA_command_ctrl_id_type (isp_dma_DMA_command_ctrl_id)—Offset 4200Ch" on page 1178	00000000h
42010h	4	"reg_isp_dma_DMA_FSM_Ctrl_status_type (isp_dma_DMA_FSM_Ctrl_status)—Offset 42010h" on page 1179	00000001h
42014h	4	"reg_isp_dma_DMA_FSM_Pack_status_type (isp_dma_DMA_FSM_Pack_status)—Offset 42014h" on page 1179	00000001h
42018h	4	"reg_isp_dma_DMA_FSM_request_status_type (isp_dma_DMA_FSM_request_status)—Offset 42018h" on page 1180	00000000h
4201Ch	4	"reg_isp_dma_DMA_FSM_write_status_type (isp_dma_DMA_FSM_write_status)—Offset 4201Ch" on page 1181	00000000h
42110h	4	"reg_isp_dma_DMA_FSM_Ctrl_dev_idx_type (isp_dma_DMA_FSM_Ctrl_dev_idx)—Offset 42110h" on page 1182	00000000h

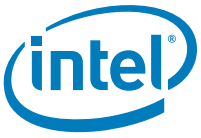


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
42114h	4	"reg_isp_dma_DMA_FSM_Pack_cnt_Yb_type (isp_dma_DMA_FSM_Pack_cnt_Yb)—Offset 42114h" on page 1182	00000000h
42118h	4	"reg_isp_dma_DMA_FSM_Request_cnt_Yb_type (isp_dma_DMA_FSM_Request_cnt_Yb)—Offset 42118h" on page 1183	00000000h
4211Ch	4	"reg_isp_dma_DMA_FSM_Write_cnt_Y_type (isp_dma_DMA_FSM_Write_cnt_Y)—Offset 4211Ch" on page 1184	00000000h
42210h	4	"reg_isp_dma_DMA_FSM_Ctrl_req_addr_type (isp_dma_DMA_FSM_Ctrl_req_addr)—Offset 42210h" on page 1184	00000000h
42214h	4	"reg_isp_dma_DMA_FSM_Pack_req_cnt_Xb_type (isp_dma_DMA_FSM_Pack_req_cnt_Xb)—Offset 42214h" on page 1185	00000000h
42218h	4	"reg_isp_dma_DMA_FSM_Request_cnt_Xb_type (isp_dma_DMA_FSM_Request_cnt_Xb)—Offset 42218h" on page 1186	00000000h
4221Ch	4	"reg_isp_dma_DMA_FSM_Write_cnt_Xb_type (isp_dma_DMA_FSM_Write_cnt_Xb)—Offset 4221Ch" on page 1186	00000000h
42310h	4	"reg_isp_dma_DMA_FSM_Ctrl_req_stride_type (isp_dma_DMA_FSM_Ctrl_req_stride)—Offset 42310h" on page 1187	00000000h
42314h	4	"reg_isp_dma_DMA_FSM_Pack_wr_cnt_Xb_type (isp_dma_DMA_FSM_Pack_wr_cnt_Xb)—Offset 42314h" on page 1188	00000000h
42318h	4	"reg_isp_dma_DMA_FSM_Req_remining_Xb_type (isp_dma_DMA_FSM_Req_remining_Xb)—Offset 42318h" on page 1188	00000000h
4231Ch	4	"reg_isp_dma_DMA_FSM_Wr_remining_Xb_type (isp_dma_DMA_FSM_Wr_remining_Xb)—Offset 4231Ch" on page 1189	00000000h
42410h	4	"reg_isp_dma_DMA_FSM_Ctrl_req_Xb_type (isp_dma_DMA_FSM_Ctrl_req_Xb)—Offset 42410h" on page 1190	00000000h
42418h	4	"reg_isp_dma_DMA_FSM_Req_burst_cnt_type (isp_dma_DMA_FSM_Req_burst_cnt)—Offset 42418h" on page 1191	0000FFFFh
4241Ch	4	"reg_isp_dma_DMA_FSM_Wr_burst_cnt_type (isp_dma_DMA_FSM_Wr_burst_cnt)—Offset 4241Ch" on page 1191	0000FFFFh
42510h	4	"reg_isp_dma_DMA_FSM_Ctrl_req_Yb_type (isp_dma_DMA_FSM_Ctrl_req_Yb)—Offset 42510h" on page 1192	00000000h

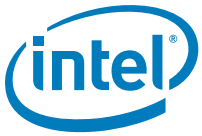


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
42610h	4	"reg_isp_dma_DMA_FSM_Ctrl_Pack_req_dev_idx_type (isp_dma_DMA_FSM_Ctrl_Pack_req_dev_idx)—Offset 42610h" on page 1193	00000000h
42710h	4	"reg_isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx_type (isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx)—Offset 42710h" on page 1194	00000000h
42810h	4	"reg_isp_dma_DMA_FSM_Ctrl_Wr_addr_type (isp_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 42810h" on page 1194	00000000h
42910h	4	"reg_isp_dma_DMA_FSM_Ctrl_Wr_stride_type (isp_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 42910h" on page 1195	00000000h
42A10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_req_Xb_type (isp_dma_DMA_FSM_Ctrl_pack_req_Xb)—Offset 42A10h" on page 1195	00000000h
42B10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_Yb_type (isp_dma_DMA_FSM_Ctrl_pack_Yb)—Offset 42B10h" on page 1196	00000000h
42C10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_wr_Xb_type (isp_dma_DMA_FSM_Ctrl_pack_wr_Xb)—Offset 42C10h" on page 1197	00000000h
42D10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_req_elem_type (isp_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 42D10h" on page 1198	00000000h
42E10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_wr_elem_type (isp_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 42E10h" on page 1198	00000000h
42F10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id_type (isp_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id)—Offset 42F10h" on page 1199	00000000h
43000h	4	"reg_isp_dma_Dev_Interf_0_req_side_type (isp_dma_Dev_Interf_0_req_side)—Offset 43000h" on page 1200	00000000h
43004h	4	"reg_isp_dma_Dev_Interf_1_req_side_type (isp_dma_Dev_Interf_1_req_side)—Offset 43004h" on page 1201	00000006h
43008h	4	"reg_isp_dma_Dev_Interf_2_req_side_type (isp_dma_Dev_Interf_2_req_side)—Offset 43008h" on page 1202	00000006h
43100h	4	"reg_isp_dma_Dev_Interf_0_snd_side_type (isp_dma_Dev_Interf_0_snd_side)—Offset 43100h" on page 1203	00000004h
43104h	4	"reg_isp_dma_Dev_Interf_1_snd_side_type (isp_dma_Dev_Interf_1_snd_side)—Offset 43104h" on page 1204	00000006h

Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
43108h	4	"reg_isp_dma_Dev_Interf_2_snd_side_type (isp_dma_Dev_Interf_2_snd_side)—Offset 43108h" on page 1205	00000006h
43200h	4	"reg_isp_dma_Dev_Interf_0_Fifo_status_type (isp_dma_Dev_Interf_0_Fifo_status)—Offset 43200h" on page 1206	00000004h
43204h	4	"reg_isp_dma_Dev_Interf_1_Fifo_status_type (isp_dma_Dev_Interf_1_Fifo_status)—Offset 43204h" on page 1207	00000004h
43208h	4	"reg_isp_dma_Dev_Interf_2_Fifo_status_type (isp_dma_Dev_Interf_2_Fifo_status)—Offset 43208h" on page 1208	00000004h
43300h	4	"reg_isp_dma_Dev_Interf_0_Req_complete_bust_type (isp_dma_Dev_Interf_0_Req_complete_bust)—Offset 43300h" on page 1209	00000000h
43304h	4	"reg_isp_dma_Dev_Interf_1_Req_complete_bust_type (isp_dma_Dev_Interf_1_Req_complete_bust)—Offset 43304h" on page 1210	00000000h
43308h	4	"reg_isp_dma_Dev_Interf_2_Req_complete_bust_type (isp_dma_Dev_Interf_2_Req_complete_bust)—Offset 43308h" on page 1211	00000000h
43408h	4	"reg_isp_dma_Dev_Interf_2_Max_burst_Size_type (isp_dma_Dev_Interf_2_Max_burst_Size)—Offset 43408h" on page 1212	0000007Fh
50000h	4	"reg_gdc1_reg0_type (gdc1_reg0)—Offset 50000h" on page 1213	00000000h
50004h	4	"reg_gdc1_woi_x_type (gdc1_woi_x)—Offset 50004h" on page 1214	00000000h
50008h	4	"reg_gdc1_woi_y_type (gdc1_woi_y)—Offset 50008h" on page 1214	00000000h
5000Ch	4	"reg_gdc1_bpp_type (gdc1_bpp)—Offset 5000Ch" on page 1215	00000000h
50010h	4	"reg_gdc1_fryipxfrx_start_type (gdc1_fryipxfrx_start)—Offset 50010h" on page 1215	00000000h
50014h	4	"reg_gdc1_oxdim_type (gdc1_oxdim)—Offset 50014h" on page 1216	00000000h
50018h	4	"reg_gdc1_oydim_type (gdc1_oydim)—Offset 50018h" on page 1217	00000000h
5001Ch	4	"reg_gdc1_src_addr_type (gdc1_src_addr)—Offset 5001Ch" on page 1217	00000000h
50020h	4	"reg_gdc1_src_end_type (gdc1_src_end)—Offset 50020h" on page 1218	00000000h
50024h	4	"reg_gdc1_src_wrap_type (gdc1_src_wrap)—Offset 50024h" on page 1218	00000000h

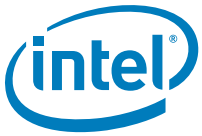


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
50028h	4	"reg_gdc1_src_stride_type (gdc1_src_stride)—Offset 50028h" on page 1219	00000000h
5002Ch	4	"reg_gdc1_dst_addr_type (gdc1_dst_addr)—Offset 5002Ch" on page 1219	00000000h
50030h	4	"reg_gdc1_dst_stride_type (gdc1_dst_stride)—Offset 50030h" on page 1220	00000000h
50034h	4	"reg_gdc1_dx_type (gdc1_dx)—Offset 50034h" on page 1221	00000000h
50038h	4	"reg_gdc1_dy_type (gdc1_dy)—Offset 50038h" on page 1221	00000000h
5003Ch	4	"reg_gdc1_P0_primX_ixdim_type (gdc1_P0_primX_ixdim)—Offset 5003Ch" on page 1222	00000000h
50040h	4	"reg_gdc1_P0_primY_iydim_type (gdc1_P0_primY_iydim)—Offset 50040h" on page 1222	00000000h
50044h	4	"reg_gdc1_P1_primX_type (gdc1_P1_primX)—Offset 50044h" on page 1223	00000000h
50048h	4	"reg_gdc1_P1_primY_type (gdc1_P1_primY)—Offset 50048h" on page 1224	00000000h
5004Ch	4	"reg_gdc1_P2_primX_type (gdc1_P2_primX)—Offset 5004Ch" on page 1224	00000000h
50050h	4	"reg_gdc1_P2_primY_type (gdc1_P2_primY)—Offset 50050h" on page 1225	00000000h
50054h	4	"reg_gdc1_P3_primX_type (gdc1_P3_primX)—Offset 50054h" on page 1225	00000000h
50058h	4	"reg_gdc1_P3_primY_type (gdc1_P3_primY)—Offset 50058h" on page 1226	00000000h
5005Ch	4	"reg_gdc1_perf_mode_type (gdc1_perf_mode)—Offset 5005Ch" on page 1226	00000000h
50060h	4	"reg_gdc1_interp_type_type (gdc1_interp_type)—Offset 50060h" on page 1227	00000000h
50064h	4	"reg_gdc1_scan_mode_type (gdc1_scan_mode)—Offset 50064h" on page 1228	00000000h
50068h	4	"reg_gdc1_proc_mode_type (gdc1_proc_mode)—Offset 50068h" on page 1228	00000000h
60000h	4	"reg_gdc2_reg0_type (gdc2_reg0)—Offset 60000h" on page 1229	00000000h
60004h	4	"reg_gdc2_woi_x_type (gdc2_woi_x)—Offset 60004h" on page 1230	00000000h
60008h	4	"reg_gdc2_woi_y_type (gdc2_woi_y)—Offset 60008h" on page 1230	00000000h
6000Ch	4	"reg_gdc2_bpp_type (gdc2_bpp)—Offset 6000Ch" on page 1231	00000000h
60010h	4	"reg_gdc2_fryipxfrx_start_type (gdc2_fryipxfrx_start)—Offset 60010h" on page 1231	00000000h

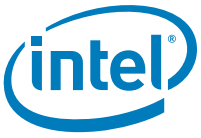


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
60014h	4	"reg_gdc2_oxdim_type (gdc2_oxdim)—Offset 60014h" on page 1232	00000000h
60018h	4	"reg_gdc2_oydim_type (gdc2_oydim)—Offset 60018h" on page 1232	00000000h
6001Ch	4	"reg_gdc2_src_addr_type (gdc2_src_addr)—Offset 6001Ch" on page 1233	00000000h
60020h	4	"reg_gdc2_src_end_type (gdc2_src_end)—Offset 60020h" on page 1233	00000000h
60024h	4	"reg_gdc2_src_wrap_type (gdc2_src_wrap)—Offset 60024h" on page 1234	00000000h
60028h	4	"reg_gdc2_src_stride_type (gdc2_src_stride)—Offset 60028h" on page 1234	00000000h
6002Ch	4	"reg_gdc2_dst_addr_type (gdc2_dst_addr)—Offset 6002Ch" on page 1235	00000000h
60030h	4	"reg_gdc2_dst_stride_type (gdc2_dst_stride)—Offset 60030h" on page 1236	00000000h
60034h	4	"reg_gdc2_dx_type (gdc2_dx)—Offset 60034h" on page 1236	00000000h
60038h	4	"reg_gdc2_dy_type (gdc2_dy)—Offset 60038h" on page 1237	00000000h
6003Ch	4	"reg_gdc2_P0_primX_ixdim_type (gdc2_P0_primX_ixdim)—Offset 6003Ch" on page 1237	00000000h
60040h	4	"reg_gdc2_P0_primY_iydim_type (gdc2_P0_primY_iydim)—Offset 60040h" on page 1238	00000000h
60044h	4	"reg_gdc2_P1_primX_type (gdc2_P1_primX)—Offset 60044h" on page 1238	00000000h
60048h	4	"reg_gdc2_P1_primY_type (gdc2_P1_primY)—Offset 60048h" on page 1239	00000000h
6004Ch	4	"reg_gdc2_P2_primX_type (gdc2_P2_primX)—Offset 6004Ch" on page 1239	00000000h
60050h	4	"reg_gdc2_P2_primY_type (gdc2_P2_primY)—Offset 60050h" on page 1240	00000000h
60054h	4	"reg_gdc2_P3_primX_type (gdc2_P3_primX)—Offset 60054h" on page 1241	00000000h
60058h	4	"reg_gdc2_P3_primY_type (gdc2_P3_primY)—Offset 60058h" on page 1241	00000000h
6005Ch	4	"reg_gdc2_perf_mode_type (gdc2_perf_mode)—Offset 6005Ch" on page 1242	00000000h
60060h	4	"reg_gdc2_interp_type_type (gdc2_interp_type)—Offset 60060h" on page 1242	00000000h
60064h	4	"reg_gdc2_scan_mode_type (gdc2_scan_mode)—Offset 60064h" on page 1243	00000000h
60068h	4	"reg_gdc2_proc_mode_type (gdc2_proc_mode)—Offset 60068h" on page 1244	00000000h

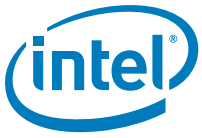


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
70000h	4	"reg_data_out_sys_c_mmu_MMU_invalidate_cache_type (data_out_sys_c_mmu_MMU_invalidate_cache)—Offset 70000h" on page 1244	00000000h
70004h	4	"reg_data_out_sys_c_mmu_MMU_page_table_base_type (data_out_sys_c_mmu_MMU_page_table_base)—Offset 70004h" on page 1245	00000000h
80100h	4	"reg_inp_sys_csi_receiver_csi1_dev_ready_type (inp_sys_csi_receiver_csi1_dev_ready)—Offset 80100h" on page 1246	00000000h
80104h	4	"reg_inp_sys_csi_receiver_csi1_int_status_type (inp_sys_csi_receiver_csi1_int_status)—Offset 80104h" on page 1247	00000000h
80108h	4	"reg_inp_sys_csi_receiver_csi1_int_enable_type (inp_sys_csi_receiver_csi1_int_enable)—Offset 80108h" on page 1248	00000000h
8010Ch	4	"reg_inp_sys_csi_receiver_csi1_func_prg_type (inp_sys_csi_receiver_csi1_func_prg)—Offset 8010Ch" on page 1250	0007FFFFh
80110h	4	"reg_inp_sys_csi_receiver_csi1_init_cnt_type (inp_sys_csi_receiver_csi1_init_cnt)—Offset 80110h" on page 1250	00000000h
8011Ch	4	"reg_inp_sys_csi_receiver_csi_backend_fs_ls_type (inp_sys_csi_receiver_csi_backend_fs_ls)—Offset 8011Ch" on page 1251	00000002h
80120h	4	"reg_inp_sys_csi_receiver_csi_backend_ls_dvalid_type (inp_sys_csi_receiver_csi_backend_ls_dvalid)—Offset 80120h" on page 1252	00000002h
80124h	4	"reg_inp_sys_csi_receiver_csi_backend_dvalid_le_type (inp_sys_csi_receiver_csi_backend_dvalid_le)—Offset 80124h" on page 1252	00000002h
80128h	4	"reg_inp_sys_csi_receiver_csi_backend_le_fe_type (inp_sys_csi_receiver_csi_backend_le_fe)—Offset 80128h" on page 1253	00000002h
8012Ch	4	"reg_inp_sys_csi_receiver_csi_backend_fe_fs_type (inp_sys_csi_receiver_csi_backend_fe_fs)—Offset 8012Ch" on page 1254	00000002h
80130h	4	"reg_inp_sys_csi_receiver_csi_backend_le_ls_type (inp_sys_csi_receiver_csi_backend_le_ls)—Offset 80130h" on page 1255	00000004h
80134h	4	"reg_inp_sys_csi_receiver_csi_backend_two_pixel_en_type (inp_sys_csi_receiver_csi_backend_two_pixel_en)—Offset 80134h" on page 1255	00000000h
80138h	4	"reg_inp_sys_csi_receiver_csi1_raw16_18_data_id_type (inp_sys_csi_receiver_csi1_raw16_18_data_id)—Offset 80138h" on page 1256	00000000h

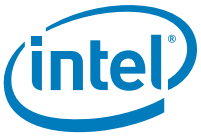


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
8013Ch	4	"reg_inp_sys_csi_receiver_csi1_sync_cnt_type (inp_sys_csi_receiver_csi1_sync_cnt)—Offset 8013Ch" on page 1257	FFFFFFFFh
80140h	4	"reg_inp_sys_csi_receiver_csi1_rx_cnt_type (inp_sys_csi_receiver_csi1_rx_cnt)—Offset 80140h" on page 1258	FFFFFFFFh
80144h	4	"reg_inp_sys_csi_receiver_csi_backend_rst_type (inp_sys_csi_receiver_csi_backend_rst)—Offset 80144h" on page 1258	00000000h
80148h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0)—Offset 80148h" on page 1259	00000000h
8014Ch	4	"reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc0_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc0)—Offset 8014Ch" on page 1261	00000000h
80150h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1)—Offset 80150h" on page 1261	00000000h
80154h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc1_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc1)—Offset 80154h" on page 1263	00000000h
80158h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2)—Offset 80158h" on page 1264	00000000h
8015Ch	4	"reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc2_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc2)—Offset 8015Ch" on page 1265	00000000h
80160h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3)—Offset 80160h" on page 1266	00000000h
80164h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc3_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc3)—Offset 80164h" on page 1268	00000000h
80168h	4	"reg_inp_sys_csi_receiver_csi_backend_raw18_reg_type (inp_sys_csi_receiver_csi_backend_raw18_reg)—Offset 80168h" on page 1268	00000000h
8016Ch	4	"reg_inp_sys_csi_receiver_csi_backend_force_raw8_reg_type (inp_sys_csi_receiver_csi_backend_force_raw8_reg)—Offset 8016Ch" on page 1269	00000000h
80170h	4	"reg_inp_sys_csi_receiver_csi_backend_raw16_reg_type (inp_sys_csi_receiver_csi_backend_raw16_reg)—Offset 80170h" on page 1270	00000000h
80200h	4	"reg_inp_sys_csi_receiver_csi2_dev_ready_type (inp_sys_csi_receiver_csi2_dev_ready)—Offset 80200h" on page 1271	00000000h

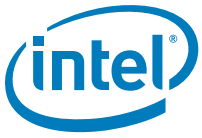


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
80204h	4	"reg_inp_sys_csi_receiver_csi2_int_status_type (inp_sys_csi_receiver_csi2_int_status)—Offset 80204h" on page 1272	00000000h
80208h	4	"reg_inp_sys_csi_receiver_csi2_int_enable_type (inp_sys_csi_receiver_csi2_int_enable)—Offset 80208h" on page 1274	00000000h
8020Ch	4	"reg_inp_sys_csi_receiver_csi2_func_prg_type (inp_sys_csi_receiver_csi2_func_prg)—Offset 8020Ch" on page 1275	0007FFFFh
80210h	4	"reg_inp_sys_csi_receiver_csi2_init_cnt_type (inp_sys_csi_receiver_csi2_init_cnt)—Offset 80210h" on page 1276	00000000h
80238h	4	"reg_inp_sys_csi_receiver_csi2_raw16_18_data_id_type (inp_sys_csi_receiver_csi2_raw16_18_data_id)—Offset 80238h" on page 1276	00000000h
8023Ch	4	"reg_inp_sys_csi_receiver_csi2_sync_cnt_type (inp_sys_csi_receiver_csi2_sync_cnt)—Offset 8023Ch" on page 1277	000000FFh
80240h	4	"reg_inp_sys_csi_receiver_csi2_rx_cnt_type (inp_sys_csi_receiver_csi2_rx_cnt)—Offset 80240h" on page 1278	000000FFh
80300h	4	"reg_inp_sys_csi_receiver_csi3_dev_ready_type (inp_sys_csi_receiver_csi3_dev_ready)—Offset 80300h" on page 1279	00000000h
80304h	4	"reg_inp_sys_csi_receiver_csi3_int_status_type (inp_sys_csi_receiver_csi3_int_status)—Offset 80304h" on page 1280	00000000h
80308h	4	"reg_inp_sys_csi_receiver_csi3_int_enable_type (inp_sys_csi_receiver_csi3_int_enable)—Offset 80308h" on page 1281	00000000h
8030Ch	4	"reg_inp_sys_csi_receiver_csi3_func_prg_type (inp_sys_csi_receiver_csi3_func_prg)—Offset 8030Ch" on page 1282	0007FFFFh
80310h	4	"reg_inp_sys_csi_receiver_csi3_init_cnt_type (inp_sys_csi_receiver_csi3_init_cnt)—Offset 80310h" on page 1283	00000000h
80338h	4	"reg_inp_sys_csi_receiver_csi3_raw16_18_data_id_type (inp_sys_csi_receiver_csi3_raw16_18_data_id)—Offset 80338h" on page 1284	00000000h
8033Ch	4	"reg_inp_sys_csi_receiver_csi3_sync_cnt_type (inp_sys_csi_receiver_csi3_sync_cnt)—Offset 8033Ch" on page 1285	0000FFFFh
80340h	4	"reg_inp_sys_csi_receiver_csi3_rx_cnt_type (inp_sys_csi_receiver_csi3_rx_cnt)—Offset 80340h" on page 1285	00000000h

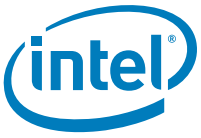


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
80800h	4	"reg_inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl_type (inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl)—Offset 80800h" on page 1286	00000000h
80804h	4	"reg_inp_sys_csi_receiver_csi_sh_be_srst_type (inp_sys_csi_receiver_csi_sh_be_srst)—Offset 80804h" on page 1287	00000000h
80808h	4	"reg_inp_sys_csi_receiver_csi_sh_be_two_ppc_type (inp_sys_csi_receiver_csi_sh_be_two_ppc)—Offset 80808h" on page 1288	00000000h
8080Ch	4	"reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0)—Offset 8080Ch" on page 1289	00000000h
80810h	4	"reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1)—Offset 80810h" on page 1290	00000000h
80814h	4	"reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2)—Offset 80814h" on page 1291	00000000h
80818h	4	"reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3)—Offset 80818h" on page 1293	00000000h
8081Ch	4	"reg_inp_sys_csi_receiver_csi_sh_be_sel_be_type (inp_sys_csi_receiver_csi_sh_be_sel_be)—Offset 8081Ch" on page 1294	00000000h
80820h	4	"reg_inp_sys_csi_receiver_csi_sh_be_raw16_reg_type (inp_sys_csi_receiver_csi_sh_be_raw16_reg)—Offset 80820h" on page 1295	00000000h
80824h	4	"reg_inp_sys_csi_receiver_csi_sh_be_raw18_reg_type (inp_sys_csi_receiver_csi_sh_be_raw18_reg)—Offset 80824h" on page 1295	00000000h
80828h	4	"reg_inp_sys_csi_receiver_csi_sh_be_force_raw8_reg_type (inp_sys_csi_receiver_csi_sh_be_force_raw8_reg)—Offset 80828h" on page 1296	00000000h
8082Ch	4	"reg_inp_sys_csi_receiver_csi_sh_be_irq_stat_reg_type (inp_sys_csi_receiver_csi_sh_be_irq_stat_reg)—Offset 8082Ch" on page 1297	00000000h
80830h	4	"reg_inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg_type (inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg)—Offset 80830h" on page 1298	00000000h
80834h	4	"reg_inp_sys_csi_receiver_csi_sh_be_custom_enable_reg_type (inp_sys_csi_receiver_csi_sh_be_custom_enable_reg)—Offset 80834h" on page 1299	00000000h
81000h	4	"reg_inp_sys_capt_unit_a_reg_CaptStartMode_type (inp_sys_capt_unit_a_reg_CaptStartMode)—Offset 81000h" on page 1300	00000000h

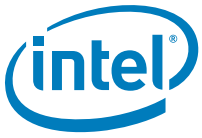


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
81004h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Start_Addr_type (inp_sys_capt_unit_a_reg_Capt_Start_Addr)—Offset 81004h" on page 1301	00000000h
81008h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size)—Offset 81008h" on page 1302	00000080h
8100Ch	4	"reg_inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions)—Offset 8100Ch" on page 1302	00000003h
81010h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Init_type (inp_sys_capt_unit_a_reg_Capt_Init)—Offset 81010h" on page 1303	00000000h
81014h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Start_Addr_type (inp_sys_capt_unit_a_reg_Capt_Start_Addr)—Offset 81004h" on page 1301	00000000h
81018h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Stop_type (inp_sys_capt_unit_a_reg_Capt_Stop)—Offset 81018h" on page 1305	00000000h
8101Ch	4	"reg_inp_sys_capt_unit_a_reg_Capt_Packet_Length_type (inp_sys_capt_unit_a_reg_Capt_Packet_Length)—Offset 8101Ch" on page 1306	00000000h
81020h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Received_Length_type (inp_sys_capt_unit_a_reg_Capt_Received_Length)—Offset 81020h" on page 1306	00000000h
81024h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets)—Offset 81024h" on page 1307	00000000h
81028h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets)—Offset 81028h" on page 1308	00000000h
8102Ch	4	"reg_inp_sys_capt_unit_a_reg_Capt_Last_Command_type (inp_sys_capt_unit_a_reg_Capt_Last_Command)—Offset 8102Ch" on page 1308	0000000Fh
81030h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Next_Command_type (inp_sys_capt_unit_a_reg_Capt_Next_Command)—Offset 81030h" on page 1309	0000000Fh
81034h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge)—Offset 81034h" on page 1310	0000000Fh
81038h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge)—Offset 81038h" on page 1310	0000000Fh
8103Ch	4	"reg_inp_sys_capt_unit_a_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_a_reg_Capt_FSM_State_Info)—Offset 8103Ch" on page 1311	00000000h

Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
82000h	4	"reg_inp_sys_capt_unit_b_reg_CaptStartMode_type (inp_sys_capt_unit_b_reg_CaptStartMode)—Offset 82000h" on page 1312	00000000h
82004h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Start_Addr_type (inp_sys_capt_unit_b_reg_Capt_Start_Addr)—Offset 82004h" on page 1313	00000000h
82008h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size)—Offset 82008h" on page 1313	00000080h
8200Ch	4	"reg_inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions)—Offset 8200Ch" on page 1314	00000003h
82010h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Init_type (inp_sys_capt_unit_b_reg_Capt_Init)—Offset 82010h" on page 1315	00000000h
82014h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Start_Addr_type (inp_sys_capt_unit_b_reg_Capt_Start_Addr)—Offset 82004h" on page 1313	00000000h
82018h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Stop_type (inp_sys_capt_unit_b_reg_Capt_Stop)—Offset 82018h" on page 1317	00000000h
8201Ch	4	"reg_inp_sys_capt_unit_b_reg_Capt_Packet_Length_type (inp_sys_capt_unit_b_reg_Capt_Packet_Length)—Offset 8201Ch" on page 1317	00000000h
82020h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Received_Length_type (inp_sys_capt_unit_b_reg_Capt_Received_Length)—Offset 82020h" on page 1318	00000000h
82024h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets)—Offset 82024h" on page 1319	00000000h
82028h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets)—Offset 82028h" on page 1319	00000000h
8202Ch	4	"reg_inp_sys_capt_unit_b_reg_Capt_Last_Command_type (inp_sys_capt_unit_b_reg_Capt_Last_Command)—Offset 8202Ch" on page 1320	0000000Fh
82030h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Next_Command_type (inp_sys_capt_unit_b_reg_Capt_Next_Command)—Offset 82030h" on page 1321	0000000Fh
82034h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge)—Offset 82034h" on page 1321	0000000Fh
82038h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge)—Offset 82038h" on page 1322	0000000Fh

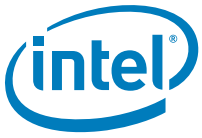


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
8203Ch	4	"reg_inp_sys_capt_unit_b_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_b_reg_Capt_FSM_State_Info)—Offset 8203Ch" on page 1323	00000000h
83000h	4	"reg_inp_sys_capt_unit_c_reg_CaptStartMode_type (inp_sys_capt_unit_c_reg_CaptStartMode)—Offset 83000h" on page 1324	00000000h
83004h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Start_Addr_type (inp_sys_capt_unit_c_reg_Capt_Start_Addr)—Offset 83004h" on page 1324	00000000h
83008h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size)—Offset 83008h" on page 1325	00000080h
8300Ch	4	"reg_inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions)—Offset 8300Ch" on page 1326	00000003h
83010h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Init_type (inp_sys_capt_unit_c_reg_Capt_Init)—Offset 83010h" on page 1326	00000000h
83014h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Start_Addr_type (inp_sys_capt_unit_c_reg_Capt_Start_Addr)—Offset 83004h" on page 1324	00000000h
83018h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Stop_type (inp_sys_capt_unit_c_reg_Capt_Stop)—Offset 83018h" on page 1328	00000000h
8301Ch	4	"reg_inp_sys_capt_unit_c_reg_Capt_Packet_Length_type (inp_sys_capt_unit_c_reg_Capt_Packet_Length)—Offset 8301Ch" on page 1329	00000000h
83020h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Received_Length_type (inp_sys_capt_unit_c_reg_Capt_Received_Length)—Offset 83020h" on page 1329	00000000h
83024h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets)—Offset 83024h" on page 1330	00000000h
83028h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets)—Offset 83028h" on page 1331	00000000h
8302Ch	4	"reg_inp_sys_capt_unit_c_reg_Capt_Last_Command_type (inp_sys_capt_unit_c_reg_Capt_Last_Command)—Offset 8302Ch" on page 1331	0000000Fh
83030h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Next_Command_type (inp_sys_capt_unit_c_reg_Capt_Next_Command)—Offset 83030h" on page 1332	0000000Fh
83034h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge)—Offset 83034h" on page 1333	0000000Fh

Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
83038h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge)—Offset 83038h" on page 1333	0000000Fh
8303Ch	4	"reg_inp_sys_capt_unit_c_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_c_reg_Capt_FSM_State_Info)—Offset 8303Ch" on page 1334	00000000h
84000h	4	"reg_inp_sys_acq_unit_reg_Acq_Start_Addr_type (inp_sys_acq_unit_reg_Acq_Start_Addr)—Offset 84000h" on page 1335	00000000h
84004h	4	"reg_inp_sys_acq_unit_reg_Acq_Mem_Region_Size_type (inp_sys_acq_unit_reg_Acq_Mem_Region_Size)—Offset 84004h" on page 1336	00000080h
84008h	4	"reg_inp_sys_acq_unit_reg_Acq_Num_Mem_Regions_type (inp_sys_acq_unit_reg_Acq_Num_Mem_Regions)—Offset 84008h" on page 1336	00000003h
8400Ch	4	"reg_inp_sys_acq_unit_reg_Acq_Init_type (inp_sys_acq_unit_reg_Acq_Init)—Offset 8400Ch" on page 1337	00000000h
84010h	4	"reg_inp_sys_acq_unit_reg_Acq_Received_Short_Packets_type (inp_sys_acq_unit_reg_Acq_Received_Short_Packets)—Offset 84010h" on page 1338	00000000h
84014h	4	"reg_inp_sys_acq_unit_reg_Acq_Received_Long_Packets_type (inp_sys_acq_unit_reg_Acq_Received_Long_Packets)—Offset 84014h" on page 1339	00000000h
84018h	4	"reg_inp_sys_acq_unit_reg_Acq_Last_Command_type (inp_sys_acq_unit_reg_Acq_Last_Command)—Offset 84018h" on page 1339	0000000Fh
8401Ch	4	"reg_inp_sys_acq_unit_reg_Acq_Next_Command_type (inp_sys_acq_unit_reg_Acq_Next_Command)—Offset 8401Ch" on page 1340	0000000Fh
84020h	4	"reg_inp_sys_acq_unit_reg_Acq_Last_Acknowledge_type (inp_sys_acq_unit_reg_Acq_Last_Acknowledge)—Offset 84020h" on page 1341	0000000Fh
84024h	4	"reg_inp_sys_acq_unit_reg_Acq_Next_Acknowledge_type (inp_sys_acq_unit_reg_Acq_Next_Acknowledge)—Offset 84024h" on page 1341	0000000Fh
84028h	4	"reg_inp_sys_acq_unit_reg_Acq_FSM_State_Info_type (inp_sys_acq_unit_reg_Acq_FSM_State_Info)—Offset 84028h" on page 1342	00000000h
8402Ch	4	"reg_inp_sys_acq_unit_reg_Acq_Int_Cntr_Info_type (inp_sys_acq_unit_reg_Acq_Int_Cntr_Info)—Offset 8402Ch" on page 1343	00000000h
85000h	4	"reg_inp_sys_dma_DMA_FSM_Command_type (inp_sys_dma_DMA_FSM_Command)—Offset 85000h" on page 1344	00000000h

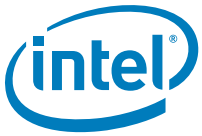


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
86000h	4	"reg_inp_sys_dma_DMA_CH0_Packing_setup_type (inp_sys_dma_DMA_CH0_Packing_setup)—Offset 86000h" on page 1345	00000000h
86100h	4	"reg_inp_sys_dma_DMA_CH0_dev_stride_A_type (inp_sys_dma_DMA_CH0_dev_stride_A)—Offset 86100h" on page 1345	00000000h
86200h	4	"reg_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A_type (inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A)—Offset 86200h" on page 1346	00000000h
86300h	4	"reg_inp_sys_dma_DMA_CH0_Device_Xb_A_type (inp_sys_dma_DMA_CH0_Device_Xb_A)—Offset 86300h" on page 1347	00000000h
86400h	4	"reg_inp_sys_dma_DMA_CH0_dev_stride_B_type (inp_sys_dma_DMA_CH0_dev_stride_B)—Offset 86400h" on page 1348	00000000h
86500h	4	"reg_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B_type (inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B)—Offset 86500h" on page 1349	00000000h
86600h	4	"reg_inp_sys_dma_DMA_CH0_Device_Xb_B_type (inp_sys_dma_DMA_CH0_Device_Xb_B)—Offset 86600h" on page 1350	00000000h
86700h	4	"reg_inp_sys_dma_DMA_CH0_Yb_type (inp_sys_dma_DMA_CH0_Yb)—Offset 86700h" on page 1350	00000000h
86800h	4	"reg_inp_sys_dma_DMA_CH0_pending_command_type (inp_sys_dma_DMA_CH0_pending_command)—Offset 86800h" on page 1351	00000000h
87000h	4	"reg_inp_sys_dma_DMA_command_token_type (inp_sys_dma_DMA_command_token)—Offset 87000h" on page 1352	00000000h
87004h	4	"reg_inp_sys_dma_DMA_command_src_addr_type (inp_sys_dma_DMA_command_src_addr)—Offset 87004h" on page 1352	00000000h
87008h	4	"reg_inp_sys_dma_DMA_command_dst_addr_type (inp_sys_dma_DMA_command_dst_addr)—Offset 87008h" on page 1353	00000000h
8700Ch	4	"reg_inp_sys_dma_DMA_command_ctrl_id_type (inp_sys_dma_DMA_command_ctrl_id)—Offset 8700Ch" on page 1354	00000000h
87010h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_status_type (inp_sys_dma_DMA_FSM_Ctrl_status)—Offset 87010h" on page 1354	00000001h
87014h	4	"reg_inp_sys_dma_DMA_FSM_Pack_status_type (inp_sys_dma_DMA_FSM_Pack_status)—Offset 87014h" on page 1355	00000000h

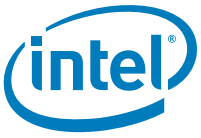


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
87018h	4	"reg_inp_sys_dma_DMA_FSM_request_status_type (inp_sys_dma_DMA_FSM_request_status)—Offset 87018h" on page 1356	00000000h
8701Ch	4	"reg_inp_sys_dma_DMA_FSM_write_status_type (inp_sys_dma_DMA_FSM_write_status)—Offset 8701Ch" on page 1357	00000000h
87110h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_dev_idx)—Offset 87110h" on page 1358	00000000h
87114h	4	"reg_inp_sys_dma_DMA_FSM_Pack_cnt_Yb_type (inp_sys_dma_DMA_FSM_Pack_cnt_Yb)—Offset 87114h" on page 1358	00000000h
87118h	4	"reg_inp_sys_dma_DMA_FSM_Request_cnt_Yb_type (inp_sys_dma_DMA_FSM_Request_cnt_Yb)—Offset 87118h" on page 1359	00000000h
8711Ch	4	"reg_inp_sys_dma_DMA_FSM_Write_cnt_Y_type (inp_sys_dma_DMA_FSM_Write_cnt_Y)—Offset 8711Ch" on page 1360	00000000h
87210h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_req_addr_type (inp_sys_dma_DMA_FSM_Ctrl_req_addr)—Offset 87210h" on page 1360	00000000h
87214h	4	"reg_inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb_type (inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb)—Offset 87214h" on page 1361	00000000h
87218h	4	"reg_inp_sys_dma_DMA_FSM_Request_cnt_Xb_type (inp_sys_dma_DMA_FSM_Request_cnt_Xb)—Offset 87218h" on page 1362	00000000h
8721Ch	4	"reg_inp_sys_dma_DMA_FSM_Write_cnt_Xb_type (inp_sys_dma_DMA_FSM_Write_cnt_Xb)—Offset 8721Ch" on page 1362	00000000h
87310h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_req_stride_type (inp_sys_dma_DMA_FSM_Ctrl_req_stride)—Offset 87310h" on page 1363	00000000h
87314h	4	"reg_inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb_type (inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb)—Offset 87314h" on page 1364	00000000h
87318h	4	"reg_inp_sys_dma_DMA_FSM_Req_remining_Xb_type (inp_sys_dma_DMA_FSM_Req_remining_Xb)—Offset 87318h" on page 1365	00000000h
8731Ch	4	"reg_inp_sys_dma_DMA_FSM_Wr_remining_Xb_type (inp_sys_dma_DMA_FSM_Wr_remining_Xb)—Offset 8731Ch" on page 1365	00000000h
87410h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_req_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_req_Xb)—Offset 87410h" on page 1366	00000000h

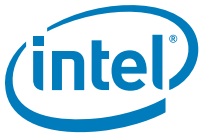


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
87418h	4	"reg_inp_sys_dma_DMA_FSM_Req_burst_cnt_type (inp_sys_dma_DMA_FSM_Req_burst_cnt)—Offset 87418h" on page 1367	0000FFFFh
8741Ch	4	"reg_inp_sys_dma_DMA_FSM_Wr_burst_cnt_type (inp_sys_dma_DMA_FSM_Wr_burst_cnt)—Offset 8741Ch" on page 1368	0000FFFFh
87510h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_req_Yb_type (inp_sys_dma_DMA_FSM_Ctrl_req_Yb)—Offset 87510h" on page 1368	00000000h
87610h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx)—Offset 87610h" on page 1369	00000000h
87710h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx)—Offset 87710h" on page 1370	00000000h
87810h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_Wr_addr_type (inp_sys_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 87810h" on page 1371	00000000h
87910h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_Wr_stride_type (inp_sys_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 87910h" on page 1372	00000000h
87A10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb)—Offset 87A10h" on page 1372	00000000h
87B10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_Yb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_Yb)—Offset 87B10h" on page 1373	00000000h
87C10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb)—Offset 87C10h" on page 1374	00000000h
87D10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem_type (inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 87D10h" on page 1374	00000000h
87E10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem_type (inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 87E10h" on page 1375	00000000h
87F10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id_type (inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id)—Offset 87F10h" on page 1376	00000000h
88000h	4	"reg_inp_sys_dma_Dev_Interf_0_req_side_type (inp_sys_dma_Dev_Interf_0_req_side)—Offset 88000h" on page 1377	00000000h
88004h	4	"reg_inp_sys_dma_Dev_Interf_1_req_side_type (inp_sys_dma_Dev_Interf_1_req_side)—Offset 88004h" on page 1378	00000006h

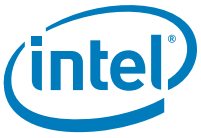


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
88100h	4	"reg_inp_sys_dma_Dev_Interf_0_snd_side_type (inp_sys_dma_Dev_Interf_0_snd_side)—Offset 88100h" on page 1379	00000004h
88104h	4	"reg_inp_sys_dma_Dev_Interf_1_snd_side_type (inp_sys_dma_Dev_Interf_1_snd_side)—Offset 88104h" on page 1380	00000006h
88200h	4	"reg_inp_sys_dma_Dev_Interf_0_Fifo_status_type (inp_sys_dma_Dev_Interf_0_Fifo_status)—Offset 88200h" on page 1381	00000004h
88204h	4	"reg_inp_sys_dma_Dev_Interf_1_Fifo_status_type (inp_sys_dma_Dev_Interf_1_Fifo_status)—Offset 88204h" on page 1382	00000004h
88300h	4	"reg_inp_sys_dma_Dev_Interf_0_Req_complete_bust_type (inp_sys_dma_Dev_Interf_0_Req_complete_bust)—Offset 88300h" on page 1383	00000000h
88304h	4	"reg_inp_sys_dma_Dev_Interf_1_Req_complete_bust_type (inp_sys_dma_Dev_Interf_1_Req_complete_bust)—Offset 88304h" on page 1384	00000000h
88400h	4	"reg_inp_sys_dma_Dev_Interf_1_Max_burst_Size_type (inp_sys_dma_Dev_Interf_1_Max_burst_Size)—Offset 88400h" on page 1385	0000007Fh
89000h	4	"reg_inp_sys_inp_ctrl_inpsys_captA_start_addr_type (inp_sys_inp_ctrl_inpsys_captA_start_addr)—Offset 89000h" on page 1386	00000000h
89004h	4	"reg_inp_sys_inp_ctrl_inpsys_captB_start_addr_type (inp_sys_inp_ctrl_inpsys_captB_start_addr)—Offset 89004h" on page 1387	00000000h
89008h	4	"reg_inp_sys_inp_ctrl_inpsys_captC_start_addr_type (inp_sys_inp_ctrl_inpsys_captC_start_addr)—Offset 89008h" on page 1388	00000000h
8900Ch	4	"reg_inp_sys_inp_ctrl_inpsys_captA_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captA_mem_region_size)—Offset 8900Ch" on page 1388	00000080h
89010h	4	"reg_inp_sys_inp_ctrl_inpsys_captB_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captB_mem_region_size)—Offset 89010h" on page 1389	00000080h
89014h	4	"reg_inp_sys_inp_ctrl_inpsys_captC_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captC_mem_region_size)—Offset 89014h" on page 1390	00000080h
89018h	4	"reg_inp_sys_inp_ctrl_inpsys_captA_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captA_num_mem_regions)—Offset 89018h" on page 1391	00000003h
8901Ch	4	"reg_inp_sys_inp_ctrl_inpsys_captB_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captB_num_mem_regions)—Offset 8901Ch" on page 1392	00000003h

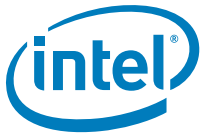


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
89020h	4	"reg_inp_sys_inp_ctrl_inpsys_captC_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captC_num_mem_regions)—Offset 89020h" on page 1393	00000003h
89024h	4	"reg_inp_sys_inp_ctrl_inpsys_acq_start_addr_type (inp_sys_inp_ctrl_inpsys_acq_start_addr)—Offset 89024h" on page 1394	00000000h
89028h	4	"reg_inp_sys_inp_ctrl_inpsys_acq_mem_region_size_type (inp_sys_inp_ctrl_inpsys_acq_mem_region_size)—Offset 89028h" on page 1395	00000080h
8902Ch	4	"reg_inp_sys_inp_ctrl_inpsys_acq_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_acq_num_mem_regions)—Offset 8902Ch" on page 1396	00000003h
89030h	4	"reg_inp_sys_inp_ctrl_inpsys_ctrl_init_type (inp_sys_inp_ctrl_inpsys_ctrl_init)—Offset 89030h" on page 1396	00000000h
89034h	4	"reg_inp_sys_inp_ctrl_inpsys_last_cmd_type (inp_sys_inp_ctrl_inpsys_last_cmd)—Offset 89034h" on page 1397	0000000Fh
89038h	4	"reg_inp_sys_inp_ctrl_inpsys_next_cmd_type (inp_sys_inp_ctrl_inpsys_next_cmd)—Offset 89038h" on page 1398	0000000Fh
8903Ch	4	"reg_inp_sys_inp_ctrl_inpsys_last_ack_type (inp_sys_inp_ctrl_inpsys_last_ack)—Offset 8903Ch" on page 1398	0000000Fh
89040h	4	"reg_inp_sys_inp_ctrl_inpsys_next_ack_type (inp_sys_inp_ctrl_inpsys_next_ack)—Offset 89040h" on page 1399	0000000Fh
89044h	4	"reg_inp_sys_inp_ctrl_inpsys_top_fsm_state_type (inp_sys_inp_ctrl_inpsys_top_fsm_state)—Offset 89044h" on page 1399	00000000h
89048h	4	"reg_inp_sys_inp_ctrl_inpsys_captA_fsm_state_type (inp_sys_inp_ctrl_inpsys_captA_fsm_state)—Offset 89048h" on page 1400	00000000h
8904Ch	4	"reg_inp_sys_inp_ctrl_inpsys_captB_fsm_state_type (inp_sys_inp_ctrl_inpsys_captB_fsm_state)—Offset 8904Ch" on page 1401	00000000h
89050h	4	"reg_inp_sys_inp_ctrl_inpsys_captC_fsm_state_type (inp_sys_inp_ctrl_inpsys_captC_fsm_state)—Offset 89050h" on page 1402	00000000h
89054h	4	"reg_inp_sys_inp_ctrl_inpsys_acq_fsm_state_type (inp_sys_inp_ctrl_inpsys_acq_fsm_state)—Offset 89054h" on page 1402	00000000h
89058h	4	"reg_inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region_type (inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region)—Offset 89058h" on page 1403	00000000h

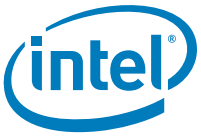


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
8A000h	4	"reg_inp_sys_gpreg_str_multicastA_sel_type (inp_sys_gpreg_str_multicastA_sel)—Offset 8A000h" on page 1404	00000000h
8A004h	4	"reg_inp_sys_gpreg_str_multicastB_sel_type (inp_sys_gpreg_str_multicastB_sel)—Offset 8A004h" on page 1405	00000000h
8A008h	4	"reg_inp_sys_gpreg_str_multicastC_sel_type (inp_sys_gpreg_str_multicastC_sel)—Offset 8A008h" on page 1406	00000000h
8A00Ch	4	"reg_inp_sys_gpreg_str_mux_sel_type (inp_sys_gpreg_str_mux_sel)—Offset 8A00Ch" on page 1406	00000000h
8A010h	4	"reg_inp_sys_gpreg_str_mon_status_type (inp_sys_gpreg_str_mon_status)—Offset 8A010h" on page 1407	00000000h
8A014h	4	"reg_inp_sys_gpreg_str_mon_irq_cond_type (inp_sys_gpreg_str_mon_irq_cond)—Offset 8A014h" on page 1408	00000000h
8A018h	4	"reg_inp_sys_gpreg_str_mon_irq_en_type (inp_sys_gpreg_str_mon_irq_en)—Offset 8A018h" on page 1409	00000000h
8A01Ch	4	"reg_inp_sys_gpreg_isys_srst_type (inp_sys_gpreg_isys_srst)—Offset 8A01Ch" on page 1411	00000000h
8A020h	4	"reg_inp_sys_gpreg_isys_slv_reg_srst_type (inp_sys_gpreg_isys_slv_reg_srst)—Offset 8A020h" on page 1412	00000000h
8A024h	4	"reg_inp_sys_gpreg_str_deint_portA_cnt_type (inp_sys_gpreg_str_deint_portA_cnt)—Offset 8A024h" on page 1413	00000000h
8A028h	4	"reg_inp_sys_gpreg_str_deint_portB_cnt_type (inp_sys_gpreg_str_deint_portB_cnt)—Offset 8A028h" on page 1414	00000000h
8B008h	4	"reg_inp_sys_fifo_adapter_CSI_generic_short_packet_available_type (inp_sys_fifo_adapter_CSI_generic_short_packet_available)—Offset 8B008h" on page 1415	00000001h
8C000h	4	"reg_inp_sys_irq_ctrl_irq_edge_type (inp_sys_irq_ctrl_irq_edge)—Offset 8C000h" on page 1415	00000000h
8C004h	4	"reg_inp_sys_irq_ctrl_irq_mask_type (inp_sys_irq_ctrl_irq_mask)—Offset 8C004h" on page 1417	00000000h
8C008h	4	"reg_inp_sys_irq_ctrl_irq_status_type (inp_sys_irq_ctrl_irq_status)—Offset 8C008h" on page 1418	00000000h
8C00Ch	4	"reg_inp_sys_irq_ctrl_irq_clear_type (inp_sys_irq_ctrl_irq_clear)—Offset 8C00Ch" on page 1419	00000000h
8C010h	4	"reg_inp_sys_irq_ctrl_irq_en_type (inp_sys_irq_ctrl_irq_en)—Offset 8C010h" on page 1420	00000000h

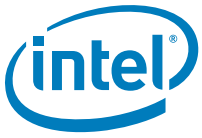


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
8C014h	4	"reg_inp_sys_irq_ctrl_irq_level_not_pulse_type (inp_sys_irq_ctrl_irq_level_not_pulse)—Offset 8C014h" on page 1421	00000000h
90000h	4	"reg_isel_gpr_reg_gp_syncgen_enable_type (isel_gpr_reg_gp_syncgen_enable)—Offset 90000h" on page 1422	00000000h
90004h	4	"reg_isel_gpr_reg_gp_syncgen_free_running_type (isel_gpr_reg_gp_syncgen_free_running)—Offset 90004h" on page 1423	00000000h
90008h	4	"reg_isel_gpr_reg_gp_syncgen_pause_type (isel_gpr_reg_gp_syncgen_pause)—Offset 90008h" on page 1424	00000000h
9000Ch	4	"reg_isel_gpr_reg_gp_nr_frames_type (isel_gpr_reg_gp_nr_frames)—Offset 9000Ch" on page 1425	00000000h
90010h	4	"reg_isel_gpr_reg_gp_syngen_nr_pix_type (isel_gpr_reg_gp_syngen_nr_pix)—Offset 90010h" on page 1425	00000000h
90014h	4	"reg_isel_gpr_reg_gp_syngen_nr_lines_type (isel_gpr_reg_gp_syngen_nr_lines)—Offset 90014h" on page 1426	00000000h
90018h	4	"reg_isel_gpr_reg_gp_syngen_hblank_cycles_type (isel_gpr_reg_gp_syngen_hblank_cycles)—Offset 90018h" on page 1427	00000000h
9001Ch	4	"reg_isel_gpr_reg_gp_syngen_vblank_cycles_type (isel_gpr_reg_gp_syngen_vblank_cycles)—Offset 9001Ch" on page 1427	00000000h
90020h	4	"reg_isel_gpr_reg_gp_isel_sof_type (isel_gpr_reg_gp_isel_sof)—Offset 90020h" on page 1428	00000000h
90024h	4	"reg_isel_gpr_reg_gp_isel_eof_type (isel_gpr_reg_gp_isel_eof)—Offset 90024h" on page 1429	00000000h
90028h	4	"reg_isel_gpr_reg_gp_isel_sol_type (isel_gpr_reg_gp_isel_sol)—Offset 90028h" on page 1430	00000000h
9002Ch	4	"reg_isel_gpr_reg_gp_isel_eol_type (isel_gpr_reg_gp_isel_eol)—Offset 9002Ch" on page 1430	00000000h
90030h	4	"reg_isel_gpr_reg_gp_isel_lfsr_enable_type (isel_gpr_reg_gp_isel_lfsr_enable)—Offset 90030h" on page 1431	00000000h
90034h	4	"reg_isel_gpr_reg_gp_isel_lfsr_enable_b_type (isel_gpr_reg_gp_isel_lfsr_enable_b)—Offset 90034h" on page 1432	00000000h
90038h	4	"reg_isel_gpr_reg_gp_isel_lfsr_reset_value_type (isel_gpr_reg_gp_isel_lfsr_reset_value)—Offset 90038h" on page 1432	00000000h

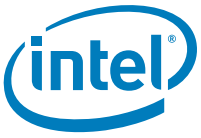


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
9003Ch	4	"reg_isel_gpr_reg_gp_isel_tpg_enable_type (isel_gpr_reg_gp_isel_tpg_enable)—Offset 9003Ch" on page 1433	00000000h
90040h	4	"reg_isel_gpr_reg_gp_isel_tpg_enable_b_type (isel_gpr_reg_gp_isel_tpg_enable_b)—Offset 90040h" on page 1434	00000000h
90044h	4	"reg_isel_gpr_reg_gp_isel_hor_cnt_mask_type (isel_gpr_reg_gp_isel_hor_cnt_mask)—Offset 90044h" on page 1434	00000000h
90048h	4	"reg_isel_gpr_reg_gp_isel_ver_cnt_mask_type (isel_gpr_reg_gp_isel_ver_cnt_mask)—Offset 90048h" on page 1435	00000000h
9004Ch	4	"reg_isel_gpr_reg_gp_isel_xy_cnt_mask_type (isel_gpr_reg_gp_isel_xy_cnt_mask)—Offset 9004Ch" on page 1436	00000000h
90050h	4	"reg_isel_gpr_reg_gp_isel_hor_cnt_delta_type (isel_gpr_reg_gp_isel_hor_cnt_delta)—Offset 90050h" on page 1436	00000000h
90054h	4	"reg_isel_gpr_reg_gp_isel_ver_cnt_delta_type (isel_gpr_reg_gp_isel_ver_cnt_delta)—Offset 90054h" on page 1437	00000000h
90058h	4	"reg_isel_gpr_reg_gp_isel_tpg_mode_type (isel_gpr_reg_gp_isel_tpg_mode)—Offset 90058h" on page 1438	00000000h
9005Ch	4	"reg_isel_gpr_reg_gp_isel_tpg_red1_type (isel_gpr_reg_gp_isel_tpg_red1)—Offset 9005Ch" on page 1438	00000000h
90060h	4	"reg_isel_gpr_reg_gp_isel_tpg_green1_type (isel_gpr_reg_gp_isel_tpg_green1)—Offset 90060h" on page 1439	00000000h
90064h	4	"reg_isel_gpr_reg_gp_isel_tpg_blue1_type (isel_gpr_reg_gp_isel_tpg_blue1)—Offset 90064h" on page 1440	00000000h
90068h	4	"reg_isel_gpr_reg_gp_isel_tpg_red2_type (isel_gpr_reg_gp_isel_tpg_red2)—Offset 90068h" on page 1440	00000000h
9006Ch	4	"reg_isel_gpr_reg_gp_isel_tpg_green2_type (isel_gpr_reg_gp_isel_tpg_green2)—Offset 9006Ch" on page 1441	00000000h
90070h	4	"reg_isel_gpr_reg_gp_isel_tpg_blue2_type (isel_gpr_reg_gp_isel_tpg_blue2)—Offset 90070h" on page 1442	00000000h
90074h	4	"reg_isel_gpr_reg_gp_isel_ch_id_type (isel_gpr_reg_gp_isel_ch_id)—Offset 90074h" on page 1442	00000000h
90078h	4	"reg_isel_gpr_reg_gp_isel_fmt_type_type (isel_gpr_reg_gp_isel_fmt_type)—Offset 90078h" on page 1443	00000000h
9007Ch	4	"reg_isel_gpr_reg_gp_isel_data_sel_type (isel_gpr_reg_gp_isel_data_sel)—Offset 9007Ch" on page 1444	00000000h
90080h	4	"reg_isel_gpr_reg_gp_isel_sband_sel_type (isel_gpr_reg_gp_isel_sband_sel)—Offset 90080h" on page 1444	00000000h

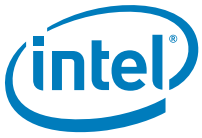


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
90084h	4	"reg_isel_gpr_reg_gp_isel_sync_sel_type (isel_gpr_reg_gp_isel_sync_sel)—Offset 90084h" on page 1445	00000000h
90088h	4	"reg_isel_gpr_reg_gp_syncgen_hor_cnt_type (isel_gpr_reg_gp_syncgen_hor_cnt)—Offset 90088h" on page 1446	00000000h
9008Ch	4	"reg_isel_gpr_reg_gp_syncgen_ver_cnt_type (isel_gpr_reg_gp_syncgen_ver_cnt)—Offset 9008Ch" on page 1446	00000000h
90090h	4	"reg_isel_gpr_reg_gp_syncgen_frame_cnt_type (isel_gpr_reg_gp_syncgen_frame_cnt)—Offset 90090h" on page 1447	00000000h
90094h	4	"reg_isel_gpr_reg_gp_soft_reset_type (isel_gpr_reg_gp_soft_reset)—Offset 90094h" on page 1448	00000000h
90100h	4	"reg_isel_fa_send_to_GP_FIFO_type (isel_fa_send_to_GP_FIFO)—Offset 90100h" on page 1449	00000000h
90108h	4	"reg_isel_fa_check_send_to_GP_FIFO_type (isel_fa_check_send_to_GP_FIFO)—Offset 90108h" on page 1449	00000001h
90200h	4	"reg_isel_irq_ctrl_reg_irq_edge_type (isel_irq_ctrl_reg_irq_edge)—Offset 90200h" on page 1450	00000000h
90204h	4	"reg_isel_irq_ctrl_reg_irq_mask_type (isel_irq_ctrl_reg_irq_mask)—Offset 90204h" on page 1451	00000000h
90208h	4	"reg_isel_irq_ctrl_reg_irq_status_type (isel_irq_ctrl_reg_irq_status)—Offset 90208h" on page 1451	00000000h
9020Ch	4	"reg_isel_irq_ctrl_reg_irq_clear_type (isel_irq_ctrl_reg_irq_clear)—Offset 9020Ch" on page 1452	00000000h
90210h	4	"reg_isel_irq_ctrl_reg_irq_enable_type (isel_irq_ctrl_reg_irq_enable)—Offset 90210h" on page 1453	00000000h
90214h	4	"reg_isel_irq_ctrl_reg_irq_level_not_pulse_type (isel_irq_ctrl_reg_irq_level_not_pulse)—Offset 90214h" on page 1453	00000000h
A0000h	4	"reg_icache_out_sys_c_mmu_MMU_invalidate_cache_type (icache_out_sys_c_mmu_MMU_invalidate_cache)—Offset A0000h" on page 1454	00000000h
A0004h	4	"reg_icache_out_sys_c_mmu_MMU_page_table_base_type (icache_out_sys_c_mmu_MMU_page_table_base)—Offset A0004h" on page 1455	00000000h
B0000h	8	"mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first)—Offset B0000h" on page 1455	0000000000000000h
B7FF8h	8	"mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last)—Offset B7FF8h" on page 1456	0000000000000000h

Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
1C0000h	2	"mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1C0000h" on page 1456	0000h
1C0FFEh	2	"mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1C0FFEh" on page 1457	0000h
1D0000h	2	"mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1D0000h" on page 1458	0000h
1D0FFEh	2	"mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1D0FFEh" on page 1458	0000h
1E0000h	2	"mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1E0000h" on page 1459	0000h
1E0FFEh	2	"mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1E0FFEh" on page 1459	0000h
1F0000h	4	"mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first)—Offset 1F0000h" on page 1460	00000000h
1F0FFCh	4	"mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last)—Offset 1F0FFCh" on page 1461	00000000h
200000h	4	"mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_first_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_first)—Offset 200000h" on page 1461	00000000h
203FFCh	4	"mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_last_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_last)—Offset 203FFCh" on page 1462	00000000h
300000h	4	"mem_scp_dmem_mem_sl_ip_dmem_mem_first_type (scp_dmem_mem_sl_ip_dmem_mem_first)—Offset 300000h" on page 1462	00000000h
307FFCh	4	"mem_scp_dmem_mem_sl_ip_dmem_mem_last_type (scp_dmem_mem_sl_ip_dmem_mem_last)—Offset 307FFCh" on page 1463	00000000h
380008h	4	"reg_fa_sp_isp_send_to_SP_type (fa_sp_isp_send_to_SP)—Offset 380008h" on page 1463	00000000h
38000Ch	4	"reg_fa_sp_isp_send_to_ISP_type (fa_sp_isp_send_to_ISP)—Offset 38000Ch" on page 1464	00000000h

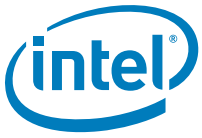


Table 15. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
380010h	4	"reg_fa_sp_isp_check_receive_from_SP_type (fa_sp_isp_check_receive_from_SP)—Offset 380010h" on page 1464	00000001h
380014h	4	"reg_fa_sp_isp_check_receive_from_ISP_type (fa_sp_isp_check_receive_from_ISP)—Offset 380014h" on page 1465	00000001h
380018h	4	"reg_fa_sp_isp_check_send_to_SP_type (fa_sp_isp_check_send_to_SP)—Offset 380018h" on page 1466	00000000h
38001Ch	4	"reg_fa_sp_isp_check_send_to_ISP_type (fa_sp_isp_check_send_to_ISP)—Offset 38001Ch" on page 1467	00000000h

3.7.1 reg_gpd_gp_reg_reg_gp_sdram_wakeup_type (gpd_gp_reg_reg_gp_sdram_wakeup)—Offset 0h

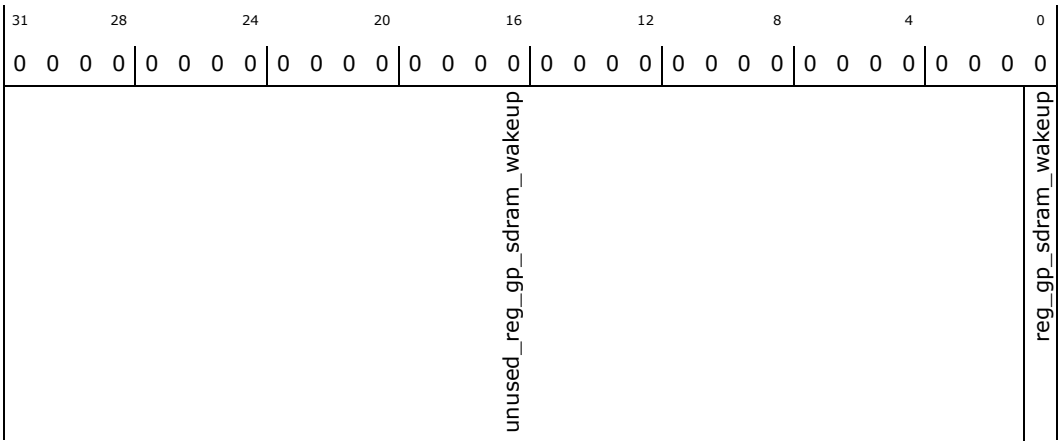
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sdram_wakeup: [ISPMMADR] + 0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_sdram_wakeup:** Unused
0	0h RW	**reg_gp_sdram_wakeup:** when set to 1, this signal will cause the memory controller to bring the external SDRAM into an active state.

3.7.2 reg_gpd_gp_reg_reg_gp_idle_type (gpd_gp_reg_reg_gp_idle)—Offset 4h

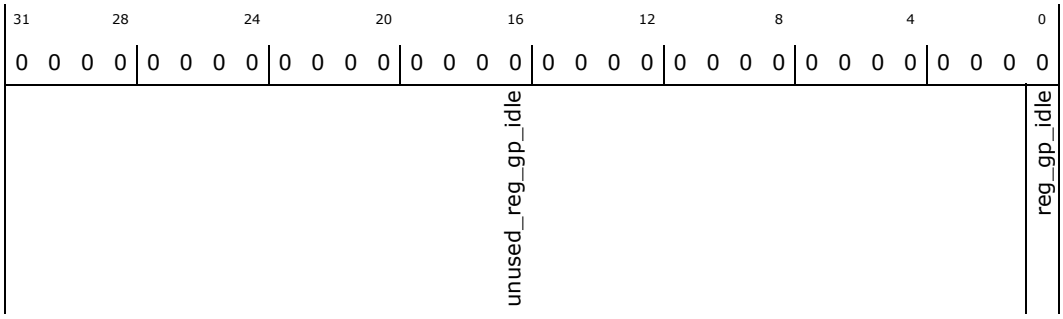
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_idle: [ISPMMADR] + 4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_idle:** Unused
0	0h RW	**reg_gp_idle:** Should be set to 1 when ISP system is in ?idle? mode.

3.7.3 reg_gpd_gp_reg_reg_gp_irq_req0_type (gpd_gp_reg_reg_gp_irq_req0)—Offset 8h

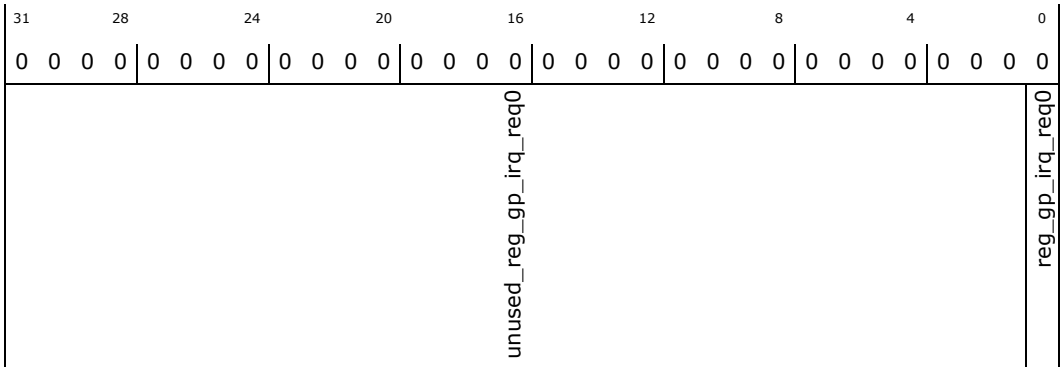
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_irq_req0: [ISPMMADR] + 8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_irq_req0:** Unused
0	0h RW	**reg_gp_irq_req0:** possibly causes an interrupt request (if the host interrupt controller is properly configured)

3.7.4 reg_gpd_gp_reg_reg_gp_irq_req1_type (gpd_gp_reg_reg_gp_irq_req1)—Offset Ch

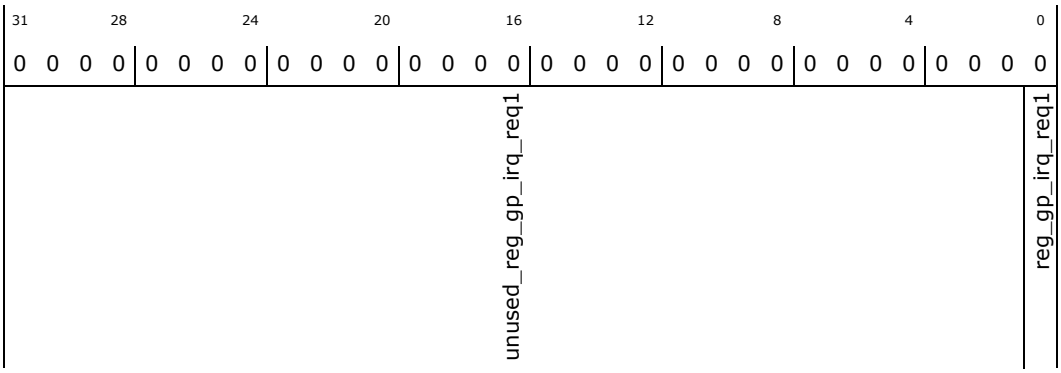
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_irq_req1: [ISPMMADR] + Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_irq_req1:** Unused
0	0h RW	**reg_gp_irq_req1:** possibly causes an interrupt request (if the host interrupt controller is properly configured)

3.7.5 reg_gpd_gp_reg_reg_gp_sp_stream_stat_type (gpd_gp_reg_reg_gp_sp_stream_stat)—Offset 10h

Indicate the status of the streaming ports of the scalar processor. All valid and accept signals of the scalar processor are reflected in this register and in reg_gp_sp_stream_stat_b.

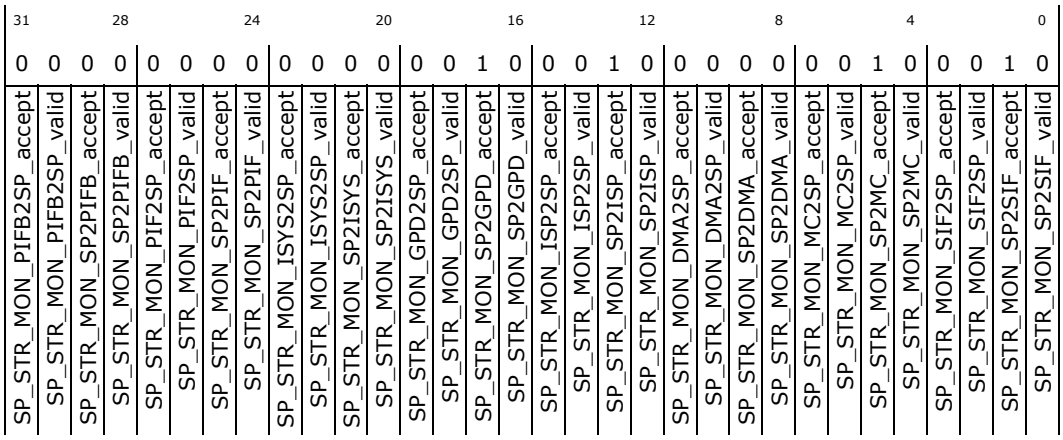
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat: [ISPMMADR] + 10h

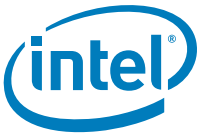
ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00022022h



Bit Range	Default & Access	Description
31	0h RO	**SP_STR_MON_PIFB2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the primary input formatter B acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
30	0h RO	**SP_STR_MON_PIFB2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter B acknowledge port and the SP, is present on the primary input formatter B input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
29	0h RO	**SP_STR_MON_SP2PIFB_accept:** Returns the value 1 if the command FIFO between SP and the Primary input formatter B can accept a command from the SP. Returns the value 0 if this FIFO cannot accept a token from the SP.
28	0h RO	**SP_STR_MON_SP2PIFB_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the Primary Input Formatter B command FIFO. Returns the value 0 if the SP does not send a command to this FIFO
27	0h RO	**SP_STR_MON_PIF2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the primary input formatter acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
26	0h RO	**SP_STR_MON_PIF2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter acknowledge port and the SP, is present on the primary input formatter input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
25	0h RO	**SP_STR_MON_SP2PIF_accept:** Returns the value 1 if the command FIFO between SP and the Primary input formatter can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.

Bit Range	Default & Access	Description
24	0h RO	**SP_STR_MON_SP2PIF_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the Primary Input Formatter command FIFO. Returns the value 0 if the SP does not send a command to the Primary Input formatter
23	0h RO	**SP_STR_MON_ISYS2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the input system acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
22	0h RO	**SP_STR_MON_ISYS2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the input system acknowledge port and the SP, is present on the input system input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
21	0h RO	**SP_STR_MON_SP2ISYS_accept:** Returns the value 1 if the command FIFO between SP and the input system can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
20	0h RO	**SP_STR_MON_SP2ISYS_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the input system command FIFO. Returns the value 0 if the SP does not send a command to the input system
19	0h RO	**SP_STR_MON_GPD2SP_accept:** Returns the value 1 if the SP can accept a token from the streaming FIFO between the fifo adapter in GP devices and the SP. Returns 0 if the SP cannot accept a token from this FIFO.
18	0h RO	**SP_STR_MON_GPD2SP_valid:** Returns the value 1 if the streaming FIFO between the fifo adapter in GP devices and the SP has a valid token for the SP. Returns the value 0 if this FIFO is empty.
17	1h RO	**SP_STR_MON_SP2GPD_accept:** Returns the value 1 if the token FIFO between SP and fifo adapter can accept a token from the SP. Returns the value 0 if this token FIFO is full.
16	0h RO	**SP_STR_MON_SP2GPD_valid:** Returns the value 1 if SP sends a token using the streaming port connected to the token FIFO between the SP and the fifo adapter in GP_devices. Returns the value 0 if the SP does not send a token to the fifo adapter.
15	0h RO	**SP_STR_MON_ISP2SP_accept:** Returns the value 1 if the SP can accept a token from the streaming FIFO between the ISP and the SP. Returns 0 if the SP cannot accept a token from this FIFO.
14	0h RO	**SP_STR_MON_ISP2SP_valid:** Returns the value 1 if the streaming FIFO between the ISP and the SP has a valid token for the SP. Returns the value 0 if this FIFO is empty
13	1h RO	**SP_STR_MON_SP2ISP_accept:** Returns the value 1 if the token FIFO between SP and ISP can accept a token from the SP. Returns the value 0 if this token FIFO is full.
12	0h RO	**SP_STR_MON_SP2ISP_valid:** Returns the value 1 if SP sends a token using the streaming port connected to the ISP token FIFO. Returns the value 0 if the SP does not send a token to the ISP



Bit Range	Default & Access	Description
11	0h RO	**SP_STR_MON_DMA2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the DMA acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
10	0h RO	**SP_STR_MON_DMA2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the DMA acknowledge port and the SP, is present on the DMA input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
9	0h RO	**SP_STR_MON_SP2DMA_accept:** Returns the value 1 if the command FIFO between SP and the DMA can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
8	0h RO	**SP_STR_MON_SP2DMA_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the DMA command FIFO. Returns the value 0 if the SP does not send a command to the DMA
7	0h RO	**SP_STR_MON_MC2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the stream2mem acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
6	0h RO	**SP_STR_MON_MC2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the stream2mem acknowledge port and the SP, is present on the stream2mem input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
5	1h RO	**SP_STR_MON_SP2MC_accept:** Returns the value 1 if the command FIFO between SP and the stream2mem can accept a command from the SP. Returns the value 0 if this command FIFO is full.
4	0h RO	**SP_STR_MON_SP2MC_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the stream2mem command FIFO. Returns the value 0 if the SP does not send a command to the stream2mem
3	0h RO	**SP_STR_MON_SIF2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the secondary input formatter acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
2	0h RO	**SP_STR_MON_SIF2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the secondary input formatter acknowledge port and the SP, is present on the secondary input formatter input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
1	1h RO	**SP_STR_MON_SP2SIF_accept:** Returns the value 1 if the command FIFO between SP and the secondary input formatter can accept a command from the SP. Returns the value 0 if this command FIFO is full.
0	0h RO	**SP_STR_MON_SP2SIF_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the Secondary Input Formatter command FIFO. Returns the value 0 if the SP does not send a command to the Secondary Input formatter

3.7.6 reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_type (gpd_gp_reg_reg_gp_sp_stream_stat_b)—Offset 14h

Indicate the status of the streaming ports of the scalar processor. All valid and accept signals of the scalar processor are reflected in this register and in reg_gp_sp_stream_stat.

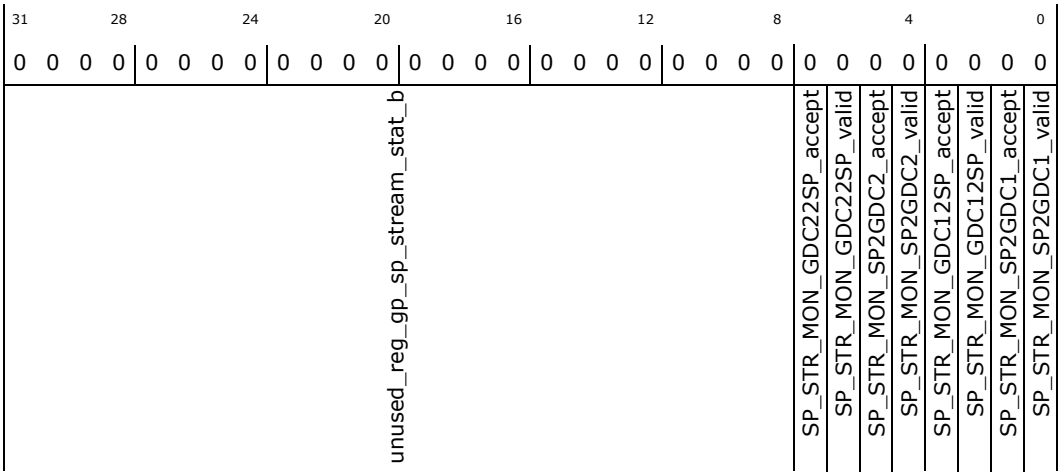
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat_b: [ISPMMADR] + 14h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_reg_gp_sp_stream_stat_b:** Unused
7	0h RO	**SP_STR_MON_GDC22SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the GDC2 acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
6	0h RO	**SP_STR_MON_GDC22SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC2 acknowledge port and the SP, is present on the GDC2 input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
5	0h RO	**SP_STR_MON_SP2GDC2_accept:** Returns the value 1 if the command FIFO between SP and GDC2 can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
4	0h RO	**SP_STR_MON_SP2GDC2_valid:** Returns the value 1 if SP sends a command using the streaming port connected to GDC2 command FIFO. Returns the value 0 if the SP does not send a command to GDC2

Bit Range	Default & Access	Description
3	0h RO	**SP_STR_MON_GDC12SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the GDC1 acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
2	0h RO	**SP_STR_MON_GDC12SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC1 acknowledge port and the SP, is present on the GDC1 input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
1	0h RO	**SP_STR_MON_SP2GDC1_accept:** Returns the value 1 if the command FIFO between SP and GDC1 can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
0	0h RO	**SP_STR_MON_SP2GDC1_valid:** Returns the value 1 if SP sends a command using the streaming port connected to GDC1 command FIFO. Returns the value 0 if the SP does not send a command to GDC1

3.7.7 reg_gpd_gp_reg_reg_gp_isp_stream_stat_type (gpd_gp_reg_reg_gp_isp_stream_stat)—Offset 18h

Indicate the status of the streaming ports of the vector processor. All valid and accept signals of the vector processor are reflected in this register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

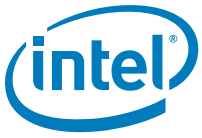
gpd_gp_reg_reg_gp_isp_stream_stat: [ISPMMADR] + 18h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

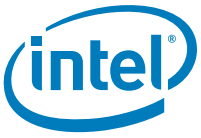
Default: 02200000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_reg_gp_isp_stream_stat				ISP_STR_MON_SP2ISP_accept	ISP_STR_MON_SP2ISP_valid	ISP_STR_MON_ISP2SP_accept	ISP_STR_MON_ISP2SP_valid	ISP_STR_MON_GPD2ISP_accept	ISP_STR_MON_GPD2ISP_valid	ISP_STR_MON_ISP2GPD_accept	ISP_STR_MON_ISP2GPD_valid	ISP_STR_MON_GDC22ISP_accept	ISP_STR_MON_GDC22ISP_valid	ISP_STR_MON_ISP2GDC2_accept	ISP_STR_MON_ISP2GDC2_valid	ISP_STR_MON_GDC12ISP_accept	ISP_STR_MON_GDC12ISP_valid	ISP_STR_MON_ISP2GDC1_accept	ISP_STR_MON_ISP2GDC1_valid	ISP_STR_MON_DMA2ISP_accept	ISP_STR_MON_DMA2ISP_valid	ISP_STR_MON_ISP2DMA_accept	ISP_STR_MON_ISP2DMA_valid	ISP_STR_MON_PIFB2ISP_accept	ISP_STR_MON_PIFB2ISP_valid	ISP_STR_MON_ISP2PIFB_accept	ISP_STR_MON_ISP2PIFB_valid	ISP_STR_MON_PIF2ISP_accept	ISP_STR_MON_PIF2ISP_valid	ISP_STR_MON_ISP2PIF_accept	ISP_STR_MON_ISP2PIF_valid

Bit Range	Default & Access	Description
31:28	0h RW	**unused_reg_gp_isp_stream_stat:** Unused



Bit Range	Default & Access	Description
27	0h RO	**ISP_STR_MON_SP2ISP_accept:** Returns the value 1 if the ISP can accept a token from the streaming FIFO between the SP and the ISP. Returns 0 if the ISP cannot accept a token from this FIFO.
26	0h RO	**ISP_STR_MON_SP2ISP_valid:** Returns the value 1 if the streaming FIFO between the SP and the ISP has a valid token for the ISP. Returns the value 0 if this FIFO is empty
25	1h RO	**ISP_STR_MON_ISP2SP_accept:** Returns the value 1 if the token FIFO between ISP and SP can accept a token from the ISP. Returns the value 0 if this token FIFO is full.
24	0h RO	**ISP_STR_MON_ISP2SP_valid:** Returns the value 1 if ISP sends a token using the streaming port connected to the SP token FIFO. Returns the value 0 if the ISP does not send a token to the SP
23	0h RO	**ISP_STR_MON_GPD2ISP_accept:** Returns the value 1 if the ISP can accept a token from the streaming FIFO between the fifo adapter in GP devices and the ISP. Returns 0 if the ISP cannot accept a token from this FIFO.
22	0h RO	**ISP_STR_MON_GPD2ISP_valid:** Returns the value 1 if the streaming FIFO between the fifo adapter in GP devices and the ISP has a valid token for the ISP. Returns the value 0 if this FIFO is empty.
21	1h RO	**ISP_STR_MON_ISP2GPD_accept:** Returns the value 1 if the token FIFO between ISP and fifo adapter can accept a token from the ISP. Returns the value 0 if this token FIFO is full.
20	0h RO	**ISP_STR_MON_ISP2GPD_valid:** Returns the value 1 if ISP sends a token using the streaming port connected to the token FIFO between the ISP and the fifo adapter in GP_devices. Returns the value 0 if the ISP does not send a token to the fifo adapter.
19	0h RO	**ISP_STR_MON_GDC22ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the GDC2 acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
18	0h RO	**ISP_STR_MON_GDC22ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC2 acknowledge port and the ISP, is present on the GDC2 input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
17	0h RO	**ISP_STR_MON_ISP2GDC2_accept:** Returns the value 1 if the command FIFO between ISP and GDC2 can accept a command from the ISP. Returns the value 0 if this command FIFO is full.
16	0h RO	**ISP_STR_MON_ISP2GDC2_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the GDC2 command FIFO. Returns the value 0 if the ISP does not send a command to GDC2
15	0h RO	**ISP_STR_MON_GDC12ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the GDC1 acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
14	0h RO	**ISP_STR_MON_GDC12ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC1 acknowledge port and the ISP, is present on the GDC1 input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.



Bit Range	Default & Access	Description
13	0h RO	**ISP_STR_MON_ISP2GDC1_accept:** Returns the value 1 if the command FIFO between ISP and GDC1 can accept a command from the ISP. Returns the value 0 if this command FIFO is full.
12	0h RO	**ISP_STR_MON_ISP2GDC1_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the GDC1 command FIFO. Returns the value 0 if the ISP does not send a command to GDC1
11	0h RO	**ISP_STR_MON_DMA2ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the DMA acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
10	0h RO	**ISP_STR_MON_DMA2ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the DMA acknowledge port and the ISP, is present on the DMA input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
9	0h RO	**ISP_STR_MON_ISP2DMA_accept:** Returns the value 1 if the command FIFO between ISP and the DMA can accept a command from the ISP. Returns the value 0 if this command FIFO cannot accept a token from the ISP.
8	0h RO	**ISP_STR_MON_ISP2DMA_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the DMA command FIFO. Returns the value 0 if the ISP does not send a command to the DMA
7	0h RO	**ISP_STR_MON_PIFB2ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the primary input formatter B acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
6	0h RO	**ISP_STR_MON_PIFB2ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter B acknowledge port and the ISP, is present on the primary input formatter B input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
5	0h RO	**ISP_STR_MON_ISP2PIFB_accept:** Returns the value 1 if the command FIFO between ISP and the Primary input formatter B can accept a command from the ISP. Returns the value 0 if this FIFO cannot accept a command from the ISP.
4	0h RO	**ISP_STR_MON_ISP2PIFB_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the Primary Input Formatter B command FIFO. Returns the value 0 if the ISP does not send a command to the Primary Input formatter B
3	0h RO	**ISP_STR_MON_PIF2ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the primary input formatter acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
2	0h RO	**ISP_STR_MON_PIF2ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter acknowledge port and the ISP, is present on the primary input formatter input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
1	0h RO	**ISP_STR_MON_ISP2PIF_accept:** Returns the value 1 if the command FIFO between ISP and the Primary input formatter can accept a command from the ISP. Returns the value 0 if this command FIFO is full.

Bit Range	Default & Access	Description
0	0h RO	**ISP_STR_MON_ISP2PIF_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the Primary Input Formatter command FIFO. Returns the value 0 if the ISP does not send a command to the Primary Input formatter

3.7.8 reg_gpd_gp_reg_reg_gp_mod_stream_stat_type (gpd_gp_reg_reg_gp_mod_stream_stat)—Offset 1Ch

Indicate the status of the streaming ports of the modules. All module's valid and accept ports used for control are reflected in this register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

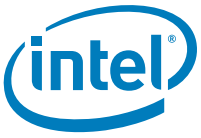
gpd_gp_reg_reg_gp_mod_stream_stat: [ISPMMADR] + 1Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

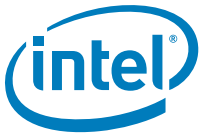
Default: AA88A222h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
MOD_STR_MON_CELLS2GDC2_accept	MOD_STR_MON_CELLS2GDC2_valid	MOD_STR_MON_GDC22CELLS_accept	MOD_STR_MON_GDC22CELLS_valid	MOD_STR_MON_CELLS2GDC1_accept	MOD_STR_MON_CELLS2GDC1_valid	MOD_STR_MON_GDC12CELLS_accept	MOD_STR_MON_GDC12CELLS_valid	MOD_STR_MON_SP2DMA_accept	MOD_STR_MON_SP2DMA_valid	MOD_STR_MON_DMA2SP_accept	MOD_STR_MON_DMA2SP_valid	MOD_STR_MON_ISP2DMA_accept	MOD_STR_MON_ISP2DMA_valid	MOD_STR_MON_DMA2ISP_accept	MOD_STR_MON_DMA2ISP_valid	MOD_STR_MON_SP2MC_accept	MOD_STR_MON_SP2MC_valid	MOD_STR_MON_MC2SP_accept	MOD_STR_MON_MC2SP_valid	MOD_STR_MON_SP2SIF_accept	MOD_STR_MON_SP2SIF_valid	MOD_STR_MON_SIF2SP_accept	MOD_STR_MON_SIF2SP_valid	MOD_STR_MON_CELLS2PIFB_accept	MOD_STR_MON_CELLS2PIFB_valid	MOD_STR_MON_PIFB2CELLS_accept	MOD_STR_MON_PIFB2CELLS_valid	MOD_STR_MON_CELLS2PIFA_accept	MOD_STR_MON_CELLS2PIFA_valid	MOD_STR_MON_PIFA2CELLS_accept	MOD_STR_MON_PIFA2CELLS_valid

Bit Range	Default & Access	Description
31	1h RO	**MOD_STR_MON_CELLS2GDC2_accept:** Returns the value 1 if the acknowledge FIFO between GDC2 and ISP/SP can accept an acknowledge token from GDC2. Returns the value 0 if this FIFO is full.
30	0h RO	**MOD_STR_MON_CELLS2GDC2_valid:** Returns the value 1 if GDC2 sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if GDC2 does not send an acknowledge token to this FIFO.
29	1h RO	**MOD_STR_MON_GDC22CELLS_accept:** Returns the value 1 if GDC2 can accept a command token from the command FIFO between the ISP/SP and GDC2. Returns the value 0 if GDC2 cannot accept a command token.



Bit Range	Default & Access	Description
28	0h RO	**MOD_STR_MON_GDC22CELLS_valid:** Returns the value 1 if there is a command available on the command fifo between SP/ISP and GDC2. Returns the value 0 if the command FIFO for GDC2 is empty.
27	1h RO	**MOD_STR_MON_CELLS2GDC1_accept:** Returns the value 1 if the acknowledge FIFO between GDC1 and ISP/SP can accept an acknowledge token from GDC1. Returns the value 0 if this FIFO is full.
26	0h RO	**MOD_STR_MON_CELLS2GDC1_valid:** Returns the value 1 if GDC1 sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if GDC1 does not send an acknowledge token to this FIFO.
25	1h RO	**MOD_STR_MON_GDC12CELLS_accept:** Returns the value 1 if GDC1 can accept a command token from the command FIFO between the ISP/SP and GDC1. Returns the value 0 if GDC1 cannot accept a command token.
24	0h RO	**MOD_STR_MON_GDC12CELLS_valid:** Returns the value 1 if there is a command available on the command fifo between SP/ISP and GDC1. Returns the value 0 if the command FIFO for GDC1 is empty.
23	1h RO	**MOD_STR_MON_SP2DMA_accept:** Returns the value 1 if the acknowledge FIFO between the DMA and SP can accept an acknowledge token from the DMA. Returns the value 0 if this FIFO is full.
22	0h RO	**MOD_STR_MON_SP2DMA_valid:** Returns the value 1 if DMA sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the SP. Returns the value 0 if the DMA does not send an acknowledge token to this FIFO.
21	0h RO	**MOD_STR_MON_DMA2SP_accept:** Returns the value 1 if the DMA can accept a command token from the command FIFO between the SP and the DMA. Returns the value 0 if the DMA cannot accept a command token.
20	0h RO	**MOD_STR_MON_DMA2SP_valid:** Returns the value 1 if there is a command available on the command fifo between SP and the DMA. Returns the value 0 if the command FIFO for the DMA is empty.
19	1h RO	**MOD_STR_MON_ISP2DMA_accept:** Returns the value 1 if the acknowledge FIFO between the DMA and ISP can accept an acknowledge token from the DMA. Returns the value 0 if this FIFO is full.
18	0h RO	**MOD_STR_MON_ISP2DMA_valid:** Returns the value 1 if DMA sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP. Returns the value 0 if the DMA does not send an acknowledge token to this FIFO.
17	0h RO	**MOD_STR_MON_DMA2ISP_accept:** Returns the value 1 if the DMA can accept a command token from the command FIFO between the SP and the DMA. Returns the value 0 if the DMA cannot accept a command token.
16	0h RO	**MOD_STR_MON_DMA2ISP_valid:** Returns the value 1 if there is a command available on the command fifo between ISP and the DMA. Returns the value 0 if the command FIFO for the DMA is empty.
15	1h RO	**MOD_STR_MON_SP2MC_accept:** Returns the value 1 if stream2mem can accept a command token from the command FIFO between the SP and the stream2mem. Returns the value 0 if stream2mem cannot accept a command token.



Bit Range	Default & Access	Description
14	0h RO	**MOD_STR_MON_SP2MC_valid:** Returns the value 1 if there is a command available on the command fifo between the SP and the stream2mem. Returns the value 0 if the command FIFO for the stream2mem is empty.
13	1h RO	**MOD_STR_MON_MC2SP_accept:** Returns the value 1 if the acknowledge FIFO between the stream2mem and the SP can accept an acknowledge token from the stream2mem. Returns the value 0 if this FIFO is full.
12	0h RO	**MOD_STR_MON_MC2SP_valid:** Returns the value 1 if the stream2mem sends an acknowledge token using its acknowledge output port connected to the acknowledge FIFO between the stream2mem and the SP. Returns the value 0 if the stream2mem does not send an acknowledge token to this FIFO.
11	0h RO	**MOD_STR_MON_SP2SIF_accept:** Returns the value 1 if secondary input formatter can accept a command token from the command FIFO between the SP and the secondary input formatter. Returns the value 0 if this FIFO is full.
10	0h RO	**MOD_STR_MON_SP2SIF_valid:** Returns the value 1 if there is a command available on the command fifo between the SP and the secondary input formatter. Returns the value 0 if the command FIFO for the secondary input formatter is empty.
9	1h RO	**MOD_STR_MON_SIF2SP_accept:** Returns the value 1 if the acknowledge FIFO between the secondary input formatter and the SP can accept an acknowledge token from the secondary input formatter. Returns the value 0 if this FIFO is full.
8	0h RO	**MOD_STR_MON_SIF2SP_valid:** Returns the value 1 if the secondary input formatter sends an acknowledge token using its acknowledge output port connected to the acknowledge FIFO between the secondary input formatter and the SP. Returns the value 0 if the secondary input formatter does not send an acknowledge token to this FIFO.
7	0h RO	**MOD_STR_MON_CELLS2PIFB_accept:** Returns the value 1 if primary input formatter B can accept a command token from the command FIFO between the ISP/SP and the primary input formatter B. Returns the value 0 if the primary input formatter B cannot accept a command token.
6	0h RO	**MOD_STR_MON_CELLS2PIFB_valid:** Returns the value 1 if there is a command available on the command fifo between SP/ISP and the primary input formatter B. Returns the value 0 if the command FIFO for the primary input formatter B is empty.
5	1h RO	**MOD_STR_MON_PIFB2CELLS_accept:** Returns the value 1 if the acknowledge FIFO between the primary input formatter B and the ISP/SP can accept an acknowledge token from the primary input formatter B. Returns the value 0 if this command FIFO is full.
4	0h RO	**MOD_STR_MON_PIFB2CELLS_valid:** Returns the value 1 if primary input formatter B sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if the primary input formatter B does not send an acknowledge token to this FIFO.
3	0h RO	**MOD_STR_MON_CELLS2PIFA_accept:** Returns the value 1 if primary input formatter A can accept a command token from the command FIFO between the ISP/SP and the primary input formatter A. Returns the value 0 if the primary input formatter A cannot accept a command token.

Bit Range	Default & Access	Description
2	0h RO	**MOD_STR_MON_CELLS2PIFA_valid:** Returns the value 1 if there is a command available on the command fifo between SP/ISP and the primary input formatter A. Returns the value 0 if the command FIFO for the primary input formatter A is empty.
1	1h RO	**MOD_STR_MON_PIFA2CELLS_accept:** Returns the value 1 if the acknowledge FIFO between the primary input formatter A and the ISP/SP can accept an acknowledge token from the primary input formatter A. Returns the value 0 if this command FIFO is full.
0	0h RO	**MOD_STR_MON_PIFA2CELLS_valid:** Returns the value 1 if primary input formatter A sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if the primary input formatter A does not send an acknowledge token to this FIFO.

3.7.9 reg_gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond)—Offset 20h

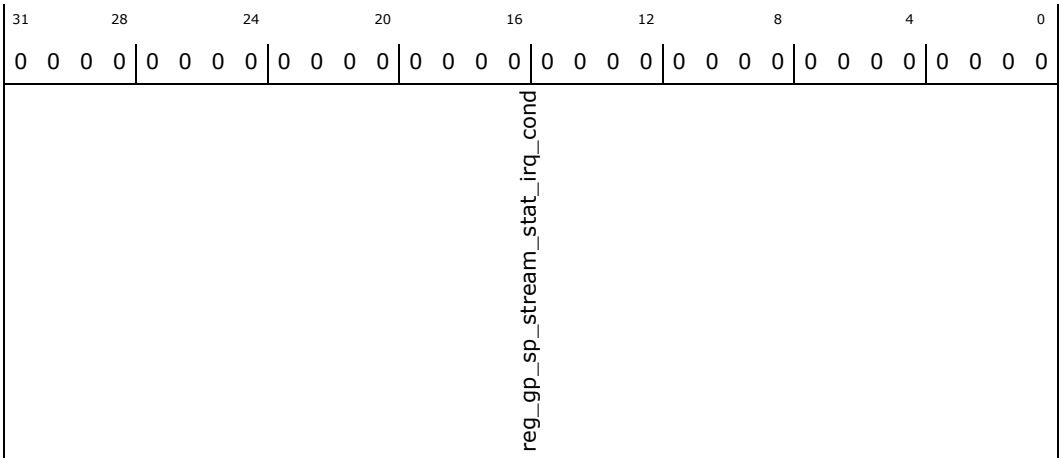
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond: [ISPMMADR] + 20h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_gp_sp_stream_stat_irq_cond:** This register indicates which condition of the SP streaming ports will enable the SP streaming stat irq output

3.7.10 reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond_type (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond)—Offset 24h

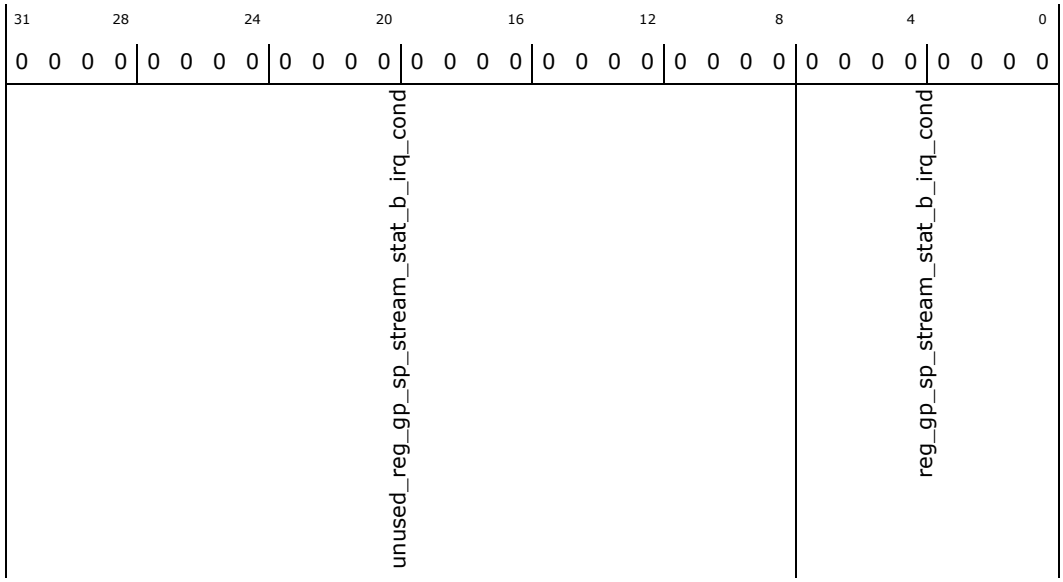
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond: [ISPMMADR] + 24h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_reg_gp_sp_stream_stat_b_irq_cond:** Unused
7:0	0h RW	**reg_gp_sp_stream_stat_b_irq_cond:** This register indicates which condition of the SP streaming ports b will enable the SP streaming stat b irq output

3.7.11 reg_gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond)—Offset 28h

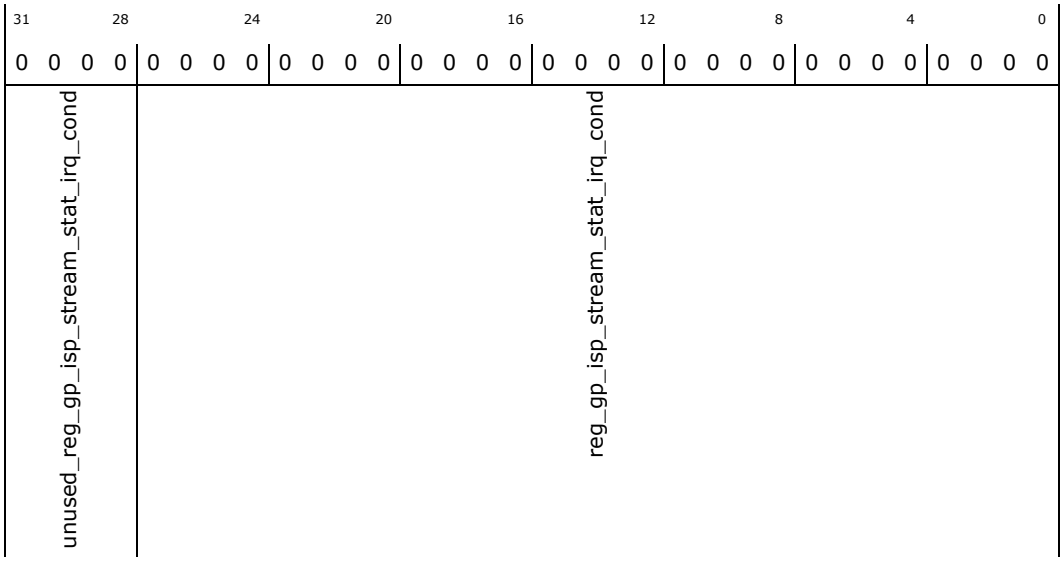
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond: [ISPMMADR] + 28h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**unused_reg_gp_isp_stream_stat_irq_cond:** Unused
27:0	0h RW	**reg_gp_isp_stream_stat_irq_cond:** This register indicates which condition of the ISP streaming ports will enable the ISP streaming stat irq output

3.7.12 reg_gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond)—Offset 2Ch

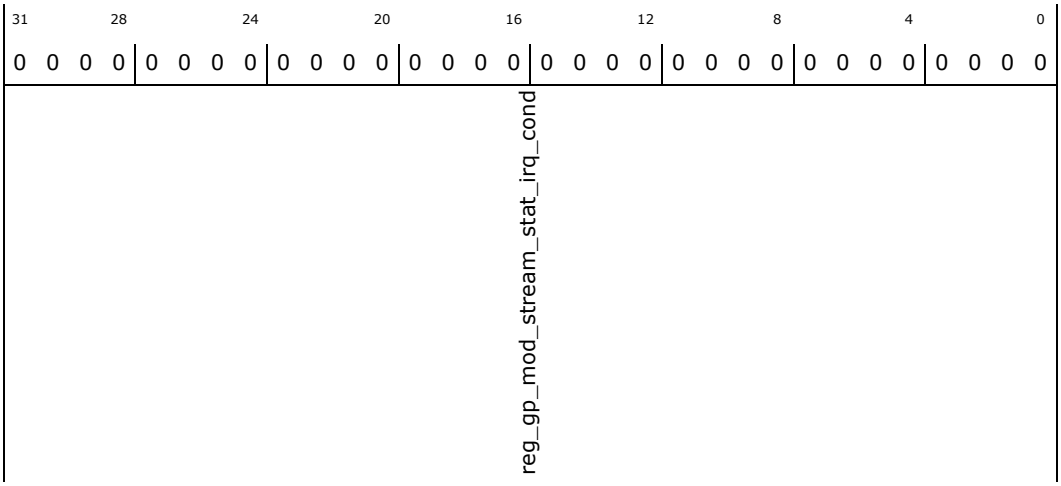
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond: [ISPMMADR] + 2Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_gp_mod_stream_stat_irq_cond:** This register indicates which condition of the MOD streaming ports will enable the MOD streaming stat irq output

3.7.13 reg_gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable)—Offset 30h

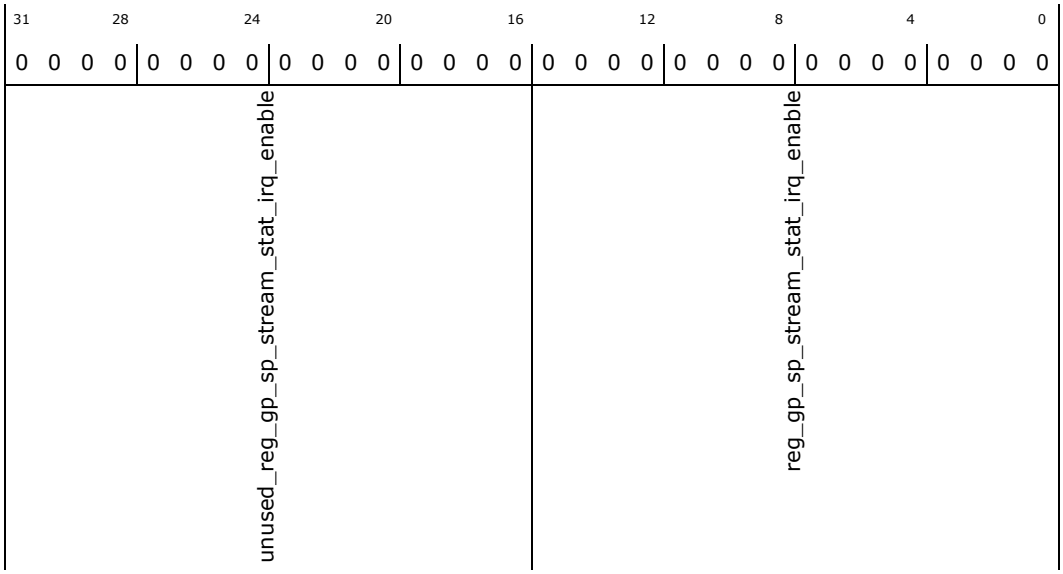
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable: [ISPMMADR] + 30h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_reg_gp_sp_stream_stat_irq_enable:** Unused
15:0	0h RW	**reg_gp_sp_stream_stat_irq_enable:** This register enables the SP streaming stat irq output for each of the 16 ports

3.7.14 reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable_type (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable)—Offset 34h

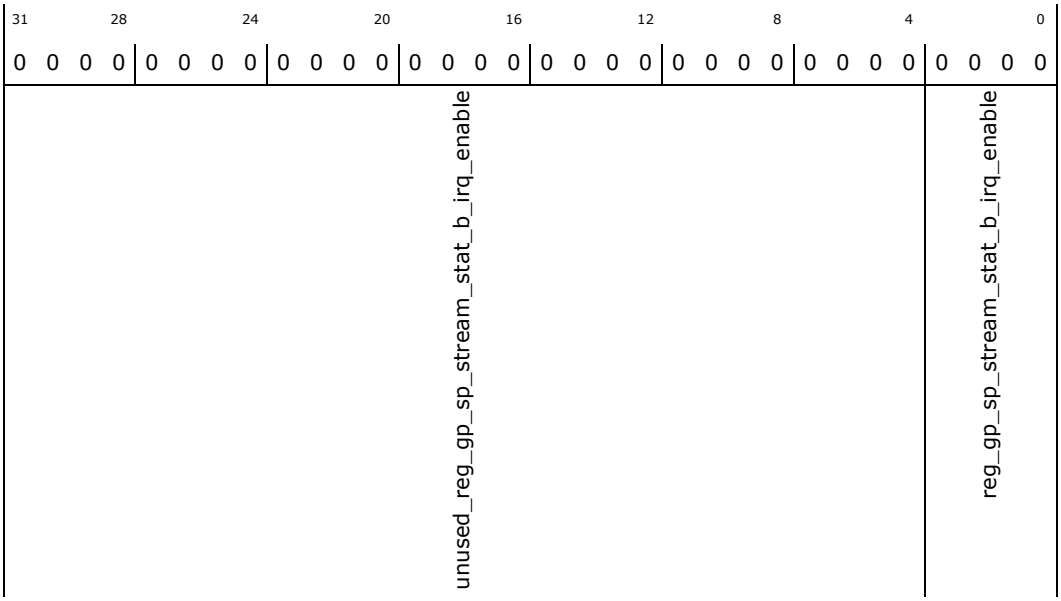
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable: [ISPMMADR] + 34h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_gp_sp_stream_stat_b_irq_enable:** Unused
3:0	0h RW	**reg_gp_sp_stream_stat_b_irq_enable:** This register enables the SP streaming stat b irq output for each of the 4 ports

3.7.15 reg_gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable)—Offset 38h

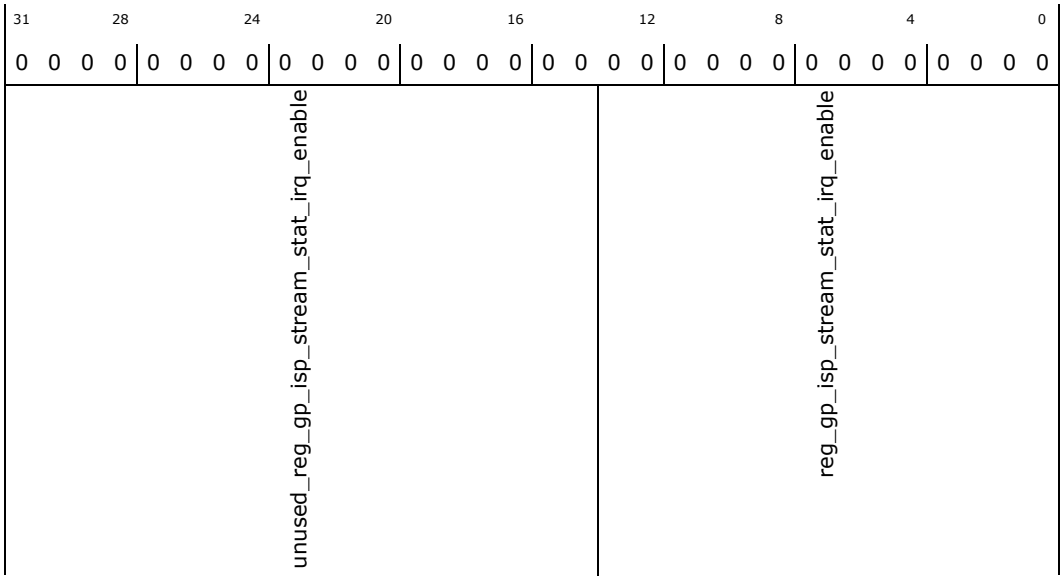
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable: [ISPMMADR] + 38h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_isp_stream_stat_irq_enable:** Unused
13:0	0h RW	**reg_gp_isp_stream_stat_irq_enable:** This register enables the ISP streaming stat irq output for each of the 14 ports

3.7.16 reg_gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable)—Offset 3Ch

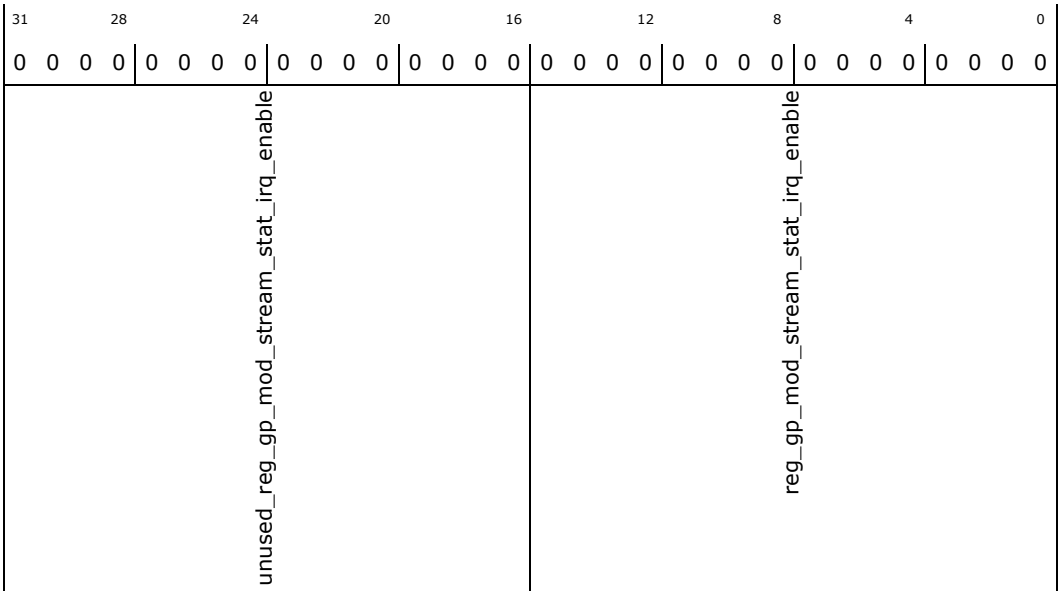
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable: [ISPMMADR] + 3Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_reg_gp_mod_stream_stat_irq_enable:** Unused
15:0	0h RW	**reg_gp_mod_stream_stat_irq_enable:** This register enables the MOD streaming stat irq output for each of the 16 ports

3.7.17 reg_gpd_gp_reg_reg_gp_switch_if_type (gpd_gp_reg_reg_gp_switch_if)—Offset 40h

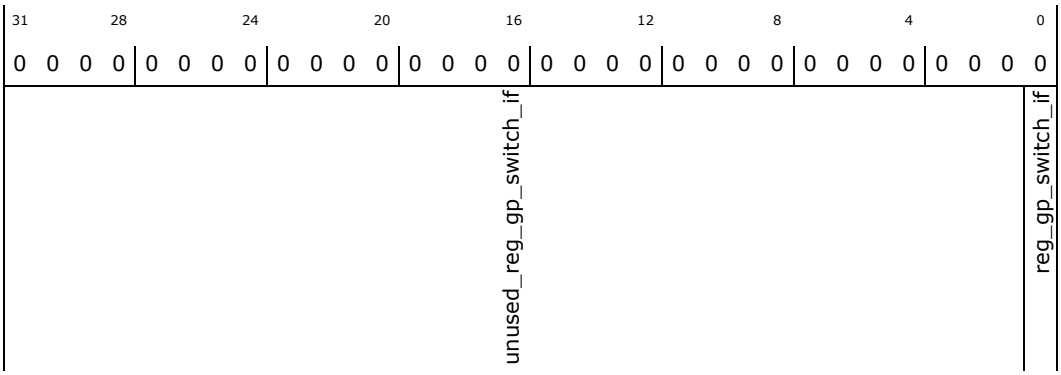
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_switch_if: [ISPMMADR] + 40h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_switch_if:** Unused
0	0h RW	**reg_gp_switch_if:** Selects the control stream switch for the primary input formatter and for primary input formatter b. The input formatters can be controlled by the scalar processor (value=1) or by the ISP (value=0)

3.7.18 reg_gpd_gp_reg_reg_gp_switch_gdc1_type (gpd_gp_reg_reg_gp_switch_gdc1)—Offset 44h

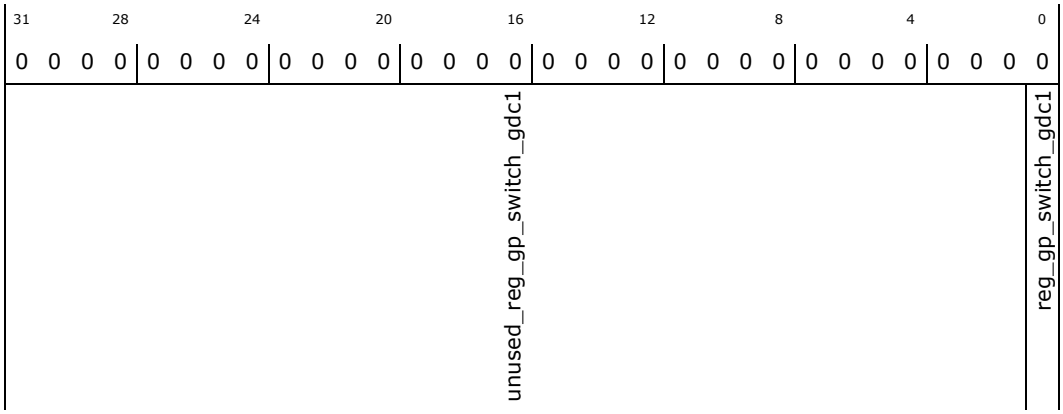
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_switch_gdc1: [ISPMMADR] + 44h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_switch_gdc1:** Unused
0	0h RW	**reg_gp_switch_gdc1:** Selects the control stream switch for the GDC1. GDC1 can be controlled by the scalar processor (value=1) or the ISP (value=0)

3.7.19 reg_gpd_gp_reg_reg_gp_switch_gdc2_type (gpd_gp_reg_reg_gp_switch_gdc2)—Offset 48h

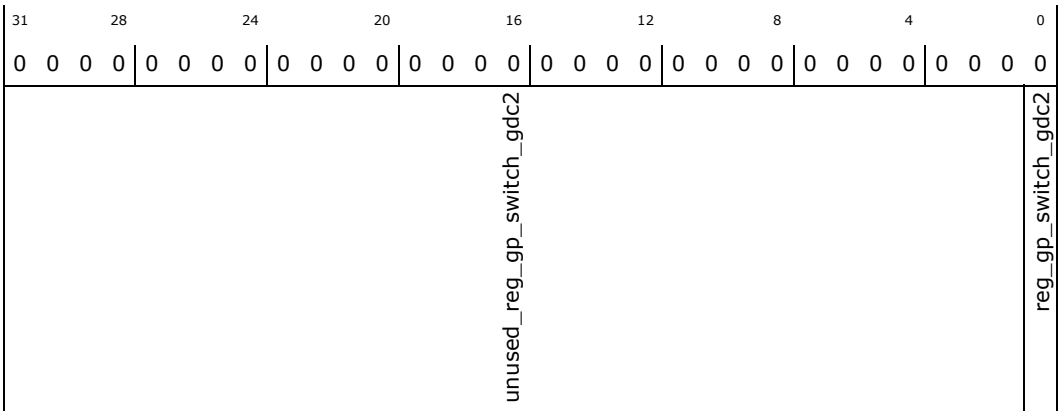
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_switch_gdc2: [ISPMMADR] + 48h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_switch_gdc2:** Unused
0	0h RW	**reg_gp_switch_gdc2:** Selects the control stream switch for the GDC2. GDC2 can be controlled by the scalar processor (value=1) or the ISP (value=0)

3.7.20 reg_gpd_gp_reg_reg_gp_srst_type (gpd_gp_reg_reg_gp_srst)—Offset 4Ch

Soft reset for several modules in the system. If '1' is written to a bit, the module(s) connected to that bit are held in reset until a '0' is written to that bit.

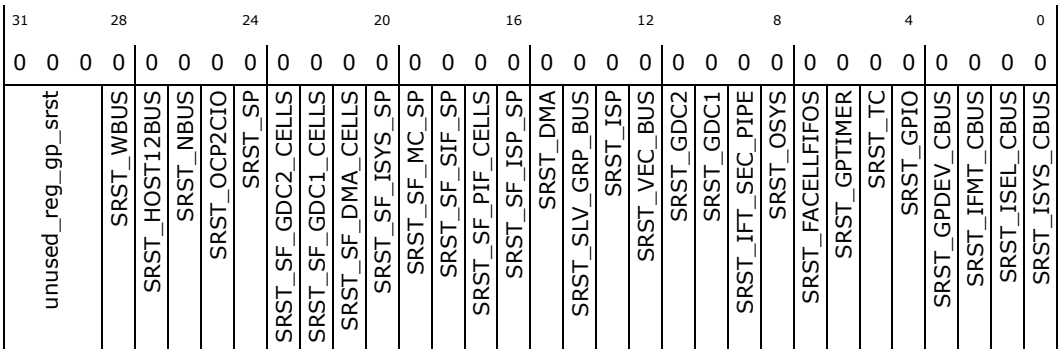
Access Method

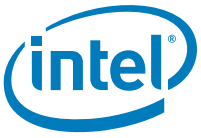
Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_srst: [ISPMMADR] + 4Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31:29	0h RW	**unused_reg_gp_srst:** Unused
28	0h RW	**SRST_WBUS:** soft reset bit for the wide bus
27	0h RW	**SRST_HOST12BUS:** soft reset bit for the bus from host to fifo adapters
26	0h RW	**SRST_NBUS:** soft reset bit for the narrow bus
25	0h RW	**SRST_OCP2CIO:** soft reset bit for the OCP2CIO converter
24	0h RW	**SRST_SP:** soft reset bit for the SP
23	0h RW	**SRST_SF_GDC2_CELLS:** soft reset bit for the FIFOs between the GDC2 and the cells
22	0h RW	**SRST_SF_GDC1_CELLS:** soft reset bit for the FIFOs between the GDC1 and the cells
21	0h RW	**SRST_SF_DMA_CELLS:** soft reset bit for the FIFOs between the DMA and the cells
20	0h RW	**SRST_SF_ISYS_SP:** soft reset bit for the FIFOs between the input system and the SP
19	0h RW	**SRST_SF_MC_SP:** soft reset bit for the FIFOs between the stream2memory and the SP
18	0h RW	**SRST_SF_SIF_SP:** soft reset bit for the FIFOs between the secondary input formatter and the SP
17	0h RW	**SRST_SF_PIF_CELLS:** soft reset bit for the FIFOs between the primary input formatters and the cells
16	0h RW	**SRST_SF_ISP_SP:** soft reset bit for the FIFOs between SP and ISP
15	0h RW	**SRST_DMA:** soft reset bit for the DMA
14	0h RW	**SRST_SLV_GRP_BUS:** soft reset bit for the slave group bus
13	0h RW	**SRST_ISP:** soft reset bit for the isp (vector processor)
12	0h RW	**SRST_VEC_BUS:** soft reset bit for the vector bus
11	0h RW	**SRST_GDC2:** soft reset bit for the GDC2 block
10	0h RW	**SRST_GDC1:** soft reset bit for the GDC1 block
9	0h RW	**SRST_IFT_SEC_PIPE:** soft reset bit for the CIO pipeline after the secondary input formatter
8	0h RW	**SRST_OSYS:** soft reset bit for the blocks in the output system cluster

Bit Range	Default & Access	Description
7	0h RW	**SRST_FACELLFIFOS:** soft reset bit for the fifo's connected to the fifo adapter between host and cells
6	0h RW	**SRST_GPTIMER:** soft reset bit for the GP timer block
5	0h RW	**SRST_TC:** soft reset bit for the timed controller block
4	0h RW	**SRST_GPIO:** soft reset bit for the gpio block
3	0h RW	**SRST_GPDEV_CBUS:** soft reset bit for the gp devices cluster control bus
2	0h RW	**SRST_IFMT_CBUS:** soft reset bit for the input formatting cluster control bus
1	0h RW	**SRST_ISEL_CBUS:** soft reset bit for the input selector cluster control bus
0	0h RW	**SRST_ISYS_CBUS:** soft reset bit for the input system control bus

3.7.21 reg_gpd_gp_reg_reg_gp_slv_reg_srst_type (gpd_gp_reg_reg_gp_slv_reg_srst)—Offset 50h

Soft reset for the slave accessible registers in some blocks. If '1' is written to a bit, the attached registers get their default value. They can only be overwritten after writing a '0' to this bit

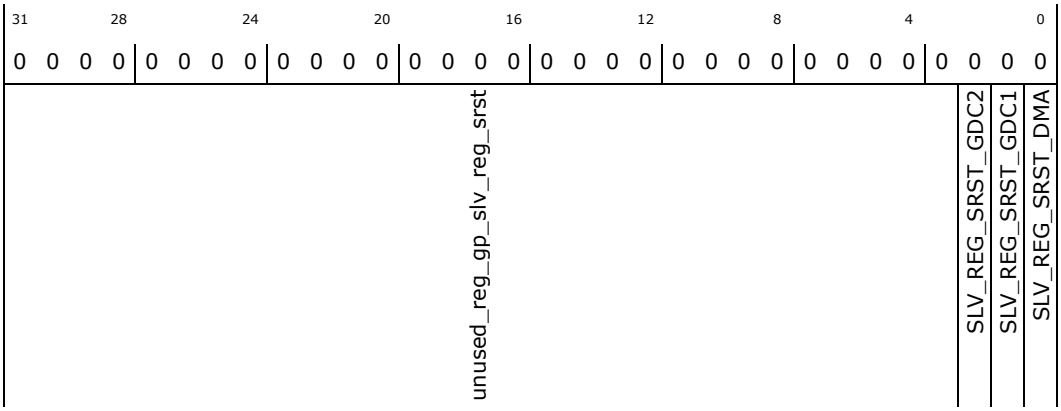
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_slv_reg_srst: [ISPMMADR] + 50h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_reg_gp_slv_reg_srst:** Unused
2	0h RW	**SLV_REG_SRST_GDC2:** soft reset bit for the slave registers in the GDC2
1	0h RW	**SLV_REG_SRST_GDC1:** soft reset bit for the slave registers in the GDC1
0	0h RW	**SLV_REG_SRST_DMA:** soft reset bit for the slave registers in the DMA

3.7.22 reg_gpd_tc_FifoWriteCmd_type (gpd_tc_FifoWriteCmd)—Offset 100h

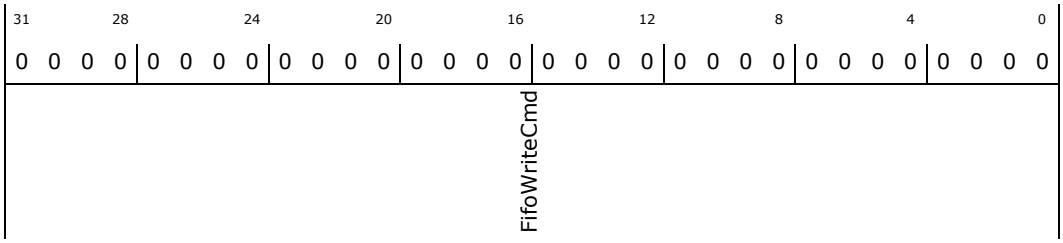
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_tc_FifoWriteCmd: [ISPMMADR] + 100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h WO	**FifoWriteCmd:** Timed controller Command input. A Timed Controller command consists of 5 32-bit tokens that need to be written sequentially to this register location

3.7.23 reg_gpd_c_gpio_reg_gpio_doe_type (gpd_c_gpio_reg_gpio_doe)—Offset 400h

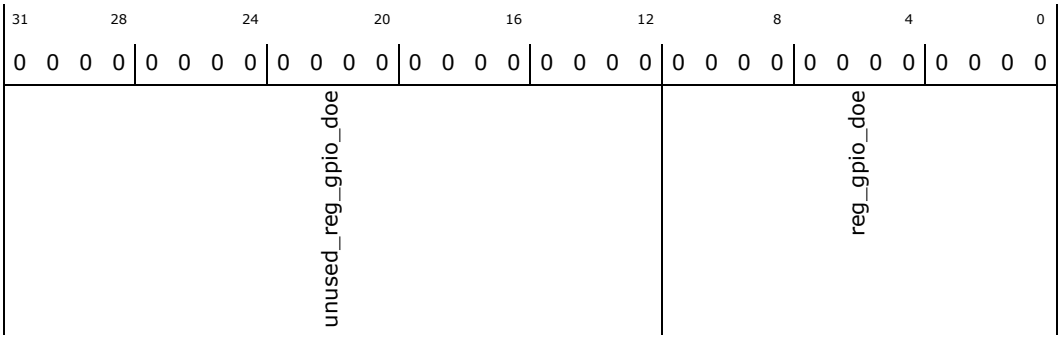
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_doe: [ISPMMADR] + 400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_doe:** Unused
11:0	0h RW	**reg_gpio_doe:** indicates for each bit whether it is intended to be an input (value='0') or an output (value='1')

3.7.24 reg_gpd_c_gpio_reg_gpio_do_select_type (gpd_c_gpio_reg_gpio_do_select)—Offset 404h

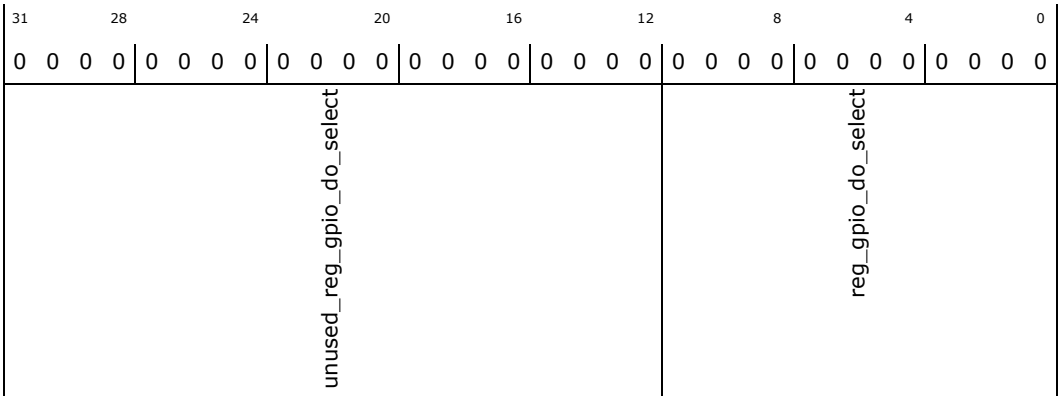
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_select: [ISPMMADR] + 404h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_do_select:** Unused
11:0	0h RW	**reg_gpio_do_select:** indicates for each bit of gpio_do whether it should have the value from source 0 (value='0') or source 1 (value='1').

3.7.25 reg_gpd_c_gpio_reg_gpio_do_0_type (gpd_c_gpio_reg_gpio_do_0)—Offset 408h

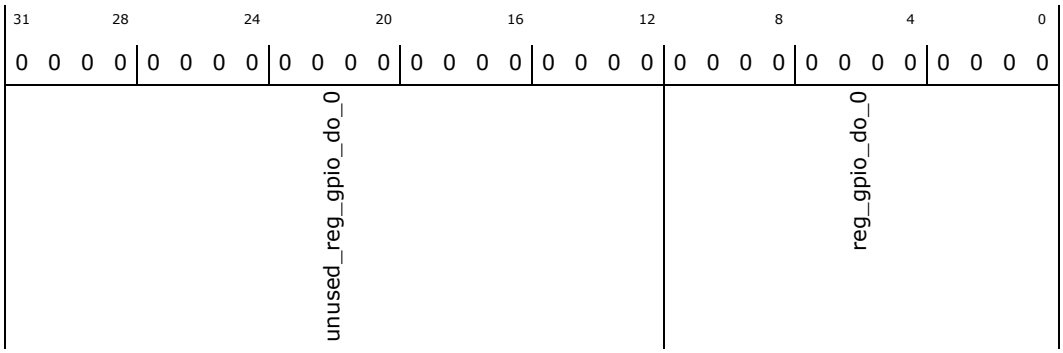
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_0: [ISPMMADR] + 408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_do_0:** Unused
11:0	0h RW	**reg_gpio_do_0:** provides the value for each of the output bits (source 0)

3.7.26 reg_gpd_c_gpio_reg_gpio_do_1_type (gpd_c_gpio_reg_gpio_do_1)—Offset 40Ch

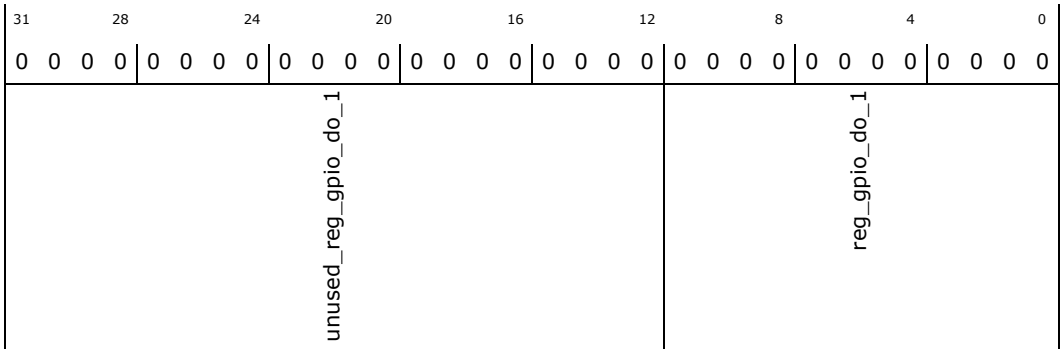
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_1: [ISPMMADR] + 40Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_do_1:** Unused
11:0	0h RW	**reg_gpio_do_1:** provides the value for each of the output bits (source 1)

3.7.27 reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_0_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_0)—Offset 410h

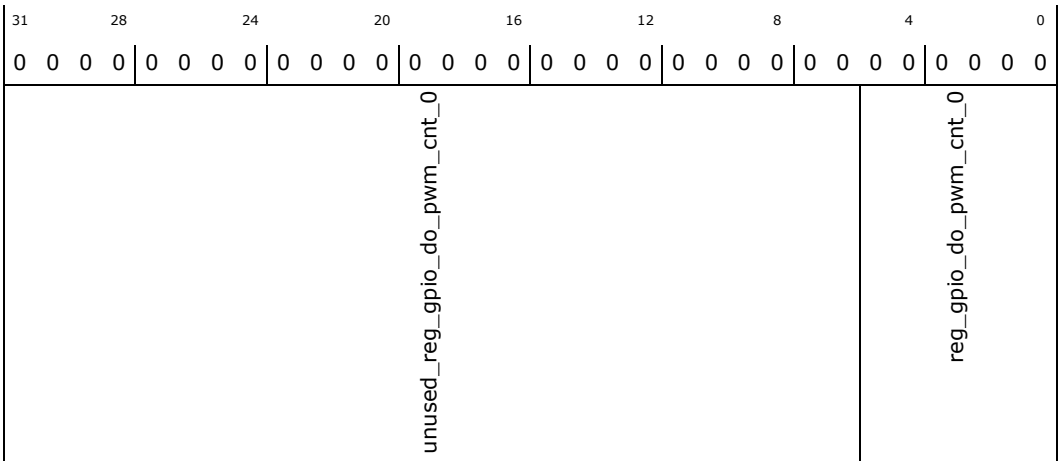
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_cnt_0: [ISPMMADR] + 410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_reg_gpio_do_pwm_cnt_0:** Unused
5:0	0h RW	**reg_gpio_do_pwm_cnt_0:** indicates duty cycle for PWM output 0. value d means duty cycle d/64

3.7.28 reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_1_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_1)—Offset 414h

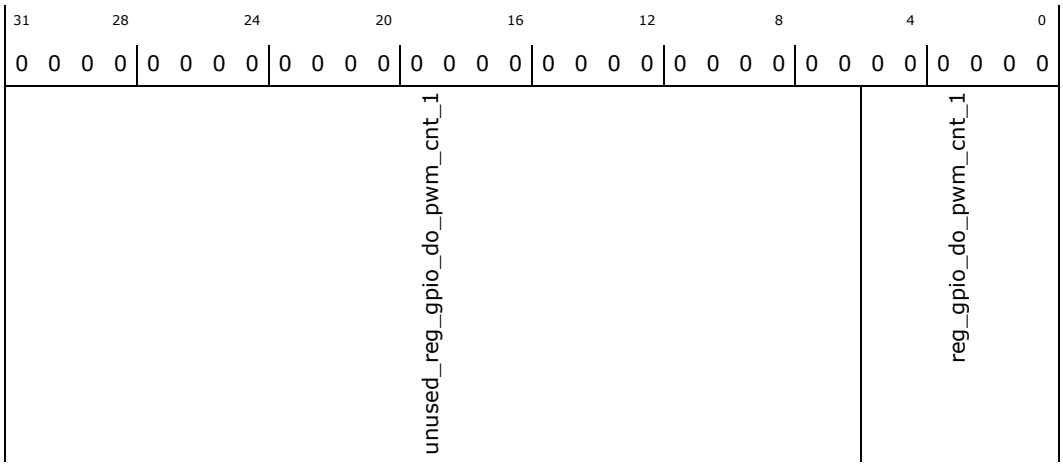
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_cnt_1: [ISPMMADR] + 414h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_reg_gpio_do_pwm_cnt_1:** Unused
5:0	0h RW	**reg_gpio_do_pwm_cnt_1:** indicates duty cycle for PWM output 1. value d means duty cycle d/64

3.7.29 reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_2_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_2)—Offset 418h

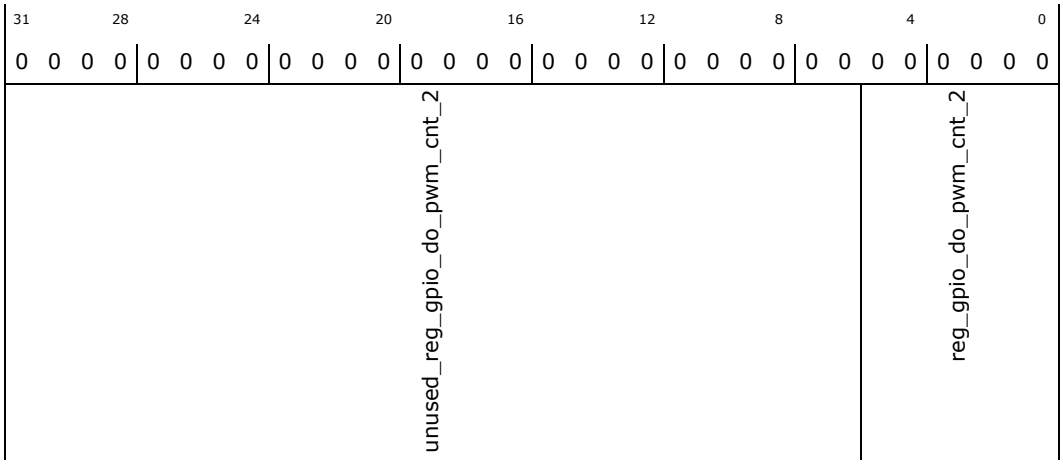
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_cnt_2: [ISPMMADR] + 418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_reg_gpio_do_pwm_cnt_2:** Unused
5:0	0h RW	**reg_gpio_do_pwm_cnt_2:** indicates duty cycle for PWM output 2. value d means duty cycle d/64

3.7.30 reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_3_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_3)—Offset 41Ch

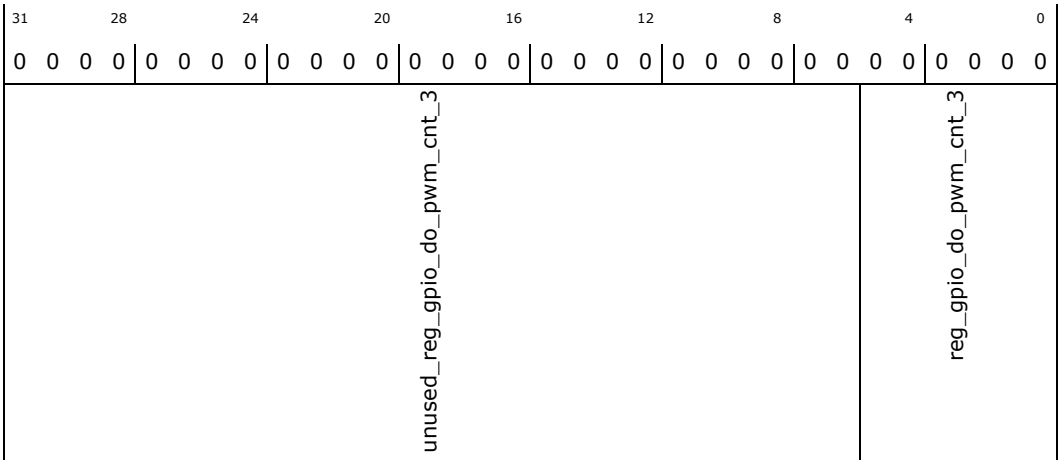
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_cnt_3: [ISPMMADR] + 41Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_reg_gpio_do_pwm_cnt_3:** Unused
5:0	0h RW	**reg_gpio_do_pwm_cnt_3:** indicates duty cycle for PWM output 3. value d means duty cycle d/64

3.7.31 reg_gpd_c_gpio_reg_gpio_do_pwm_main_cnt_type (gpd_c_gpio_reg_gpio_do_pwm_main_cnt)—Offset 420h

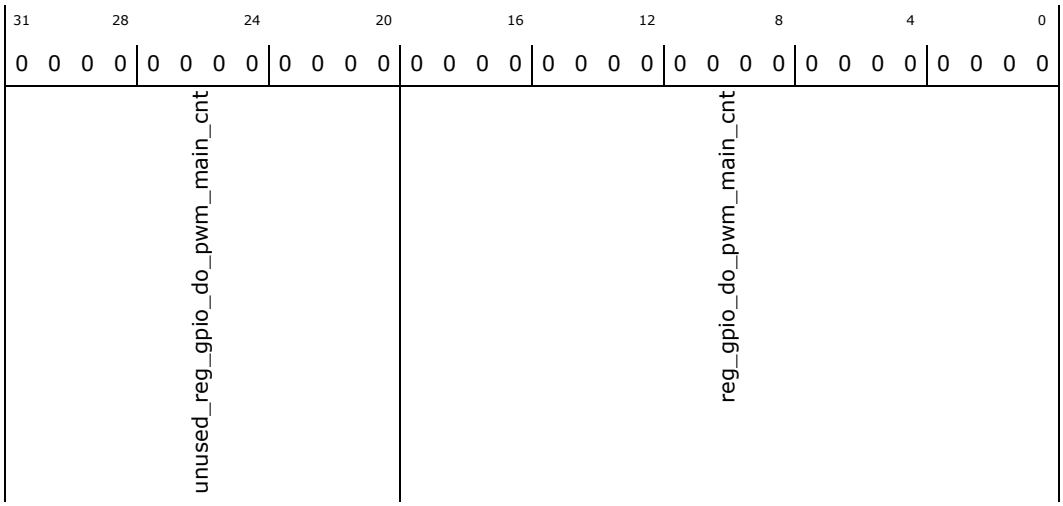
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_main_cnt: [ISPMMADR] + 420h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**unused_reg_gpio_do_pwm_main_cnt:** Unused
19:0	0h RW	**reg_gpio_do_pwm_main_cnt:** indicates wrapping value for PWM main counter

3.7.32 reg_gpd_c_gpio_reg_gpio_do_pwm_enable_type (gpd_c_gpio_reg_gpio_do_pwm_enable)—Offset 424h

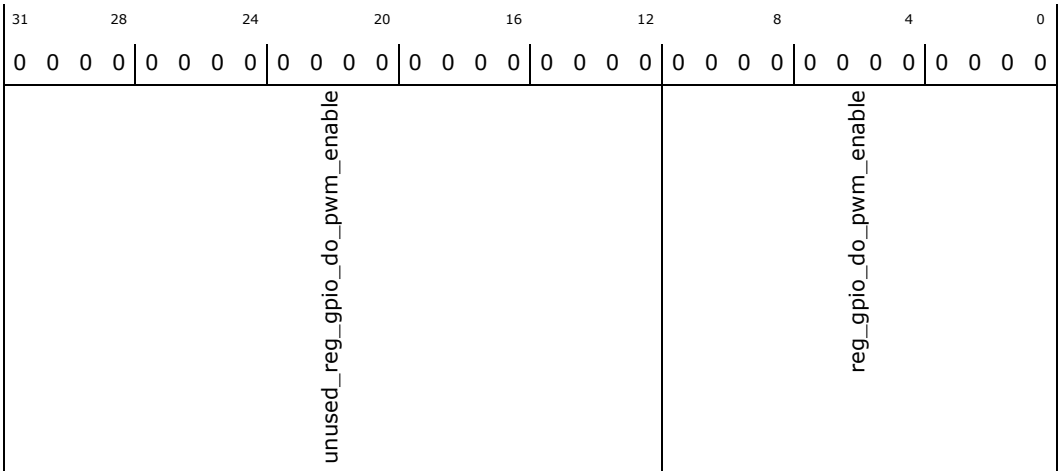
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_enable: [ISPMMADR] + 424h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_do_pwm_enable:** Unused
11:0	0h RW	**reg_gpio_do_pwm_enable:** indicates per bit whether PWM is on (value='1') or output is fixed '0' (value='0')

3.7.33 reg_gpd_c_gpio_reg_gpio_di_debouncemethod_type (gpd_c_gpio_reg_gpio_di_debouncemethod)—Offset 428h

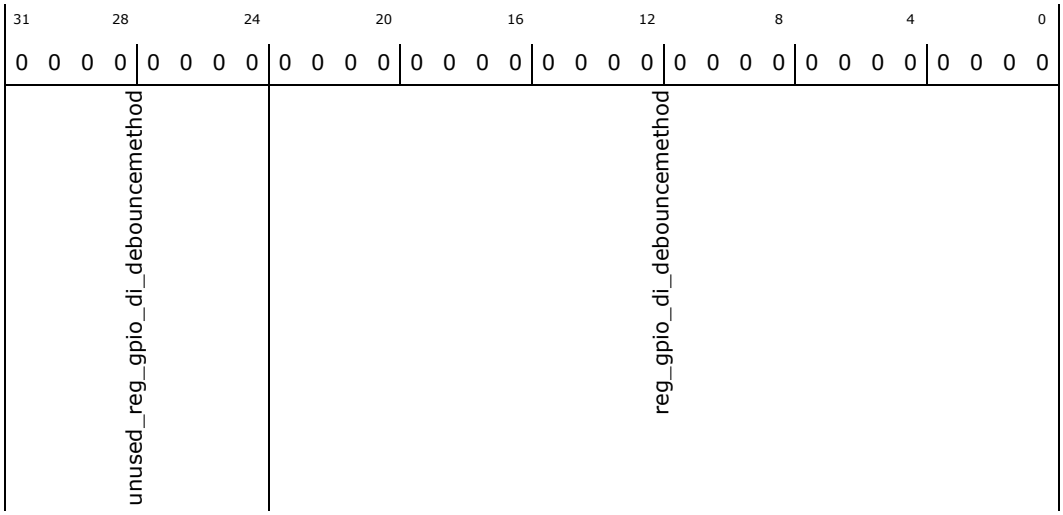
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_debouncemethod: [ISPMMADR] + 428h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_reg_gpio_di_debouncemethod:** Unused
23:0	0h RW	**reg_gpio_di_debouncemethod:** indicates for each input bit which debouncing counter value is chosen: '00': debounce_cnt0, '01': debounce_cnt1, '10': debounce_cnt2, '11': debounce_cnt3'

3.7.34 reg_gpd_c_gpio_reg_gpio_di_debounce_cnt0_type (gpd_c_gpio_reg_gpio_di_debounce_cnt0)—Offset 42Ch

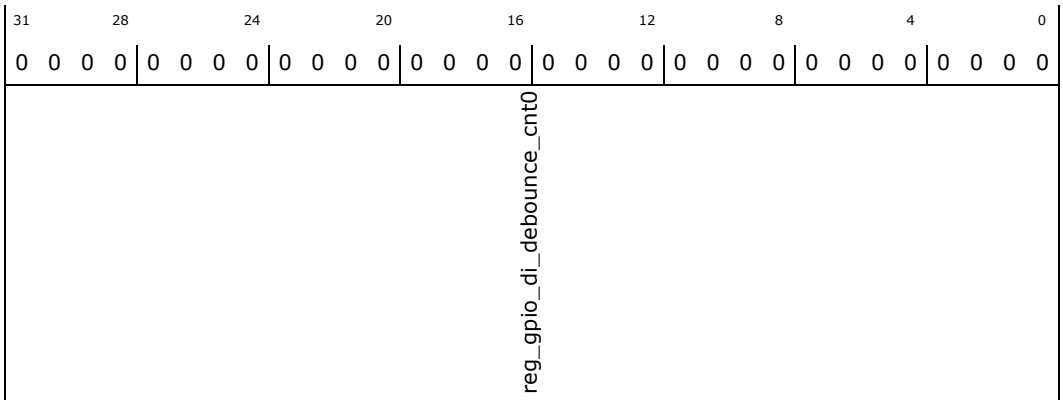
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_debounce_cnt0: [ISPMMADR] + 42Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_gpio_di_debounce_cnt0:** Indicates the period an input has to be stable before passing its value to the output*

3.7.35 reg_gpd_c_gpio_reg_gpio_di_debounce_cnt1_type (gpd_c_gpio_reg_gpio_di_debounce_cnt1)—Offset 430h

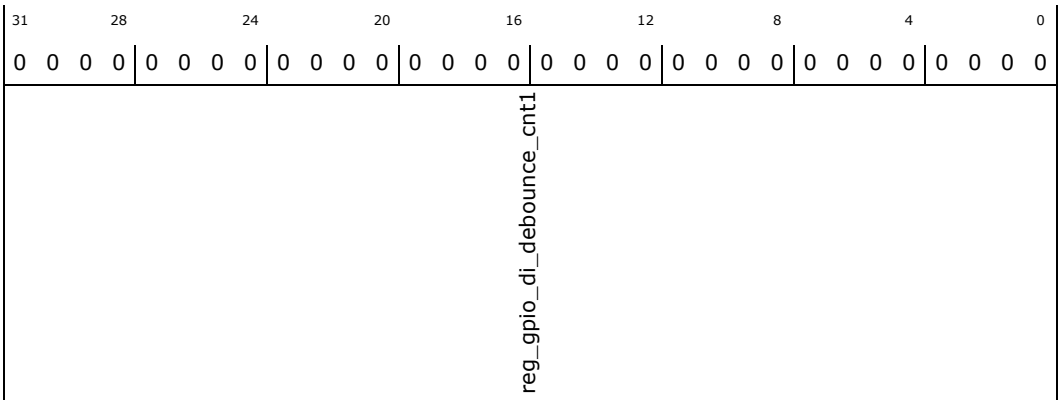
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_debounce_cnt1: [ISPMMADR] + 430h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_gpio_di_debounce_cnt1:** Indicates the period an input has to be stable before passing its value to the output*

3.7.36 reg_gpd_c_gpio_reg_gpio_di_debounce_cnt2_type (gpd_c_gpio_reg_gpio_di_debounce_cnt2)—Offset 434h

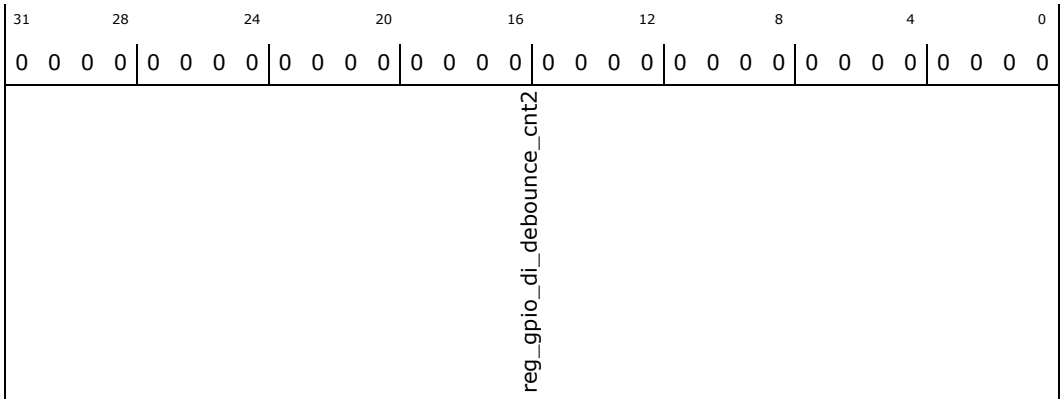
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_debounce_cnt2: [ISPMMADR] + 434h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_gpio_di_debounce_cnt2:** Indicates the period an input has to be stable before passing its value to the output

3.7.37 reg_gpd_c_gpio_reg_gpio_di_debounce_cnt3_type (gpd_c_gpio_reg_gpio_di_debounce_cnt3)—Offset 438h

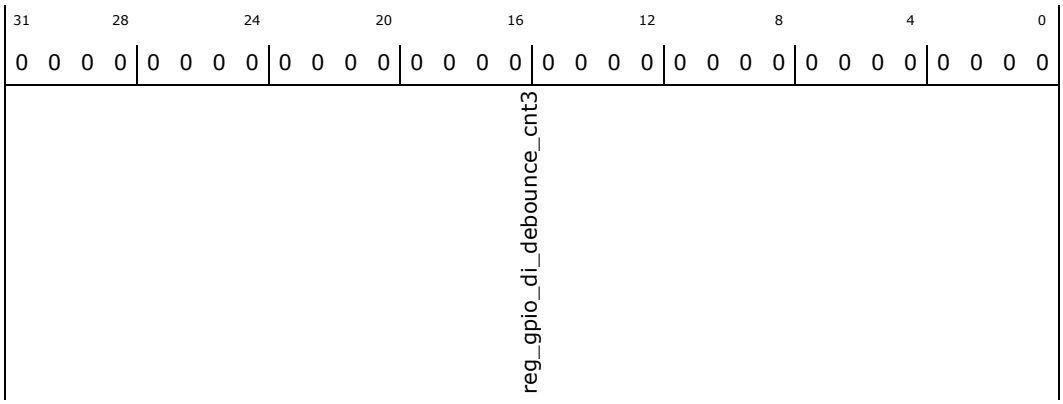
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_debounce_cnt3: [ISPMMADR] + 438h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_gpio_di_debounce_cnt3:** Indicates the period an input has to be stable before passing its value to the output

3.7.38 reg_gpd_c_gpio_reg_gpio_di_activelevel_type (gpd_c_gpio_reg_gpio_di_activelevel)—Offset 43Ch

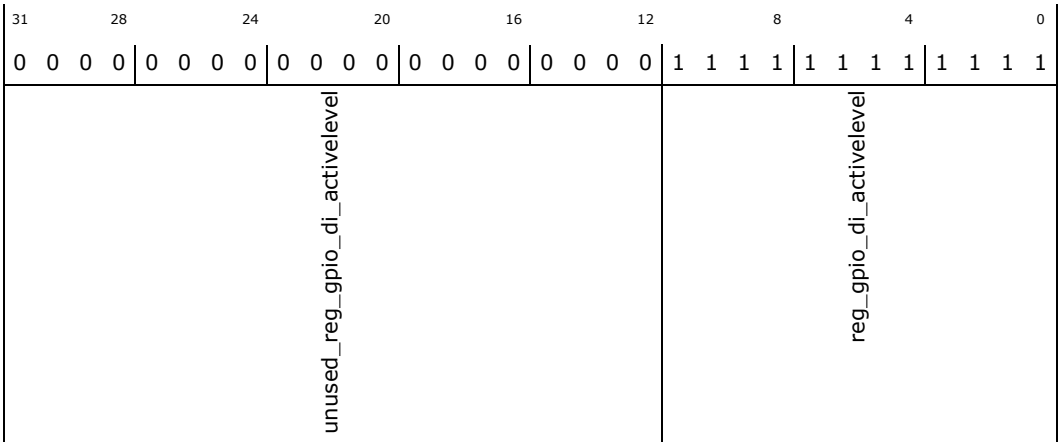
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_activelevel: [ISPMMADR] + 43Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000FFFh



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_di_activelevel:** Unused
11:0	FFFh RW	**reg_gpio_di_activelevel:** indicates for each bit whether it is intended to be active low (value='0') or active high (value='1').

3.7.39 reg_gpd_c_gpio_reg_gpio_di_type (gpd_c_gpio_reg_gpio_di)—Offset 440h

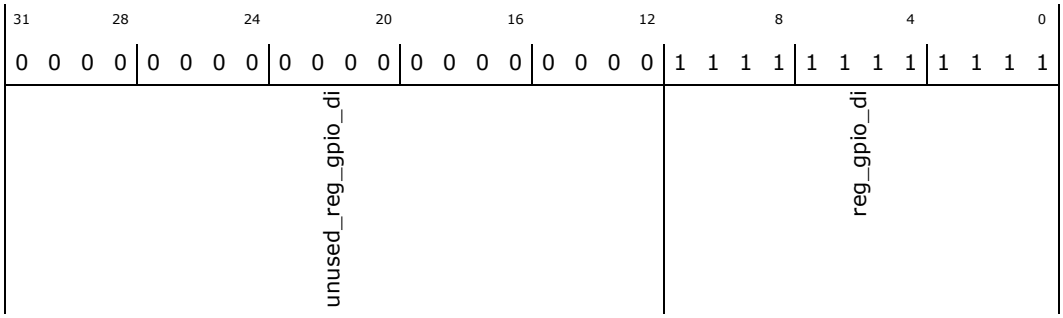
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di: [ISPMMADR] + 440h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000FFFh



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_di:** Unused
11:0	FFFh RO	**reg_gpio_di:** contains the values of all debounced, active level compensated inputs

3.7.40 reg_gpd_irq_ctrl_reg_irq_edge_type (gpd_irq_ctrl_reg_irq_edge)—Offset 500h

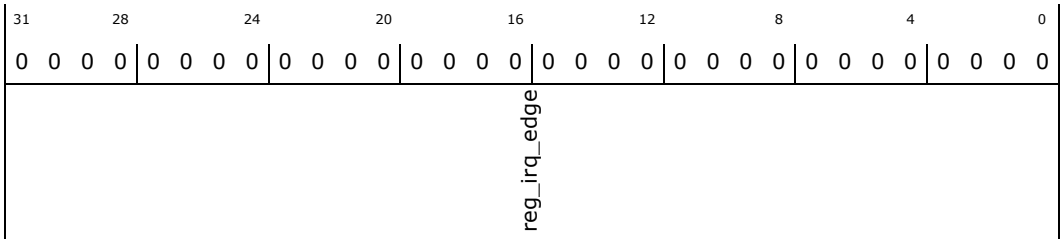
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_irq_ctrl_reg_irq_edge: [ISPMMADR] + 500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_irq_edge:** indicates for each bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

3.7.41 reg_gpd_irq_ctrl_reg_irq_mask_type (gpd_irq_ctrl_reg_irq_mask)—Offset 504h

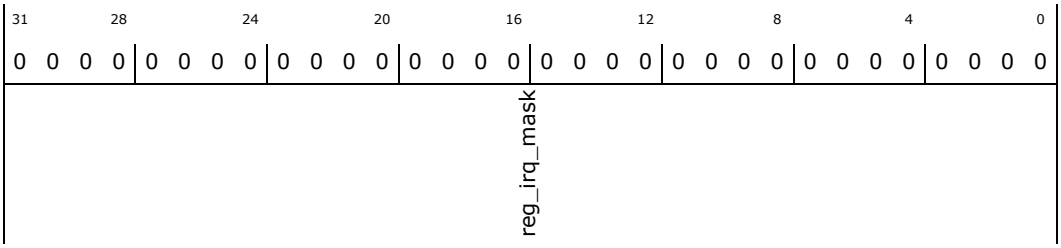
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_irq_ctrl_reg_irq_mask: [ISPMMADR] + 504h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_irq_mask:** indicates for each bit of irq_di whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

3.7.42 reg_gpd_irq_ctrl_reg_irq_status_type (gpd_irq_ctrl_reg_irq_status)—Offset 508h

Indicates for each bit whether a non-masked interrupt has been generated (value='1'). Can be cleared by writing a '1' into the the corresponding bit of the req_irq_clear register.

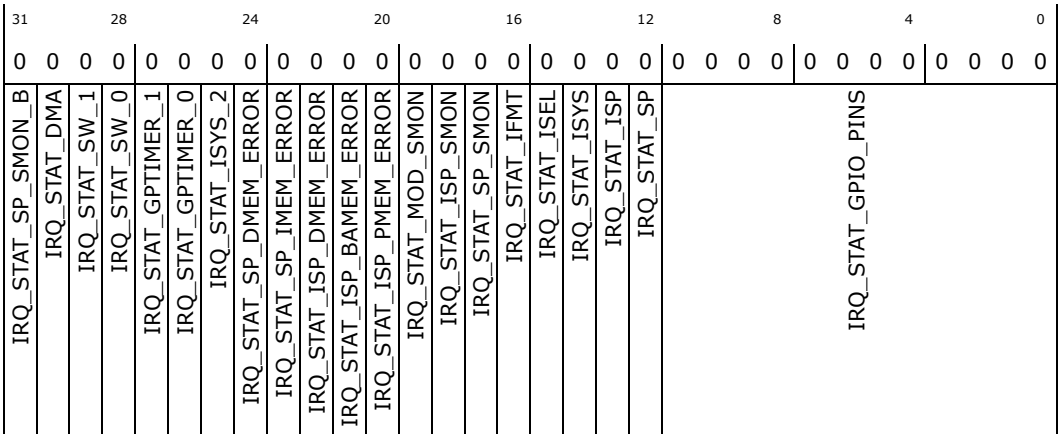
Access Method

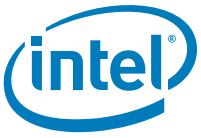
Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_irq_ctrl_reg_irq_status: [ISPMMADR] + 508h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31	0h RO	**IRQ_STAT_SP_SMON_B:** Represents the irq status of the irq_out from the SP streaming monitor b
30	0h RO	**IRQ_STAT_DMA:** Represents the irq status of the DMA
29	0h RO	**IRQ_STAT_SW_1:** Represents the irq status of the GP register IRQ SW 1
28	0h RO	**IRQ_STAT_SW_0:** Represents the irq status of the GP register IRQ SW 0
27	0h RO	**IRQ_STAT_GPTIMER_1:** Represents the irq status of the irq[1] out signal from the GP Timer block
26	0h RO	**IRQ_STAT_GPTIMER_0:** Represents the irq status of the irq[0] out signal from the GP Timer block
25	0h RO	**IRQ_STAT_ISYS_2:** Represents the irq status of the irq out signal from the input system
24	0h RO	**IRQ_STAT_SP_DMEM_ERROR:** Represents the irq status of the error signal from the SP data memory
23	0h RO	**IRQ_STAT_SP_IMEM_ERROR:** Represents the irq status of the error signal from the SP instruction cache memory
22	0h RO	**IRQ_STAT_ISP_DMEM_ERROR:** Represents the irq status of the error signal from the ISP data memory
21	0h RO	**IRQ_STAT_ISP_BAMEM_ERROR:** Represents the irq status of the error signal from the ISP vector memory
20	0h RO	**IRQ_STAT_ISP_PMEM_ERROR:** Represents the irq status of the error signal from the ISP program memory
19	0h RO	**IRQ_STAT_MOD_SMON:** Represents the irq status of the irq_out from the MOD streaming monitor
18	0h RO	**IRQ_STAT_ISP_SMON:** Represents the irq status of the irq_out from the ISP streaming monitor
17	0h RO	**IRQ_STAT_SP_SMON:** Represents the irq status of the irq_out from the SP streaming monitor
16	0h RO	**IRQ_STAT_IFMT:** Represents the irq status of the irq_out from the input formatting subsystem
15	0h RO	**IRQ_STAT_ISEL:** Represents the irq status of the irq_out from the input selector
14	0h RO	**IRQ_STAT_ISYS:** Represents the irq status of the irq_out from the input system
13	0h RO	**IRQ_STAT_ISP:** Represents the irq status of the irq_out from isp2300
12	0h RO	**IRQ_STAT_SP:** Represents the irq status of the irq_out from scalar processor
11:0	0h RO	**IRQ_STAT_GPIO_PINS:** Represents the irq status of the - potentially debounced - GPIO input pins

3.7.43 reg_gpd_irq_ctrl_reg_irq_clear_type (gpd_irq_ctrl_reg_irq_clear)—Offset 50Ch

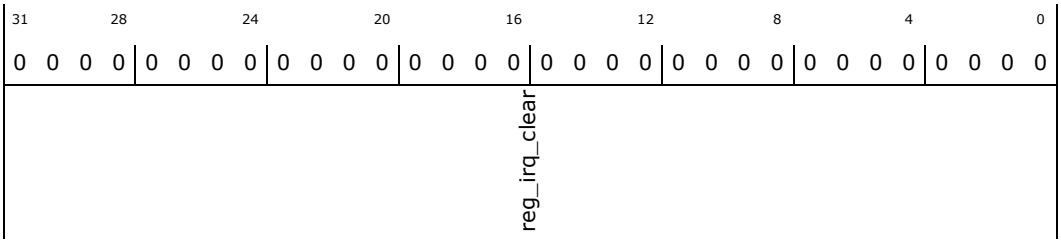
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_irq_ctrl_reg_irq_clear: [ISPMMADR] + 50Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h WO	**reg_irq_clear:** Clears (set to '0') bits in reg_irq_status. When writing a '1' into a bit of this register, the corresponding bit in the req_irq_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the req_irq_status is not affected.

3.7.44 reg_gpd_irq_ctrl_reg_irq_enable_type (gpd_irq_ctrl_reg_irq_enable)—Offset 510h

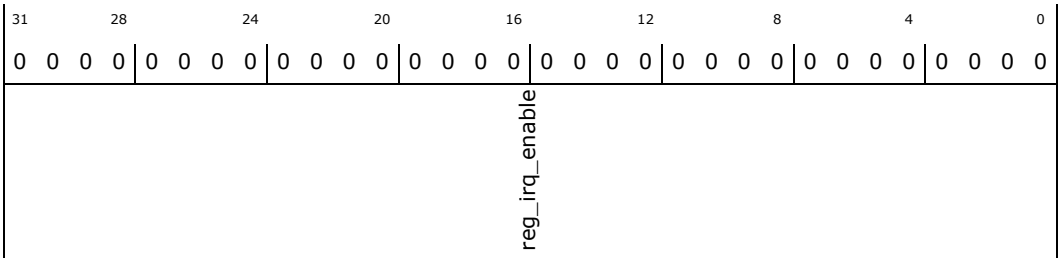
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_irq_ctrl_reg_irq_enable: [ISPMMADR] + 510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_irq_enable:** Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also affects the IRQ pin (value='1') or not (value='0')

3.7.45 reg_gpd_irq_ctrl_reg_irq_level_not_pulse_type (gpd_irq_ctrl_reg_irq_level_not_pulse)—Offset 514h

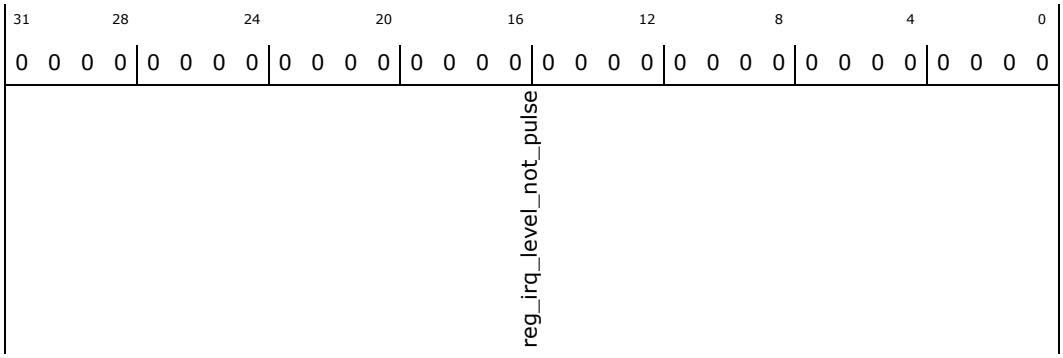
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_irq_ctrl_reg_irq_level_not_pulse: [ISPMMADR] + 514h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_irq_level_not_pulse:** Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

3.7.46 reg_gpd_irq_ctrl_reg_irq_str_out_enable_type (gpd_irq_ctrl_reg_irq_str_out_enable)—Offset 518h

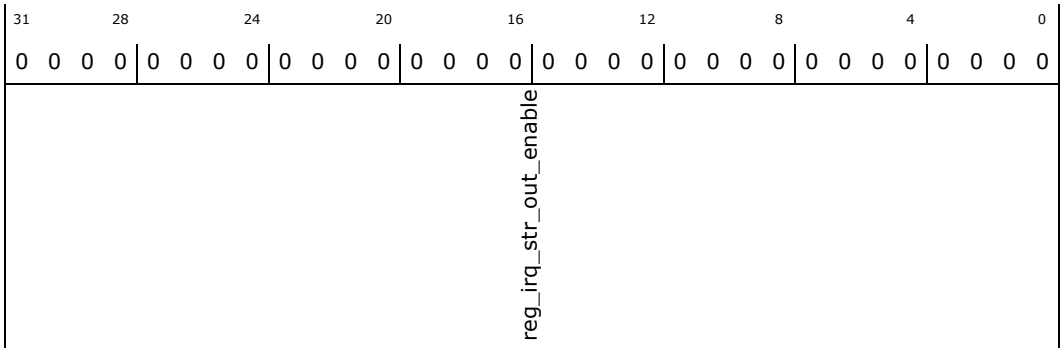
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_irq_ctrl_reg_irq_str_out_enable: [ISPMMADR] + 518h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**reg_irq_str_out_enable:** Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also results in a send token on the irq_str_out port (value='1') or not (value='0')

3.7.47 reg_gpd_gptimer_reg_reset_type (gpd_gptimer_reg_reset)—Offset 600h

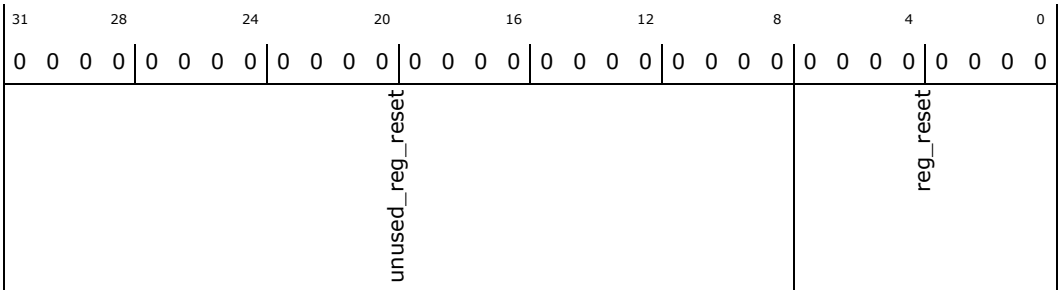
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_reg_reset: [ISPMMADR] + 600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_reg_reset:** Unused
7:0	0h WO	**reg_reset:** GP Timer reset. Write '1' to bit x to reset timer x. Write 0xFF to reset all timers.

3.7.48 reg_gpd_gptimer_overall_enable_type (gpd_gptimer_overall_enable)—Offset 604h

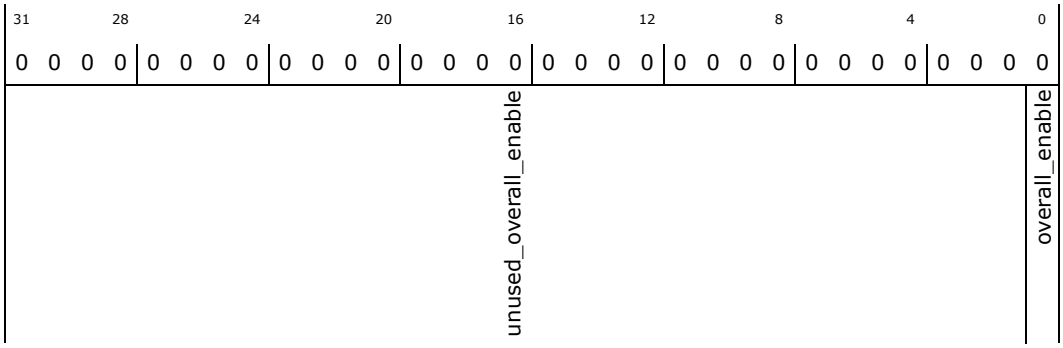
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_overall_enable: [ISPMMADR] + 604h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_overall_enable:** Unused
0	0h RW	**overall_enable:** GP Timer enable. Write '1' to enable all enabled timers, write '0' to disable all timers.

3.7.49 reg_gpd_gptimer_enable_timer_0_type (gpd_gptimer_enable_timer_0)—Offset 608h

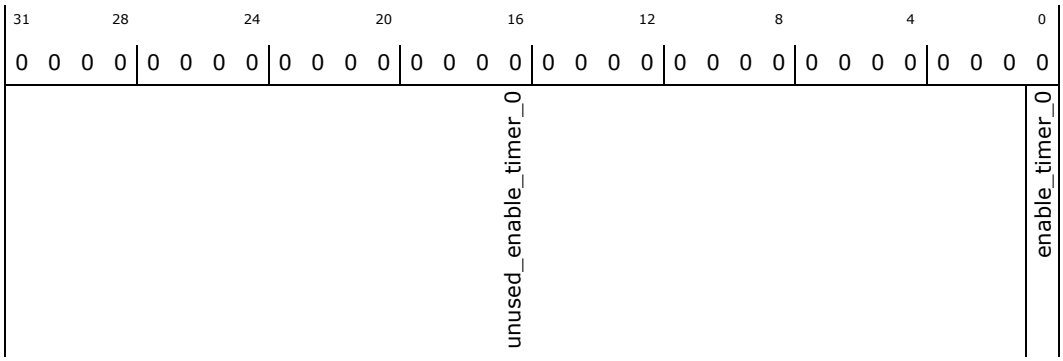
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_0: [ISPMMADR] + 608h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_0:** Unused
0	0h RW	**enable_timer_0:** GP Timer enable. Write '1' to enable timer 0. Write '0' to disable timer 0

3.7.50 reg_gpd_gptimer_enable_timer_1_type (gpd_gptimer_enable_timer_1)—Offset 60Ch

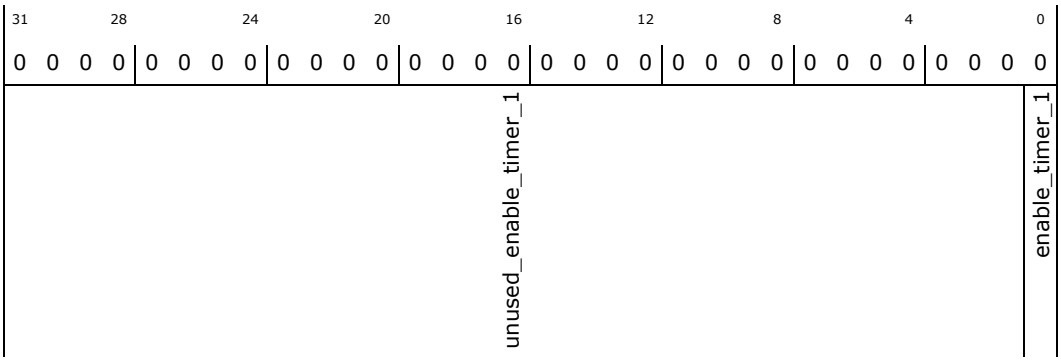
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_1: [ISPMMADR] + 60Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_1:** Unused
0	0h RW	**enable_timer_1:** GP Timer enable. Write '1' to enable timer 1. Write '0' to disable timer 1

3.7.51 reg_gpd_gptimer_enable_timer_2_type (gpd_gptimer_enable_timer_2)—Offset 610h

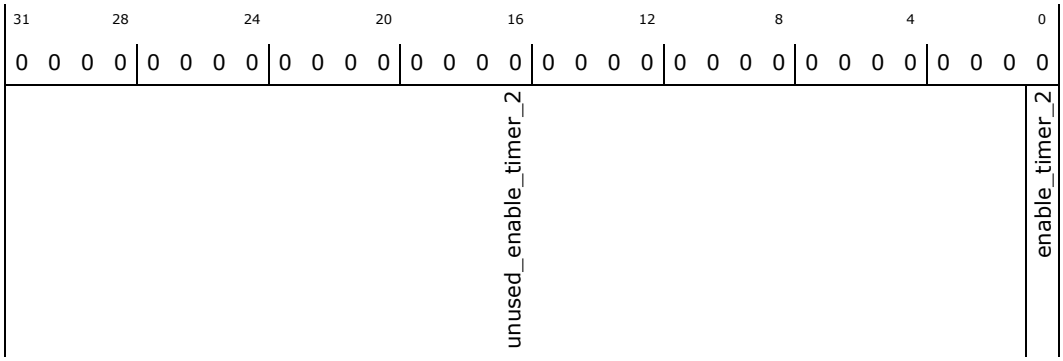
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_2: [ISPMMADR] + 610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_2:** Unused
0	0h RW	**enable_timer_2:** GP Timer enable. Write '1' to enable timer 2. Write '0' to disable timer 2

3.7.52 reg_gpd_gptimer_enable_timer_3_type (gpd_gptimer_enable_timer_3)—Offset 614h

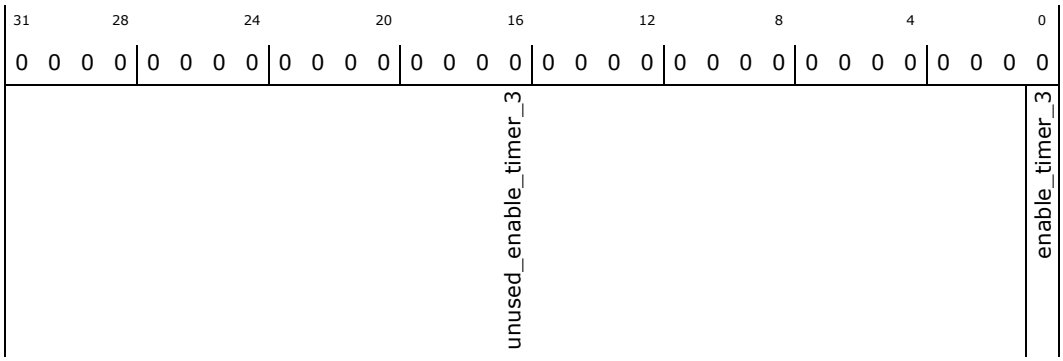
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_3: [ISPMMADR] + 614h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_3:** Unused
0	0h RW	**enable_timer_3:** GP Timer enable. Write '1' to enable timer 3. Write '0' to disable timer 3

3.7.53 reg_gpd_gptimer_enable_timer_4_type (gpd_gptimer_enable_timer_4)—Offset 618h

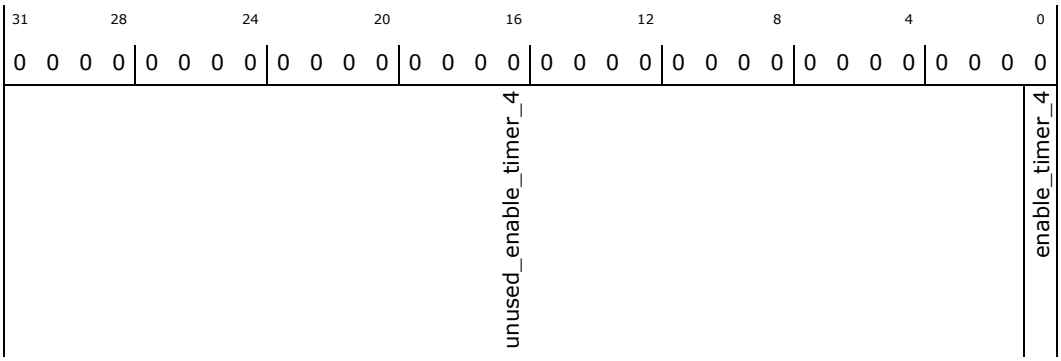
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_4: [ISPMMADR] + 618h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_4:** Unused
0	0h RW	**enable_timer_4:** GP Timer enable. Write '1' to enable timer 4. Write '0' to disable timer 4

3.7.54 reg_gpd_gptimer_enable_timer_5_type (gpd_gptimer_enable_timer_5)—Offset 61Ch

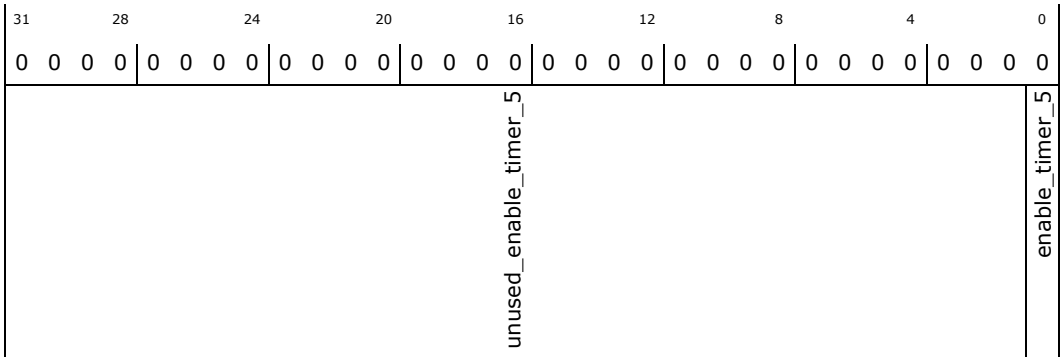
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_5: [ISPMMADR] + 61Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_5:** Unused
0	0h RW	**enable_timer_5:** GP Timer enable. Write '1' to enable timer 5. Write '0' to disable timer 5

3.7.55 reg_gpd_gptimer_enable_timer_6_type (gpd_gptimer_enable_timer_6)—Offset 620h

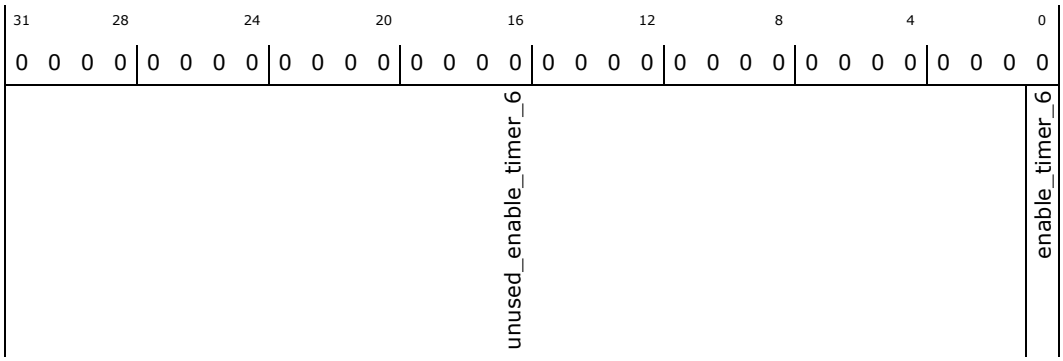
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_6: [ISPMMADR] + 620h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_6:** Unused
0	0h RW	**enable_timer_6:** GP Timer enable. Write '1' to enable timer 6. Write '0' to disable timer 6

3.7.56 reg_gpd_gptimer_enable_timer_7_type (gpd_gptimer_enable_timer_7)—Offset 624h

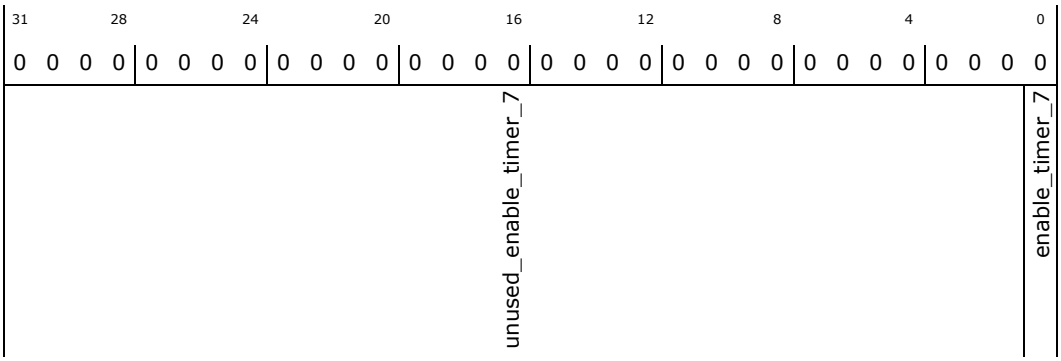
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_7: [ISPMMADR] + 624h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_7:** Unused
0	0h RW	**enable_timer_7:** GP Timer enable. Write '1' to enable timer 7. Write '0' to disable timer 7

3.7.57 reg_gpd_gptimer_value_timer_0_type (gpd_gptimer_value_timer_0)—Offset 628h

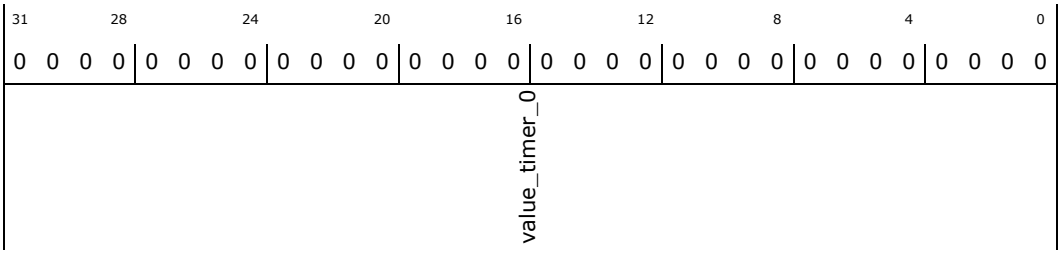
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_value_timer_0: [ISPMMADR] + 628h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_0:** Returns the value of timer 0

3.7.58 reg_gpd_gptimer_value_timer_1_type (gpd_gptimer_value_timer_1)—Offset 62Ch

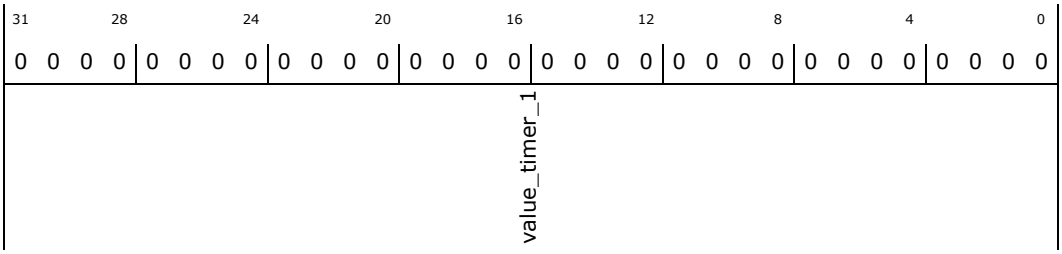
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_value_timer_1: [ISPMMADR] + 62Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_1:** Returns the value of timer 1

3.7.59 reg_gpd_gptimer_value_timer_2_type (gpd_gptimer_value_timer_2)—Offset 630h

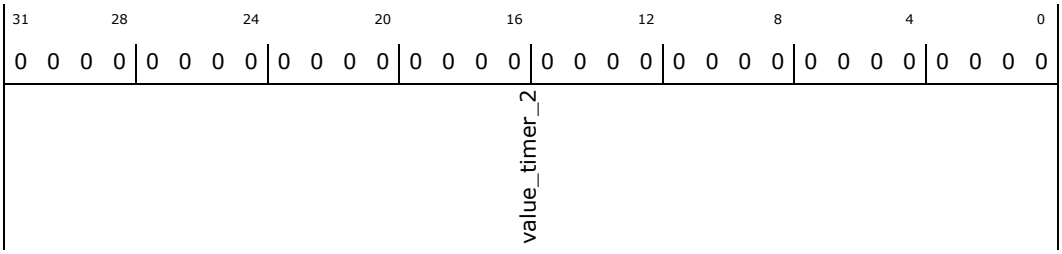
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_value_timer_2: [ISPMMADR] + 630h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_2:** Returns the value of timer 2

3.7.60 reg_gpd_gptimer_value_timer_3_type (gpd_gptimer_value_timer_3)—Offset 634h

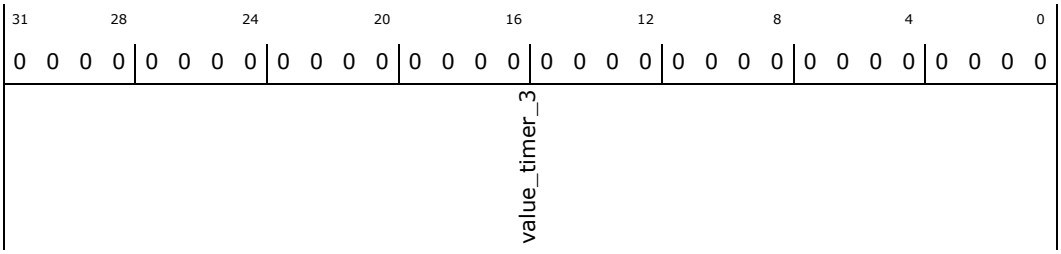
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_value_timer_3: [ISPMMADR] + 634h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_3:** Returns the value of timer 3

3.7.61 reg_gpd_gptimer_value_timer_4_type (gpd_gptimer_value_timer_4)—Offset 638h

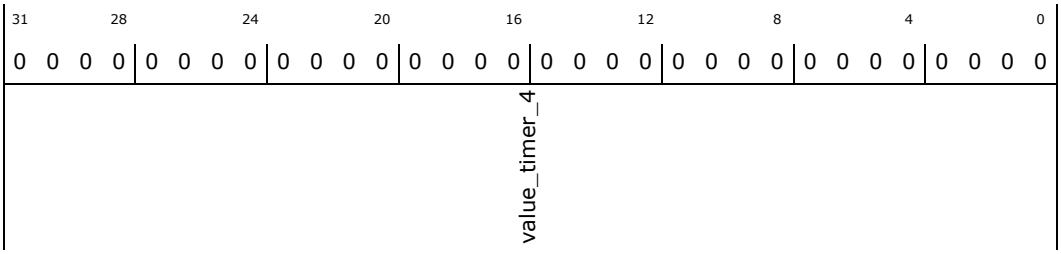
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_value_timer_4: [ISPMMADR] + 638h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_4:** Returns the value of timer 4

3.7.62 reg_gpd_gptimer_value_timer_5_type (gpd_gptimer_value_timer_5)—Offset 63Ch

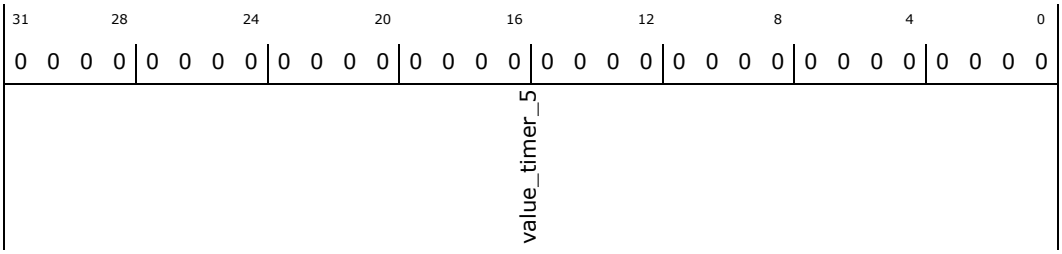
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_value_timer_5: [ISPMMADR] + 63Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_5:** Returns the value of timer 5

3.7.63 reg_gpd_gptimer_value_timer_6_type (gpd_gptimer_value_timer_6)—Offset 640h

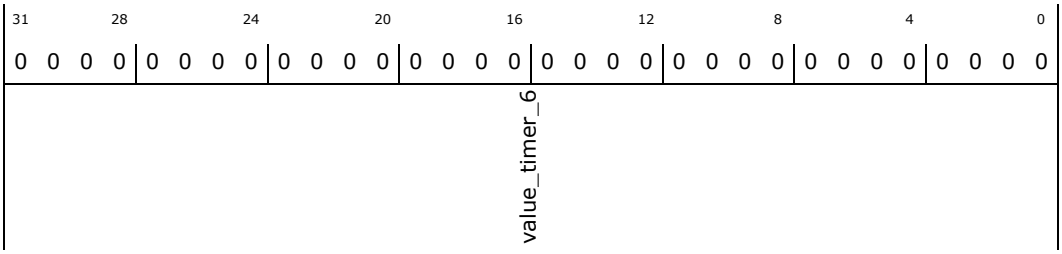
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_value_timer_6: [ISPMMADR] + 640h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_6:** Returns the value of timer 6

3.7.64 reg_gpd_gptimer_value_timer_7_type (gpd_gptimer_value_timer_7)—Offset 644h

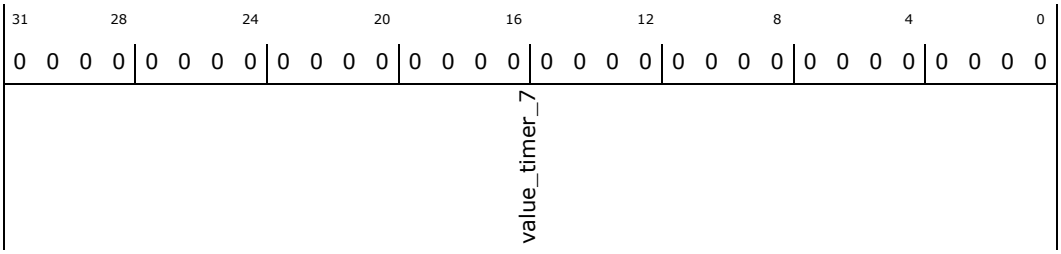
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_value_timer_7: [ISPMMADR] + 644h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_7:** Returns the value of timer 7

3.7.65 reg_gpd_gptimer_count_type_timer_0_type (gpd_gptimer_count_type_timer_0)—Offset 648h

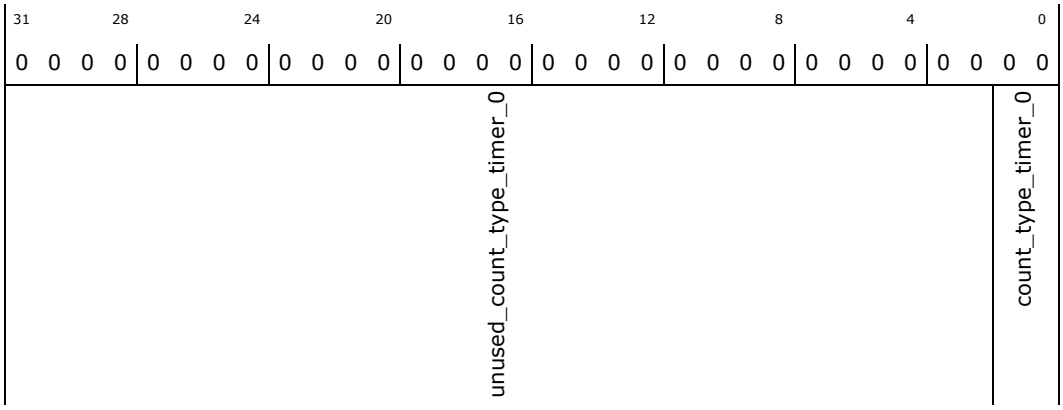
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_count_type_timer_0: [ISPMMADR] + 648h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_0:** Unused
1:0	0h RW	**count_type_timer_0:** Indicates what needs to be counted by timer 0, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

3.7.66 reg_gpd_gptimer_count_type_timer_1_type (gpd_gptimer_count_type_timer_1)—Offset 64Ch

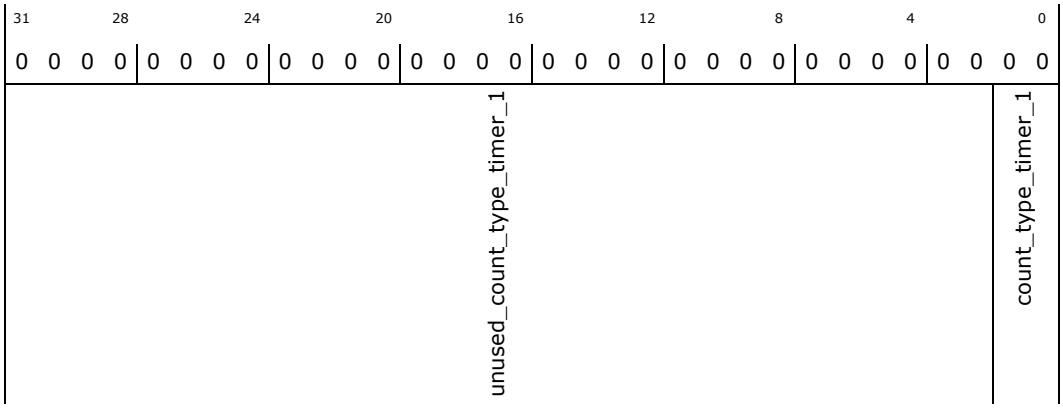
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_count_type_timer_1: [ISPMMADR] + 64Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_1:** Unused
1:0	0h RW	**count_type_timer_1:** Indicates what needs to be counted by timer 1, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

3.7.67 reg_gpd_gptimer_count_type_timer_2_type (gpd_gptimer_count_type_timer_2)—Offset 650h

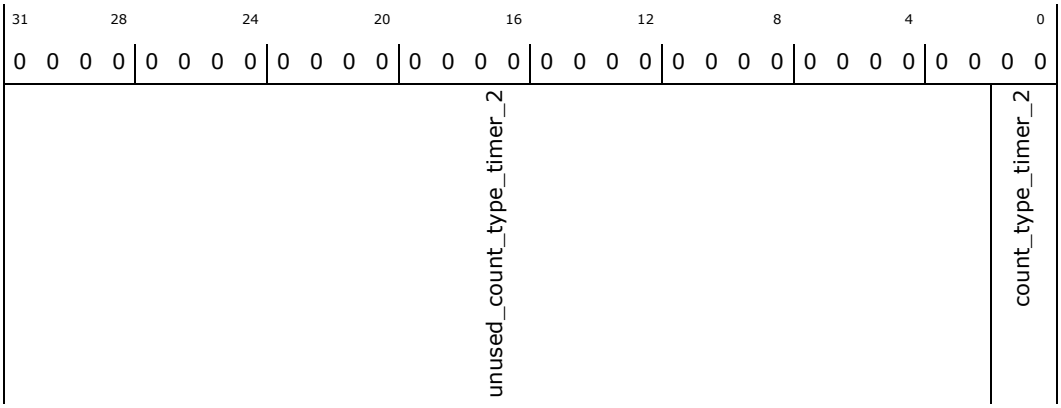
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_count_type_timer_2: [ISPMMADR] + 650h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_2:** Unused
1:0	0h RW	**count_type_timer_2:** Indicates what needs to be counted by timer 2, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

3.7.68 reg_gpd_gptimer_count_type_timer_3_type (gpd_gptimer_count_type_timer_3)—Offset 654h

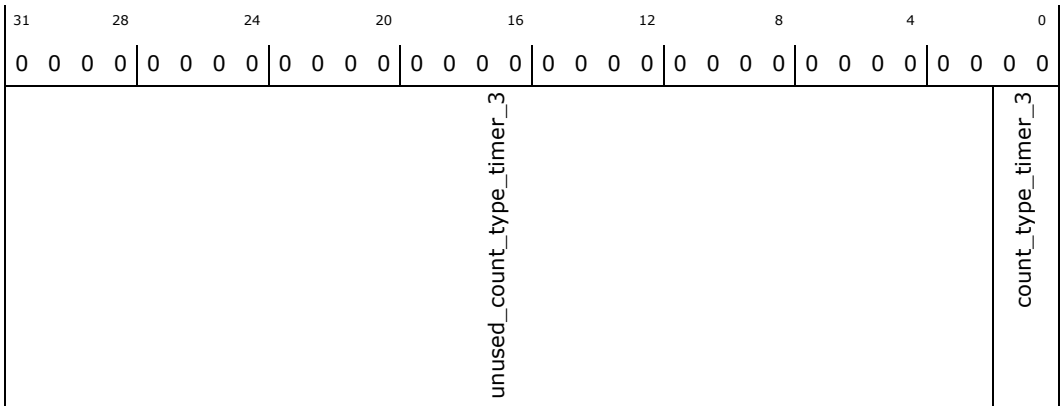
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_count_type_timer_3: [ISPMMADR] + 654h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_3:** Unused
1:0	0h RW	**count_type_timer_3:** Indicates what needs to be counted by timer 3, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

3.7.69 reg_gpd_gptimer_count_type_timer_4_type (gpd_gptimer_count_type_timer_4)—Offset 658h

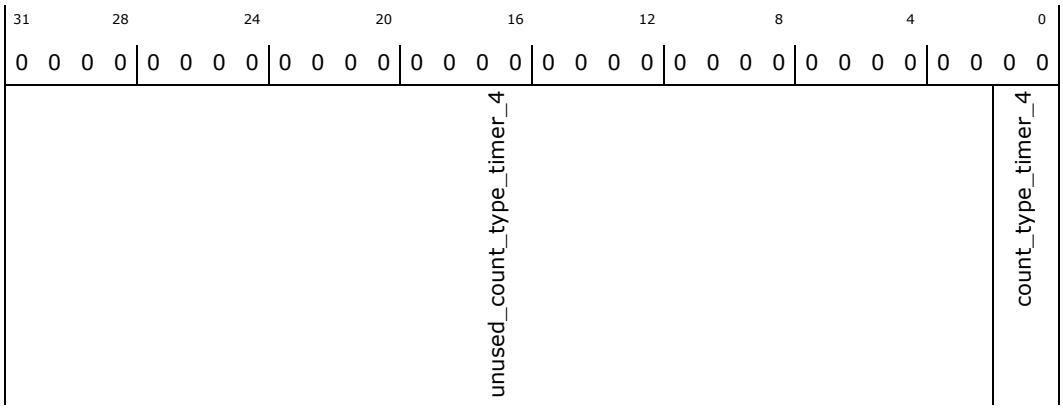
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_count_type_timer_4: [ISPMMADR] + 658h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_4:** Unused
1:0	0h RW	**count_type_timer_4:** Indicates what needs to be counted by timer 4, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

3.7.70 reg_gpd_gptimer_count_type_timer_5_type (gpd_gptimer_count_type_timer_5)—Offset 65Ch

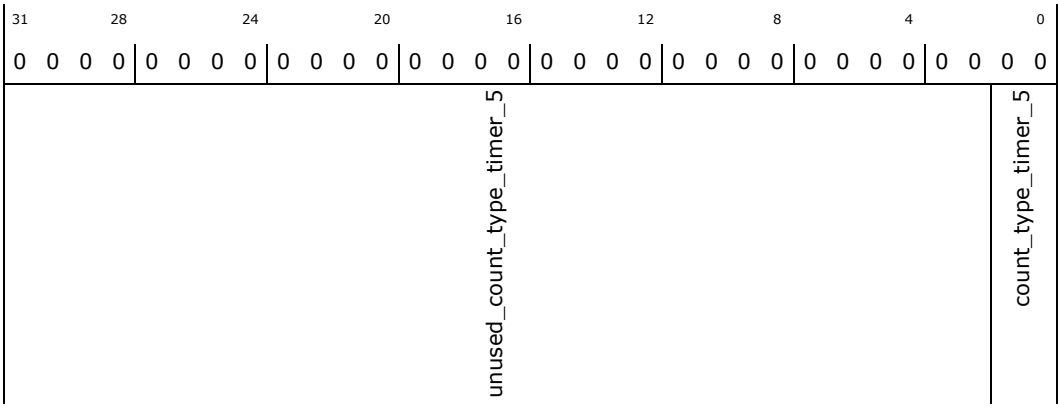
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_count_type_timer_5: [ISPMMADR] + 65Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_5:** Unused
1:0	0h RW	**count_type_timer_5:** Indicates what needs to be counted by timer 5, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

3.7.71 reg_gpd_gptimer_count_type_timer_6_type (gpd_gptimer_count_type_timer_6)—Offset 660h

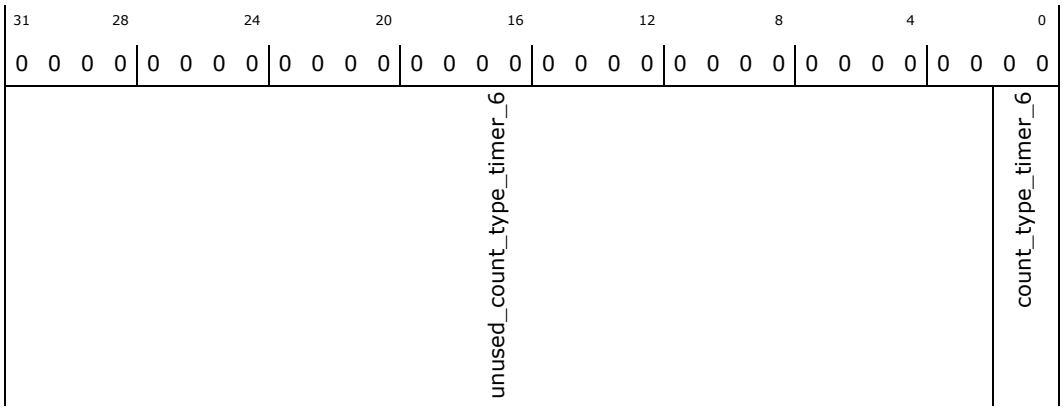
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_count_type_timer_6: [ISPMMADR] + 660h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_6:** Unused
1:0	0h RW	**count_type_timer_6:** Indicates what needs to be counted by timer 6, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

3.7.72 reg_gpd_gptimer_count_type_timer_7_type (gpd_gptimer_count_type_timer_7)—Offset 664h

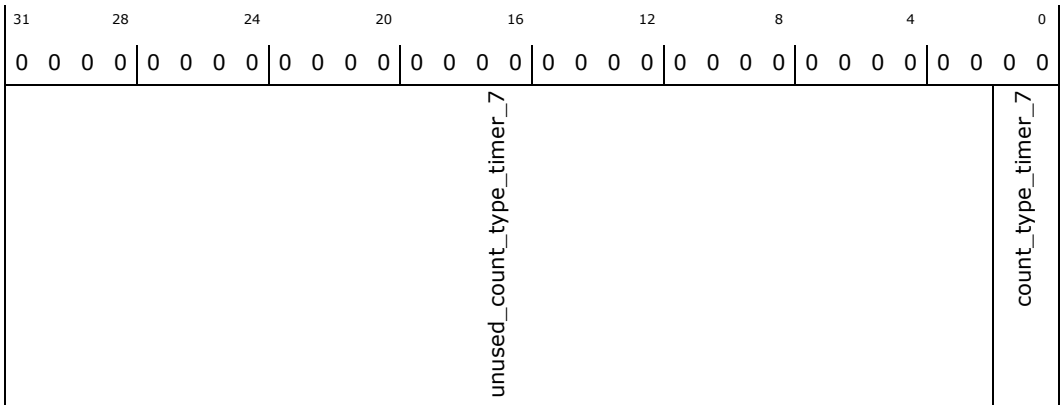
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_count_type_timer_7: [ISPMMADR] + 664h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_7:** Unused
1:0	0h RW	**count_type_timer_7:** Indicates what needs to be counted by timer 7, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

3.7.73 reg_gpd_gptimer_signal_select_timer_0_type (gpd_gptimer_signal_select_timer_0)—Offset 668h

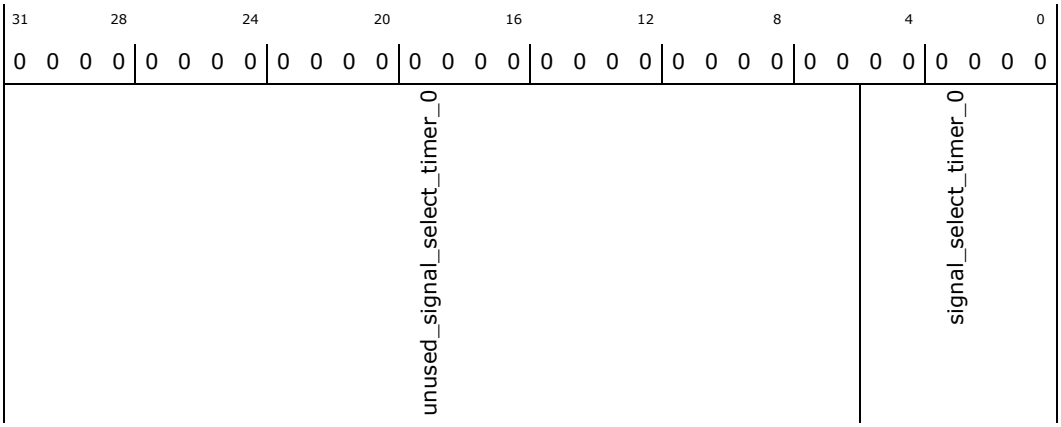
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_0: [ISPMMADR] + 668h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_0:** Unused
5:0	0h RW	**signal_select_timer_0:** Selects which of the 55 input signals is counted by timer 0

3.7.74 reg_gpd_gptimer_signal_select_timer_1_type (gpd_gptimer_signal_select_timer_1)—Offset 66Ch

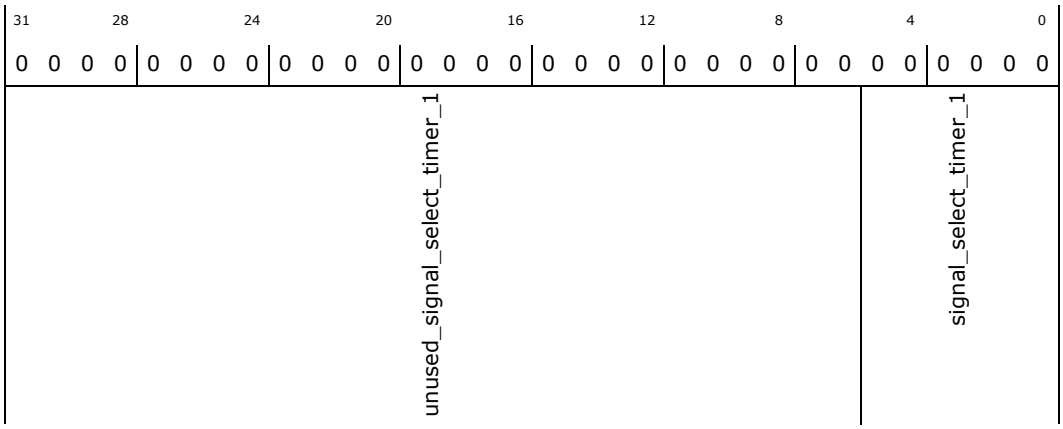
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_1: [ISPMMADR] + 66Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_1:** Unused
5:0	0h RW	**signal_select_timer_1:** Selects which of the 55 input signals is counted by timer 1

3.7.75 reg_gpd_gptimer_signal_select_timer_2_type (gpd_gptimer_signal_select_timer_2)—Offset 670h

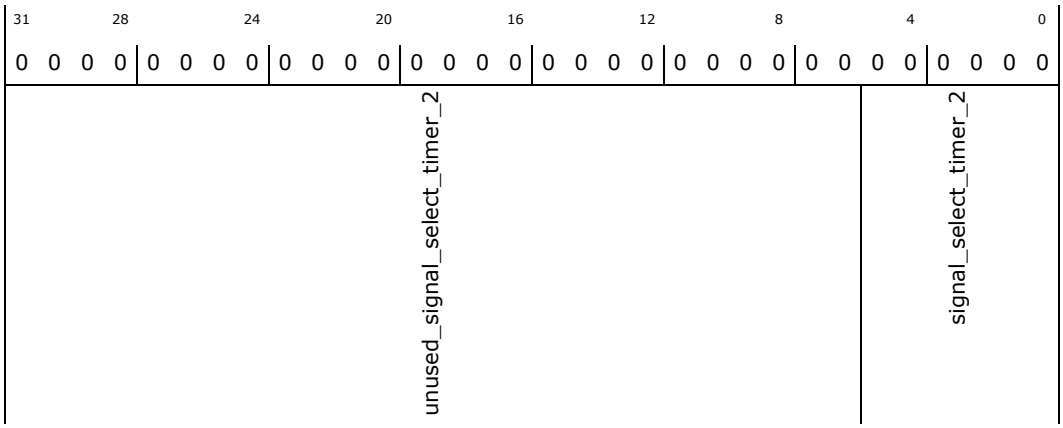
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_2: [ISPMMADR] + 670h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_2:** Unused
5:0	0h RW	**signal_select_timer_2:** Selects which of the 55 input signals is counted by timer 2

3.7.76 reg_gpd_gptimer_signal_select_timer_3_type (gpd_gptimer_signal_select_timer_3)—Offset 674h

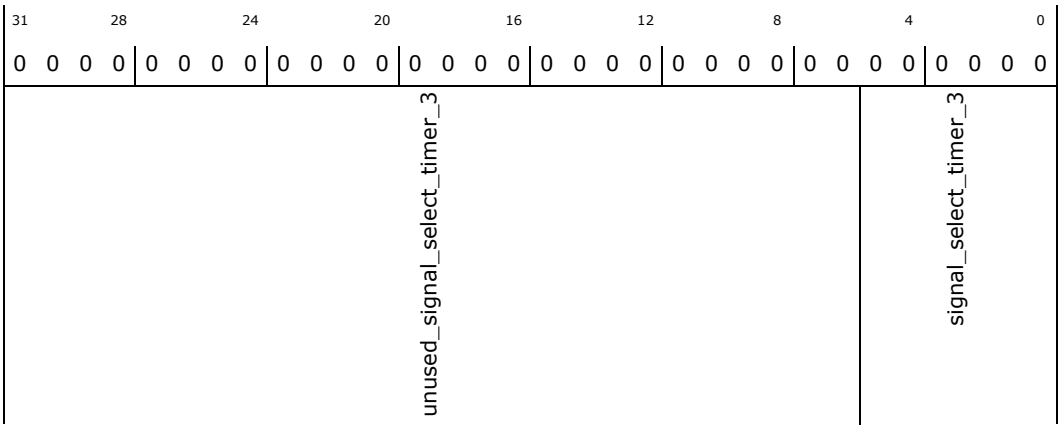
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_3: [ISPMMADR] + 674h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_3:** Unused
5:0	0h RW	**signal_select_timer_3:** Selects which of the 55 input signals is counted by timer 3

3.7.77 reg_gpd_gptimer_signal_select_timer_4_type (gpd_gptimer_signal_select_timer_4)—Offset 678h

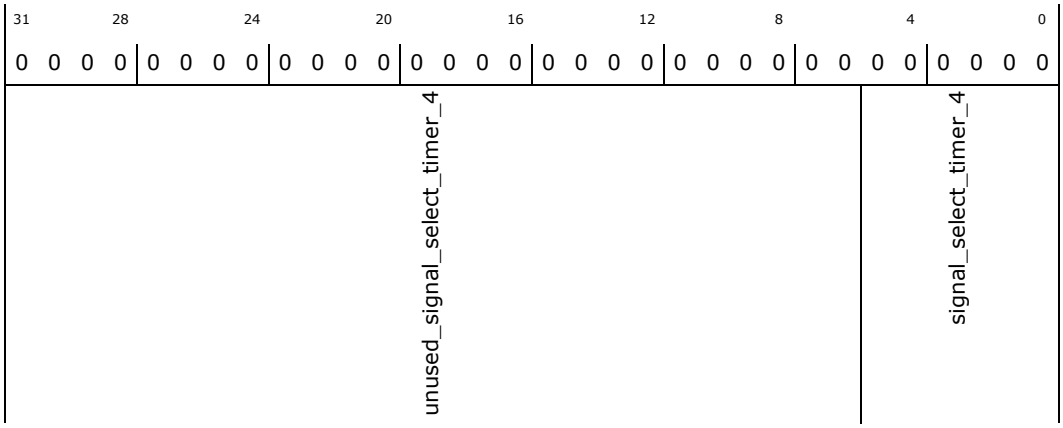
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_4: [ISPMMADR] + 678h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_4:** Unused
5:0	0h RW	**signal_select_timer_4:** Selects which of the 55 input signals is counted by timer 4

3.7.78 reg_gpd_gptimer_signal_select_timer_5_type (gpd_gptimer_signal_select_timer_5)—Offset 67Ch

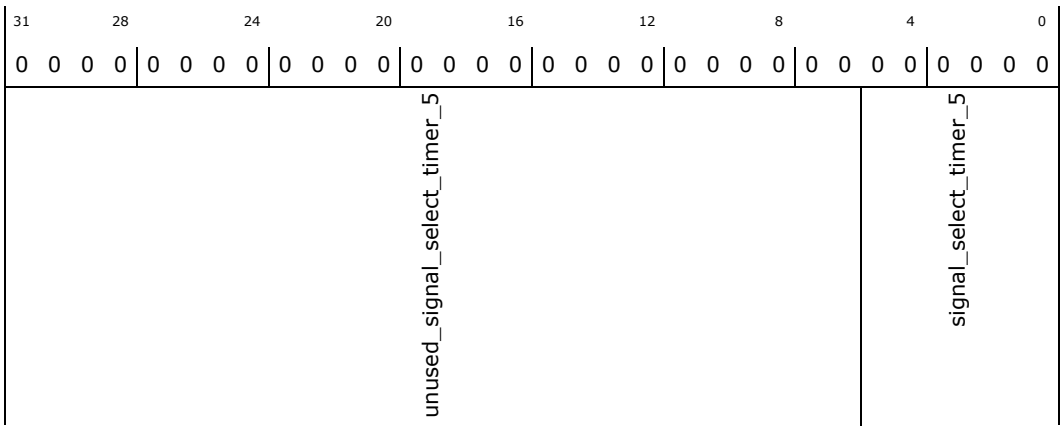
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_5: [ISPMMADR] + 67Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_5:** Unused
5:0	0h RW	**signal_select_timer_5:** Selects which of the 55 input signals is counted by timer 5

3.7.79 reg_gpd_gptimer_signal_select_timer_6_type (gpd_gptimer_signal_select_timer_6)—Offset 680h

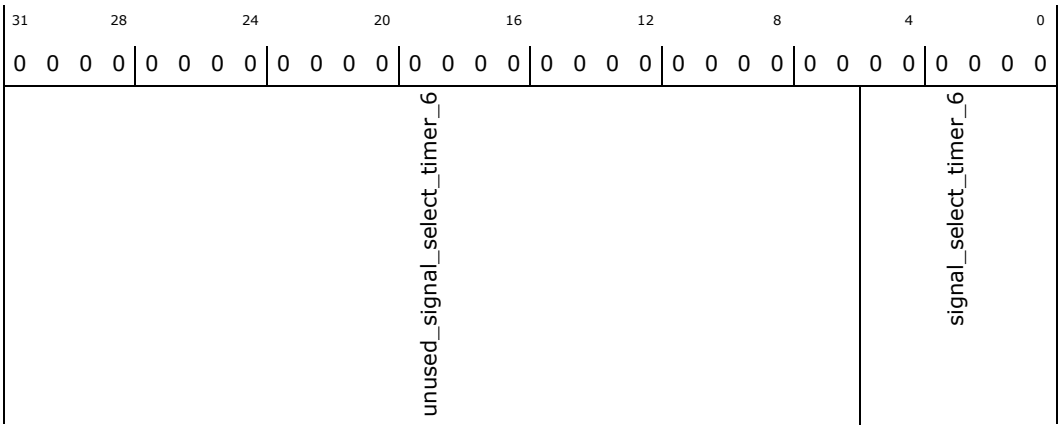
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_6: [ISPMMADR] + 680h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_6:** Unused
5:0	0h RW	**signal_select_timer_6:** Selects which of the 55 input signals is counted by timer 6

3.7.80 reg_gpd_gptimer_signal_select_timer_7_type (gpd_gptimer_signal_select_timer_7)—Offset 684h

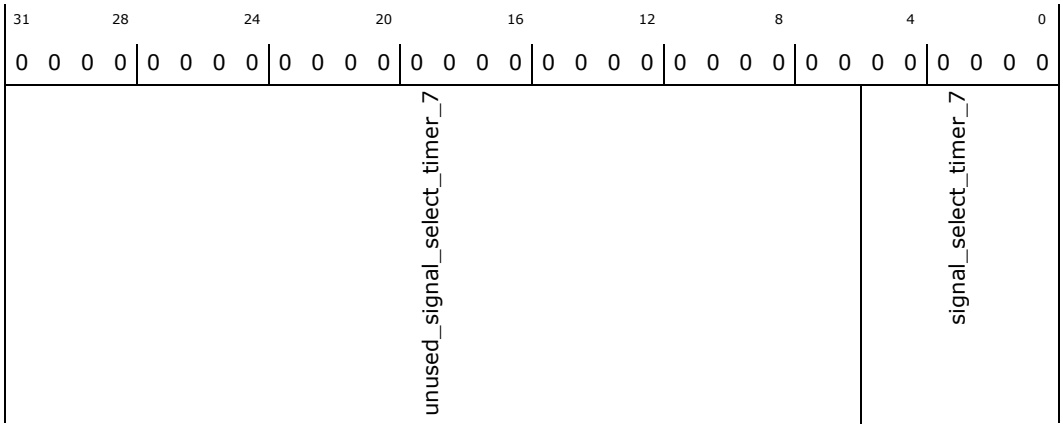
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_7: [ISPMMADR] + 684h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_7:** Unused
5:0	0h RW	**signal_select_timer_7:** Selects which of the 55 input signals is counted by timer 7

3.7.81 reg_gpd_gptimer_irq_trigger_value_0_type (gpd_gptimer_irq_trigger_value_0)—Offset 688h

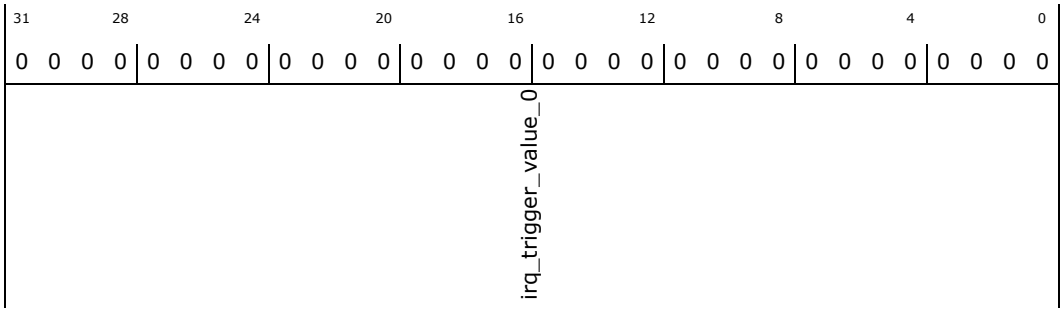
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_irq_trigger_value_0: [ISPMMADR] + 688h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**irq_trigger_value_0:** IRQ trigger value for interrupt 0. If the timer selected by irq_timer_select_0 reaches this value, irq_0 will be enabled

3.7.82 reg_gpd_gptimer_irq_trigger_value_1_type (gpd_gptimer_irq_trigger_value_1)—Offset 68Ch

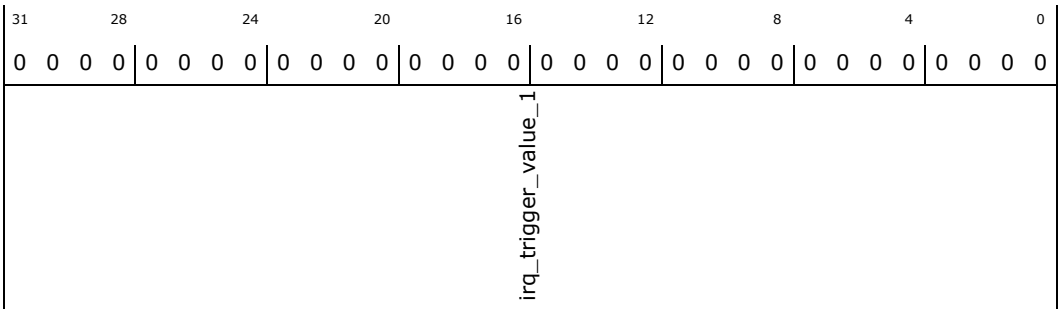
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_irq_trigger_value_1: [ISPMMADR] + 68Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**irq_trigger_value_1:** IRQ trigger value for interrupt 1. If the timer selected by irq_timer_select_1 reaches this value, irq_1 will be enabled

3.7.83 reg_gpd_gptimer_irq_timer_select_0_type (gpd_gptimer_irq_timer_select_0)—Offset 690h

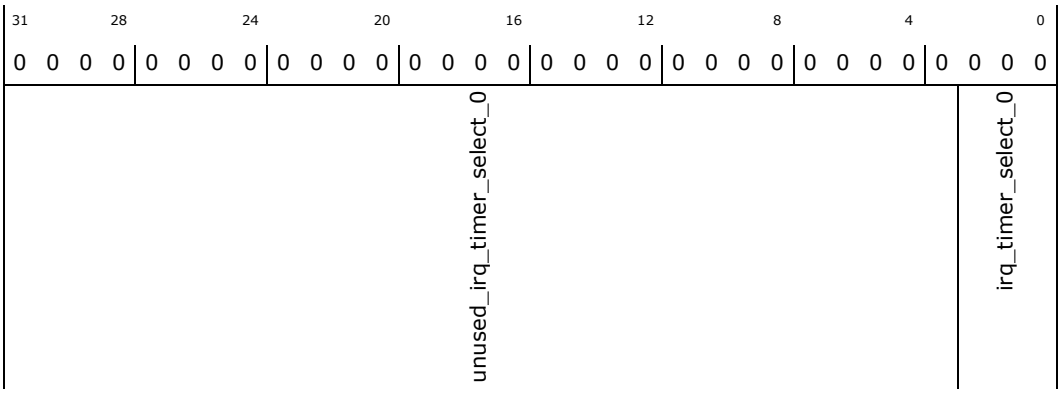
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_irq_timer_select_0: [ISPMMADR] + 690h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_irq_timer_select_0:** Unused
2:0	0h RW	**irq_timer_select_0:** Indicates which of the 8 timers will be used for irq_0 generation

3.7.84 reg_gpd_gptimer_irq_timer_select_1_type (gpd_gptimer_irq_timer_select_1)—Offset 694h

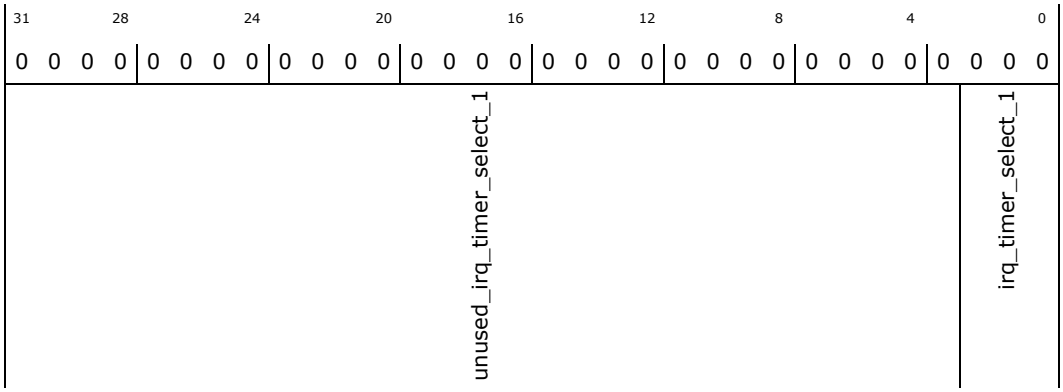
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_irq_timer_select_1: [ISPMMADR] + 694h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_irq_timer_select_1:** Unused
2:0	0h RW	**irq_timer_select_1:** Indicates which of the 8 timers will be used for irq_1 generation

3.7.85 reg_gpd_gptimer_irq_enable_0_type (gpd_gptimer_irq_enable_0)—Offset 698h

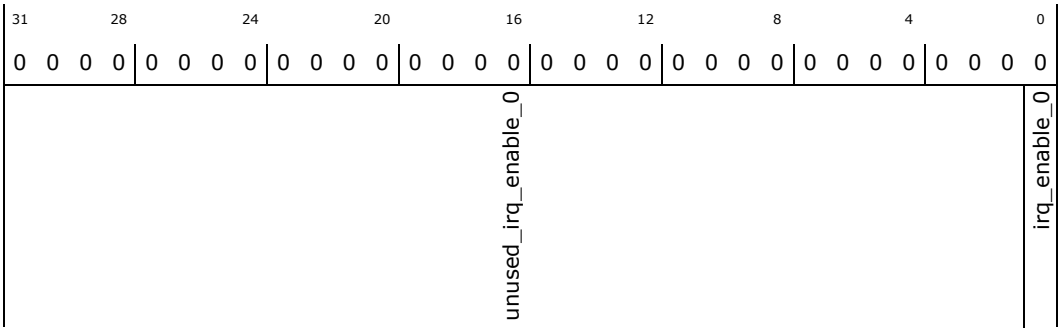
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_irq_enable_0: [ISPMMADR] + 698h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_irq_enable_0:** Unused
0	0h RW	**irq_enable_0:** Enable interrupt 0

3.7.86 reg_gpd_gptimer_irq_enable_1_type (gpd_gptimer_irq_enable_1)—Offset 69Ch

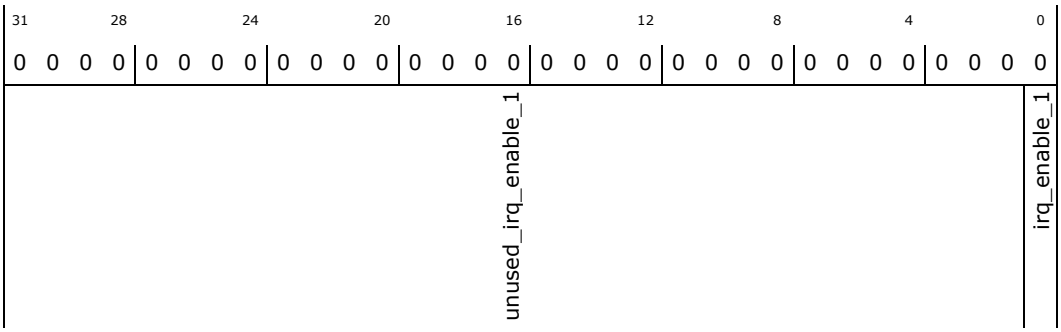
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_irq_enable_1: [ISPMMADR] + 69Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_irq_enable_1:** Unused
0	0h RW	**irq_enable_1:** Enable interrupt 1

3.7.87 reg_scp_stat_and_ctrl_type (scp_stat_and_ctrl)—Offset 10000h

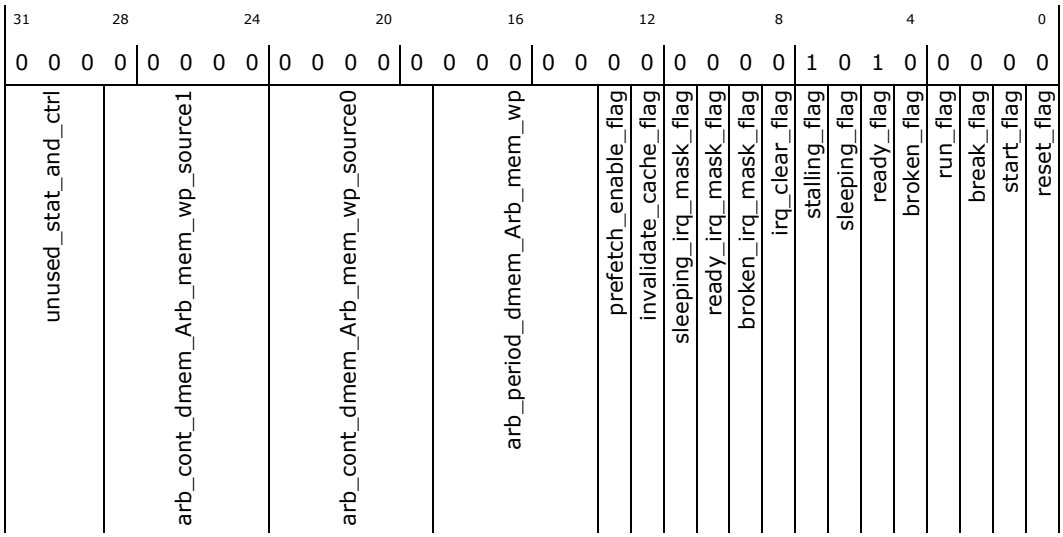
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_stat_and_ctrl: [ISPMMADR] + 10000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000A0h



Bit Range	Default & Access	Description
31:29	0h RW	**unused_stat_and_ctrl:** Unused
28:24	0h RW	**arb_cont_dmem_Arb_mem_wp_source1:** Arbiter contender group bandwidth for dmem_Arb_mem_wp_source1
23:19	0h RW	**arb_cont_dmem_Arb_mem_wp_source0:** Arbiter contender group bandwidth for dmem_Arb_mem_wp_source0
18:14	0h RW	**arb_period_dmem_Arb_mem_wp:** Arbiter period for dmem_Arb_mem_wp
13	0h RW	**prefetch_enable_flag:** Prefetch enable flag for config_ilm_conf_ilm_icache
12	0h RW	**invalidate_cache_flag:** Invalidate cache flag for config_ilm_conf_ilm_icache
11	0h RW	**sleeping_irq_mask_flag:** Sleeping IRQ mask flag
10	0h RW	**ready_irq_mask_flag:** Ready IRQ mask flag
9	0h RW	**broken_irq_mask_flag:** Broken IRQ mask flag

Bit Range	Default & Access	Description
8	0h RW	**irq_clear_flag:** IRQ clear flag
7	1h RO	**stalling_flag:** Stalling flag. Set to one when not executing an instruction.
6	0h RO	**sleeping_flag:** Sleeping flag
5	1h RO	**ready_flag:** Ready flag. Set to one when not executing a program.
4	0h RO	**broken_flag:** Broken flag
3	0h RW	**run_flag:** Run flag
2	0h RW	**break_flag:** Break flag
1	0h WO	**start_flag:** Start flag
0	0h WO	**reset_flag:** Reset flag

3.7.88 reg_scp_base_address_type (scp_base_address)—Offset 10004h

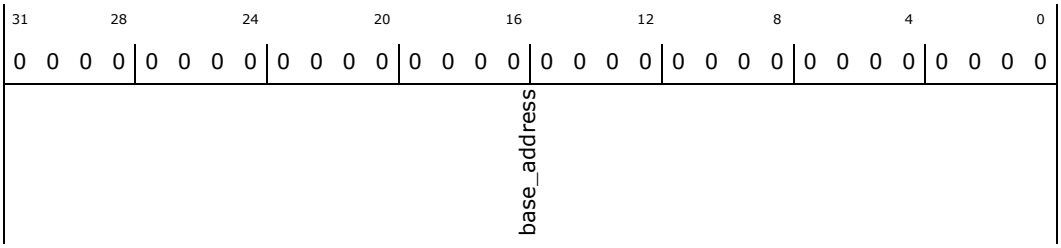
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_base_address: [ISPMMADR] + 10004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**base_address:** Start address

3.7.89 reg_scp_unused_2_type (scp_unused_2)—Offset 10008h

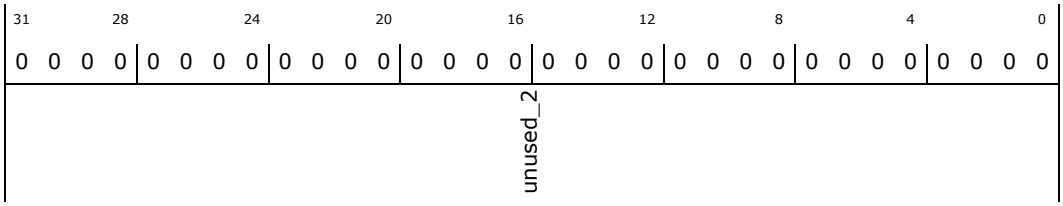
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_unused_2: [ISPMMADR] + 10008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**unused_2:** Unused

3.7.90 reg_scp_base_addr_seg_0_MI_xmem_master_int_type (scp_base_addr_seg_0_MI_xmem_master_int)—Offset 10010h

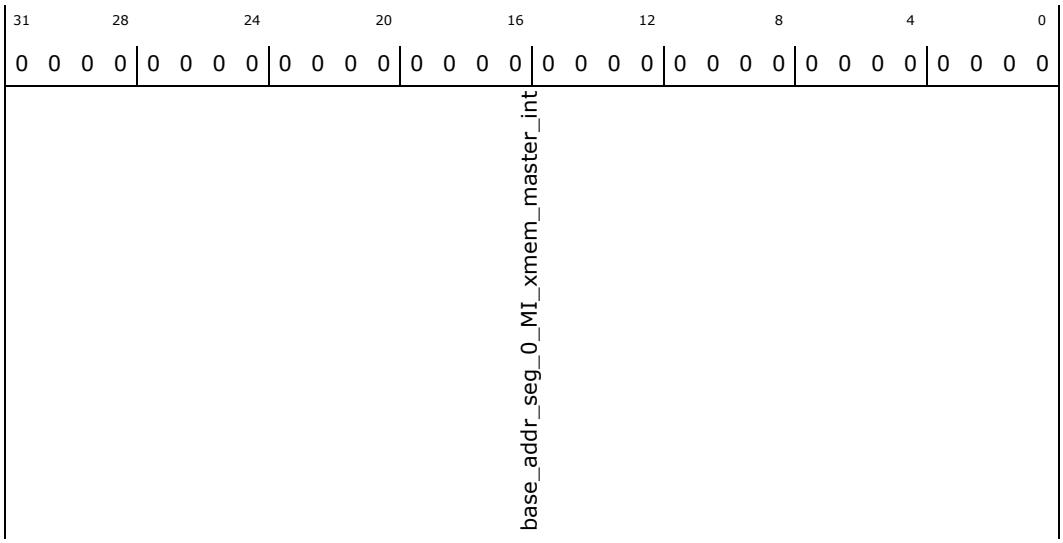
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_base_addr_seg_0_MI_xmem_master_int: [ISPMMADR] + 10010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**base_addr_seg_0_MI_xmem_master_int:** Base address for segment 0 of master interface xmem_master_int

3.7.91 reg_scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master_type (scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master)—Offset 10014h

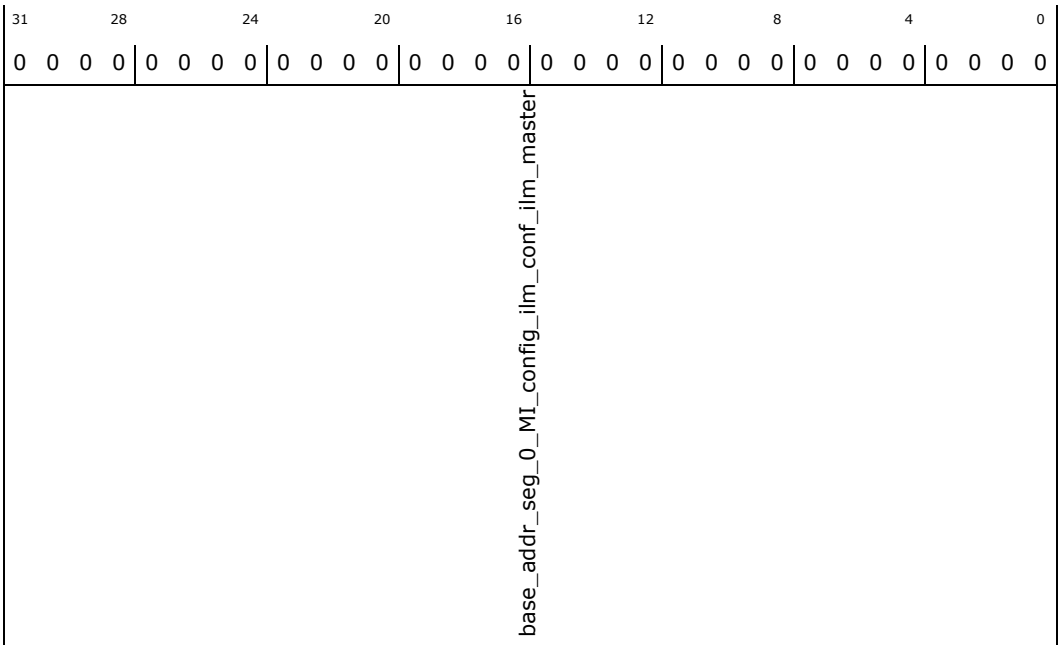
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master: [ISPMMADR] + 10014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**base_addr_seg_0_MI_config_ilm_conf_ilm_master:** Base address for segment 0 of master interface config_ilm_conf_ilm_master

3.7.92 reg_scp_unused_6_type (scp_unused_6)—Offset 10018h

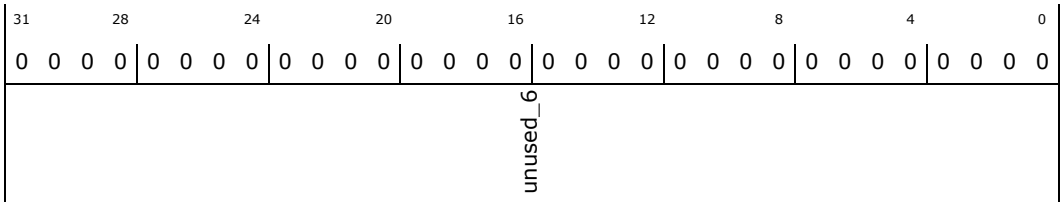
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_unused_6: [ISPMMADR] + 10018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**unused_6:** Unused

3.7.93 reg_scp_unused_7_type (scp_unused_7)—Offset 1001Ch

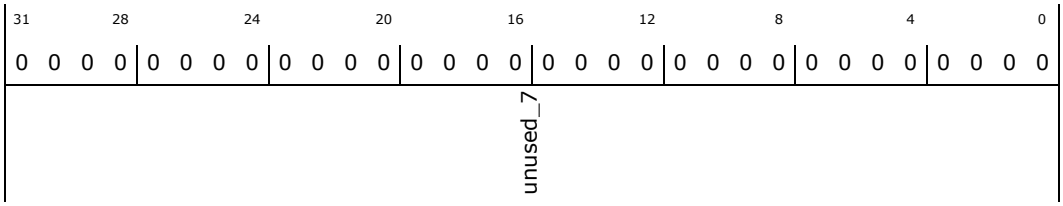
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_unused_7: [ISPMMADR] + 1001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**unused_7:** Unused

3.7.94 reg_scp_debug_pc_type (scp_debug_pc)—Offset 10024h

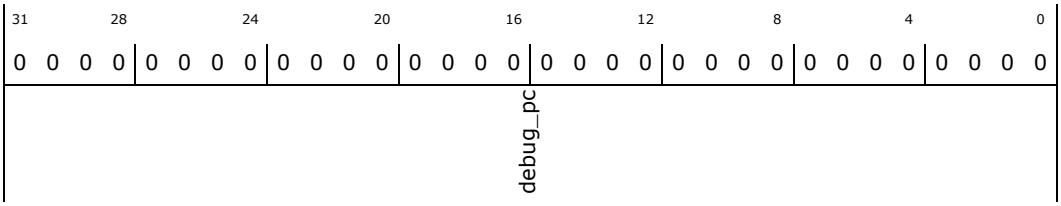
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_debug_pc: [ISPMMADR] + 10024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**debug_pc:** Debug program counter

3.7.95 reg_scp_stall_stat_fifo_loc_mt_am_inst_0_op0_type (scp_stall_stat_fifo_loc_mt_am_inst_0_op0)—Offset 10028h

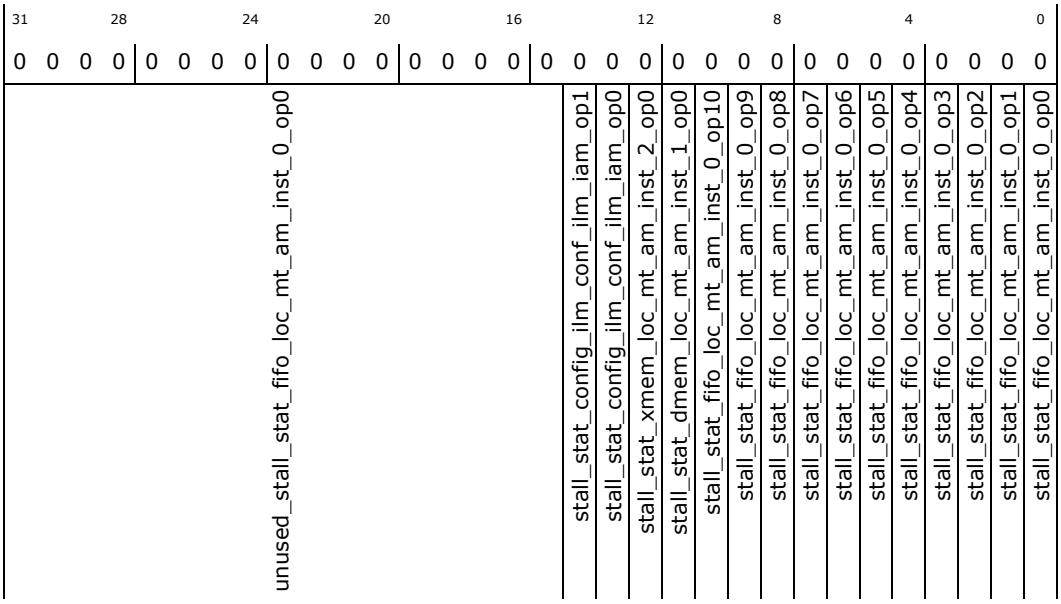
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

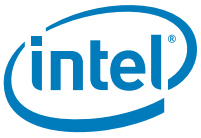
scp_stall_stat_fifo_loc_mt_am_inst_0_op0: [ISPMMADR] + 10028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RW	**unused_stall_stat_fifo_loc_mt_am_inst_0_op0:** Unused



Bit Range	Default & Access	Description
14	0h RO	**stall_stat_config_ilm_conf_ilm_iam_op1:** Stalling flag for msink config_ilm_conf_ilm_iam_op1
13	0h RO	**stall_stat_config_ilm_conf_ilm_iam_op0:** Stalling flag for msink config_ilm_conf_ilm_iam_op0
12	0h RO	**stall_stat_xmem_loc_mt_am_inst_2_op0:** Stalling flag for msink xmem_loc_mt_am_inst_2_op0
11	0h RO	**stall_stat_dmem_loc_mt_am_inst_1_op0:** Stalling flag for msink dmem_loc_mt_am_inst_1_op0
10	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op10:** Stalling flag for msink fifo_loc_mt_am_inst_0_op10
9	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op9:** Stalling flag for msink fifo_loc_mt_am_inst_0_op9
8	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op8:** Stalling flag for msink fifo_loc_mt_am_inst_0_op8
7	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op7:** Stalling flag for msink fifo_loc_mt_am_inst_0_op7
6	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op6:** Stalling flag for msink fifo_loc_mt_am_inst_0_op6
5	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op5:** Stalling flag for msink fifo_loc_mt_am_inst_0_op5
4	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op4:** Stalling flag for msink fifo_loc_mt_am_inst_0_op4
3	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op3:** Stalling flag for msink fifo_loc_mt_am_inst_0_op3
2	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op2:** Stalling flag for msink fifo_loc_mt_am_inst_0_op2
1	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op1:** Stalling flag for msink fifo_loc_mt_am_inst_0_op1
0	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op0:** Stalling flag for msink fifo_loc_mt_am_inst_0_op0

3.7.96 reg_scp_unused_11_type (scp_unused_11)—Offset 1002Ch

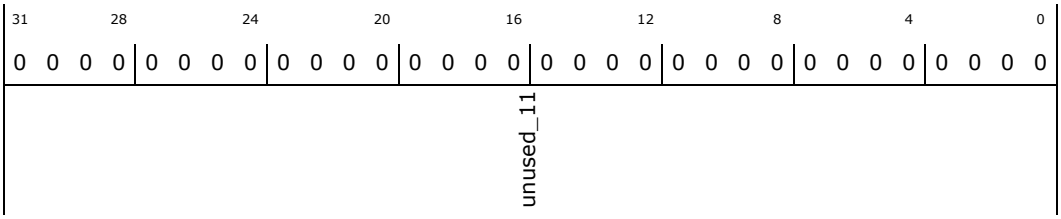
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_unused_11: [ISPMMADR] + 1002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**unused_11:** Unused

3.7.97 reg_scp_pmem_slave_access_type (scp_pmem_slave_access)—Offset 10030h

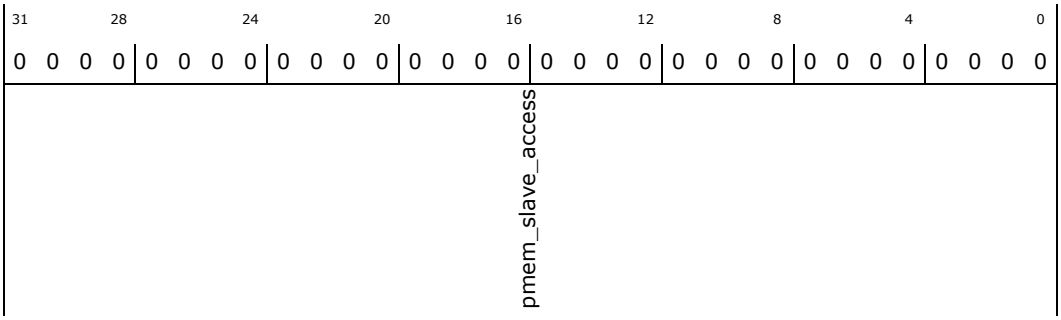
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_pmem_slave_access: [ISPMMADR] + 10030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**pmem_slave_access:** Pmem slave access flag

3.7.98 reg_isp_stat_and_ctrl_type (isp_stat_and_ctrl)—Offset 20000h

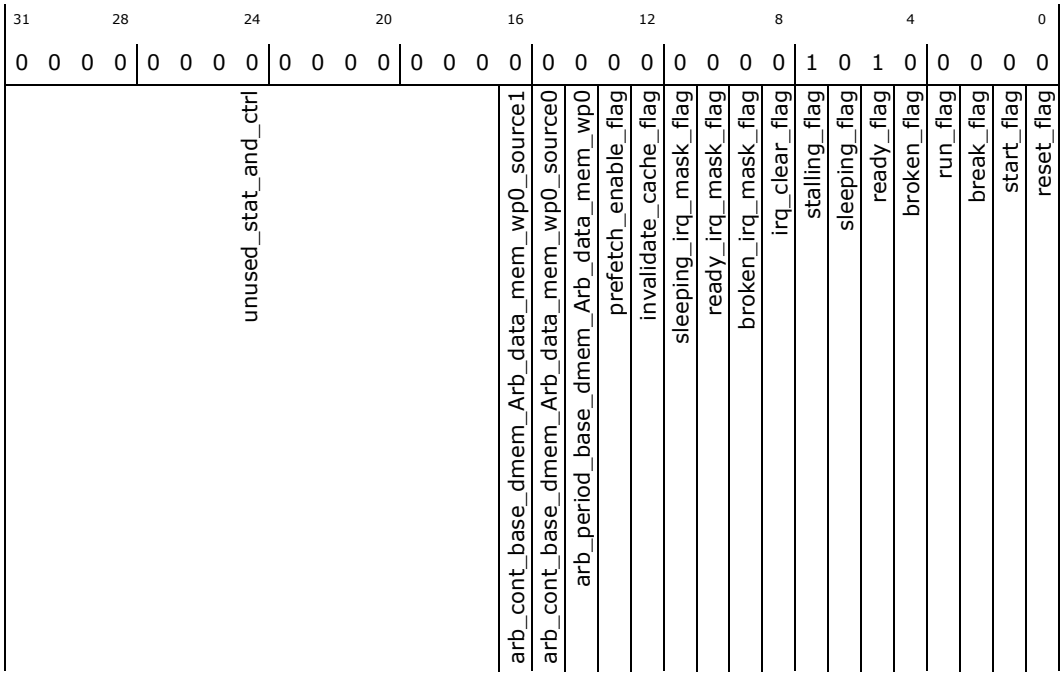
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_stat_and_ctrl: [ISPMMADR] + 20000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000A0h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_stat_and_ctrl:** Unused
16	0h RW	**arb_cont_base_dmem_Arb_data_mem_wp0_source1:** Arbiter contender group bandwidth for base_dmem_Arb_data_mem_wp0_source1
15	0h RW	**arb_cont_base_dmem_Arb_data_mem_wp0_source0:** Arbiter contender group bandwidth for base_dmem_Arb_data_mem_wp0_source0
14	0h RW	**arb_period_base_dmem_Arb_data_mem_wp0:** Arbiter period for base_dmem_Arb_data_mem_wp0
13	0h RW	**prefetch_enable_flag:** Prefetch enable flag for base_config_mem_icache
12	0h RW	**invalidate_cache_flag:** Invalidate cache flag for base_config_mem_icache
11	0h RW	**sleeping_irq_mask_flag:** Sleeping IRQ mask flag
10	0h RW	**ready_irq_mask_flag:** Ready IRQ mask flag
9	0h RW	**broken_irq_mask_flag:** Broken IRQ mask flag
8	0h RW	**irq_clear_flag:** IRQ clear flag
7	1h RO	**stalling_flag:** Stalling flag. Set to one when not executing an instruction.
6	0h RO	**sleeping_flag:** Sleeping flag

Bit Range	Default & Access	Description
5	1h RO	**ready_flag:** Ready flag. Set to one when not executing a program.
4	0h RO	**broken_flag:** Broken flag
3	0h RW	**run_flag:** Run flag
2	0h RW	**break_flag:** Break flag
1	0h WO	**start_flag:** Start flag
0	0h WO	**reset_flag:** Reset flag

3.7.99 reg_isp_base_address_type (isp_base_address)—Offset 20004h

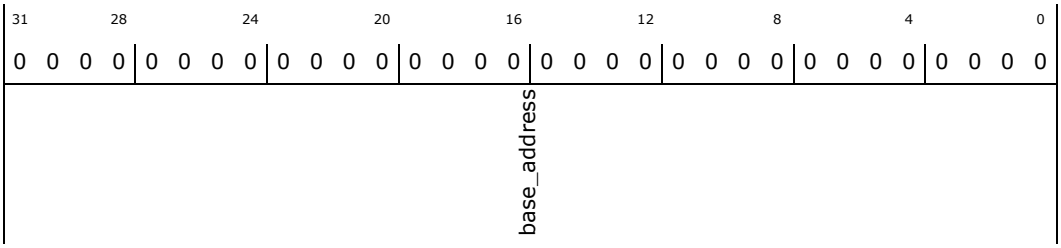
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_base_address: [ISPMMADR] + 20004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**base_address:** Start address

3.7.100 reg_isp_unused_2_type (isp_unused_2)—Offset 20008h

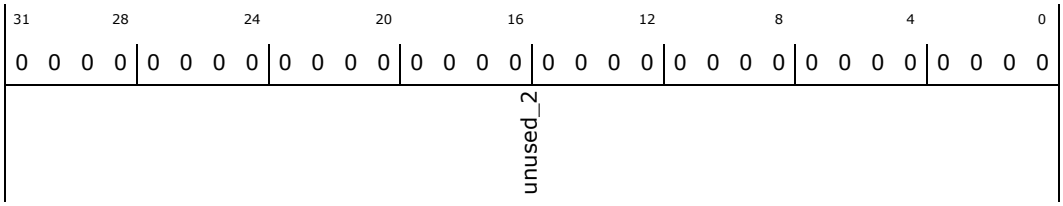
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_unused_2: [ISPMMADR] + 20008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**unused_2:** Unused

3.7.101 reg_isp_base_addr_seg_0_MI_base_config_mem_master_type (isp_base_addr_seg_0_MI_base_config_mem_master)—Offset 20010h

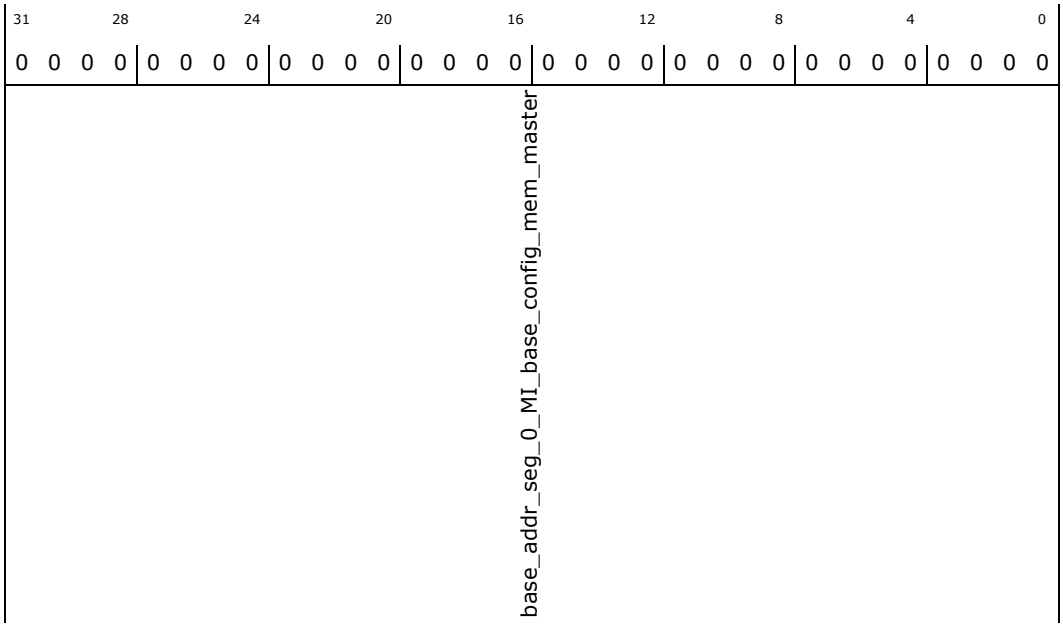
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_base_addr_seg_0_MI_base_config_mem_master: [ISPMMADR] + 20010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**base_addr_seg_0_MI_base_config_mem_master:** Base address for segment 0 of master interface base_config_mem_master

3.7.102 reg_isp_unused_5_type (isp_unused_5)—Offset 20014h

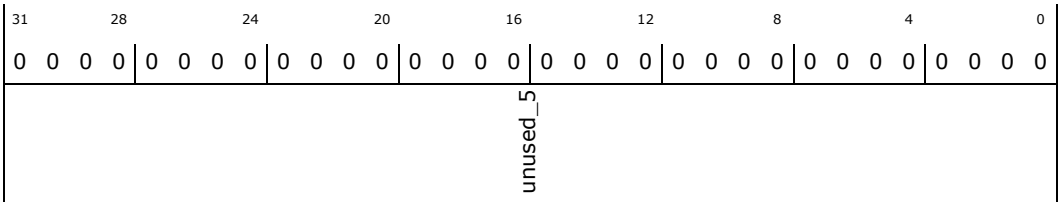
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_unused_5: [ISPMMADR] + 20014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**unused_5:** Unused

3.7.103 reg_isp_debug_pc_type (isp_debug_pc)—Offset 2001Ch

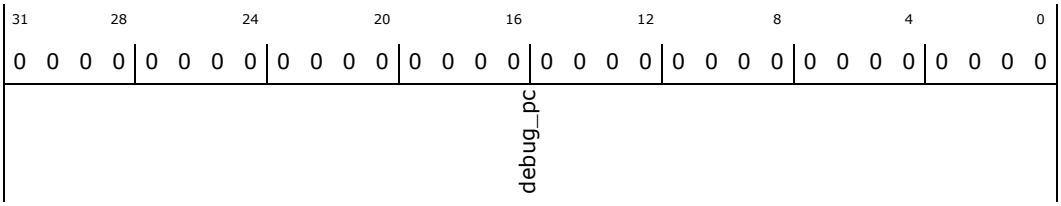
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_debug_pc: [ISPMMADR] + 2001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**debug_pc:** Debug program counter

3.7.104 reg_isp_stall_stat_base_config_mem_iam_op0_type (isp_stall_stat_base_config_mem_iam_op0)—Offset 20020h

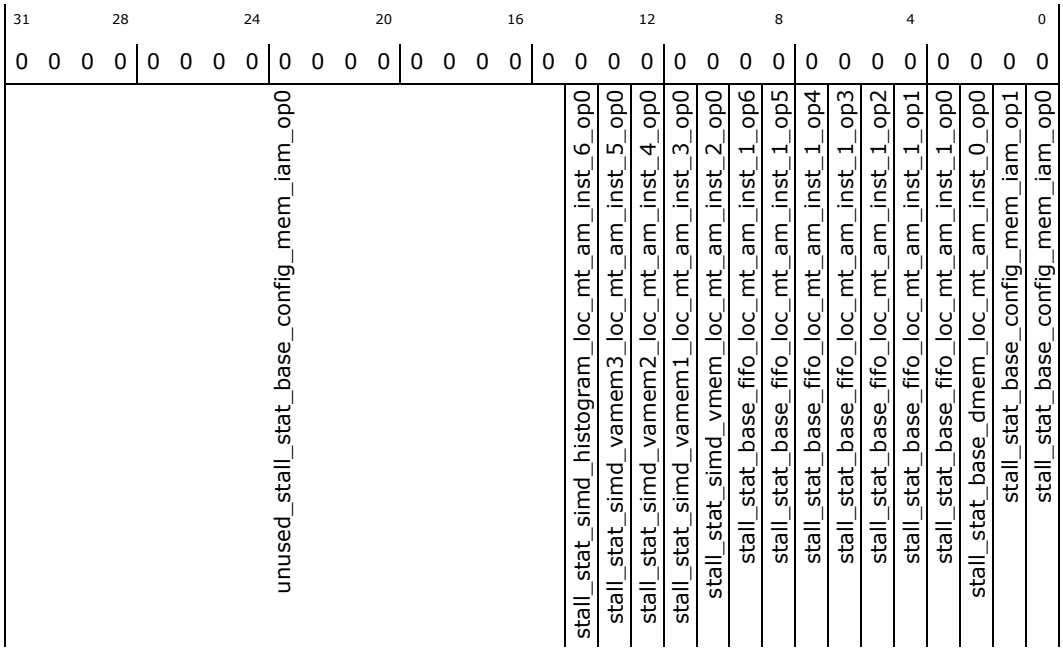
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_stall_stat_base_config_mem_iam_op0: [ISPMMADR] + 20020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RW	**unused_stall_stat_base_config_mem_iam_op0:** Unused
14	0h RO	**stall_stat_simd_histogram_loc_mt_am_inst_6_op0:** Stalling flag for msink simd_histogram_loc_mt_am_inst_6_op0
13	0h RO	**stall_stat_simd_vamem3_loc_mt_am_inst_5_op0:** Stalling flag for msink simd_vamem3_loc_mt_am_inst_5_op0
12	0h RO	**stall_stat_simd_vamem2_loc_mt_am_inst_4_op0:** Stalling flag for msink simd_vamem2_loc_mt_am_inst_4_op0
11	0h RO	**stall_stat_simd_vamem1_loc_mt_am_inst_3_op0:** Stalling flag for msink simd_vamem1_loc_mt_am_inst_3_op0
10	0h RO	**stall_stat_simd_vmem_loc_mt_am_inst_2_op0:** Stalling flag for msink simd_vmem_loc_mt_am_inst_2_op0
9	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op6:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op6

Bit Range	Default & Access	Description
8	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op5:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op5
7	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op4:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op4
6	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op3:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op3
5	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op2:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op2
4	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op1:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op1
3	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op0:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op0
2	0h RO	**stall_stat_base_dmem_loc_mt_am_inst_0_op0:** Stalling flag for msink base_dmem_loc_mt_am_inst_0_op0
1	0h RO	**stall_stat_base_config_mem_iam_op1:** Stalling flag for msink base_config_mem_iam_op1
0	0h RO	**stall_stat_base_config_mem_iam_op0:** Stalling flag for msink base_config_mem_iam_op0

3.7.105 reg_isp_unused_9_type (isp_unused_9)—Offset 20024h

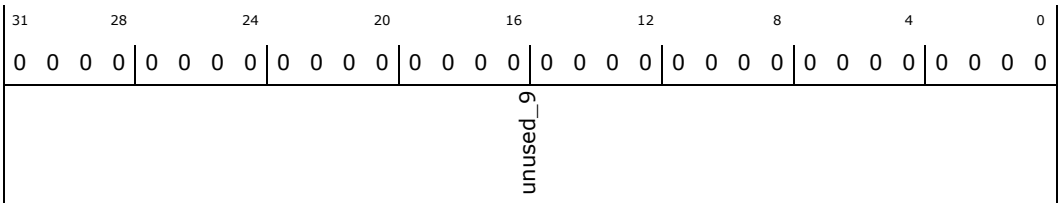
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_unused_9: [ISPMMADR] + 20024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**unused_9:** Unused

3.7.106 reg_isp_pmem_slave_access_type (isp_pmem_slave_access)—Offset 20028h

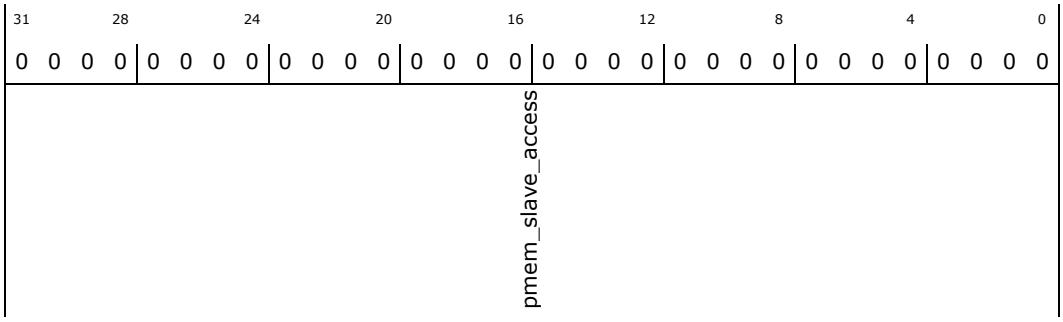
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_pmem_slave_access: [ISPMMADR] + 20028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**pmem_slave_access:** Pmem slave access flag

3.7.107 reg_ifmt_ift_prim_IF_sw_rst_type (ifmt_ift_prim_IF_sw_rst)—Offset 30000h

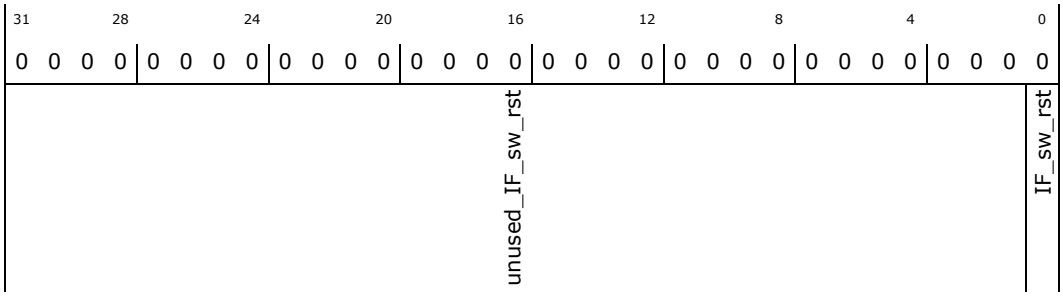
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_sw_rst: [ISPMMADR] + 30000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_sw_rst:** Unused
0	0h RW	**IF_sw_rst:** Software Reset

3.7.108 reg_ifmt_ift_prim_IF_start_line_type (ifmt_ift_prim_IF_start_line)—Offset 30004h

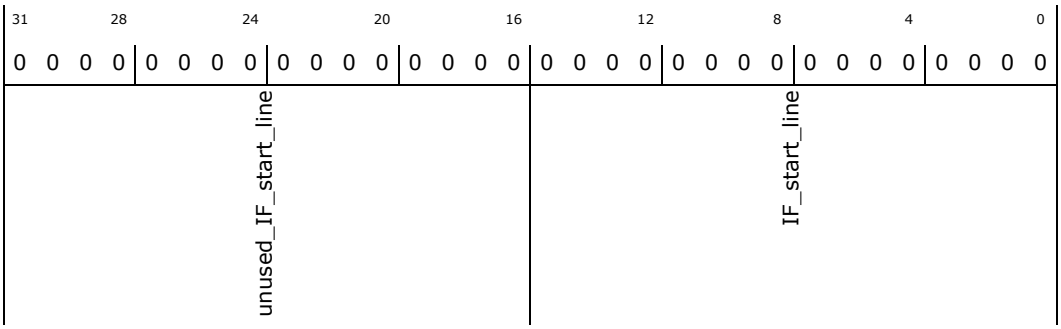
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_start_line: [ISPMMADR] + 30004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_line:** Unused
15:0	0h RW	**IF_start_line:** Start line: number of line to skip before passing the 1st line

3.7.109 reg_ifmt_ift_prim_IF_start_column_type (ifmt_ift_prim_IF_start_column)—Offset 30008h

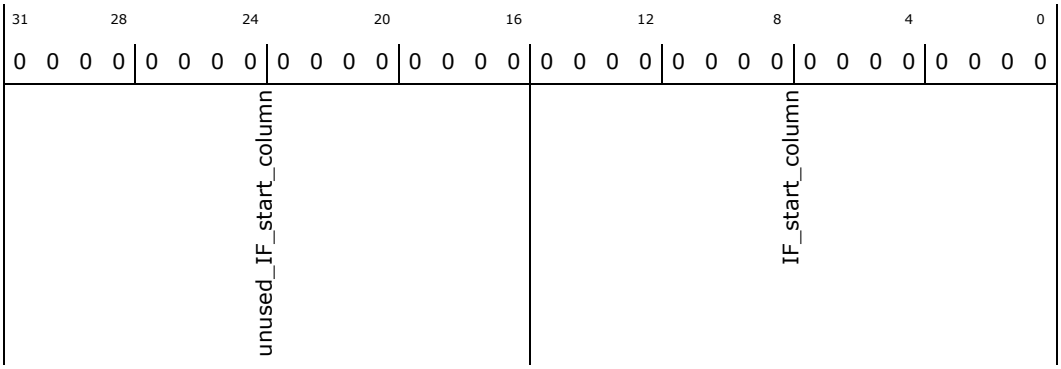
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_start_column: [ISPMMADR] + 30008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_column:** Unused
15:0	0h RW	**IF_start_column:** Start column: number pixel component to skip before passing the 1st of a line

3.7.110 reg_ifmt_ift_prim_IF_Cropped_height_type (ifmt_ift_prim_IF_Cropped_height)—Offset 3000Ch

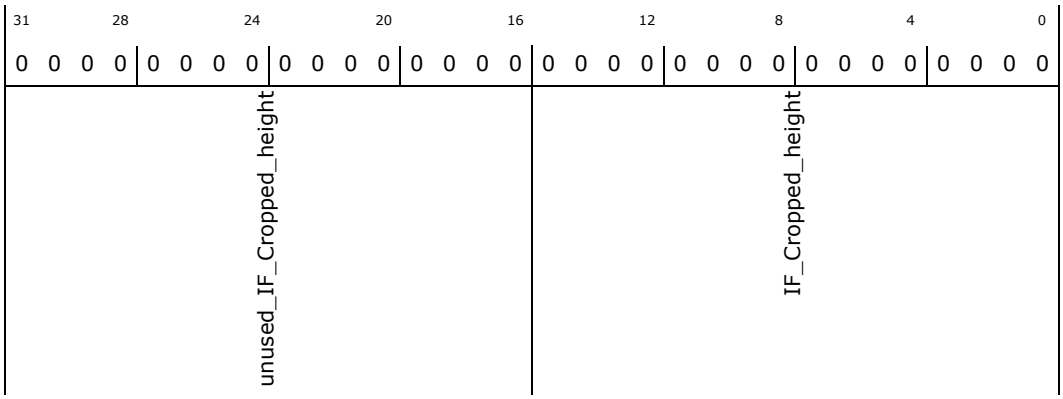
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Cropped_height: [ISPMMADR] + 3000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_height:** Unused
15:0	0h RW	**IF_Cropped_height:** Cropped height: number of lines of the cropped image

3.7.111 reg_ifmt_ift_prim_IF_Cropped_width_type (ifmt_ift_prim_IF_Cropped_width)—Offset 30010h

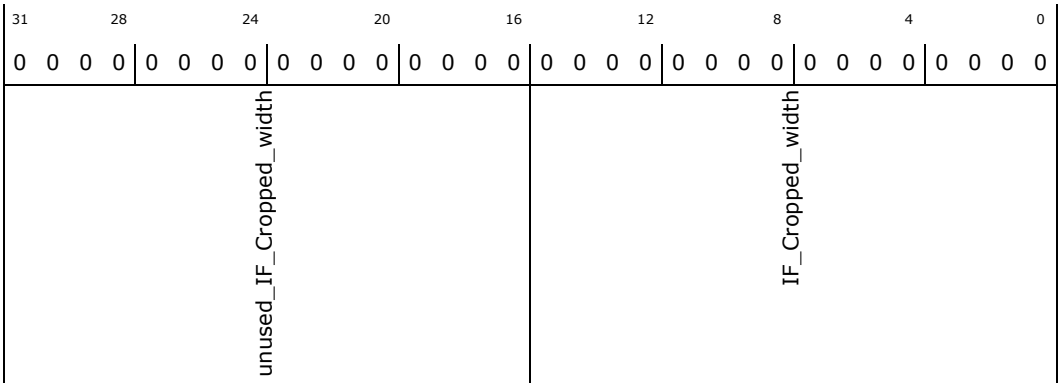
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Cropped_width: [ISPMMADR] + 30010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_width:** Unused
15:0	0h RW	**IF_Cropped_width:** Cropped width: number of pixel component of the cropped image

3.7.112 reg_ifmt_ift_prim_IF_Vert_Decim_type (ifmt_ift_prim_IF_Vert_Decim)—Offset 30014h

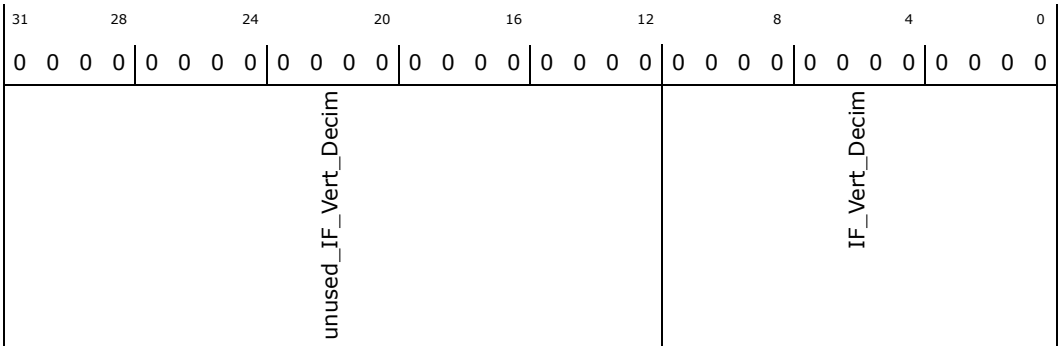
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Vert_Decim: [ISPMMADR] + 30014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Vert_Decim:** Unused
11:0	0h RW	**IF_Vert_Decim:** Vertical decimation factor

3.7.113 reg_ifmt_ift_prim_IF_Horiz_Decim_type (ifmt_ift_prim_IF_Horiz_Decim)—Offset 30018h

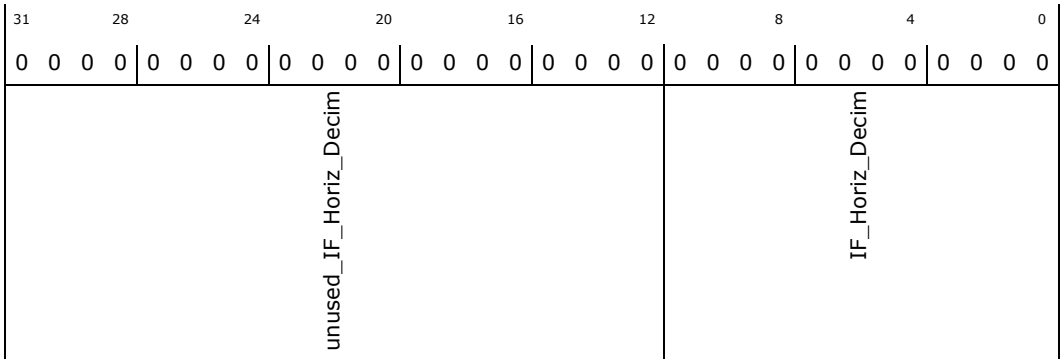
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Horiz_Decim: [ISPMMADR] + 30018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Horiz_Decim:** Unused
11:0	0h RW	**IF_Horiz_Decim:** Horizontal decimation factor

3.7.114 reg_ifmt_ift_prim_IF_Horiz_Deinter_type (ifmt_ift_prim_IF_Horiz_Deinter)—Offset 3001Ch

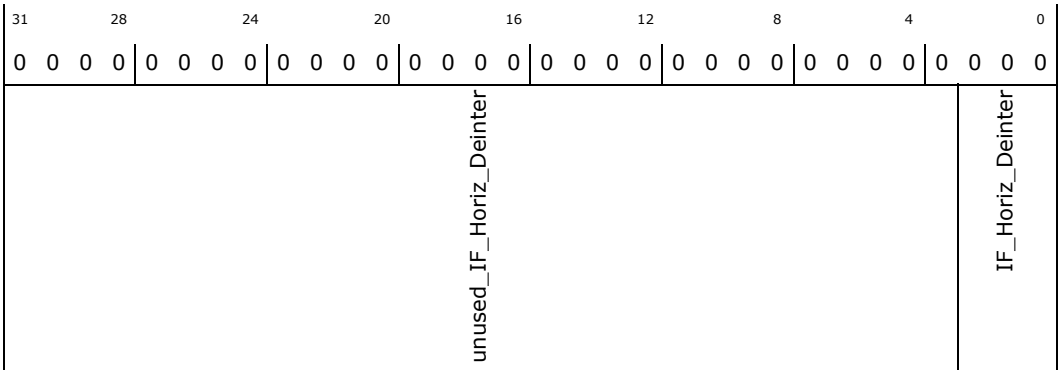
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Horiz_Deinter: [ISPMMADR] + 3001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Horiz_Deinter:** Unused
2:0	0h RW	**IF_Horiz_Deinter:** Horizontal deinterleaving factor

3.7.115 reg_ifmt_ift_prim_IF_Left_Pad_type (ifmt_ift_prim_IF_Left_Pad)—Offset 30020h

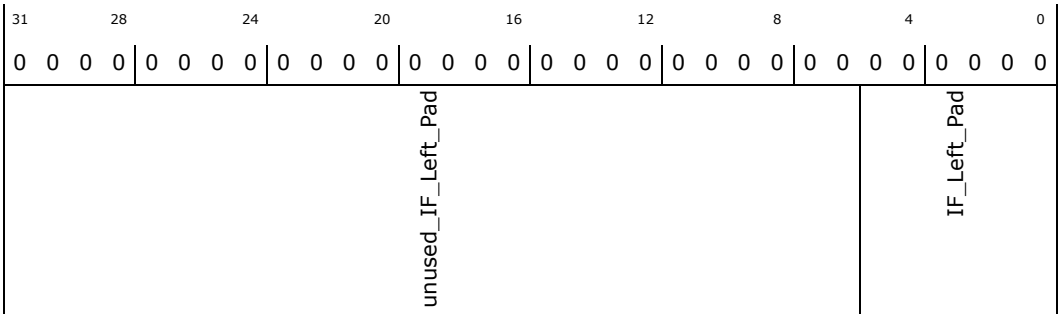
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Left_Pad: [ISPMMADR] + 30020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_Left_Pad:** Unused
5:0	0h RW	**IF_Left_Pad:** Left padding: pizel component to be padded at the beginning of each line

3.7.116 reg_ifmt_ift_prim_IF_EOF_Offset_type (ifmt_ift_prim_IF_EOF_Offset)—Offset 30024h

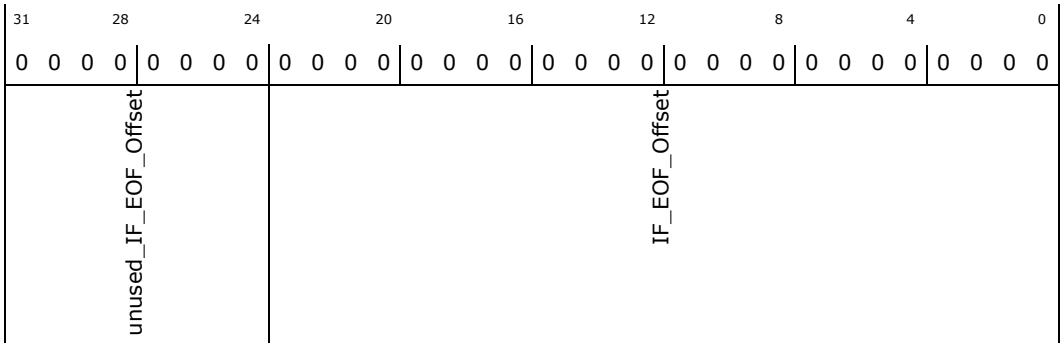
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_EOF_Offset: [ISPMMADR] + 30024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_EOF_Offset:** Unused
23:0	0h RW	**IF_EOF_Offset:** End of line offset in bytes: number of bytes to add at the address at the end of a line

3.7.117 reg_ifmt_ift_prim_IF_Start_addr_type (ifmt_ift_prim_IF_Start_addr)—Offset 30028h

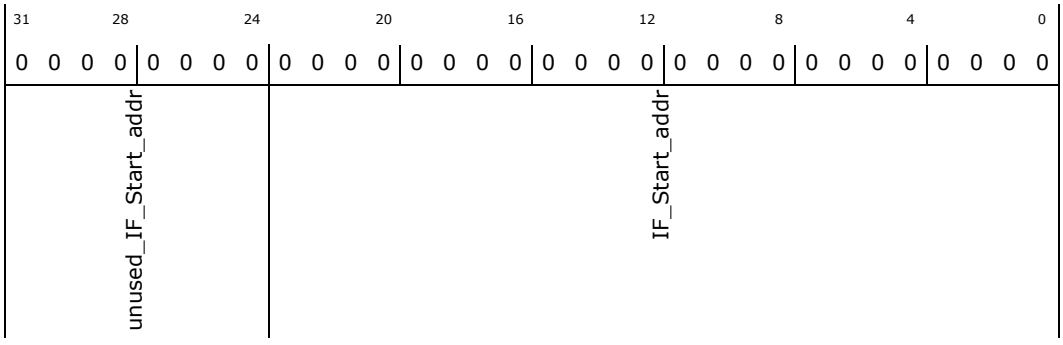
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Start_addr: [ISPMMADR] + 30028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_Start_addr:** Unused
23:0	0h RW	**IF_Start_addr:** Start address in bytes: memory buffer start address

3.7.118 reg_ifmt_ift_prim_IF_End_addr_type (ifmt_ift_prim_IF_End_addr)—Offset 3002Ch

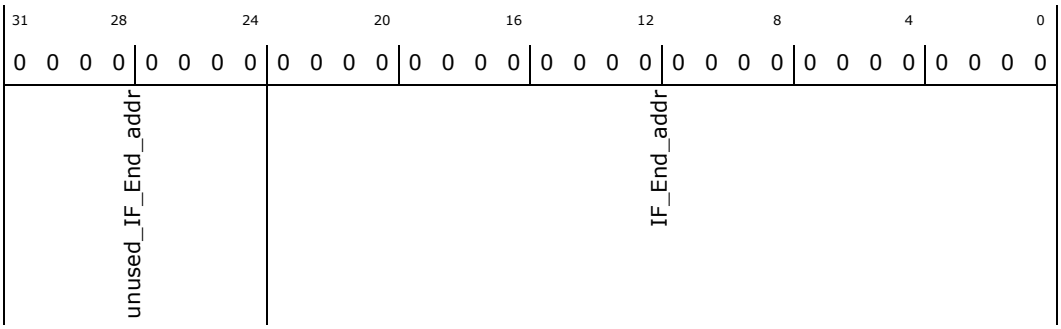
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_End_addr: [ISPMMADR] + 3002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_End_addr:** Unused
23:0	0h RW	**IF_End_addr:** End address in bytes: memory buffer end address

3.7.119 reg_ifmt_ift_prim_IF_incr_type (ifmt_ift_prim_IF_incr)—Offset 30030h

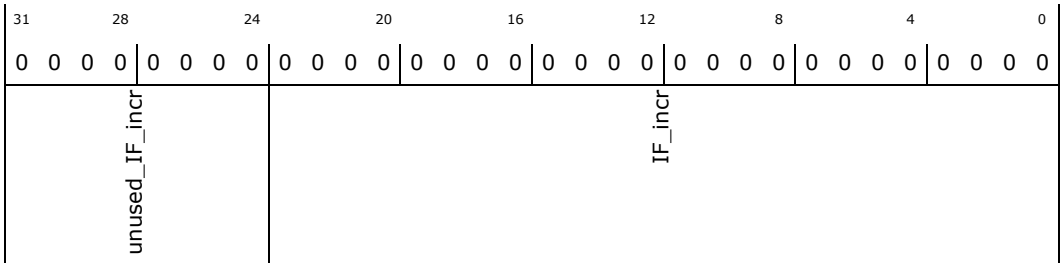
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_incr: [ISPMMADR] + 30030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_incr:** Unused
23:0	0h RW	**IF_incr:** Word increment in memory word: word increment value after writing each word

3.7.120 reg_ifmt_ift_prim_IF_YUV_420_format_type (ifmt_ift_prim_IF_YUV_420_format)—Offset 30034h

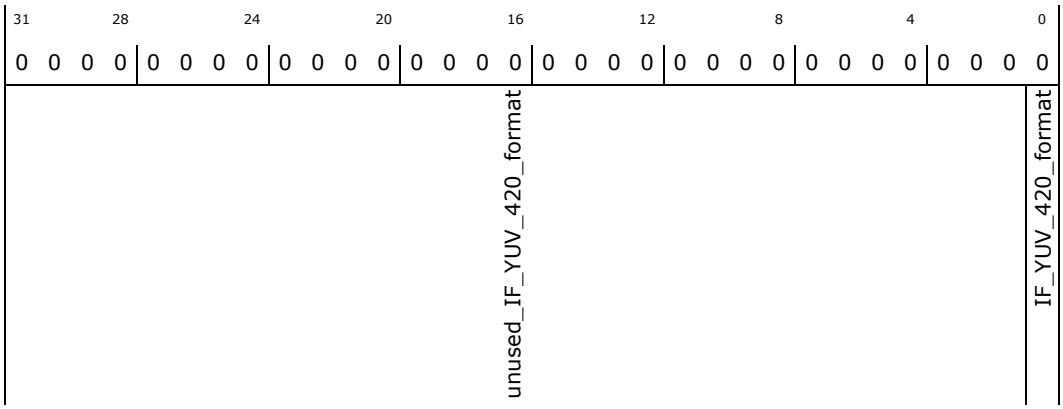
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_YUV_420_format: [ISPMMADR] + 30034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_YUV_420_format:** Unused
0	0h RW	**IF_YUV_420_format:** YUV 420 format: set to work on legacy format YUV420

3.7.121 reg_ifmt_ift_prim_IF_Vsynch_active_low_type (ifmt_ift_prim_IF_Vsynch_active_low)—Offset 30038h

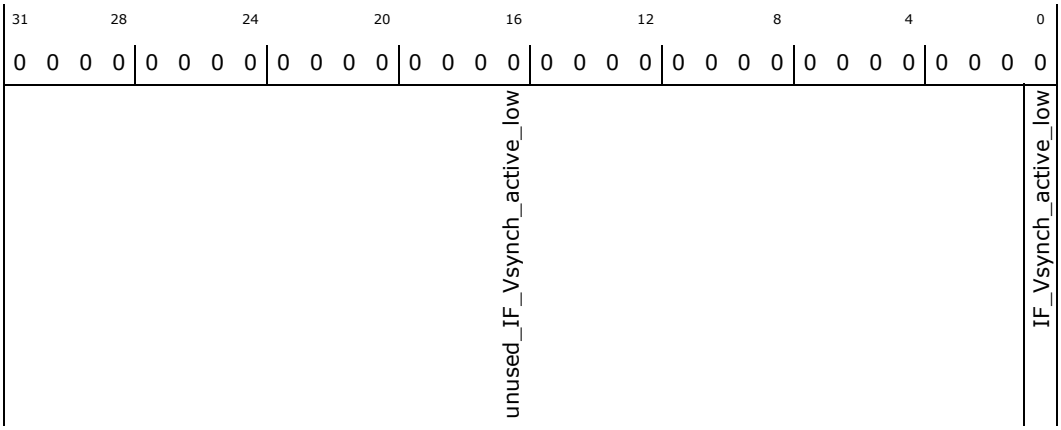
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Vsynch_active_low: [ISPMMADR] + 30038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Vsynch_active_low:** Unused
0	0h RW	**IF_Vsynch_active_low:** Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

3.7.122 reg_ifmt_ift_prim_IF_Hsynch_active_low_type (ifmt_ift_prim_IF_Hsynch_active_low)—Offset 3003Ch

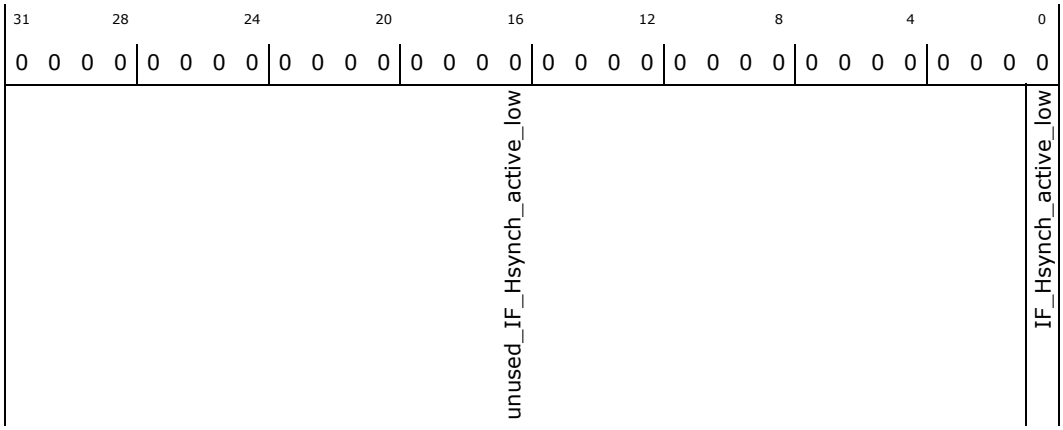
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Hsynch_active_low: [ISPMMADR] + 3003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Hsynch_active_low:** Unused
0	0h RW	**IF_Hsynch_active_low:** Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

3.7.123 reg_ifmt_ift_prim_IF_ReEnable_type (ifmt_ift_prim_IF_ReEnable)—Offset 30040h

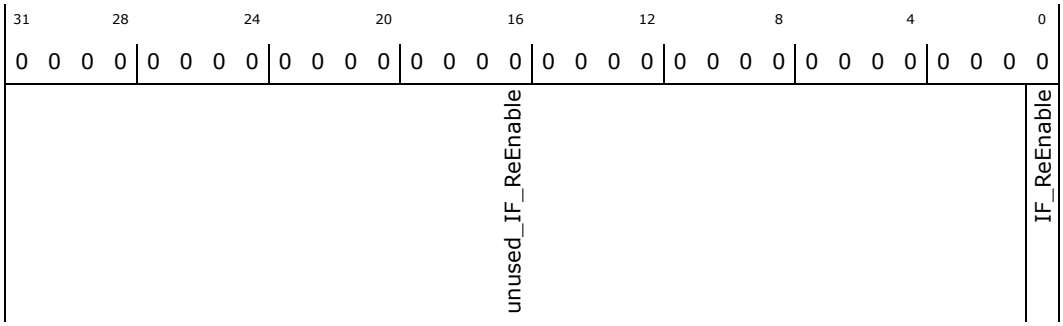
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_ReEnable: [ISPMMADR] + 30040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_ReEnable:** Unused
0	0h RW	**IF_ReEnable:** Re-enable status update: set to 1 to re-enable status update after an error situation

3.7.124 reg_ifmt_ift_prim_IF_block_input_type (ifmt_ift_prim_IF_block_input)—Offset 30044h

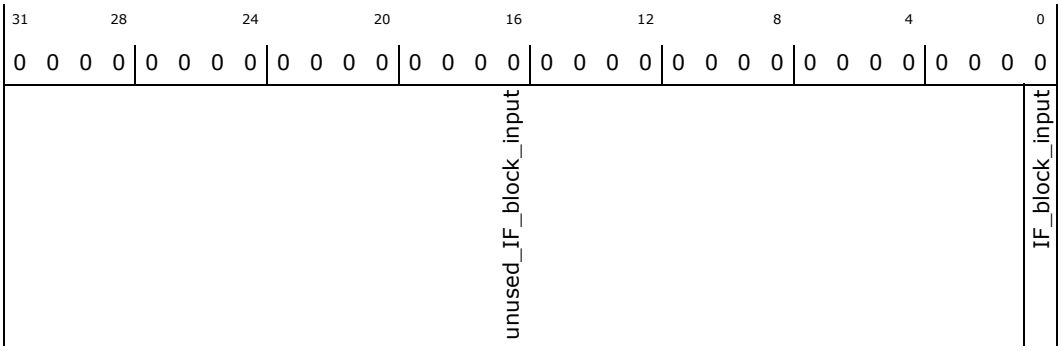
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_block_input: [ISPMMADR] + 30044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_block_input:** Unused
0	0h RW	**IF_block_input:** Block input when no req: set to 1 to block data streaming input when no request is received

3.7.125 reg_ifmt_ift_prim_IF_Vert_Deinter_type (ifmt_ift_prim_IF_Vert_Deinter)—Offset 30048h

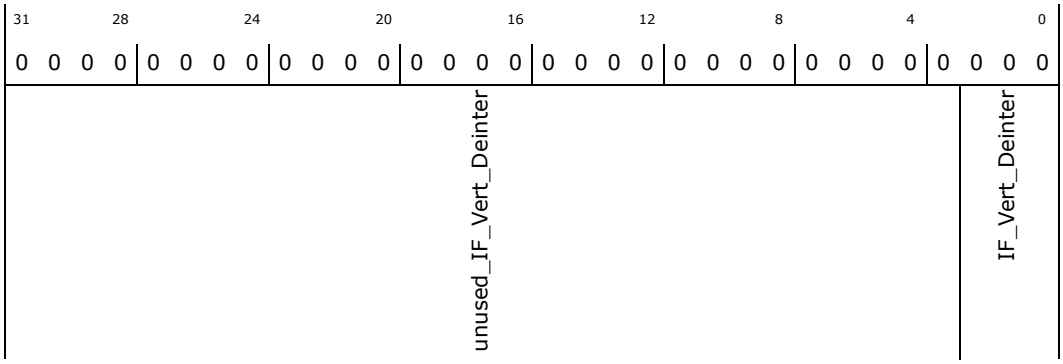
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Vert_Deinter: [ISPMMADR] + 30048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Vert_Deinter:** Unused
2:0	0h RW	**IF_Vert_Deinter:** Vertical deinterleaving factor

3.7.126 reg_ifmt_ift_prim_IF_FSM_Sync_status_type (ifmt_ift_prim_IF_FSM_Sync_status)—Offset 30100h

FSM Sync status

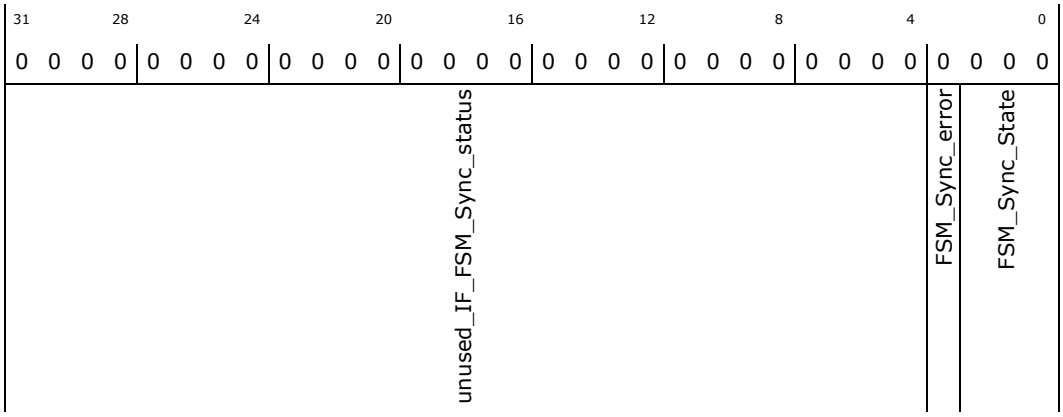
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Sync_status: [ISPMMADR] + 30100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Sync_status:** Unused

Bit Range	Default & Access	Description
3	0h RO	**FSM_Sync_error:** Error flag: when set in combination with: Idle state an unknown command has been received; Req. Lines state an unexpected vsynch or eof has been received; Req. Vectors state an unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0h RO	**FSM_Sync_State:** FSM State: State: 0)Idle -- 1)Req Frame -- 2)Req. Lines -- 3)Req. Vectors -- 4)Send Acknowledge

3.7.127 reg_ifmt_ift_prim_FSM_Sync_counter_type (ifmt_ift_prim_FSM_Sync_counter)—Offset 30104h

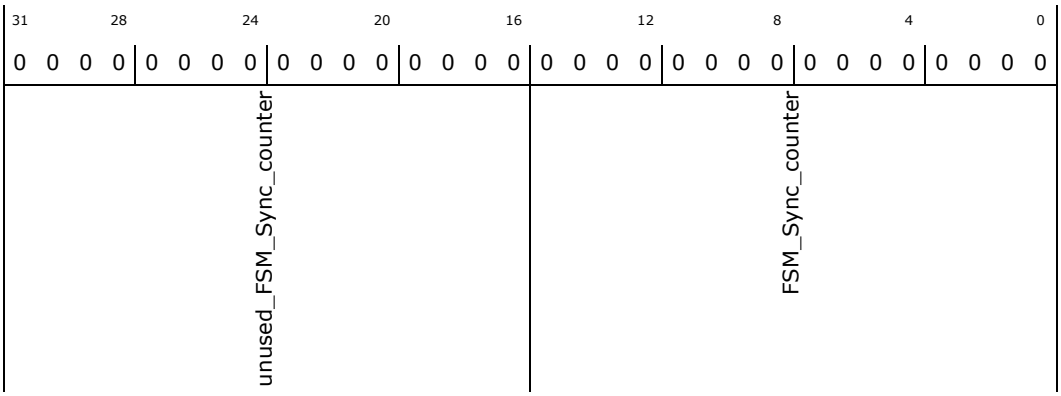
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Sync_counter: [ISPMMADR] + 30104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Sync_counter:** Unused
15:0	0h RO	**FSM_Sync_counter:** FSM Sync counter: counts the pixel components of the request being served (starting from value 1)

3.7.128 reg_ifmt_ift_prim_FSM_Crop_status_type (ifmt_ift_prim_FSM_Crop_status)—Offset 30108h

FSM Crop status

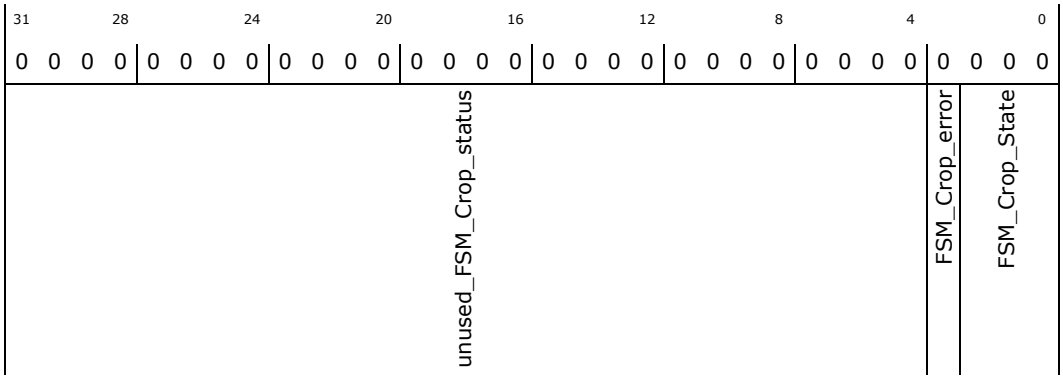
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Crop_status: [ISPMMADR] + 30108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_FSM_Crop_status:** Unused
3	0h RO	**FSM_Crop_error:** Error flag: when set in combination with: Crop Line state unexpected vsynch or eof has been received; Req. Lines state unexpected vsynch or eof has been received; Req. Vectors state unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0h RO	**FSM_Crop_State:** FSM State: State: 0)Idle -- 1)Wait Line -- 2)Crop Line -- 3)Crop Pixel -- 4)Pass pixel -- 5) Pass Line

3.7.129 reg_ifmt_ift_prim_FSM_Crop_line_counter_type (ifmt_ift_prim_FSM_Crop_line_counter)—Offset 3010Ch

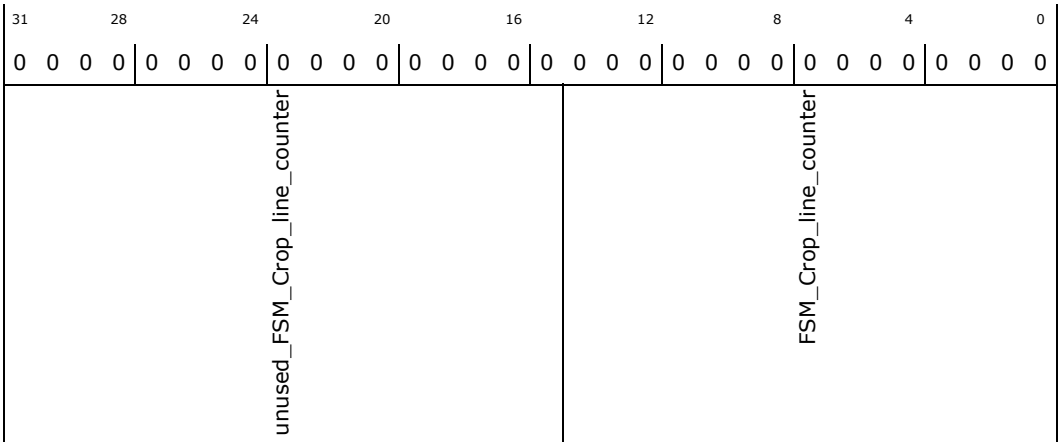
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Crop_line_counter: [ISPMMADR] + 3010Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RW	**unused_FSM_Crop_line_counter:** Unused
14:0	0h RO	**FSM_Crop_line_counter:** FSM Crop line counter

3.7.130 reg_ifmt_ift_prim_FSM_Crop_pixel_counter_type (ifmt_ift_prim_FSM_Crop_pixel_counter)—Offset 30110h

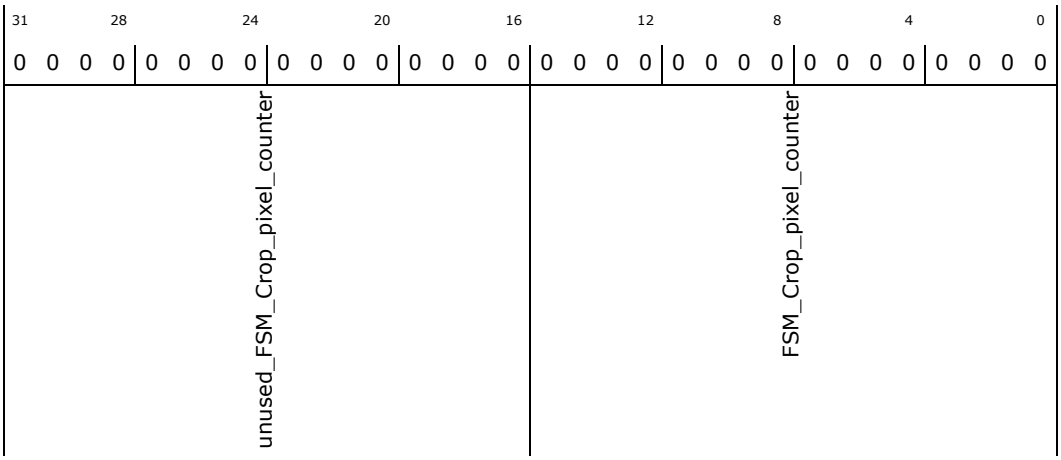
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Crop_pixel_counter: [ISPMMADR] + 30110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Crop_pixel_counter:** Unused
15:0	0h RO	**FSM_Crop_pixel_counter:** FSM Crop pixel component counter

3.7.131 reg_ifmt_ift_prim_FSM_Deinterl_idx_buffer_type (ifmt_ift_prim_FSM_Deinterl_idx_buffer)—Offset 30114h

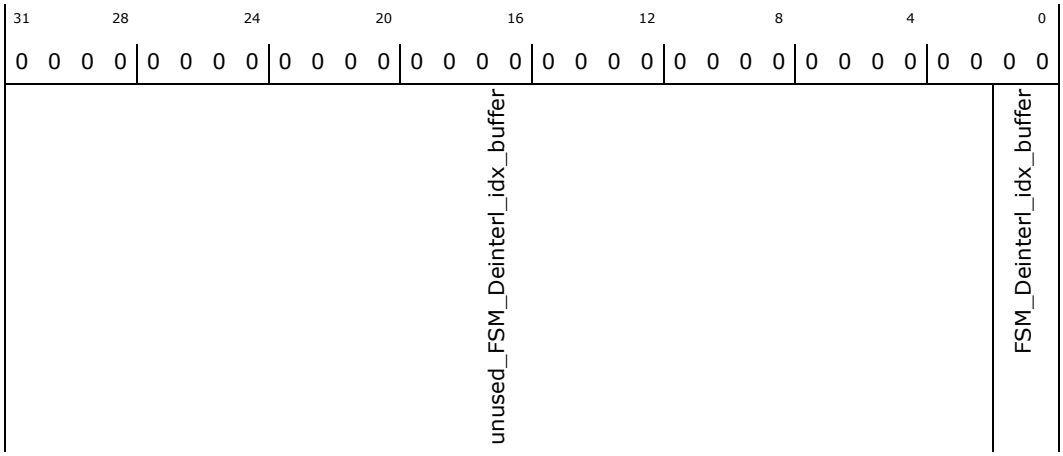
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Deinterl_idx_buffer: [ISPMMADR] + 30114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Deinterl_idx_buffer:** Unused
1:0	0h RO	**FSM_Deinterl_idx_buffer:** FSM Deinterleaving idx buffer

3.7.132 reg_ifmt_ift_prim_FSM_Horiz_Decim_cnt_type (ifmt_ift_prim_FSM_Horiz_Decim_cnt)—Offset 30118h

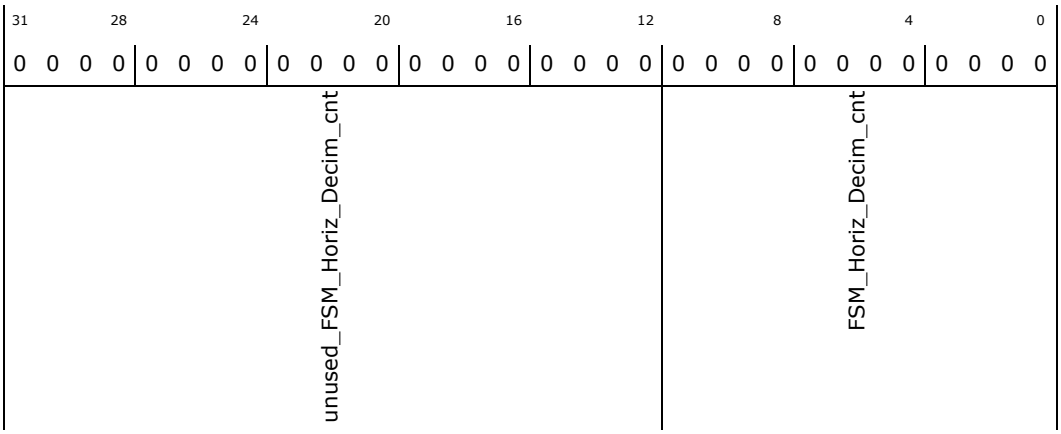
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Horiz_Decim_cnt: [ISPMMADR] + 30118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Horiz_Decim_cnt:** Unused
11:0	0h RO	**FSM_Horiz_Decim_cnt:** FSM Horizontal Decimation counter

3.7.133 reg_ifmt_ift_prim_FSM_Vertic_Decim_cnt_type (ifmt_ift_prim_FSM_Vertic_Decim_cnt)—Offset 3011Ch

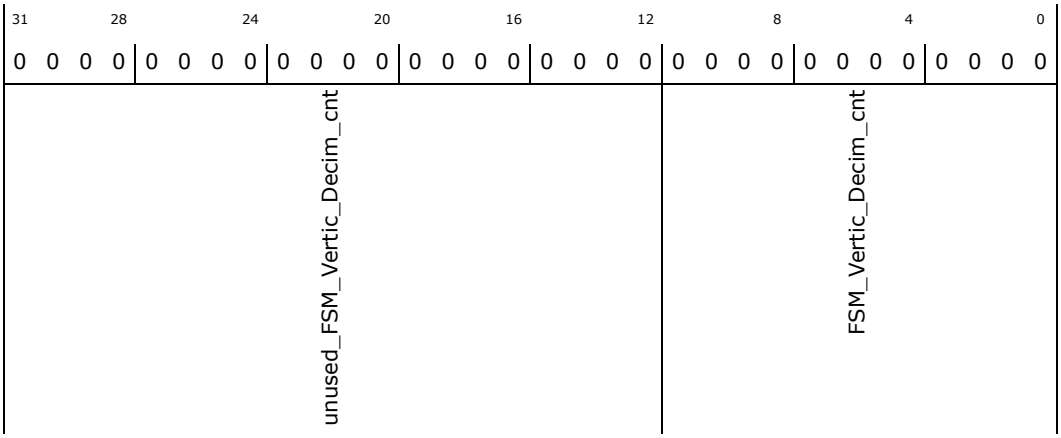
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Vertic_Decim_cnt: [ISPMMADR] + 3011Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Vertic_Decim_cnt:** Unused
11:0	0h RO	**FSM_Vertic_Decim_cnt:** FSM Vertical decimation counter

3.7.134 reg_ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt)—Offset 30120h

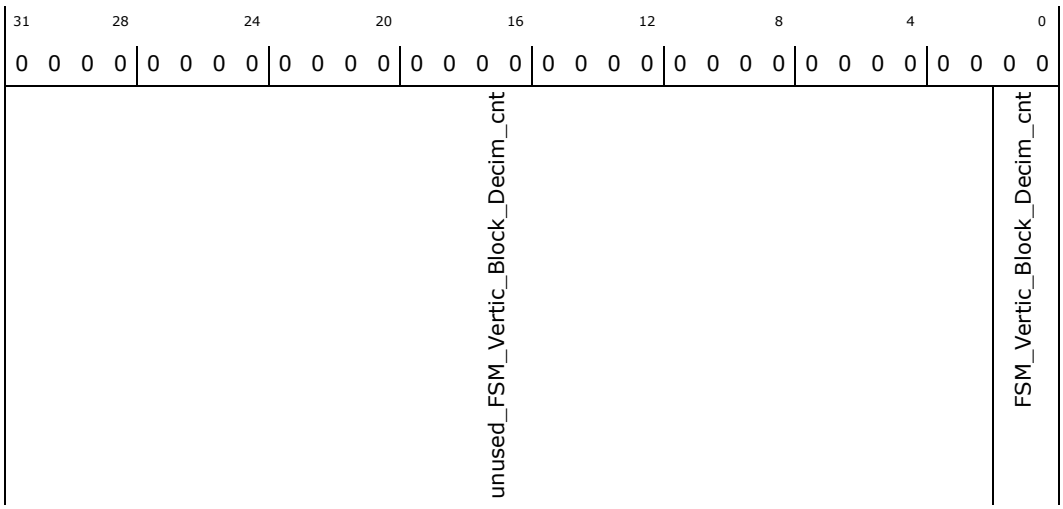
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt: [ISPMMADR] + 30120h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Vertic_Block_Decim_cnt:** Unused
1:0	0h RO	**FSM_Vertic_Block_Decim_cnt:** FSM Vertical block decimation counter

3.7.135 reg_ifmt_ift_prim_IF_FSM_Padding_status_type (ifmt_ift_prim_IF_FSM_Padding_status)—Offset 30124h

FSM Padding status

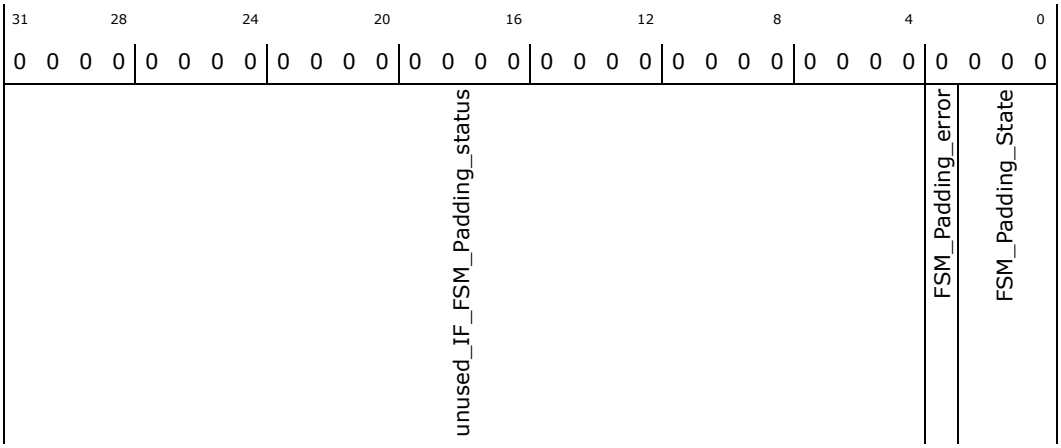
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Padding_status: [ISPMMADR] + 30124h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Padding_status:** Unused
3	0h RO	**FSM_Padding_error:** Error flag: when set in combination with: Left Padding state an unexpected vsynch or hsync has been received; Write state an unexpected vsynch or hsync has been received; Right padding state unexpected vsynch has been received; Send EOL state an unexpected vsynch has been received; another state an illegal state transition has occurred.
2:0	0h RO	**FSM_Padding_State:** FSM State: State: 0)Idle -- 1)Left Padding -- 2)Write -- 3)Right padding -- 4)Sending EOL

3.7.136 reg_ifmt_ift_prim_IF_FSM_Padding_elem_idx_type (ifmt_ift_prim_IF_FSM_Padding_elem_idx)—Offset 30128h

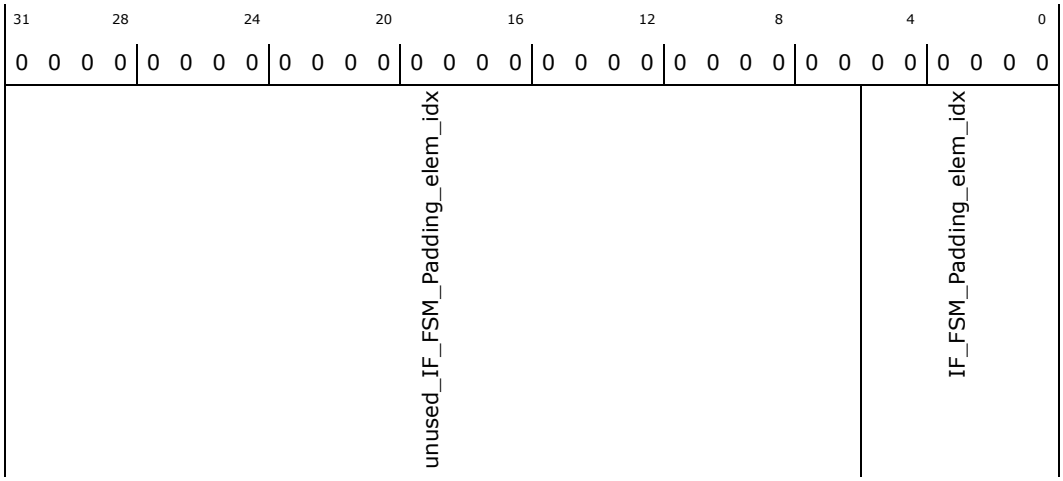
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Padding_elem_idx: [ISPMMADR] + 30128h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_FSM_Padding_elem_idx:** Unused
5:0	0h RO	**IF_FSM_Padding_elem_idx:** FSM Padding element index counter

3.7.137 reg_ifmt_ift_prim_IF_FSM_Vec_Sup_type (ifmt_ift_prim_IF_FSM_Vec_Sup)—Offset 3012Ch

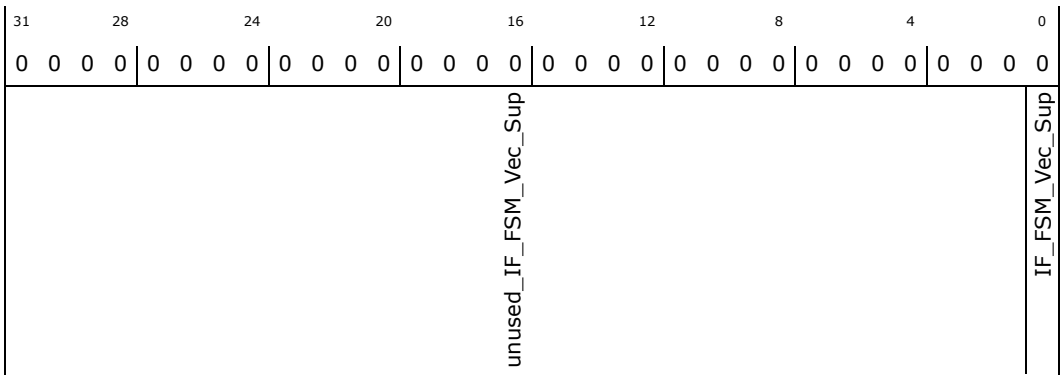
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Vec_Sup: [ISPMMADR] + 3012Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup:** Unused
0	0h RO	**IF_FSM_Vec_Sup:** FSM Vector support error state: if set the FSM Vector support is in error state

3.7.138 reg_ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full)—Offset 30130h

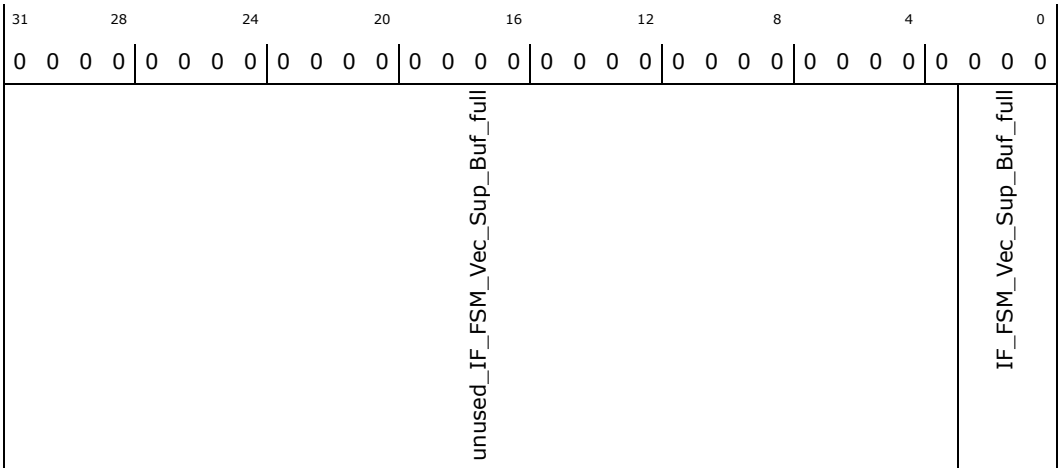
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full: [ISPMMADR] + 30130h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_FSM_Vec_Sup_Buf_full:** Unused
2:0	0h RO	**IF_FSM_Vec_Sup_Buf_full:** FSM Vector support buf full: one-hot encoding flag signaling that the correspondent buffer is full

3.7.139 reg_ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept)—Offset 30134h

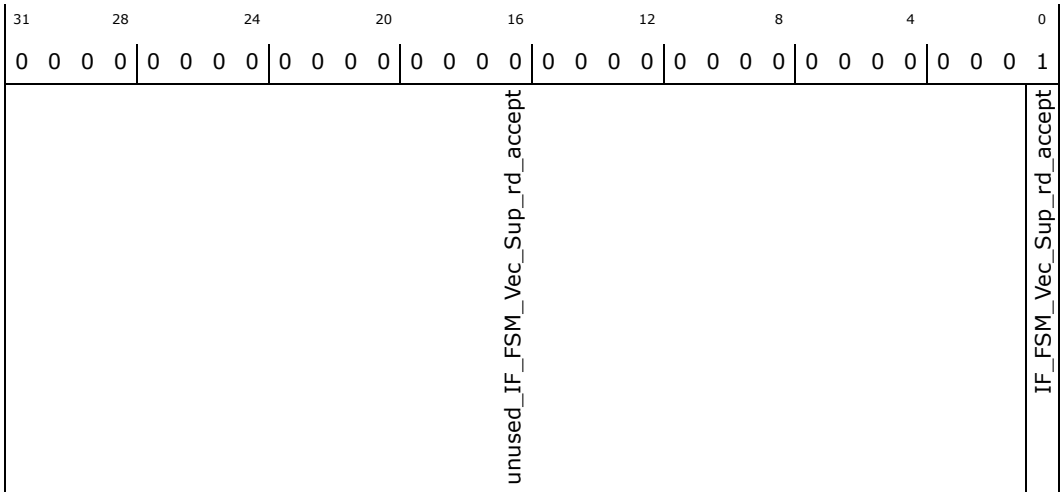
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept: [ISPMMADR] + 30134h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup_rd_accept:** Unused
0	1h RO	**IF_FSM_Vec_Sup_rd_accept:** FSM Vector Support fifo rd accept flag

3.7.140 reg_ifmt_ift_prim_IF_Pixel_Fifo_status_type (ifmt_ift_prim_IF_Pixel_Fifo_status)—Offset 30138h

Pixel Fifo status

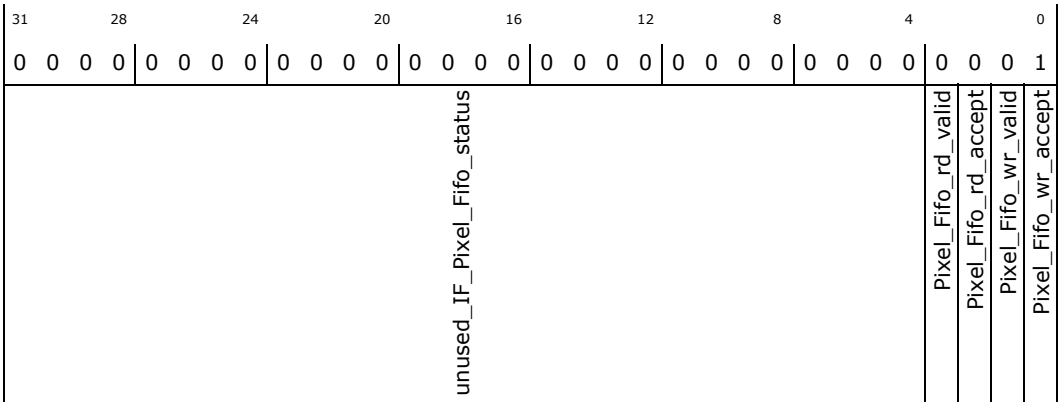
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Pixel_Fifo_status: [ISPMMADR] + 30138h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_Pixel_Fifo_status:** Unused
3	0h RO	**Pixel_Fifo_rd_valid:** Fifo has an element to be read
2	0h RO	**Pixel_Fifo_rd_accept:** IF accepts Pixel(s)
1	0h RO	**Pixel_Fifo_wr_valid:** There is an element to write into the Fifo
0	1h RO	**Pixel_Fifo_wr_accept:** Fifo is not full(1), Fifo is Full(0)

3.7.141 reg_ifmt_ift_prim_b_IF_sw_rst_type (ifmt_ift_prim_b_IF_sw_rst)—Offset 30200h

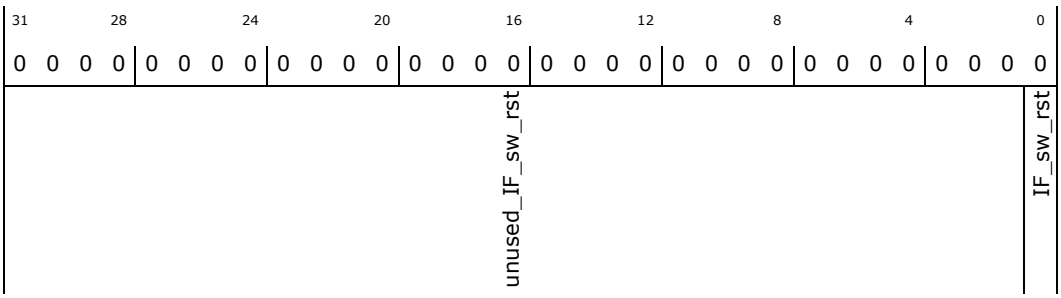
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_sw_rst: [ISPMMADR] + 30200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_sw_rst:** Unused
0	0h RW	**IF_sw_rst:** Software Reset

3.7.142 reg_ifmt_ift_prim_b_IF_start_line_type (ifmt_ift_prim_b_IF_start_line)—Offset 30204h

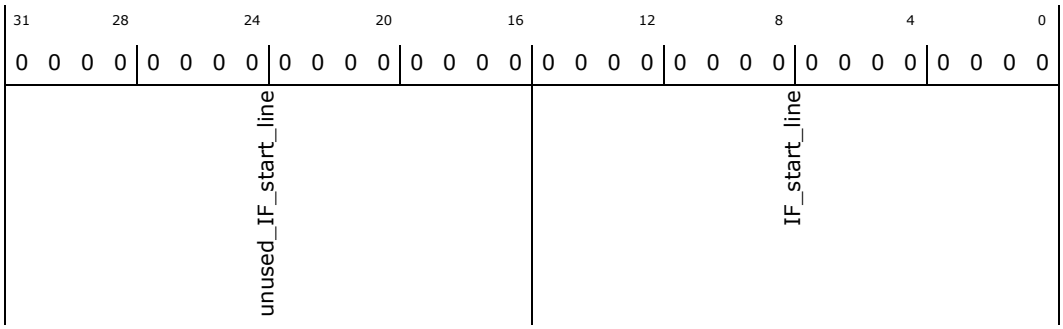
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_start_line: [ISPMMADR] + 30204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_line:** Unused
15:0	0h RW	**IF_start_line:** Start line: number of line to skip before passing the 1st line

3.7.143 reg_ifmt_ift_prim_b_IF_start_column_type (ifmt_ift_prim_b_IF_start_column)—Offset 30208h

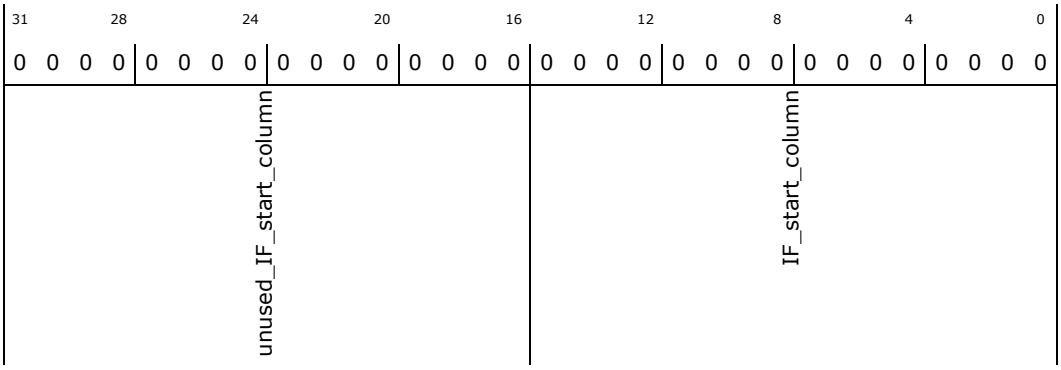
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_start_column: [ISPMMADR] + 30208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_column:** Unused
15:0	0h RW	**IF_start_column:** Start column: number pixel component to skip before passing the 1st of a line

3.7.144 reg_ifmt_ift_prim_b_IF_Cropped_height_type (ifmt_ift_prim_b_IF_Cropped_height)—Offset 3020Ch

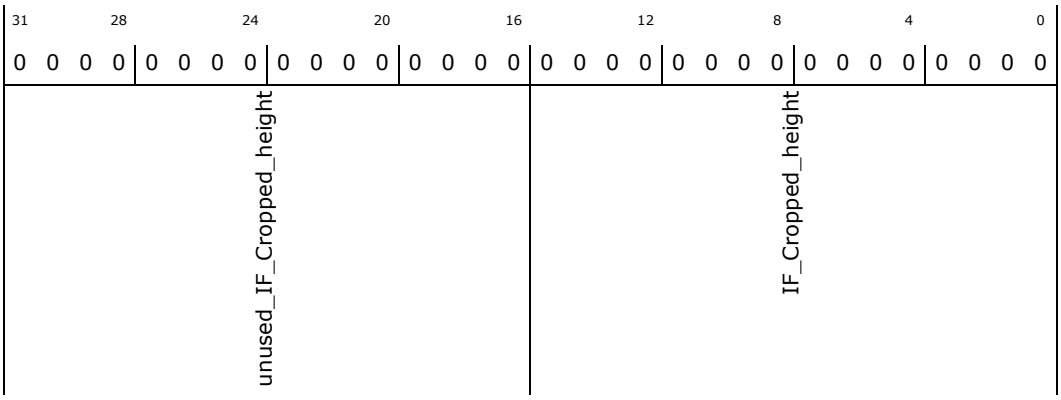
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Cropped_height: [ISPMMADR] + 3020Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_height:** Unused
15:0	0h RW	**IF_Cropped_height:** Cropped height: number of lines of the cropped image

3.7.145 reg_ifmt_ift_prim_b_IF_Cropped_width_type (ifmt_ift_prim_b_IF_Cropped_width)—Offset 30210h

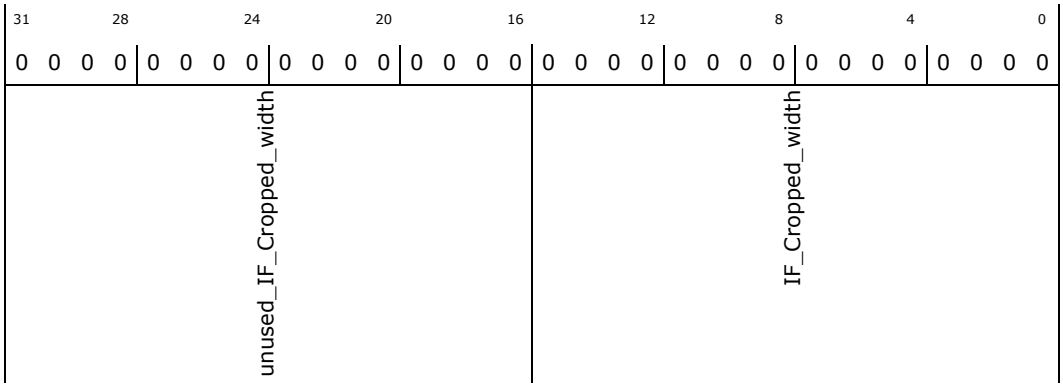
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Cropped_width: [ISPMMADR] + 30210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_width:** Unused
15:0	0h RW	**IF_Cropped_width:** Cropped width: number of pixel component of the cropped image

3.7.146 reg_ifmt_ift_prim_b_IF_Vert_Decim_type (ifmt_ift_prim_b_IF_Vert_Decim)—Offset 30214h

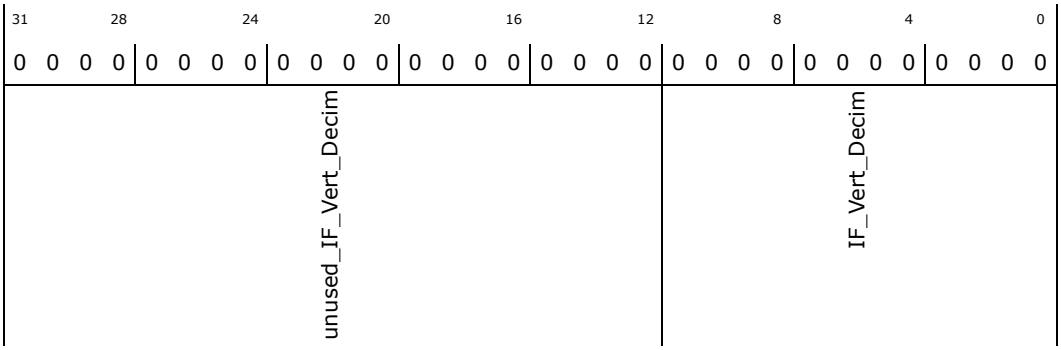
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Vert_Decim: [ISPMMADR] + 30214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Vert_Decim:** Unused
11:0	0h RW	**IF_Vert_Decim:** Vertical decimation factor

3.7.147 reg_ifmt_ift_prim_b_IF_Horiz_Decim_type (ifmt_ift_prim_b_IF_Horiz_Decim)—Offset 30218h

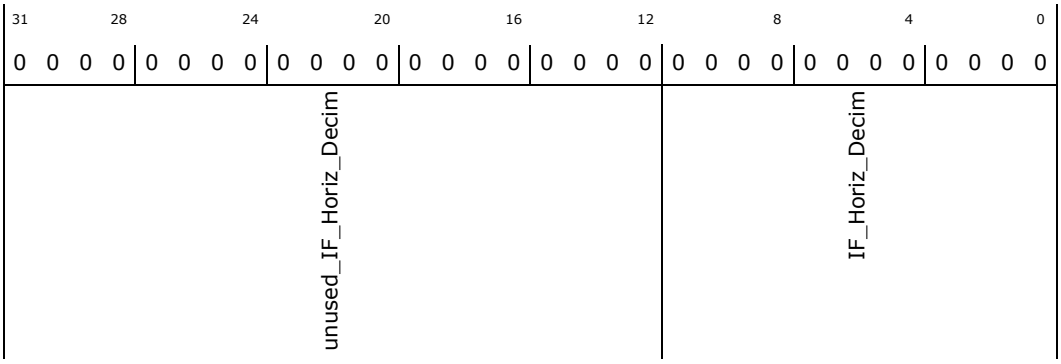
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Horiz_Decim: [ISPMMADR] + 30218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Horiz_Decim:** Unused
11:0	0h RW	**IF_Horiz_Decim:** Horizontal decimation factor

3.7.148 reg_ifmt_ift_prim_b_IF_Horiz_Deinter_type (ifmt_ift_prim_b_IF_Horiz_Deinter)—Offset 3021Ch

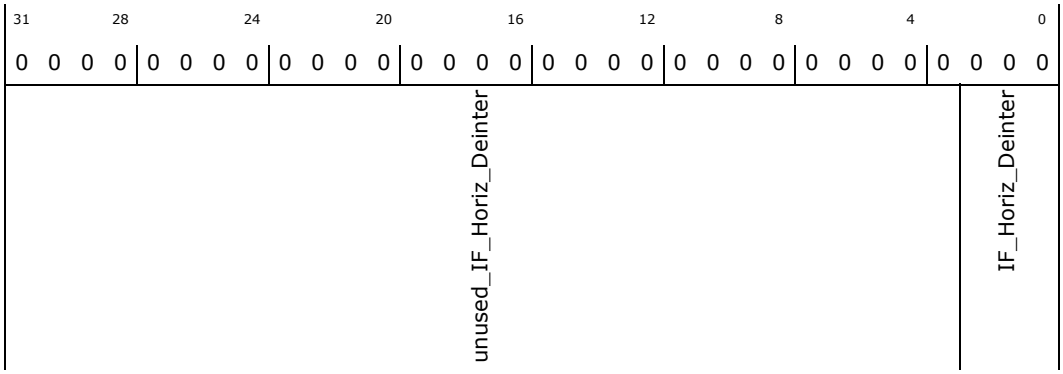
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Horiz_Deinter: [ISPMMADR] + 3021Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Horiz_Deinter:** Unused
2:0	0h RW	**IF_Horiz_Deinter:** Horizontal deinterleaving factor

3.7.149 reg_ifmt_ift_prim_b_IF_Left_Pad_type (ifmt_ift_prim_b_IF_Left_Pad)—Offset 30220h

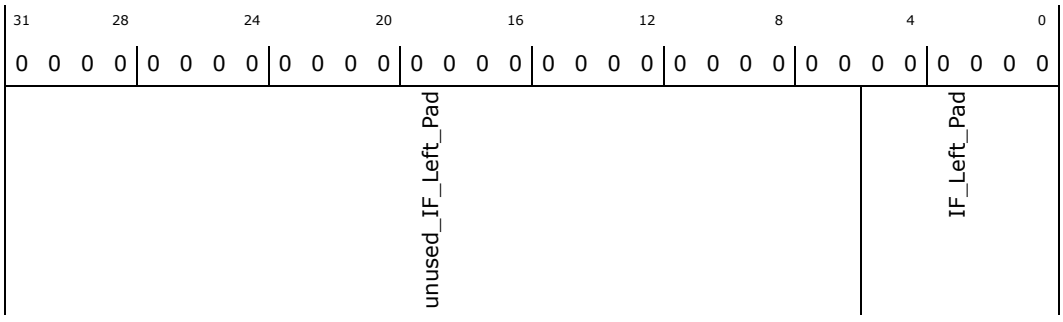
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Left_Pad: [ISPMMADR] + 30220h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_Left_Pad:** Unused
5:0	0h RW	**IF_Left_Pad:** Left padding: pizel component to be padded at the beggining of each line

3.7.150 reg_ifmt_ift_prim_b_IF_EOF_Offset_type (ifmt_ift_prim_b_IF_EOF_Offset)—Offset 30224h

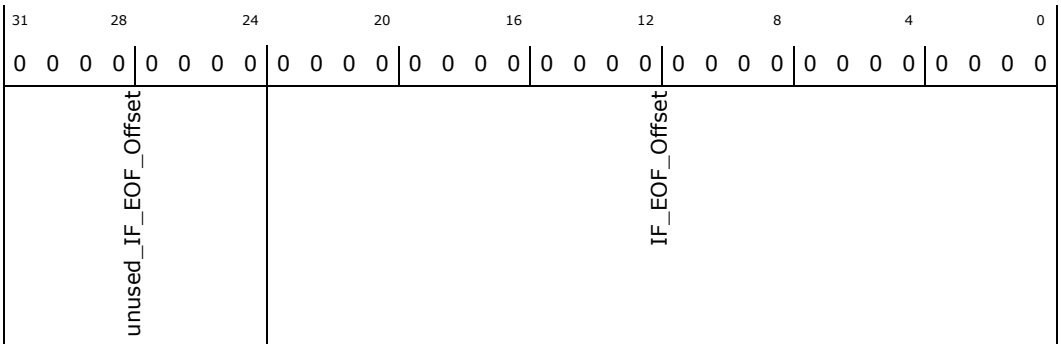
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_EOF_Offset: [ISPMMADR] + 30224h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_EOF_Offset:** Unused
23:0	0h RW	**IF_EOF_Offset:** End of line offset in bytes: number of bytes to add at the address at the end of a line

3.7.151 reg_ifmt_ift_prim_b_IF_Start_addr_type (ifmt_ift_prim_b_IF_Start_addr)—Offset 30228h

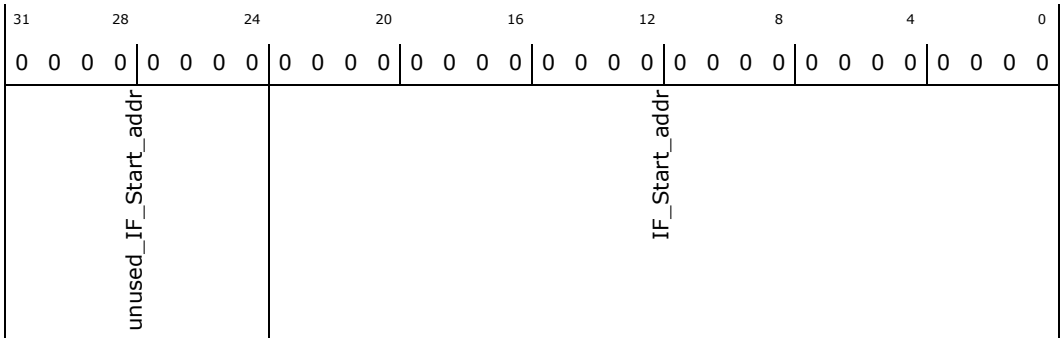
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Start_addr: [ISPMMADR] + 30228h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_Start_addr:** Unused
23:0	0h RW	**IF_Start_addr:** Start address in bytes: memory buffer start address

3.7.152 reg_ifmt_ift_prim_b_IF_End_addr_type (ifmt_ift_prim_b_IF_End_addr)—Offset 3022Ch

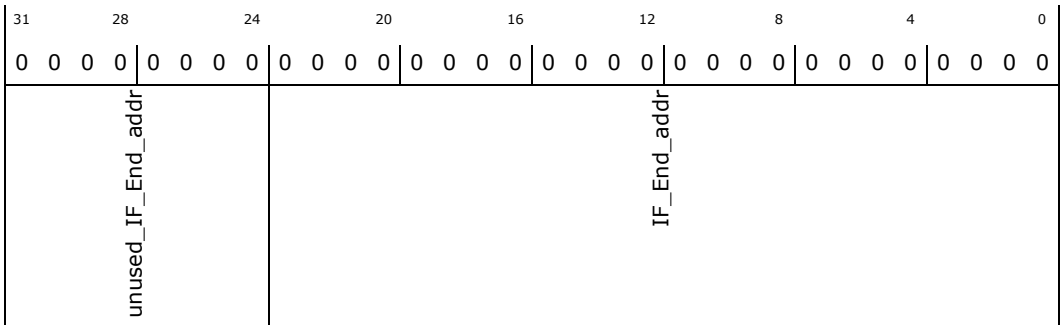
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_End_addr: [ISPMMADR] + 3022Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_End_addr:** Unused
23:0	0h RW	**IF_End_addr:** End address in bytes: memory buffer end address

3.7.153 reg_ifmt_ift_prim_b_IF_incr_type (ifmt_ift_prim_b_IF_incr)—Offset 30230h

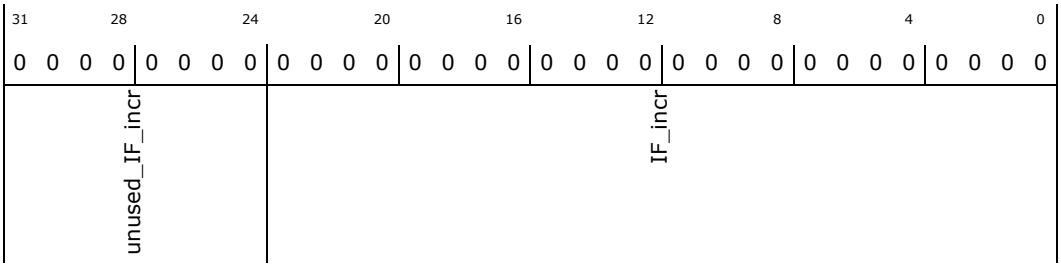
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_incr: [ISPMMADR] + 30230h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_incr:** Unused
23:0	0h RW	**IF_incr:** Word increment in memory word: word increment value after writing each word

3.7.154 reg_ifmt_ift_prim_b_IF_YUV_420_format_type (ifmt_ift_prim_b_IF_YUV_420_format)—Offset 30234h

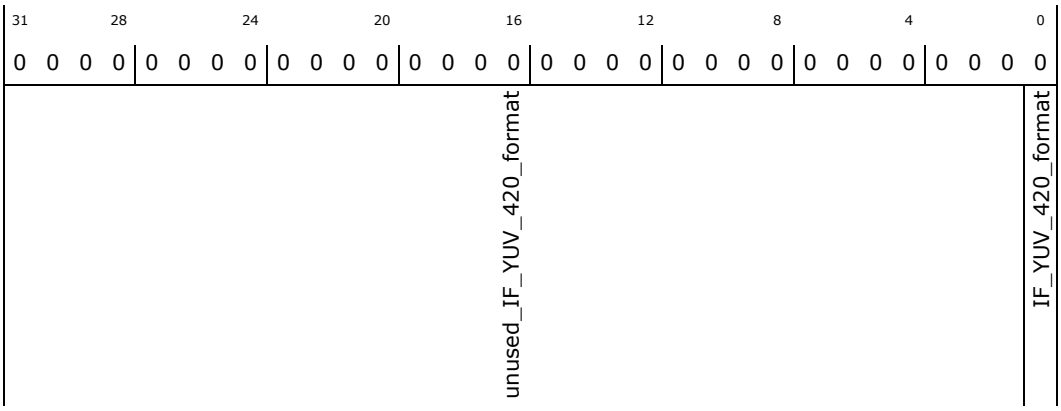
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_YUV_420_format: [ISPMMADR] + 30234h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_YUV_420_format:** Unused
0	0h RW	**IF_YUV_420_format:** YUV 420 format: set to work on legacy format YUV420

3.7.155 reg_ifmt_ift_prim_b_IF_Vsynch_active_low_type (ifmt_ift_prim_b_IF_Vsynch_active_low)—Offset 30238h

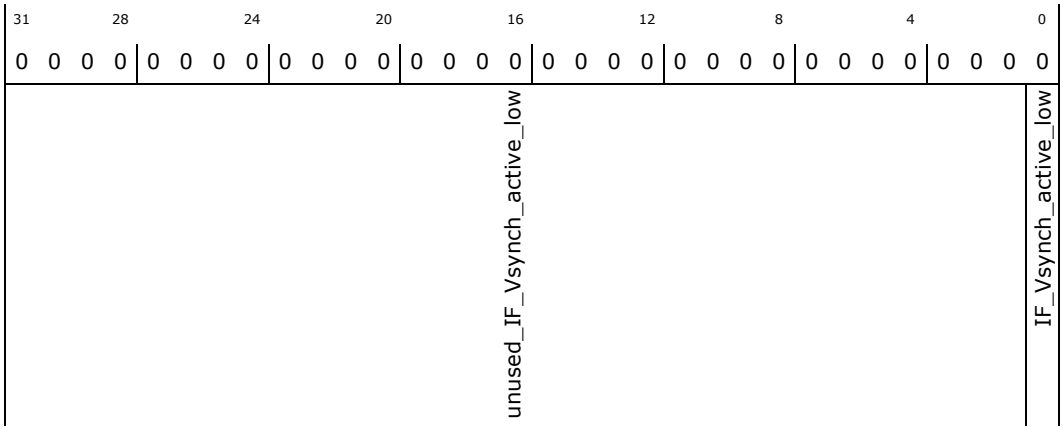
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Vsynch_active_low: [ISPMMADR] + 30238h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Vsynch_active_low:** Unused
0	0h RW	**IF_Vsynch_active_low:** Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

3.7.156 reg_ifmt_ift_prim_b_IF_Hsynch_active_low_type (ifmt_ift_prim_b_IF_Hsynch_active_low)—Offset 3023Ch

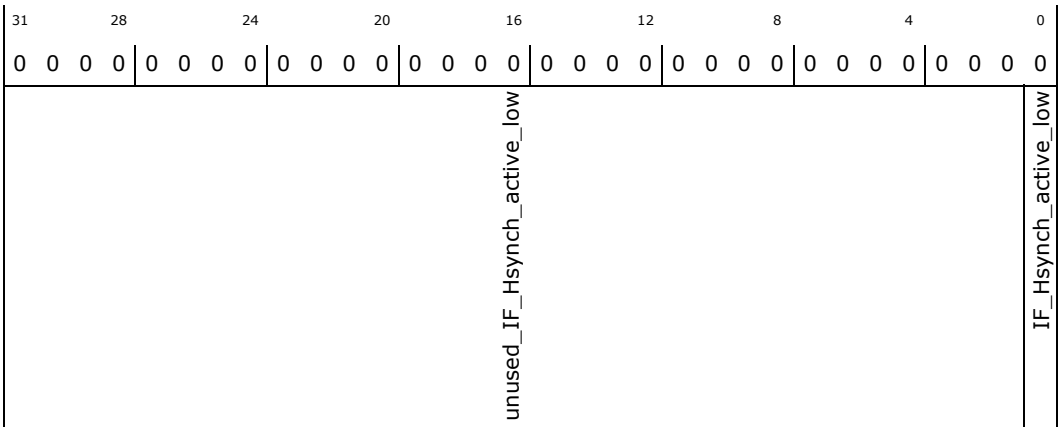
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Hsynch_active_low: [ISPMMADR] + 3023Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Hsynch_active_low:** Unused
0	0h RW	**IF_Hsynch_active_low:** Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

3.7.157 reg_ifmt_ift_prim_b_IF_ReEnable_type (ifmt_ift_prim_b_IF_ReEnable)—Offset 30240h

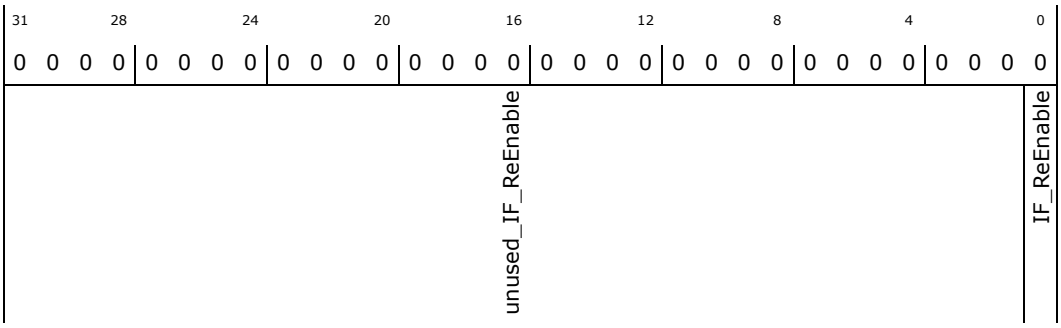
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_ReEnable: [ISPMMADR] + 30240h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_ReEnable:** Unused

Bit Range	Default & Access	Description
0	0h RW	**IF_ReEnable:** Re-enable status update: set to 1 to re-enable status update after an error situation

3.7.158 reg_ifmt_ift_prim_b_IF_block_input_type (ifmt_ift_prim_b_IF_block_input)—Offset 30244h

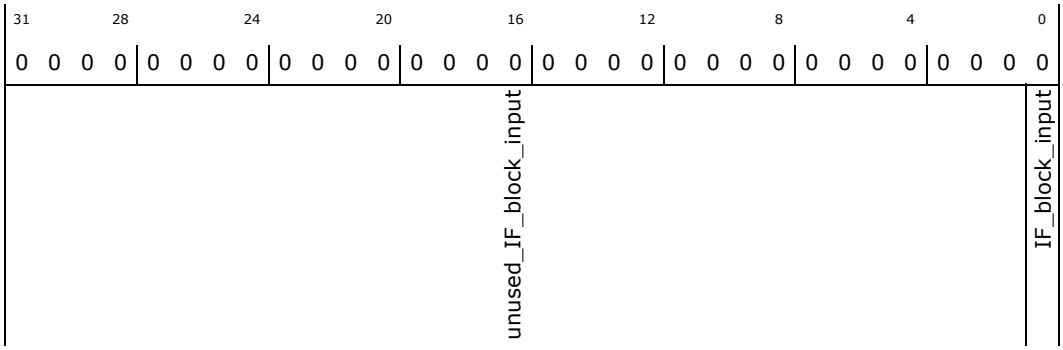
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_block_input: [ISPMMADR] + 30244h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_block_input:** Unused
0	0h RW	**IF_block_input:** Block input when no req: set to 1 to block data streaming input when no request is received

3.7.159 reg_ifmt_ift_prim_b_IF_Vert_Deinter_type (ifmt_ift_prim_b_IF_Vert_Deinter)—Offset 30248h

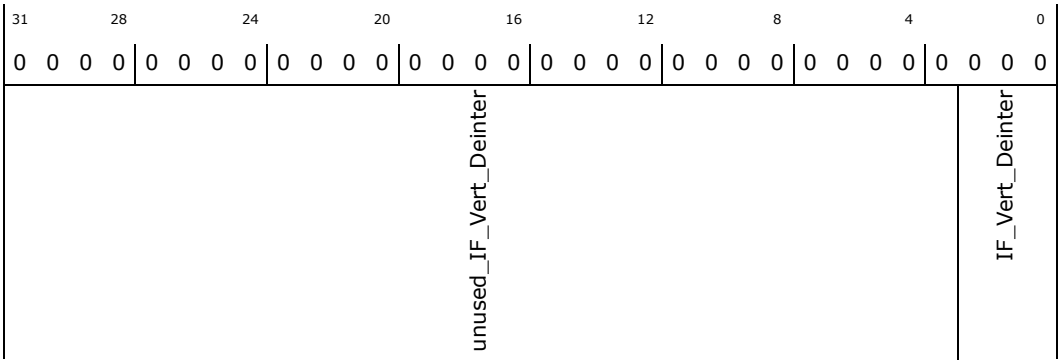
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Vert_Deinter: [ISPMMADR] + 30248h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Vert_Deinter:** Unused
2:0	0h RW	**IF_Vert_Deinter:** Vertical deinterleaving factor

3.7.160 reg_ifmt_ift_prim_b_IF_FSM_Sync_status_type (ifmt_ift_prim_b_IF_FSM_Sync_status)—Offset 30300h

FSM Sync status

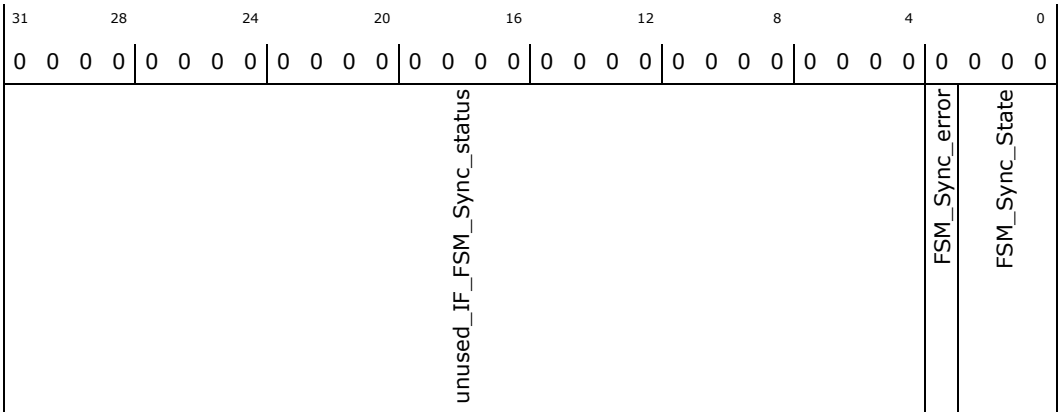
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Sync_status: [ISPMMADR] + 30300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Sync_status:** Unused
3	0h RO	**FSM_Sync_error:** Error flag: when set in combination with: Idle state an unknown command has been received; Req. Lines state an unexpected vsynch or eof has been received; Req. Vectors state an unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0h RO	**FSM_Sync_State:** FSM State: State: 0)Idle -- 1)Req Frame -- 2)Req. Lines -- 3)Req. Vectors -- 4)Send Acknowledge

3.7.161 reg_ifmt_ift_prim_b_FSM_Sync_counter_type (ifmt_ift_prim_b_FSM_Sync_counter)—Offset 30304h

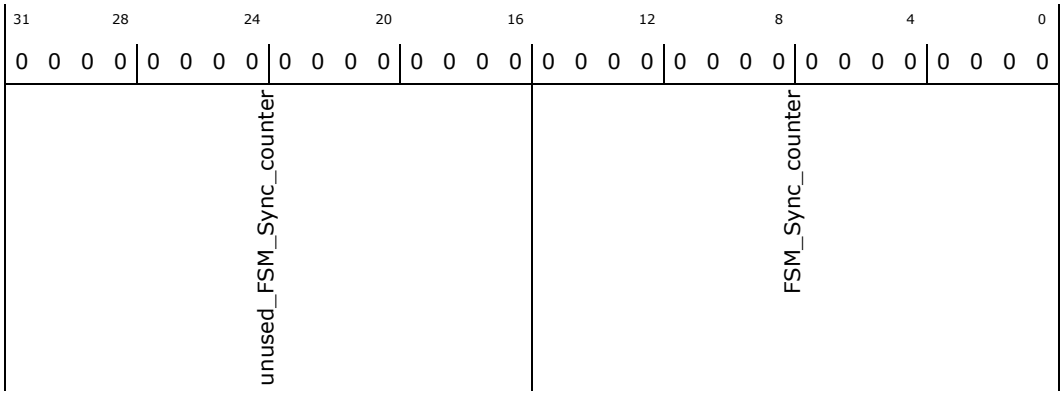
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Sync_counter: [ISPMMADR] + 30304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Sync_counter:** Unused
15:0	0h RO	**FSM_Sync_counter:** FSM Sync counter: counts the pixel components of the request being served (starting from value 1)

3.7.162 reg_ifmt_ift_prim_b_FSM_Crop_status_type (ifmt_ift_prim_b_FSM_Crop_status)—Offset 30308h

FSM Crop status

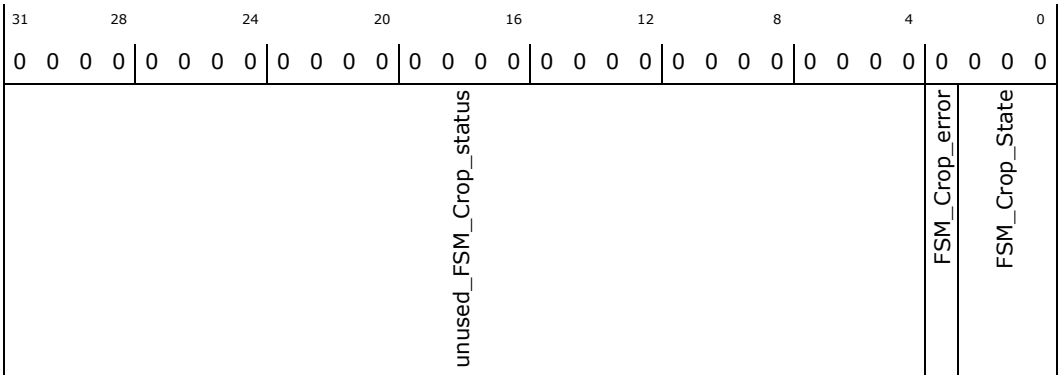
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Crop_status: [ISPMMADR] + 30308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_FSM_Crop_status:** Unused
3	0h RO	**FSM_Crop_error:** Error flag: when set in combination with: Crop Line state unexpected vsynch or eof has been received; Req. Lines state unexpected vsynch or eof has been received; Req. Vectors state unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0h RO	**FSM_Crop_State:** FSM State: State: 0)Idle -- 1)Wait Line -- 2)Crop Line -- 3)Crop Pixel -- 4)Pass pixel -- 5) Pass Line

3.7.163 reg_ifmt_ift_prim_b_FSM_Crop_line_counter_type (ifmt_ift_prim_b_FSM_Crop_line_counter)—Offset 3030Ch

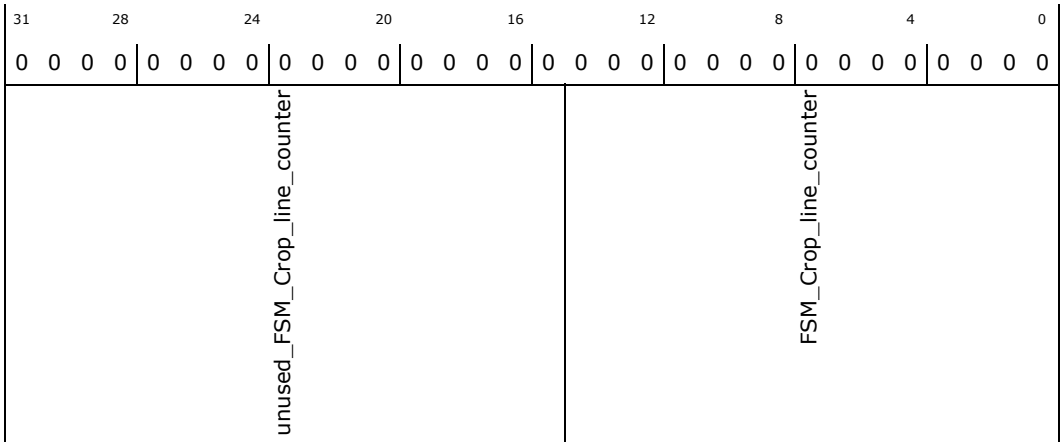
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Crop_line_counter: [ISPMMADR] + 3030Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RW	**unused_FSM_Crop_line_counter:** Unused
14:0	0h RO	**FSM_Crop_line_counter:** FSM Crop line counter

3.7.164 reg_ifmt_ift_prim_b_FSM_Crop_pixel_counter_type (ifmt_ift_prim_b_FSM_Crop_pixel_counter)—Offset 30310h

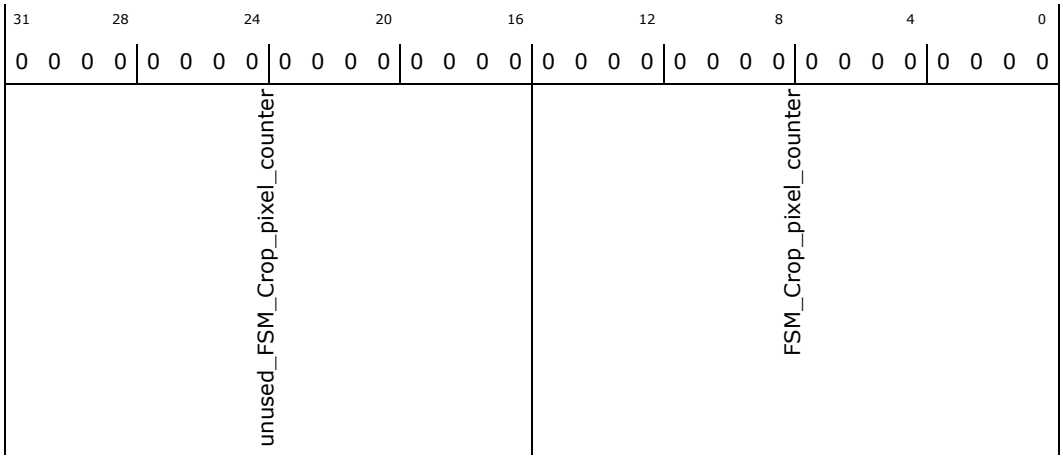
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Crop_pixel_counter: [ISPMMADR] + 30310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Crop_pixel_counter:** Unused
15:0	0h RO	**FSM_Crop_pixel_counter:** FSM Crop pixel component counter

3.7.165 reg_ifmt_ift_prim_b_FSM_Deinterl_idx_buffer_type (ifmt_ift_prim_b_FSM_Deinterl_idx_buffer)—Offset 30314h

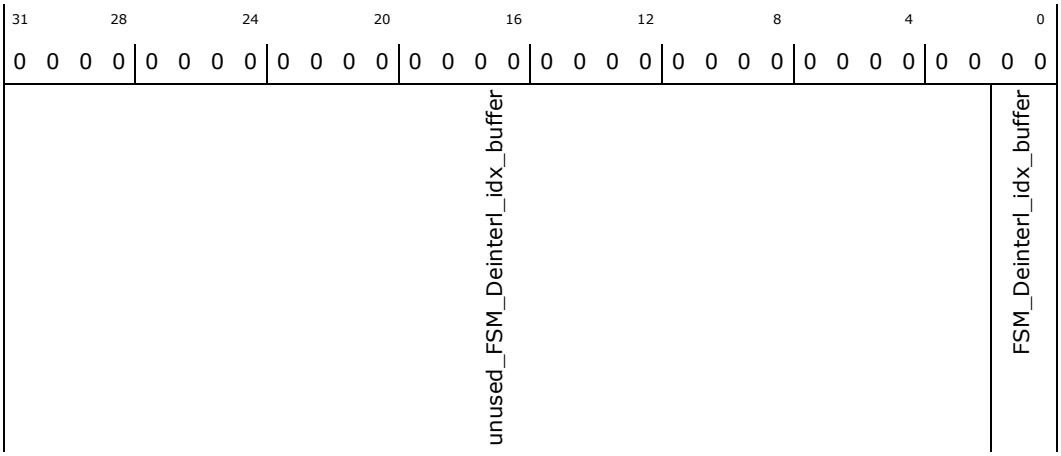
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Deinterl_idx_buffer: [ISPMMADR] + 30314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Deinterl_idx_buffer:** Unused
1:0	0h RO	**FSM_Deinterl_idx_buffer:** FSM Deinterleaving idx buffer

3.7.166 reg_ifmt_ift_prim_b_FSM_Horiz_Decim_cnt_type (ifmt_ift_prim_b_FSM_Horiz_Decim_cnt)—Offset 30318h

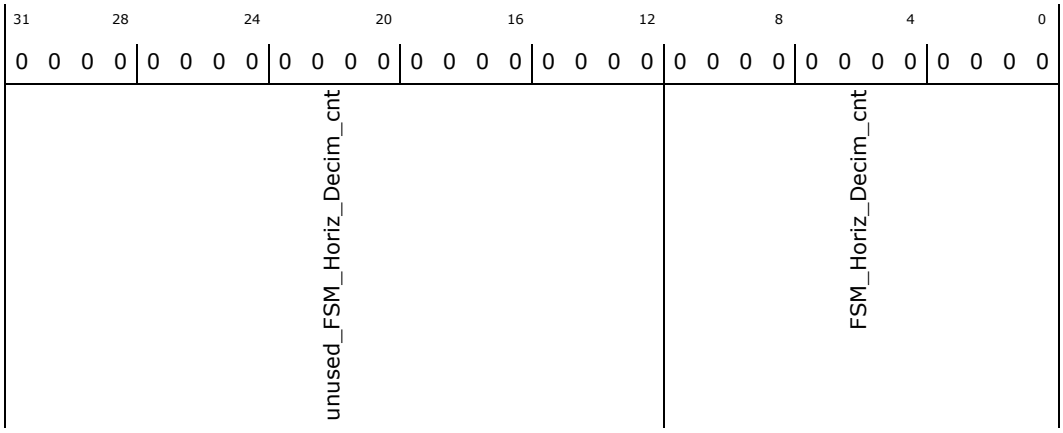
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Horiz_Decim_cnt: [ISPMMADR] + 30318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Horiz_Decim_cnt:** Unused
11:0	0h RO	**FSM_Horiz_Decim_cnt:** FSM Horizontal Decimation counter

3.7.167 reg_ifmt_ift_prim_b_FSM_Vertic_Decim_cnt_type (ifmt_ift_prim_b_FSM_Vertic_Decim_cnt)—Offset 3031Ch

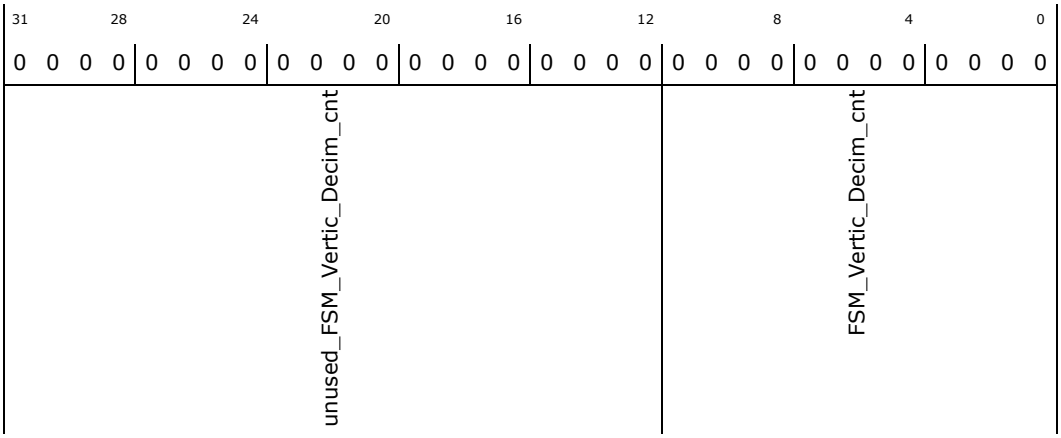
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Vertic_Decim_cnt: [ISPMMADR] + 3031Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Vertic_Decim_cnt:** Unused
11:0	0h RO	**FSM_Vertic_Decim_cnt:** FSM Vertical decimation counter

3.7.168 reg_ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt)—Offset 30320h

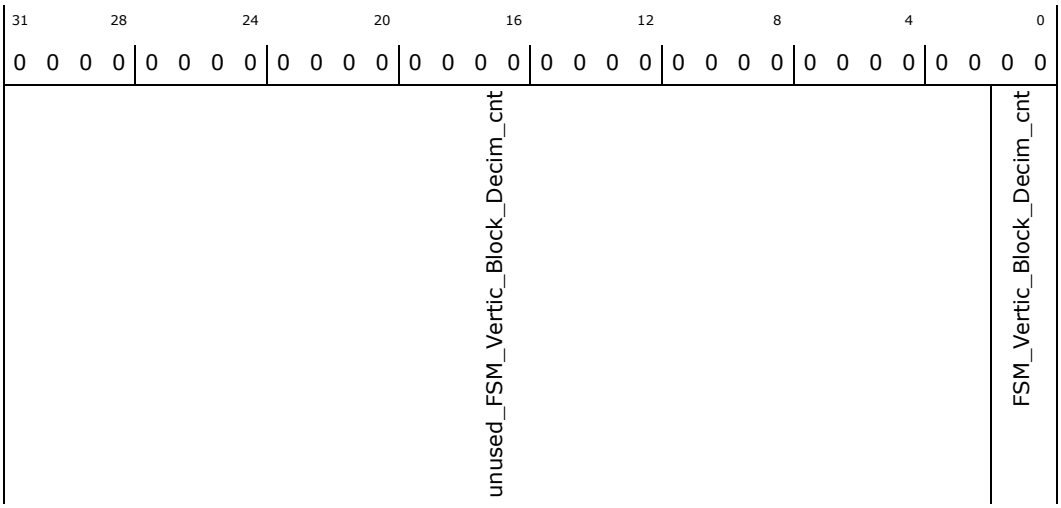
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt: [ISPMMADR] + 30320h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Vertic_Block_Decim_cnt:** Unused
1:0	0h RO	**FSM_Vertic_Block_Decim_cnt:** FSM Vertical block decimation counter

3.7.169 reg_ifmt_ift_prim_b_IF_FSM_Padding_status_type (ifmt_ift_prim_b_IF_FSM_Padding_status)—Offset 30324h

FSM Padding status

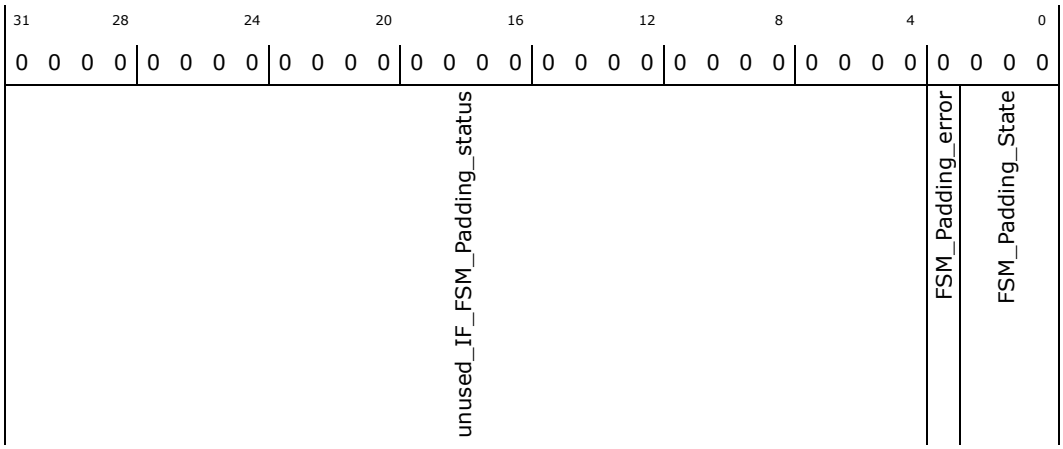
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Padding_status: [ISPMMADR] + 30324h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Padding_status:** Unused
3	0h RO	**FSM_Padding_error:** Error flag: when set in combination with: Left Padding state an unexpected vsynch or hsync has been received; Write state an unexpected vsynch or hsync has been received; Right padding state unexpected vsynch has been received; Send EOL state an unexpected vsynch has been received; another state an illegal state transition has occurred.
2:0	0h RO	**FSM_Padding_State:** FSM State: State: 0)Idle -- 1)Left Padding -- 2)Write -- 3)Right padding -- 4)Sending EOL

3.7.170 reg_ifmt_ift_prim_b_IF_FSM_Padding_elem_idx_type (ifmt_ift_prim_b_IF_FSM_Padding_elem_idx)—Offset 30328h

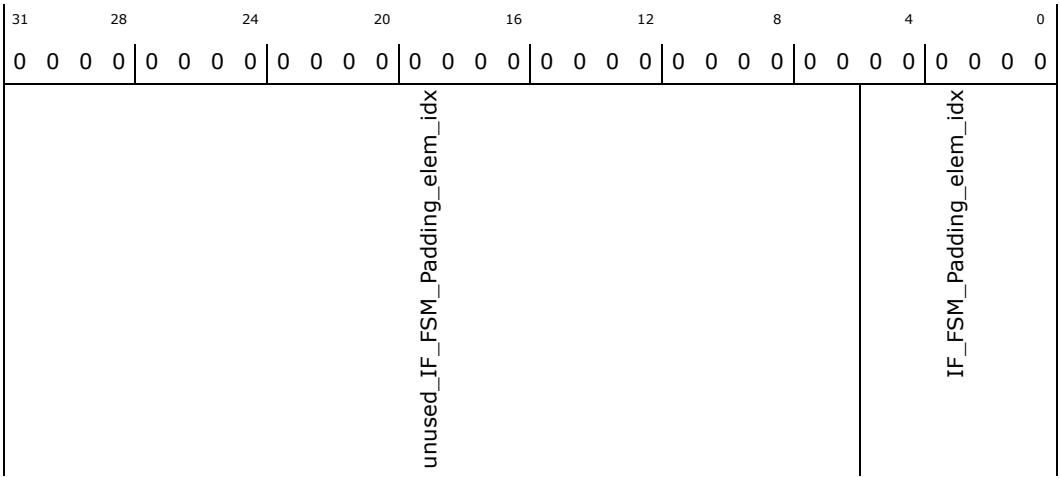
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Padding_elem_idx: [ISPMMADR] + 30328h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_FSM_Padding_elem_idx:** Unused
5:0	0h RO	**IF_FSM_Padding_elem_idx:** FSM Padding element index counter

3.7.171 reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup)—Offset 3032Ch

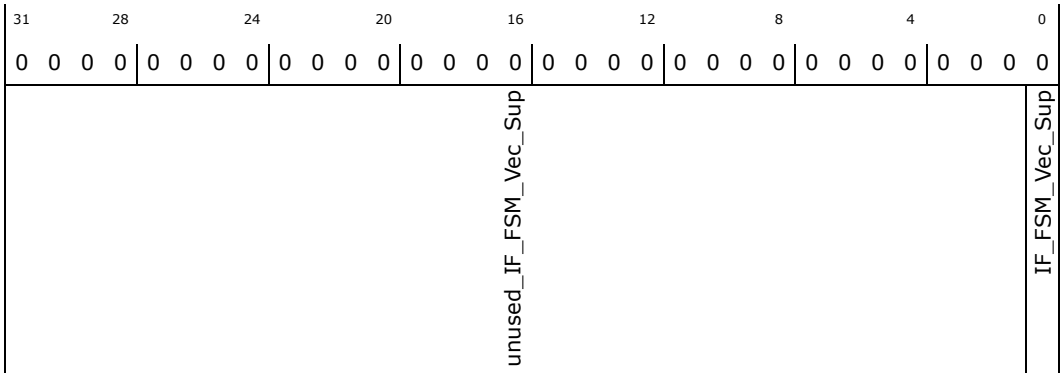
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Vec_Sup: [ISPMMADR] + 3032Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup:** Unused
0	0h RO	**IF_FSM_Vec_Sup:** FSM Vector support error state: if set the FSM Vector support is in error state

3.7.172 reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full)—Offset 30330h

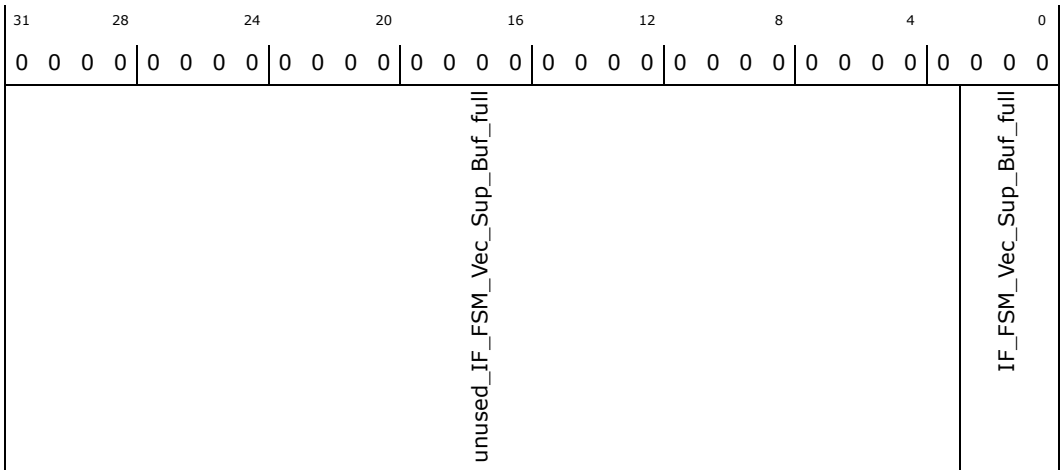
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full: [ISPMMADR] + 30330h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_FSM_Vec_Sup_Buf_full:** Unused
2:0	0h RO	**IF_FSM_Vec_Sup_Buf_full:** FSM Vector support buf full: one-hot encoding flag signaling that the correspondent buffer is full

3.7.173 reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept)—Offset 30334h

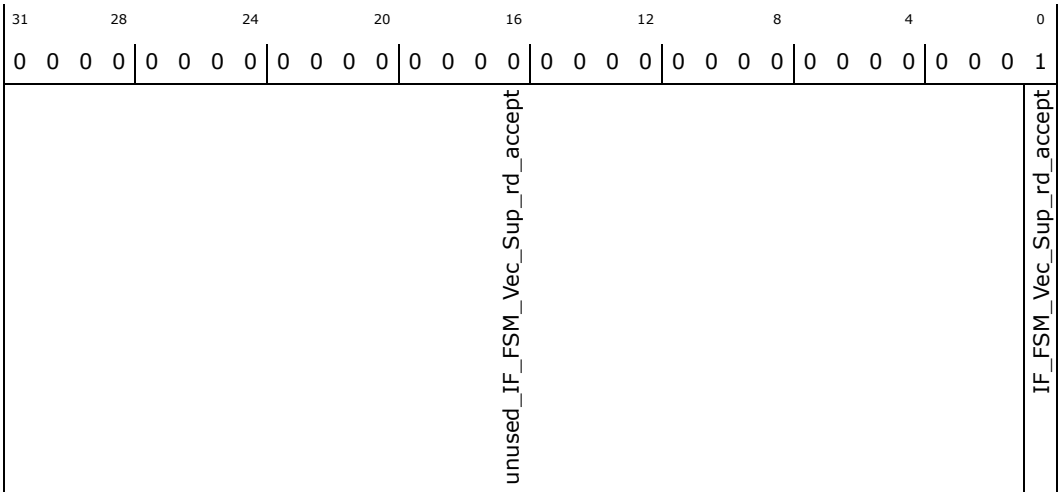
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept: [ISPMMADR] + 30334h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup_rd_accept:** Unused
0	1h RO	**IF_FSM_Vec_Sup_rd_accept:** FSM Vector Support fifo rd accept flag

3.7.174 reg_ifmt_ift_prim_b_IF_Pixel_Fifo_status_type (ifmt_ift_prim_b_IF_Pixel_Fifo_status)—Offset 30338h

Pixel Fifo status

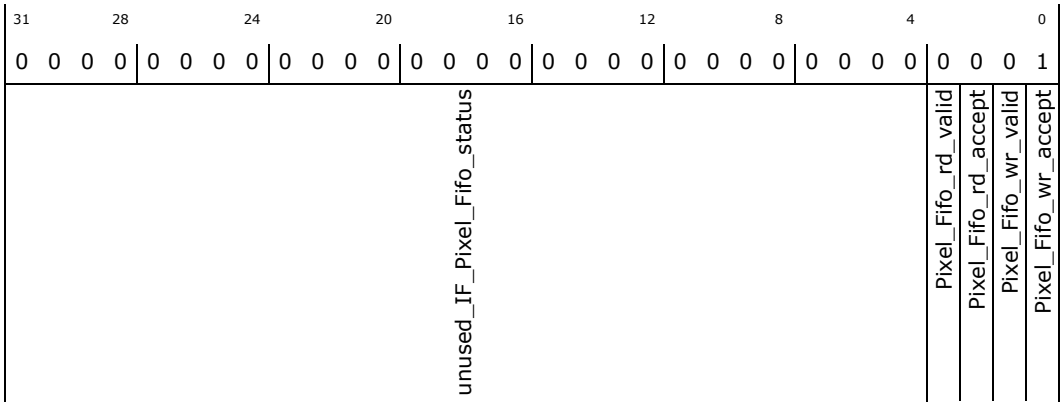
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Pixel_Fifo_status: [ISPMMADR] + 30338h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_Pixel_Fifo_status:** Unused
3	0h RO	**Pixel_Fifo_rd_valid:** Fifo has an element to be read
2	0h RO	**Pixel_Fifo_rd_accept:** IF accepts Pixel(s)
1	0h RO	**Pixel_Fifo_wr_valid:** There is an element to write into the Fifo
0	1h RO	**Pixel_Fifo_wr_accept:** Fifo is not full(1), Fifo is Full(0)

3.7.175 reg_ifmt_ift_sec_IF_sw_rst_type (ifmt_ift_sec_IF_sw_rst)—Offset 30400h

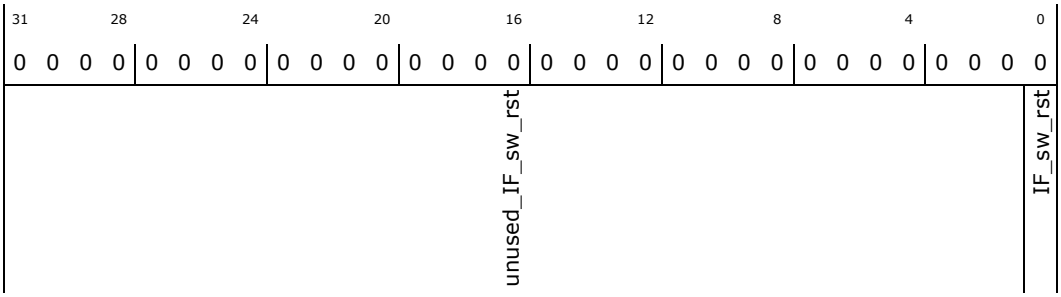
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_sw_rst: [ISPMMADR] + 30400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_sw_rst:** Unused
0	0h RW	**IF_sw_rst:** Software Reset

3.7.176 reg_ifmt_ift_sec_IF_start_line_type (ifmt_ift_sec_IF_start_line)—Offset 30404h

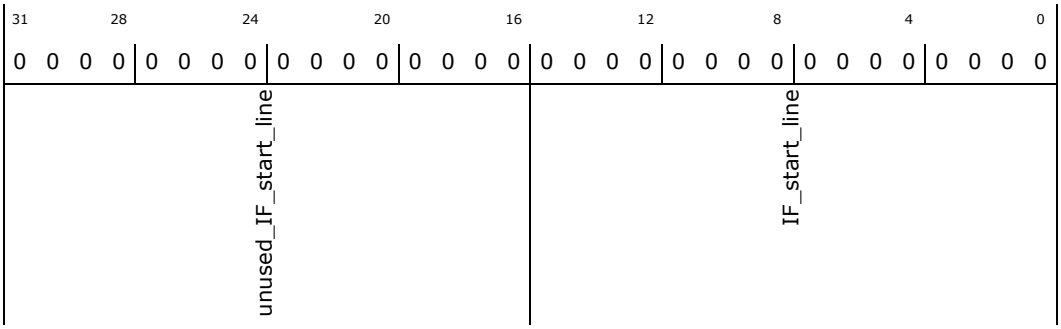
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_start_line: [ISPMMADR] + 30404h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_line:** Unused
15:0	0h RW	**IF_start_line:** Start line: number of line to skip before passing the 1st line

3.7.177 reg_ifmt_ift_sec_IF_start_column_type (ifmt_ift_sec_IF_start_column)—Offset 30408h

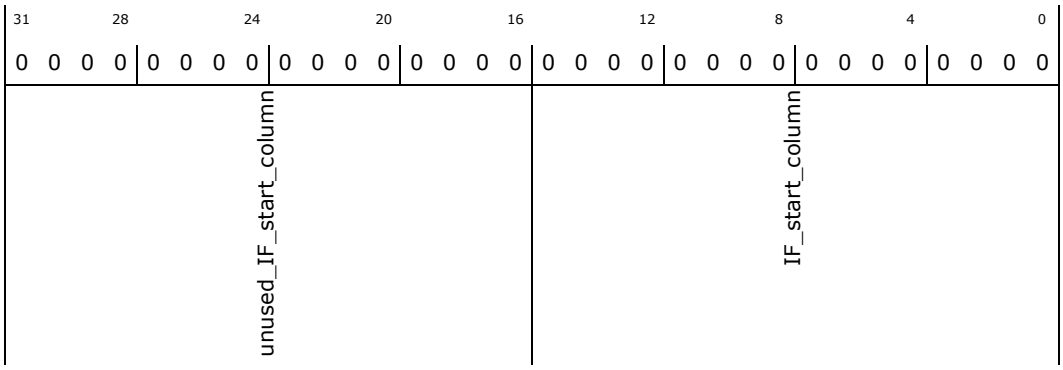
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_start_column: [ISPMMADR] + 30408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_column:** Unused
15:0	0h RW	**IF_start_column:** Start column: number pixel component to skip before passing the 1st of a line

3.7.178 reg_ifmt_ift_sec_IF_Cropped_height_type (ifmt_ift_sec_IF_Cropped_height)—Offset 3040Ch

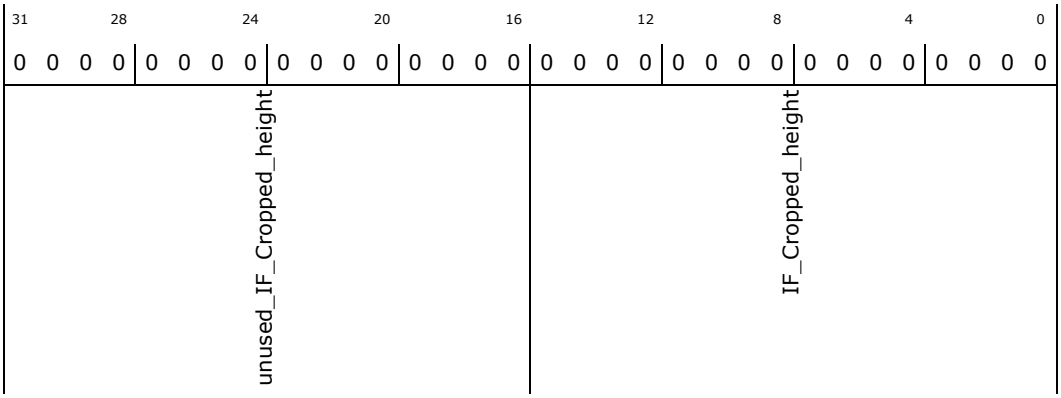
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Cropped_height: [ISPMMADR] + 3040Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_height:** Unused
15:0	0h RW	**IF_Cropped_height:** Cropped height: number of lines of the cropped image

3.7.179 reg_ifmt_ift_sec_IF_Cropped_width_type (ifmt_ift_sec_IF_Cropped_width)—Offset 30410h

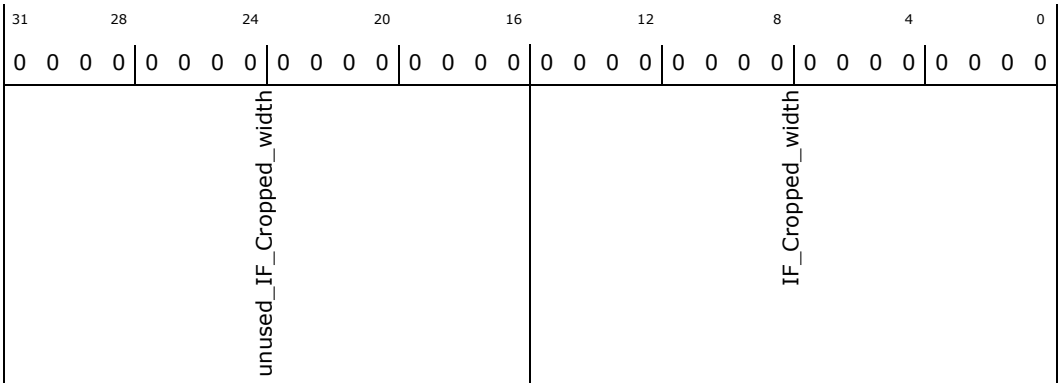
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Cropped_width: [ISPMMADR] + 30410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_width:** Unused

Bit Range	Default & Access	Description
15:0	0h RW	**IF_Cropped_width:** Cropped width: number of pixel component of the cropped image

3.7.180 reg_ifmt_ift_sec_IF_Vert_Decim_type (ifmt_ift_sec_IF_Vert_Decim)—Offset 30414h

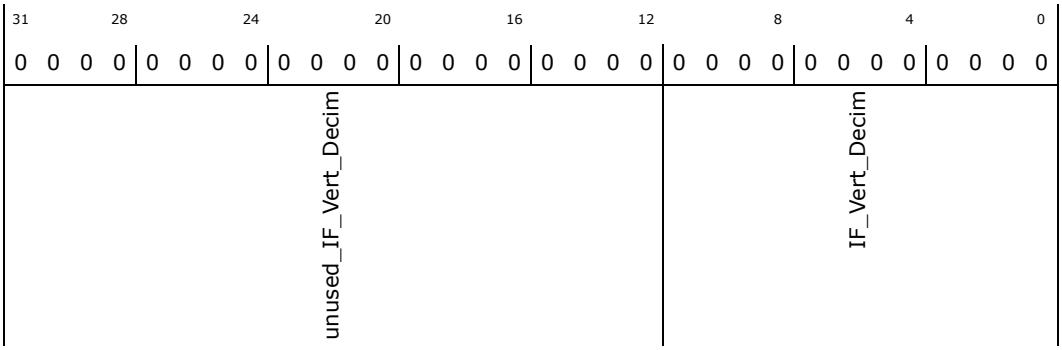
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Vert_Decim: [ISPMMADR] + 30414h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Vert_Decim:** Unused
11:0	0h RW	**IF_Vert_Decim:** Vertical decimation factor

3.7.181 reg_ifmt_ift_sec_IF_Horiz_Decim_type (ifmt_ift_sec_IF_Horiz_Decim)—Offset 30418h

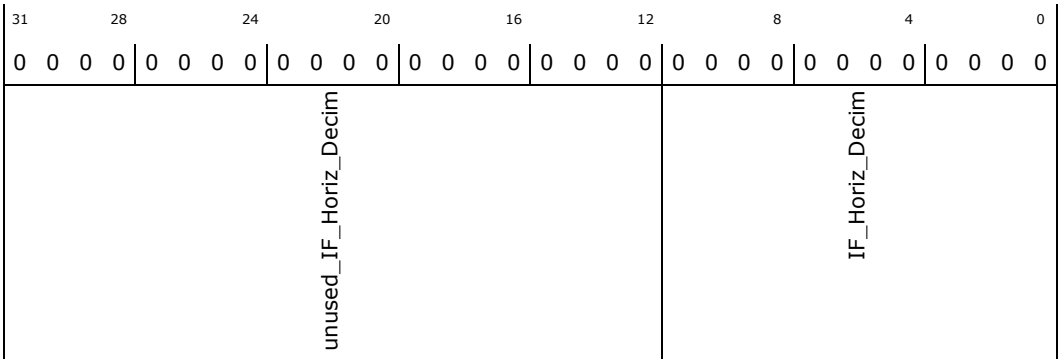
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Horiz_Decim: [ISPMMADR] + 30418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Horiz_Decim:** Unused
11:0	0h RW	**IF_Horiz_Decim:** Horizontal decimation factor

3.7.182 reg_ifmt_ift_sec_IF_Horiz_Deinter_type (ifmt_ift_sec_IF_Horiz_Deinter)—Offset 3041Ch

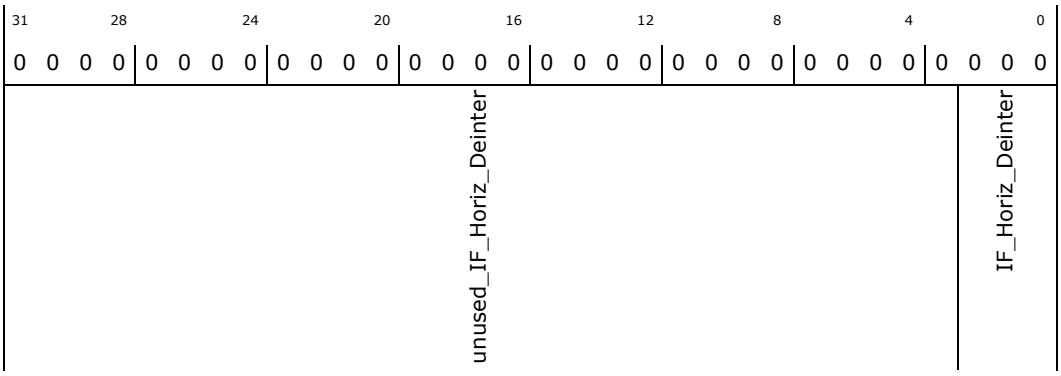
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Horiz_Deinter: [ISPMMADR] + 3041Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Horiz_Deinter:** Unused
2:0	0h RW	**IF_Horiz_Deinter:** Horizontal deinterleaving factor

3.7.183 reg_ifmt_ift_sec_IF_Left_Pad_type (ifmt_ift_sec_IF_Left_Pad)—Offset 30420h

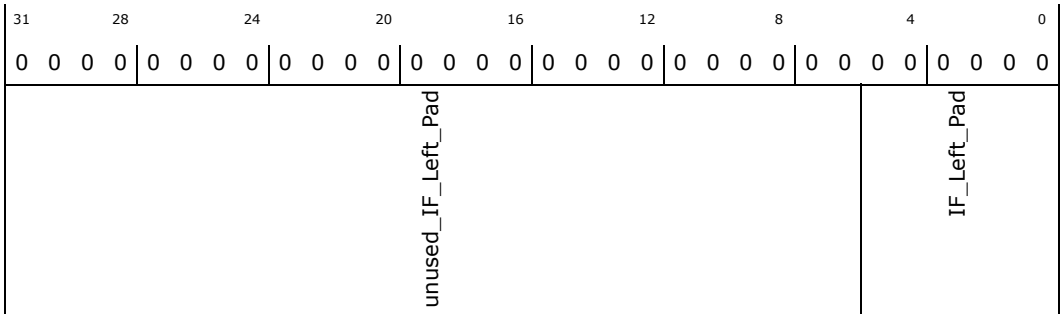
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Left_Pad: [ISPMMADR] + 30420h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_Left_Pad:** Unused
5:0	0h RW	**IF_Left_Pad:** Left padding: pizel component to be padded at the beggining of each line

3.7.184 reg_ifmt_ift_sec_IF_EOF_Offset_type (ifmt_ift_sec_IF_EOF_Offset)—Offset 30424h

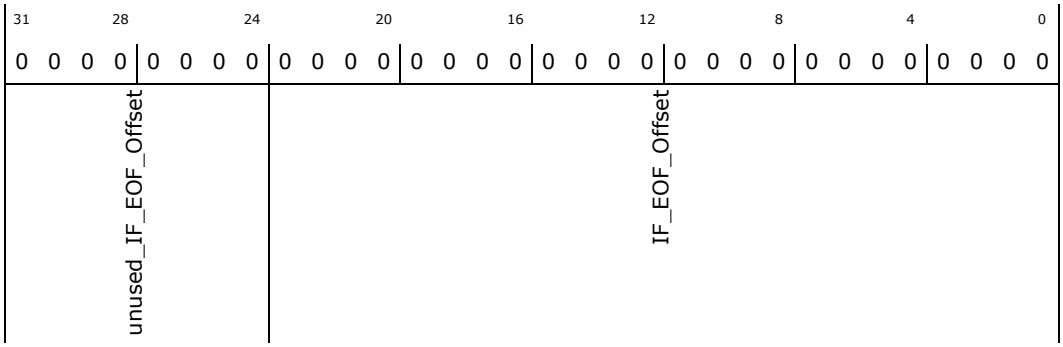
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_EOF_Offset: [ISPMMADR] + 30424h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_EOF_Offset:** Unused
23:0	0h RW	**IF_EOF_Offset:** End of line offset in bytes: number of bytes to add at the address at the end of a line

3.7.185 reg_ifmt_ift_sec_IF_Start_addr_type (ifmt_ift_sec_IF_Start_addr)—Offset 30428h

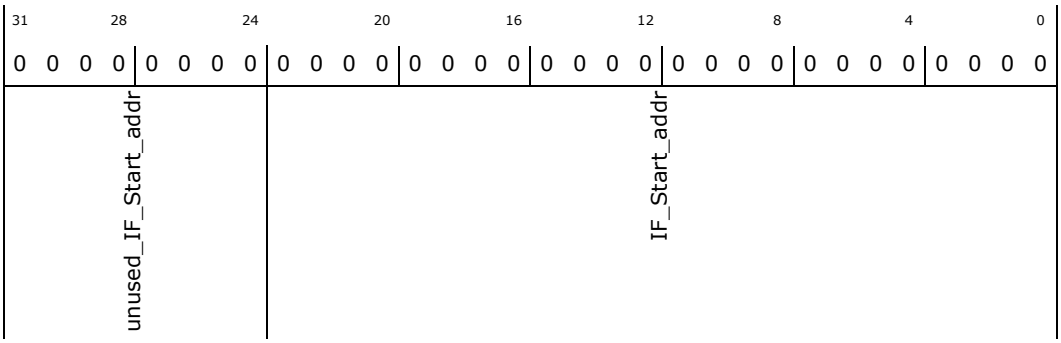
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Start_addr: [ISPMMADR] + 30428h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_Start_addr:** Unused
23:0	0h RW	**IF_Start_addr:** Start address in bytes: memory buffer start address

3.7.186 reg_ifmt_ift_sec_IF_End_addr_type (ifmt_ift_sec_IF_End_addr)—Offset 3042Ch

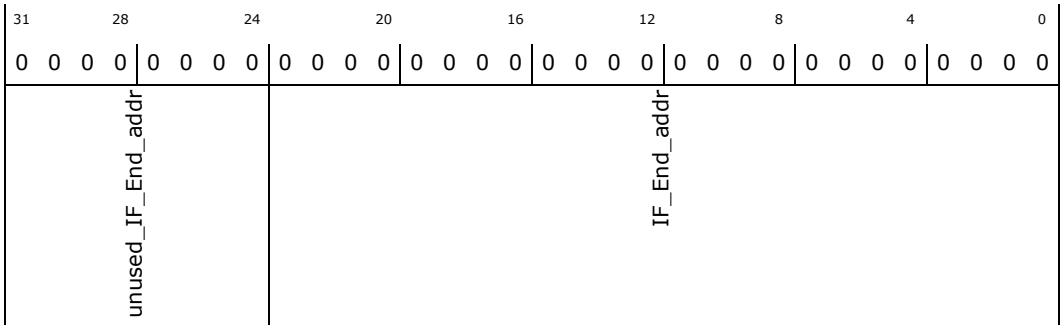
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_End_addr: [ISPMMADR] + 3042Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_End_addr:** Unused
23:0	0h RW	**IF_End_addr:** End address in bytes: memory buffer end address

3.7.187 reg_ifmt_ift_sec_IF_incr_type (ifmt_ift_sec_IF_incr)—Offset 30430h

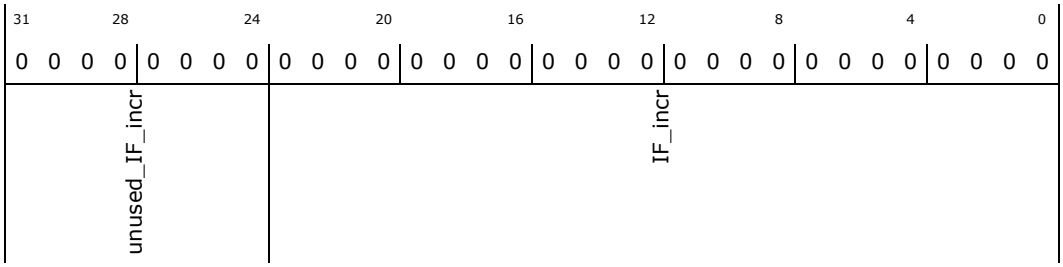
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_incr: [ISPMMADR] + 30430h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_incr:** Unused
23:0	0h RW	**IF_incr:** Word increment in memory word: word increment value after writing each word

3.7.188 reg_ifmt_ift_sec_IF_YUV_420_format_type (ifmt_ift_sec_IF_YUV_420_format)—Offset 30434h

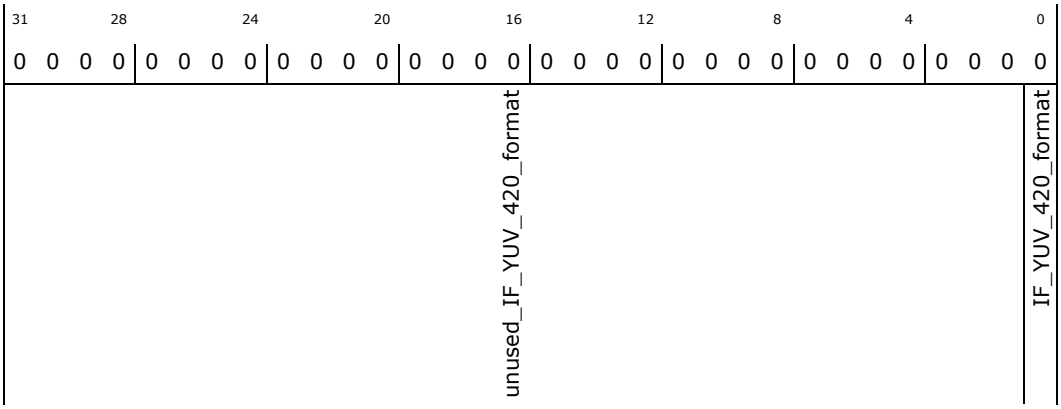
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_YUV_420_format: [ISPMMADR] + 30434h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_YUV_420_format:** Unused
0	0h RW	**IF_YUV_420_format:** YUV 420 format: set to work on legacy format YUV420

3.7.189 reg_ifmt_ift_sec_IF_Vsynch_active_low_type (ifmt_ift_sec_IF_Vsynch_active_low)—Offset 30438h

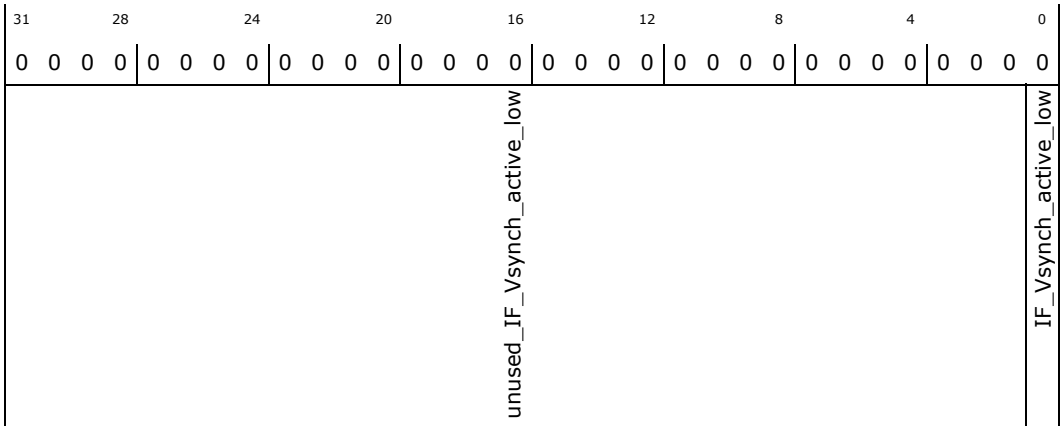
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Vsynch_active_low: [ISPMMADR] + 30438h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Vsynch_active_low:** Unused
0	0h RW	**IF_Vsynch_active_low:** Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

3.7.190 reg_ifmt_ift_sec_IF_Hsynch_active_low_type (ifmt_ift_sec_IF_Hsynch_active_low)—Offset 3043Ch

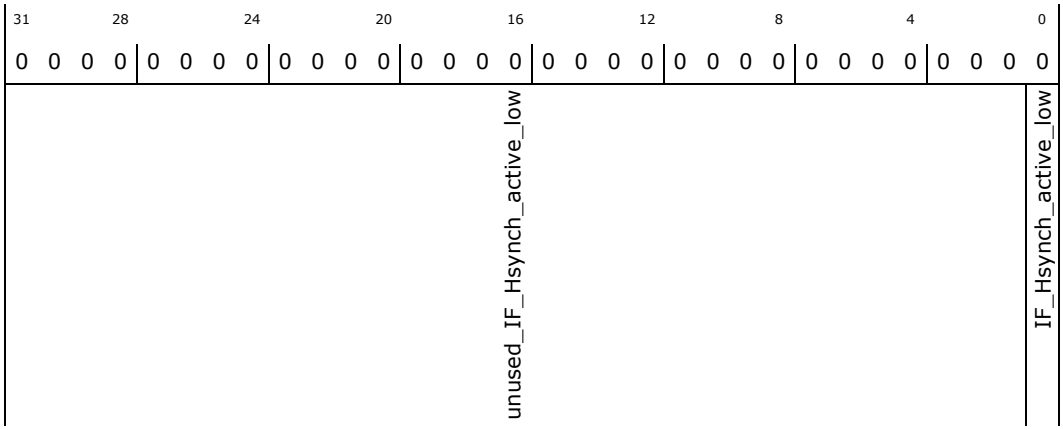
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Hsynch_active_low: [ISPMMADR] + 3043Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Hsynch_active_low:** Unused
0	0h RW	**IF_Hsynch_active_low:** Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

3.7.191 reg_ifmt_ift_sec_IF_ReEnable_type (ifmt_ift_sec_IF_ReEnable)—Offset 30440h

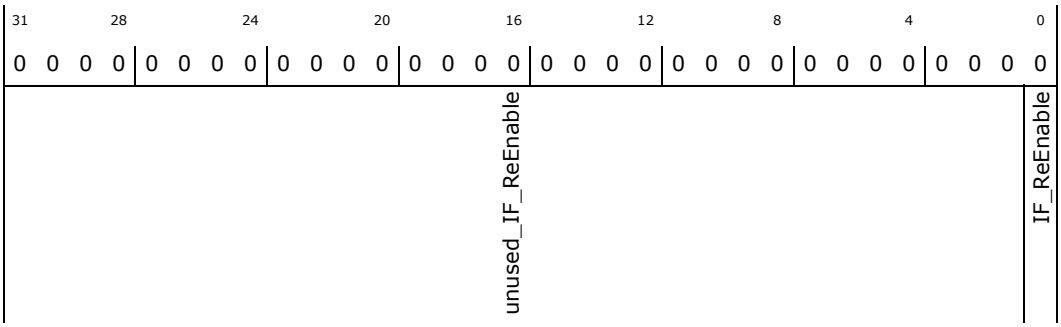
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_ReEnable: [ISPMMADR] + 30440h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_ReEnable:** Unused
0	0h RW	**IF_ReEnable:** Re-enable status update: set to 1 to re-enable status update after an error situation

3.7.192 reg_ifmt_ift_sec_IF_block_input_type (ifmt_ift_sec_IF_block_input)—Offset 30444h

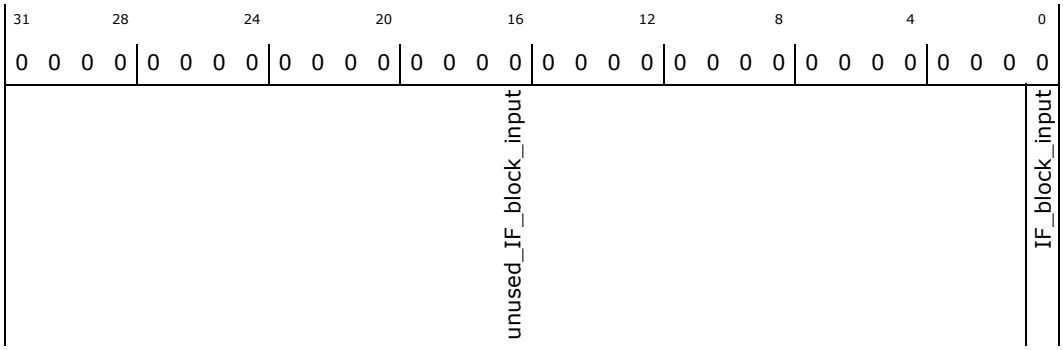
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_block_input: [ISPMMADR] + 30444h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_block_input:** Unused
0	0h RW	**IF_block_input:** Block input when no req: set to 1 to block data streaming input when no request is received

3.7.193 reg_ifmt_ift_sec_IF_Vert_Deinter_type (ifmt_ift_sec_IF_Vert_Deinter)—Offset 30448h

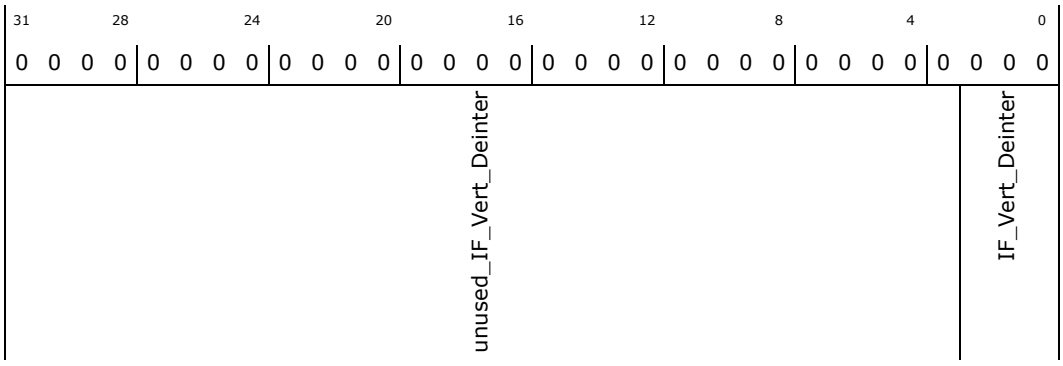
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Vert_Deinter: [ISPMMADR] + 30448h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Vert_Deinter:** Unused
2:0	0h RW	**IF_Vert_Deinter:** Vertical deinterleaving factor

3.7.194 reg_ifmt_ift_sec_IF_FSM_Sync_status_type (ifmt_ift_sec_IF_FSM_Sync_status)—Offset 30500h

FSM Sync status

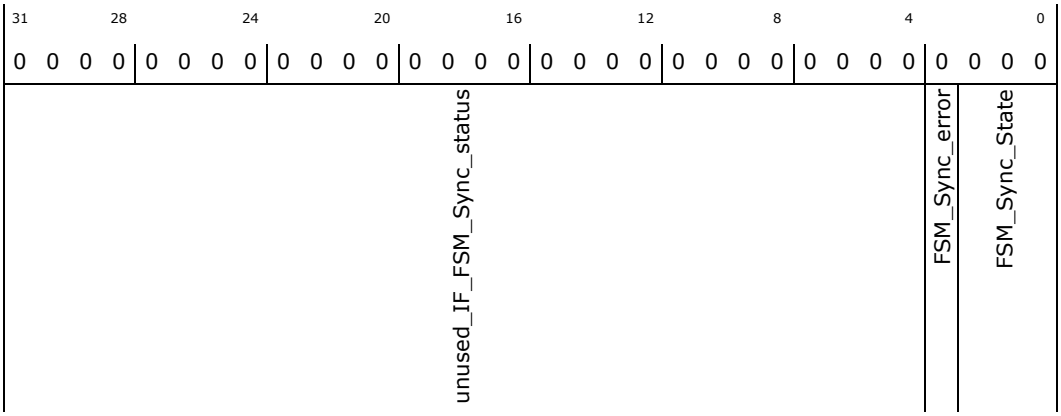
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Sync_status: [ISPMMADR] + 30500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Sync_status:** Unused
3	0h RO	**FSM_Sync_error:** Error flag: when set in combination with: Idle state an unknown command has been received; Req. Lines state an unexpected vsynch or eof has been received; Req. Vectors state an unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0h RO	**FSM_Sync_State:** FSM State: State: 0)Idle -- 1)Req Frame -- 2)Req. Lines -- 3)Req. Vectors -- 4)Send Acknowledge

3.7.195 reg_ifmt_ift_sec_FSM_Sync_counter_type (ifmt_ift_sec_FSM_Sync_counter)—Offset 30504h

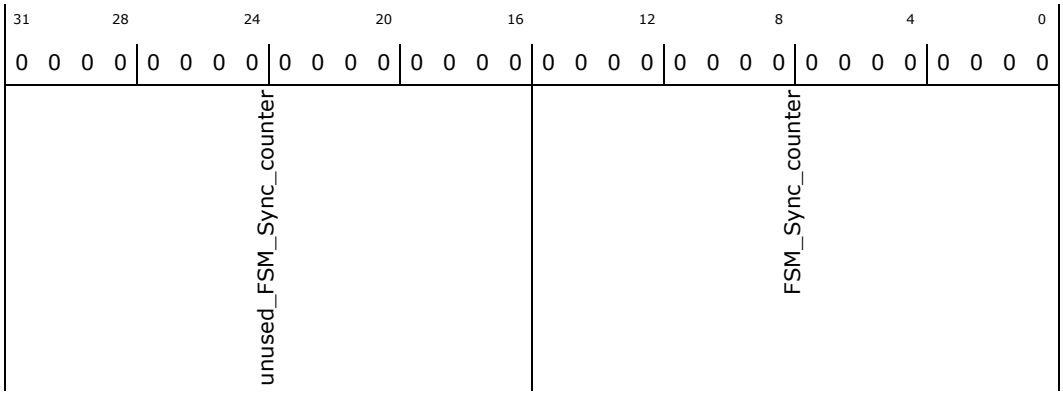
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Sync_counter: [ISPMMADR] + 30504h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Sync_counter:** Unused
15:0	0h RO	**FSM_Sync_counter:** FSM Sync counter: counts the pixel components of the request being served (starting from value 1)

3.7.196 reg_ifmt_ift_sec_FSM_Crop_status_type (ifmt_ift_sec_FSM_Crop_status)—Offset 30508h

FSM Crop status

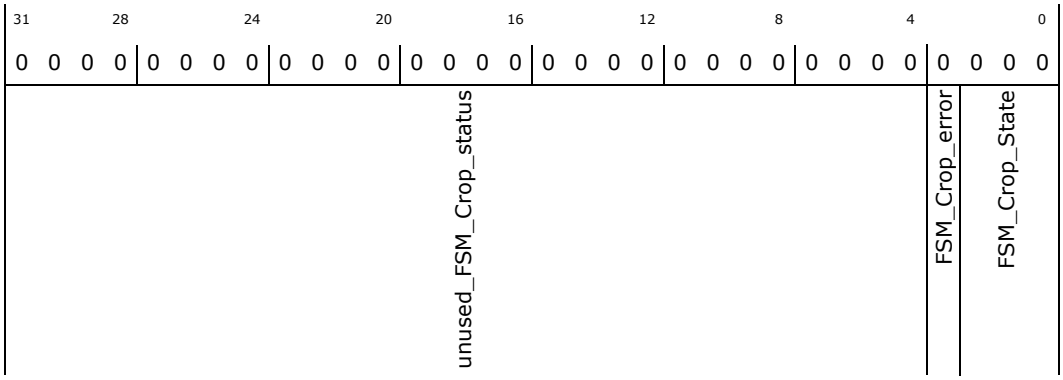
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Crop_status: [ISPMMADR] + 30508h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_FSM_Crop_status:** Unused

Bit Range	Default & Access	Description
3	0h RO	**FSM_Crop_error:** Error flag: when set in combination with: Crop Line state unexpected vsynch or eof has been received; Req. Lines state unexpected vsynch or eof has been received; Req. Vectors state unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0h RO	**FSM_Crop_State:** FSM State: State: 0)Idle -- 1)Wait Line -- 2)Crop Line -- 3)Crop Pixel -- 4)Pass pixel -- 5) Pass Line

3.7.197 reg_ifmt_ift_sec_FSM_Crop_line_counter_type (ifmt_ift_sec_FSM_Crop_line_counter)—Offset 3050Ch

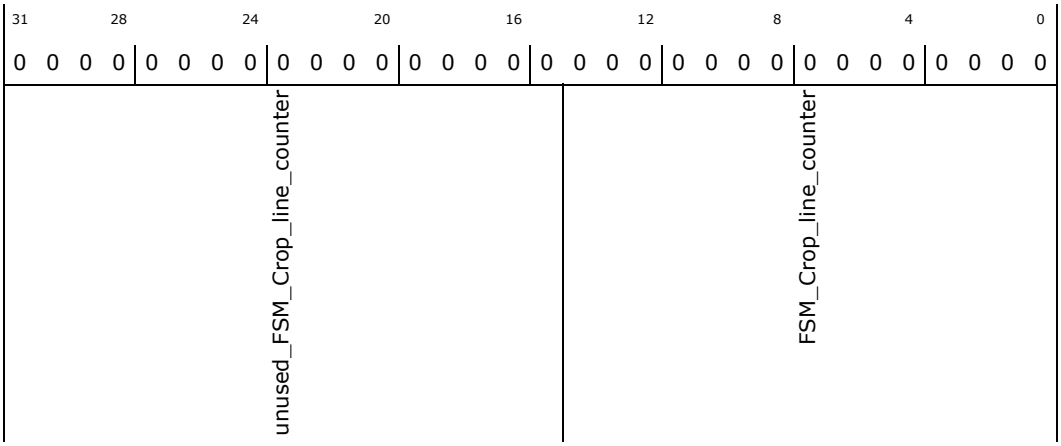
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Crop_line_counter: [ISPMMADR] + 3050Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RW	**unused_FSM_Crop_line_counter:** Unused
14:0	0h RO	**FSM_Crop_line_counter:** FSM Crop line counter

3.7.198 reg_ifmt_ift_sec_FSM_Crop_pixel_counter_type (ifmt_ift_sec_FSM_Crop_pixel_counter)—Offset 30510h

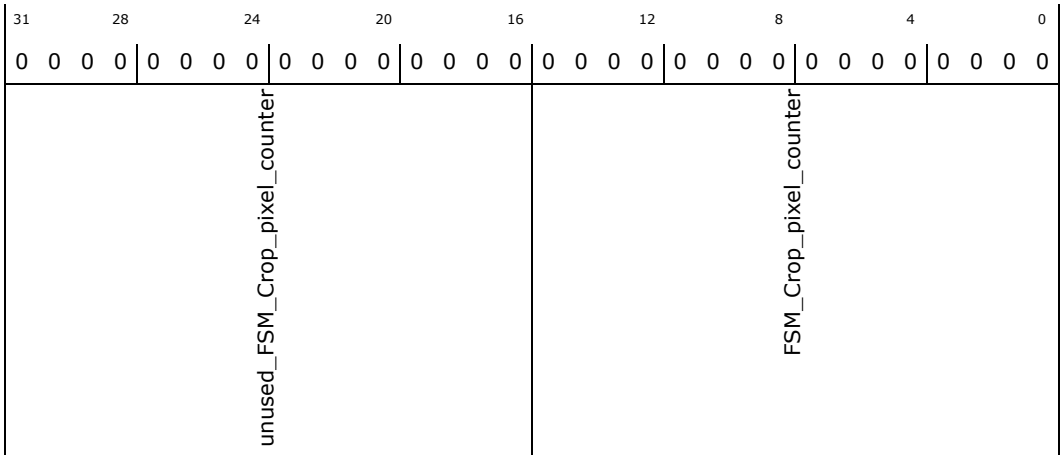
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Crop_pixel_counter: [ISPMMADR] + 30510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Crop_pixel_counter:** Unused
15:0	0h RO	**FSM_Crop_pixel_counter:** FSM Crop pixel component counter

3.7.199 reg_ifmt_ift_sec_FSM_Deinterl_idx_buffer_type (ifmt_ift_sec_FSM_Deinterl_idx_buffer)—Offset 30514h

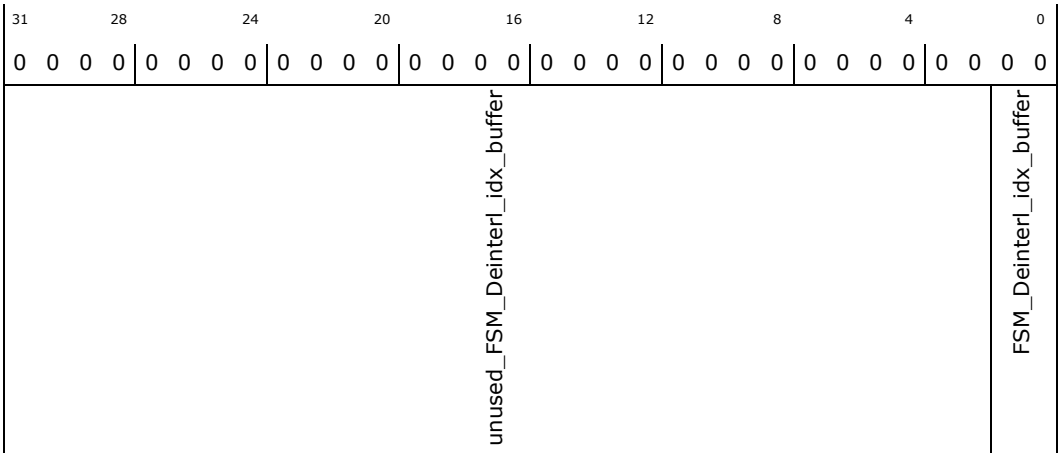
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Deinterl_idx_buffer: [ISPMMADR] + 30514h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Deinterl_idx_buffer:** Unused
1:0	0h RO	**FSM_Deinterl_idx_buffer:** FSM Deinterleaving idx buffer

3.7.200 reg_ifmt_ift_sec_FSM_Horiz_Decim_cnt_type (ifmt_ift_sec_FSM_Horiz_Decim_cnt)—Offset 30518h

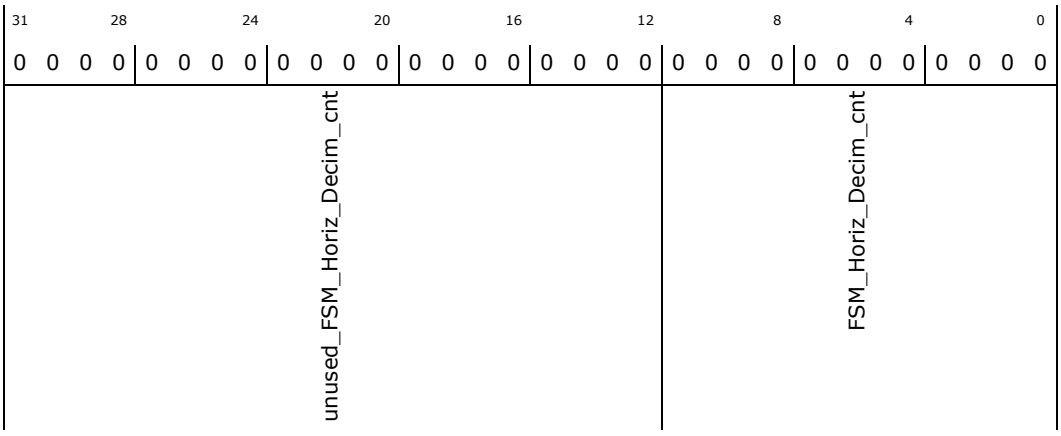
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Horiz_Decim_cnt: [ISPMMADR] + 30518h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Horiz_Decim_cnt:** Unused
11:0	0h RO	**FSM_Horiz_Decim_cnt:** FSM Horizontal Decimation counter

3.7.201 reg_ifmt_ift_sec_FSM_Vertic_Decim_cnt_type (ifmt_ift_sec_FSM_Vertic_Decim_cnt)—Offset 3051Ch

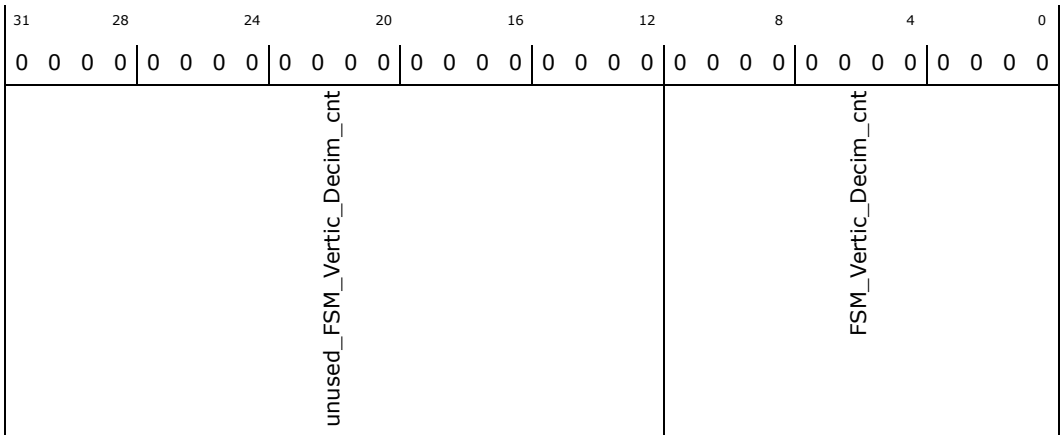
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Vertic_Decim_cnt: [ISPMMADR] + 3051Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Vertic_Decim_cnt:** Unused
11:0	0h RO	**FSM_Vertic_Decim_cnt:** FSM Vertical decimation counter

3.7.202 reg_ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt)—Offset 30520h

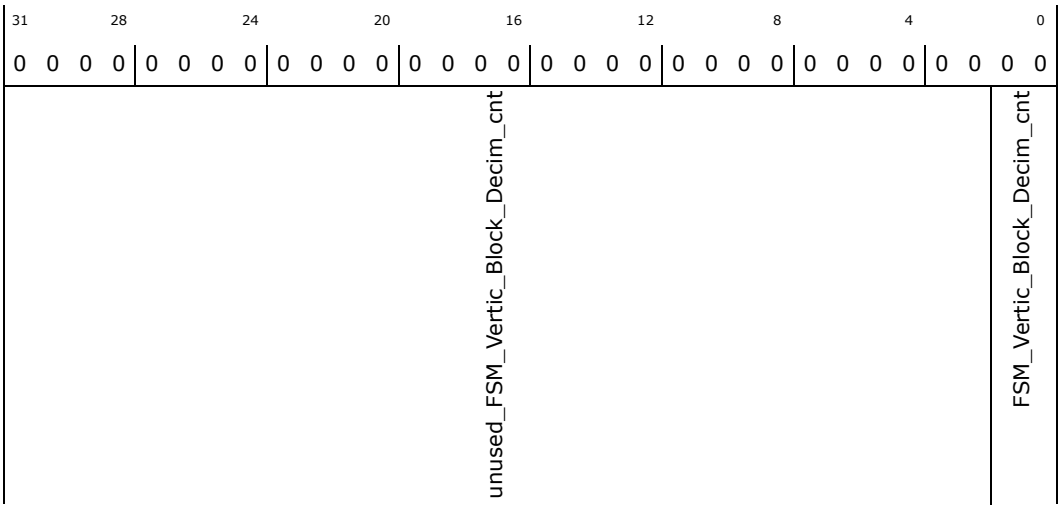
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt: [ISPMMADR] + 30520h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Vertic_Block_Decim_cnt:** Unused
1:0	0h RO	**FSM_Vertic_Block_Decim_cnt:** FSM Vertical block decimation counter

3.7.203 reg_ifmt_ift_sec_IF_FSM_Padding_status_type (ifmt_ift_sec_IF_FSM_Padding_status)—Offset 30524h

FSM Padding status

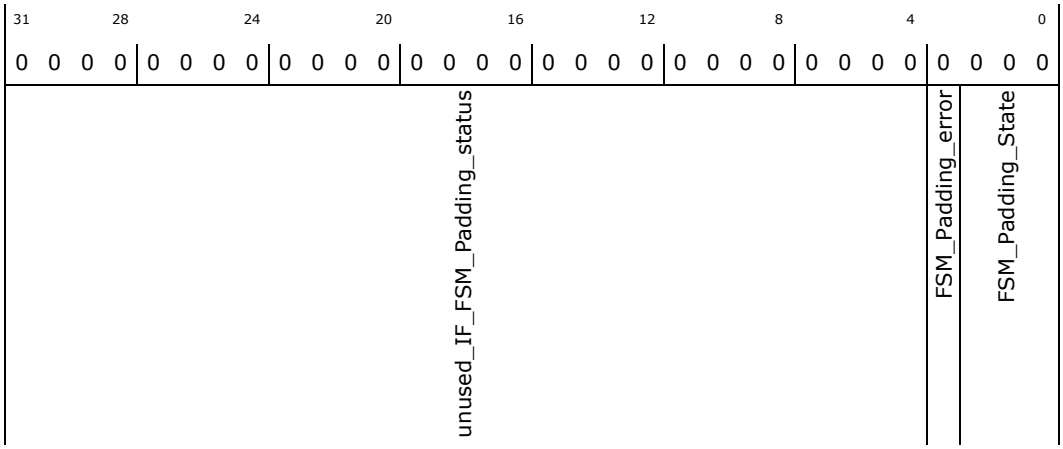
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Padding_status: [ISPMMADR] + 30524h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Padding_status:** Unused
3	0h RO	**FSM_Padding_error:** Error flag: when set in combination with: Left Padding state an unexpected vsynch or hsync has been received; Write state an unexpected vsynch or hsync has been received; Right padding state unexpected vsynch has been received; Send EOL state an unexpected vsynch has been received; another state an illegal state transition has occurred.
2:0	0h RO	**FSM_Padding_State:** FSM State: State: 0)Idle -- 1)Left Padding -- 2)Write -- 3)Right padding -- 4)Sending EOL

3.7.204 reg_ifmt_ift_sec_IF_FSM_Padding_elem_idx_type (ifmt_ift_sec_IF_FSM_Padding_elem_idx)—Offset 30528h

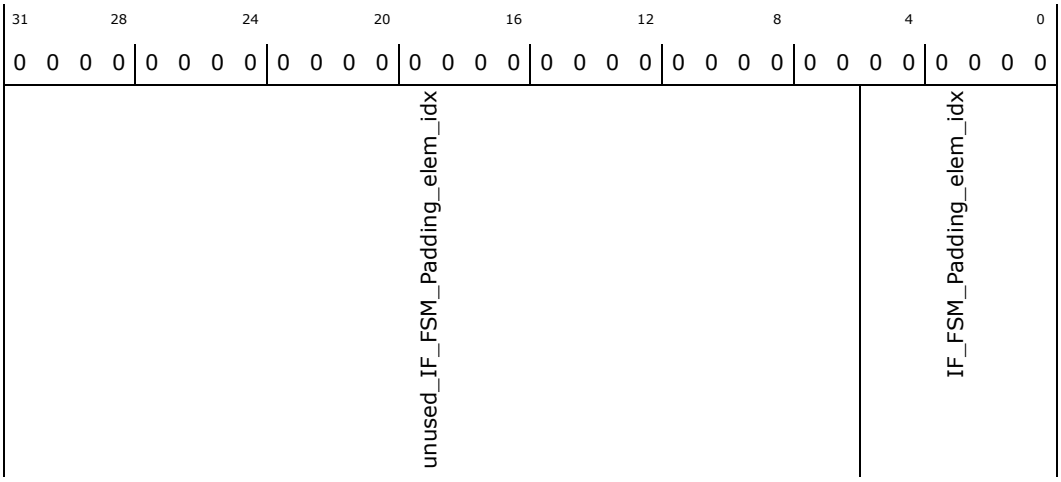
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Padding_elem_idx: [ISPMMADR] + 30528h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_FSM_Padding_elem_idx:** Unused
5:0	0h RO	**IF_FSM_Padding_elem_idx:** FSM Padding element index counter

3.7.205 reg_ifmt_ift_sec_IF_FSM_Vec_Sup_type (ifmt_ift_sec_IF_FSM_Vec_Sup)—Offset 3052Ch

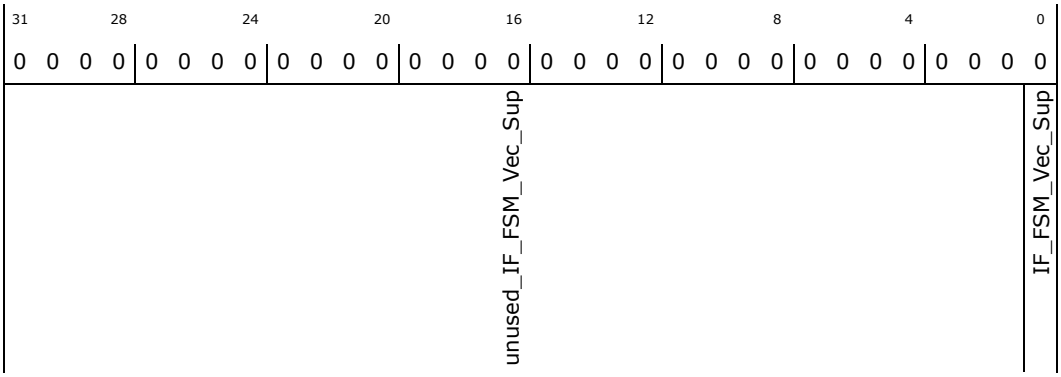
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Vec_Sup: [ISPMMADR] + 3052Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup:** Unused
0	0h RO	**IF_FSM_Vec_Sup:** FSM Vector support error state: if set the FSM Vector support is in error state

3.7.206 reg_ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full)—Offset 30530h

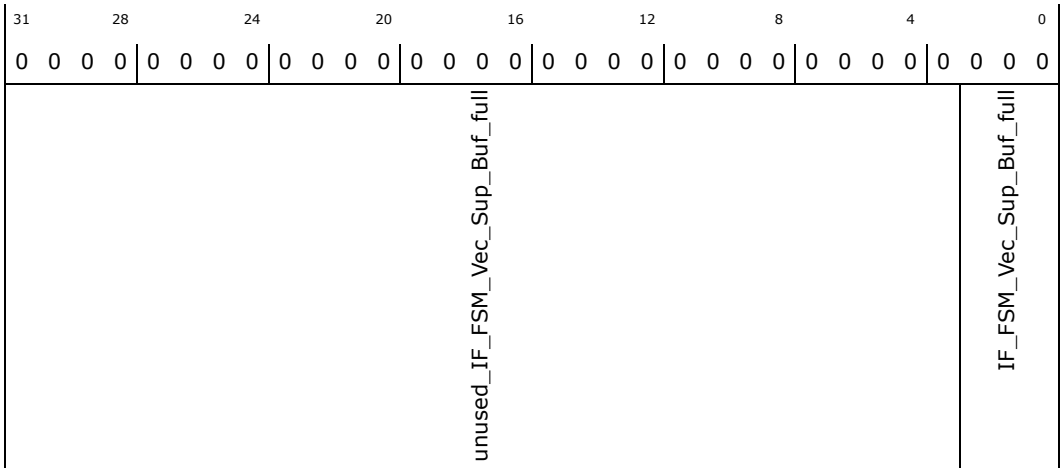
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full: [ISPMMADR] + 30530h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_FSM_Vec_Sup_Buf_full:** Unused
2:0	0h RO	**IF_FSM_Vec_Sup_Buf_full:** FSM Vector support buf full: one-hot encoding flag signaling that the correspondent buffer is full

3.7.207 reg_ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept)—Offset 30534h

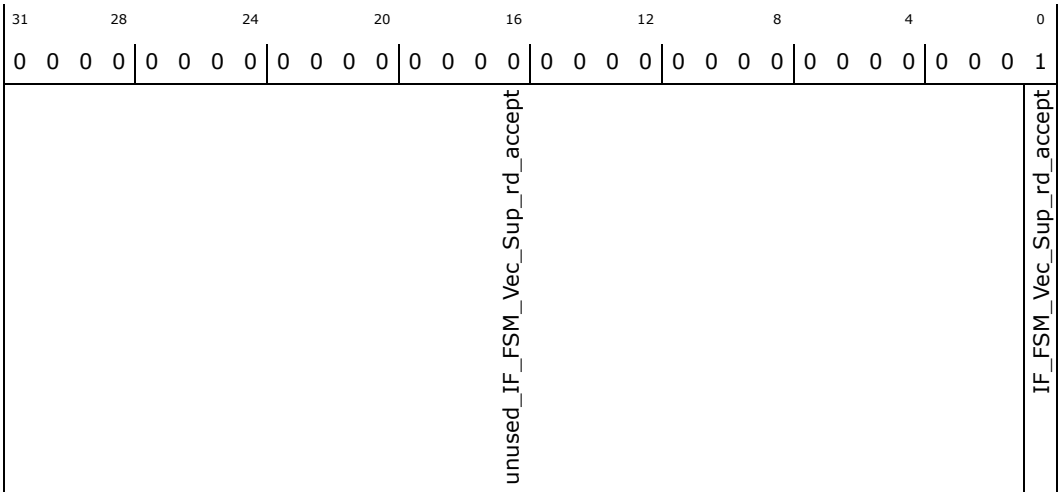
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept: [ISPMMADR] + 30534h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup_rd_accept:** Unused
0	1h RO	**IF_FSM_Vec_Sup_rd_accept:** FSM Vector Support fifo rd accept flag

3.7.208 reg_ifmt_ift_sec_IF_Pixel_Fifo_status_type (ifmt_ift_sec_IF_Pixel_Fifo_status)—Offset 30538h

Pixel Fifo status

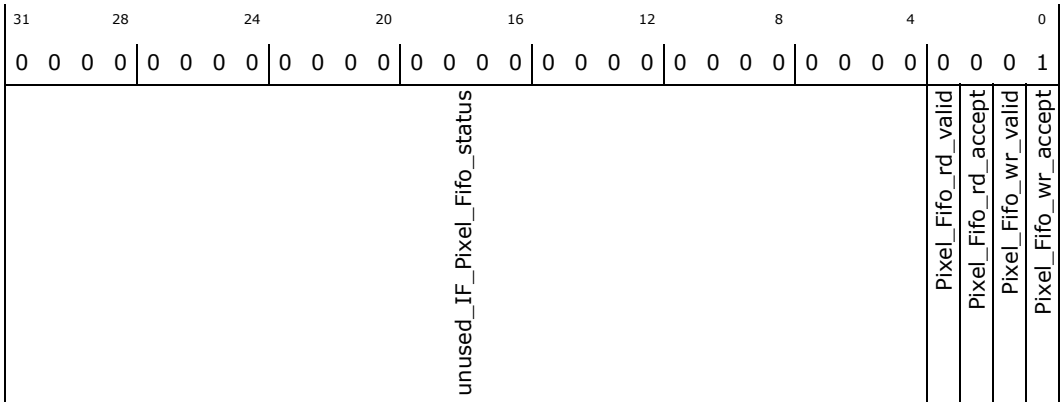
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Pixel_Fifo_status: [ISPMMADR] + 30538h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_Pixel_Fifo_status:** Unused
3	0h RO	**Pixel_Fifo_rd_valid:** Fifo has an element to be read
2	0h RO	**Pixel_Fifo_rd_accept:** IF accepts Pixel(s)
1	0h RO	**Pixel_Fifo_wr_valid:** There is an element to write into the Fifo
0	1h RO	**Pixel_Fifo_wr_accept:** Fifo is not full(1), Fifo is Full(0)

3.7.209 reg_ifmt_mem_cpy_MemCopy_sw_rst_type (ifmt_mem_cpy_MemCopy_sw_rst)—Offset 30600h

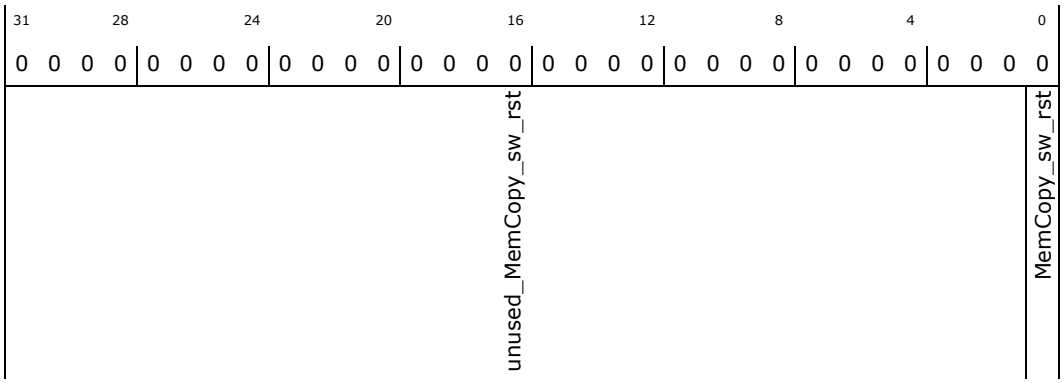
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_sw_rst: [ISPMMADR] + 30600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_sw_rst:** Unused
0	0h RW	**MemCopy_sw_rst:** Software Reset

3.7.210 reg_ifmt_mem_cpy_MemCopy_in_endian_type (ifmt_mem_cpy_MemCopy_in_endian)—Offset 30604h

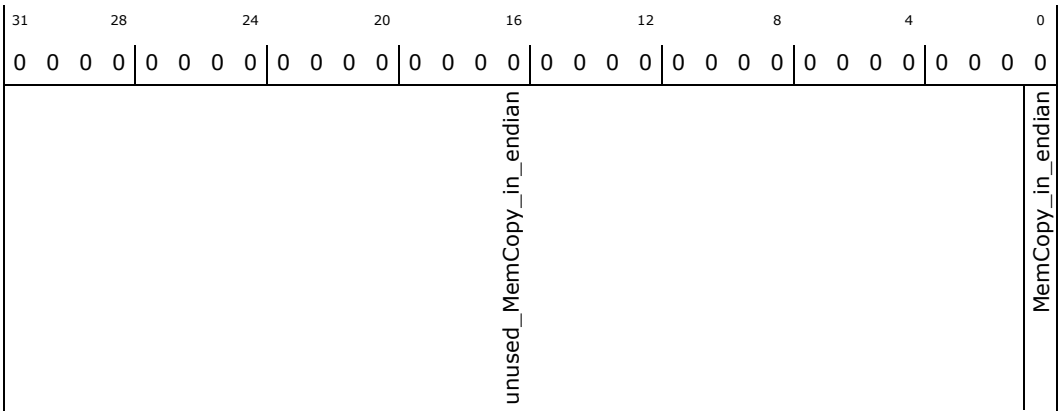
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_in_endian: [ISPMMADR] + 30604h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_in_endian:** Unused
0	0h RW	**MemCopy_in_endian:** Input endianness : set to 1 if input is big endian

3.7.211 reg_ifmt_mem_cpy_MemCopy_out_endian_type (ifmt_mem_cpy_MemCopy_out_endian)—Offset 30608h

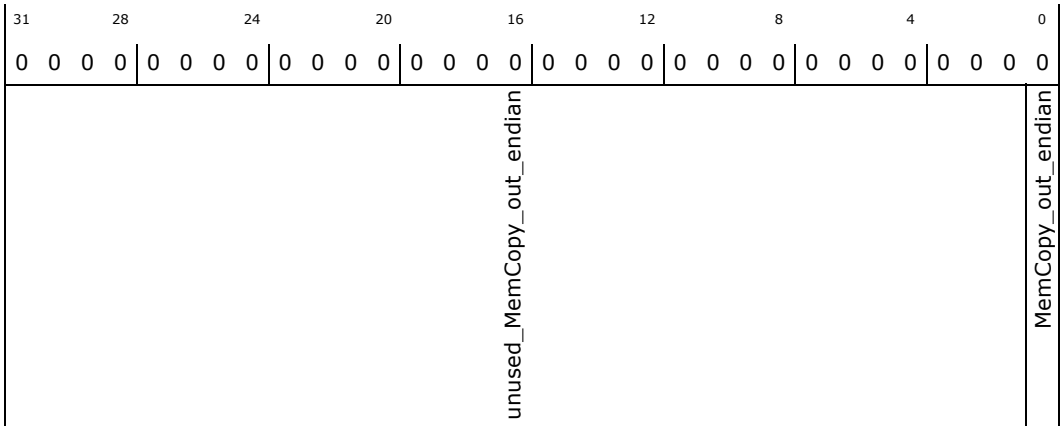
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_out_endian: [ISPMMADR] + 30608h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_out_endian:** Unused
0	0h RW	**MemCopy_out_endian:** Output endianness : set to 1 to deliver output input in big endian

3.7.212 reg_ifmt_mem_cpy_MemCopy_bit_swap_type (ifmt_mem_cpy_MemCopy_bit_swap)—Offset 3060Ch

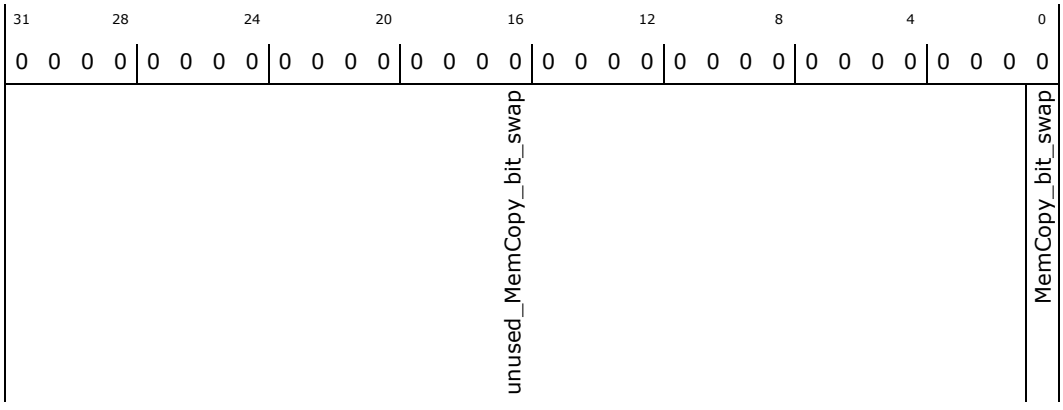
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_bit_swap: [ISPMMADR] + 3060Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_bit_swap:** Unused

Bit Range	Default & Access	Description
0	0h RW	**MemCopy_bit_swap:** Bit swapping : set to 1 to swap the bit of the incoming byte

3.7.213 reg_ifmt_mem_cpy_MemCopy_block_synch_type (ifmt_mem_cpy_MemCopy_block_synch)—Offset 30610h

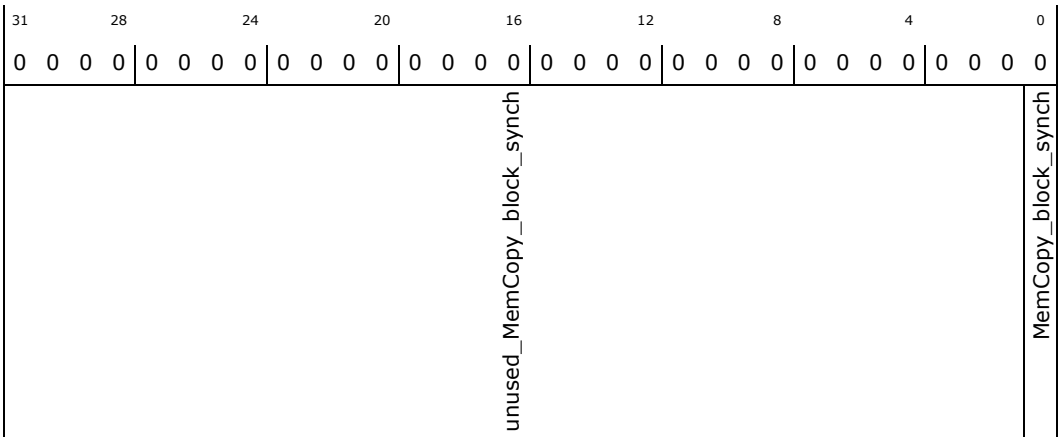
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_block_synch: [ISPMMADR] + 30610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_block_synch:** Unused
0	0h RW	**MemCopy_block_synch:** Block synchronization pulse active low: set to 1 if start of block and end of block are active low

3.7.214 reg_ifmt_mem_cpy_MemCopy_packet_synch_type (ifmt_mem_cpy_MemCopy_packet_synch)—Offset 30614h

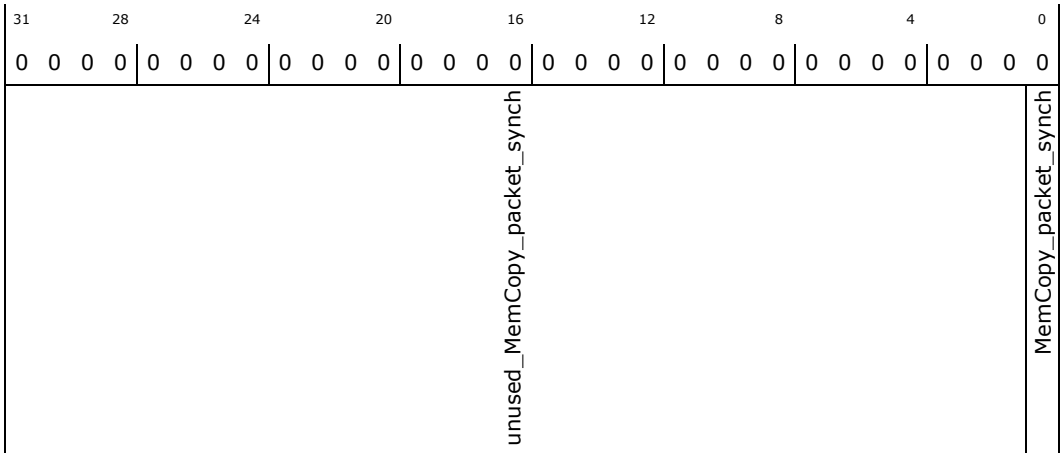
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_packet_synch: [ISPMMADR] + 30614h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_packet_synch:** Unused
0	0h RW	**MemCopy_packet_synch:** Packet synchronization pulse active low: set to 1 if start of packet and end of packet are active low

3.7.215 reg_ifmt_mem_cpy_MemCopy_rd_post_wr_sync_type (ifmt_mem_cpy_MemCopy_rd_post_wr_sync)—Offset 30618h

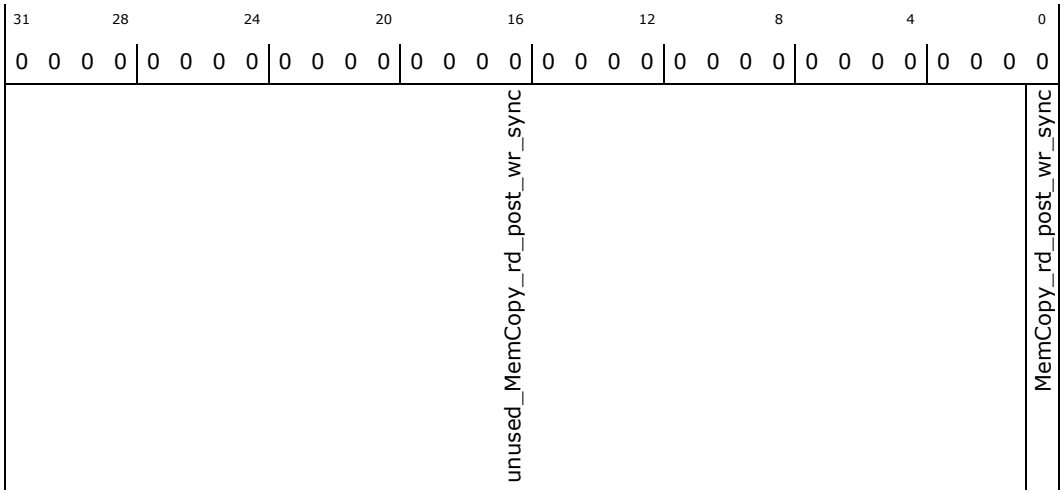
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_rd_post_wr_sync: [ISPMMADR] + 30618h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_rd_post_wr_sync:** Unused
0	0h RW	**MemCopy_rd_post_wr_sync:** Enable read post write synchronization: set to 1 to enable read post write check before sending acknowledge

3.7.216 reg_ifmt_mem_cpy_MemCopy_dual_input_type (ifmt_mem_cpy_MemCopy_dual_input)—Offset 3061Ch

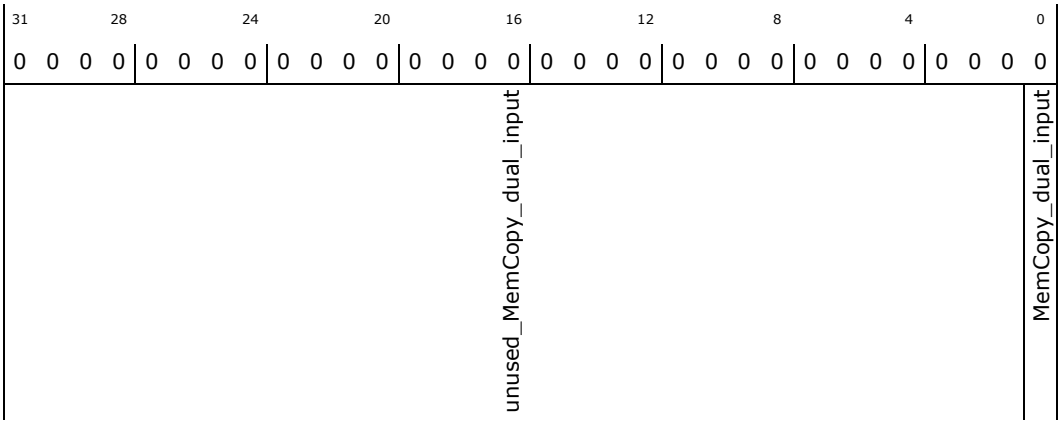
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_dual_input: [ISPMMADR] + 3061Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_dual_input:** Unused
0	0h RW	**MemCopy_dual_input:** Enable dual byte inputs: set to 1 to enable dual byte input

3.7.217 reg_ifmt_mem_cpy_MemCopy_ReEnable_type (ifmt_mem_cpy_MemCopy_ReEnable)—Offset 30620h

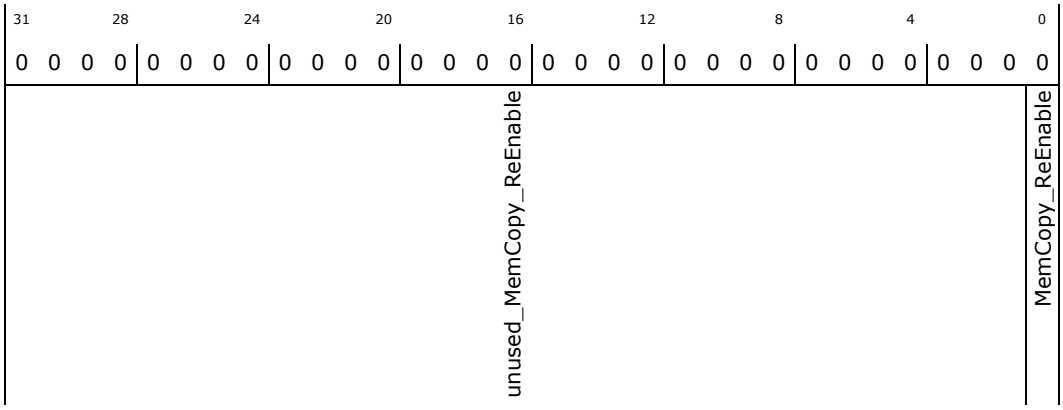
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_ReEnable: [ISPMMADR] + 30620h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_ReEnable:** Unused
0	0h RW	**MemCopy_ReEnable:** Re-enable status update: set to 1 to re-enable status update after an error situation

3.7.218 reg_ifmt_mem_cpy_MemCopy_token_data_type (ifmt_mem_cpy_MemCopy_token_data)—Offset 30700h

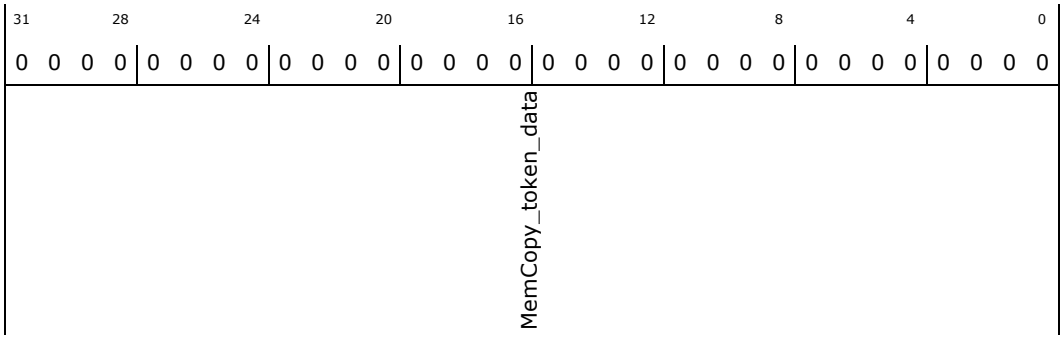
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_token_data: [ISPMMADR] + 30700h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**MemCopy_token_data:** Token data on command port

3.7.219 reg_ifmt_mem_cpy_MemCopy_FSM_Sync_status_type (ifmt_mem_cpy_MemCopy_FSM_Sync_status)—Offset 30704h

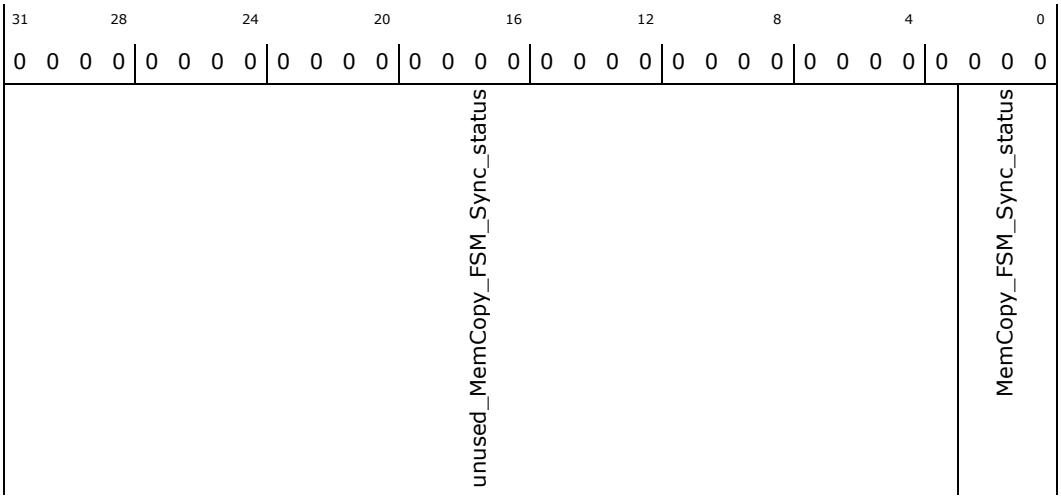
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Sync_status: [ISPMMADR] + 30704h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_MemCopy_FSM_Sync_status:** Unused
2:0	0h RO	**MemCopy_FSM_Sync_status:** FSM Synchronization Status: 0)Idle -- 1)Request Blocks -- 2)Request Packets -- 3)Request Bytes -- 4)Send Acknowledge

3.7.220 reg_ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt)—Offset 30708h

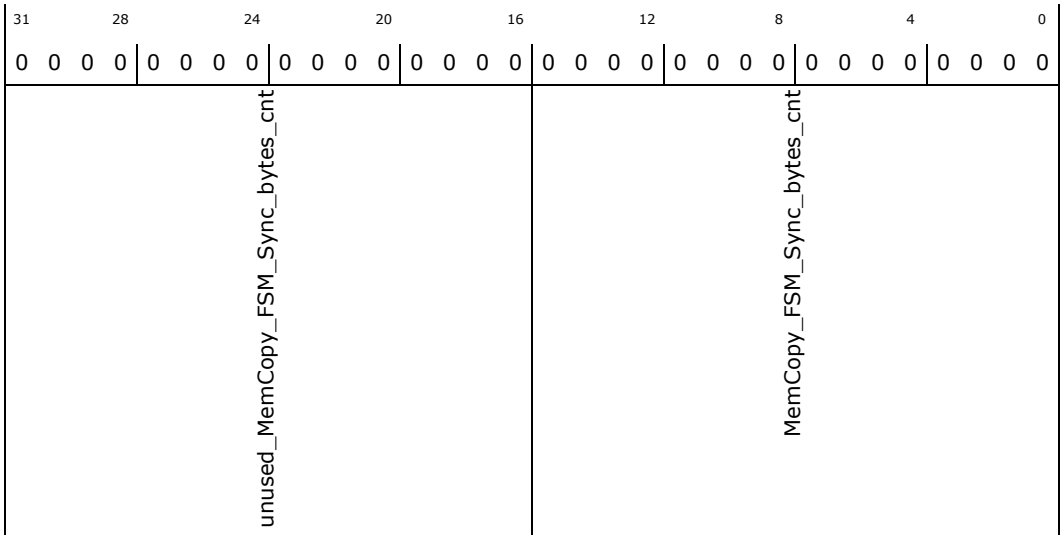
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt: [ISPMMADR] + 30708h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_MemCopy_FSM_Sync_bytes_cnt:** Unused
15:0	0h RO	**MemCopy_FSM_Sync_bytes_cnt:** FSM Synchronization bytes counter: counts the number of bytes received and packed

3.7.221 reg_ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt)—Offset 3070Ch

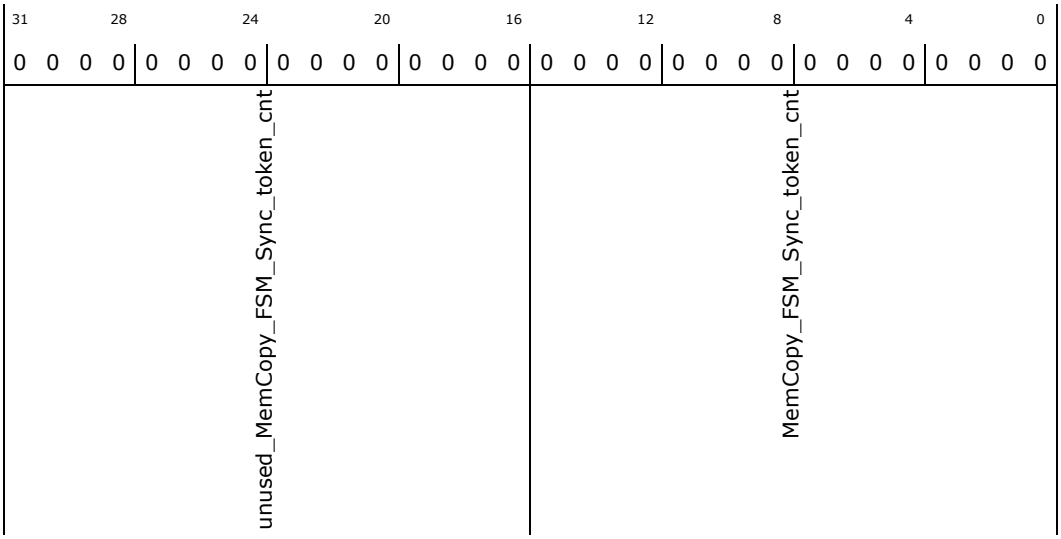
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt: [ISPMMADR] + 3070Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_MemCopy_FSM_Sync_token_cnt:** Unused
15:0	0h RO	**MemCopy_FSM_Sync_token_cnt:** FSM Synchronization token amount: counts the number of token processed

3.7.222 reg_ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt)—Offset 30710h

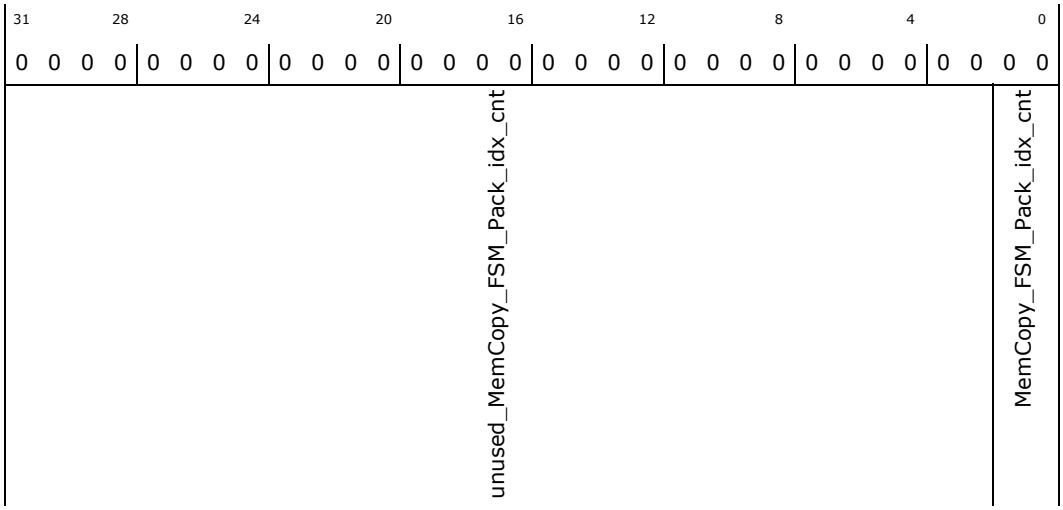
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt: [ISPMMADR] + 30710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_MemCopy_FSM_Pack_idx_cnt:** Unused
1:0	0h RO	**MemCopy_FSM_Pack_idx_cnt:** FSM Pack idx counter: element index

3.7.223 reg_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status_type (ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status)—Offset 30714h

Buffer Full and mask

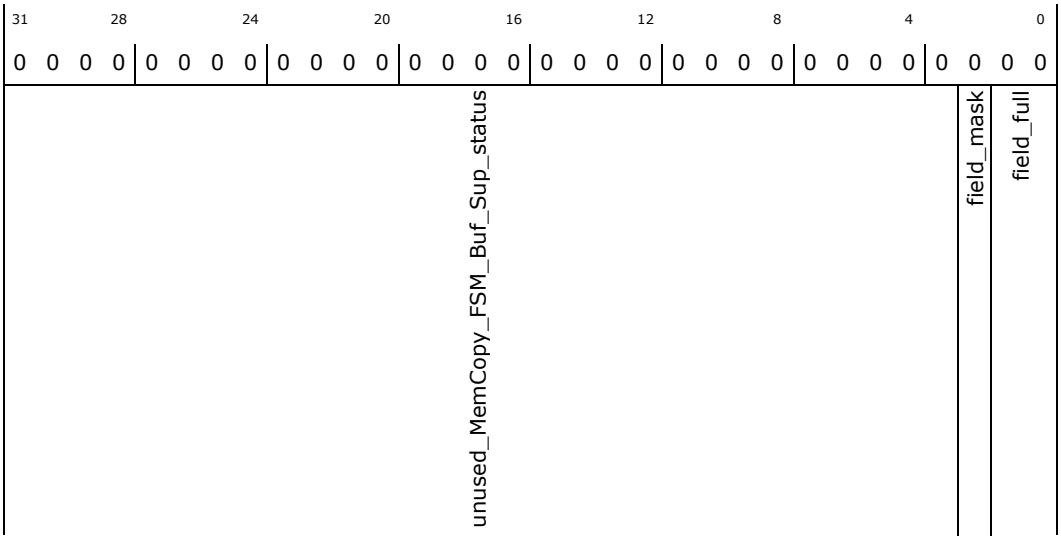
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status: [ISPMMADR] + 30714h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_MemCopy_FSM_Buf_Sup_status:** Unused
2	0h RO	**field_mask:** FSM Buffer support mask buffers full to the FSM CioWr
1:0	0h RO	**field_full:** FSM Buffer support one-hot encoding flagging when the buffer are full

3.7.224 reg_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt)—Offset 30718h

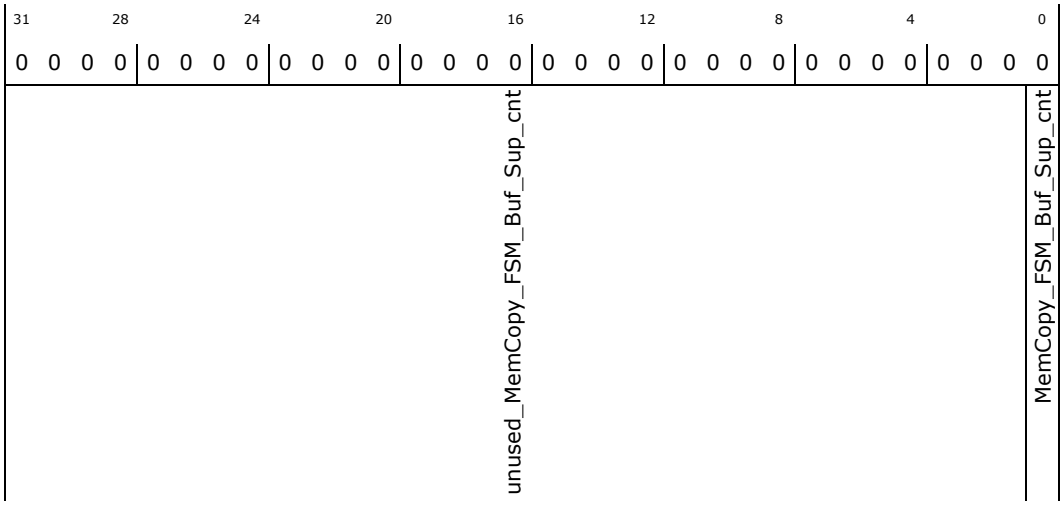
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt: [ISPMMADR] + 30718h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_FSM_Buf_Sup_cnt:** Unused
0	0h RO	**MemCopy_FSM_Buf_Sup_cnt:** FSM Buffer support: counter for buffer index

3.7.225 reg_ifmt_mem_cpy_MemCopy_FSM_CioWr_status_type (ifmt_mem_cpy_MemCopy_FSM_CioWr_status)—Offset 3071Ch

FSM CioWr Status

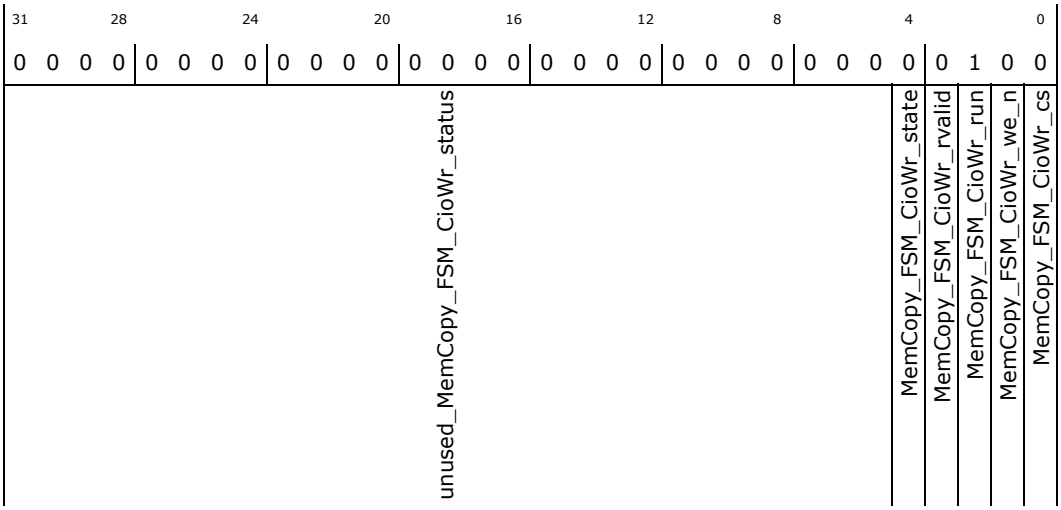
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_CioWr_status: [ISPMMADR] + 3071Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_MemCopy_FSM_CioWr_status:** Unused
4	0h RO	**MemCopy_FSM_CioWr_state:** 0)Idle - 1)Writing
3	0h RO	**MemCopy_FSM_CioWr_rvalid:** Read valid flag
2	1h RO	**MemCopy_FSM_CioWr_run:** Run flag
1	0h RO	**MemCopy_FSM_CioWr_we_n:** Write enable flag, active low
0	0h RO	**MemCopy_FSM_CioWr_cs:** CS flag

3.7.226 reg_ifmt_mem_cpy_MemCopy_FSM_CioWr_addr_type (ifmt_mem_cpy_MemCopy_FSM_CioWr_addr)—Offset 30720h

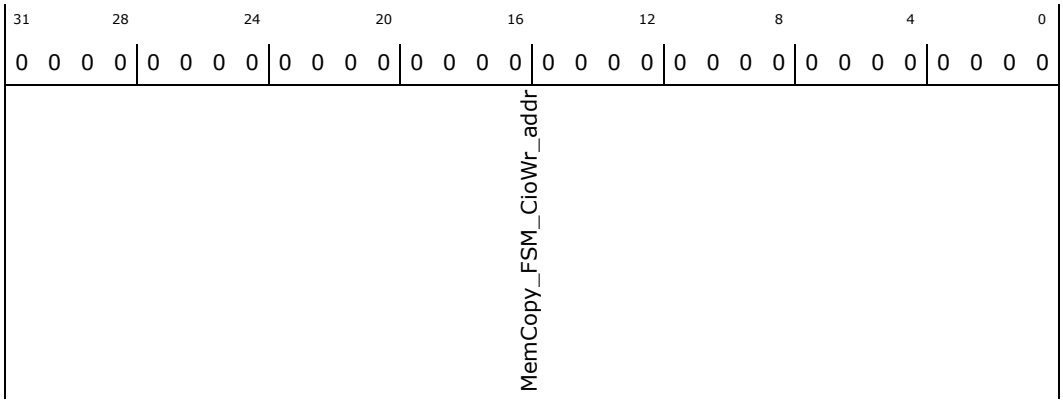
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_CioWr_addr: [ISPMMADR] + 30720h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**MemCopy_FSM_CioWr_addr:** FSM CioWr: write address in byte

3.7.227 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg0_type (ifmt_gp_reg_IFMT_input_switch_lut_reg0)—Offset 30800h

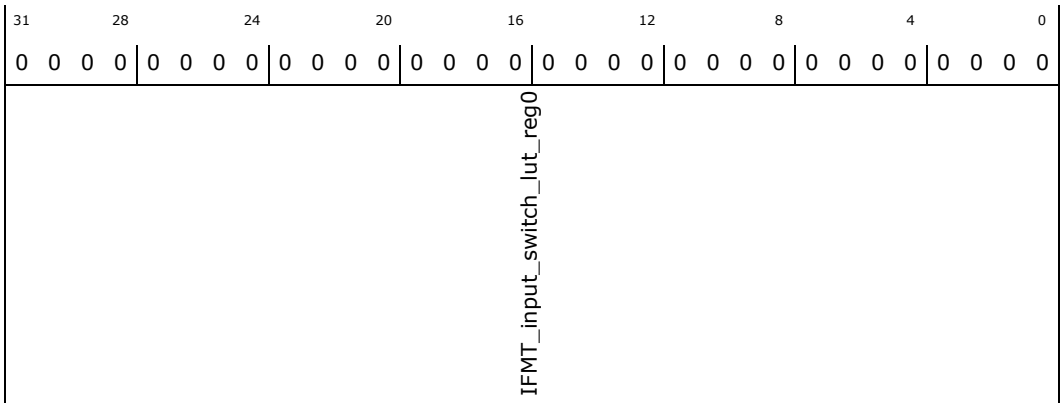
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg0: [ISPMMADR] + 30800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg0:** GP reg input switch data and hsync look-up table Register 0

3.7.228 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg1_type (ifmt_gp_reg_IFMT_input_switch_lut_reg1)—Offset 30804h

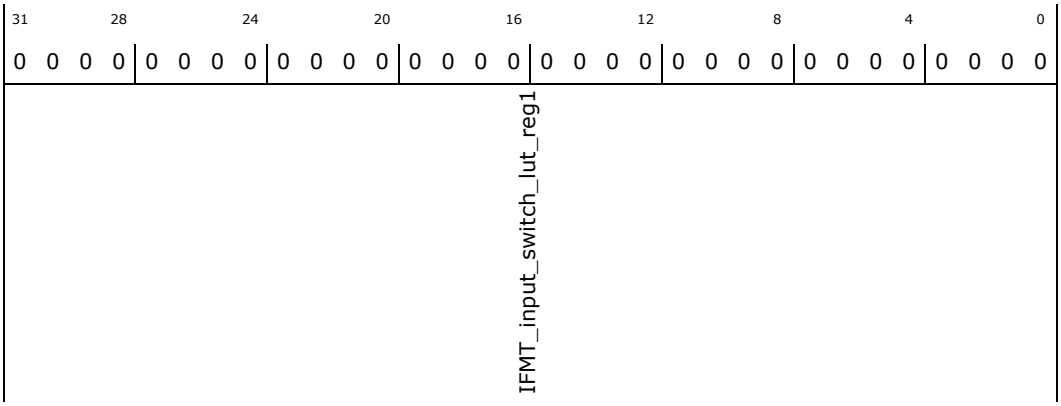
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg1: [ISPMMADR] + 30804h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg1:** GP reg input switch data and hsync look-up table Register 1

3.7.229 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg2_type (ifmt_gp_reg_IFMT_input_switch_lut_reg2)—Offset 30808h

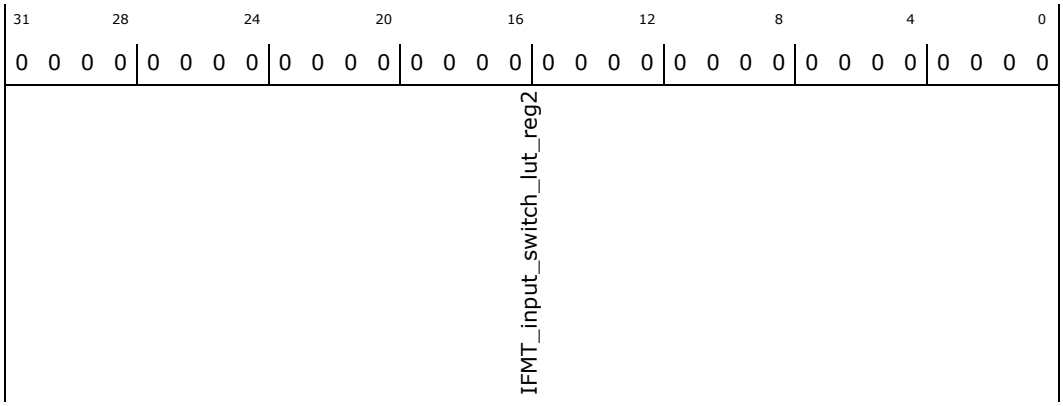
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg2: [ISPMMADR] + 30808h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg2:** GP reg input switch data and hsync look-up table Register 2

3.7.230 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg3_type (ifmt_gp_reg_IFMT_input_switch_lut_reg3)—Offset 3080Ch

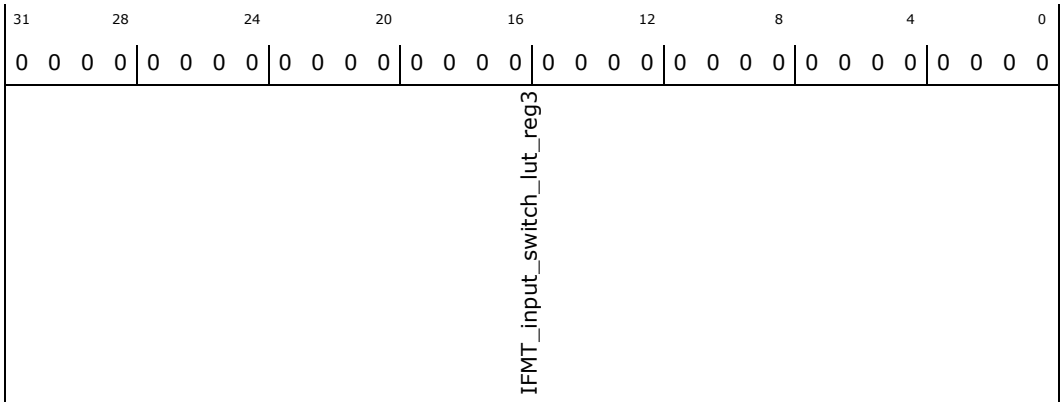
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg3: [ISPMMADR] + 3080Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg3:** GP reg input switch data and hsync look-up table Register 3

3.7.231 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg4_type (ifmt_gp_reg_IFMT_input_switch_lut_reg4)—Offset 30810h

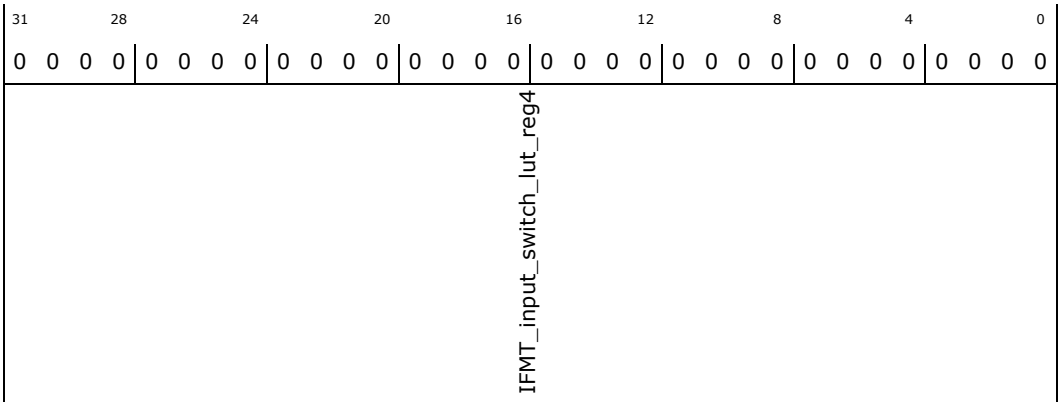
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg4: [ISPMMADR] + 30810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg4:** GP reg input switch data and hsync look-up table Register 4

3.7.232 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg5_type (ifmt_gp_reg_IFMT_input_switch_lut_reg5)—Offset 30814h

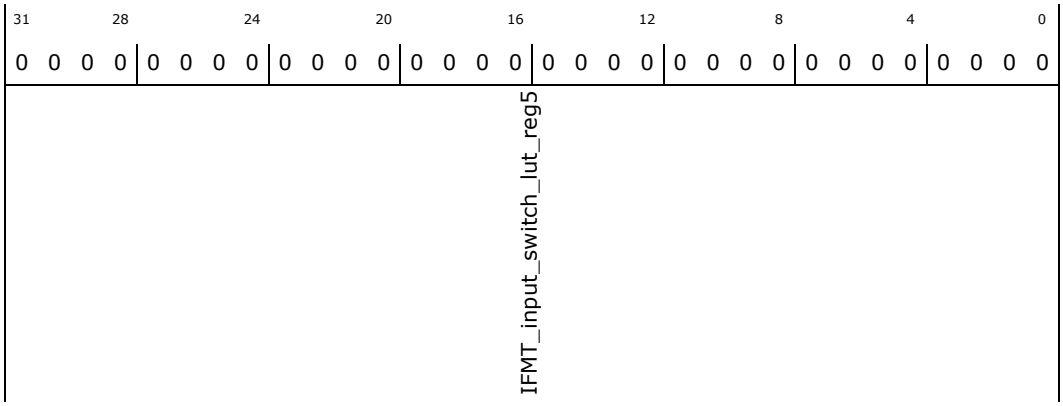
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg5: [ISPMMADR] + 30814h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg5:** GP reg input switch data and hsync look-up table Register 5

3.7.233 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg6_type (ifmt_gp_reg_IFMT_input_switch_lut_reg6)—Offset 30818h

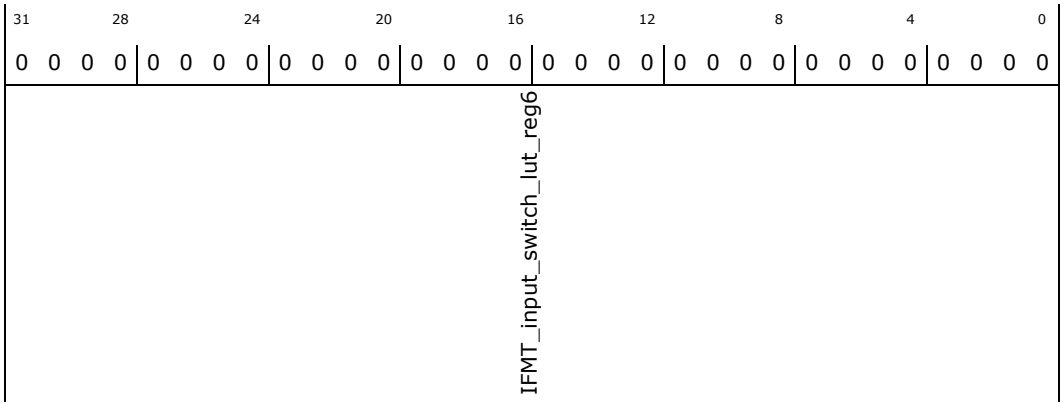
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg6: [ISPMMADR] + 30818h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg6:** GP reg input switch data and hsync look-up table Register 6

3.7.234 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg7_type (ifmt_gp_reg_IFMT_input_switch_lut_reg7)—Offset 3081Ch

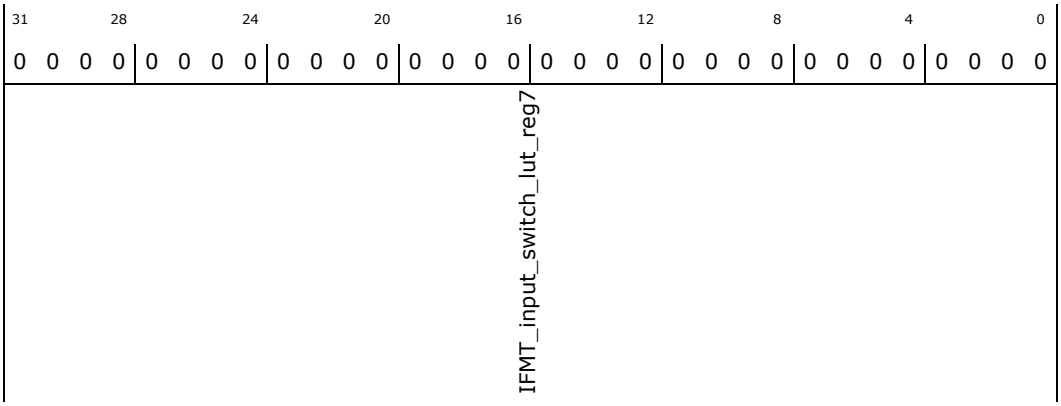
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg7: [ISPMMADR] + 3081Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg7:** GP reg input switch data and hsync look-up table Register 7

3.7.235 reg_ifmt_gp_reg_IFMT_input_switch_fsync_lut_type (ifmt_gp_reg_IFMT_input_switch_fsync_lut)—Offset 30820h

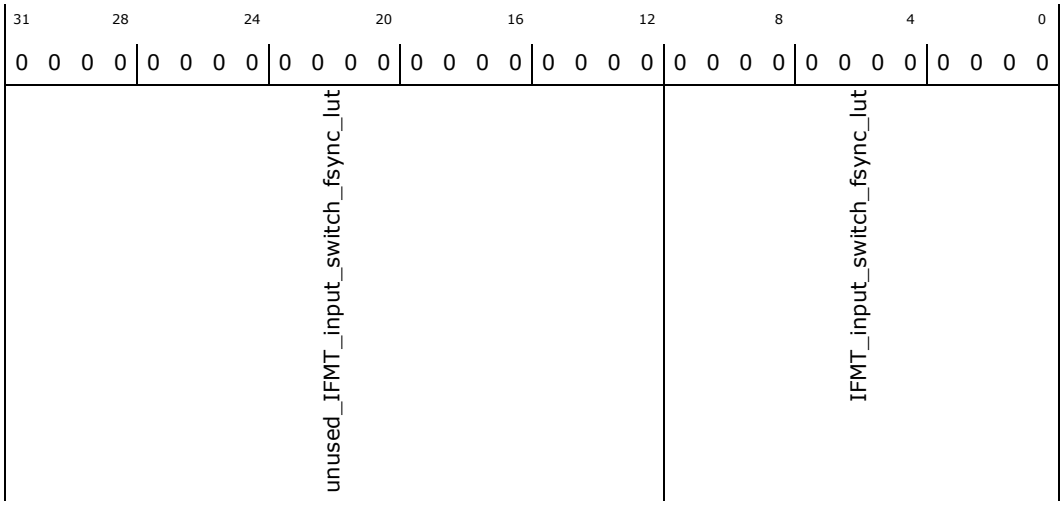
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_fsync_lut: [ISPMMADR] + 30820h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_IFMT_input_switch_fsync_lut:** Unused
11:0	0h RW	**IFMT_input_switch_fsync_lut:** GP reg input switch frame synchronization signal look-up table register

3.7.236 reg_ifmt_gp_reg_IFMT_srst_type (ifmt_gp_reg_IFMT_srst)—Offset 30824h

GP reg soft reset

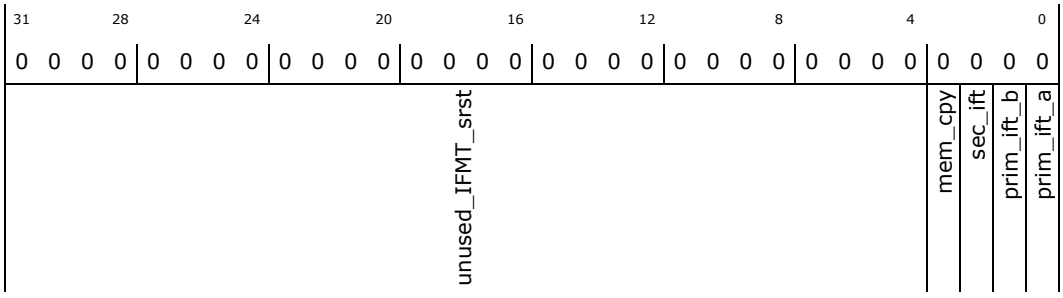
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_srst: [ISPMMADR] + 30824h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IFMT_srst:** Unused
3	0h RW	**mem_cpy:** Soft resets mem copy
2	0h RW	**sec_ift:** Soft resets secondary input formatter
1	0h RW	**prim_ift_b:** Soft resets primary input formatter B
0	0h RW	**prim_ift_a:** Soft resets primary input formatter A

3.7.237 reg_ifmt_gp_reg_IFMT_slv_reg_srst_type (ifmt_gp_reg_IFMT_slv_reg_srst)—Offset 30828h

GP reg slave register soft reset

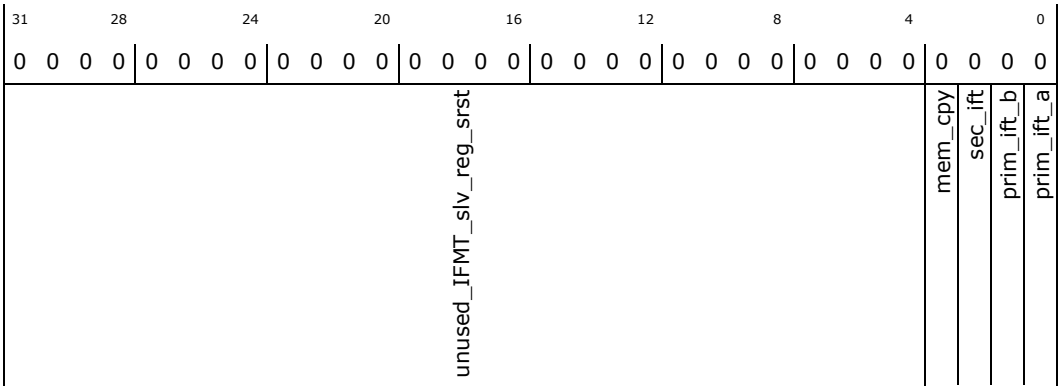
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_slv_reg_srst: [ISPMMADR] + 30828h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_IFMT_slv_reg_srst:** Unused
3	0h RW	**mem_cpy:** Soft resets slave registers of mem copy
2	0h RW	**sec_ift:** Soft resets slave registers of secondary input formatter
1	0h RW	**prim_ift_b:** Soft resets slave registers of primary input formatter B

Bit Range	Default & Access	Description
0	0h RW	**prim_ift_a:** Soft resets slave registers of primary input formatter A

3.7.238 reg_ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type_type (ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type)—Offset 3082Ch

GP reg input switch status register

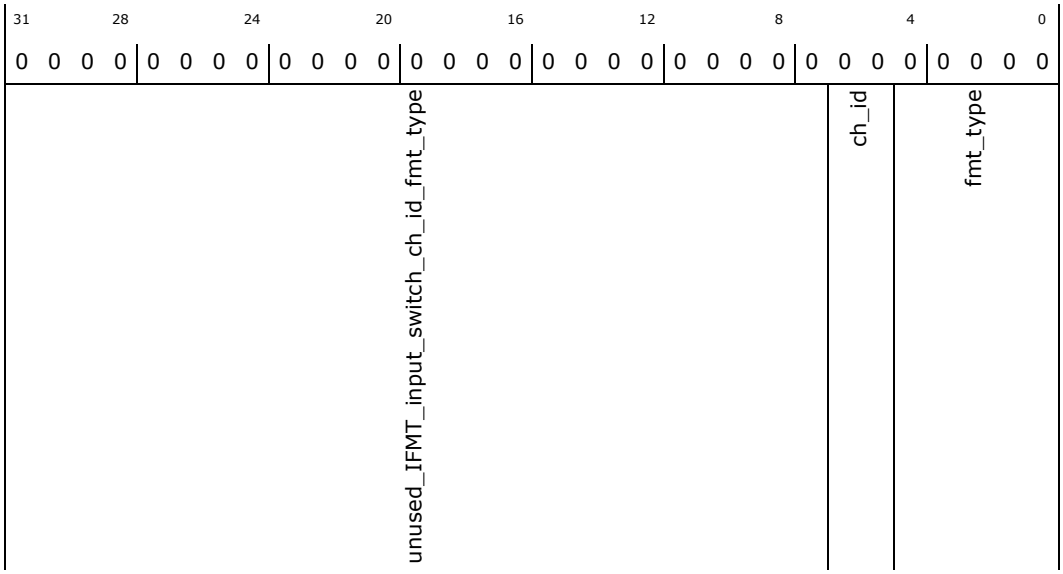
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type: [ISPMMADR] + 3082Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**unused_IFMT_input_switch_ch_id_fmt_type:** Unused
6:5	0h RO	**ch_id:** Returns the channel id as it arrives at the input of the input switch
4:0	0h RO	**fmt_type:** Returns the format type as it arrives at the input of the input switch

3.7.239 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge)—Offset 30A00h

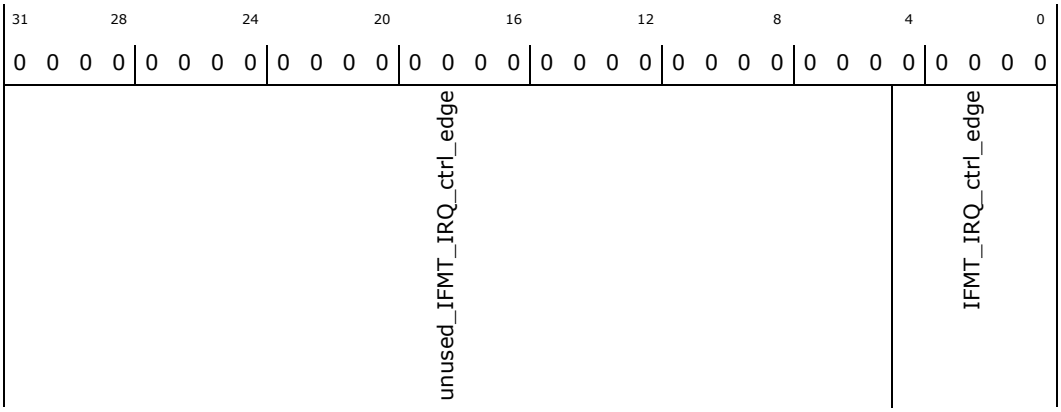
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge: [ISPMMADR] + 30A00h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_edge:** Unused
4:0	0h RW	**IFMT_IRQ_ctrl_edge:** indicates for each irq bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

3.7.240 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask)—Offset 30A04h

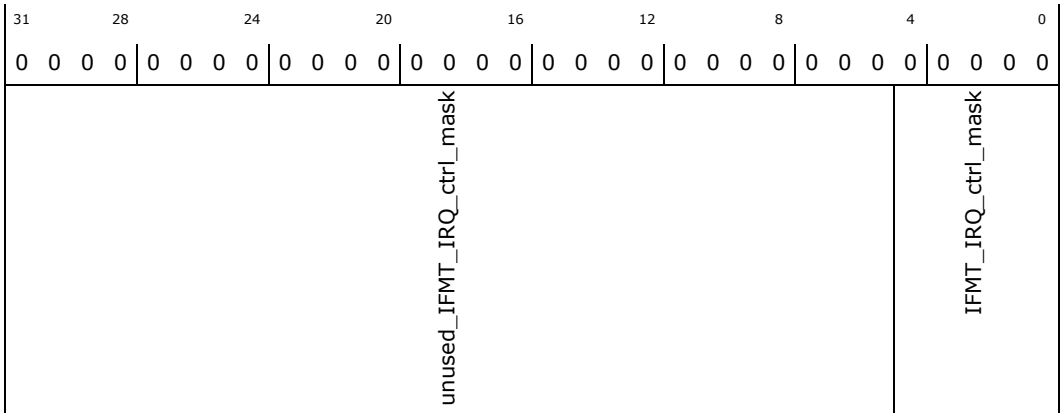
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask: [ISPMMADR] + 30A04h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_mask:** Unused
4:0	0h RW	**IFMT_IRQ_ctrl_mask:** indicates for each irq bit whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

3.7.241 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_status_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_status)—Offset 30A08h

IRQ controller STATUS

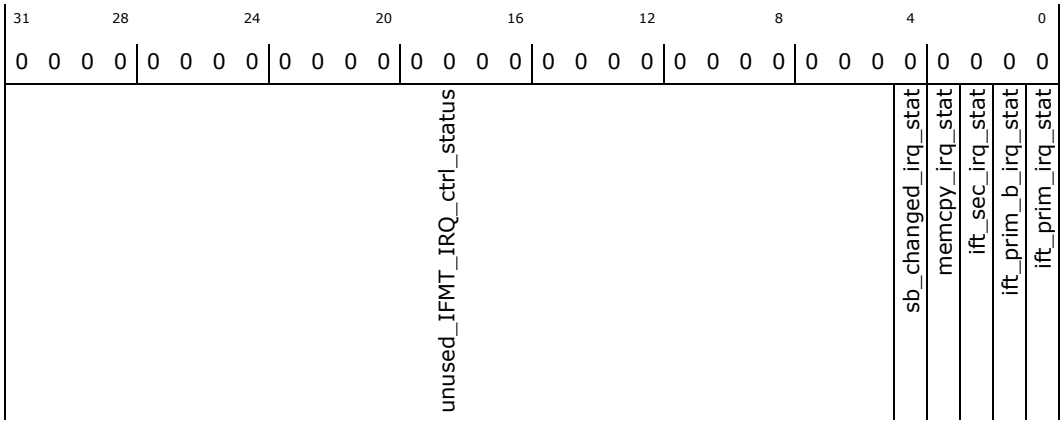
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_status: [ISPMMADR] + 30A08h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_status:** Unused
4	0h RO	**sb_changed_irq_stat:** Returns the status of the irq signal indicating a change in either the channel id or the format type
3	0h RO	**memcpy_irq_stat:** Returns the status of the irq generated by the stream to memory device
2	0h RO	**ift_sec_irq_stat:** Returns the status of the irq generated by the secondary input formatter
1	0h RO	**ift_prim_b_irq_stat:** Returns the status of the irq generated by the primary input formatter b
0	0h RO	**ift_prim_irq_stat:** Returns the status of the irq generated by the primary input formatter

3.7.242 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear)—Offset 30A0Ch

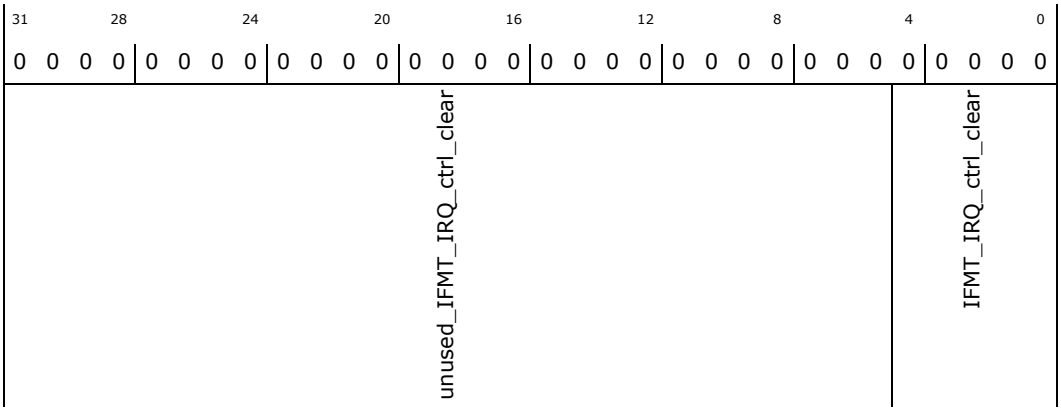
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear: [ISPMMADR] + 30A0Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_clear:** Unused
4:0	0h WO	**IFMT_IRQ_ctrl_clear:** Clears (set to '0') bits in IFMT_IRQ_ctrl_status. When writing a '1' into a bit of this register, the corresponding bit in the IFMT_IRQ_ctrl_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the IFMT_IRQ_ctrl_status is not affected.

3.7.243 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable)—Offset 30A10h

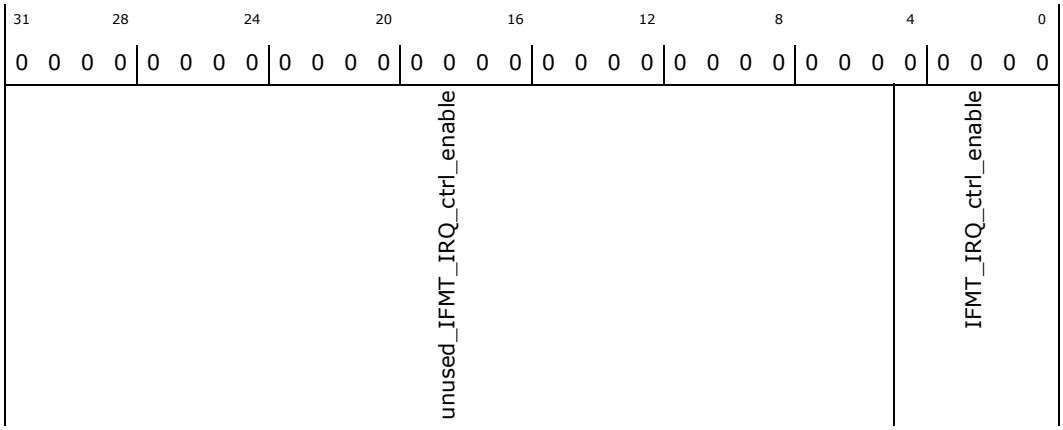
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable: [ISPMMADR] + 30A10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_enable:** Unused
4:0	0h RW	**IFMT_IRQ_ctrl_enable:** Indicates for each bit whether an interrupt cause as monitored by the IFMT_IRQ_ctrl_status register also affects the IRQ pin (value='1') or not (value='0')

3.7.244 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse)—Offset 30A14h

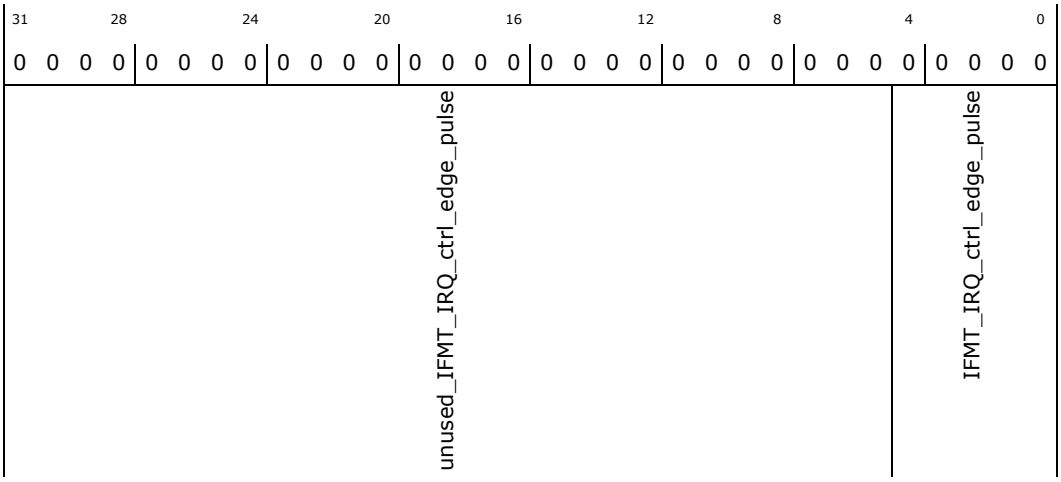
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse: [ISPMMADR] + 30A14h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_edge_pulse:** Unused
4:0	0h RW	**IFMT_IRQ_ctrl_edge_pulse:** Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

3.7.245 reg_isp_dma_DMA_FSM_Command_type (isp_dma_DMA_FSM_Command)—Offset 40000h

FSM Command: Last command and State

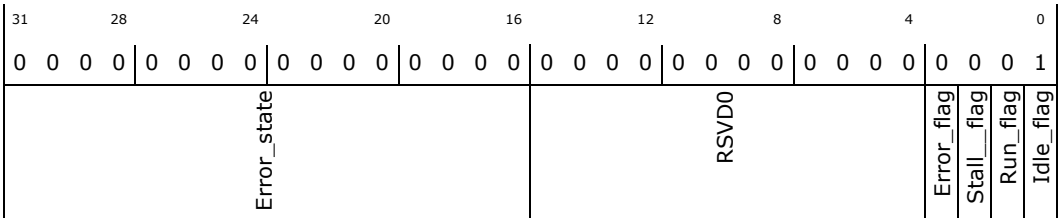
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Command: [ISPMMADR] + 40000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0h RO	**Error_state:** Lower 16 bits of the last command received and processed

Bit Range	Default & Access	Description
15:4	0b RO	**RSVD0:** Reserved
3	0h RO	**Error_flag:** Error flag
2	0h RO	**Stall__flag:** Stall flag
1	0h RO	**Run_flag:** Run flag
0	1h RO	**Idle_flag:** Idle flag

3.7.246 reg_isp_dma_DMA_CH0_Packing_setup_type (isp_dma_DMA_CH0_Packing_setup)—Offset 41000h

DMA CH 0 PARAM 0: Packing setup

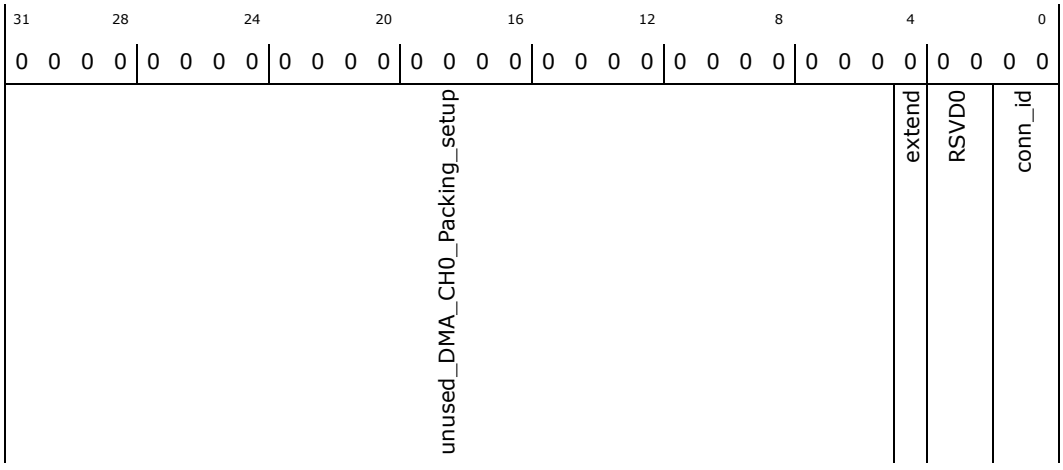
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_Packing_setup: [ISPMMADR] + 41000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH0_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
1:0	0h RO	**conn_id:** Connection ID

3.7.247 reg_isp_dma_DMA_CH1_Packing_setup_type (isp_dma_DMA_CH1_Packing_setup)—Offset 41004h

DMA CH 1 PARAM 0: Packing setup

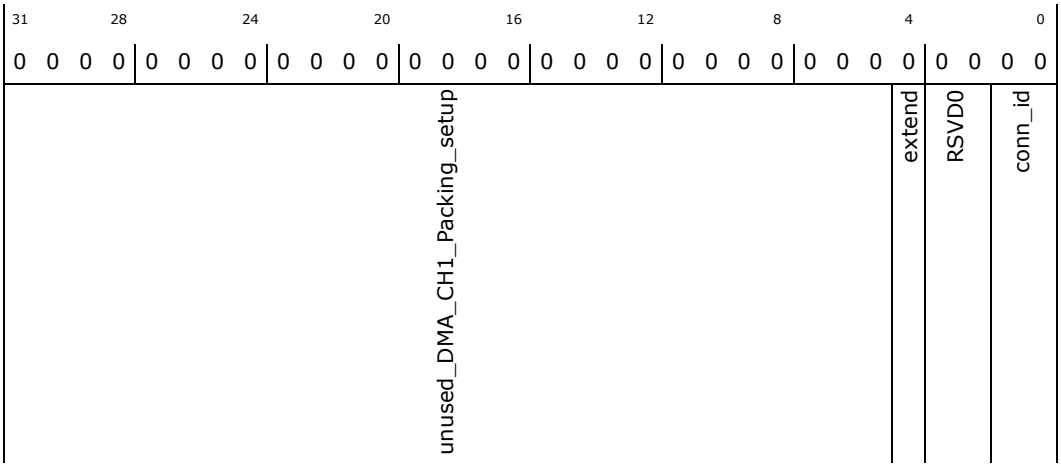
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_Packing_setup: [ISPMMADR] + 41004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH1_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.248 reg_isp_dma_DMA_CH2_Packing_setup_type (isp_dma_DMA_CH2_Packing_setup)—Offset 41008h

DMA CH 2 PARAM 0: Packing setup

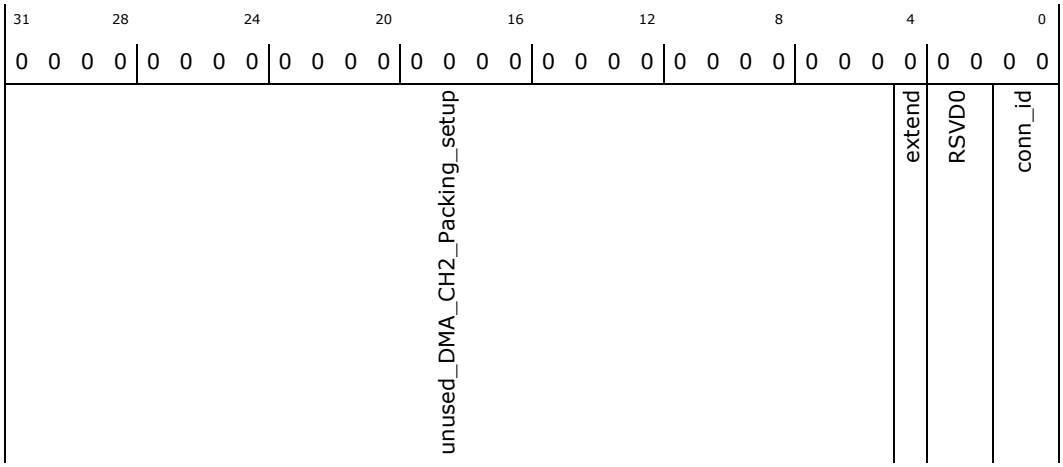
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_Packing_setup: [ISPMMADR] + 41008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH2_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.249 reg_isp_dma_DMA_CH3_Packing_setup_type (isp_dma_DMA_CH3_Packing_setup)—Offset 4100Ch

DMA CH 3 PARAM 0: Packing setup

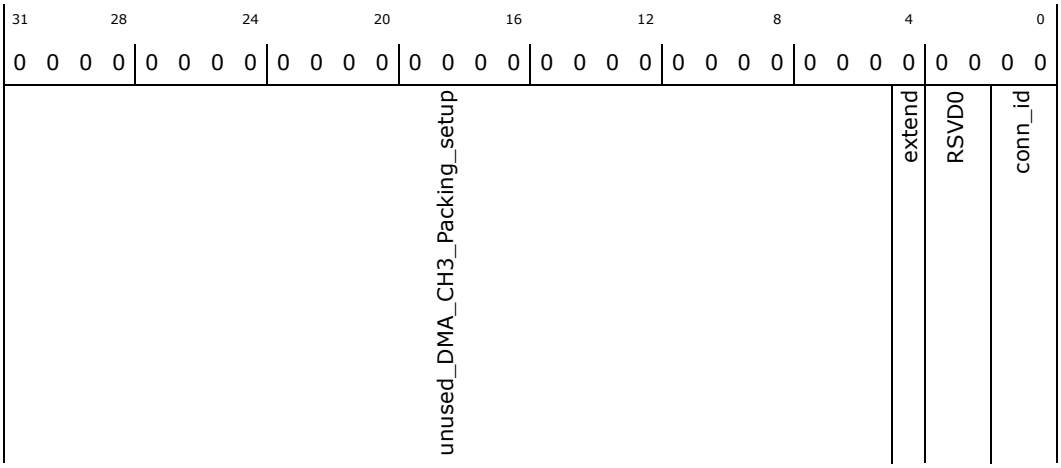
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_Packing_setup: [ISPMMADR] + 4100Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH3_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.250 reg_isp_dma_DMA_CH4_Packing_setup_type (isp_dma_DMA_CH4_Packing_setup)—Offset 41010h

DMA CH 4 PARAM 0: Packing setup

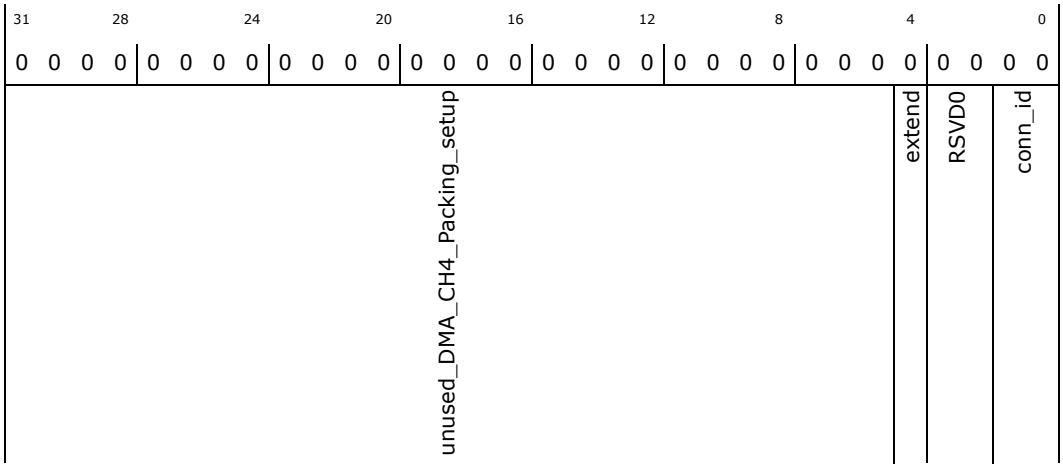
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_Packing_setup: [ISPMMADR] + 41010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH4_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.251 reg_isp_dma_DMA_CH5_Packing_setup_type (isp_dma_DMA_CH5_Packing_setup)—Offset 41014h

DMA CH 5 PARAM 0: Packing setup

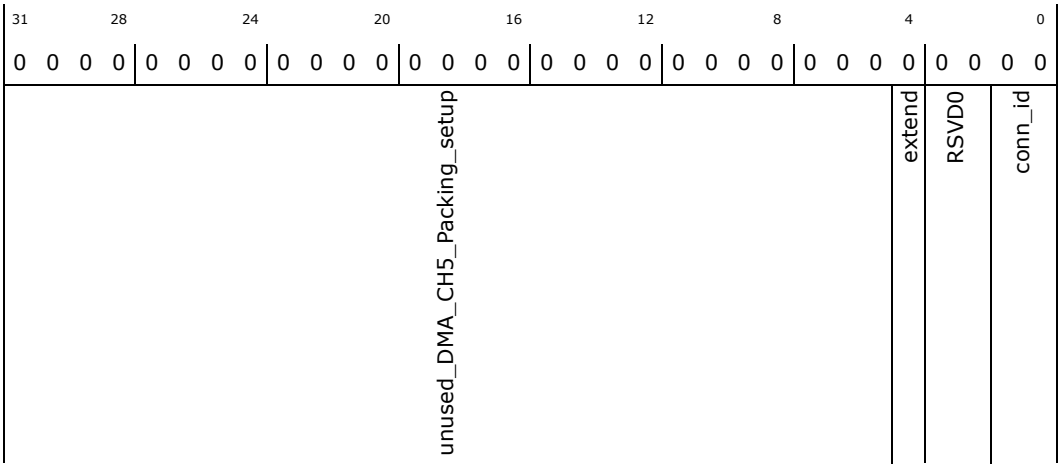
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_Packing_setup: [ISPMMADR] + 41014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH5_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.252 reg_isp_dma_DMA_CH6_Packing_setup_type (isp_dma_DMA_CH6_Packing_setup)—Offset 41018h

DMA CH 6 PARAM 0: Packing setup

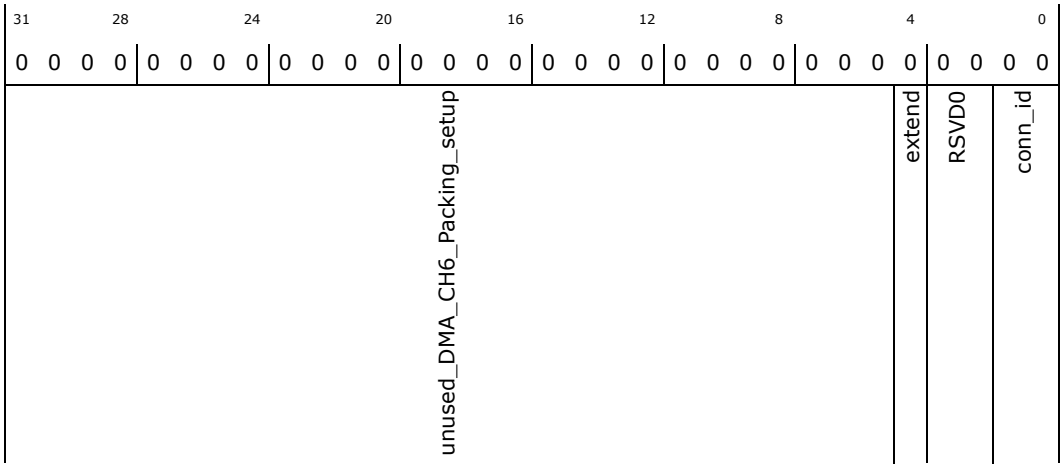
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_Packing_setup: [ISPMMADR] + 41018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH6_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.253 reg_isp_dma_DMA_CH7_Packing_setup_type (isp_dma_DMA_CH7_Packing_setup)—Offset 4101Ch

DMA CH 7 PARAM 0: Packing setup

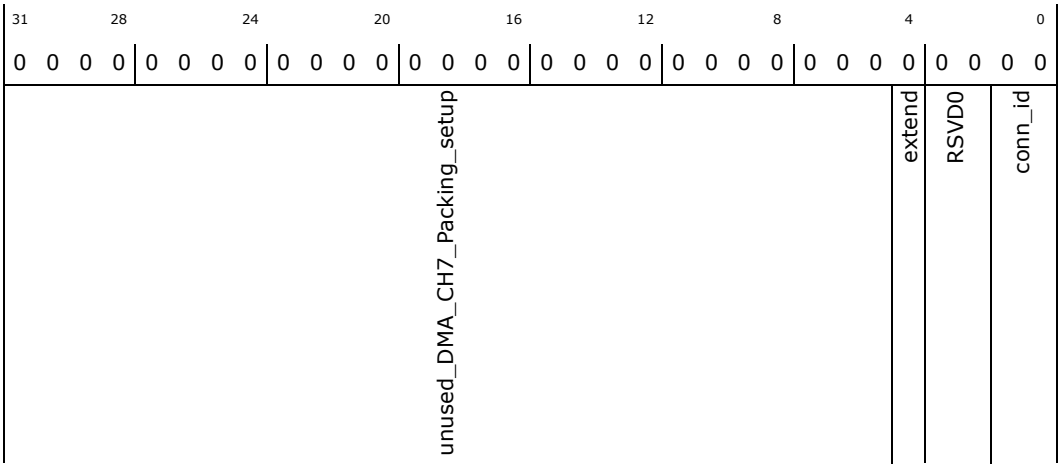
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_Packing_setup: [ISPMMADR] + 4101Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH7_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.254 reg_isp_dma_DMA_CH8_Packing_setup_type (isp_dma_DMA_CH8_Packing_setup)—Offset 41020h

DMA CH 8 PARAM 0: Packing setup

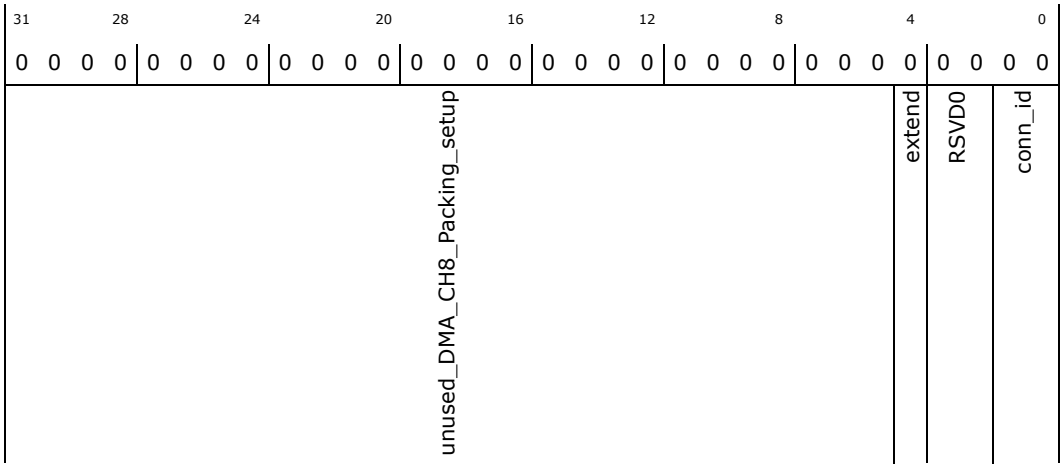
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_Packing_setup: [ISPMMADR] + 41020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH8_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.255 reg_isp_dma_DMA_CH9_Packing_setup_type (isp_dma_DMA_CH9_Packing_setup)—Offset 41024h

DMA CH 9 PARAM 0: Packing setup

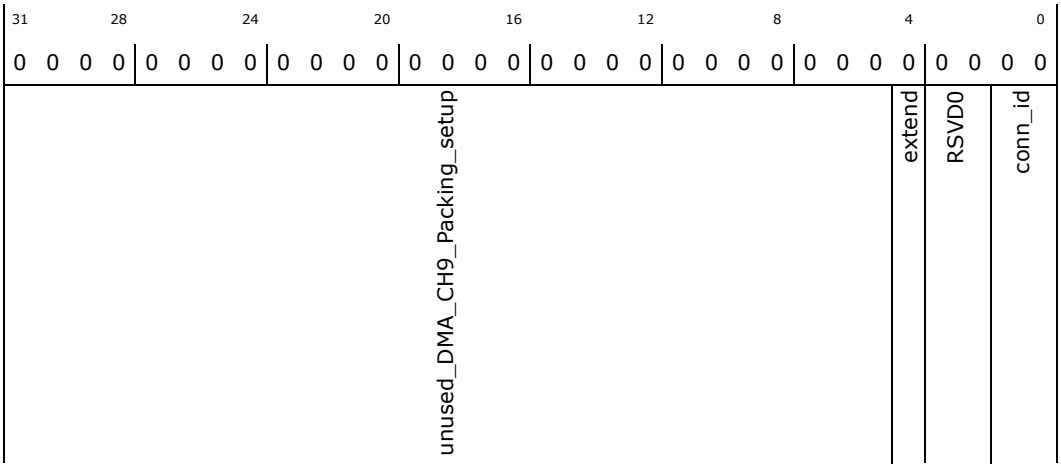
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_Packing_setup: [ISPMMADR] + 41024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH9_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.256 reg_isp_dma_DMA_CH10_Packing_setup_type (isp_dma_DMA_CH10_Packing_setup)—Offset 41028h

DMA CH 10 PARAM 0: Packing setup

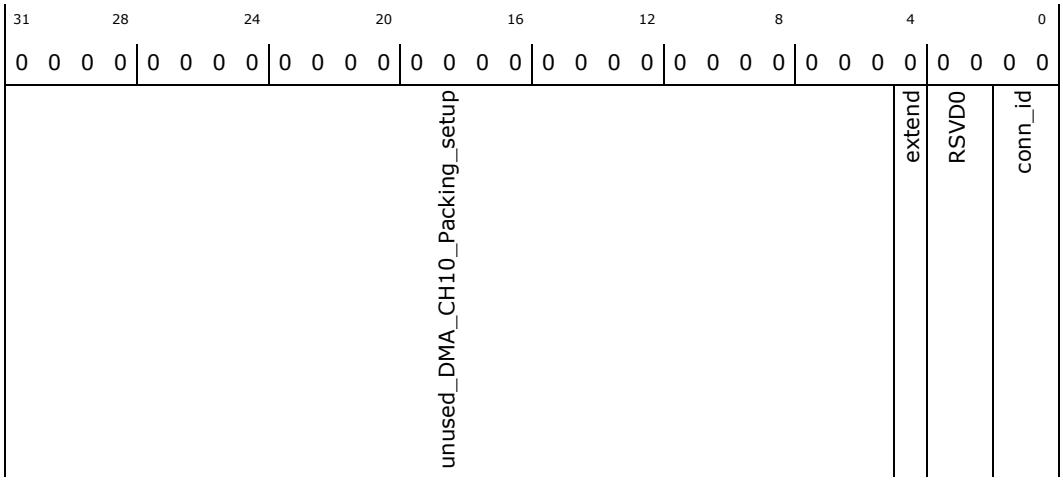
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_Packing_setup: [ISPMMADR] + 41028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH10_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.257 reg_isp_dma_DMA_CH11_Packing_setup_type (isp_dma_DMA_CH11_Packing_setup)—Offset 4102Ch

DMA CH 11 PARAM 0: Packing setup

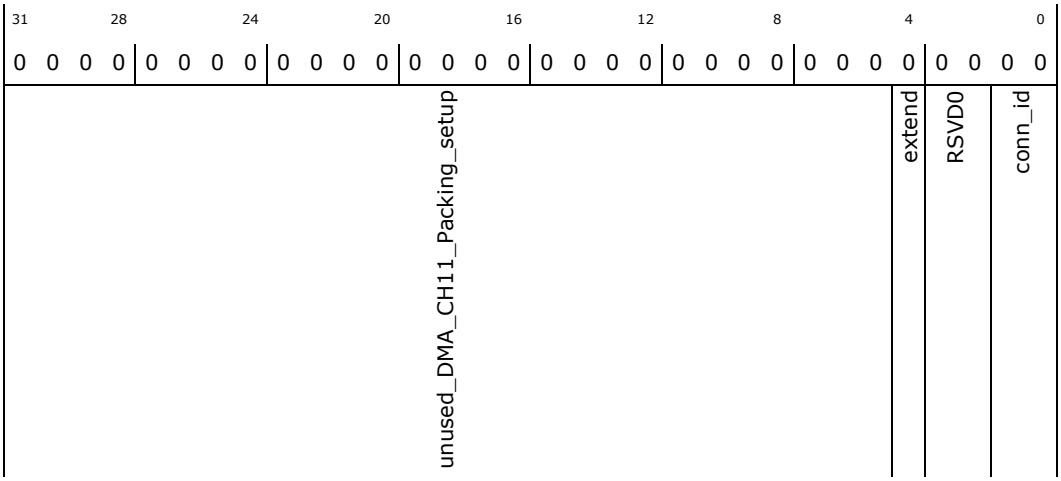
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_Packing_setup: [ISPMMADR] + 4102Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH11_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.258 reg_isp_dma_DMA_CH12_Packing_setup_type (isp_dma_DMA_CH12_Packing_setup)—Offset 41030h

DMA CH 12 PARAM 0: Packing setup

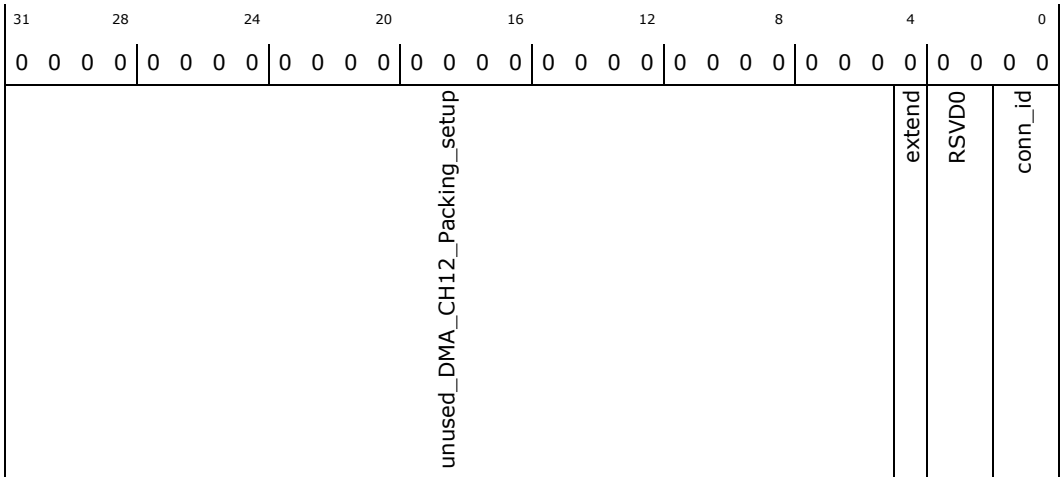
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_Packing_setup: [ISPMMADR] + 41030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH12_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.259 reg_isp_dma_DMA_CH13_Packing_setup_type (isp_dma_DMA_CH13_Packing_setup)—Offset 41034h

DMA CH 13 PARAM 0: Packing setup

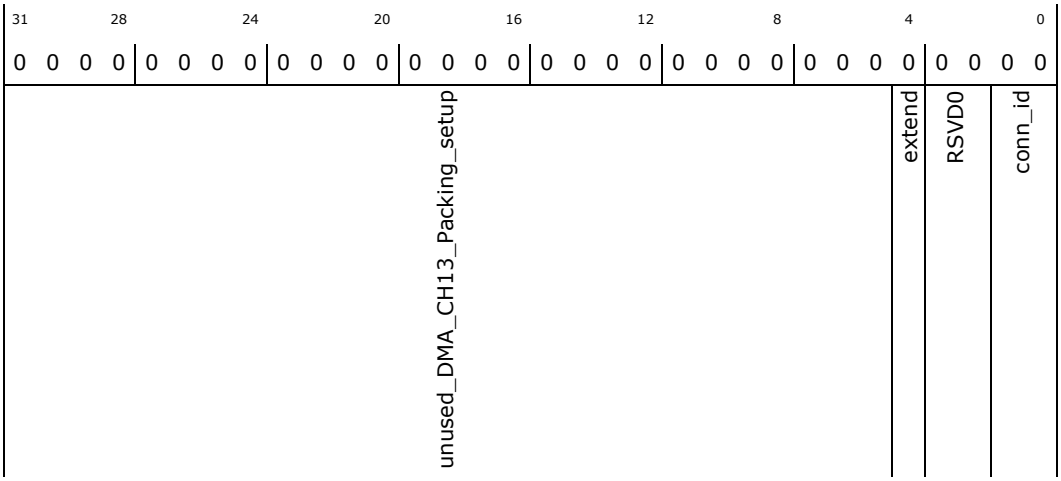
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_Packing_setup: [ISPMMADR] + 41034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH13_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.260 reg_isp_dma_DMA_CH14_Packing_setup_type (isp_dma_DMA_CH14_Packing_setup)—Offset 41038h

DMA CH 14 PARAM 0: Packing setup

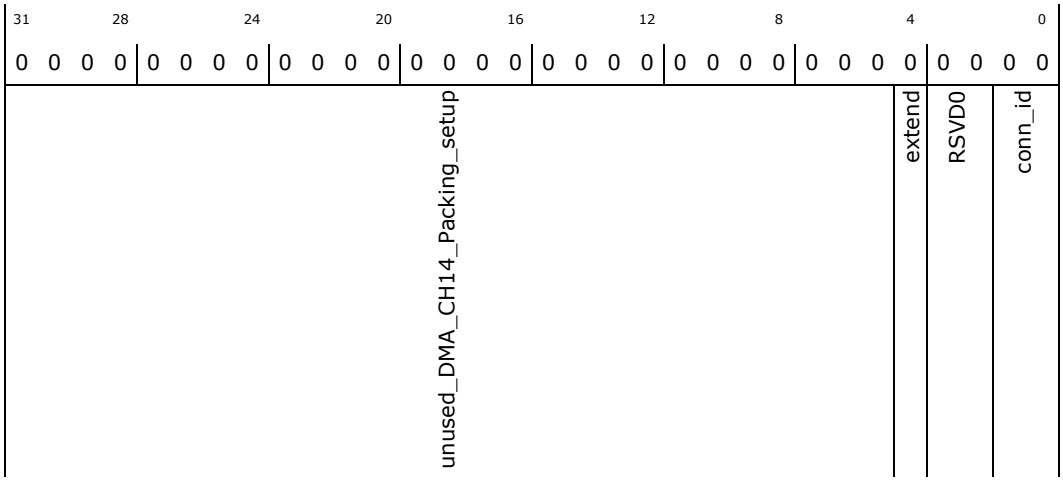
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_Packing_setup: [ISPMMADR] + 41038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH14_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.261 reg_isp_dma_DMA_CH15_Packing_setup_type (isp_dma_DMA_CH15_Packing_setup)—Offset 4103Ch

DMA CH 15 PARAM 0: Packing setup

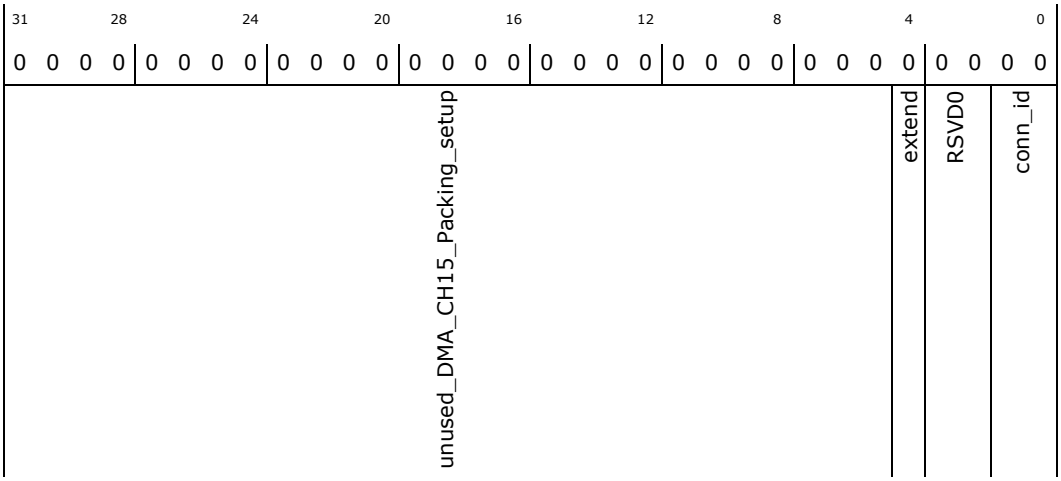
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_Packing_setup: [ISPMMADR] + 4103Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH15_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.262 reg_isp_dma_DMA_CH16_Packing_setup_type (isp_dma_DMA_CH16_Packing_setup)—Offset 41040h

DMA CH 16 PARAM 0: Packing setup

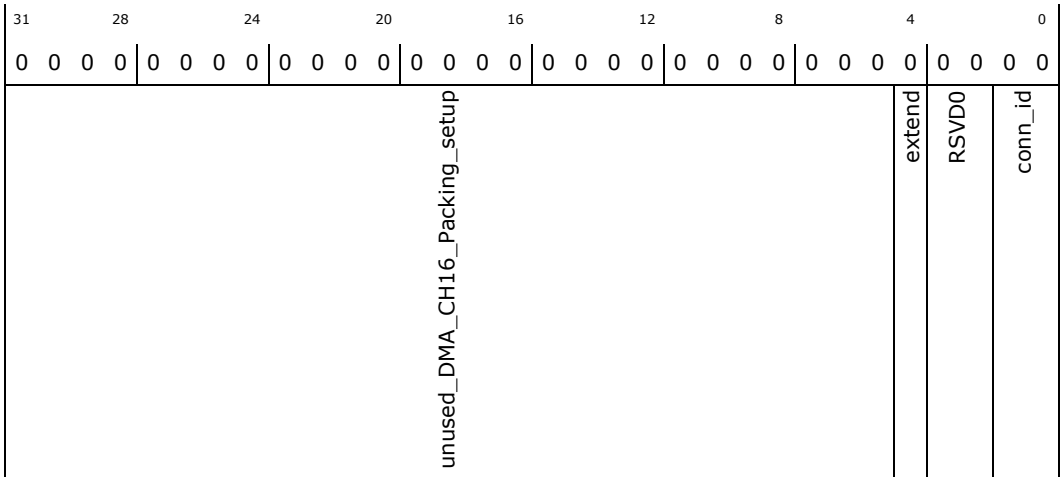
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_Packing_setup: [ISPMMADR] + 41040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH16_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.263 reg_isp_dma_DMA_CH17_Packing_setup_type (isp_dma_DMA_CH17_Packing_setup)—Offset 41044h

DMA CH 17 PARAM 0: Packing setup

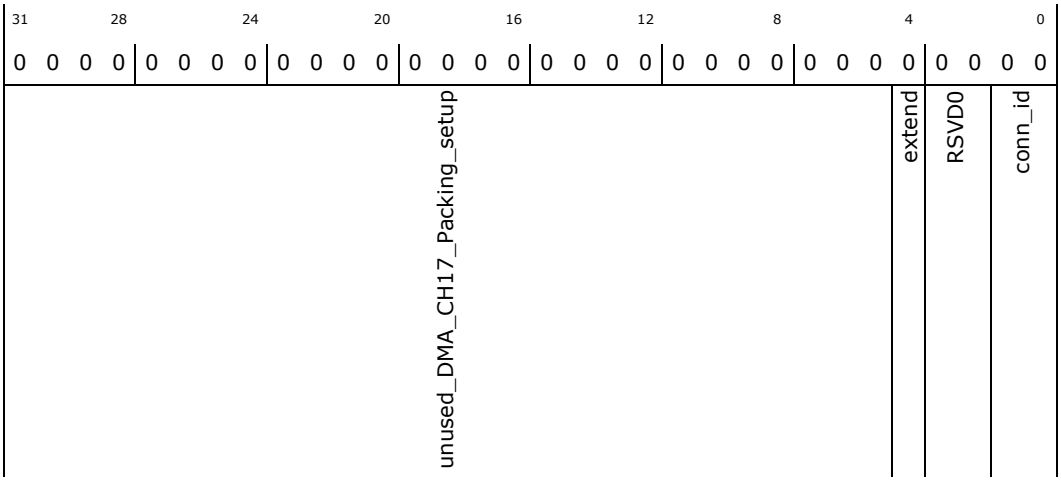
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_Packing_setup: [ISPMMADR] + 41044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH17_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.264 reg_isp_dma_DMA_CH18_Packing_setup_type (isp_dma_DMA_CH18_Packing_setup)—Offset 41048h

DMA CH 18 PARAM 0: Packing setup

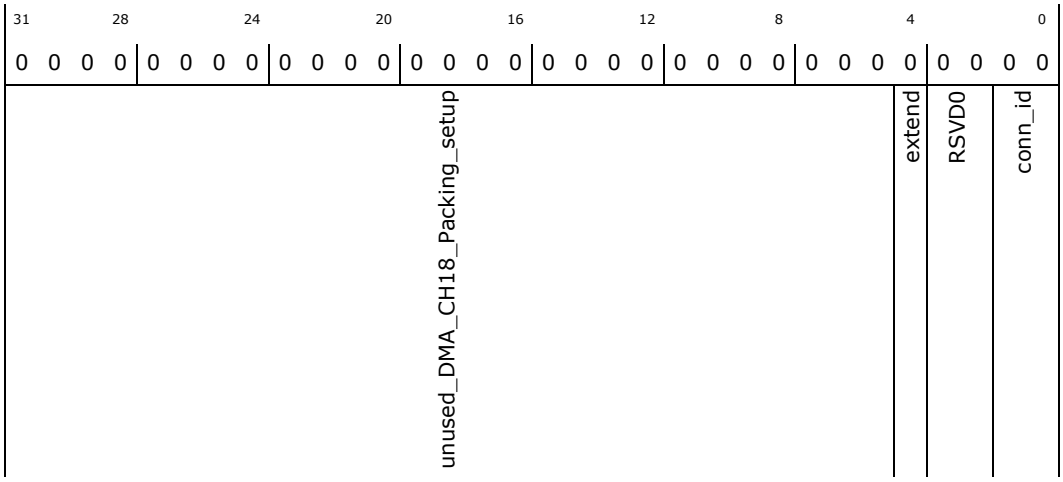
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_Packing_setup: [ISPMMADR] + 41048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH18_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.265 reg_isp_dma_DMA_CH19_Packing_setup_type (isp_dma_DMA_CH19_Packing_setup)—Offset 4104Ch

DMA CH 19 PARAM 0: Packing setup

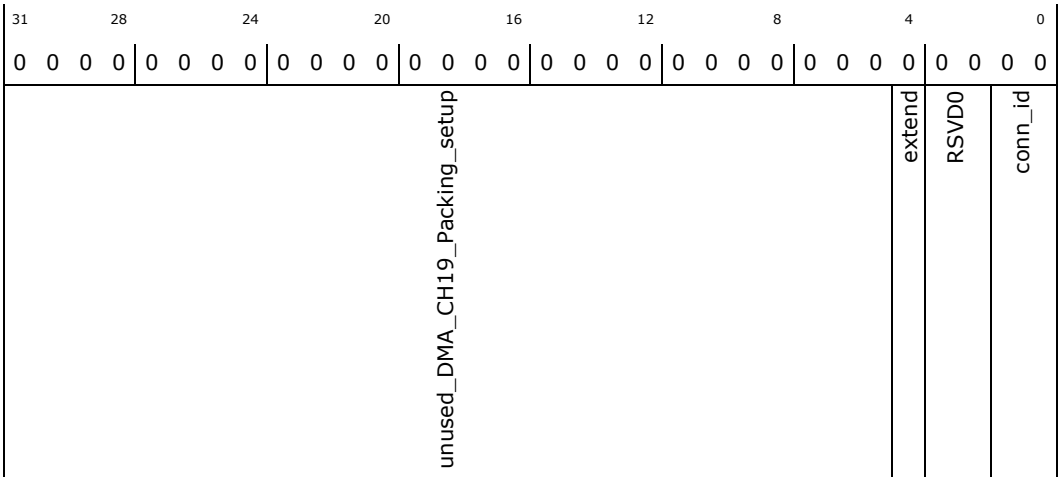
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_Packing_setup: [ISPMMADR] + 4104Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH19_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.266 reg_isp_dma_DMA_CH20_Packing_setup_type (isp_dma_DMA_CH20_Packing_setup)—Offset 41050h

DMA CH 20 PARAM 0: Packing setup

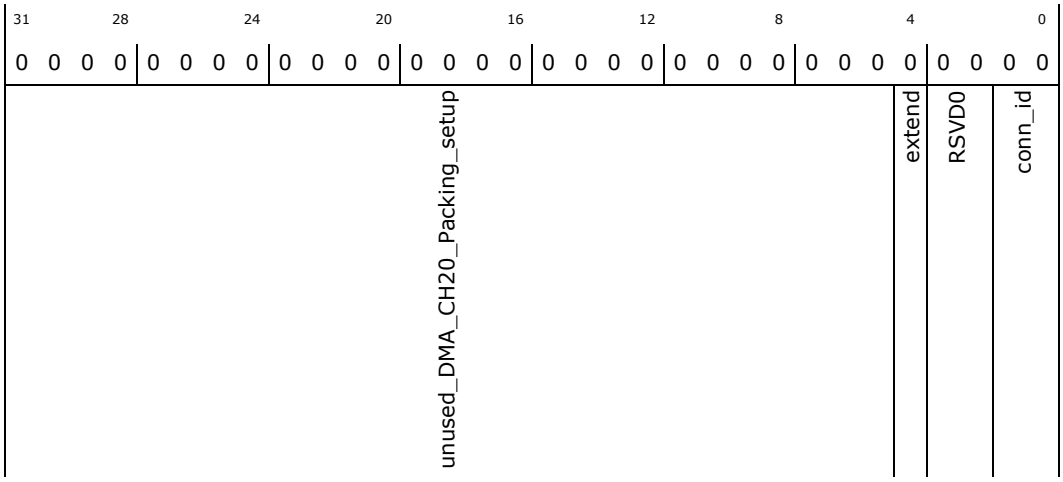
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_Packing_setup: [ISPMMADR] + 41050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH20_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.267 reg_isp_dma_DMA_CH21_Packing_setup_type (isp_dma_DMA_CH21_Packing_setup)—Offset 41054h

DMA CH 21 PARAM 0: Packing setup

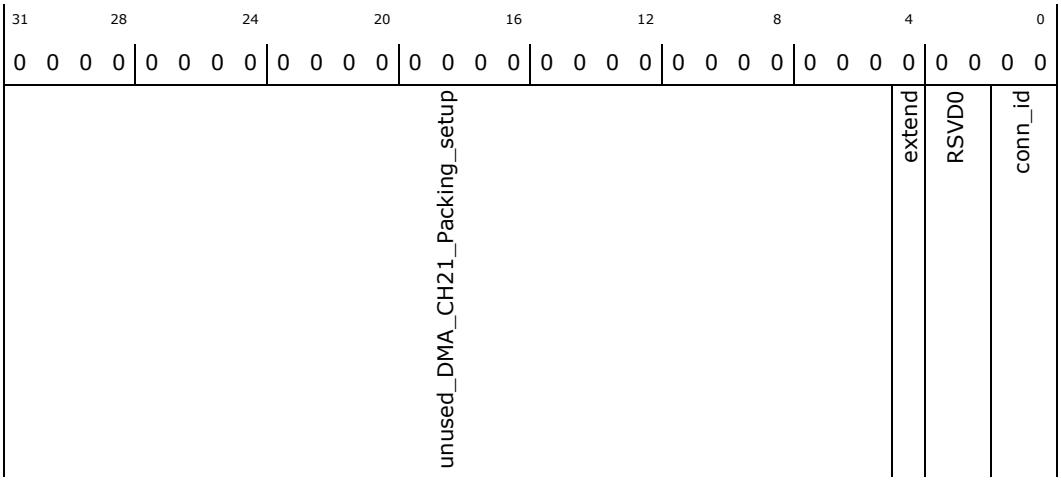
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_Packing_setup: [ISPMMADR] + 41054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH21_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.268 reg_isp_dma_DMA_CH22_Packing_setup_type (isp_dma_DMA_CH22_Packing_setup)—Offset 41058h

DMA CH 22 PARAM 0: Packing setup

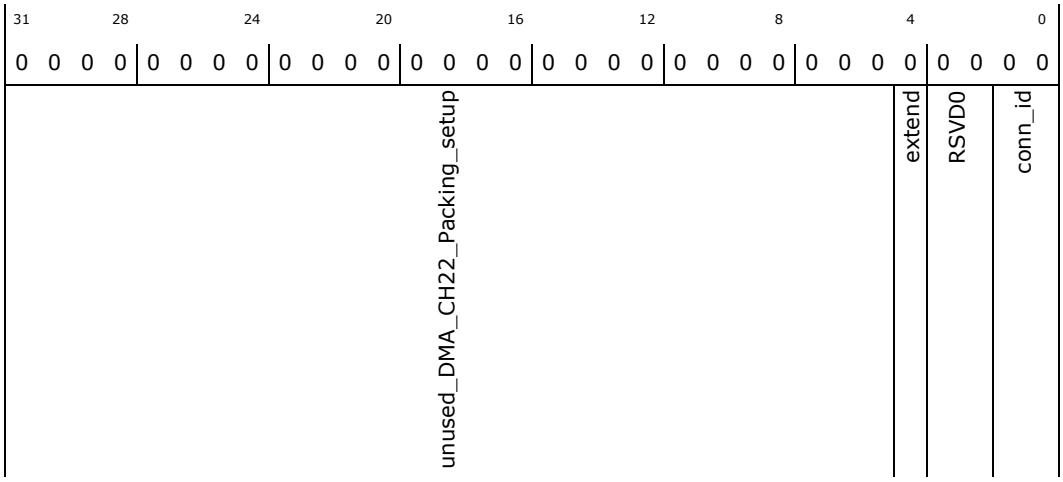
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_Packing_setup: [ISPMMADR] + 41058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH22_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.269 reg_isp_dma_DMA_CH23_Packing_setup_type (isp_dma_DMA_CH23_Packing_setup)—Offset 4105Ch

DMA CH 23 PARAM 0: Packing setup

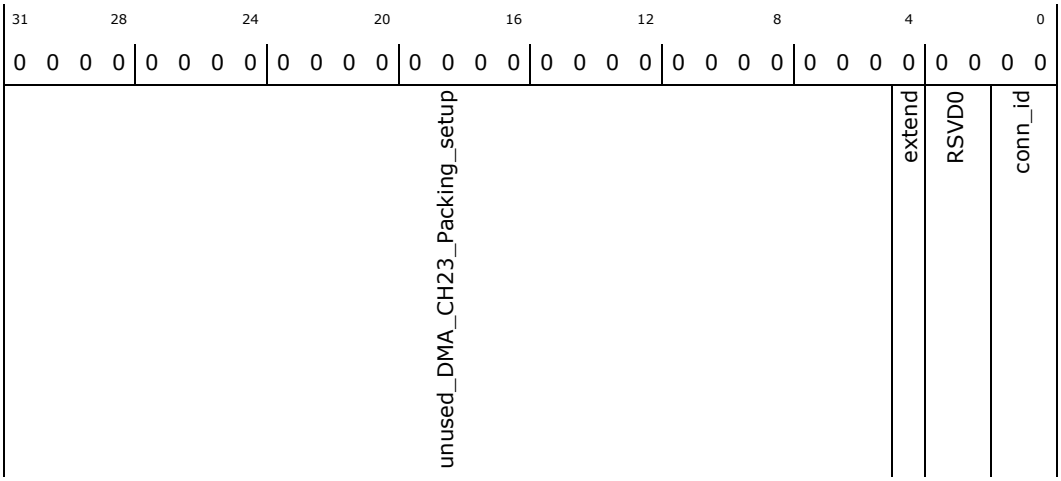
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_Packing_setup: [ISPMMADR] + 4105Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH23_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.270 reg_isp_dma_DMA_CH24_Packing_setup_type (isp_dma_DMA_CH24_Packing_setup)—Offset 41060h

DMA CH 24 PARAM 0: Packing setup

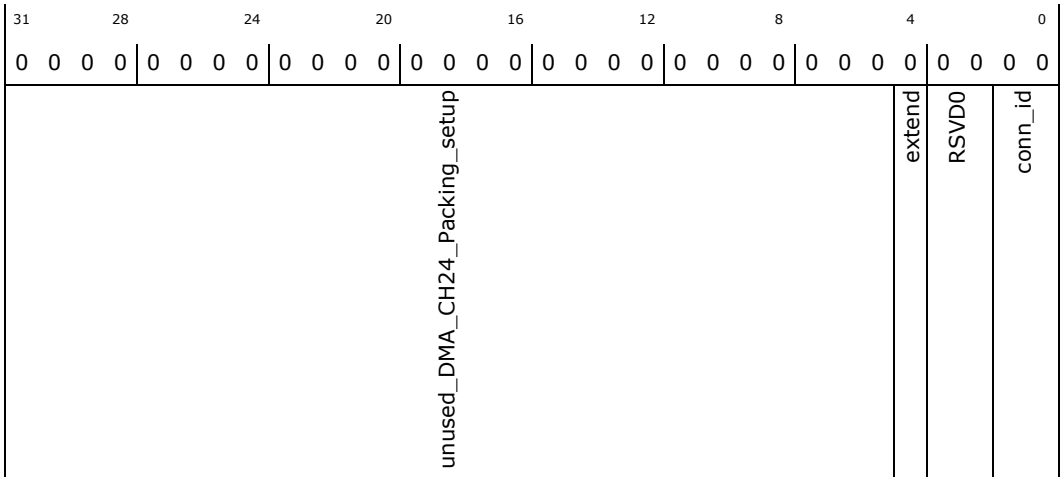
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_Packing_setup: [ISPMMADR] + 41060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH24_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.271 reg_isp_dma_DMA_CH25_Packing_setup_type (isp_dma_DMA_CH25_Packing_setup)—Offset 41064h

DMA CH 25 PARAM 0: Packing setup

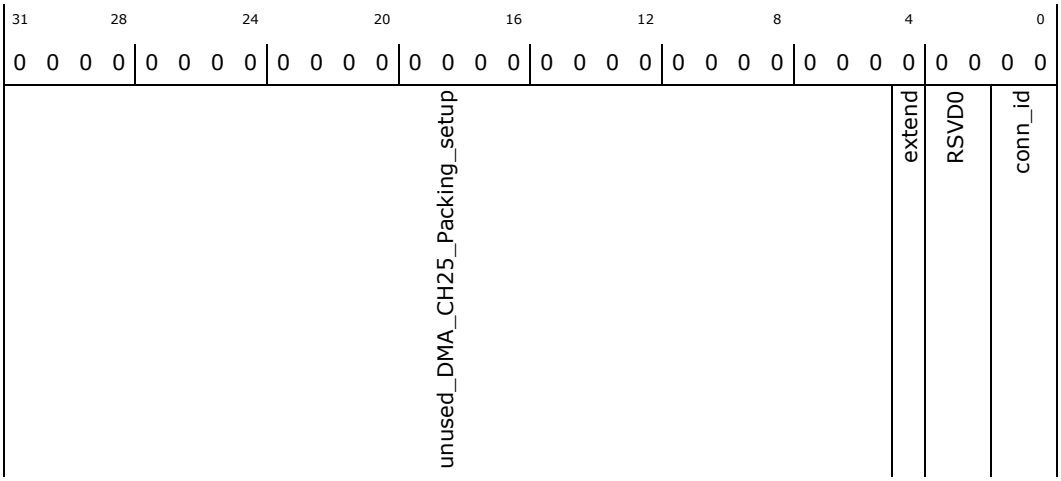
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_Packing_setup: [ISPMMADR] + 41064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH25_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.272 reg_isp_dma_DMA_CH26_Packing_setup_type (isp_dma_DMA_CH26_Packing_setup)—Offset 41068h

DMA CH 26 PARAM 0: Packing setup

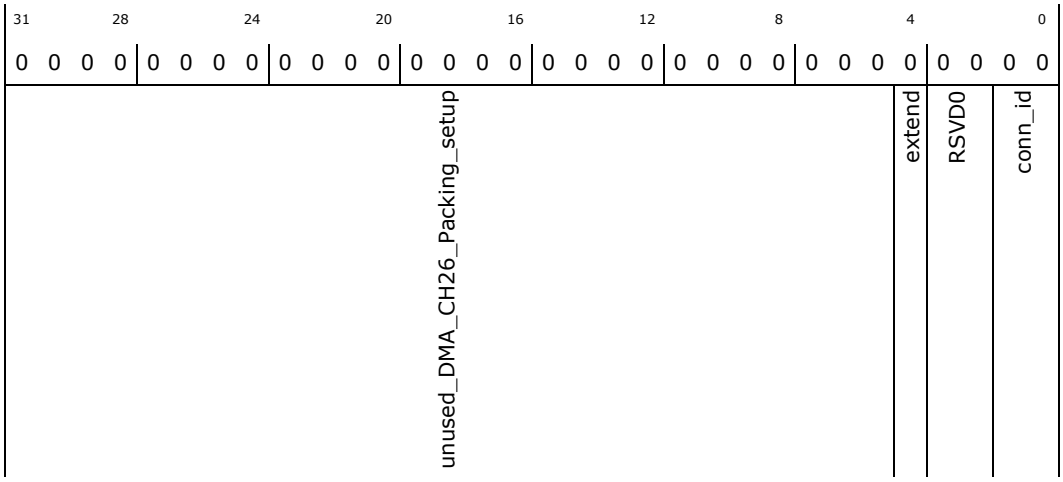
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_Packing_setup: [ISPMMADR] + 41068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH26_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.273 reg_isp_dma_DMA_CH28_Packing_setup_type (isp_dma_DMA_CH28_Packing_setup)—Offset 41070h

DMA CH 28 PARAM 0: Packing setup

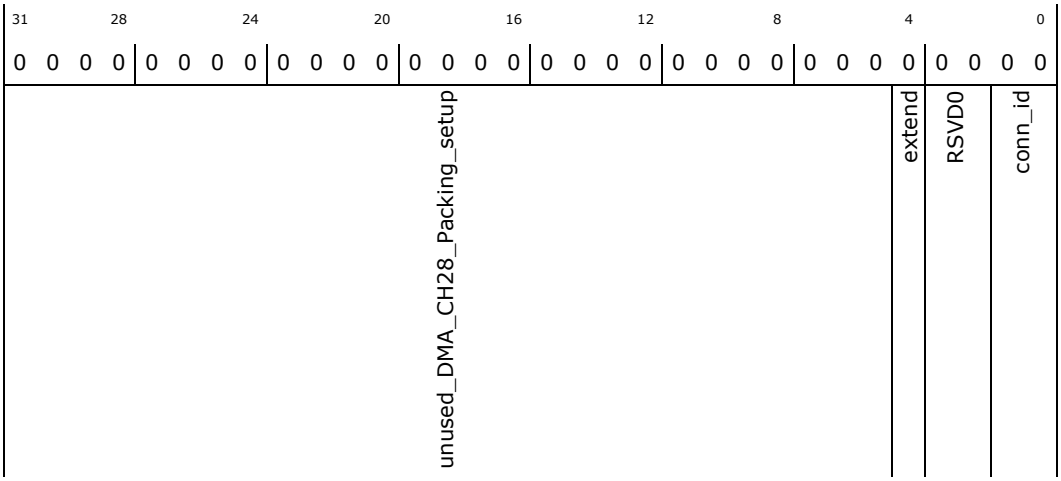
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_Packing_setup: [ISPMMADR] + 41070h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH28_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.274 reg_isp_dma_DMA_CH29_Packing_setup_type (isp_dma_DMA_CH29_Packing_setup)—Offset 41074h

DMA CH 29 PARAM 0: Packing setup

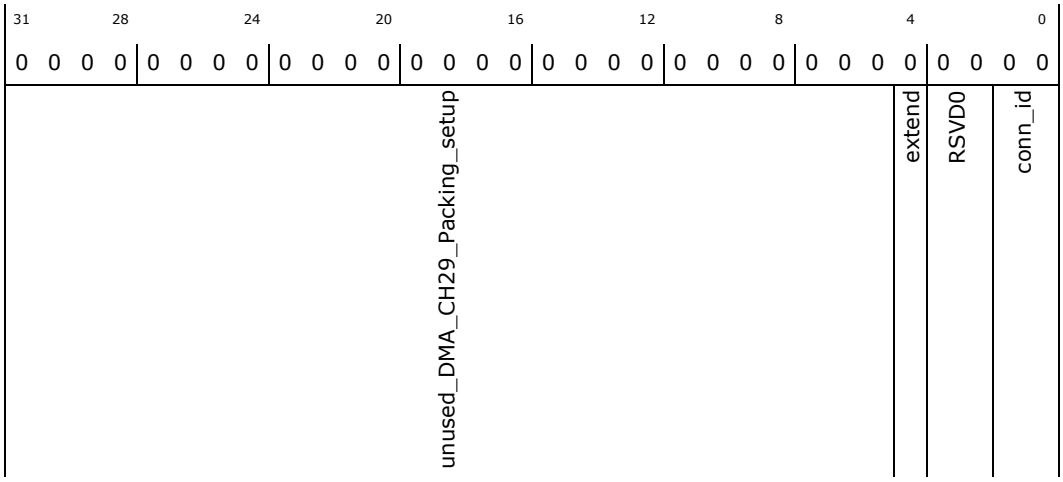
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_Packing_setup: [ISPMMADR] + 41074h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH29_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.275 reg_isp_dma_DMA_CH30_Packing_setup_type (isp_dma_DMA_CH30_Packing_setup)—Offset 41078h

DMA CH 30 PARAM 0: Packing setup

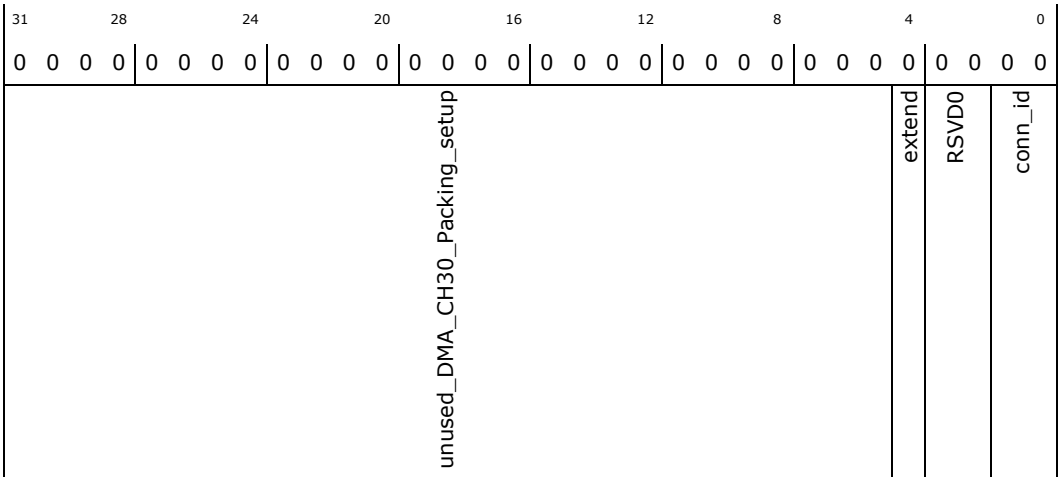
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH30_Packing_setup: [ISPMMADR] + 41078h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH30_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.276 reg_isp_dma_DMA_CH31_Packing_setup_type (isp_dma_DMA_CH31_Packing_setup)—Offset 4107Ch

DMA CH 31 PARAM 0: Packing setup

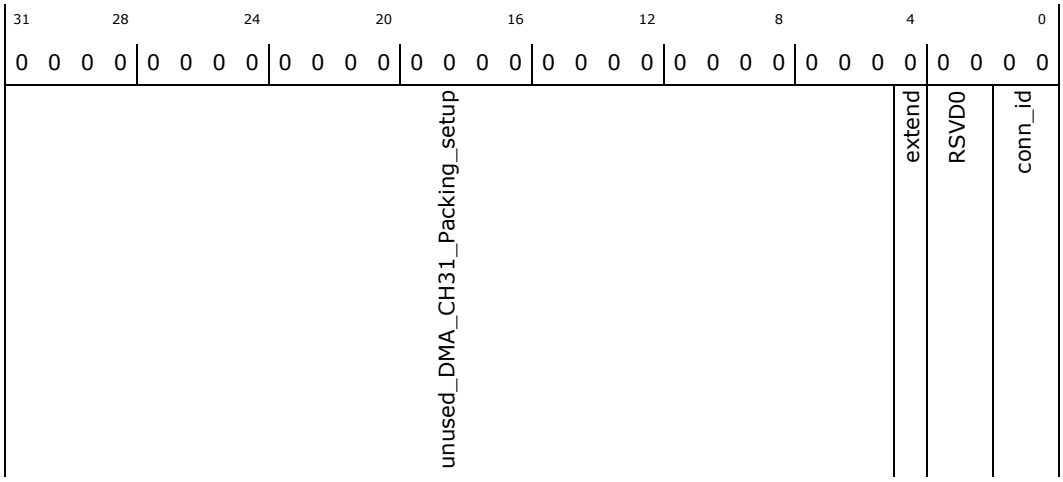
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_Packing_setup: [ISPMMADR] + 4107Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH31_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

3.7.277 reg_isp_dma_DMA_CH0_dev_stride_A_type (isp_dma_DMA_CH0_dev_stride_A)—Offset 41100h

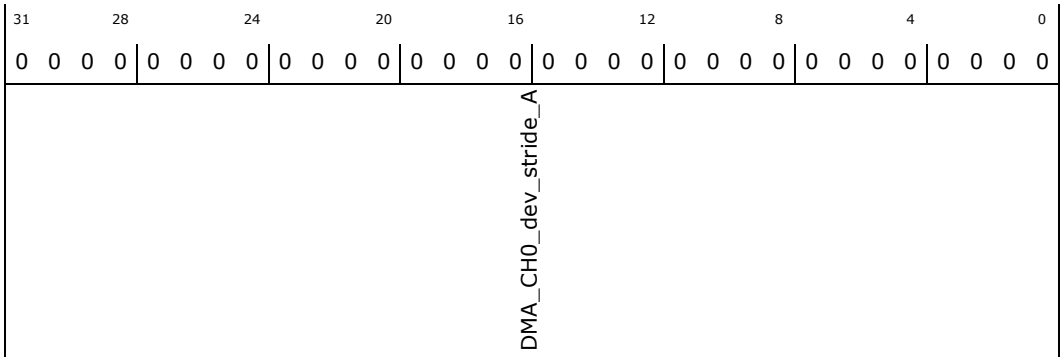
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_dev_stride_A: [ISPMMADR] + 41100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH0_dev_stride_A:** DMA CH 0 PARAM 1: Device A stride

3.7.278 reg_isp_dma_DMA_CH1_dev_stride_A_type (isp_dma_DMA_CH1_dev_stride_A)—Offset 41104h

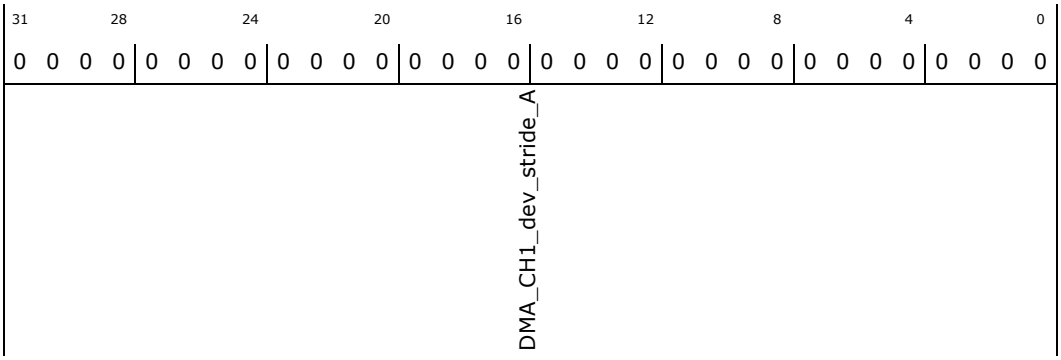
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_dev_stride_A: [ISPMMADR] + 41104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH1_dev_stride_A:** DMA CH 1 PARAM 1: Device A stride

3.7.279 reg_isp_dma_DMA_CH2_dev_stride_A_type (isp_dma_DMA_CH2_dev_stride_A)—Offset 41108h

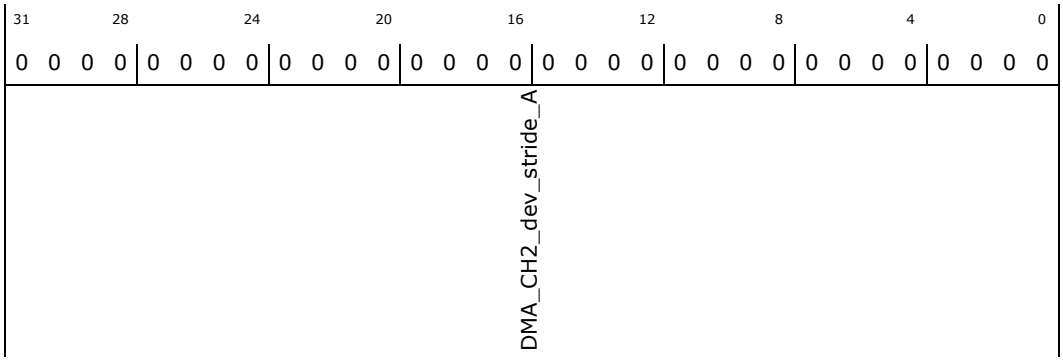
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_dev_stride_A: [ISPMMADR] + 41108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH2_dev_stride_A:** DMA CH 2 PARAM 1: Device A stride

3.7.280 reg_isp_dma_DMA_CH3_dev_stride_A_type (isp_dma_DMA_CH3_dev_stride_A)—Offset 4110Ch

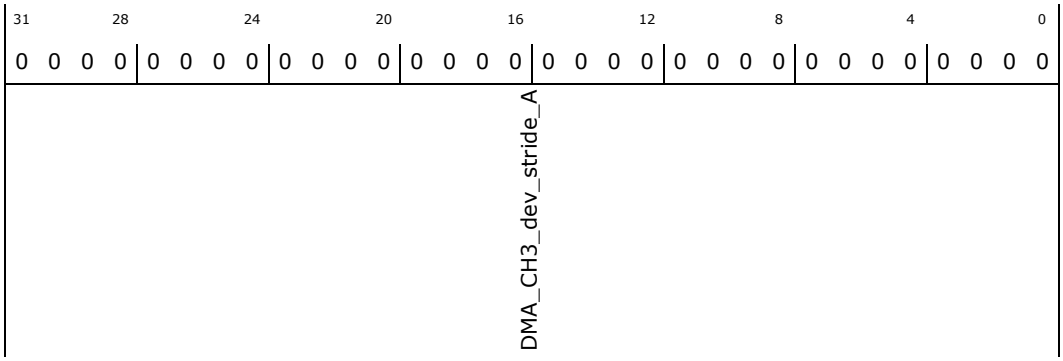
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_dev_stride_A: [ISPMMADR] + 4110Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH3_dev_stride_A:** DMA CH 3 PARAM 1: Device A stride

3.7.281 reg_isp_dma_DMA_CH4_dev_stride_A_type (isp_dma_DMA_CH4_dev_stride_A)—Offset 41110h

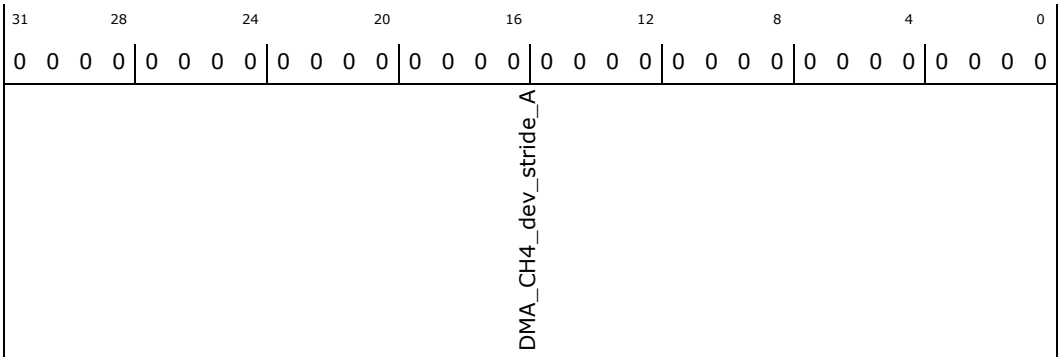
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_dev_stride_A: [ISPMMADR] + 41110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH4_dev_stride_A:** DMA CH 4 PARAM 1: Device A stride

3.7.282 reg_isp_dma_DMA_CH5_dev_stride_A_type (isp_dma_DMA_CH5_dev_stride_A)—Offset 41114h

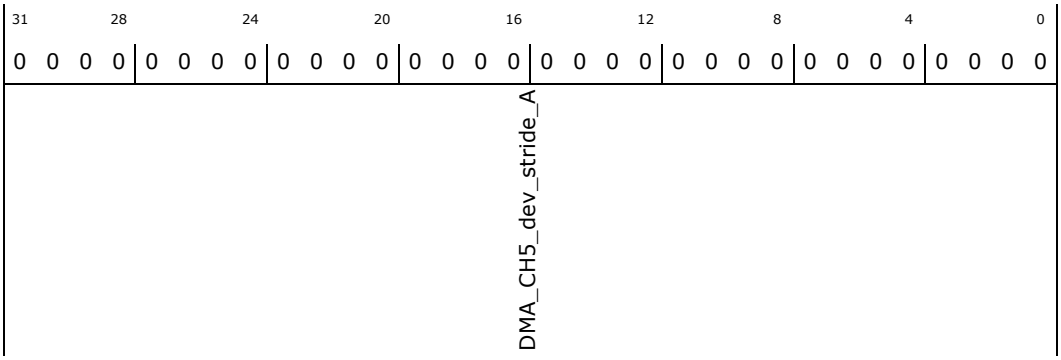
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_dev_stride_A: [ISPMMADR] + 41114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH5_dev_stride_A:** DMA CH 5 PARAM 1: Device A stride

3.7.283 reg_isp_dma_DMA_CH6_dev_stride_A_type (isp_dma_DMA_CH6_dev_stride_A)—Offset 41118h

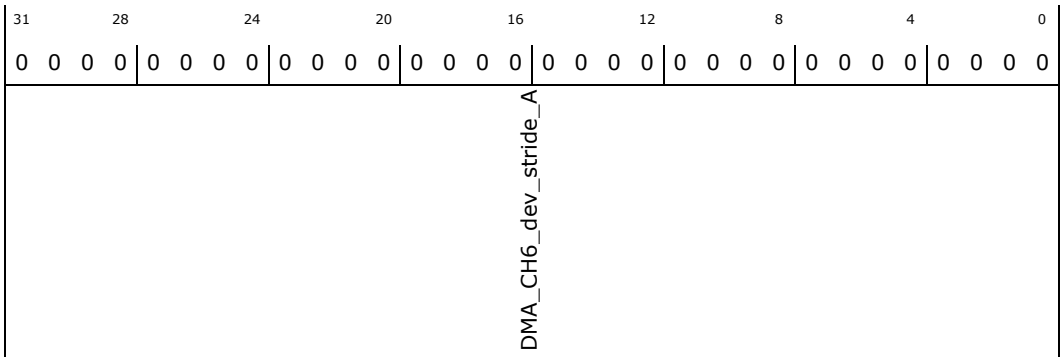
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_dev_stride_A: [ISPMMADR] + 41118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH6_dev_stride_A:** DMA CH 6 PARAM 1: Device A stride

3.7.284 reg_isp_dma_DMA_CH7_dev_stride_A_type (isp_dma_DMA_CH7_dev_stride_A)—Offset 4111Ch

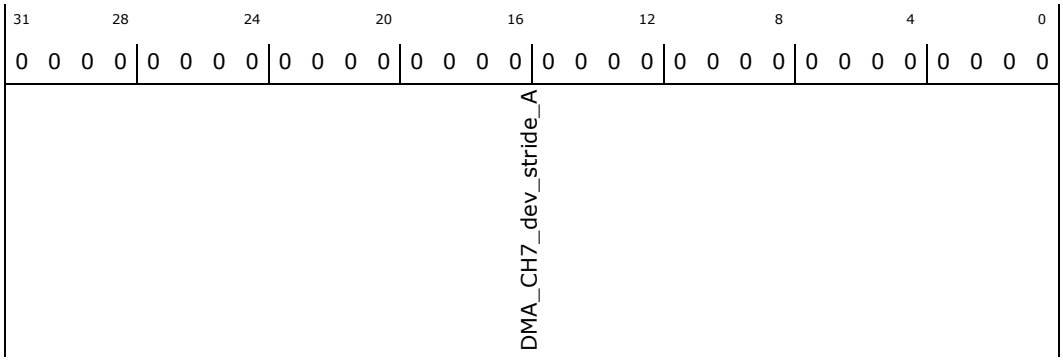
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_dev_stride_A: [ISPMMADR] + 4111Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH7_dev_stride_A:** DMA CH 7 PARAM 1: Device A stride

3.7.285 reg_isp_dma_DMA_CH8_dev_stride_A_type (isp_dma_DMA_CH8_dev_stride_A)—Offset 41120h

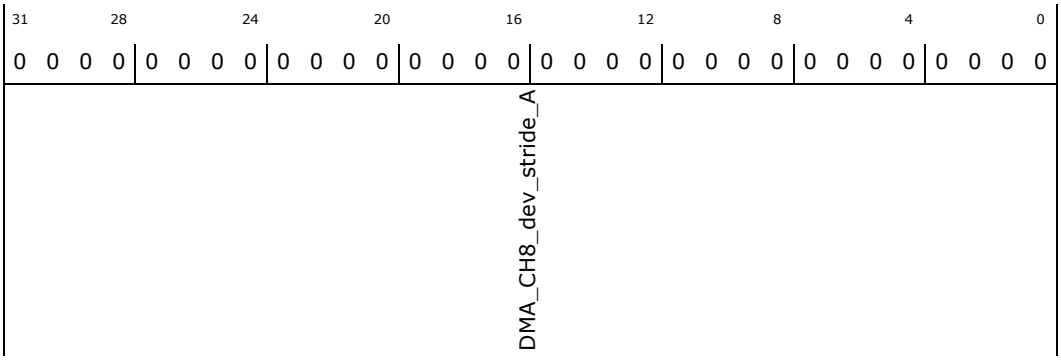
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_dev_stride_A: [ISPMMADR] + 41120h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH8_dev_stride_A:** DMA CH 8 PARAM 1: Device A stride

3.7.286 reg_isp_dma_DMA_CH9_dev_stride_A_type (isp_dma_DMA_CH9_dev_stride_A)—Offset 41124h

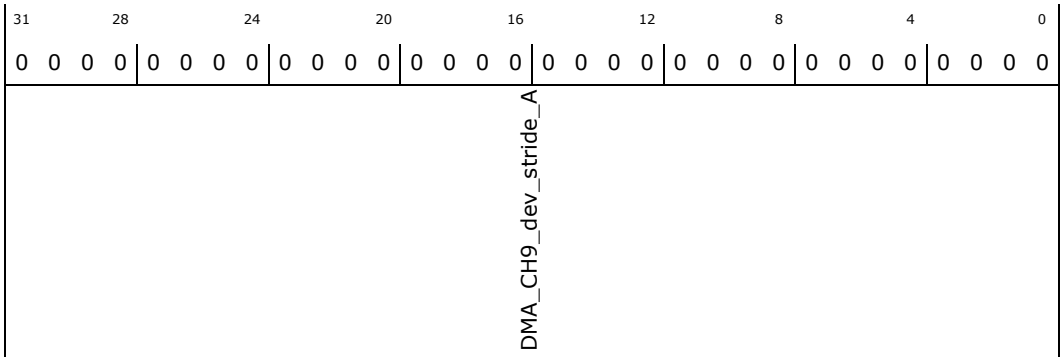
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_dev_stride_A: [ISPMMADR] + 41124h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH9_dev_stride_A:** DMA CH 9 PARAM 1: Device A stride

3.7.287 reg_isp_dma_DMA_CH10_dev_stride_A_type (isp_dma_DMA_CH10_dev_stride_A)—Offset 41128h

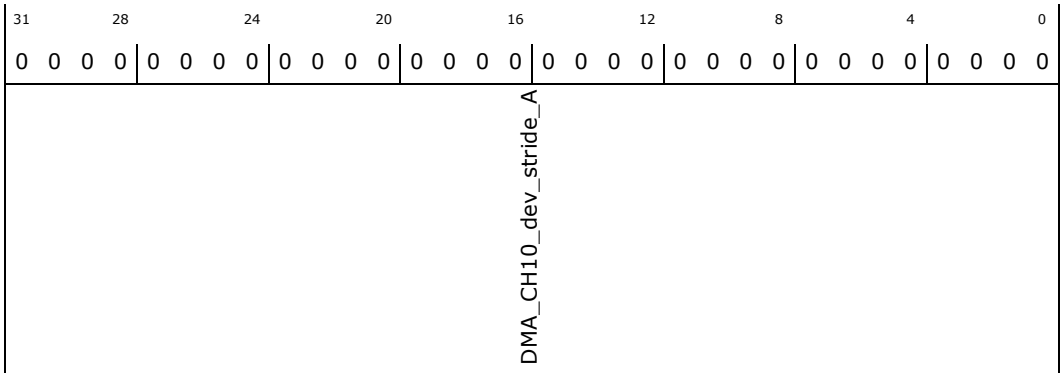
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_dev_stride_A: [ISPMMADR] + 41128h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH10_dev_stride_A:** DMA CH 10 PARAM 1: Device A stride

3.7.288 reg_isp_dma_DMA_CH11_dev_stride_A_type (isp_dma_DMA_CH11_dev_stride_A)—Offset 4112Ch

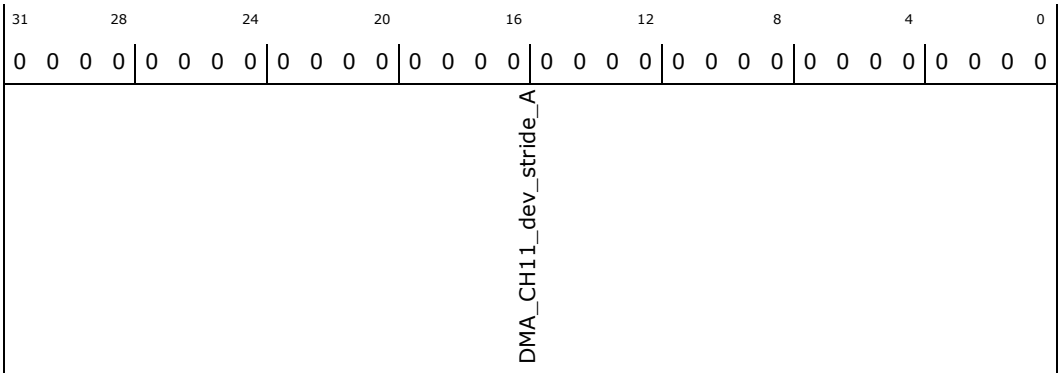
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_dev_stride_A: [ISPMMADR] + 4112Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH11_dev_stride_A:** DMA CH 11 PARAM 1: Device A stride

3.7.289 reg_isp_dma_DMA_CH12_dev_stride_A_type (isp_dma_DMA_CH12_dev_stride_A)—Offset 41130h

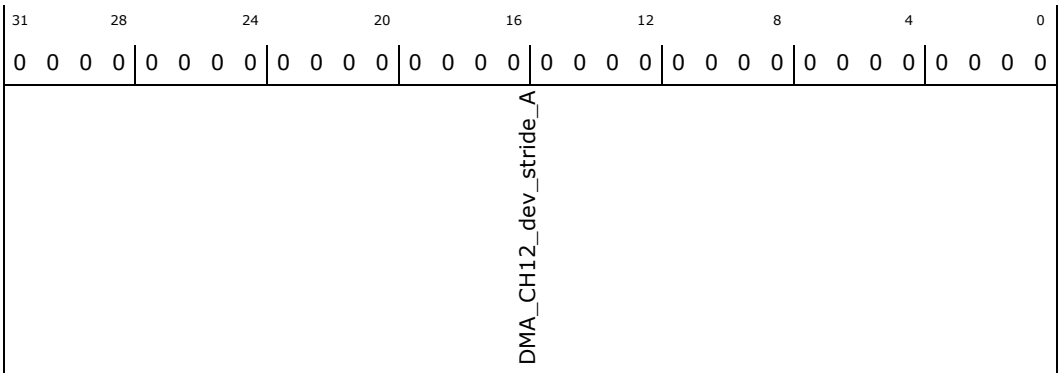
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_dev_stride_A: [ISPMMADR] + 41130h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH12_dev_stride_A:** DMA CH 12 PARAM 1: Device A stride

3.7.290 reg_isp_dma_DMA_CH13_dev_stride_A_type (isp_dma_DMA_CH13_dev_stride_A)—Offset 41134h

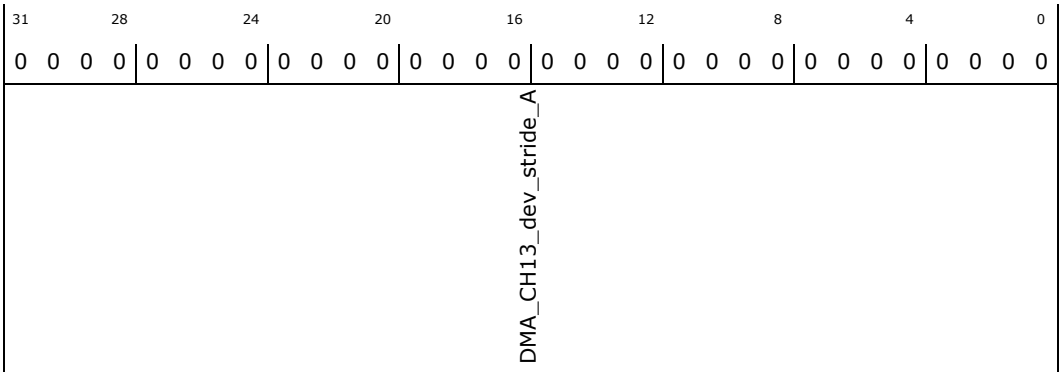
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_dev_stride_A: [ISPMMADR] + 41134h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH13_dev_stride_A:** DMA CH 13 PARAM 1: Device A stride

3.7.291 reg_isp_dma_DMA_CH14_dev_stride_A_type (isp_dma_DMA_CH14_dev_stride_A)—Offset 41138h

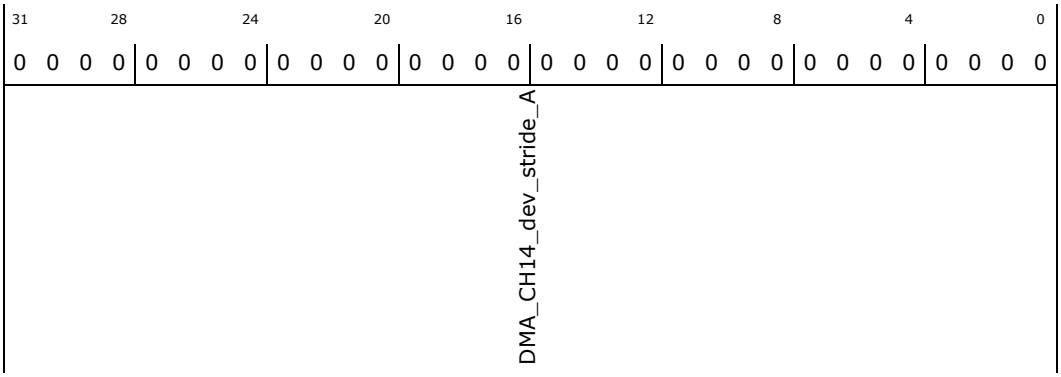
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_dev_stride_A: [ISPMMADR] + 41138h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH14_dev_stride_A:** DMA CH 14 PARAM 1: Device A stride

3.7.292 reg_isp_dma_DMA_CH15_dev_stride_A_type (isp_dma_DMA_CH15_dev_stride_A)—Offset 4113Ch

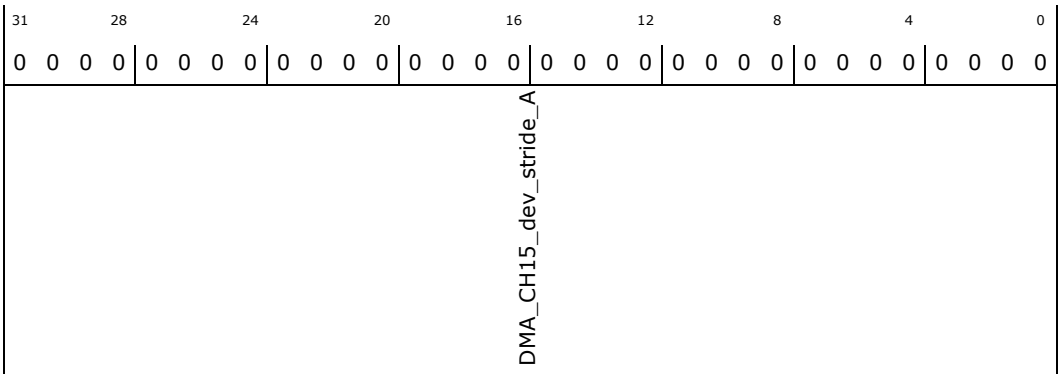
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_dev_stride_A: [ISPMMADR] + 4113Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH15_dev_stride_A:** DMA CH 15 PARAM 1: Device A stride

3.7.293 reg_isp_dma_DMA_CH16_dev_stride_A_type (isp_dma_DMA_CH16_dev_stride_A)—Offset 41140h

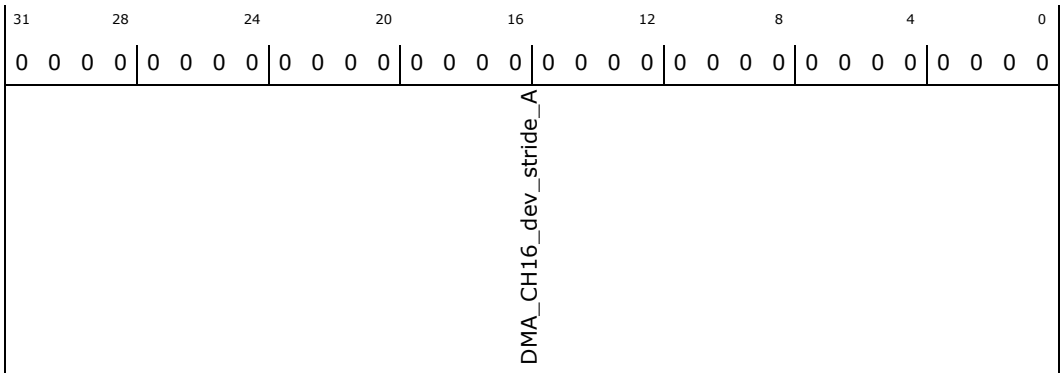
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_dev_stride_A: [ISPMMADR] + 41140h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH16_dev_stride_A:** DMA CH 16 PARAM 1: Device A stride

3.7.294 reg_isp_dma_DMA_CH17_dev_stride_A_type (isp_dma_DMA_CH17_dev_stride_A)—Offset 41144h

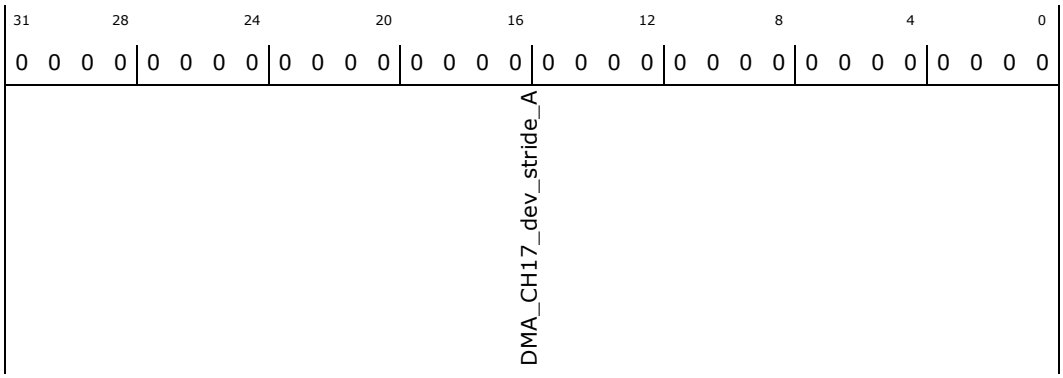
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_dev_stride_A: [ISPMMADR] + 41144h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH17_dev_stride_A:** DMA CH 17 PARAM 1: Device A stride

3.7.295 reg_isp_dma_DMA_CH18_dev_stride_A_type (isp_dma_DMA_CH18_dev_stride_A)—Offset 41148h

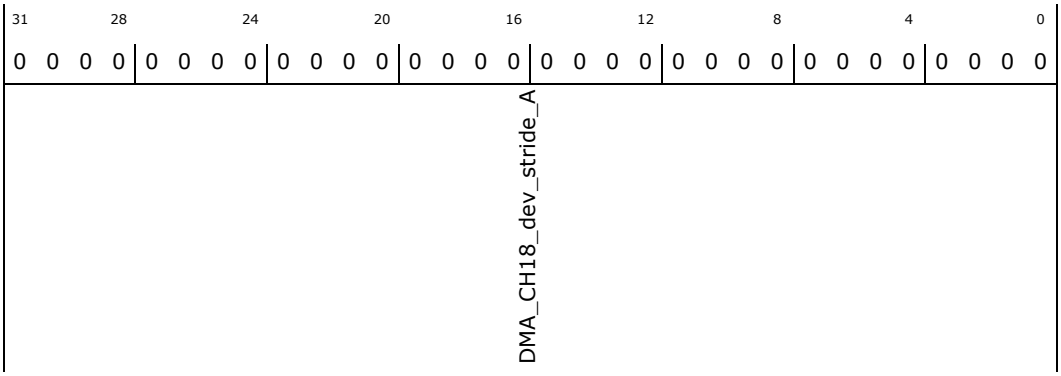
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_dev_stride_A: [ISPMMADR] + 41148h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH18_dev_stride_A:** DMA CH 18 PARAM 1: Device A stride

3.7.296 reg_isp_dma_DMA_CH19_dev_stride_A_type (isp_dma_DMA_CH19_dev_stride_A)—Offset 4114Ch

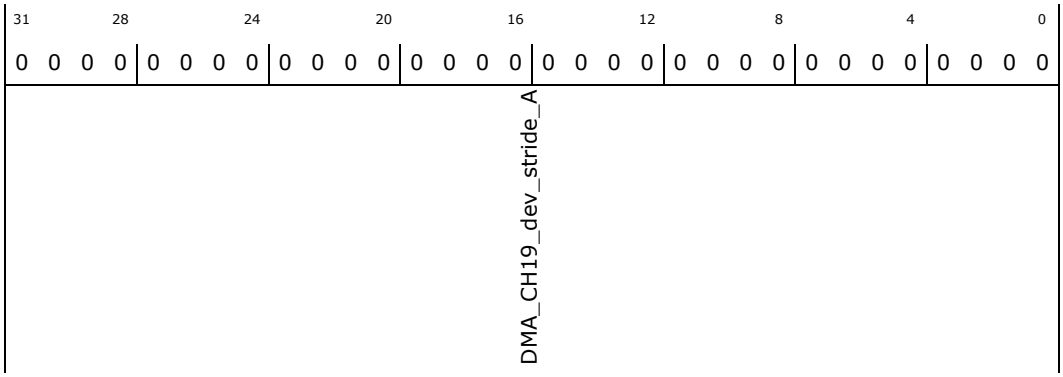
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_dev_stride_A: [ISPMMADR] + 4114Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH19_dev_stride_A:** DMA CH 19 PARAM 1: Device A stride

3.7.297 reg_isp_dma_DMA_CH20_dev_stride_A_type (isp_dma_DMA_CH20_dev_stride_A)—Offset 41150h

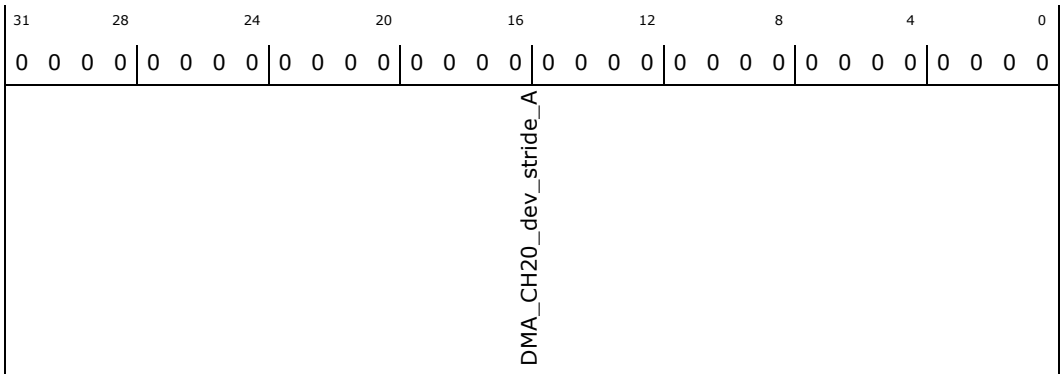
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_dev_stride_A: [ISPMMADR] + 41150h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH20_dev_stride_A:** DMA CH 20 PARAM 1: Device A stride

3.7.298 reg_isp_dma_DMA_CH21_dev_stride_A_type (isp_dma_DMA_CH21_dev_stride_A)—Offset 41154h

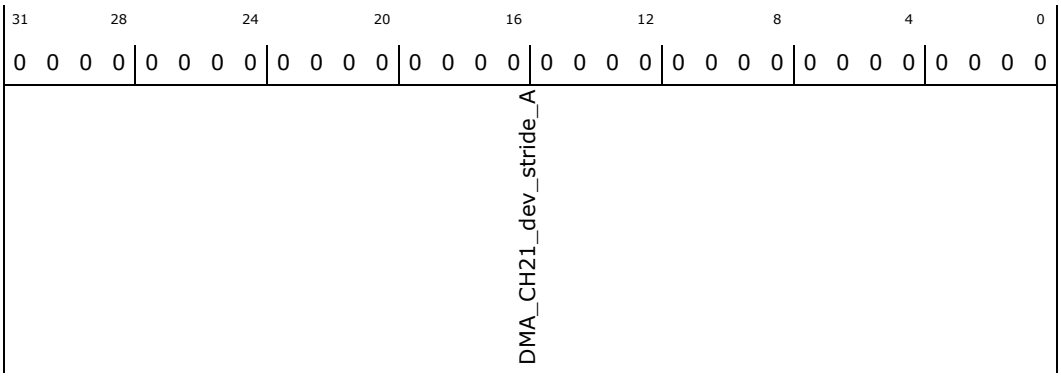
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_dev_stride_A: [ISPMMADR] + 41154h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH21_dev_stride_A:** DMA CH 21 PARAM 1: Device A stride

3.7.299 reg_isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A)—Offset 41200h

DMA CH 0 PARAM 2: Device A Packing LSE cropping/Elements

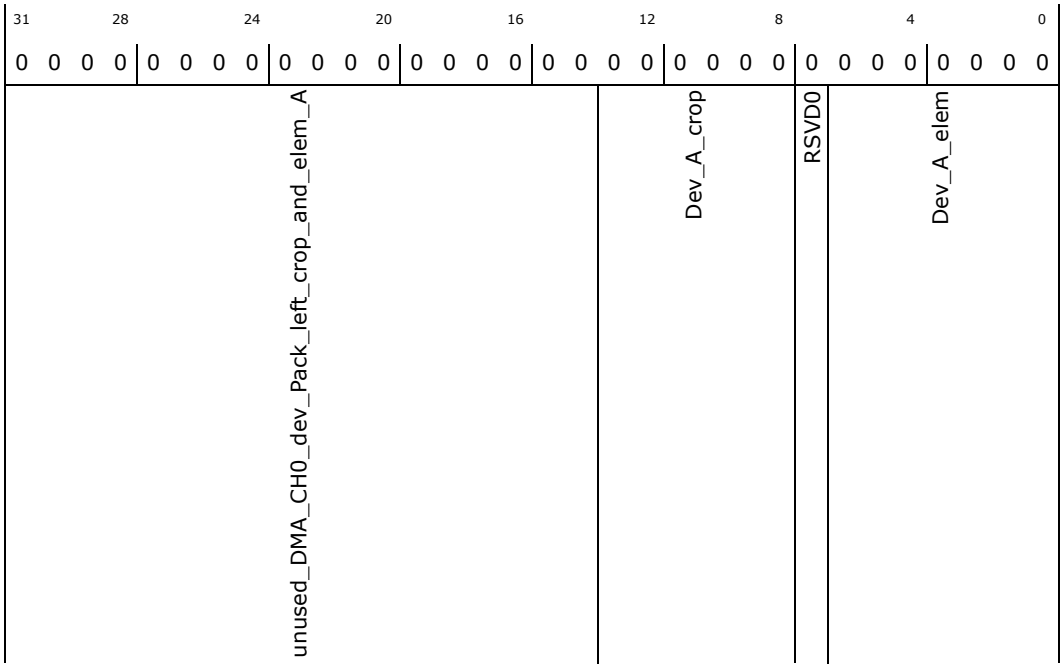
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH0_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.300 reg_isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_A)—Offset 41204h

DMA CH 1 PARAM 2: Device A Packing LSE cropping/Elements

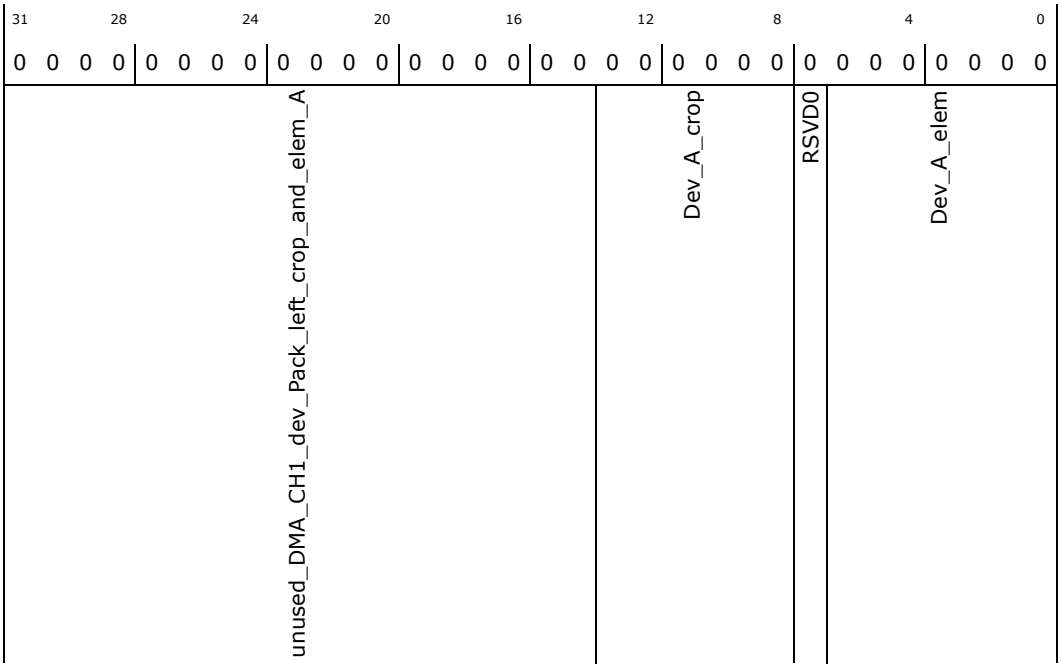
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH1_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.301 reg_isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_A)—Offset 41208h

DMA CH 2 PARAM 2: Device A Packing LSE cropping/Elements

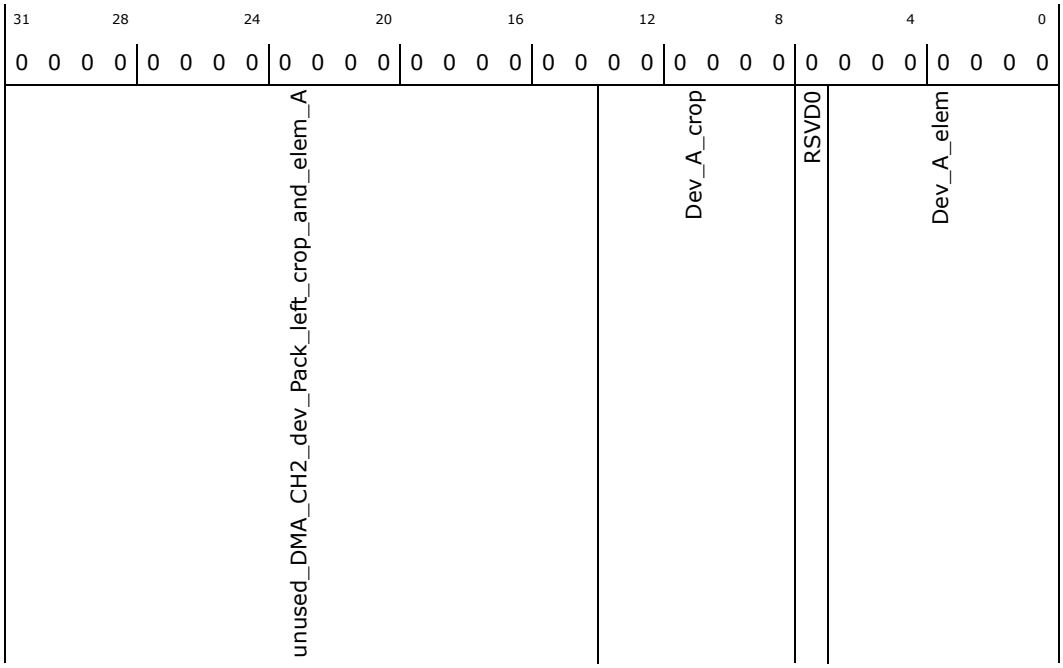
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH2_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.302 reg_isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_A)—Offset 4120Ch

DMA CH 3 PARAM 2: Device A Packing LSE cropping/Elements

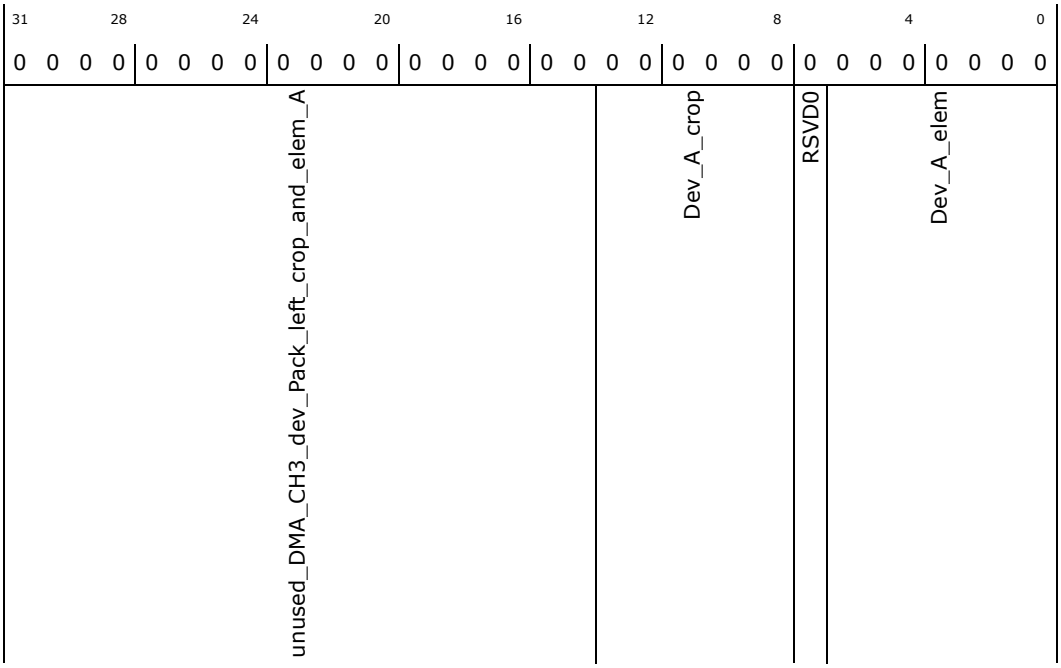
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4120Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH3_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.303 reg_isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_A)—Offset 41210h

DMA CH 4 PARAM 2: Device A Packing LSE cropping/Elements

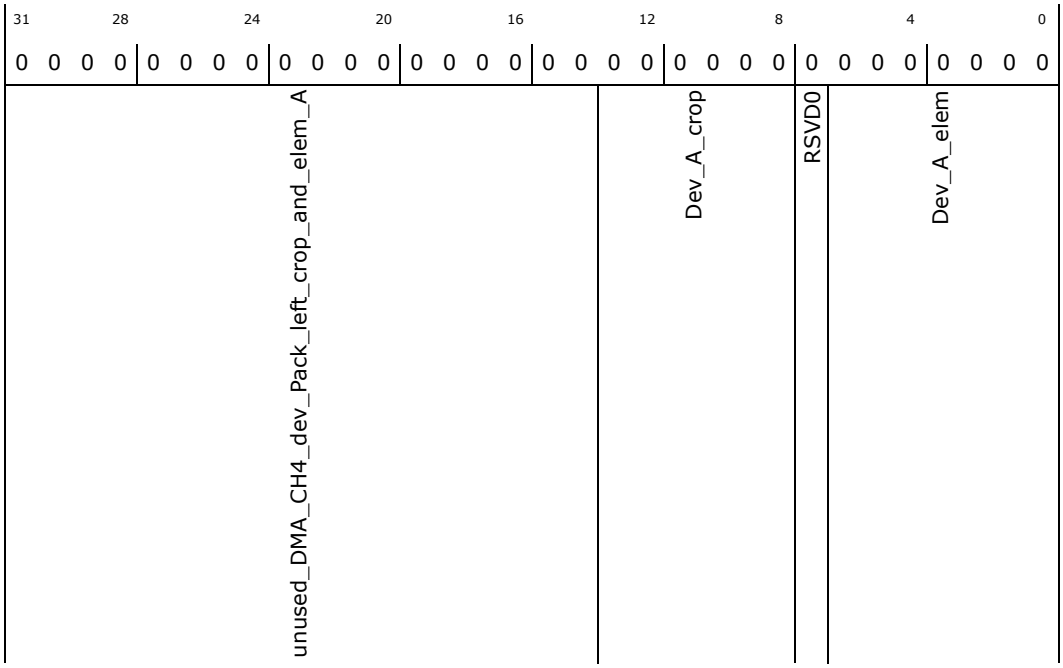
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH4_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.304 reg_isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_A)—Offset 41214h

DMA CH 5 PARAM 2: Device A Packing LSE cropping/Elements

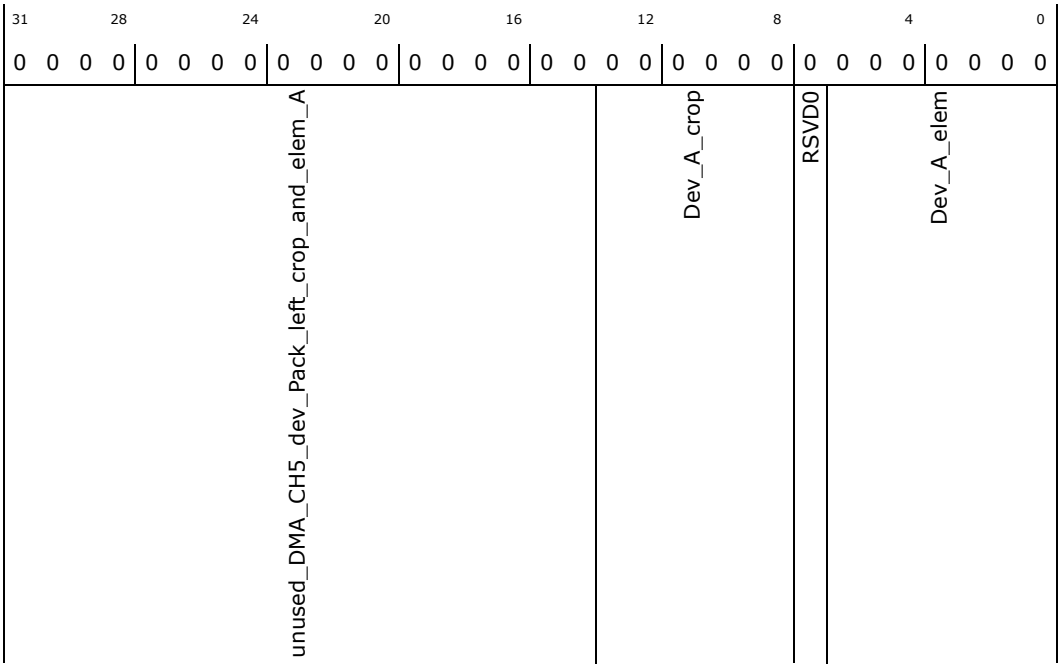
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH5_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.305 reg_isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_A)—Offset 41218h

DMA CH 6 PARAM 2: Device A Packing LSE cropping/Elements

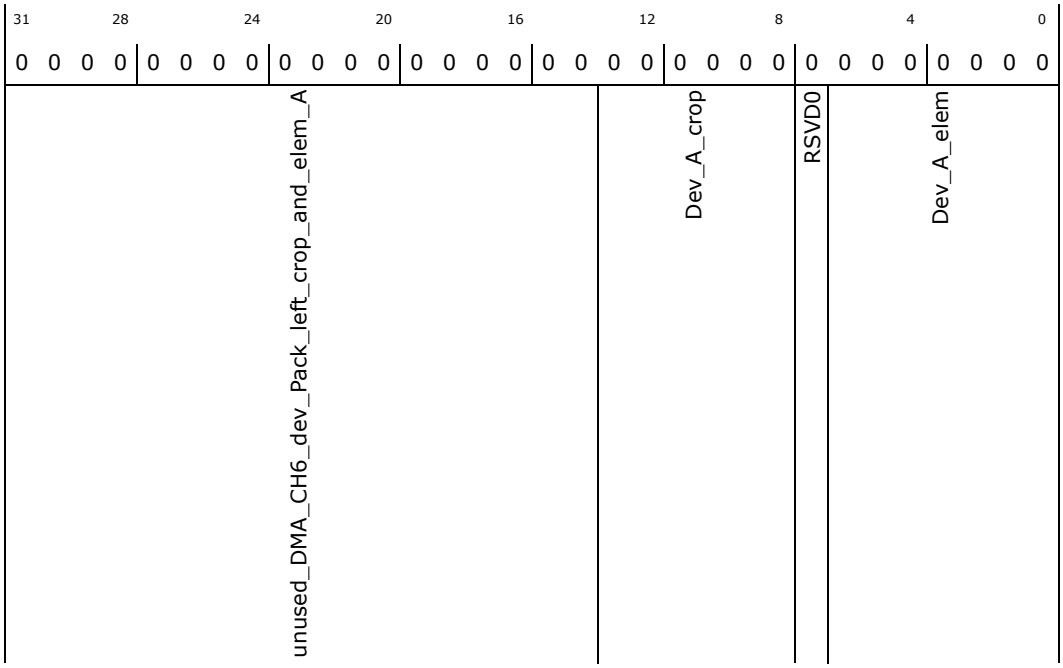
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH6_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.306 reg_isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_A)—Offset 4121Ch

DMA CH 7 PARAM 2: Device A Packing LSE cropping/Elements

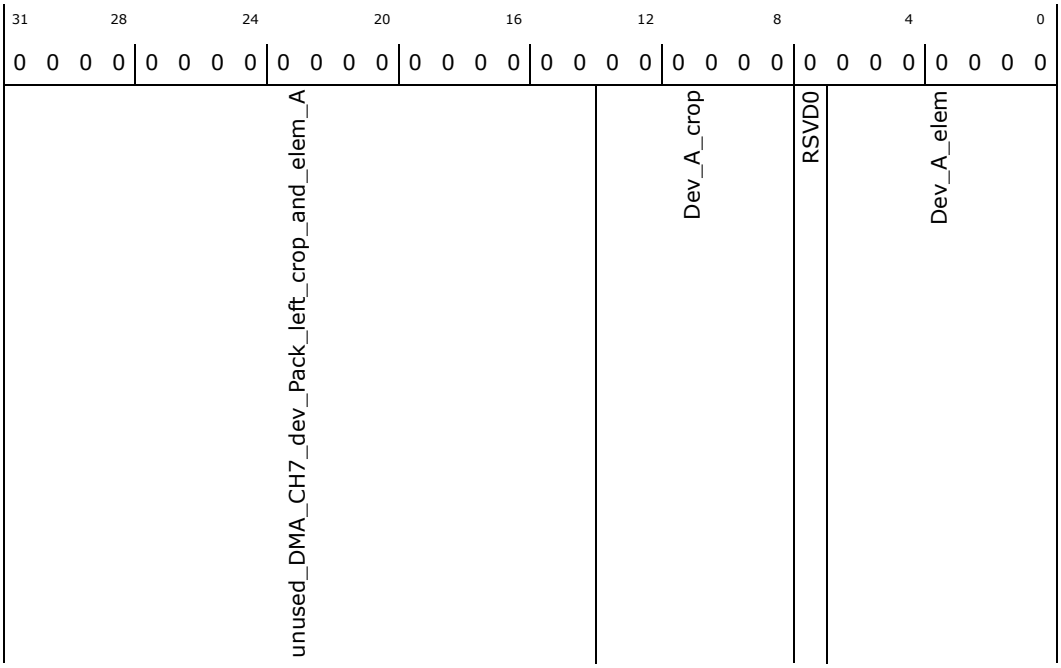
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4121Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH7_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.307 reg_isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_A)—Offset 41220h

DMA CH 8 PARAM 2: Device A Packing LSE cropping/Elements

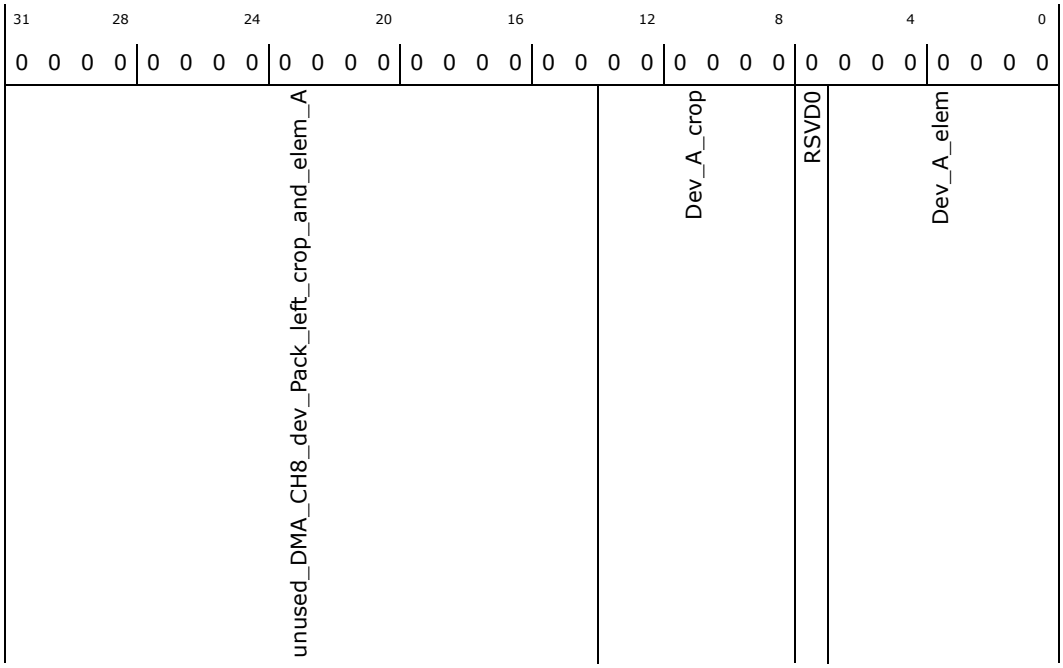
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41220h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH8_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.308 reg_isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_A)—Offset 41224h

DMA CH 9 PARAM 2: Device A Packing LSE cropping/Elements

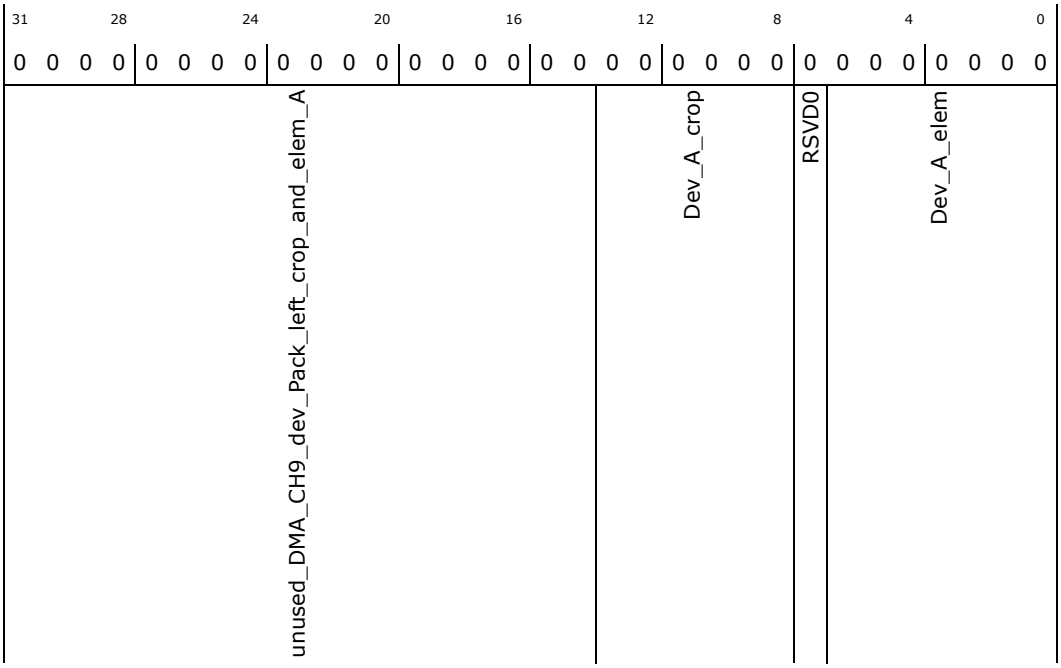
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41224h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH9_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.309 reg_isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_A) —Offset 41228h

DMA CH 10 PARAM 2: Device A Packing LSE cropping/Elements

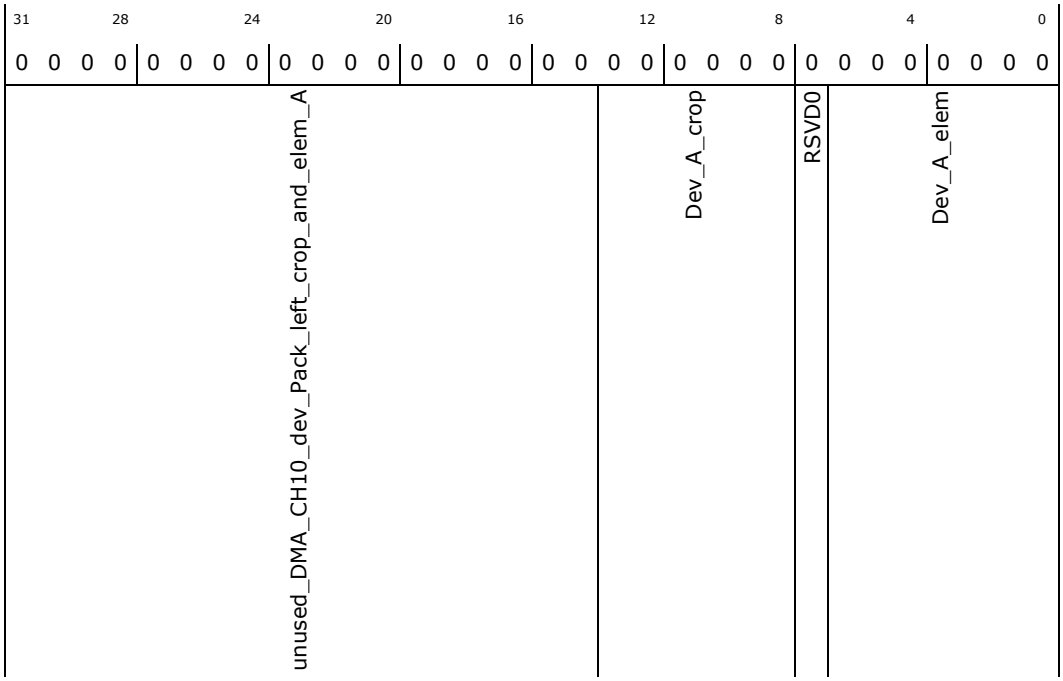
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41228h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH10_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.310 reg_isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_A)—Offset 4122Ch

DMA CH 11 PARAM 2: Device A Packing LSE cropping/Elements

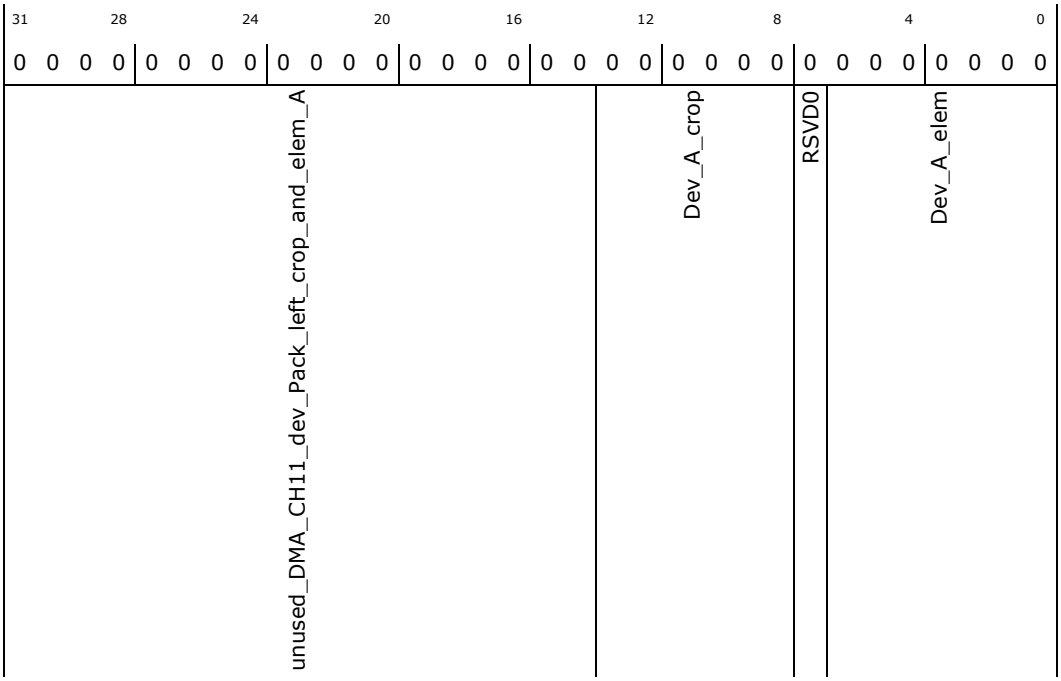
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4122Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH11_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.311 reg_isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_A)—Offset 41230h

DMA CH 12 PARAM 2: Device A Packing LSE cropping/Elements

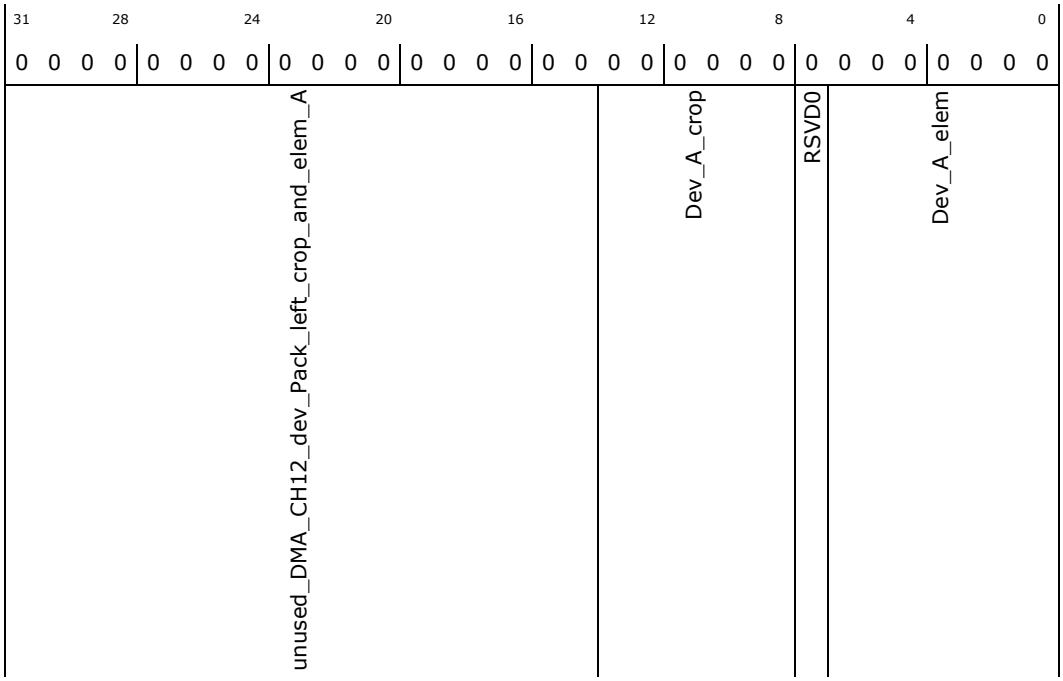
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41230h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH12_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.312 reg_isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_A) —Offset 41234h

DMA CH 13 PARAM 2: Device A Packing LSE cropping/Elements

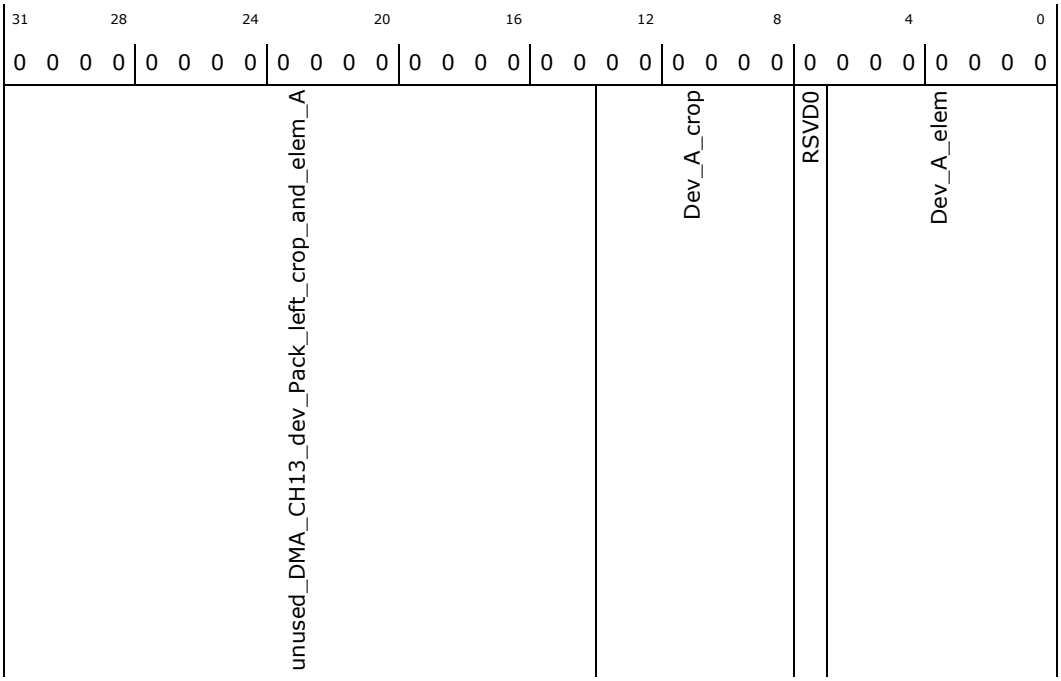
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41234h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH13_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.313 reg_isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_A)—Offset 41238h

DMA CH 14 PARAM 2: Device A Packing LSE cropping/Elements

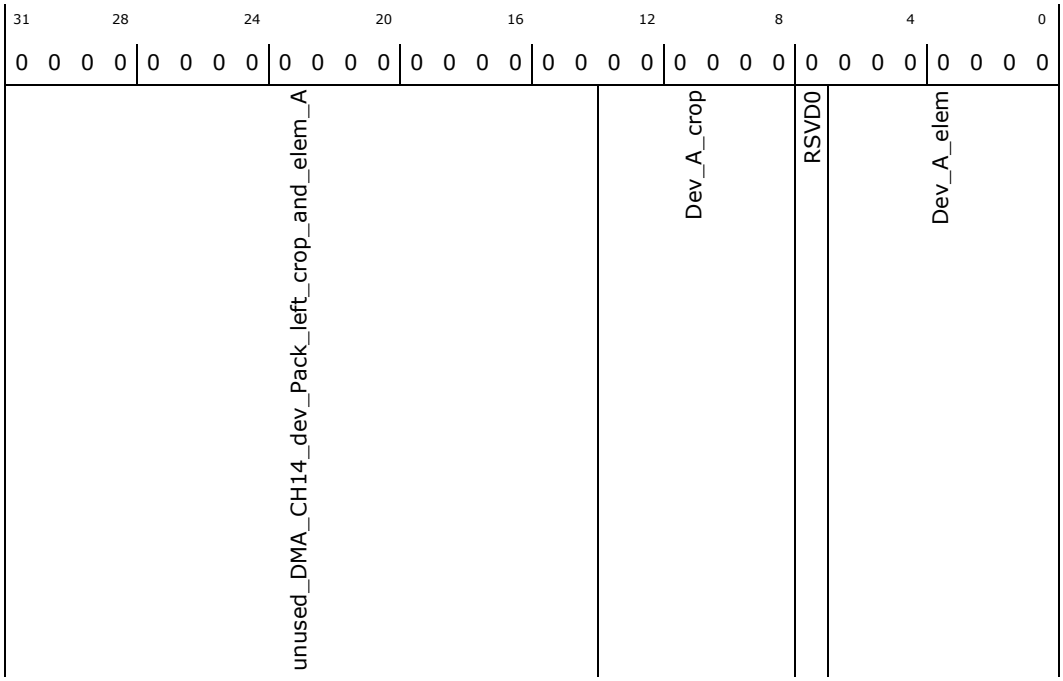
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41238h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH14_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.314 reg_isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_A)—Offset 4123Ch

DMA CH 15 PARAM 2: Device A Packing LSE cropping/Elements

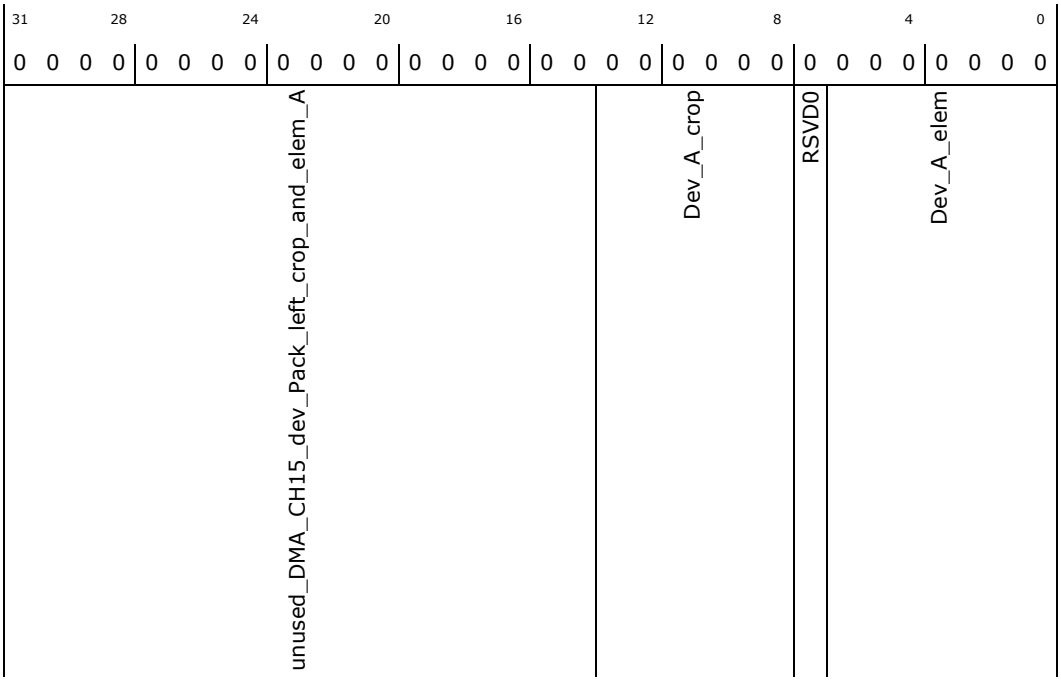
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4123Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH15_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.315 reg_isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_A)—Offset 41240h

DMA CH 16 PARAM 2: Device A Packing LSE cropping/Elements

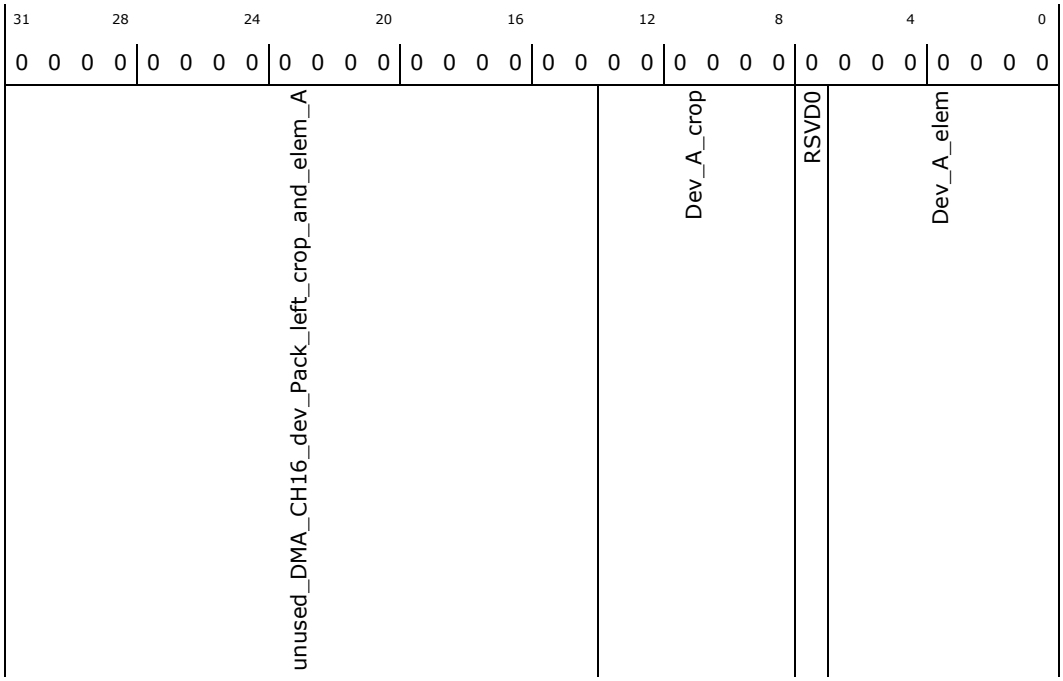
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41240h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH16_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.316 reg_isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_A)—Offset 41244h

DMA CH 17 PARAM 2: Device A Packing LSE cropping/Elements

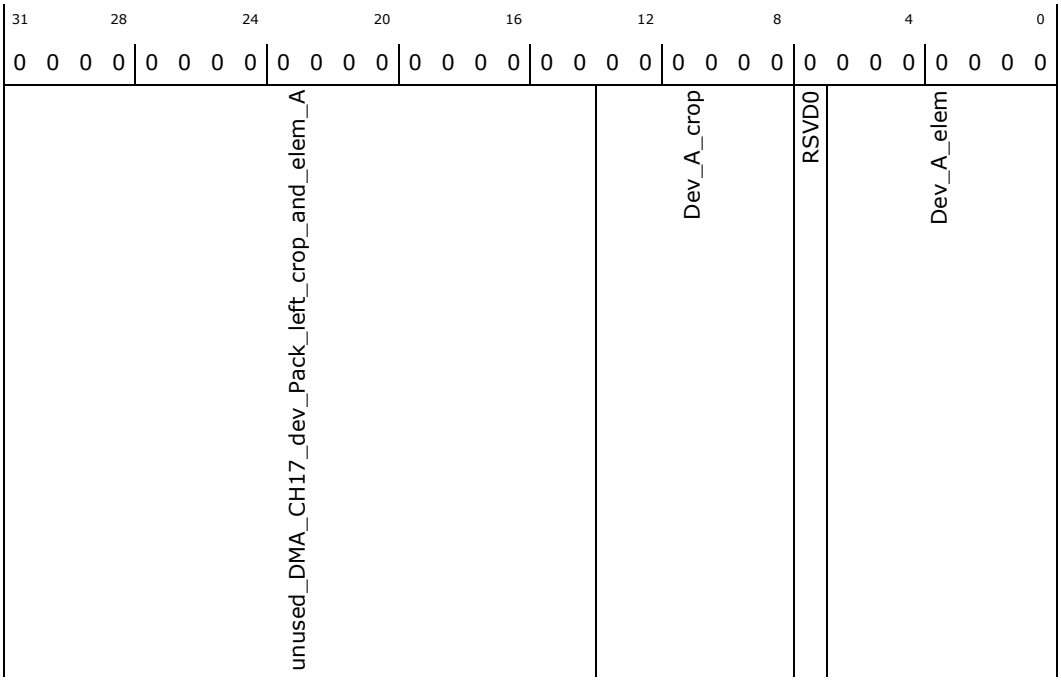
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41244h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH17_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.317 reg_isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_A)—Offset 41248h

DMA CH 18 PARAM 2: Device A Packing LSE cropping/Elements

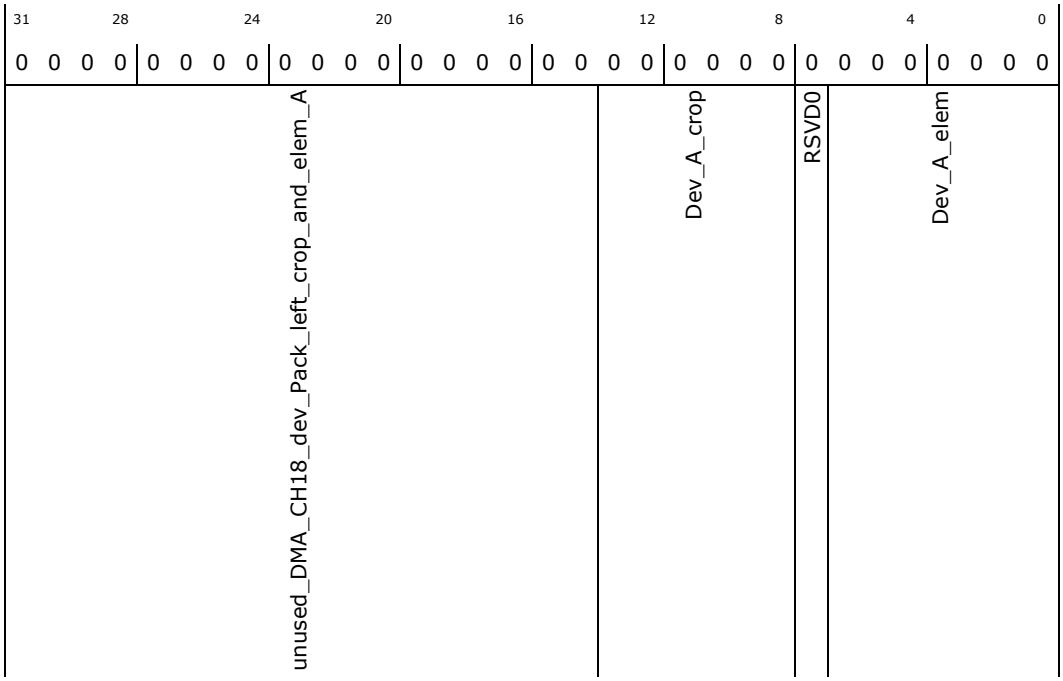
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41248h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH18_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.318 reg_isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_A)—Offset 4124Ch

DMA CH 19 PARAM 2: Device A Packing LSE cropping/Elements

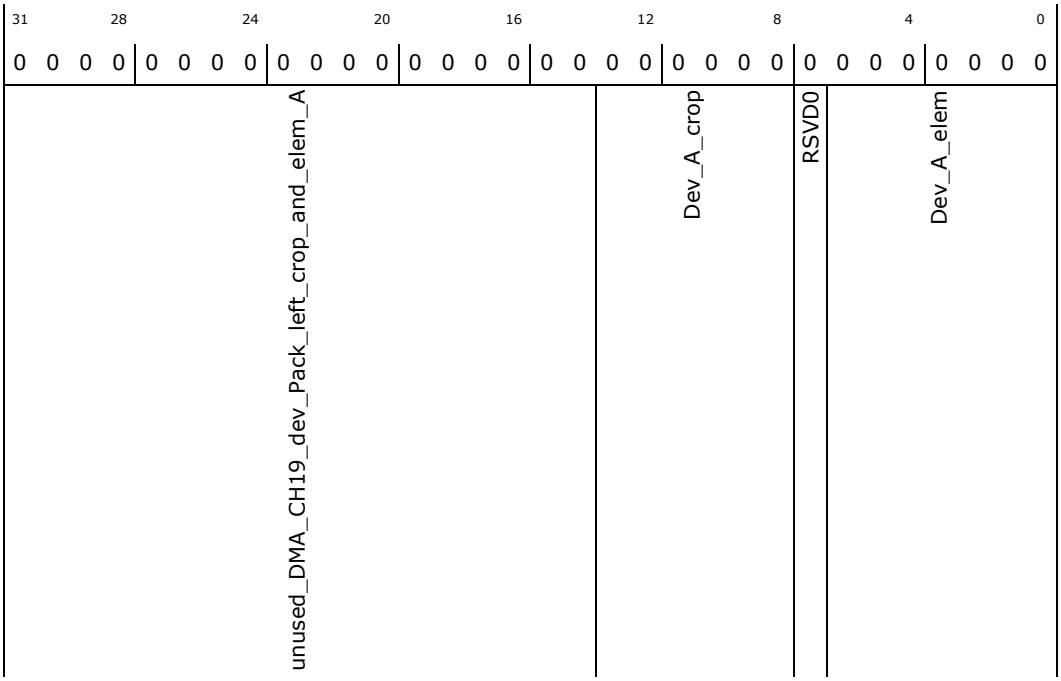
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4124Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH19_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.319 reg_isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_A)—Offset 41250h

DMA CH 20 PARAM 2: Device A Packing LSE cropping/Elements

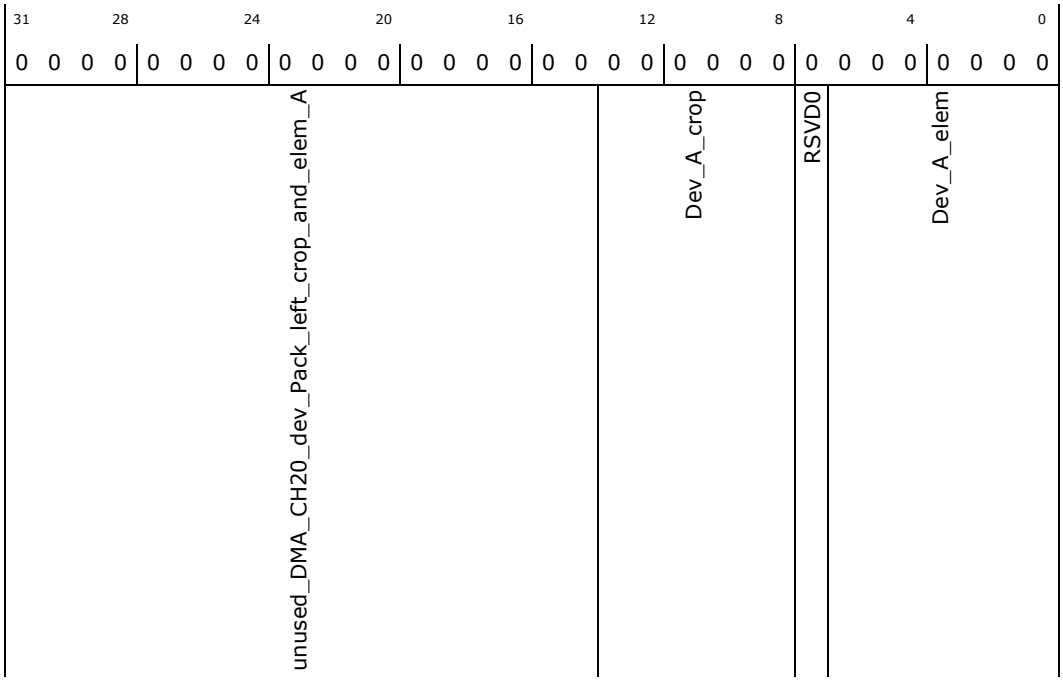
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41250h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH20_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.320 reg_isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_A)—Offset 41254h

DMA CH 21 PARAM 2: Device A Packing LSE cropping/Elements

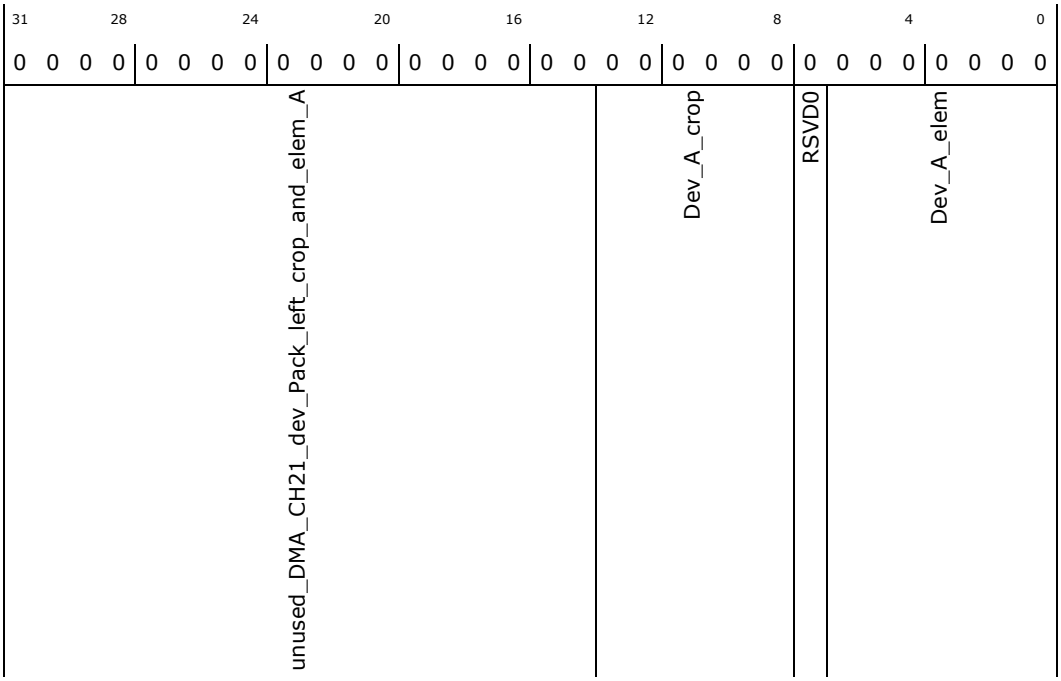
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41254h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH21_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.321 reg_isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_A)—Offset 41258h

DMA CH 22 PARAM 2: Device A Packing LSE cropping/Elements

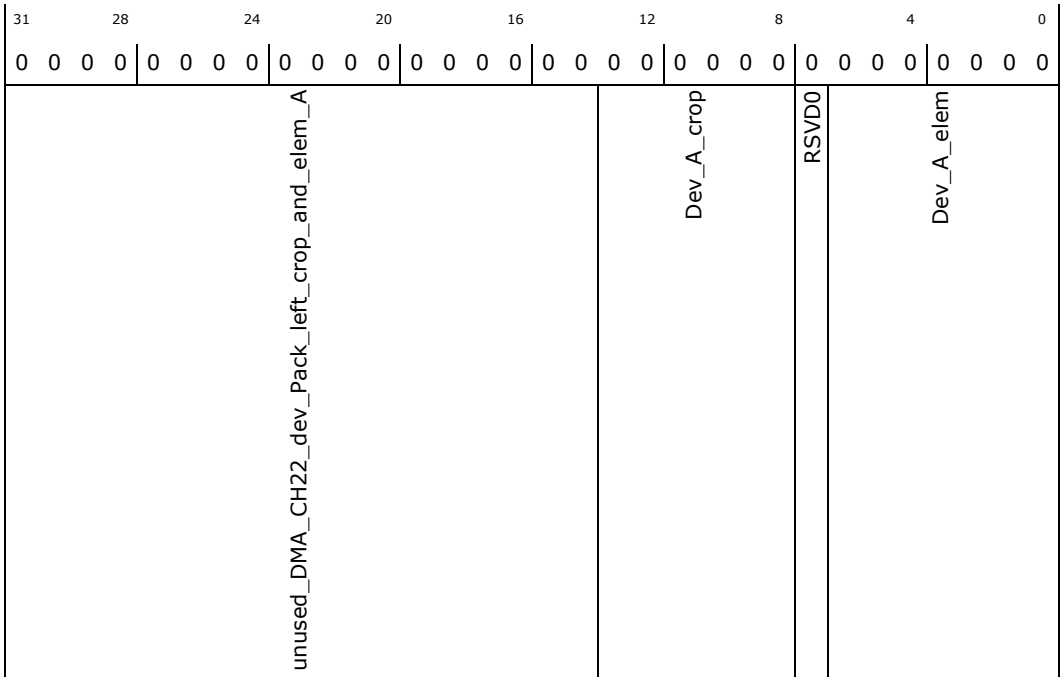
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41258h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH22_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.322 reg_isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_A)—Offset 4125Ch

DMA CH 23 PARAM 2: Device A Packing LSE cropping/Elements

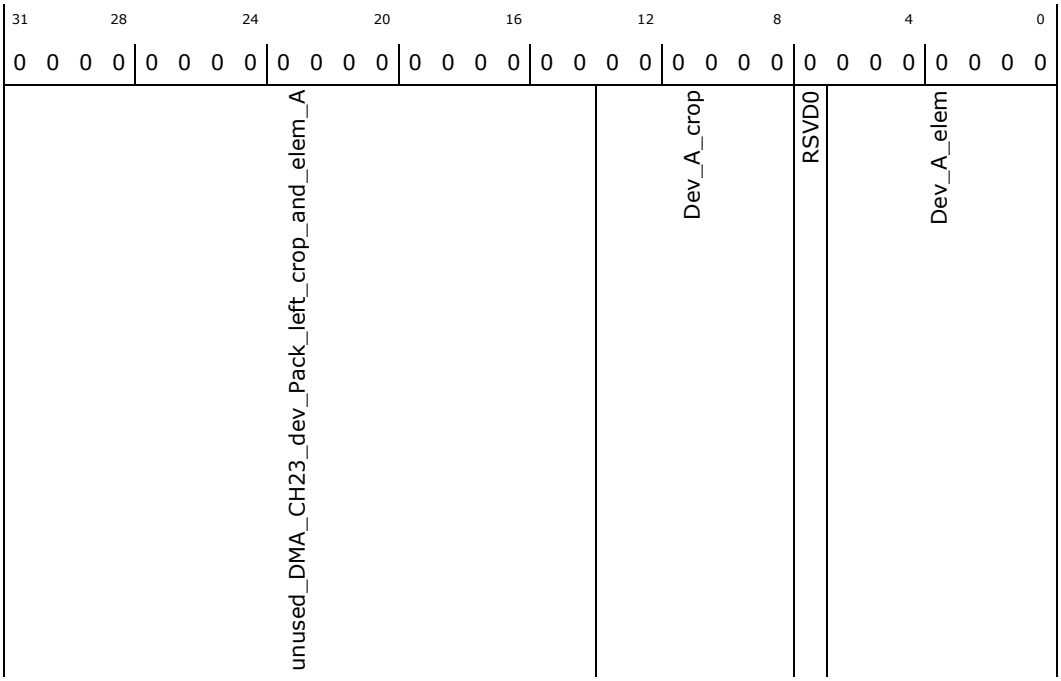
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4125Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH23_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.323 reg_isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_A)—Offset 41260h

DMA CH 24 PARAM 2: Device A Packing LSE cropping/Elements

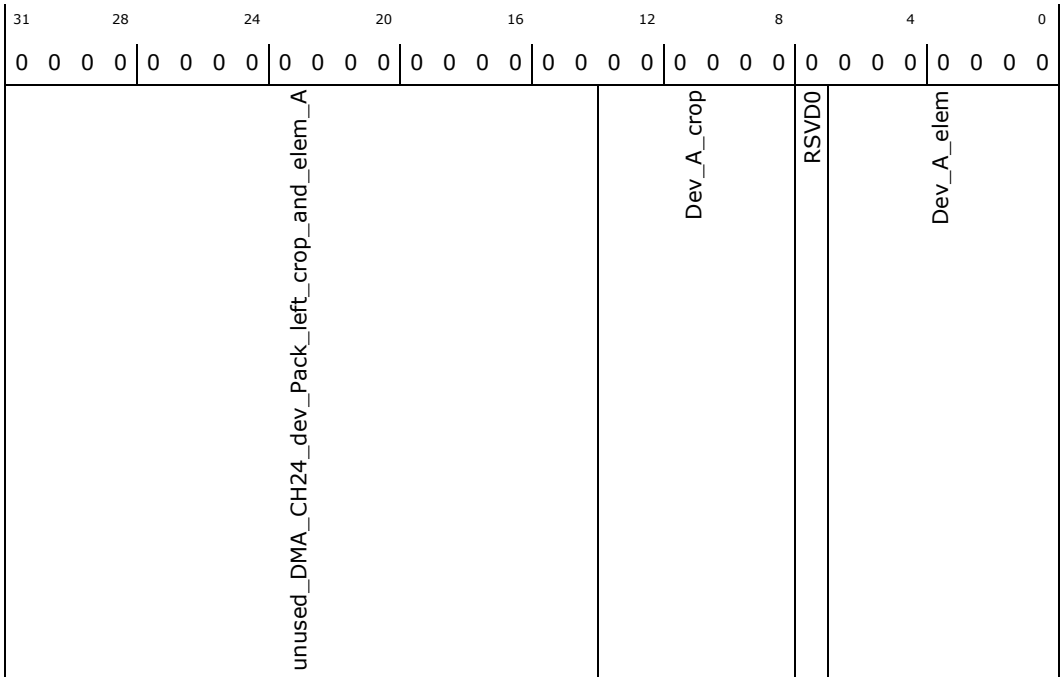
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41260h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH24_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.324 reg_isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_A)—Offset 41264h

DMA CH 25 PARAM 2: Device A Packing LSE cropping/Elements

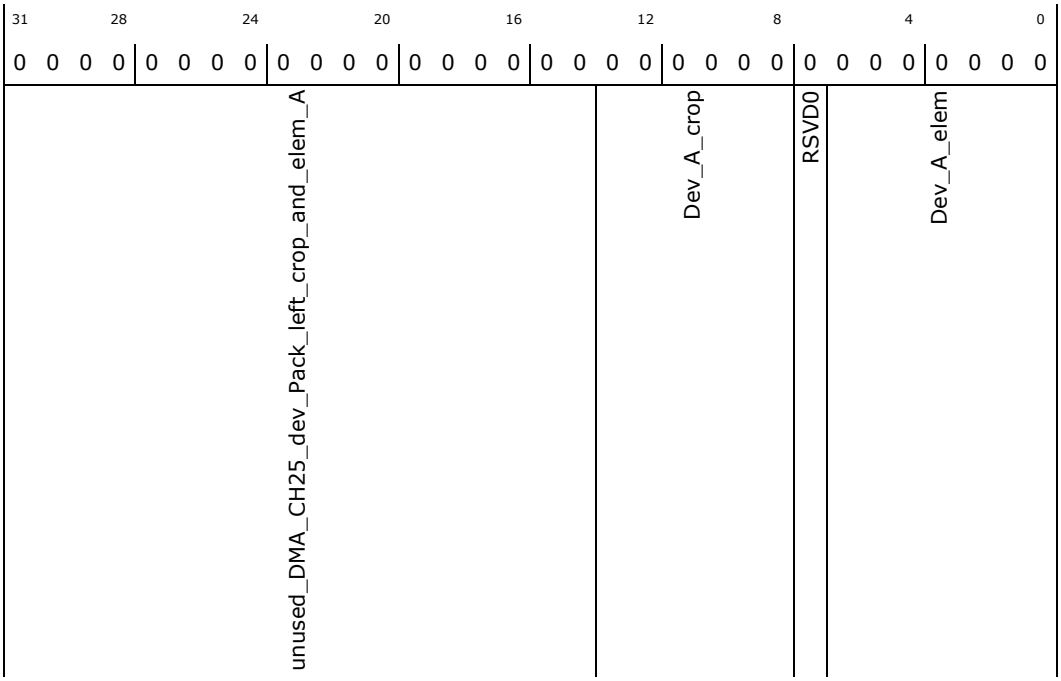
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41264h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH25_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.325 reg_isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_A)—Offset 41268h

DMA CH 26 PARAM 2: Device A Packing LSE cropping/Elements

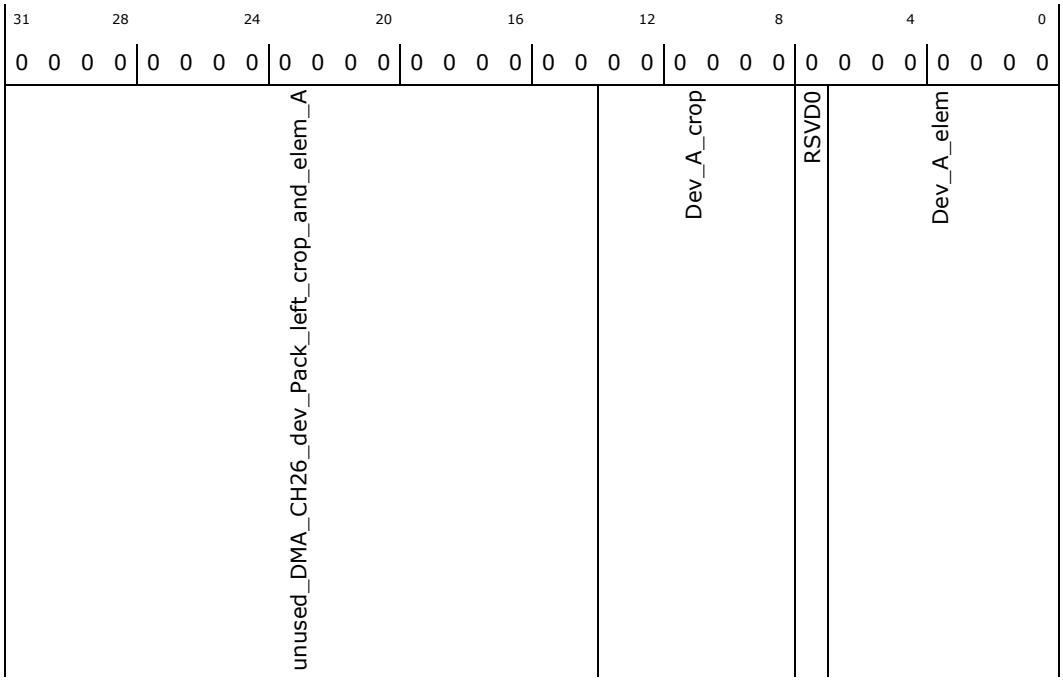
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41268h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH26_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.326 reg_isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_A)—Offset 4126Ch

DMA CH 27 PARAM 2: Device A Packing LSE cropping/Elements

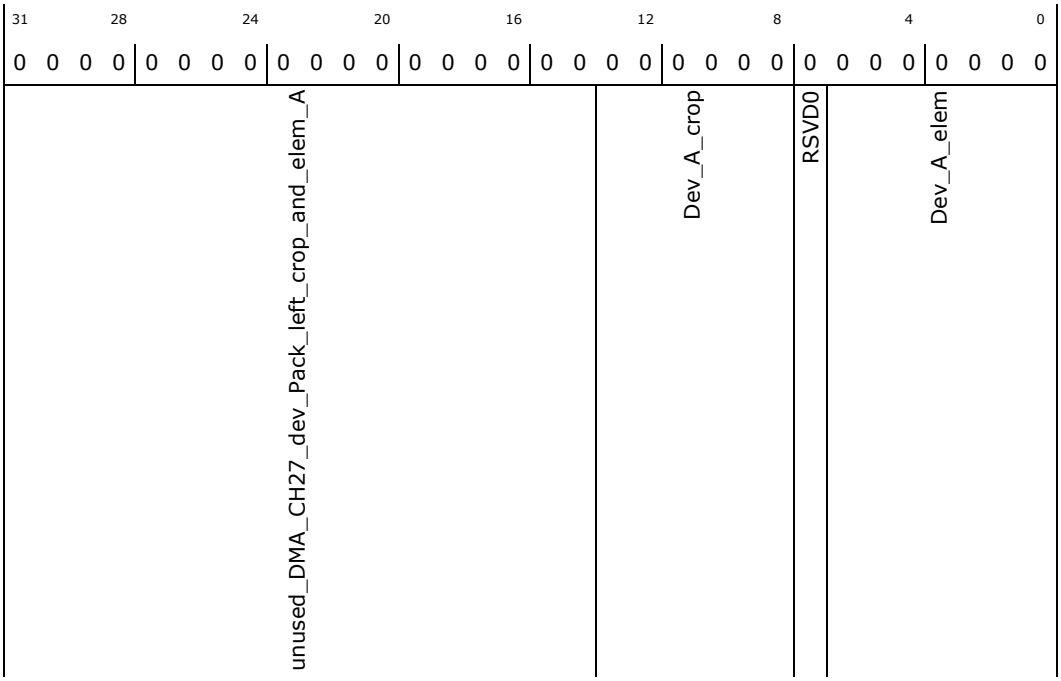
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4126Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH27_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.327 reg_isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_A)—Offset 41270h

DMA CH 28 PARAM 2: Device A Packing LSE cropping/Elements

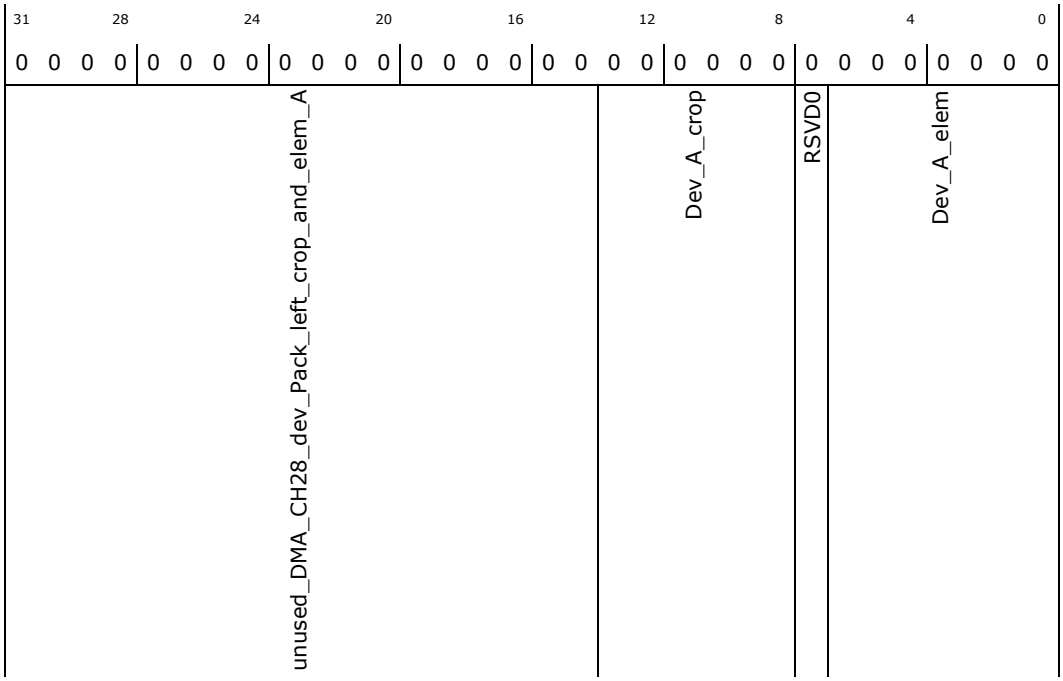
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41270h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH28_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.328 reg_isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_A) —Offset 41274h

DMA CH 29 PARAM 2: Device A Packing LSE cropping/Elements

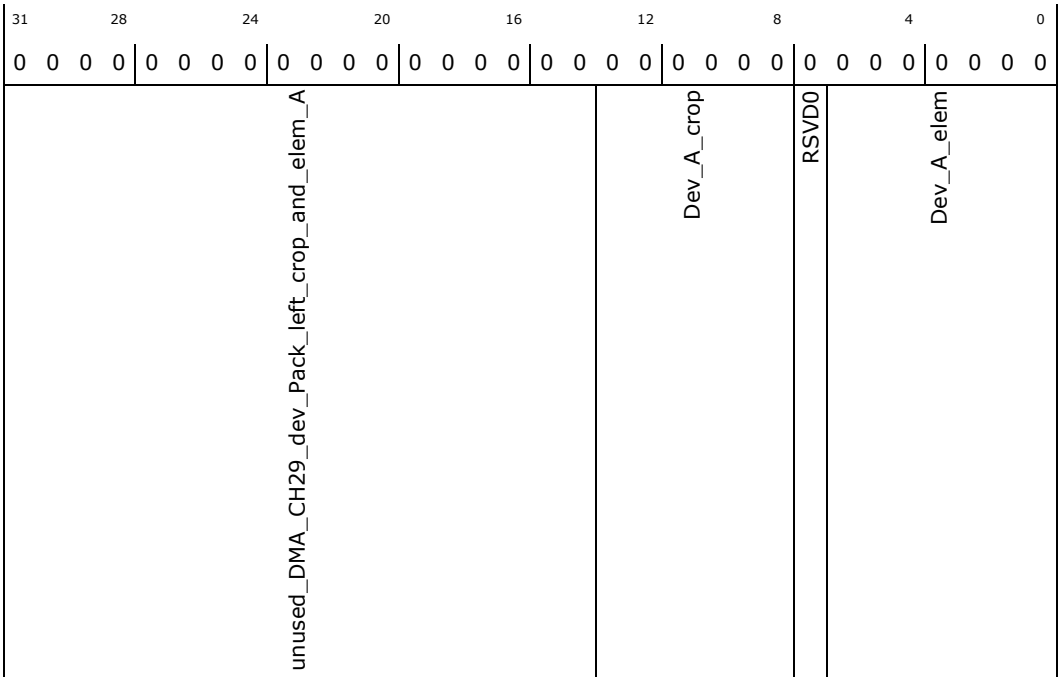
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41274h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH29_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.329 reg_isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_A)—Offset 41278h

DMA CH 30 PARAM 2: Device A Packing LSE cropping/Elements

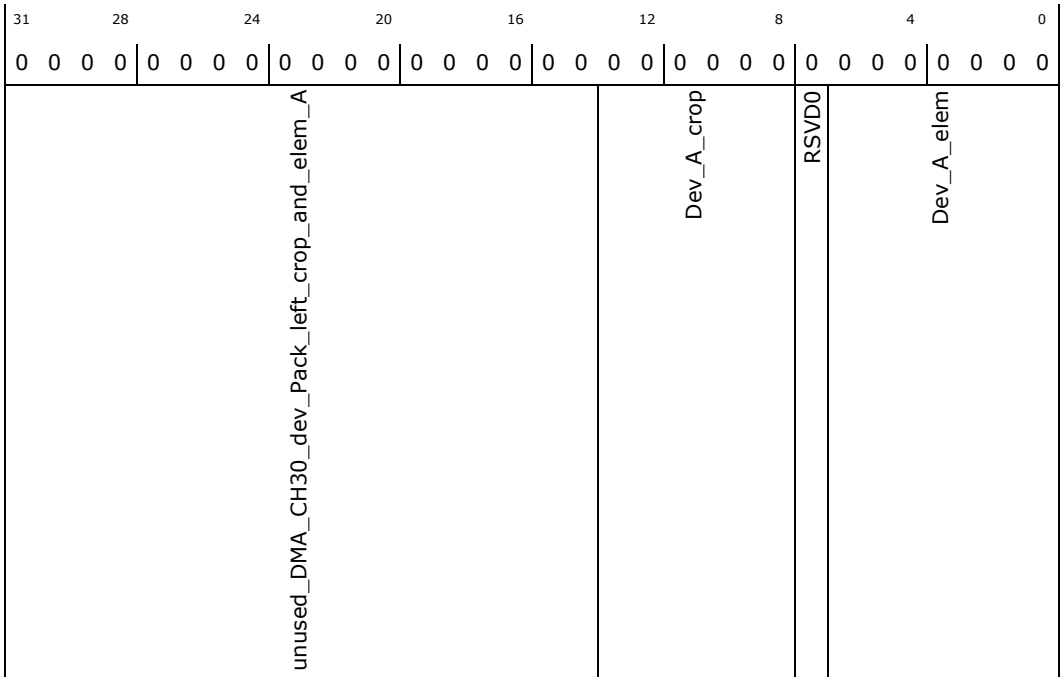
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41278h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH30_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.330 reg_isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_A)—Offset 4127Ch

DMA CH 31 PARAM 2: Device A Packing LSE cropping/Elements

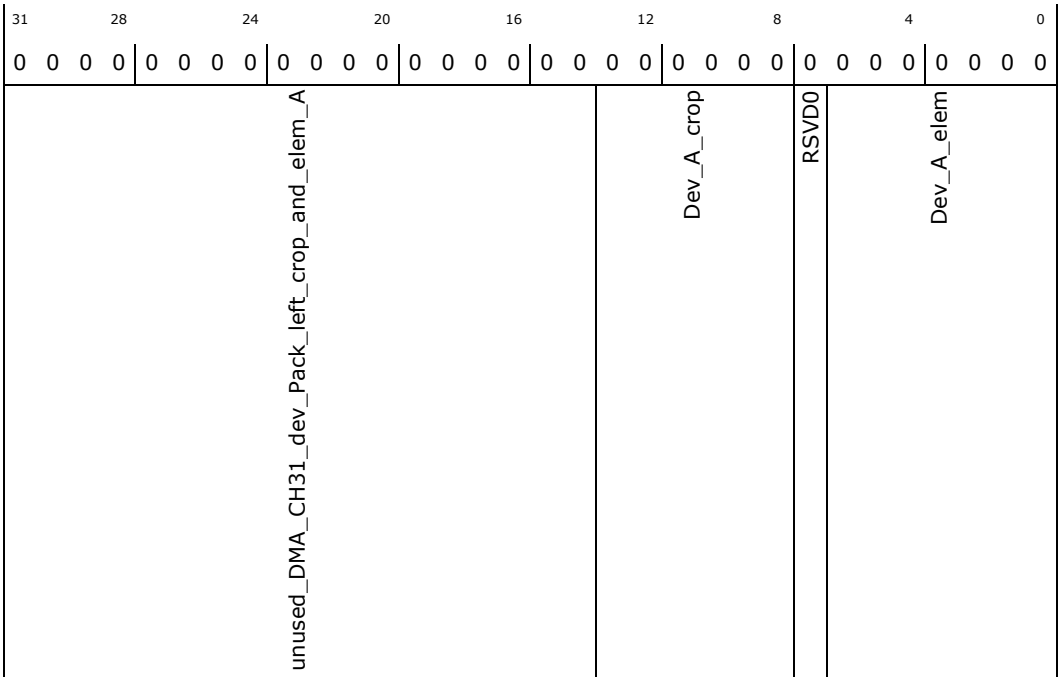
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4127Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH31_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.331 reg_isp_dma_DMA_CH22_dev_stride_A_type (isp_dma_DMA_CH22_dev_stride_A)—Offset 412C0h

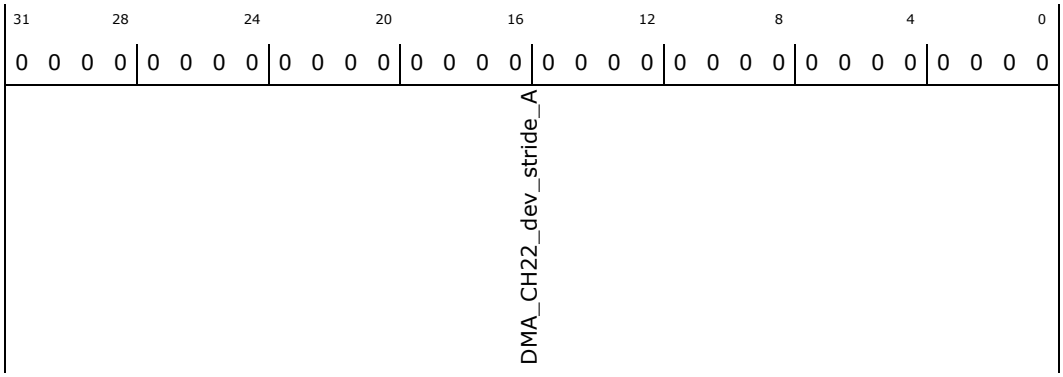
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_dev_stride_A: [ISPMMADR] + 412C0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH22_dev_stride_A:** DMA CH 22 PARAM 1: Device A stride

3.7.332 reg_isp_dma_DMA_CH23_dev_stride_A_type (isp_dma_DMA_CH23_dev_stride_A)—Offset 412C4h

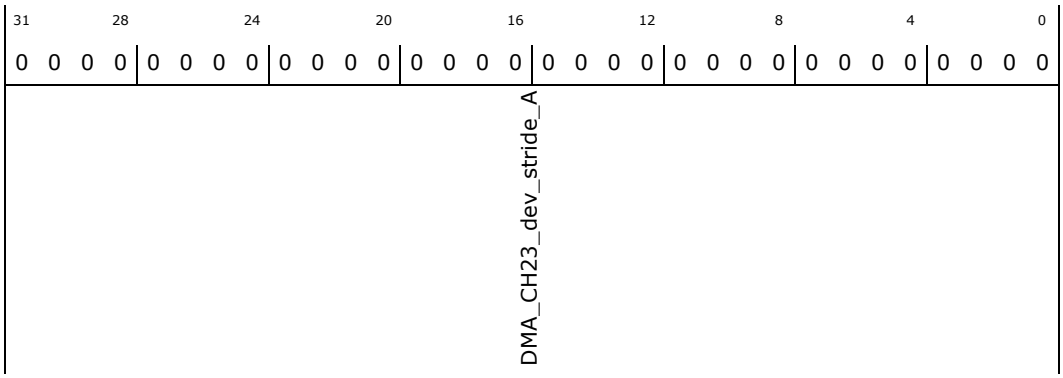
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_dev_stride_A: [ISPMMADR] + 412C4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH23_dev_stride_A:** DMA CH 23 PARAM 1: Device A stride

3.7.333 reg_isp_dma_DMA_CH24_dev_stride_A_type (isp_dma_DMA_CH24_dev_stride_A)—Offset 412C8h

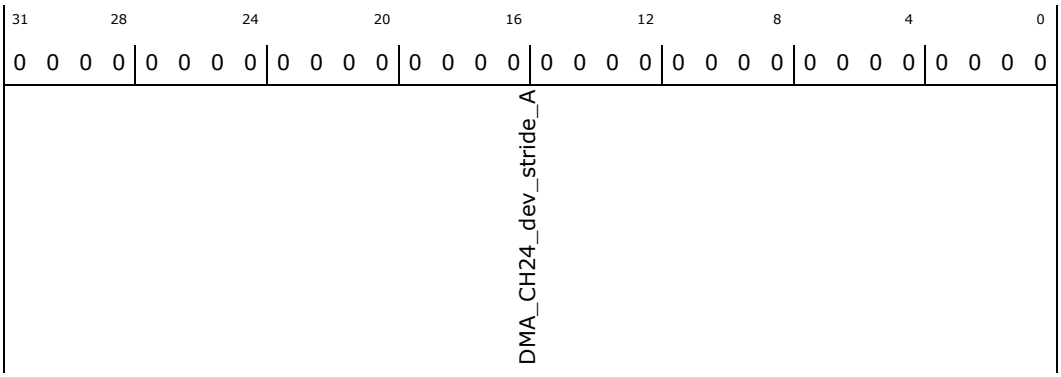
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_dev_stride_A: [ISPMMADR] + 412C8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH24_dev_stride_A:** DMA CH 24 PARAM 1: Device A stride

3.7.334 reg_isp_dma_DMA_CH25_dev_stride_A_type (isp_dma_DMA_CH25_dev_stride_A)—Offset 412CCh

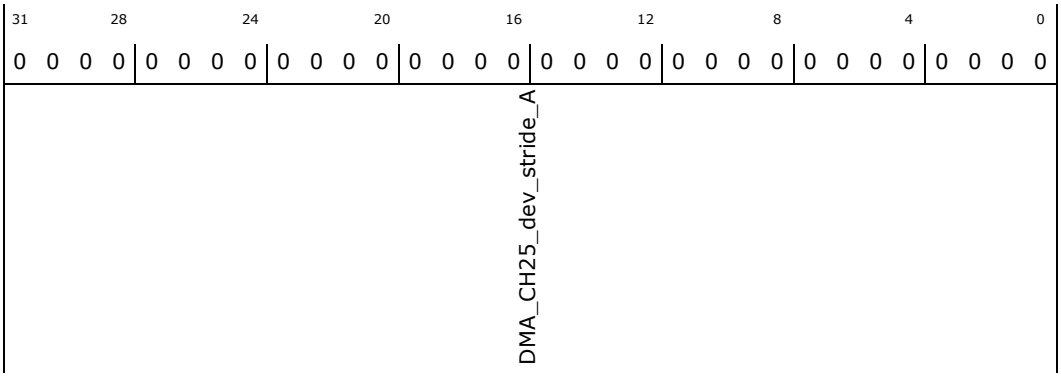
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_dev_stride_A: [ISPMMADR] + 412CCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH25_dev_stride_A:** DMA CH 25 PARAM 1: Device A stride

3.7.335 reg_isp_dma_DMA_CH26_dev_stride_A_type (isp_dma_DMA_CH26_dev_stride_A)—Offset 412D0h

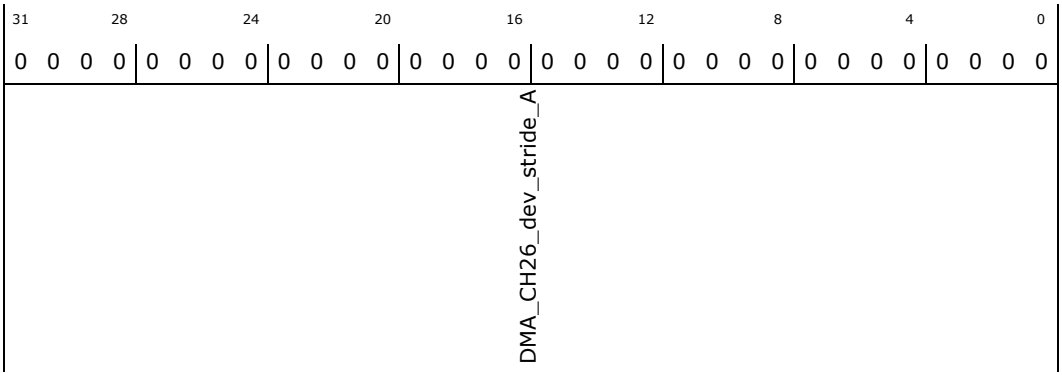
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_dev_stride_A: [ISPMMADR] + 412D0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH26_dev_stride_A:** DMA CH 26 PARAM 1: Device A stride

3.7.336 reg_isp_dma_DMA_CH27_dev_stride_A_type (isp_dma_DMA_CH27_dev_stride_A)—Offset 412D4h

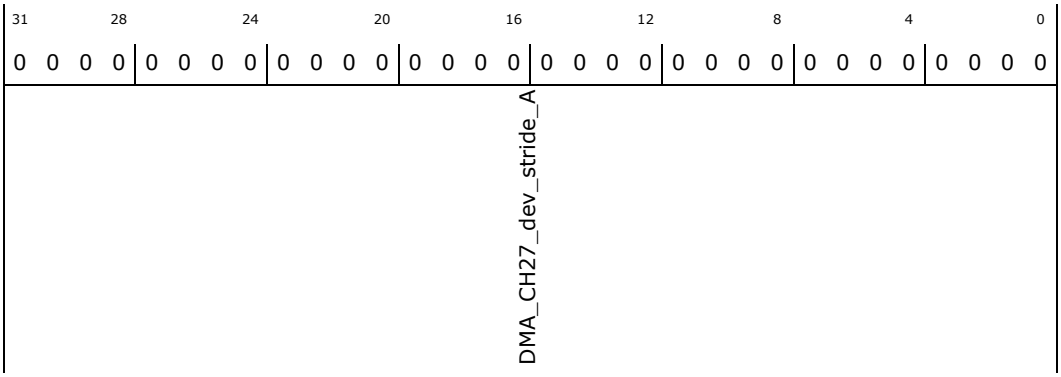
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_dev_stride_A: [ISPMMADR] + 412D4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH27_dev_stride_A:** DMA CH 27 PARAM 1: Device A stride

3.7.337 reg_isp_dma_DMA_CH28_dev_stride_A_type (isp_dma_DMA_CH28_dev_stride_A)—Offset 412D8h

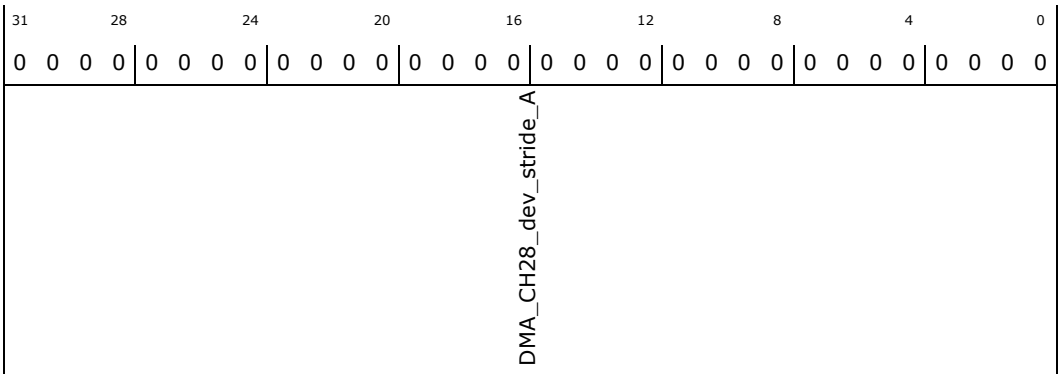
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_dev_stride_A: [ISPMMADR] + 412D8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH28_dev_stride_A:** DMA CH 28 PARAM 1: Device A stride

3.7.338 reg_isp_dma_DMA_CH29_dev_stride_A_type (isp_dma_DMA_CH29_dev_stride_A)—Offset 412DCh

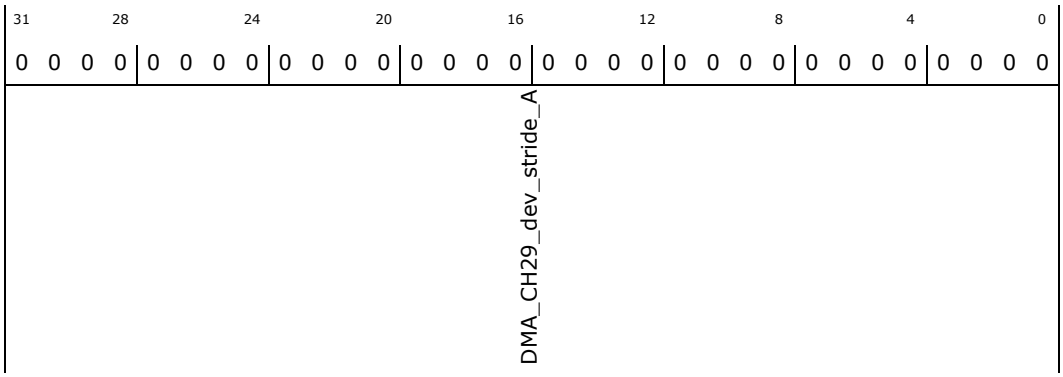
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_dev_stride_A: [ISPMMADR] + 412DCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH29_dev_stride_A:** DMA CH 29 PARAM 1: Device A stride

3.7.339 reg_isp_dma_DMA_CH30_dev_stride_A_type (isp_dma_DMA_CH30_dev_stride_A)—Offset 412E0h

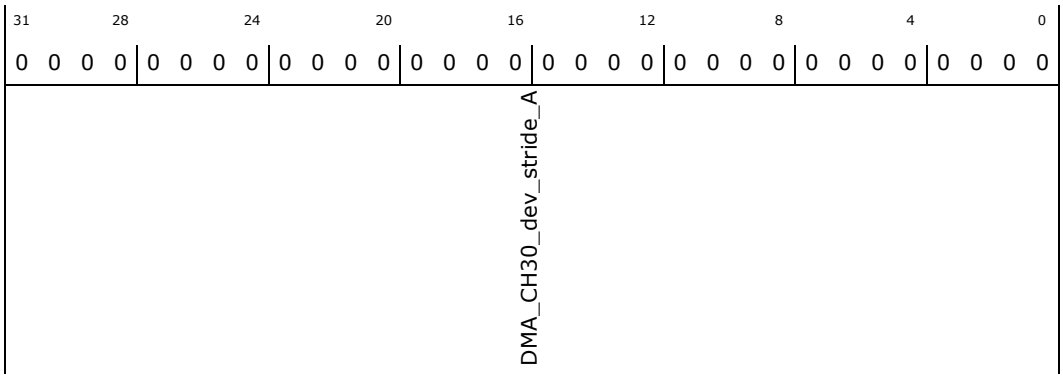
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH30_dev_stride_A: [ISPMMADR] + 412E0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH30_dev_stride_A:** DMA CH 30 PARAM 1: Device A stride

3.7.340 reg_isp_dma_DMA_CH31_dev_stride_A_type (isp_dma_DMA_CH31_dev_stride_A)—Offset 412E4h

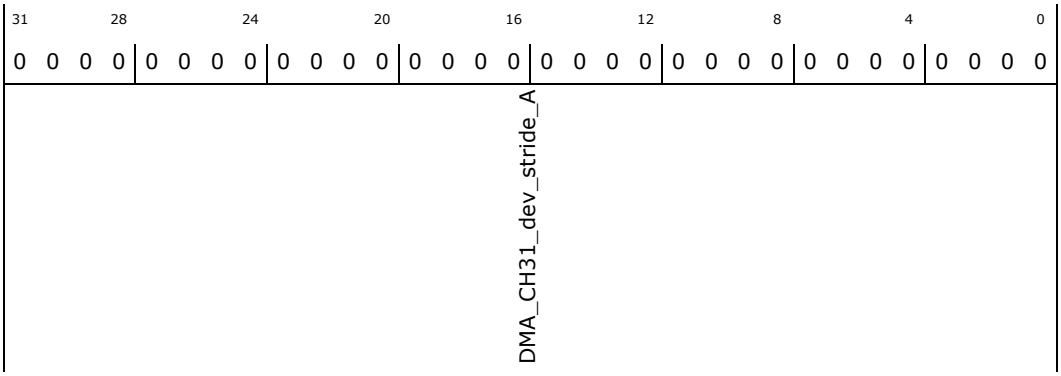
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_dev_stride_A: [ISPMMADR] + 412E4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH31_dev_stride_A:** DMA CH 31 PARAM 1: Device A stride

3.7.341 reg_isp_dma_DMA_CH0_Device_Xb_A_type (isp_dma_DMA_CH0_Device_Xb_A)—Offset 41300h

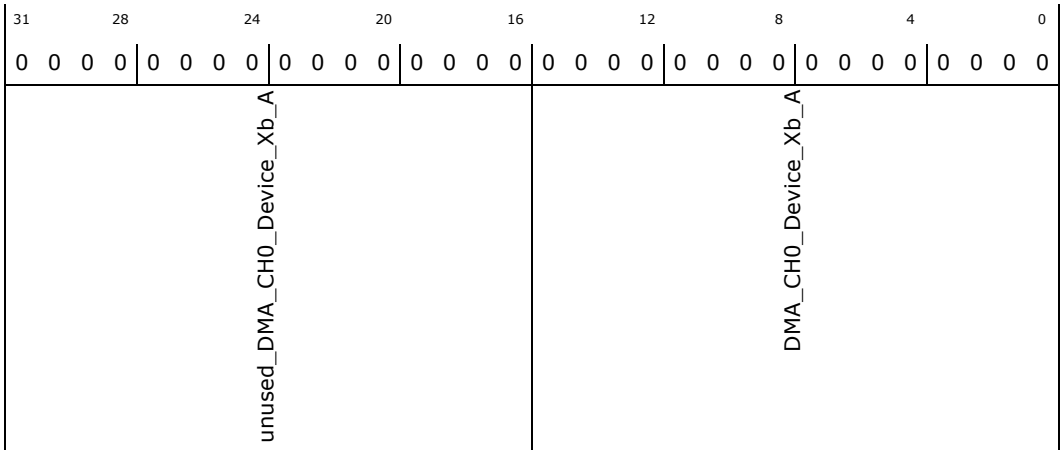
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_Device_Xb_A: [ISPMMADR] + 41300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH0_Device_Xb_A:** DMA CH 0 PARAM 3: Device A block width (Xb)

3.7.342 reg_isp_dma_DMA_CH1_Device_Xb_A_type (isp_dma_DMA_CH1_Device_Xb_A)—Offset 41304h

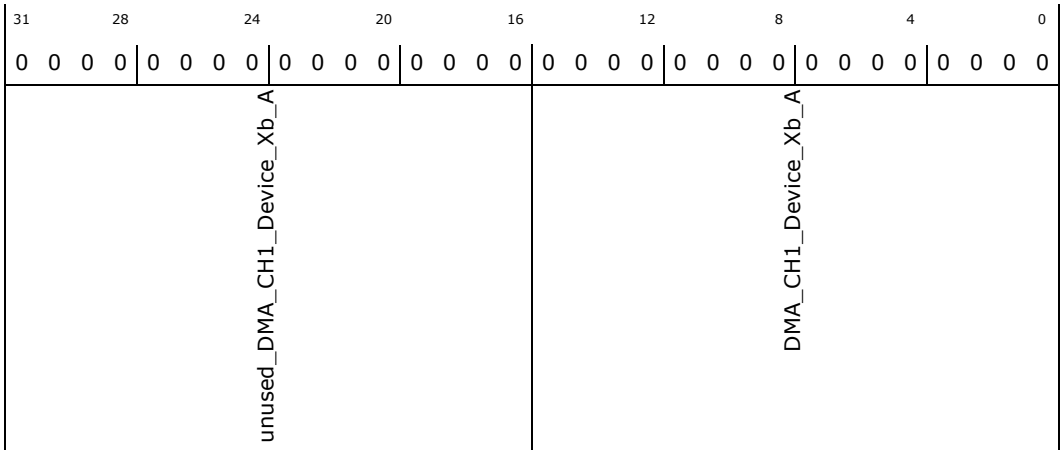
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_Device_Xb_A: [ISPMMADR] + 41304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH1_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH1_Device_Xb_A:** DMA CH 1 PARAM 3: Device A block width (Xb)

3.7.343 reg_isp_dma_DMA_CH2_Device_Xb_A_type (isp_dma_DMA_CH2_Device_Xb_A)—Offset 41308h

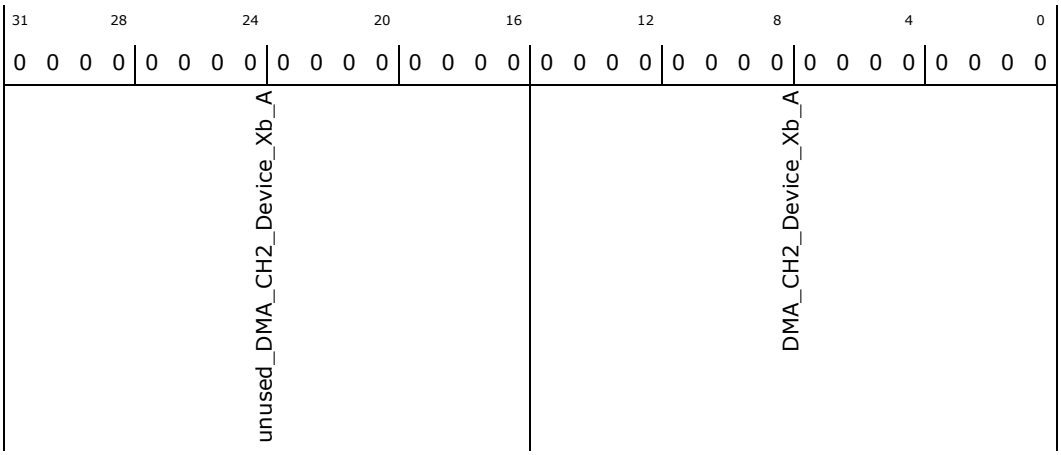
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_Device_Xb_A: [ISPMMADR] + 41308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH2_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH2_Device_Xb_A:** DMA CH 2 PARAM 3: Device A block width (Xb)

3.7.344 reg_isp_dma_DMA_CH3_Device_Xb_A_type (isp_dma_DMA_CH3_Device_Xb_A)—Offset 4130Ch

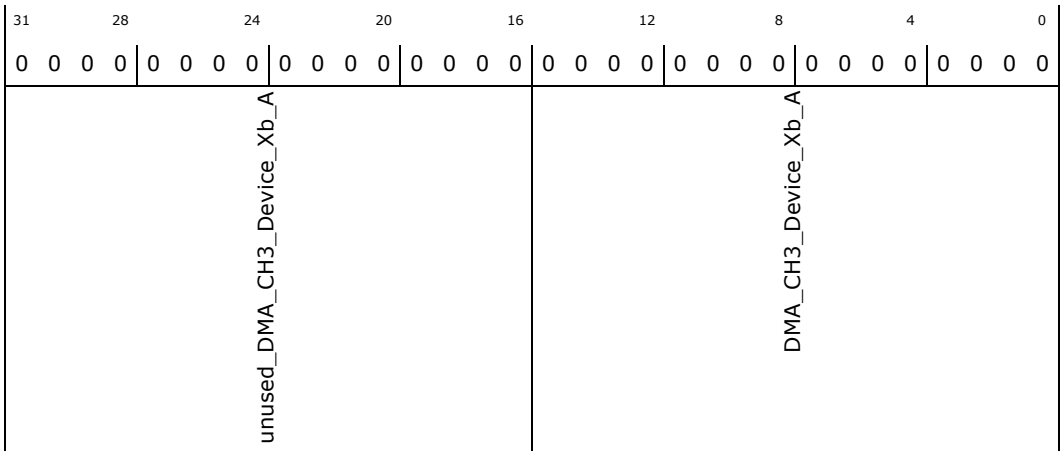
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_Device_Xb_A: [ISPMMADR] + 4130Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH3_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH3_Device_Xb_A:** DMA CH 3 PARAM 3: Device A block width (Xb)

3.7.345 reg_isp_dma_DMA_CH4_Device_Xb_A_type (isp_dma_DMA_CH4_Device_Xb_A)—Offset 41310h

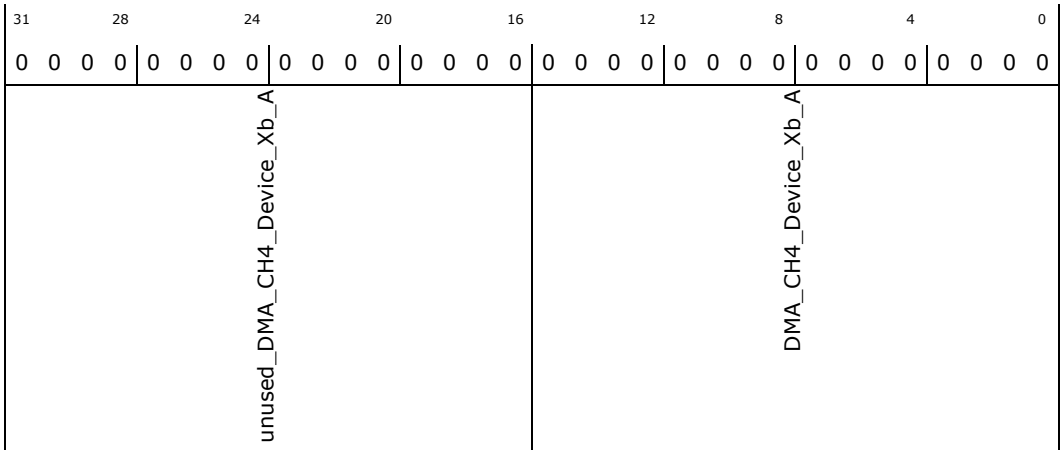
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_Device_Xb_A: [ISPMMADR] + 41310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH4_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH4_Device_Xb_A:** DMA CH 4 PARAM 3: Device A block width (Xb)

3.7.346 reg_isp_dma_DMA_CH5_Device_Xb_A_type (isp_dma_DMA_CH5_Device_Xb_A)—Offset 41314h

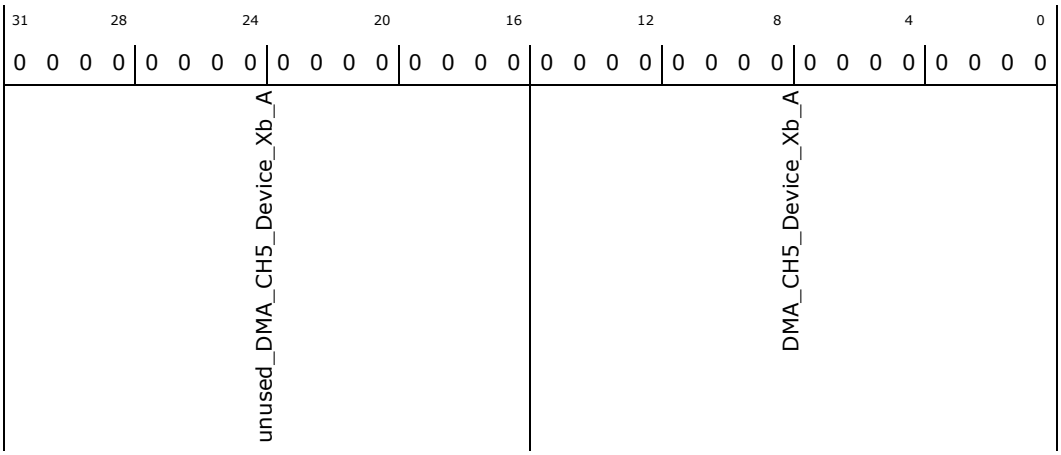
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_Device_Xb_A: [ISPMMADR] + 41314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH5_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH5_Device_Xb_A:** DMA CH 5 PARAM 3: Device A block width (Xb)

3.7.347 reg_isp_dma_DMA_CH6_Device_Xb_A_type (isp_dma_DMA_CH6_Device_Xb_A)—Offset 41318h

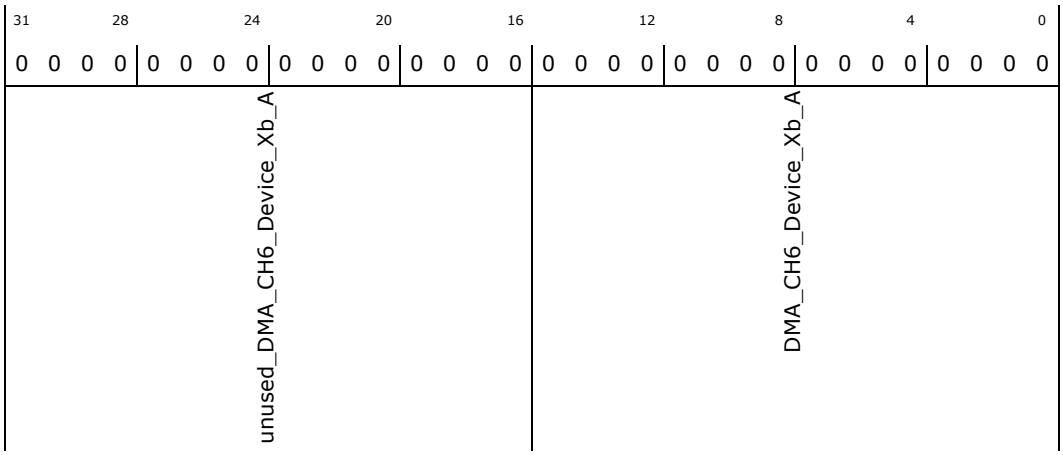
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_Device_Xb_A: [ISPMMADR] + 41318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH6_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH6_Device_Xb_A:** DMA CH 6 PARAM 3: Device A block width (Xb)

3.7.348 reg_isp_dma_DMA_CH7_Device_Xb_A_type (isp_dma_DMA_CH7_Device_Xb_A)—Offset 4131Ch

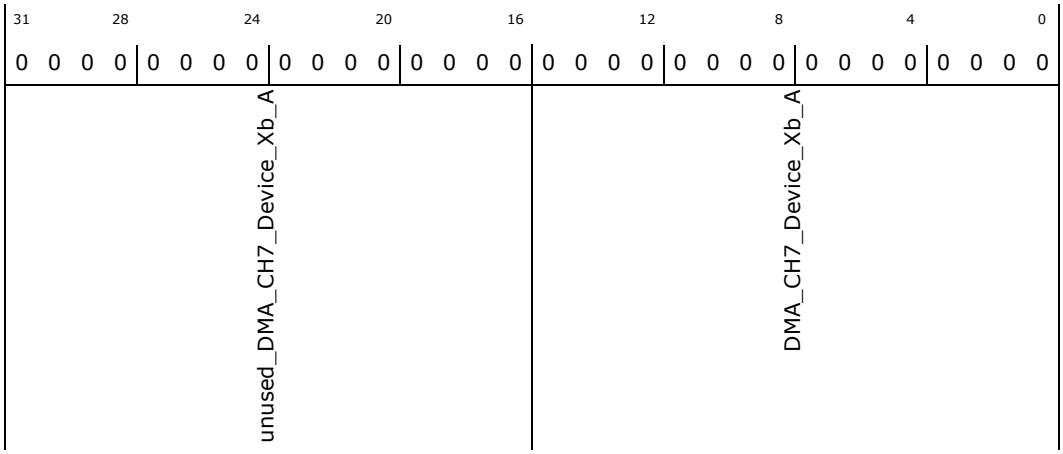
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_Device_Xb_A: [ISPMMADR] + 4131Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH7_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH7_Device_Xb_A:** DMA CH 7 PARAM 3: Device A block width (Xb)

3.7.349 reg_isp_dma_DMA_CH8_Device_Xb_A_type (isp_dma_DMA_CH8_Device_Xb_A)—Offset 41320h

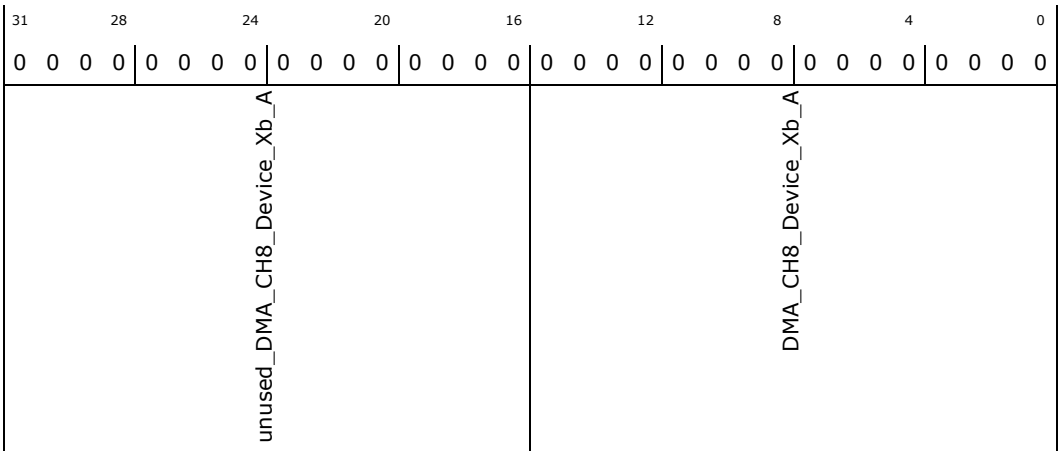
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_Device_Xb_A: [ISPMMADR] + 41320h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH8_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH8_Device_Xb_A:** DMA CH 8 PARAM 3: Device A block width (Xb)

3.7.350 reg_isp_dma_DMA_CH9_Device_Xb_A_type (isp_dma_DMA_CH9_Device_Xb_A)—Offset 41324h

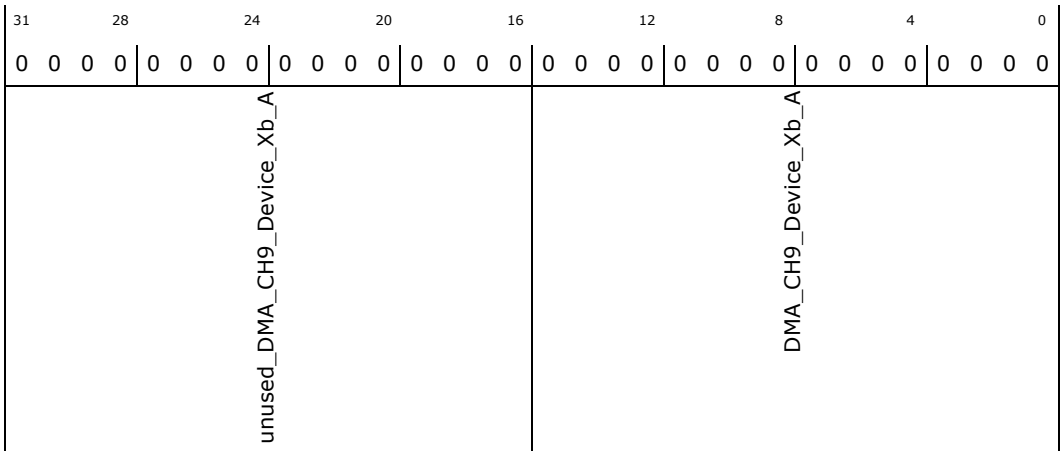
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_Device_Xb_A: [ISPMMADR] + 41324h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH9_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH9_Device_Xb_A:** DMA CH 9 PARAM 3: Device A block width (Xb)

3.7.351 reg_isp_dma_DMA_CH10_Device_Xb_A_type (isp_dma_DMA_CH10_Device_Xb_A)—Offset 41328h

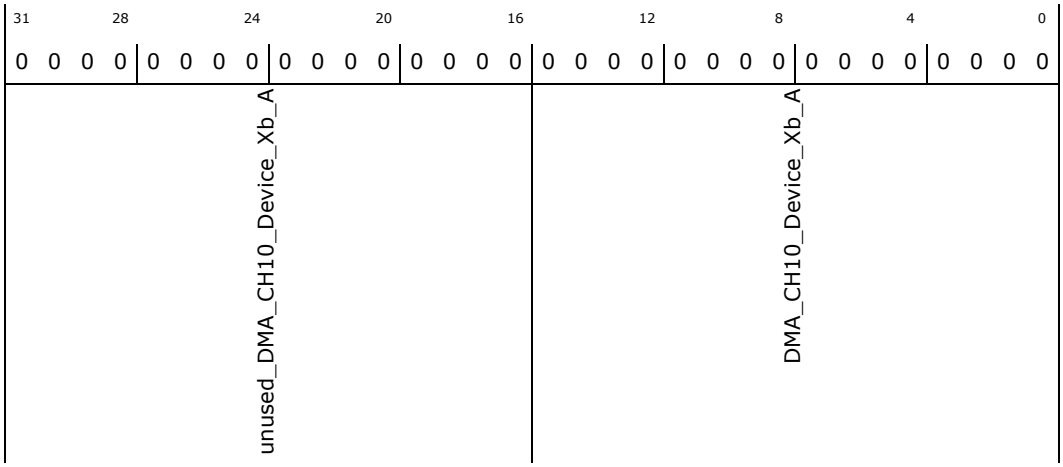
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_Device_Xb_A: [ISPMMADR] + 41328h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH10_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH10_Device_Xb_A:** DMA CH 10 PARAM 3: Device A block width (Xb)

3.7.352 reg_isp_dma_DMA_CH11_Device_Xb_A_type (isp_dma_DMA_CH11_Device_Xb_A)—Offset 4132Ch

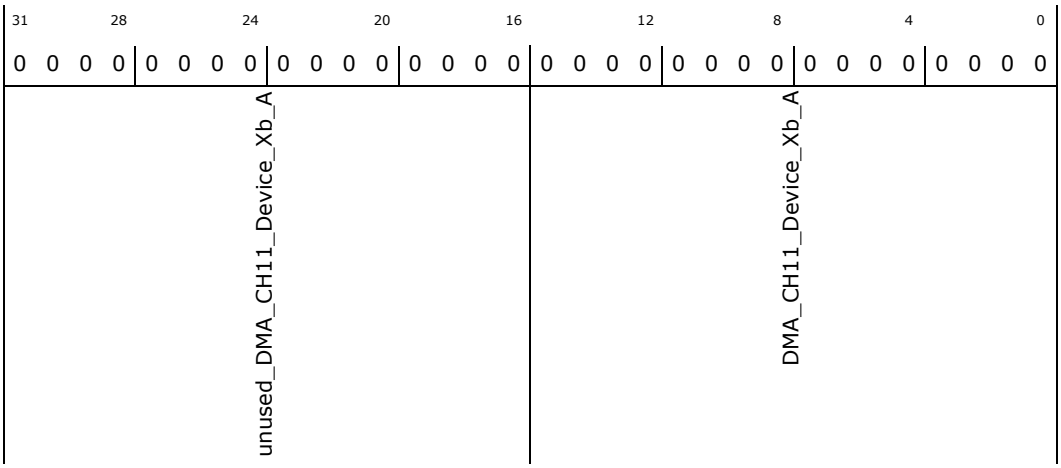
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_Device_Xb_A: [ISPMMADR] + 4132Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH11_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH11_Device_Xb_A:** DMA CH 11 PARAM 3: Device A block width (Xb)

3.7.353 reg_isp_dma_DMA_CH12_Device_Xb_A_type (isp_dma_DMA_CH12_Device_Xb_A)—Offset 41330h

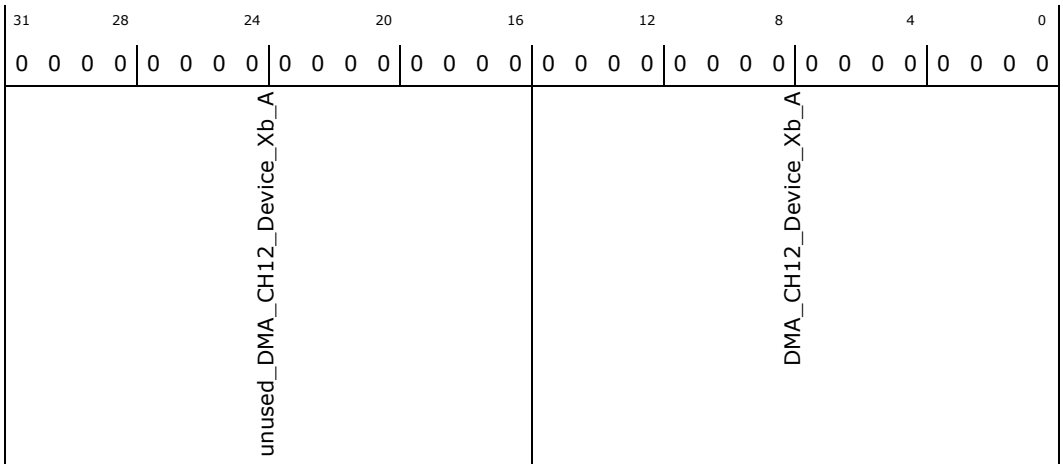
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_Device_Xb_A: [ISPMMADR] + 41330h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH12_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH12_Device_Xb_A:** DMA CH 12 PARAM 3: Device A block width (Xb)

3.7.354 reg_isp_dma_DMA_CH13_Device_Xb_A_type (isp_dma_DMA_CH13_Device_Xb_A)—Offset 41334h

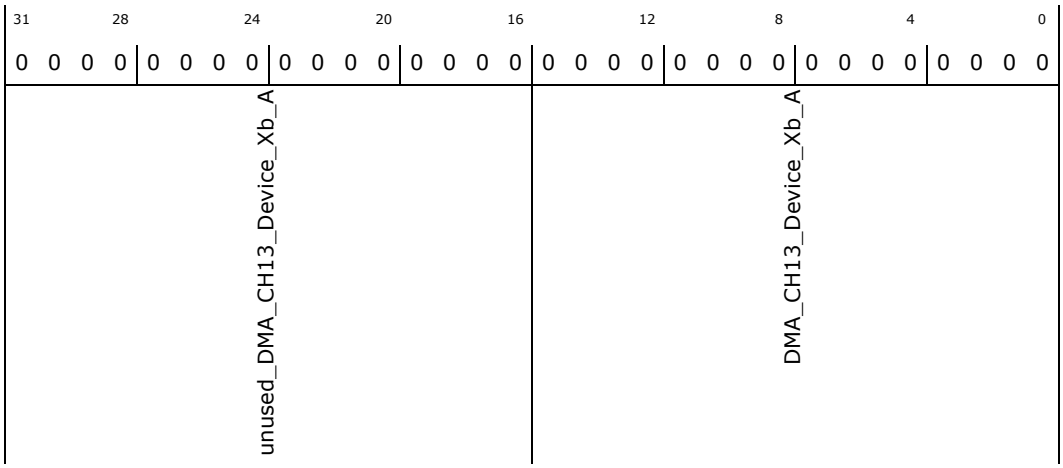
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_Device_Xb_A: [ISPMMADR] + 41334h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH13_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH13_Device_Xb_A:** DMA CH 13 PARAM 3: Device A block width (Xb)

3.7.355 reg_isp_dma_DMA_CH14_Device_Xb_A_type (isp_dma_DMA_CH14_Device_Xb_A)—Offset 41338h

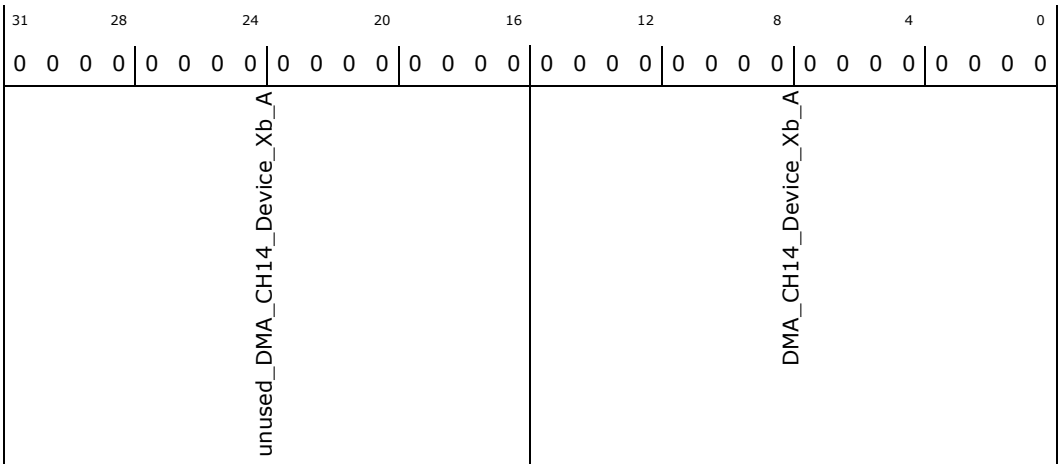
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_Device_Xb_A: [ISPMMADR] + 41338h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH14_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH14_Device_Xb_A:** DMA CH 14 PARAM 3: Device A block width (Xb)

3.7.356 reg_isp_dma_DMA_CH15_Device_Xb_A_type (isp_dma_DMA_CH15_Device_Xb_A)—Offset 4133Ch

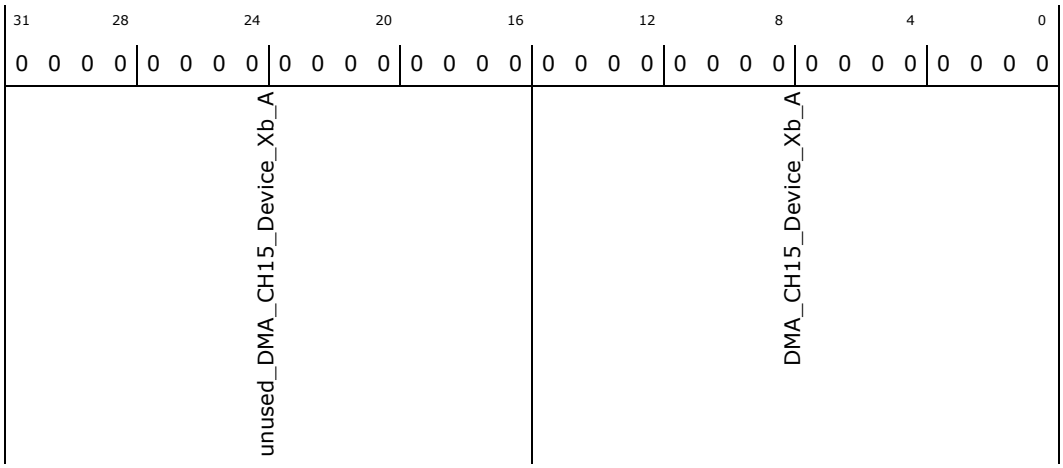
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_Device_Xb_A: [ISPMMADR] + 4133Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH15_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH15_Device_Xb_A:** DMA CH 15 PARAM 3: Device A block width (Xb)

3.7.357 reg_isp_dma_DMA_CH16_Device_Xb_A_type (isp_dma_DMA_CH16_Device_Xb_A)—Offset 41340h

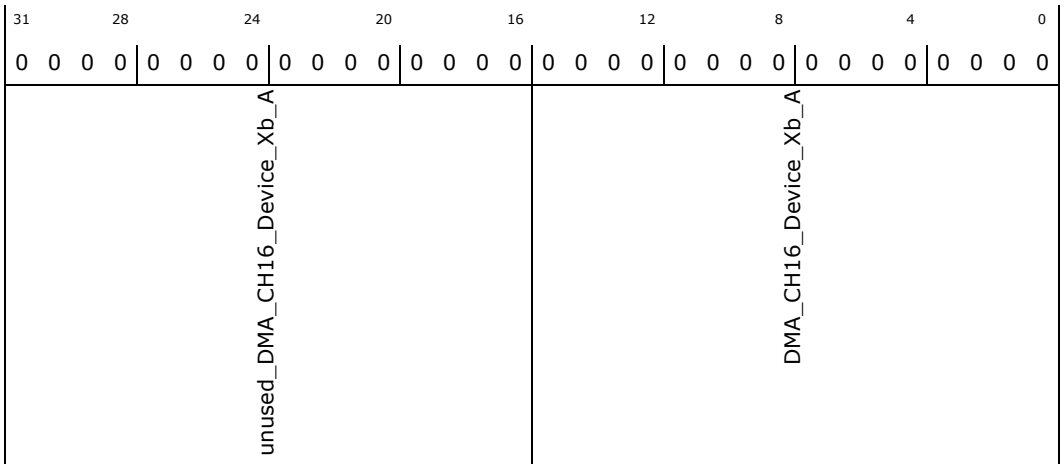
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_Device_Xb_A: [ISPMMADR] + 41340h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH16_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH16_Device_Xb_A:** DMA CH 16 PARAM 3: Device A block width (Xb)

3.7.358 reg_isp_dma_DMA_CH17_Device_Xb_A_type (isp_dma_DMA_CH17_Device_Xb_A)—Offset 41344h

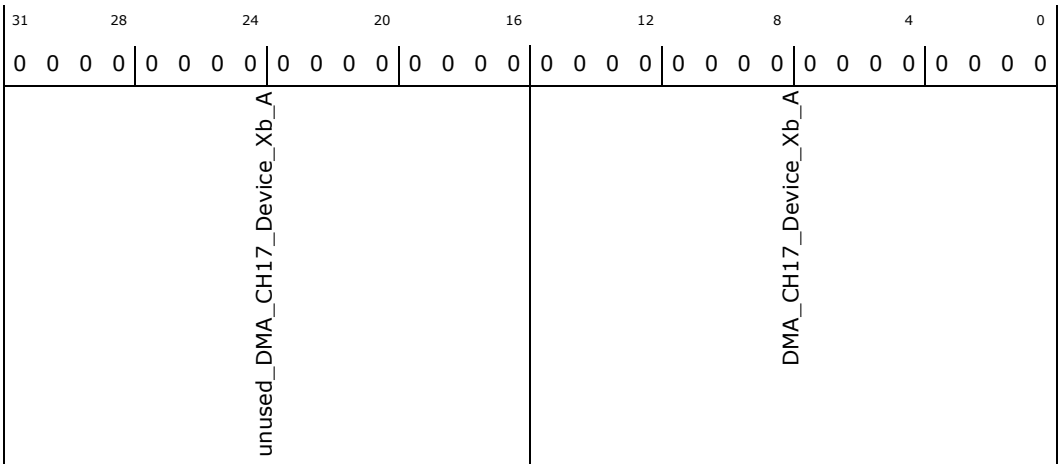
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_Device_Xb_A: [ISPMMADR] + 41344h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH17_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH17_Device_Xb_A:** DMA CH 17 PARAM 3: Device A block width (Xb)

3.7.359 reg_isp_dma_DMA_CH18_Device_Xb_A_type (isp_dma_DMA_CH18_Device_Xb_A)—Offset 41348h

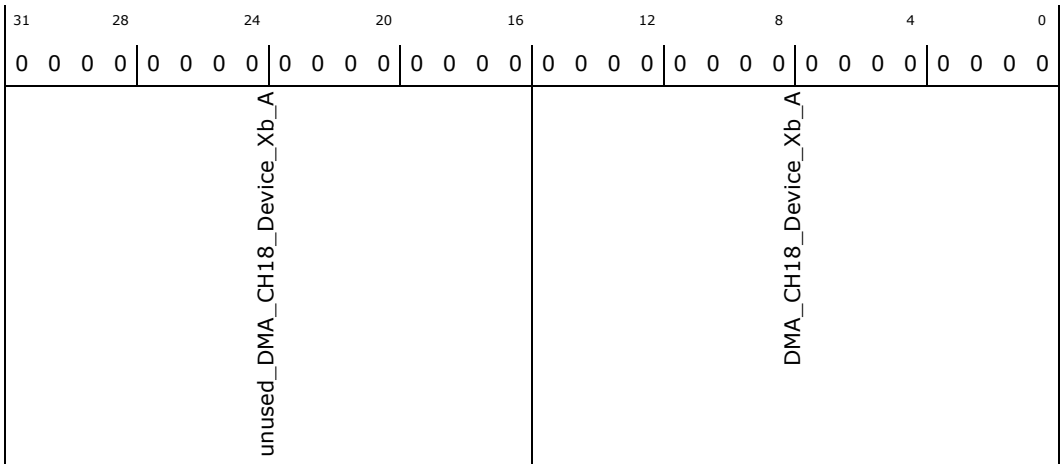
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_Device_Xb_A: [ISPMMADR] + 41348h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH18_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH18_Device_Xb_A:** DMA CH 18 PARAM 3: Device A block width (Xb)

3.7.360 reg_isp_dma_DMA_CH19_Device_Xb_A_type (isp_dma_DMA_CH19_Device_Xb_A)—Offset 4134Ch

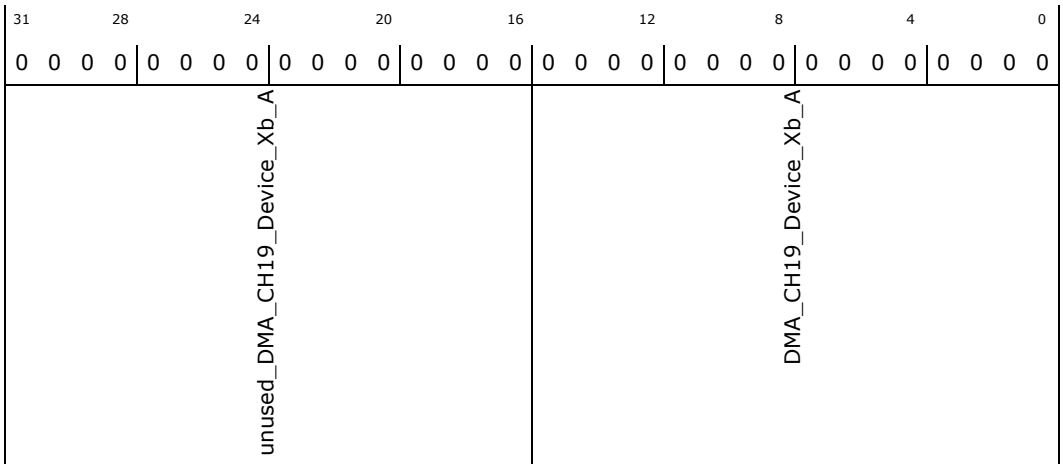
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_Device_Xb_A: [ISPMMADR] + 4134Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH19_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH19_Device_Xb_A:** DMA CH 19 PARAM 3: Device A block width (Xb)

3.7.361 reg_isp_dma_DMA_CH20_Device_Xb_A_type (isp_dma_DMA_CH20_Device_Xb_A)—Offset 41350h

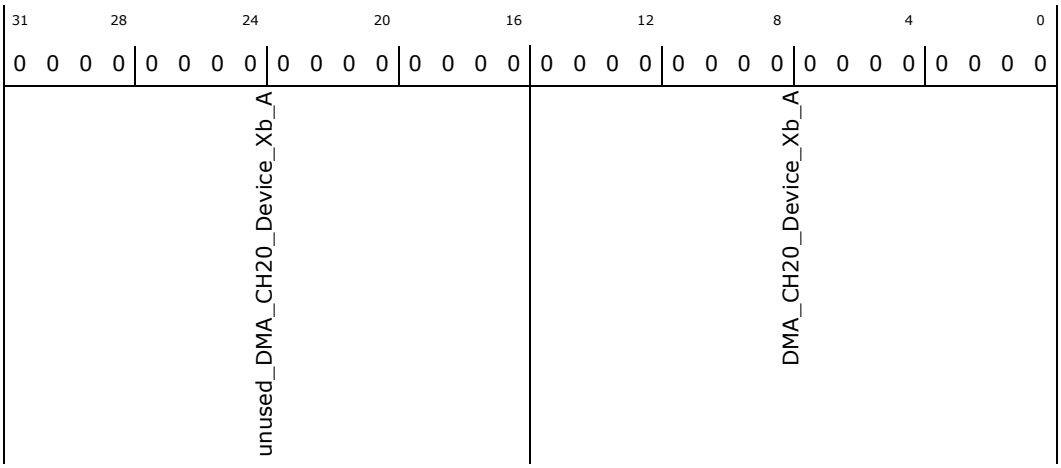
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_Device_Xb_A: [ISPMMADR] + 41350h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH20_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH20_Device_Xb_A:** DMA CH 20 PARAM 3: Device A block width (Xb)

3.7.362 reg_isp_dma_DMA_CH21_Device_Xb_A_type (isp_dma_DMA_CH21_Device_Xb_A)—Offset 41354h

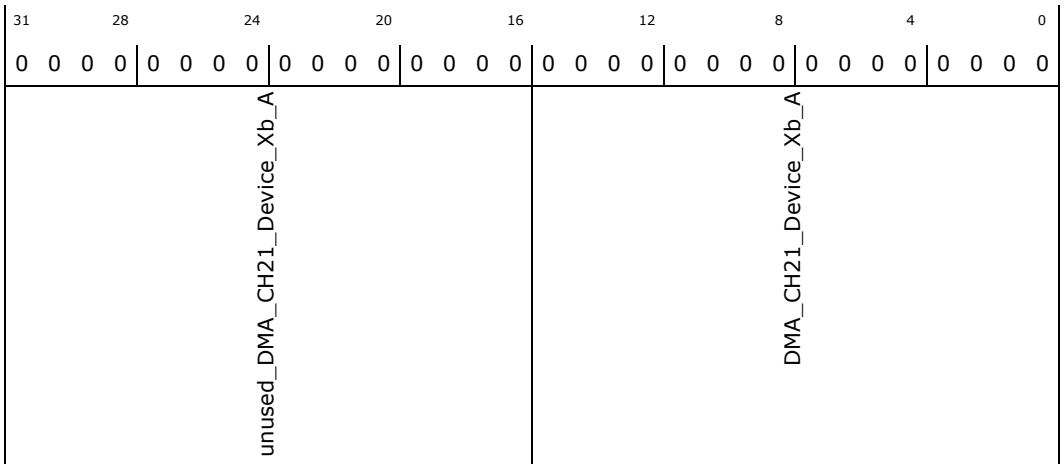
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_Device_Xb_A: [ISPMMADR] + 41354h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH21_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH21_Device_Xb_A:** DMA CH 21 PARAM 3: Device A block width (Xb)

3.7.363 reg_isp_dma_DMA_CH22_Device_Xb_A_type (isp_dma_DMA_CH22_Device_Xb_A)—Offset 41358h

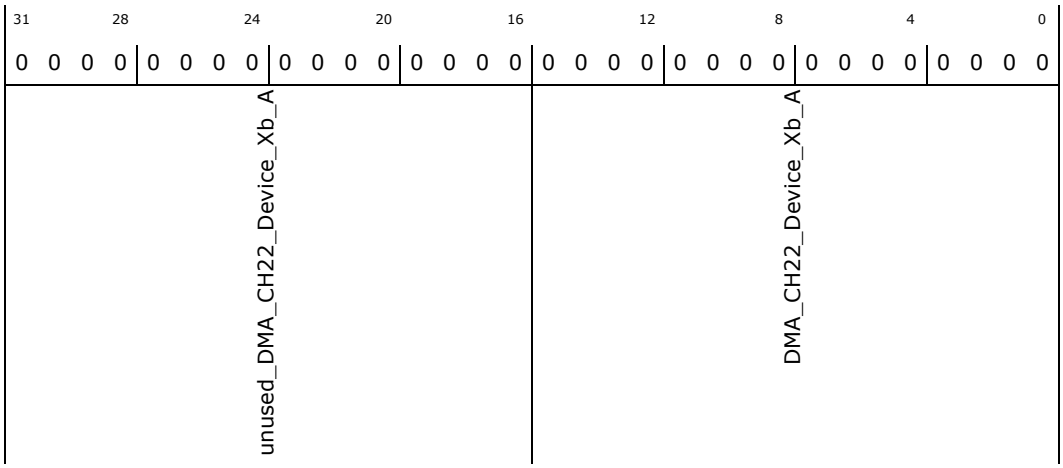
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_Device_Xb_A: [ISPMMADR] + 41358h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH22_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH22_Device_Xb_A:** DMA CH 22 PARAM 3: Device A block width (Xb)

3.7.364 reg_isp_dma_DMA_CH23_Device_Xb_A_type (isp_dma_DMA_CH23_Device_Xb_A)—Offset 4135Ch

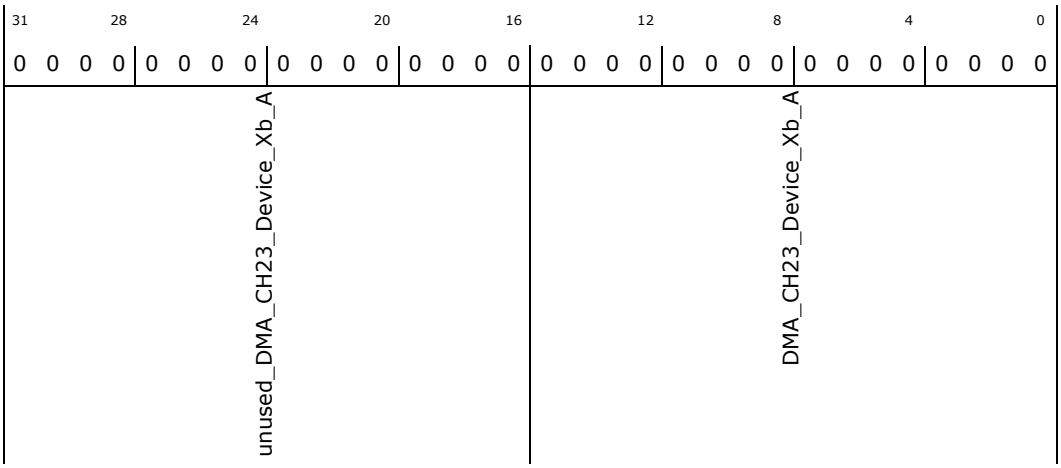
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_Device_Xb_A: [ISPMMADR] + 4135Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH23_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH23_Device_Xb_A:** DMA CH 23 PARAM 3: Device A block width (Xb)

3.7.365 reg_isp_dma_DMA_CH24_Device_Xb_A_type (isp_dma_DMA_CH24_Device_Xb_A)—Offset 41360h

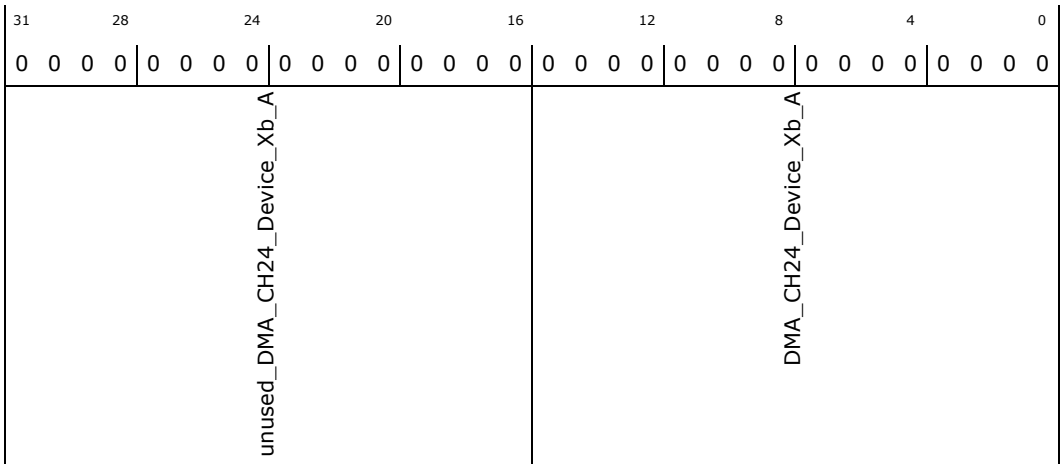
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_Device_Xb_A: [ISPMMADR] + 41360h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH24_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH24_Device_Xb_A:** DMA CH 24 PARAM 3: Device A block width (Xb)

3.7.366 reg_isp_dma_DMA_CH25_Device_Xb_A_type (isp_dma_DMA_CH25_Device_Xb_A)—Offset 41364h

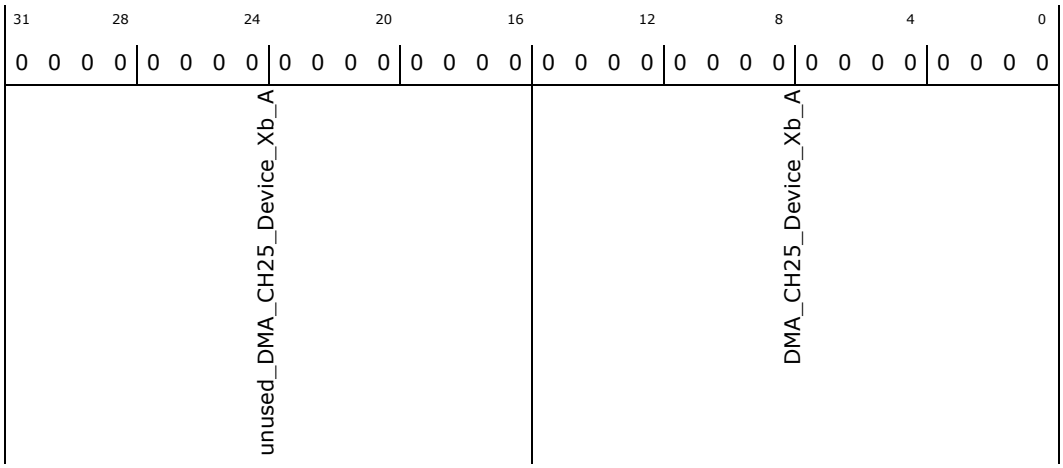
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_Device_Xb_A: [ISPMMADR] + 41364h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH25_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH25_Device_Xb_A:** DMA CH 25 PARAM 3: Device A block width (Xb)

3.7.367 reg_isp_dma_DMA_CH26_Device_Xb_A_type (isp_dma_DMA_CH26_Device_Xb_A)—Offset 41368h

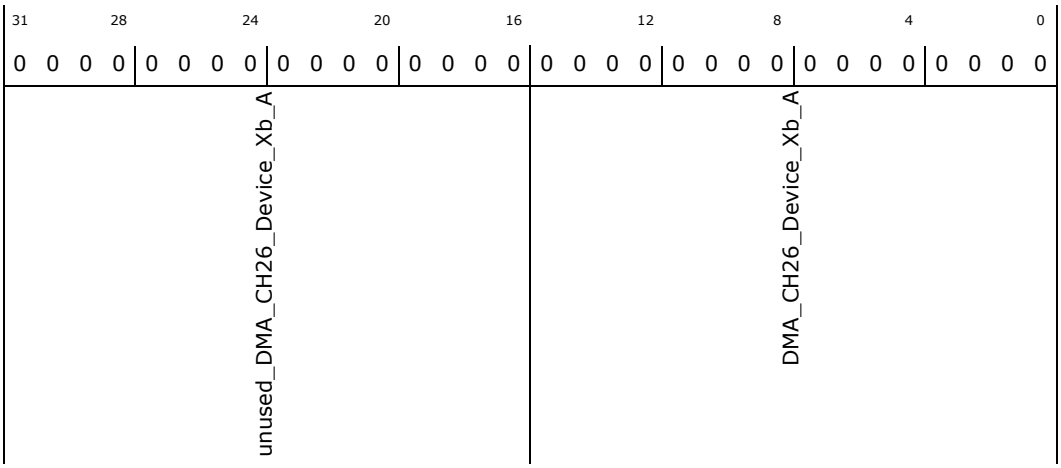
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_Device_Xb_A: [ISPMMADR] + 41368h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH26_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH26_Device_Xb_A:** DMA CH 26 PARAM 3: Device A block width (Xb)

3.7.368 reg_isp_dma_DMA_CH27_Device_Xb_A_type (isp_dma_DMA_CH27_Device_Xb_A)—Offset 4136Ch

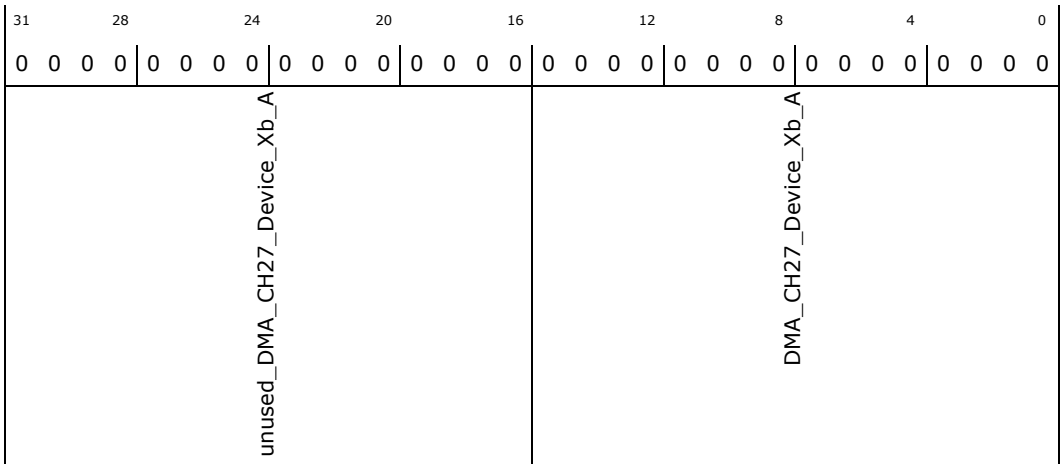
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_Device_Xb_A: [ISPMMADR] + 4136Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH27_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH27_Device_Xb_A:** DMA CH 27 PARAM 3: Device A block width (Xb)

3.7.369 reg_isp_dma_DMA_CH28_Device_Xb_A_type (isp_dma_DMA_CH28_Device_Xb_A)—Offset 41370h

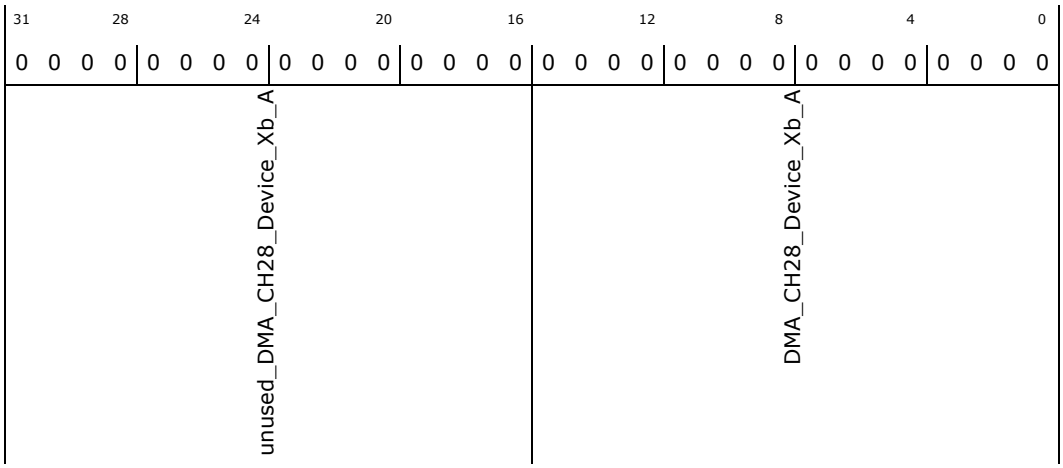
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_Device_Xb_A: [ISPMMADR] + 41370h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH28_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH28_Device_Xb_A:** DMA CH 28 PARAM 3: Device A block width (Xb)

3.7.370 reg_isp_dma_DMA_CH29_Device_Xb_A_type (isp_dma_DMA_CH29_Device_Xb_A)—Offset 41374h

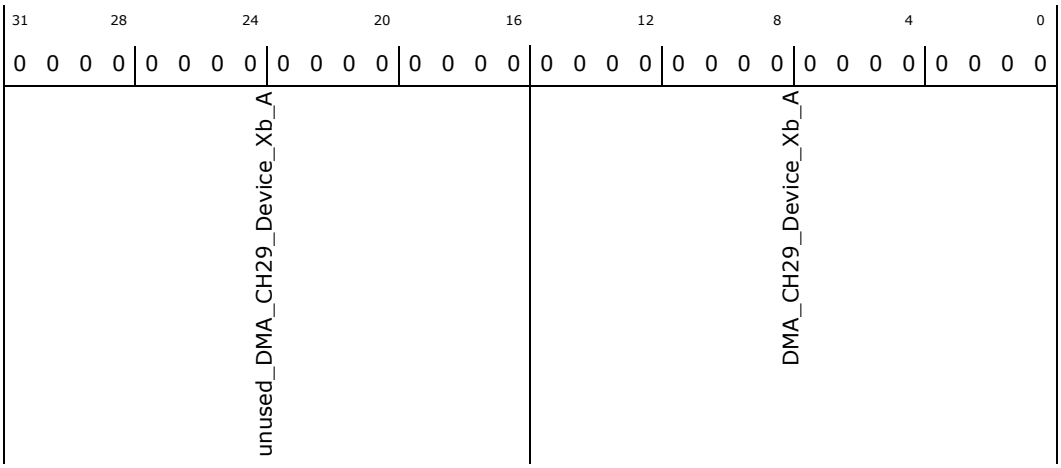
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_Device_Xb_A: [ISPMMADR] + 41374h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH29_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH29_Device_Xb_A:** DMA CH 29 PARAM 3: Device A block width (Xb)

3.7.371 reg_isp_dma_DMA_CH30_Device_Xb_A_type (isp_dma_DMA_CH30_Device_Xb_A)—Offset 41378h

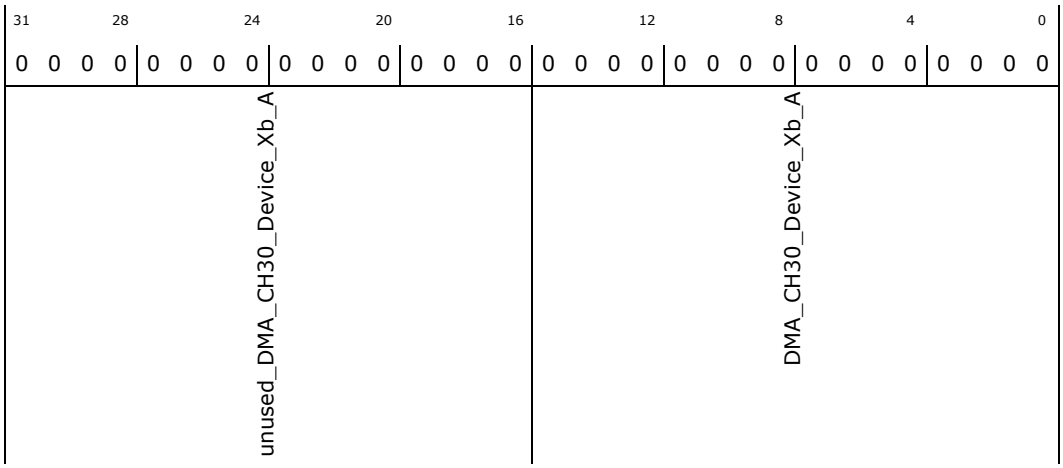
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH30_Device_Xb_A: [ISPMMADR] + 41378h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH30_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH30_Device_Xb_A:** DMA CH 30 PARAM 3: Device A block width (Xb)

3.7.372 reg_isp_dma_DMA_CH31_Device_Xb_A_type (isp_dma_DMA_CH31_Device_Xb_A)—Offset 4137Ch

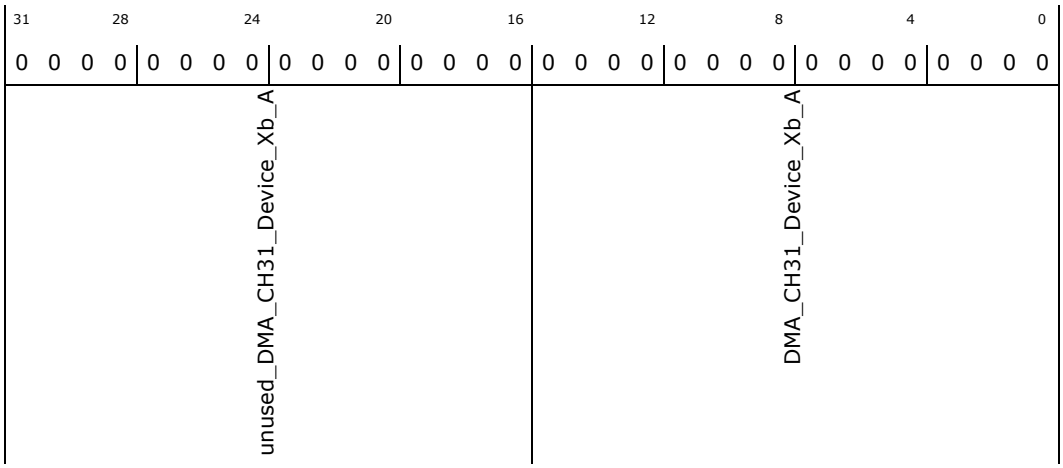
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_Device_Xb_A: [ISPMMADR] + 4137Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH31_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH31_Device_Xb_A:** DMA CH 31 PARAM 3: Device A block width (Xb)

3.7.373 reg_isp_dma_DMA_CH0_dev_stride_B_type (isp_dma_DMA_CH0_dev_stride_B)—Offset 41400h

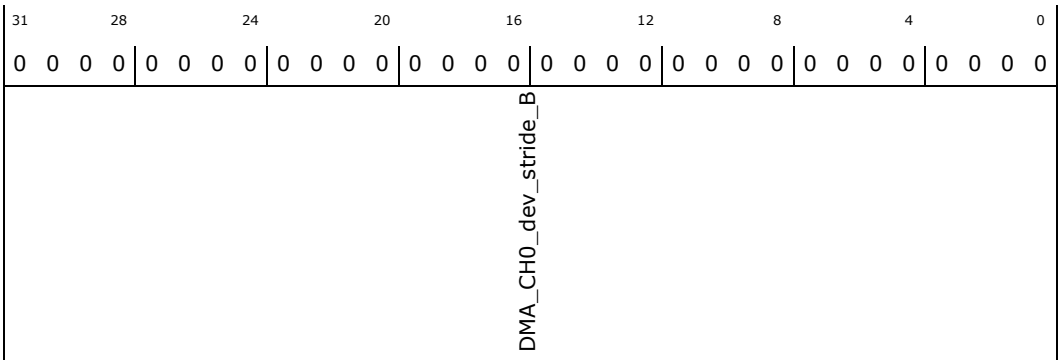
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_dev_stride_B: [ISPMMADR] + 41400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH0_dev_stride_B:** DMA CH 0 PARAM 4: Device B stride

3.7.374 reg_isp_dma_DMA_CH1_dev_stride_B_type (isp_dma_DMA_CH1_dev_stride_B)—Offset 41404h

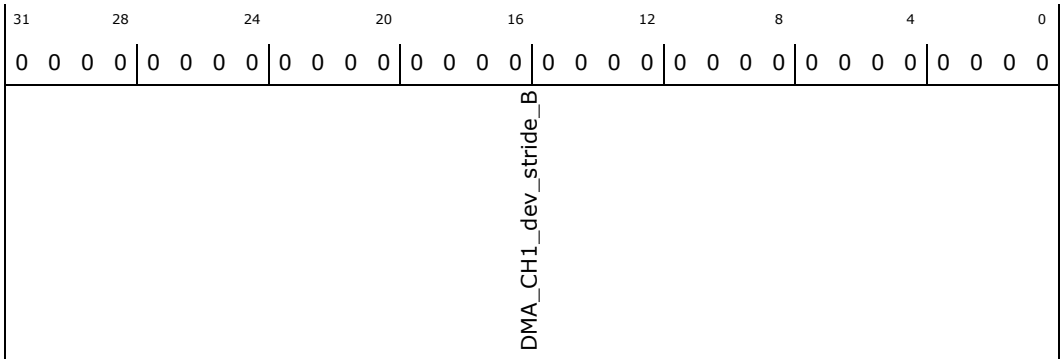
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_dev_stride_B: [ISPMMADR] + 41404h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH1_dev_stride_B:** DMA CH 1 PARAM 4: Device B stride

3.7.375 reg_isp_dma_DMA_CH2_dev_stride_B_type (isp_dma_DMA_CH2_dev_stride_B)—Offset 41408h

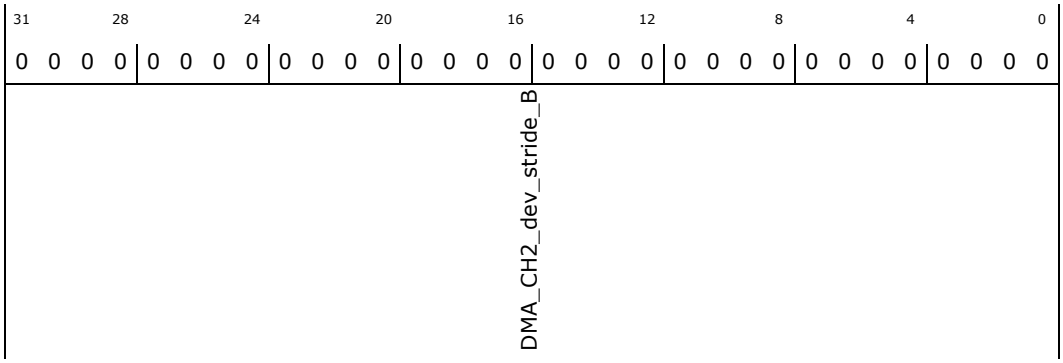
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_dev_stride_B: [ISPMMADR] + 41408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH2_dev_stride_B:** DMA CH 2 PARAM 4: Device B stride

3.7.376 reg_isp_dma_DMA_CH3_dev_stride_B_type (isp_dma_DMA_CH3_dev_stride_B)—Offset 4140Ch

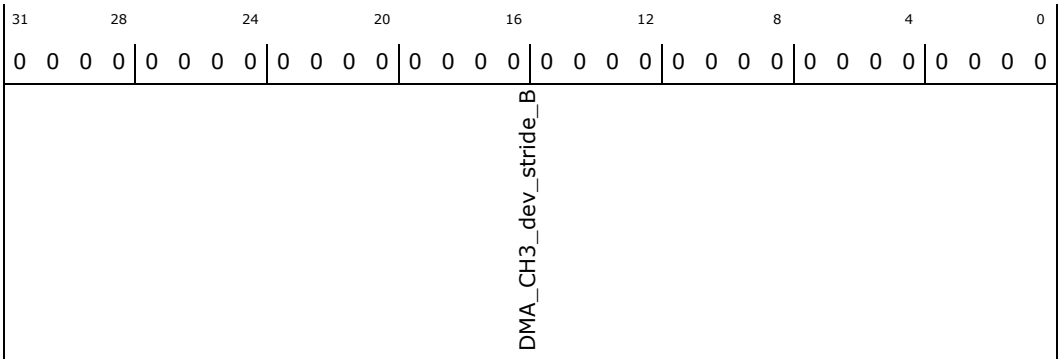
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_dev_stride_B: [ISPMMADR] + 4140Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH3_dev_stride_B:** DMA CH 3 PARAM 4: Device B stride

3.7.377 reg_isp_dma_DMA_CH4_dev_stride_B_type (isp_dma_DMA_CH4_dev_stride_B)—Offset 41410h

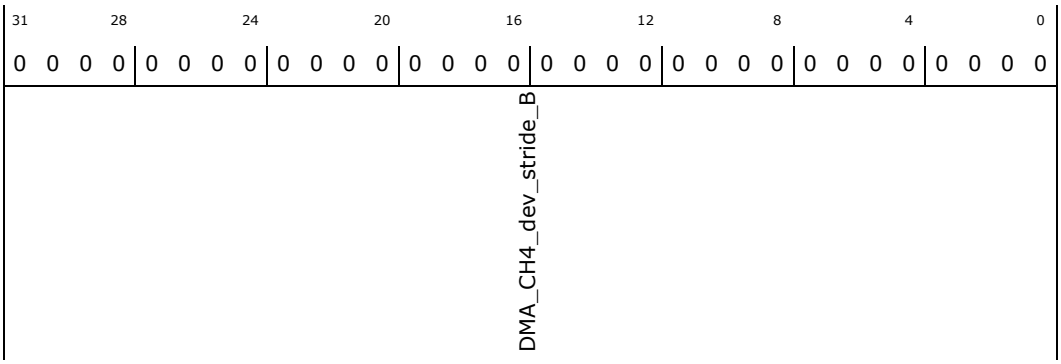
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_dev_stride_B: [ISPMMADR] + 41410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH4_dev_stride_B:** DMA CH 4 PARAM 4: Device B stride

3.7.378 reg_isp_dma_DMA_CH5_dev_stride_B_type (isp_dma_DMA_CH5_dev_stride_B)—Offset 41414h

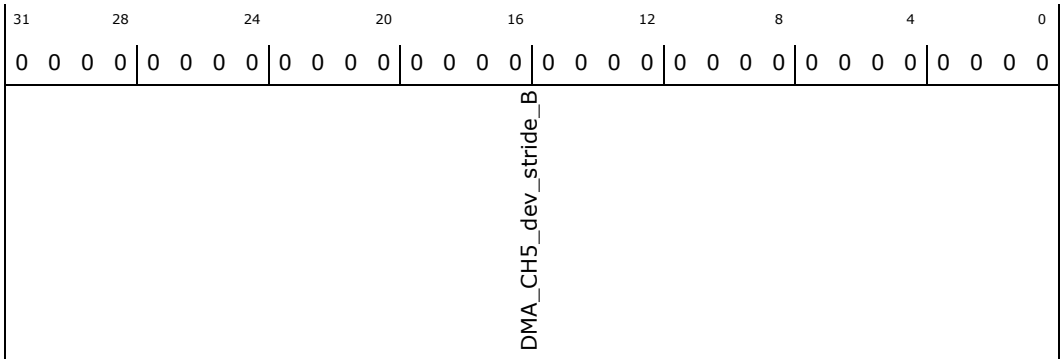
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_dev_stride_B: [ISPMMADR] + 41414h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH5_dev_stride_B:** DMA CH 5 PARAM 4: Device B stride

3.7.379 reg_isp_dma_DMA_CH6_dev_stride_B_type (isp_dma_DMA_CH6_dev_stride_B)—Offset 41418h

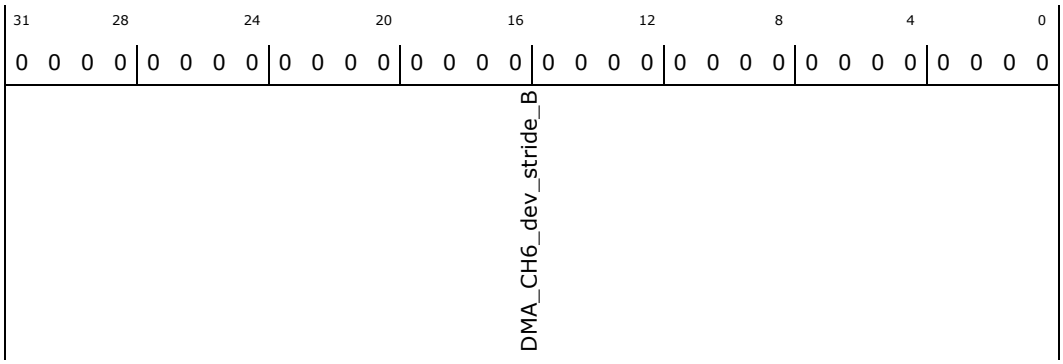
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_dev_stride_B: [ISPMMADR] + 41418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH6_dev_stride_B:** DMA CH 6 PARAM 4: Device B stride

3.7.380 reg_isp_dma_DMA_CH7_dev_stride_B_type (isp_dma_DMA_CH7_dev_stride_B)—Offset 4141Ch

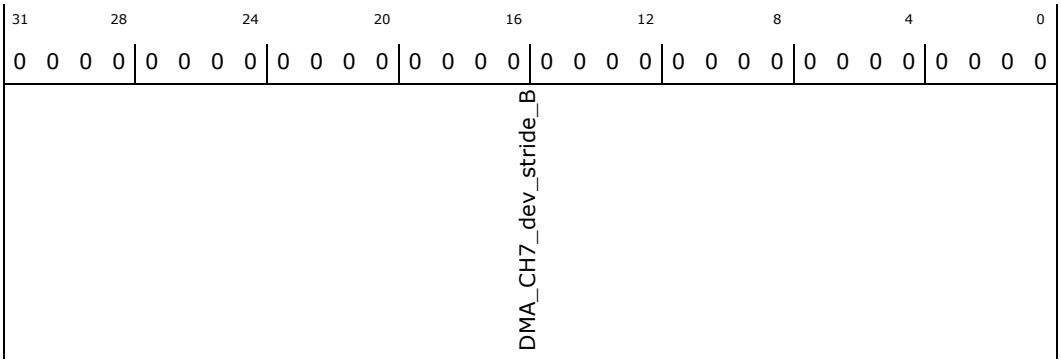
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_dev_stride_B: [ISPMMADR] + 4141Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH7_dev_stride_B:** DMA CH 7 PARAM 4: Device B stride

3.7.381 reg_isp_dma_DMA_CH8_dev_stride_B_type (isp_dma_DMA_CH8_dev_stride_B)—Offset 41420h

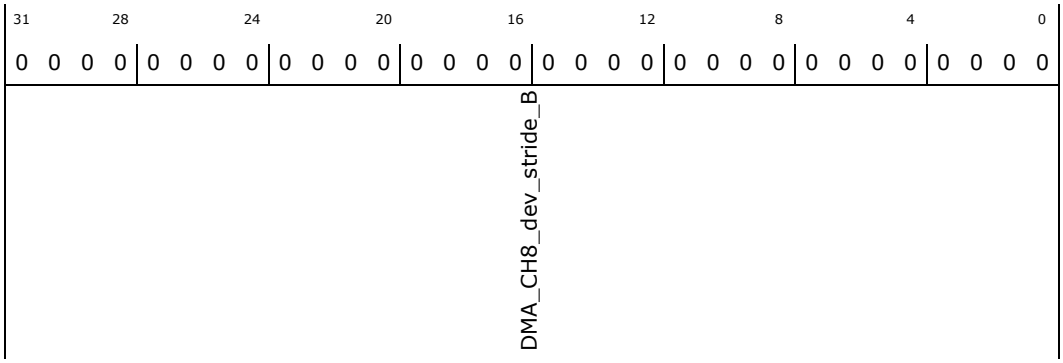
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_dev_stride_B: [ISPMMADR] + 41420h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH8_dev_stride_B:** DMA CH 8 PARAM 4: Device B stride

3.7.382 reg_isp_dma_DMA_CH9_dev_stride_B_type (isp_dma_DMA_CH9_dev_stride_B)—Offset 41424h

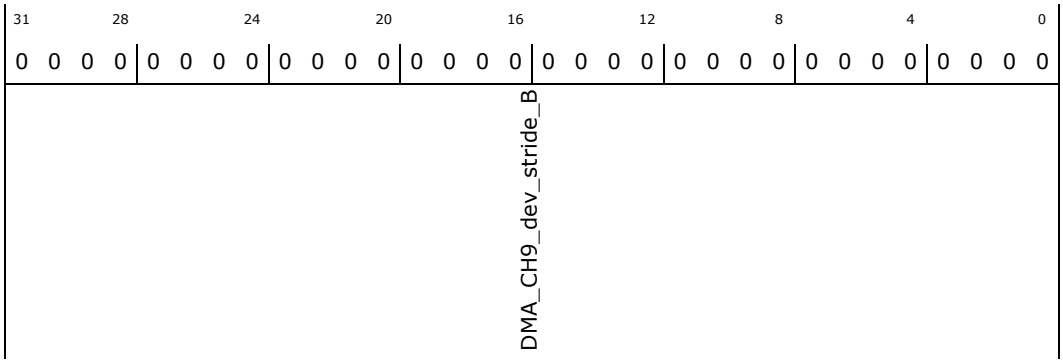
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_dev_stride_B: [ISPMMADR] + 41424h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH9_dev_stride_B:** DMA CH 9 PARAM 4: Device B stride

3.7.383 reg_isp_dma_DMA_CH10_dev_stride_B_type (isp_dma_DMA_CH10_dev_stride_B)—Offset 41428h

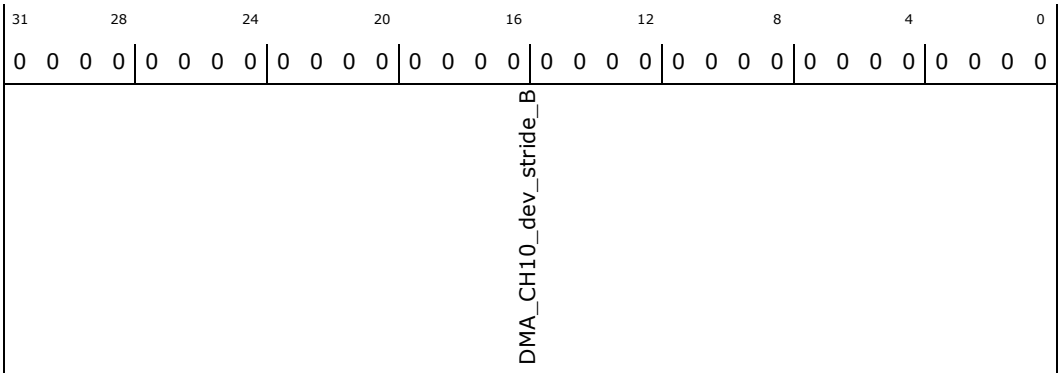
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_dev_stride_B: [ISPMMADR] + 41428h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH10_dev_stride_B:** DMA CH 10 PARAM 4: Device B stride

3.7.384 reg_isp_dma_DMA_CH11_dev_stride_B_type (isp_dma_DMA_CH11_dev_stride_B)—Offset 4142Ch

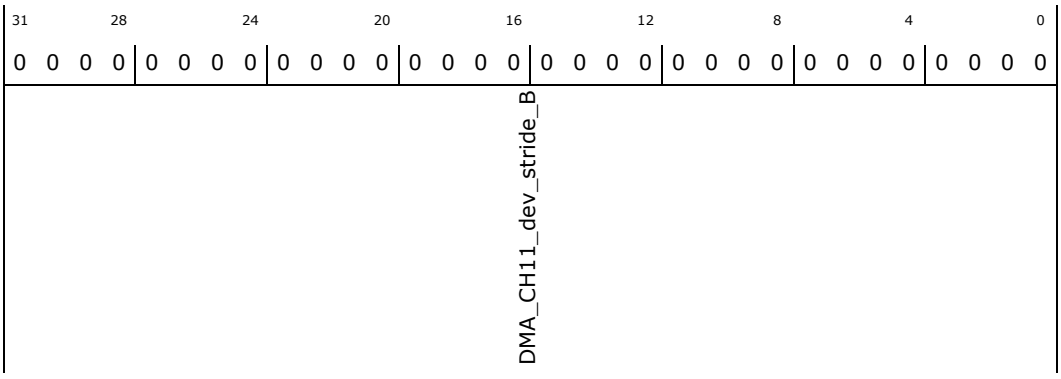
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_dev_stride_B: [ISPMMADR] + 4142Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH11_dev_stride_B:** DMA CH 11 PARAM 4: Device B stride

3.7.385 reg_isp_dma_DMA_CH12_dev_stride_B_type (isp_dma_DMA_CH12_dev_stride_B)—Offset 41430h

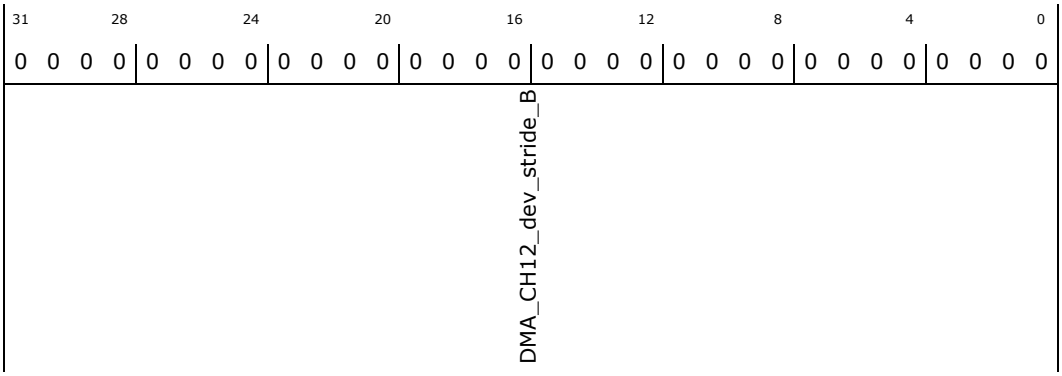
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_dev_stride_B: [ISPMMADR] + 41430h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH12_dev_stride_B:** DMA CH 12 PARAM 4: Device B stride

3.7.386 reg_isp_dma_DMA_CH13_dev_stride_B_type (isp_dma_DMA_CH13_dev_stride_B)—Offset 41434h

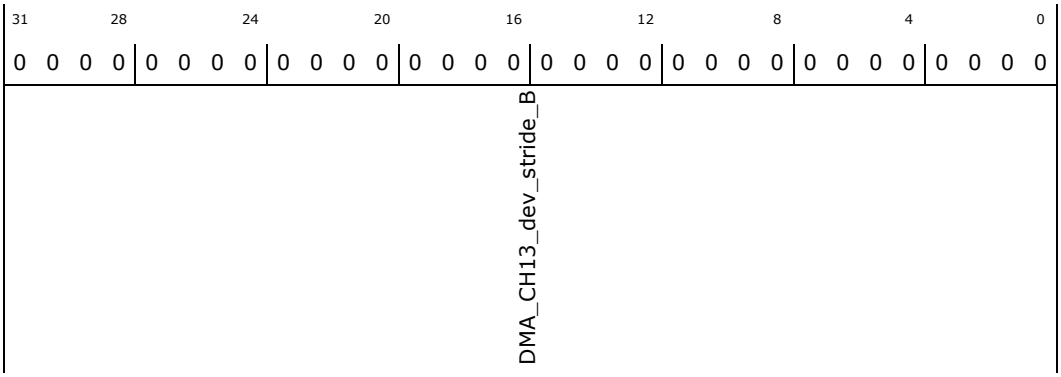
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_dev_stride_B: [ISPMMADR] + 41434h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH13_dev_stride_B:** DMA CH 13 PARAM 4: Device B stride

3.7.387 reg_isp_dma_DMA_CH14_dev_stride_B_type (isp_dma_DMA_CH14_dev_stride_B)—Offset 41438h

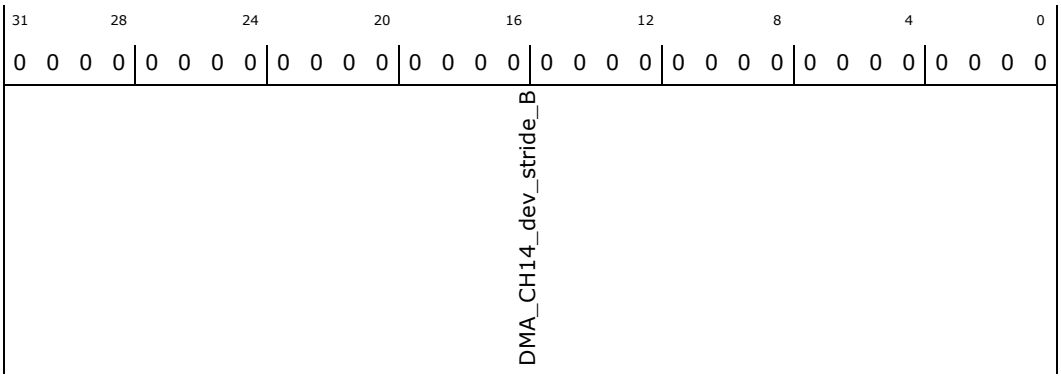
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_dev_stride_B: [ISPMMADR] + 41438h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH14_dev_stride_B:** DMA CH 14 PARAM 4: Device B stride

3.7.388 reg_isp_dma_DMA_CH15_dev_stride_B_type (isp_dma_DMA_CH15_dev_stride_B)—Offset 4143Ch

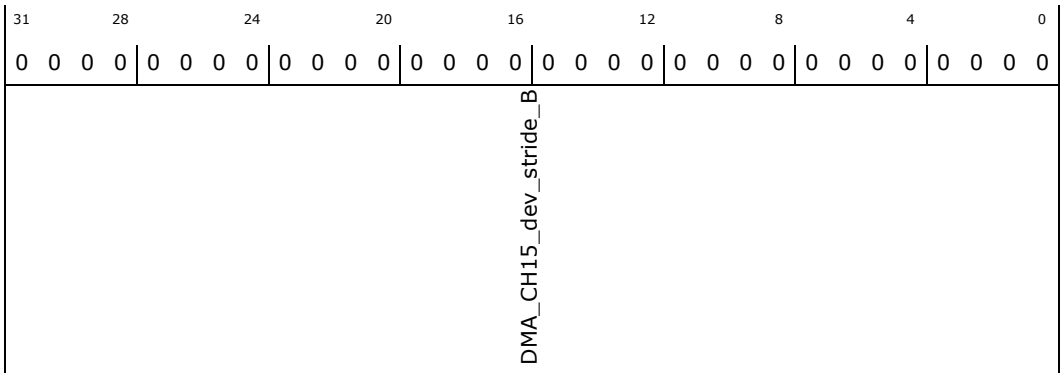
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_dev_stride_B: [ISPMMADR] + 4143Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH15_dev_stride_B:** DMA CH 15 PARAM 4: Device B stride

3.7.389 reg_isp_dma_DMA_CH16_dev_stride_B_type (isp_dma_DMA_CH16_dev_stride_B)—Offset 41440h

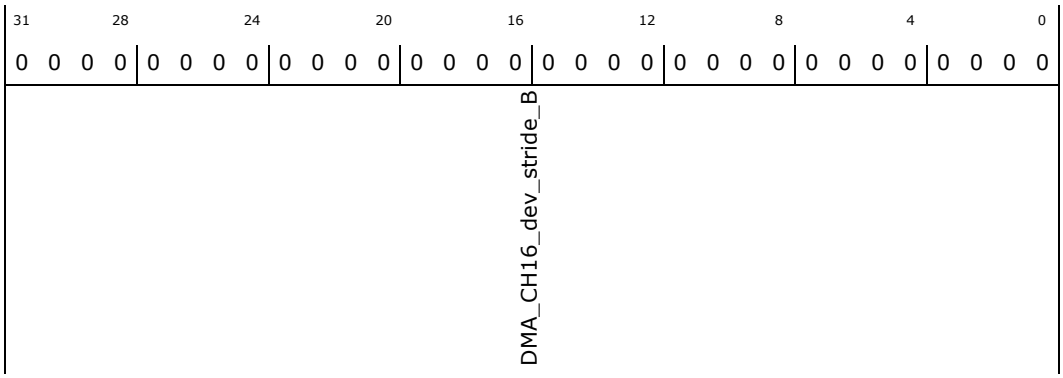
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_dev_stride_B: [ISPMMADR] + 41440h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH16_dev_stride_B:** DMA CH 16 PARAM 4: Device B stride

3.7.390 reg_isp_dma_DMA_CH17_dev_stride_B_type (isp_dma_DMA_CH17_dev_stride_B)—Offset 41444h

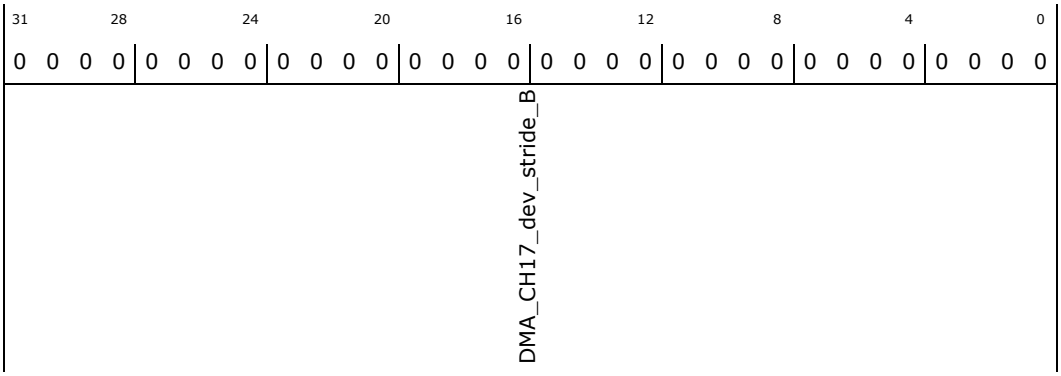
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_dev_stride_B: [ISPMMADR] + 41444h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH17_dev_stride_B:** DMA CH 17 PARAM 4: Device B stride

3.7.391 reg_isp_dma_DMA_CH18_dev_stride_B_type (isp_dma_DMA_CH18_dev_stride_B)—Offset 41448h

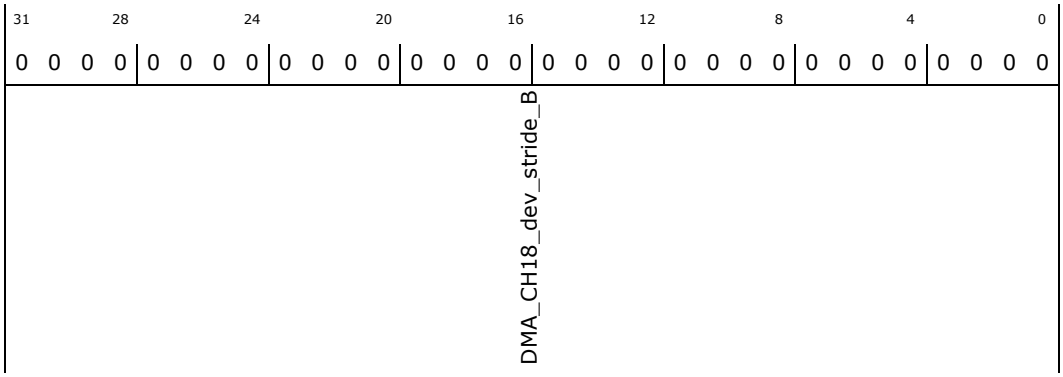
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_dev_stride_B: [ISPMMADR] + 41448h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH18_dev_stride_B:** DMA CH 18 PARAM 4: Device B stride

3.7.392 reg_isp_dma_DMA_CH19_dev_stride_B_type (isp_dma_DMA_CH19_dev_stride_B)—Offset 4144Ch

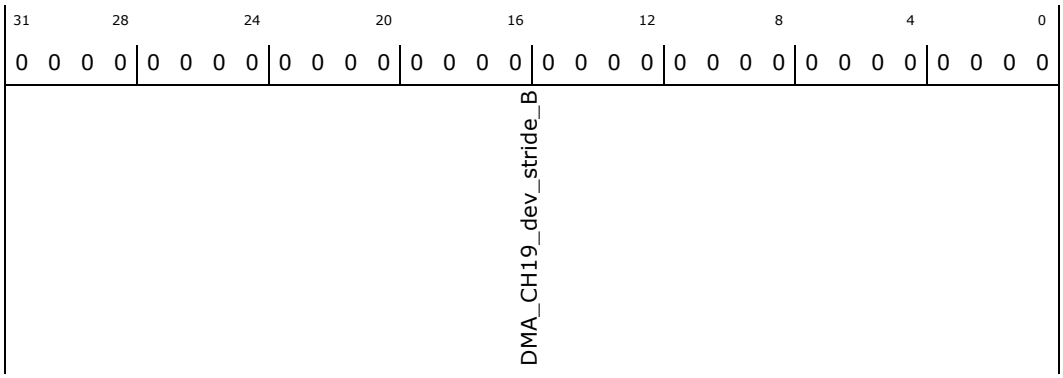
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_dev_stride_B: [ISPMMADR] + 4144Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH19_dev_stride_B:** DMA CH 19 PARAM 4: Device B stride

3.7.393 reg_isp_dma_DMA_CH20_dev_stride_B_type (isp_dma_DMA_CH20_dev_stride_B)—Offset 41450h

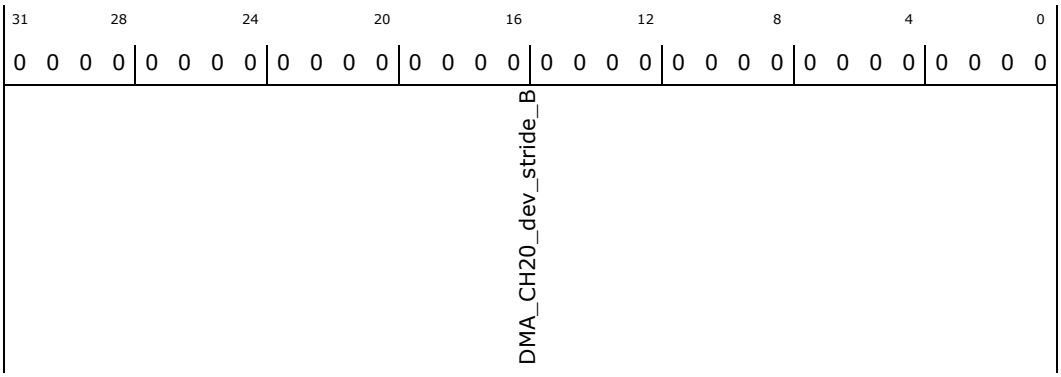
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_dev_stride_B: [ISPMMADR] + 41450h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH20_dev_stride_B:** DMA CH 20 PARAM 4: Device B stride

3.7.394 reg_isp_dma_DMA_CH21_dev_stride_B_type (isp_dma_DMA_CH21_dev_stride_B)—Offset 41454h

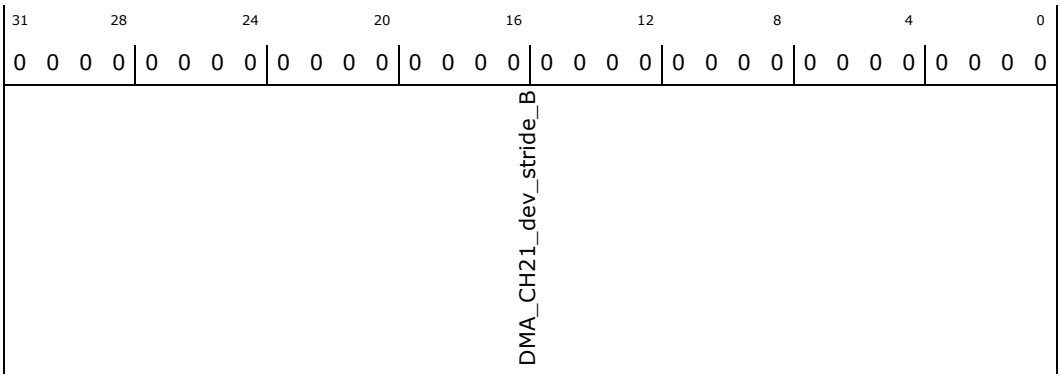
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_dev_stride_B: [ISPMMADR] + 41454h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH21_dev_stride_B:** DMA CH 21 PARAM 4: Device B stride

3.7.395 reg_isp_dma_DMA_CH22_dev_stride_B_type (isp_dma_DMA_CH22_dev_stride_B)—Offset 41458h

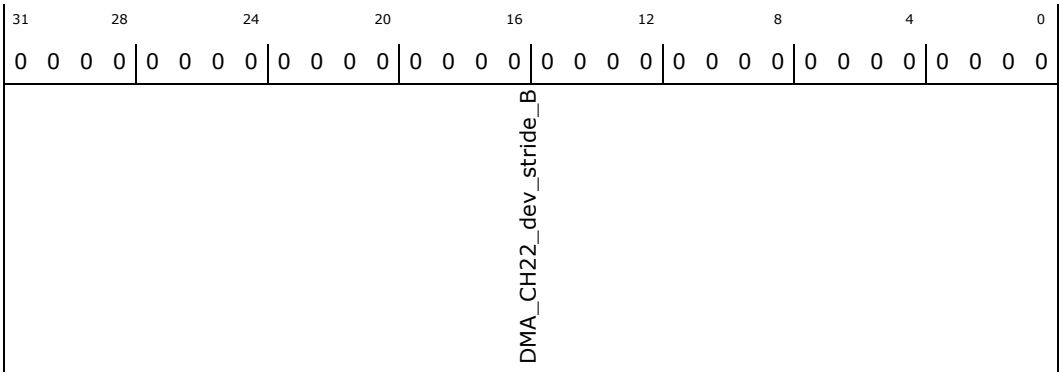
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_dev_stride_B: [ISPMMADR] + 41458h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH22_dev_stride_B:** DMA CH 22 PARAM 4: Device B stride

3.7.396 reg_isp_dma_DMA_CH23_dev_stride_B_type (isp_dma_DMA_CH23_dev_stride_B)—Offset 4145Ch

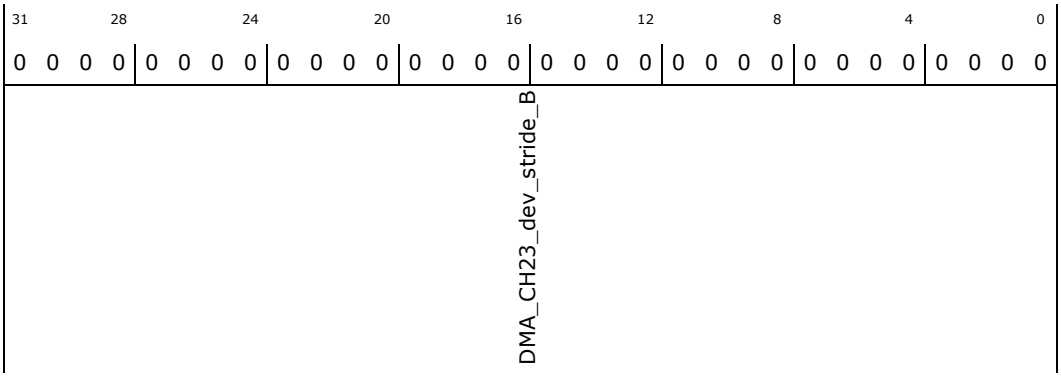
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_dev_stride_B: [ISPMMADR] + 4145Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH23_dev_stride_B:** DMA CH 23 PARAM 4: Device B stride

3.7.397 reg_isp_dma_DMA_CH24_dev_stride_B_type (isp_dma_DMA_CH24_dev_stride_B)—Offset 41460h

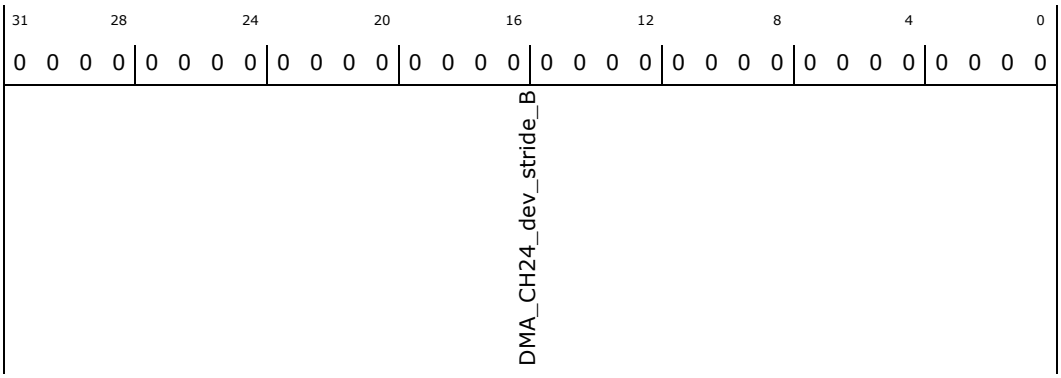
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_dev_stride_B: [ISPMMADR] + 41460h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH24_dev_stride_B:** DMA CH 24 PARAM 4: Device B stride

3.7.398 reg_isp_dma_DMA_CH26_dev_stride_B_type (isp_dma_DMA_CH26_dev_stride_B)—Offset 41468h

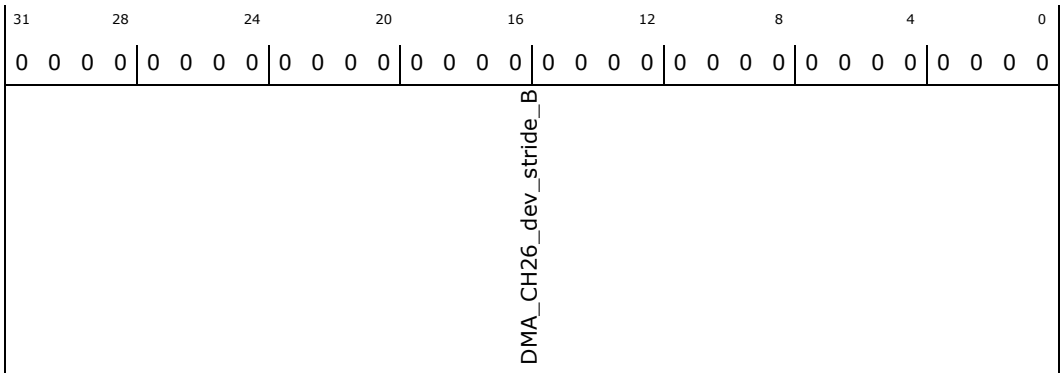
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_dev_stride_B: [ISPMMADR] + 41468h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH26_dev_stride_B:** DMA CH 26 PARAM 4: Device B stride

3.7.399 reg_isp_dma_DMA_CH27_dev_stride_B_type (isp_dma_DMA_CH27_dev_stride_B)—Offset 4146Ch

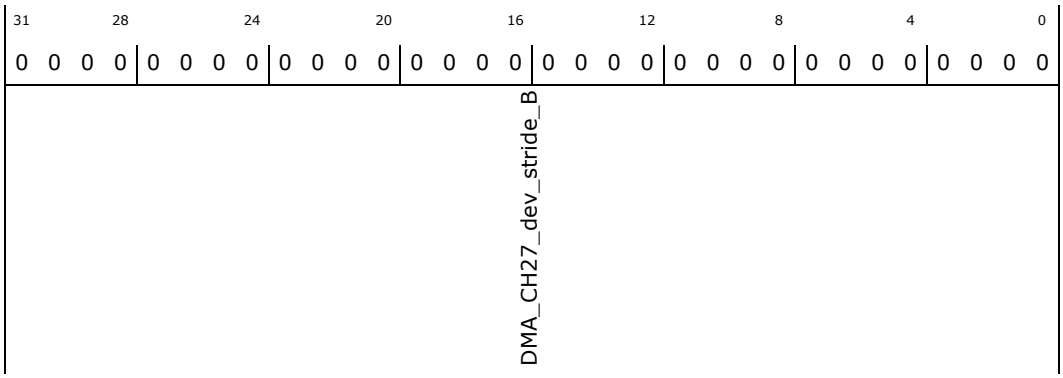
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_dev_stride_B: [ISPMMADR] + 4146Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH27_dev_stride_B:** DMA CH 27 PARAM 4: Device B stride

3.7.400 reg_isp_dma_DMA_CH28_dev_stride_B_type (isp_dma_DMA_CH28_dev_stride_B)—Offset 41470h

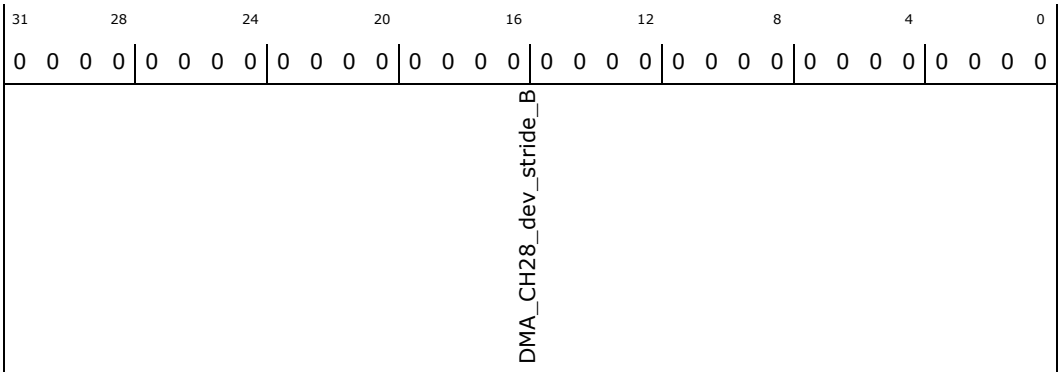
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_dev_stride_B: [ISPMMADR] + 41470h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH28_dev_stride_B:** DMA CH 28 PARAM 4: Device B stride

3.7.401 reg_isp_dma_DMA_CH29_dev_stride_B_type (isp_dma_DMA_CH29_dev_stride_B)—Offset 41474h

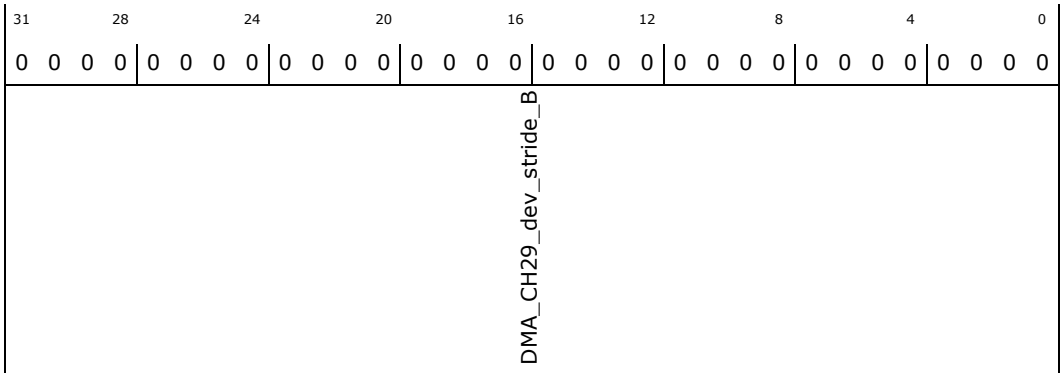
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_dev_stride_B: [ISPMMADR] + 41474h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH29_dev_stride_B:** DMA CH 29 PARAM 4: Device B stride

3.7.402 reg_isp_dma_DMA_CH30_dev_stride_B_type (isp_dma_DMA_CH30_dev_stride_B)—Offset 41478h

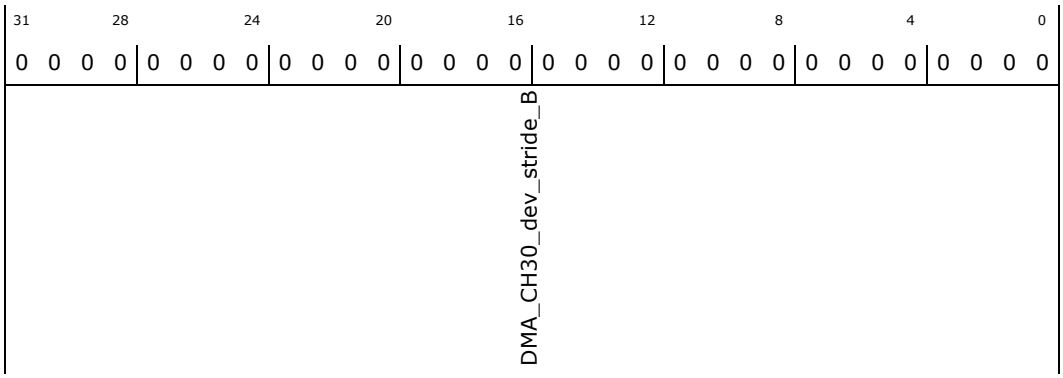
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH30_dev_stride_B: [ISPMMADR] + 41478h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH30_dev_stride_B:** DMA CH 30 PARAM 4: Device B stride

3.7.403 reg_isp_dma_DMA_CH31_dev_stride_B_type (isp_dma_DMA_CH31_dev_stride_B)—Offset 4147Ch

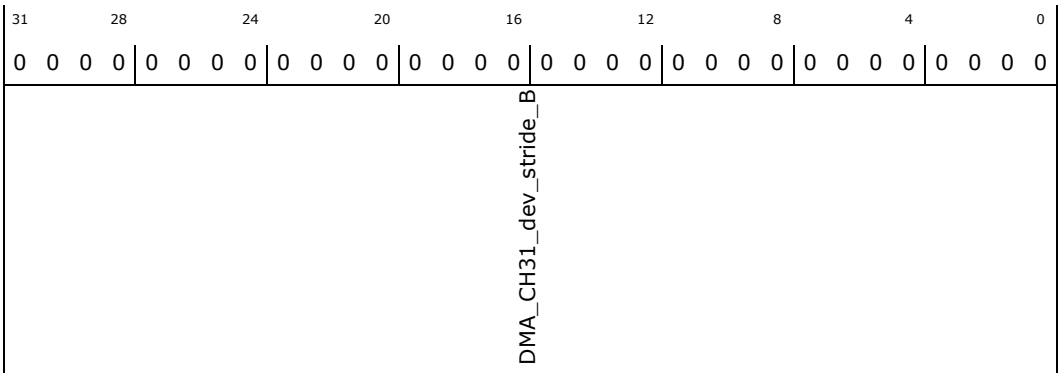
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_dev_stride_B: [ISPMMADR] + 4147Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH31_dev_stride_B:** DMA CH 30 PARAM 4: Device B stride

3.7.404 reg_isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B)—Offset 41500h

DMA CH 0 PARAM 5: Device B Packing LSE cropping/Elements

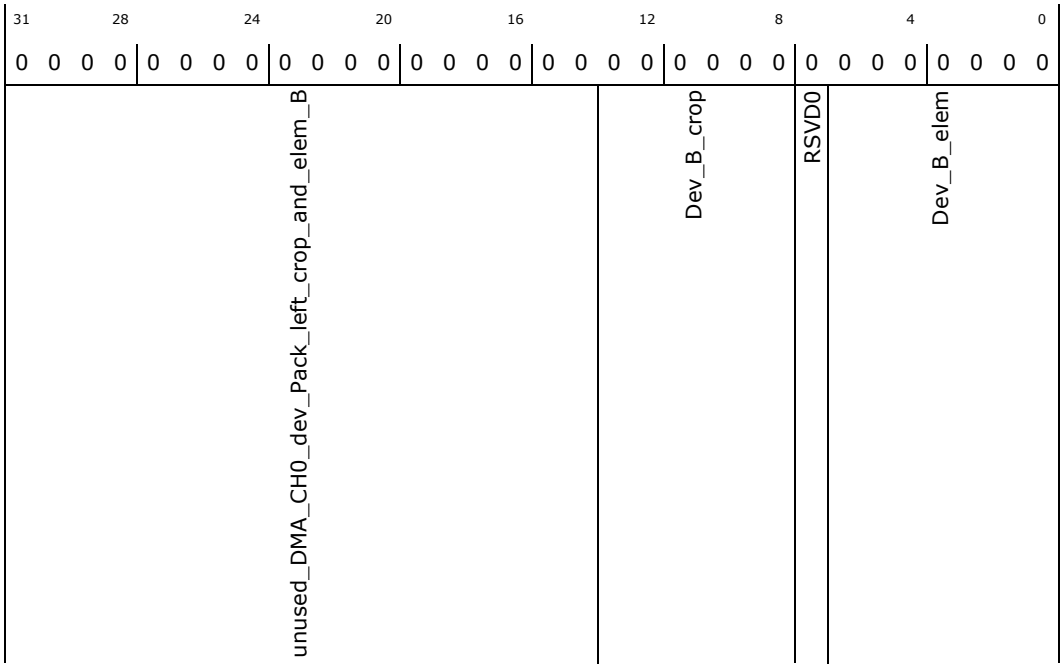
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH0_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.405 reg_isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_B)—Offset 41504h

DMA CH 1 PARAM 5: Device B Packing LSE cropping/Elements

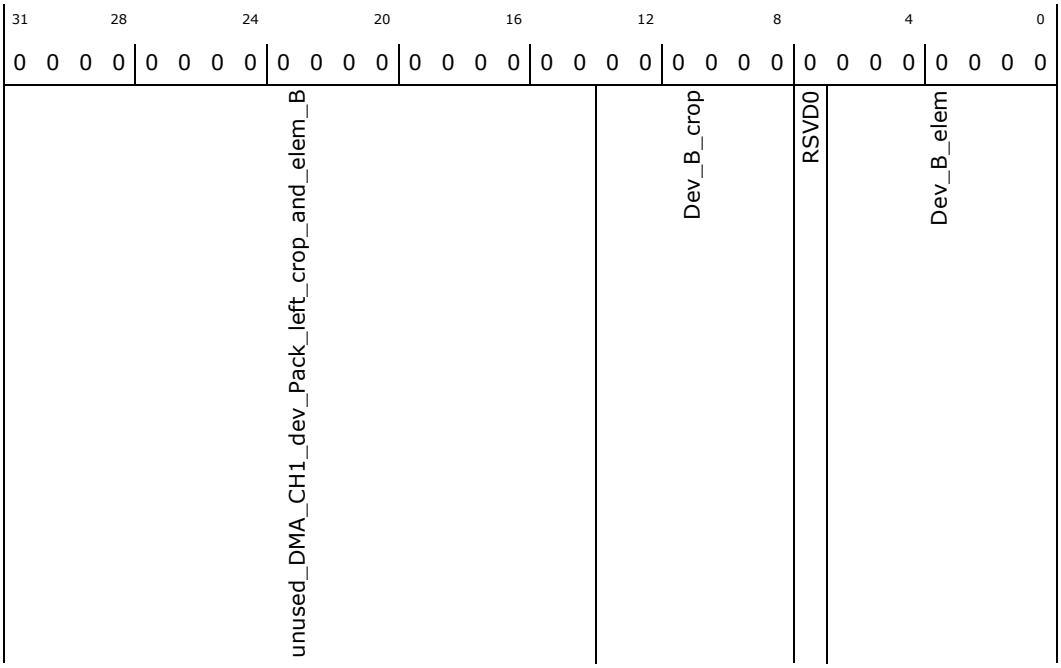
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41504h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH1_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.406 reg_isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_B)—Offset 41508h

DMA CH 2 PARAM 5: Device B Packing LSE cropping/Elements

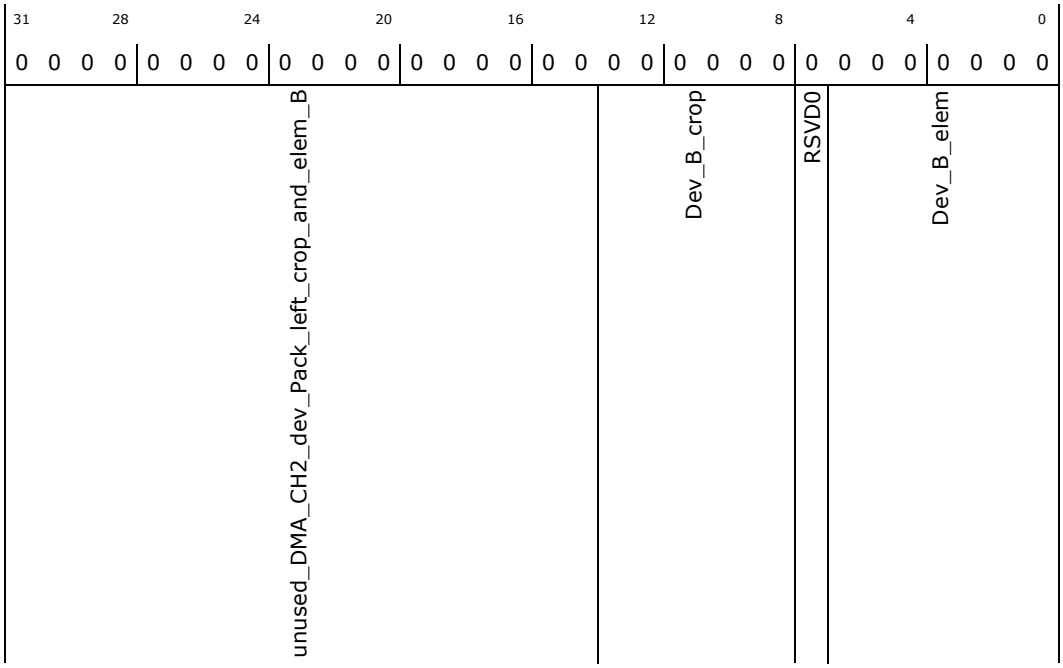
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41508h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH2_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.407 reg_isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_B)—Offset 4150Ch

DMA CH 3 PARAM 5: Device B Packing LSE cropping/Elements

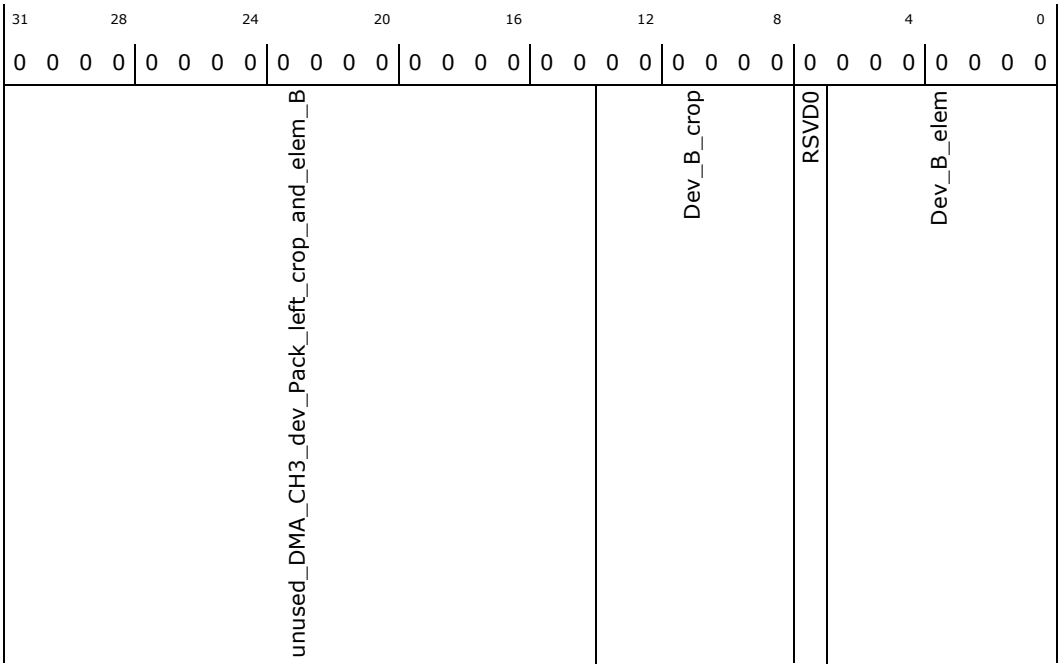
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4150Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH3_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.408 reg_isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_B)—Offset 41510h

DMA CH 4 PARAM 5: Device B Packing LSE cropping/Elements

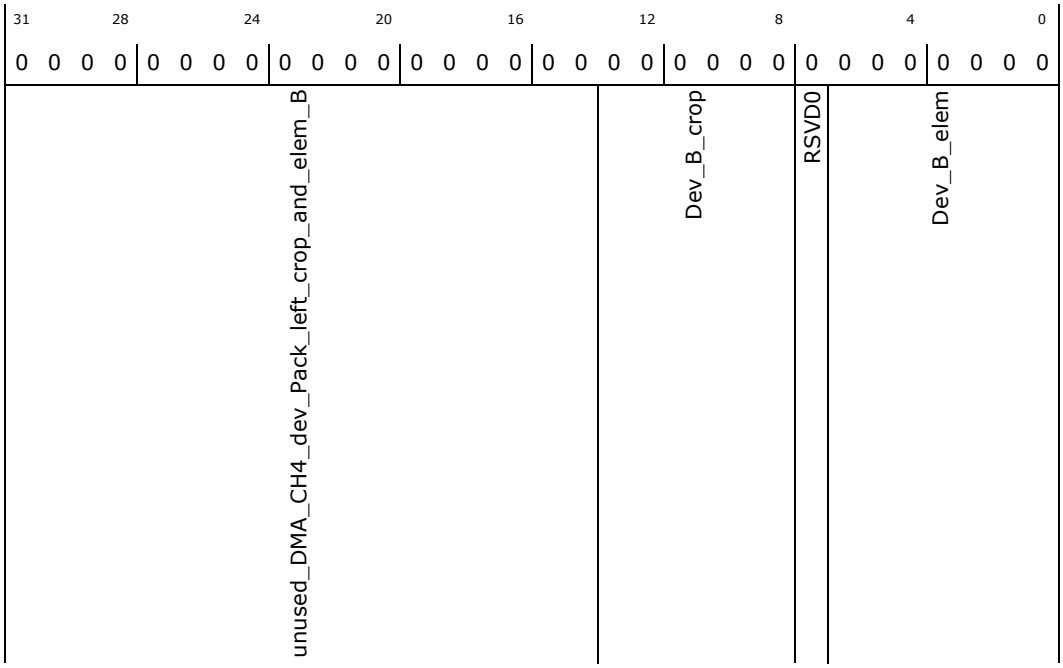
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH4_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.409 reg_isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_B)—Offset 41514h

DMA CH 5 PARAM 5: Device B Packing LSE cropping/Elements

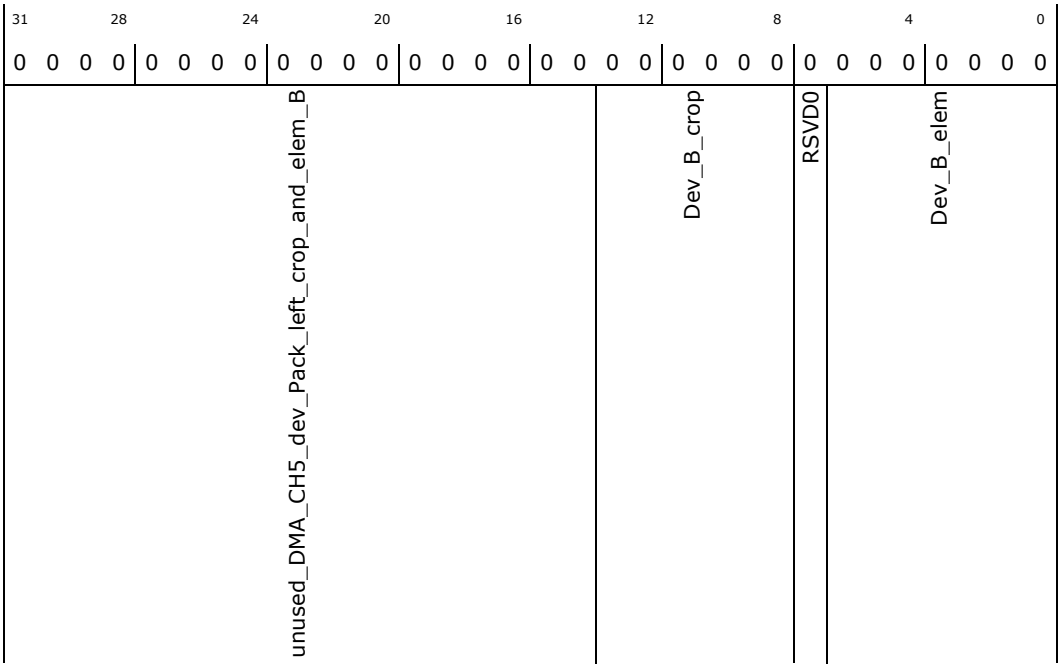
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41514h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH5_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.410 reg_isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_B)—Offset 41518h

DMA CH 6 PARAM 5: Device B Packing LSE cropping/Elements

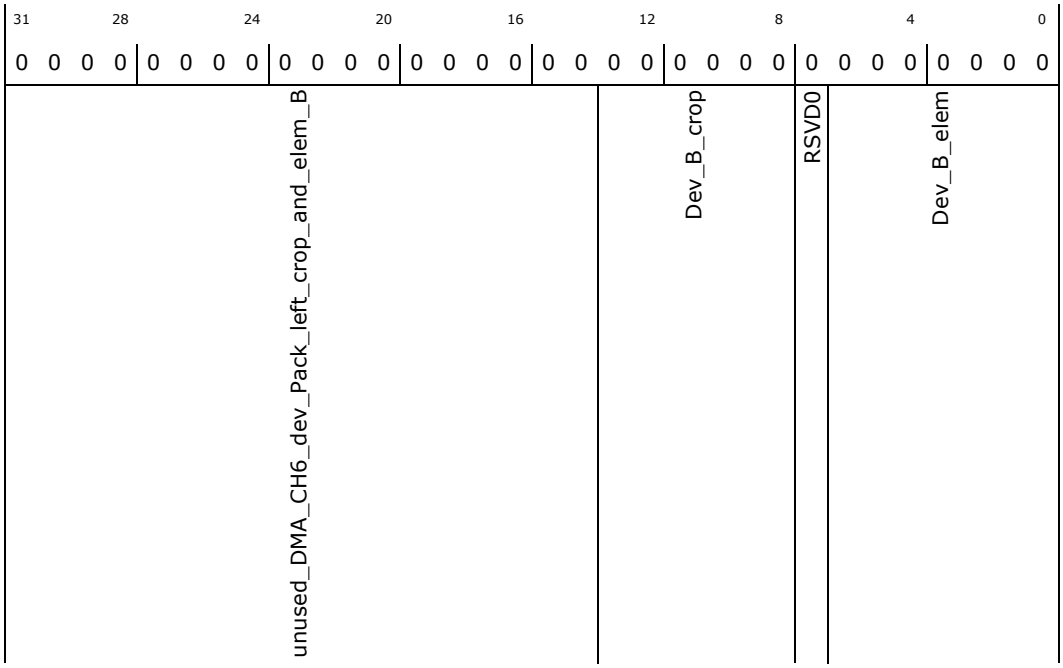
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41518h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH6_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.411 reg_isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_B)—Offset 4151Ch

DMA CH 7 PARAM 5: Device B Packing LSE cropping/Elements

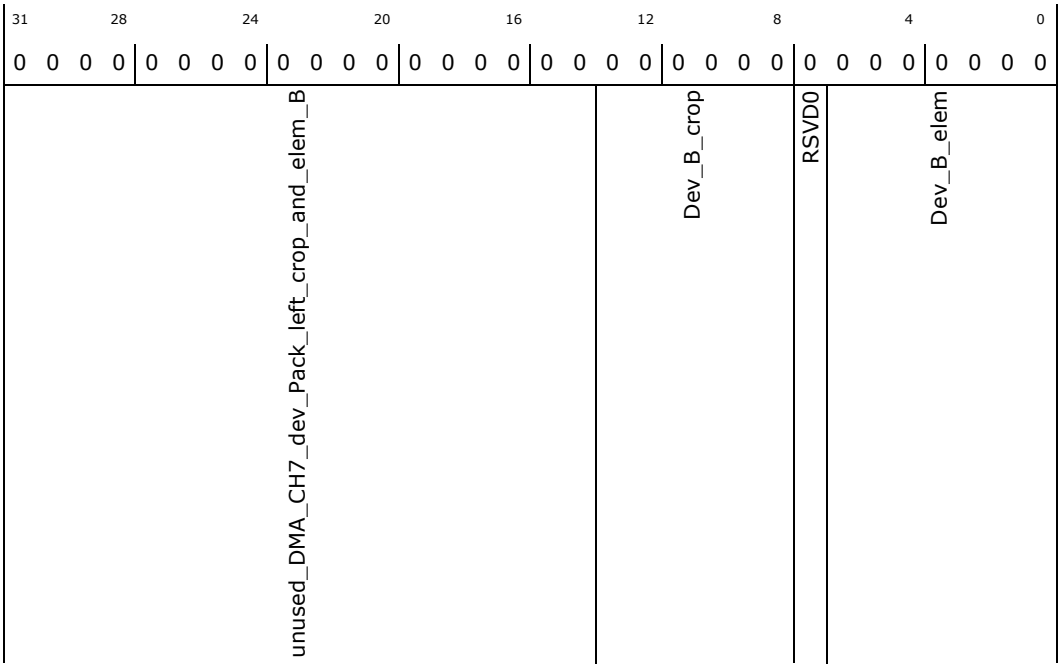
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4151Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH7_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.412 reg_isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_B)—Offset 41520h

DMA CH 8 PARAM 5: Device B Packing LSE cropping/Elements

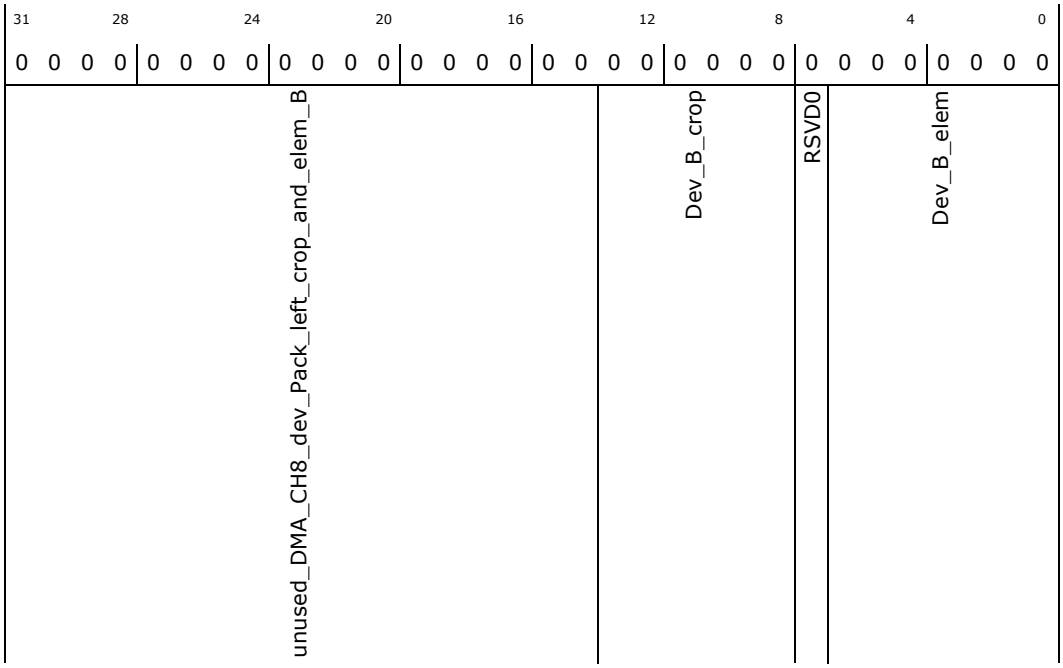
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41520h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH8_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.413 reg_isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_B)—Offset 41524h

DMA CH 9 PARAM 5: Device B Packing LSE cropping/Elements

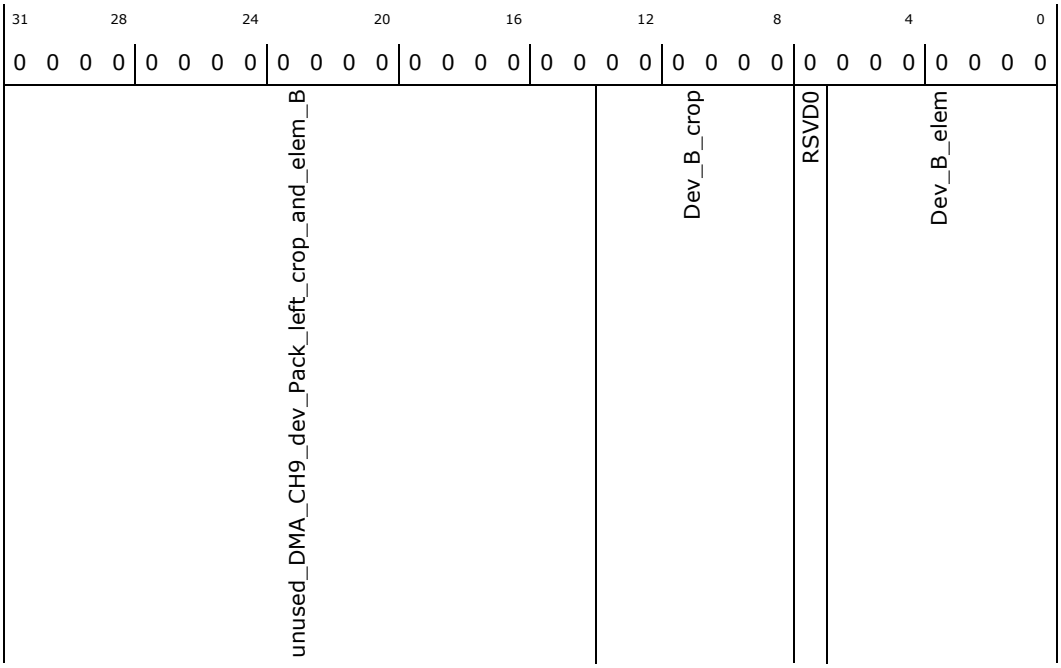
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41524h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH9_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.414 reg_isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_B) —Offset 41528h

DMA CH 10 PARAM 5: Device B Packing LSE cropping/Elements

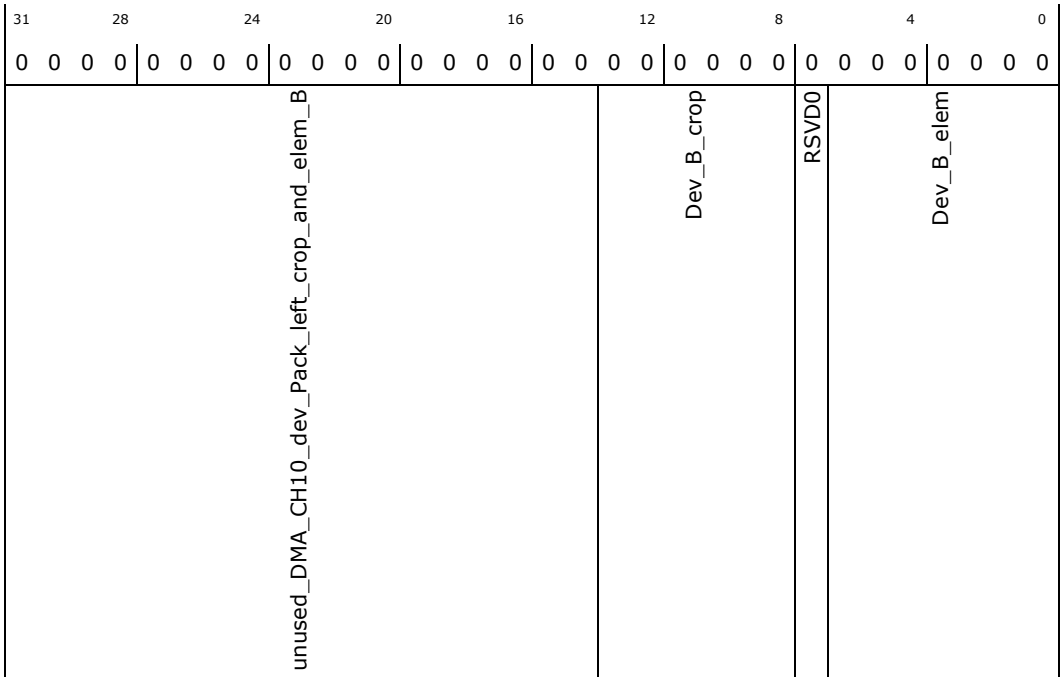
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41528h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH10_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.415 reg_isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_B)—Offset 4152Ch

DMA CH 11 PARAM 5: Device B Packing LSE cropping/Elements

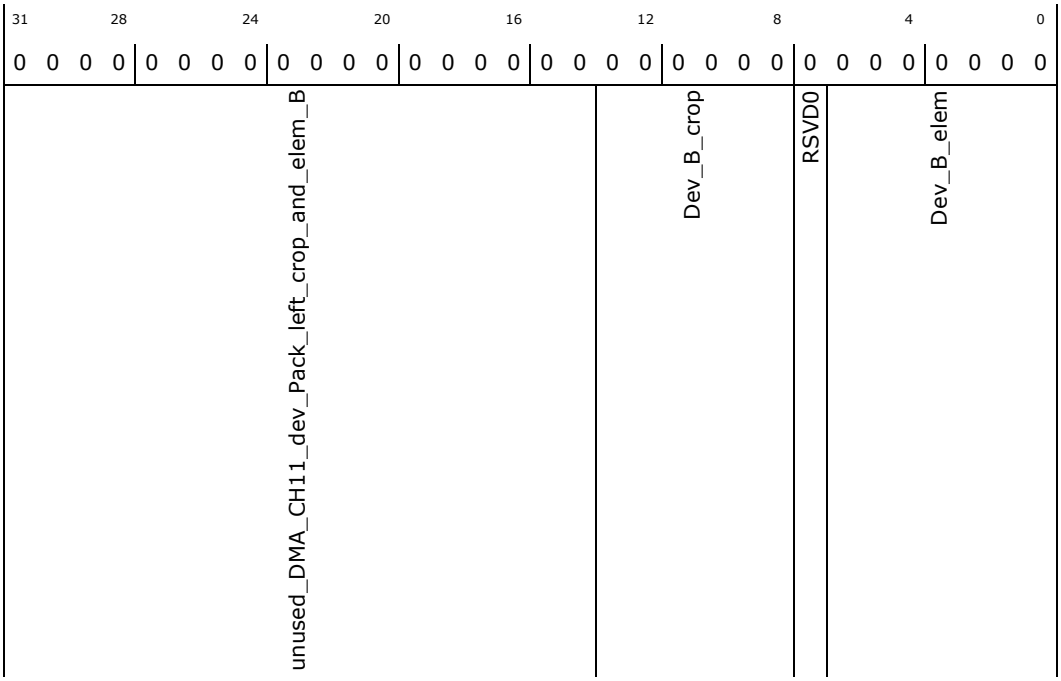
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4152Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH11_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.416 reg_isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_B)—Offset 41530h

DMA CH 12 PARAM 5: Device B Packing LSE cropping/Elements

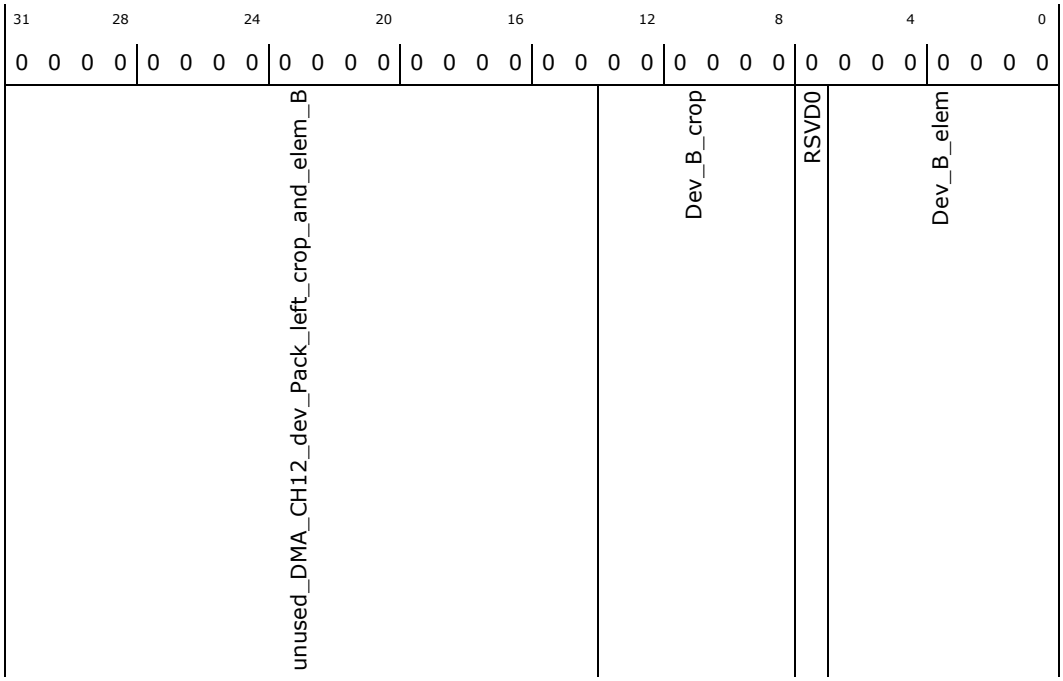
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41530h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH12_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.417 reg_isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_B)—Offset 41534h

DMA CH 13 PARAM 5: Device B Packing LSE cropping/Elements

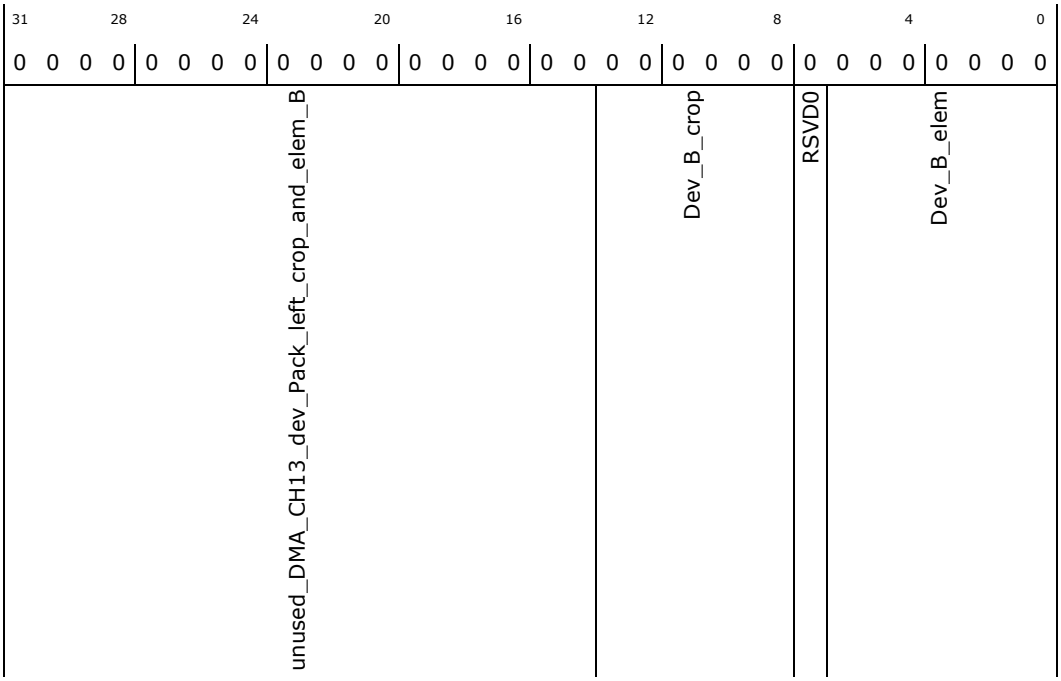
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41534h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH13_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.418 reg_isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_B)—Offset 41538h

DMA CH 14 PARAM 5: Device B Packing LSE cropping/Elements

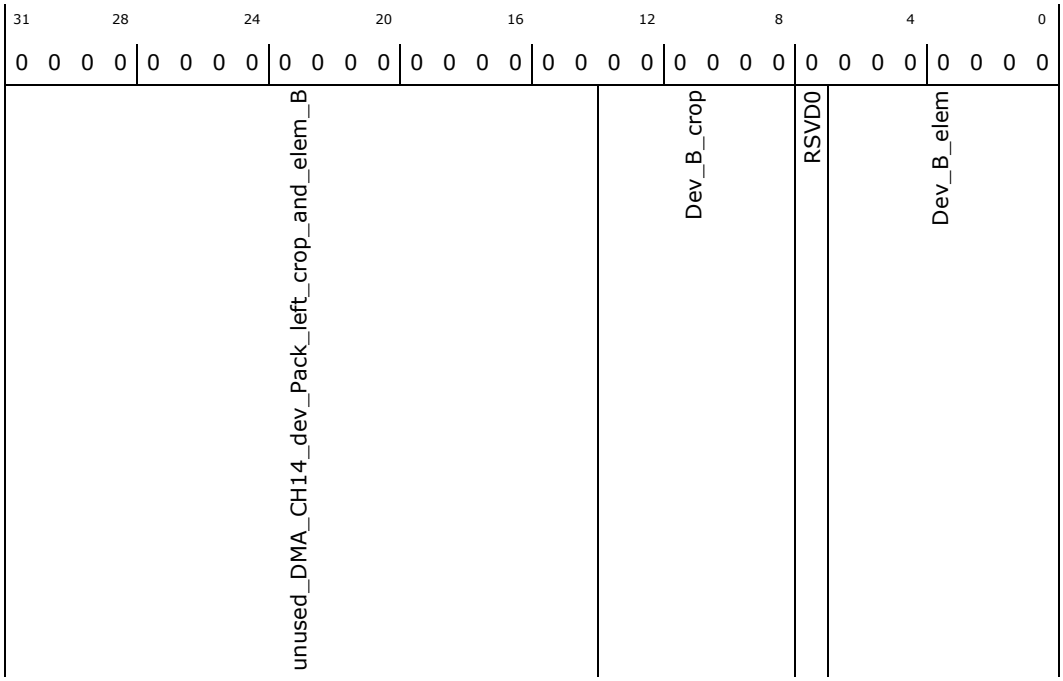
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41538h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH14_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.419 reg_isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_B)—Offset 4153Ch

DMA CH 15 PARAM 5: Device B Packing LSE cropping/Elements

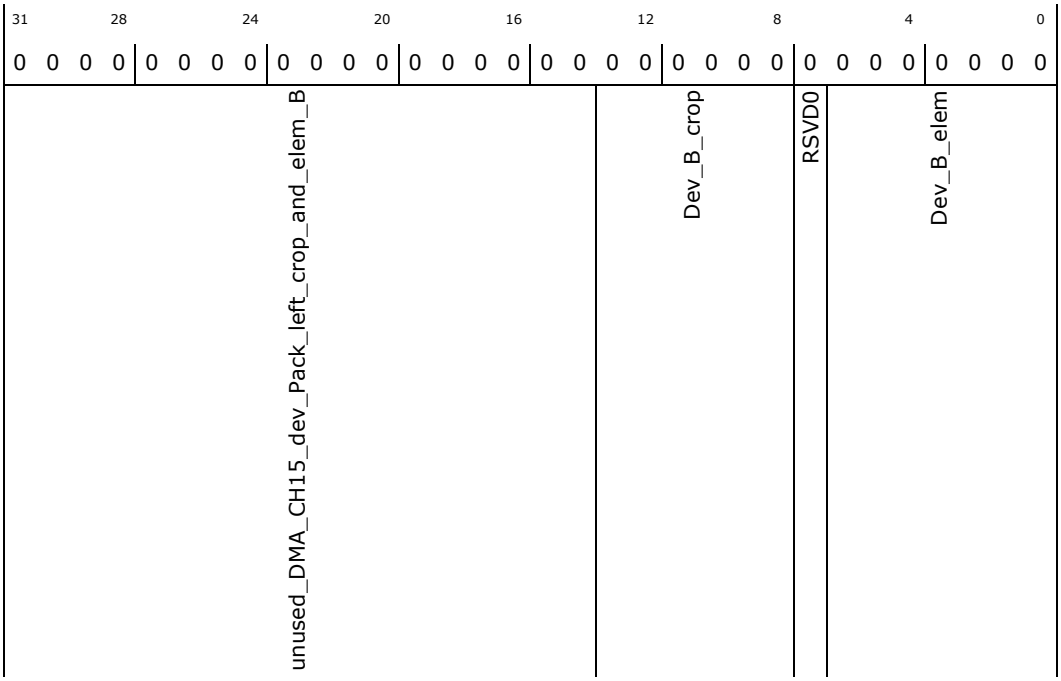
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4153Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH15_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.420 reg_isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_B)—Offset 41540h

DMA CH 16 PARAM 5: Device B Packing LSE cropping/Elements

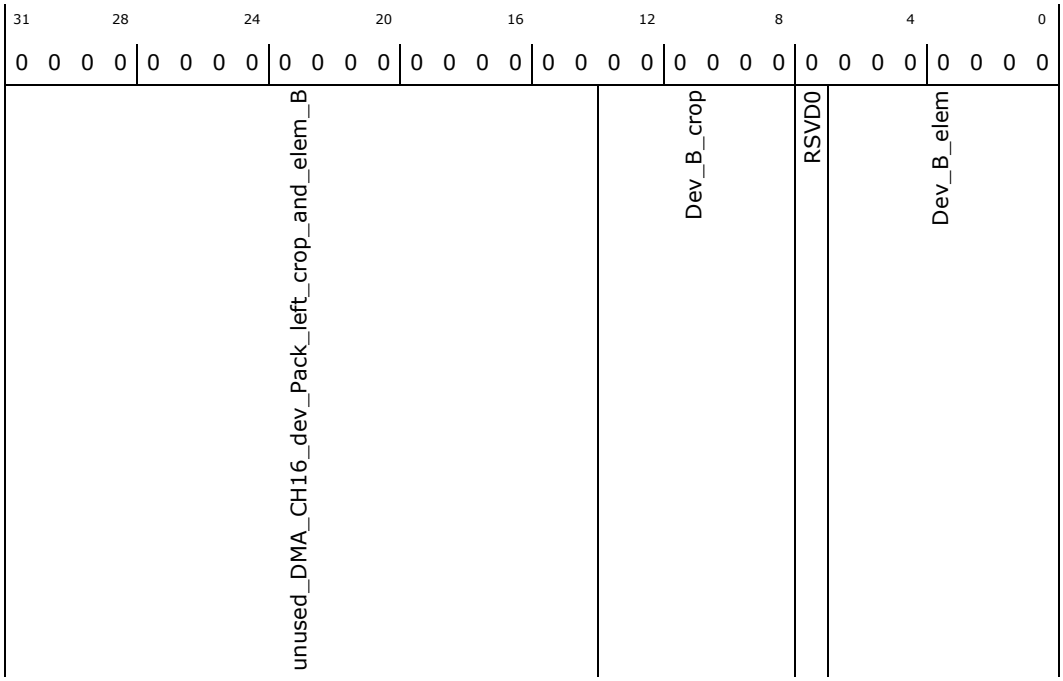
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41540h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH16_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.421 reg_isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_B)—Offset 41544h

DMA CH 17 PARAM 5: Device B Packing LSE cropping/Elements

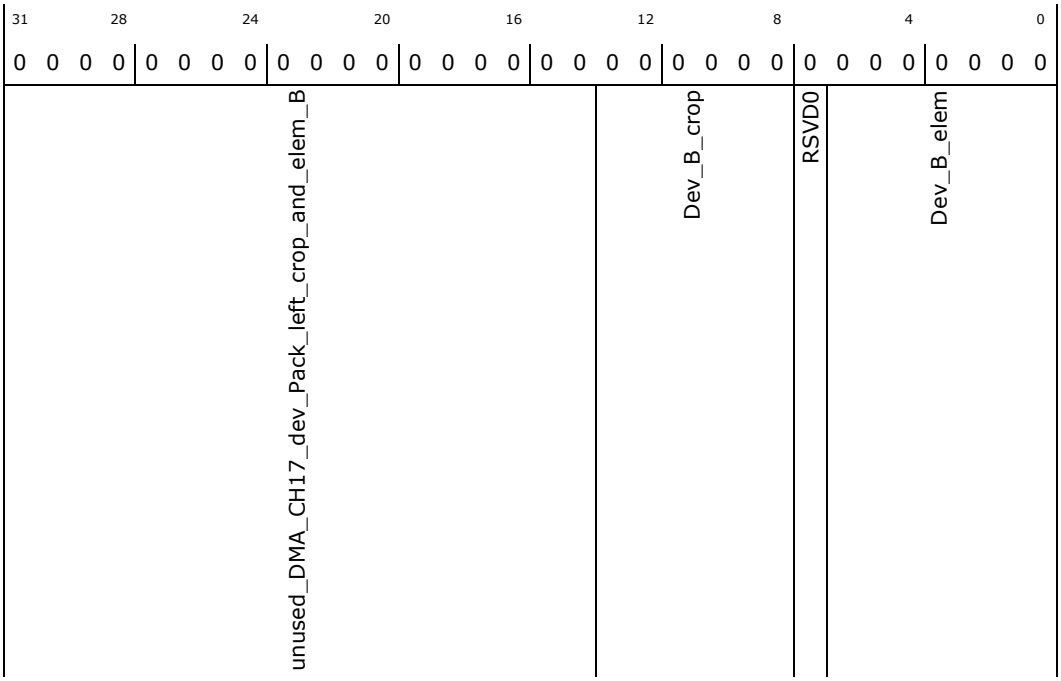
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41544h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH17_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.422 reg_isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_B)—Offset 41548h

DMA CH 18 PARAM 5: Device B Packing LSE cropping/Elements

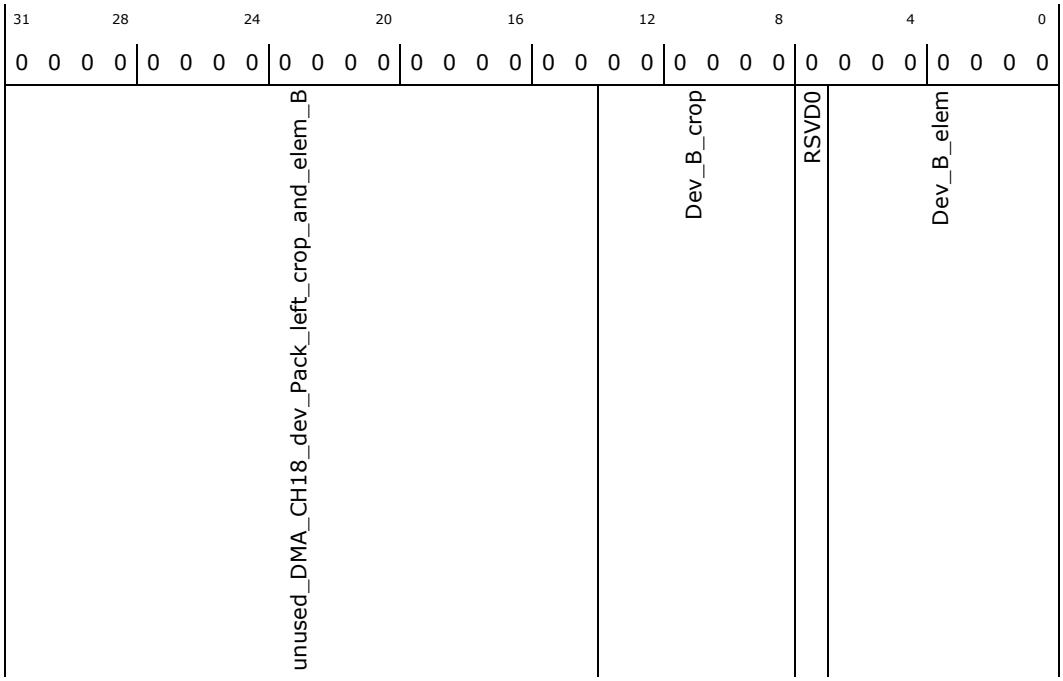
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41548h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH18_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.423 reg_isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_B)—Offset 4154Ch

DMA CH 19 PARAM 5: Device B Packing LSE cropping/Elements

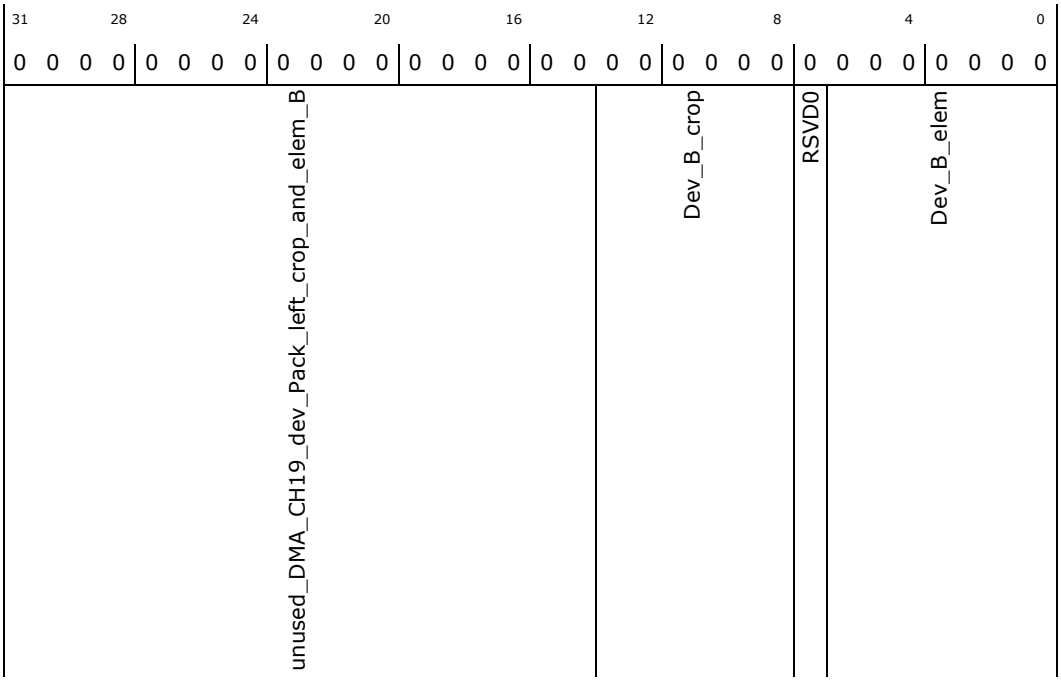
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4154Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH19_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.424 reg_isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_B)—Offset 41550h

DMA CH 20 PARAM 5: Device B Packing LSE cropping/Elements

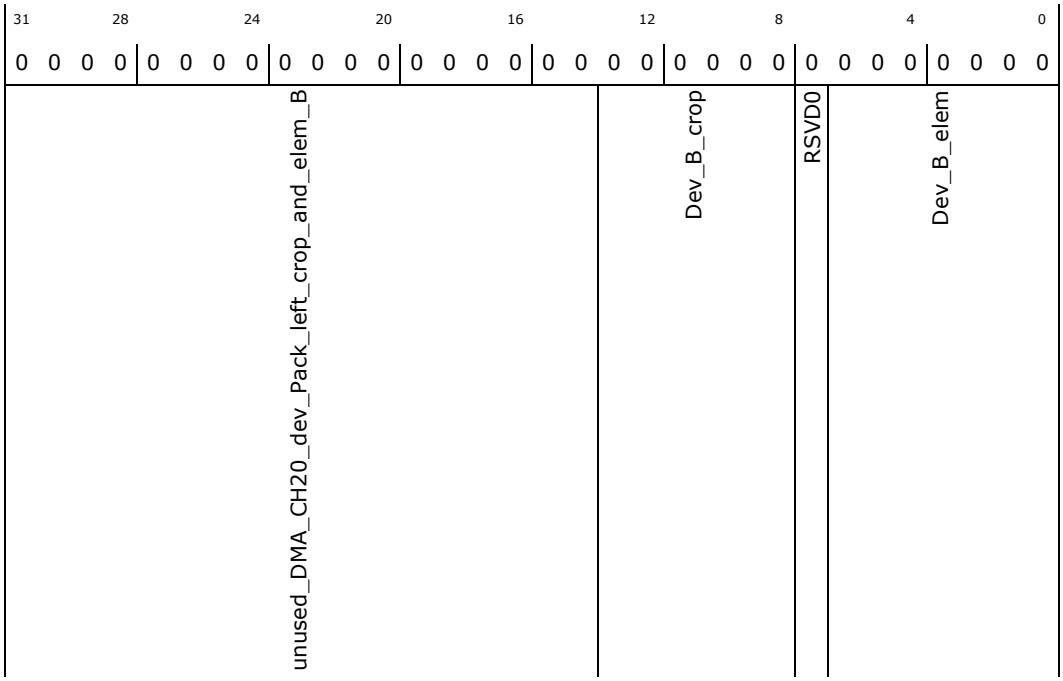
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41550h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH20_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.425 reg_isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_B)—Offset 41554h

DMA CH 21 PARAM 5: Device B Packing LSE cropping/Elements

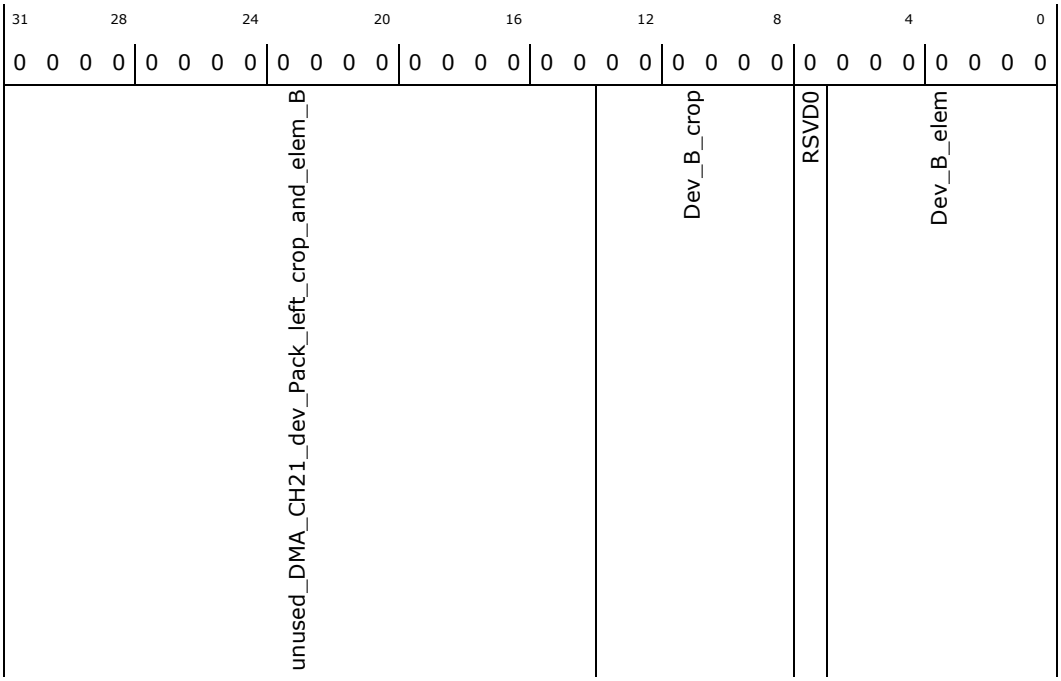
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41554h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH21_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.426 reg_isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_B)—Offset 41558h

DMA CH 22 PARAM 5: Device B Packing LSE cropping/Elements

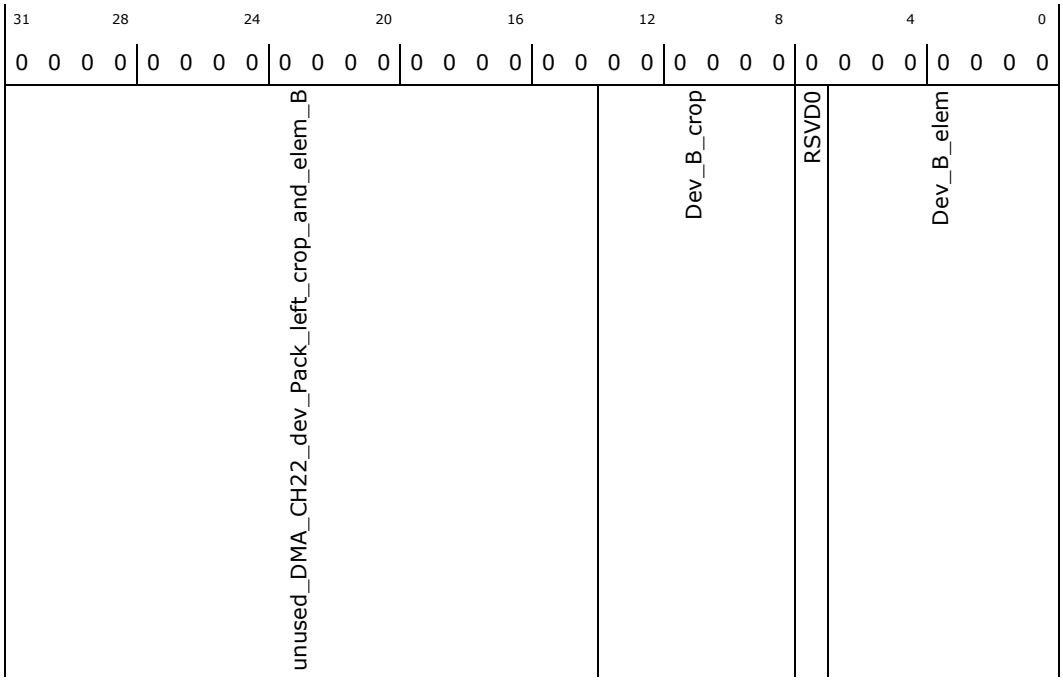
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41558h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH22_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.427 reg_isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_B)—Offset 4155Ch

DMA CH 23 PARAM 5: Device B Packing LSE cropping/Elements

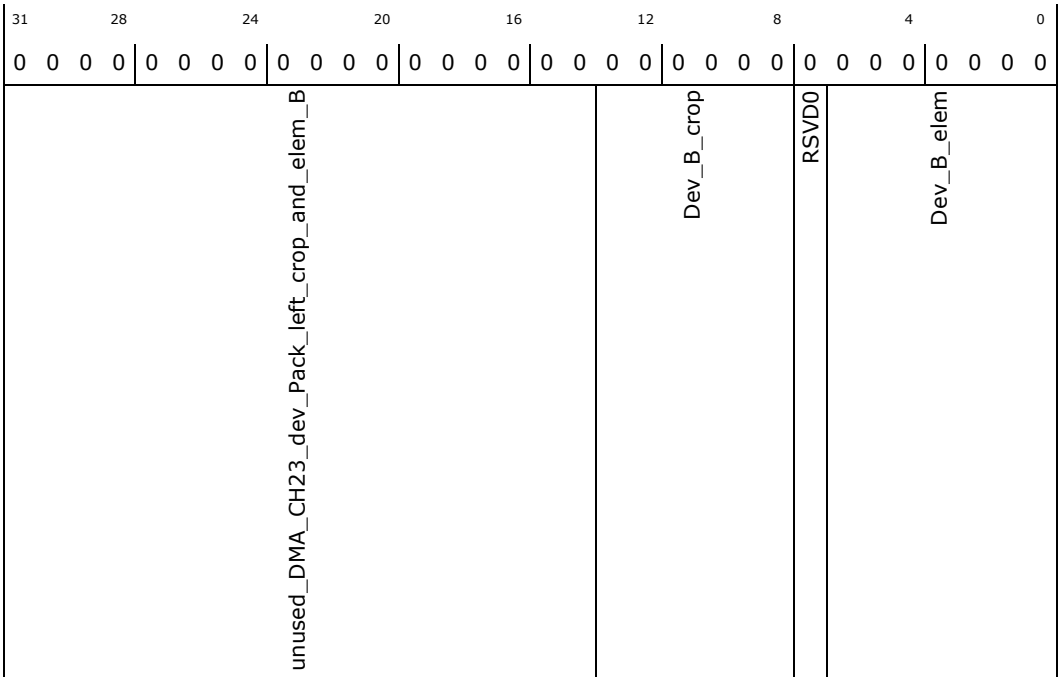
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4155Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH23_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.428 reg_isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_B)—Offset 41560h

DMA CH 24 PARAM 5: Device B Packing LSE cropping/Elements

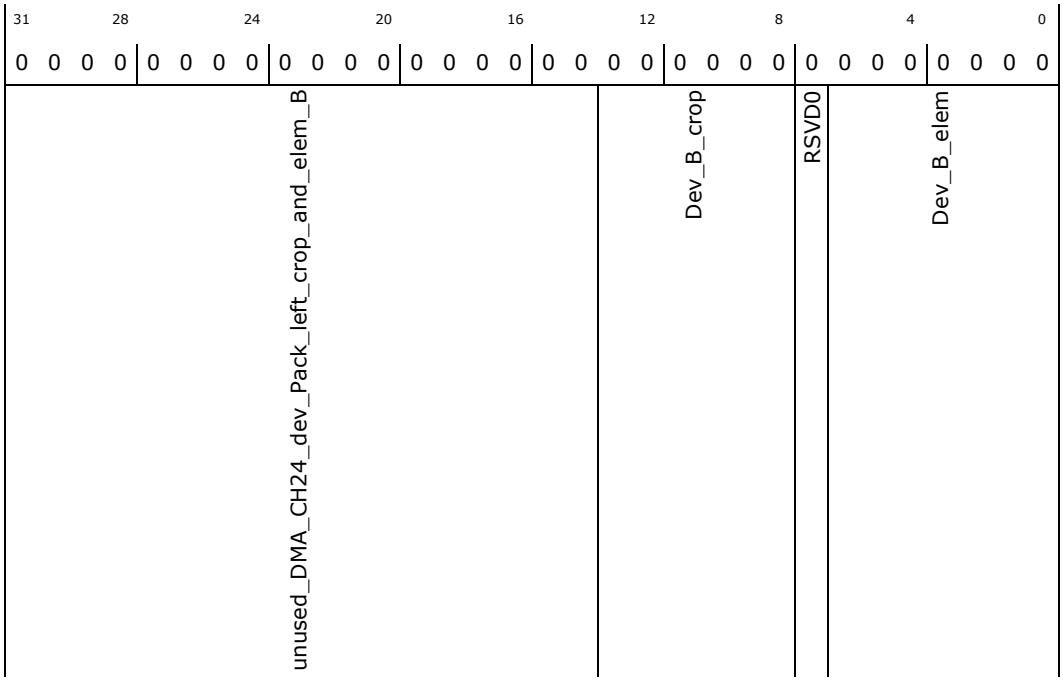
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41560h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH24_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.429 reg_isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_B)—Offset 41564h

DMA CH 25 PARAM 5: Device B Packing LSE cropping/Elements

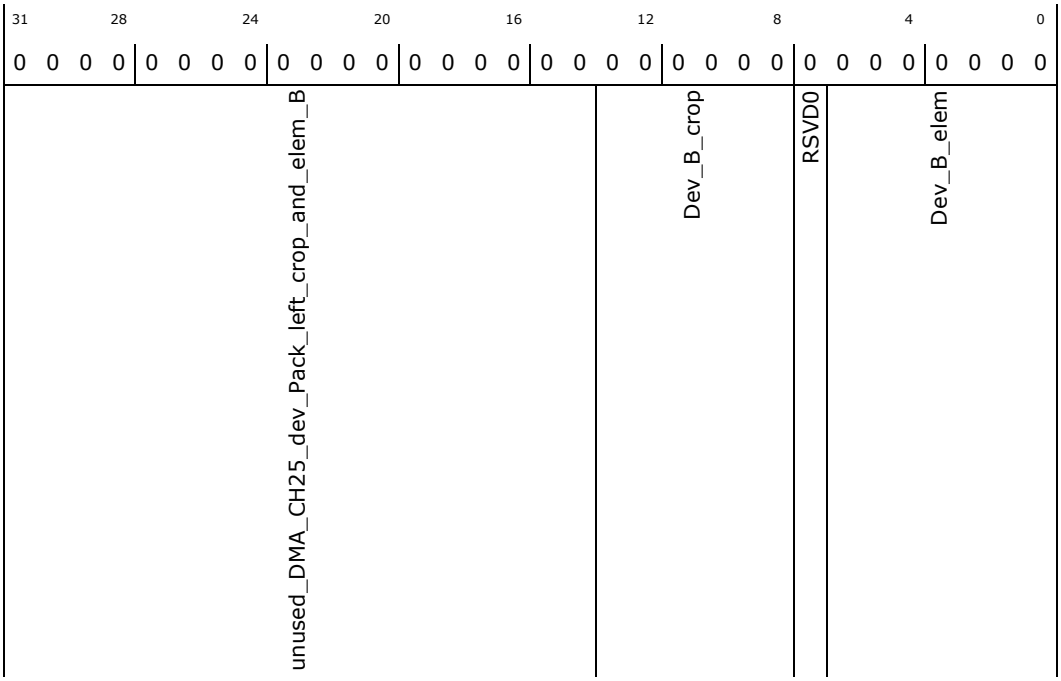
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41564h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH25_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.430 reg_isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_B)—Offset 41568h

DMA CH 26 PARAM 5: Device B Packing LSE cropping/Elements

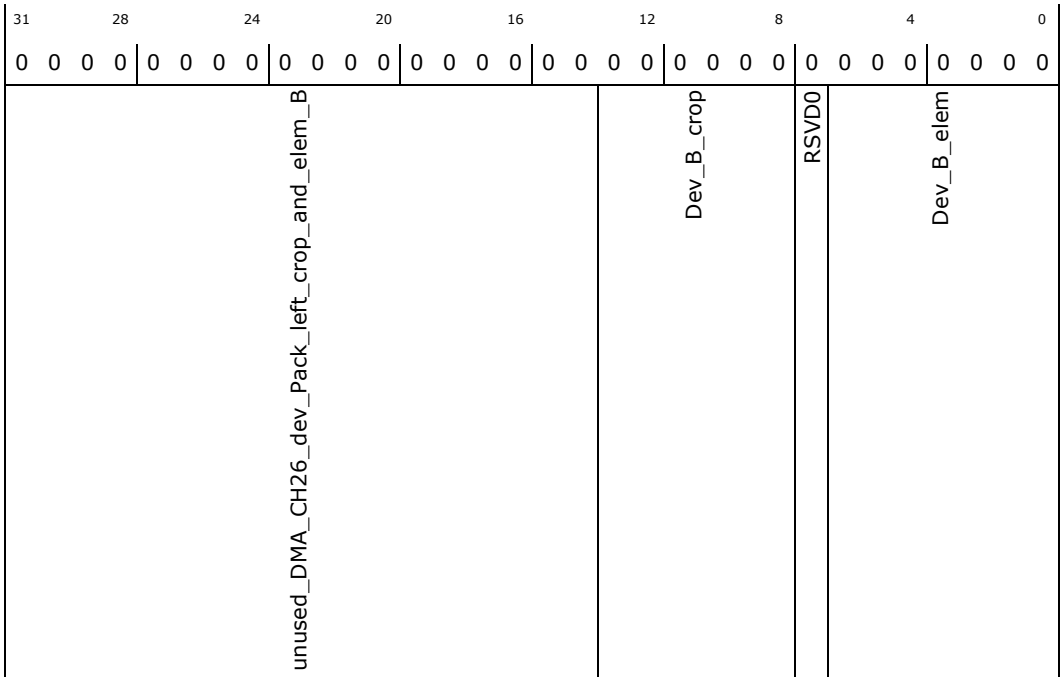
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41568h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH26_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.431 reg_isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_B)—Offset 4156Ch

DMA CH 27 PARAM 5: Device B Packing LSE cropping/Elements

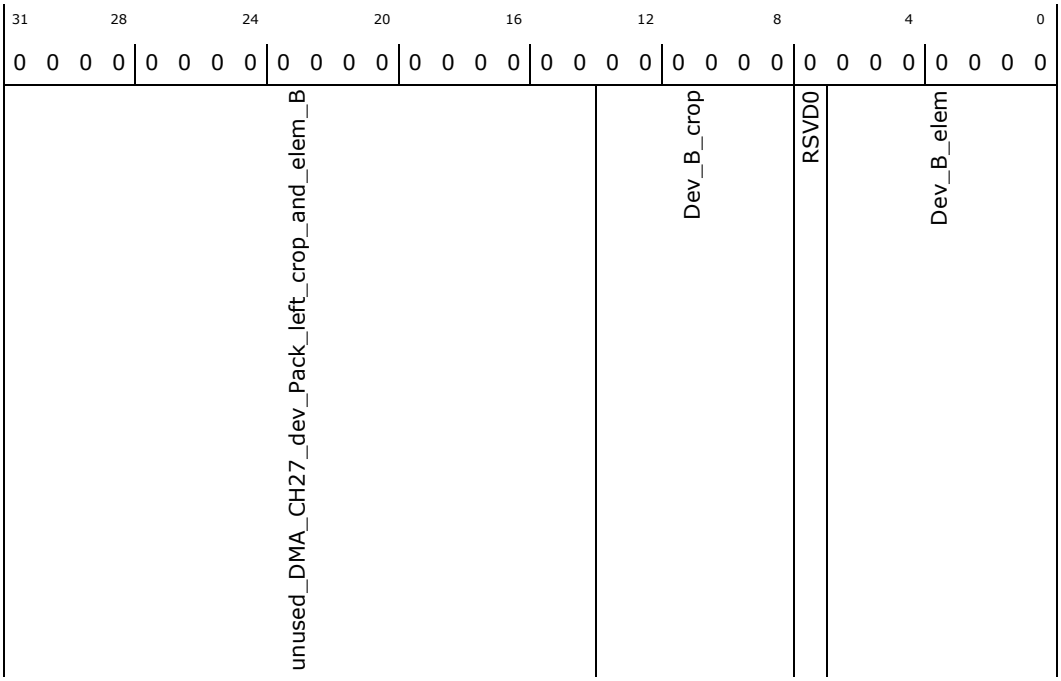
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4156Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH27_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.432 reg_isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_B)—Offset 41570h

DMA CH 28 PARAM 5: Device B Packing LSE cropping/Elements

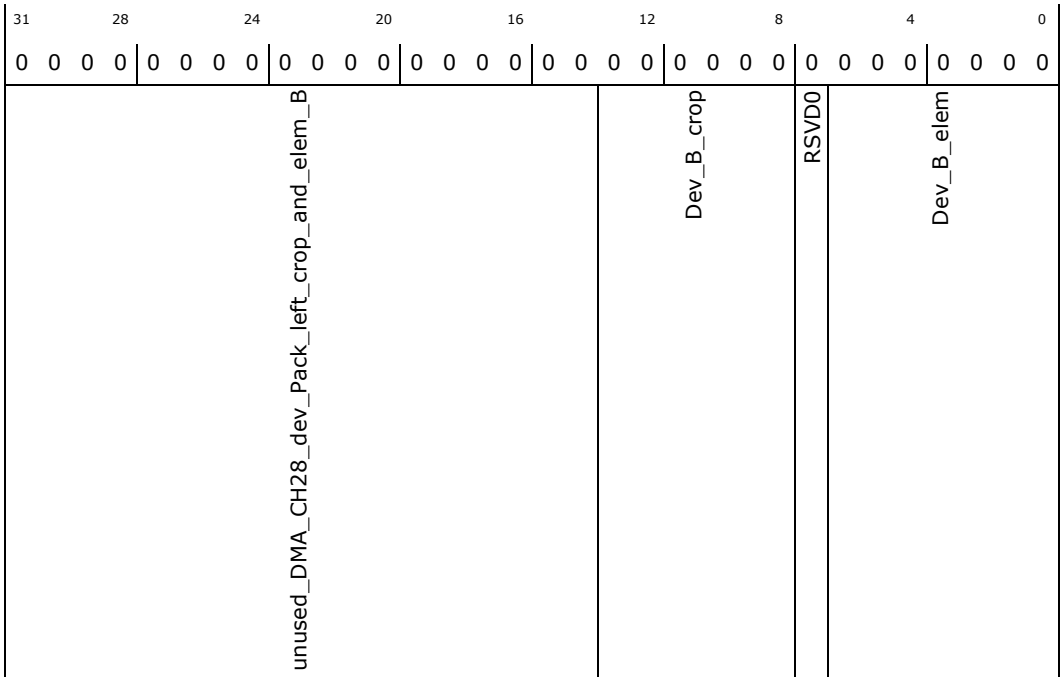
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41570h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH28_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.433 reg_isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_B) —Offset 41574h

DMA CH 29 PARAM 5: Device B Packing LSE cropping/Elements

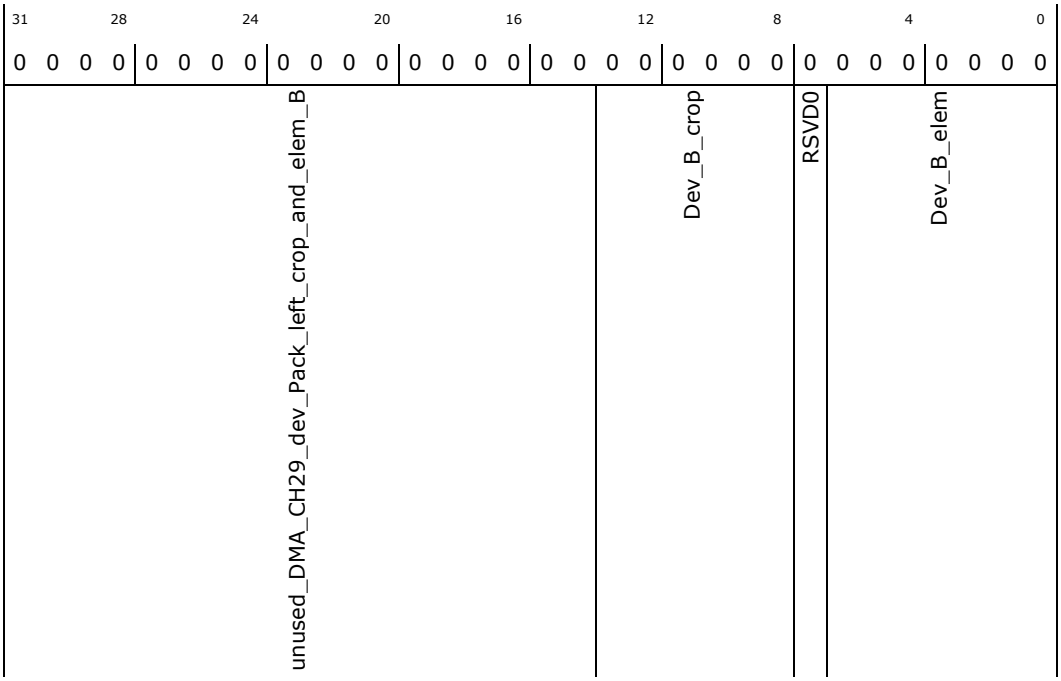
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41574h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH29_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.434 reg_isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_B)—Offset 41578h

DMA CH 30 PARAM 5: Device B Packing LSE cropping/Elements

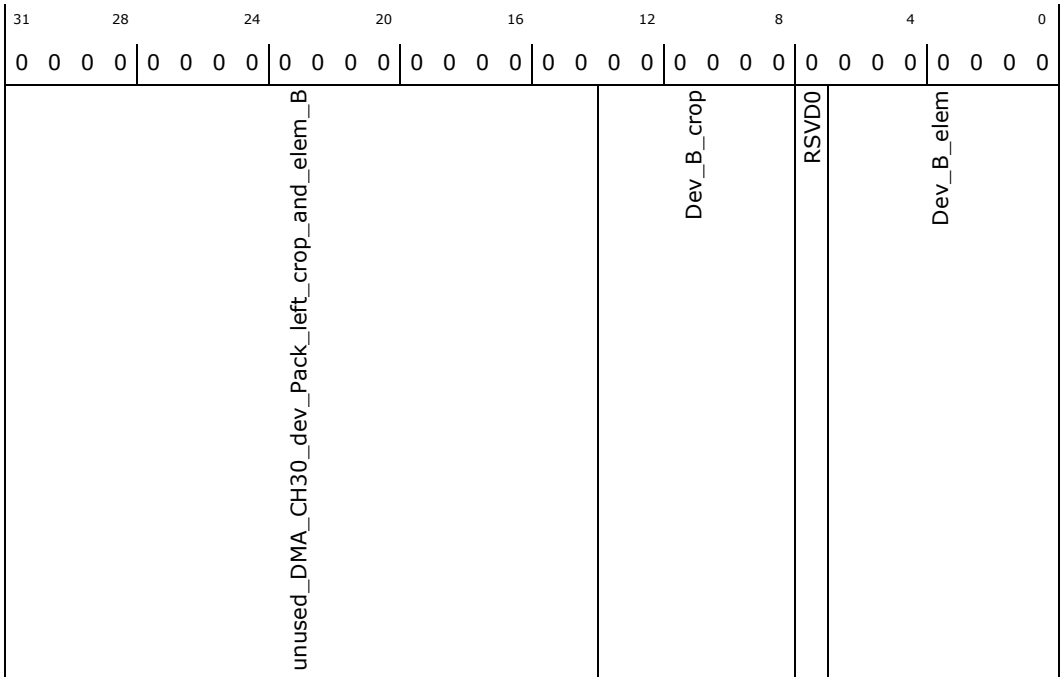
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41578h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH30_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.435 reg_isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_B)—Offset 4157Ch

DMA CH 31 PARAM 5: Device B Packing LSE cropping/Elements

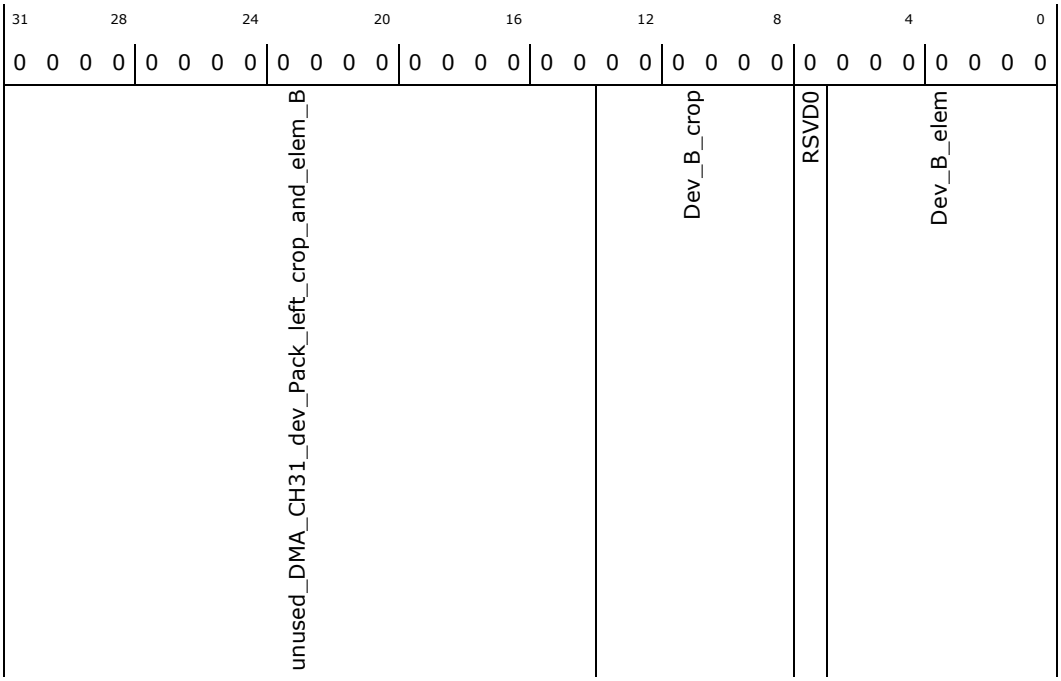
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4157Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH31_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.436 reg_isp_dma_DMA_CH0_Device_Xb_B_type (isp_dma_DMA_CH0_Device_Xb_B)—Offset 41600h

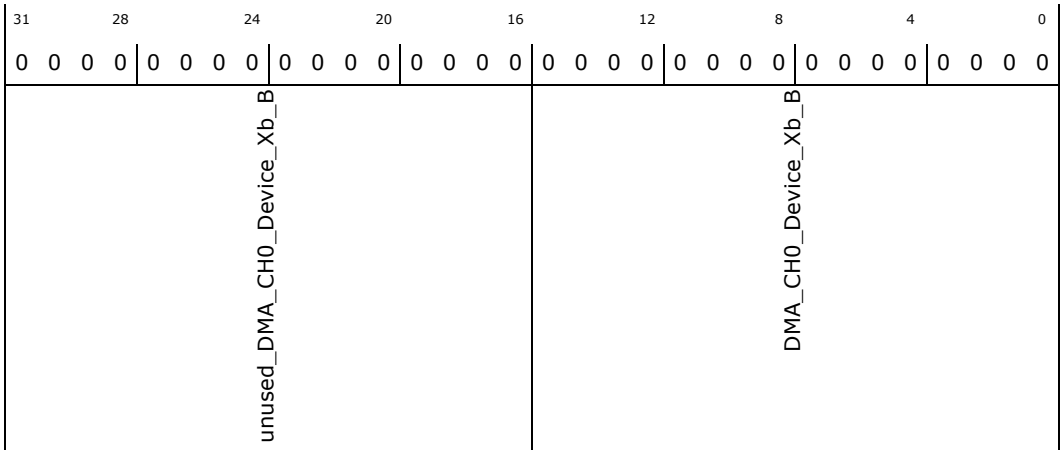
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_Device_Xb_B: [ISPMMADR] + 41600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH0_Device_Xb_B:** DMA CH 0 PARAM 6: Device B block width (Xb)

3.7.437 reg_isp_dma_DMA_CH1_Device_Xb_B_type (isp_dma_DMA_CH1_Device_Xb_B)—Offset 41604h

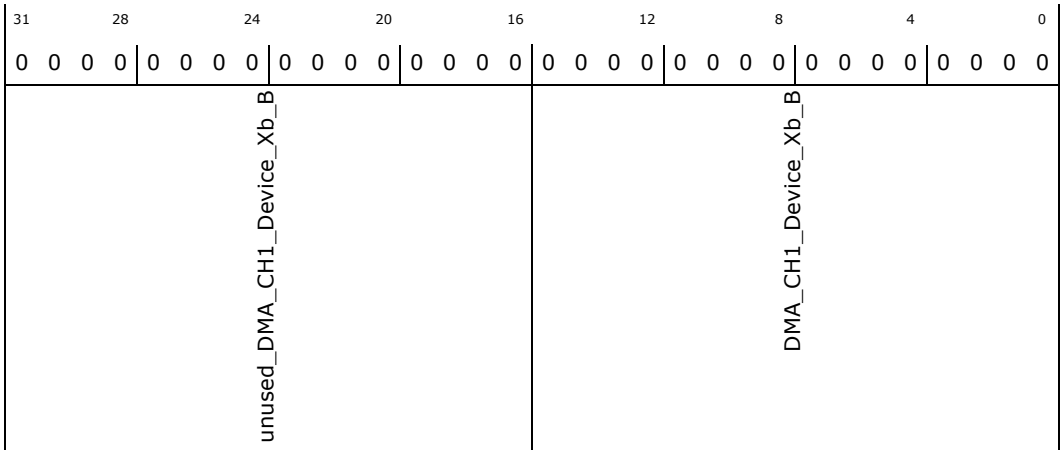
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_Device_Xb_B: [ISPMMADR] + 41604h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH1_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH1_Device_Xb_B:** DMA CH 1 PARAM 6: Device B block width (Xb)

3.7.438 reg_isp_dma_DMA_CH2_Device_Xb_B_type (isp_dma_DMA_CH2_Device_Xb_B)—Offset 41608h

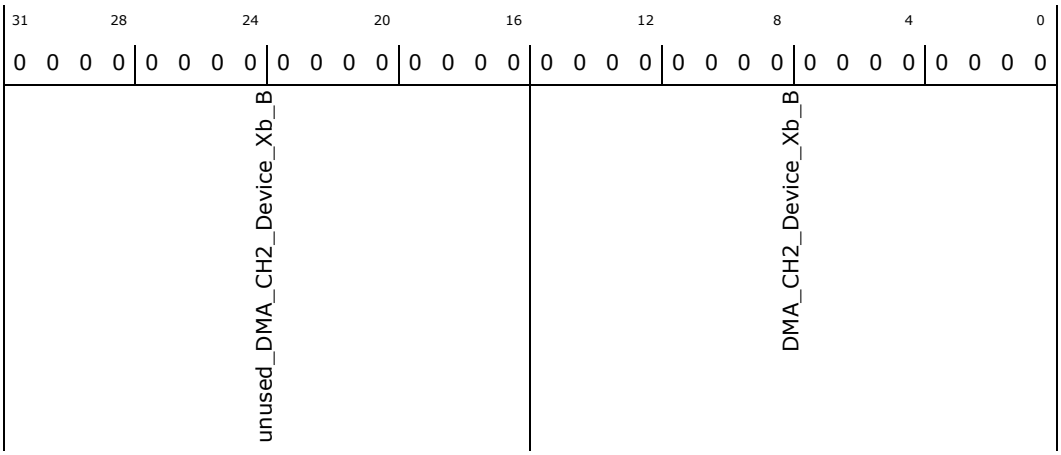
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_Device_Xb_B: [ISPMMADR] + 41608h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH2_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH2_Device_Xb_B:** DMA CH 2 PARAM 6: Device B block width (Xb)

3.7.439 reg_isp_dma_DMA_CH3_Device_Xb_B_type (isp_dma_DMA_CH3_Device_Xb_B)—Offset 4160Ch

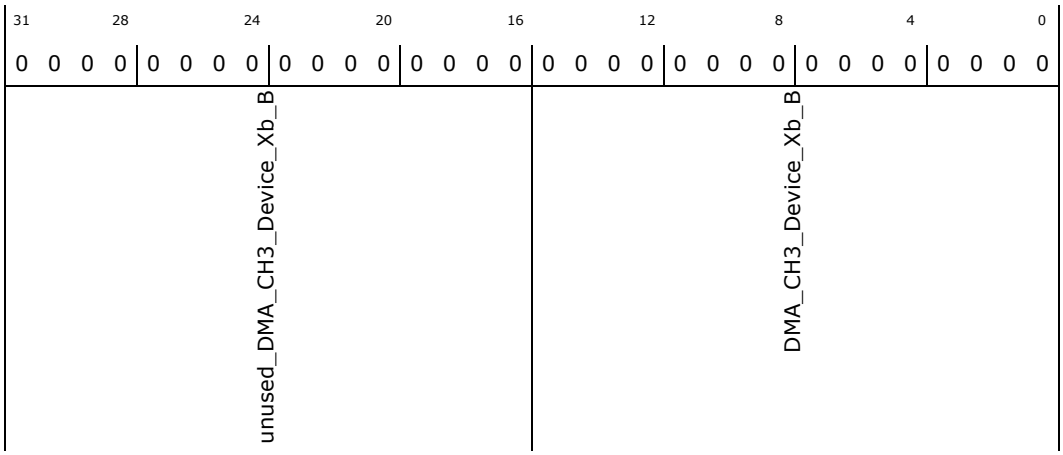
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_Device_Xb_B: [ISPMMADR] + 4160Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH3_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH3_Device_Xb_B:** DMA CH 3 PARAM 6: Device B block width (Xb)

3.7.440 reg_isp_dma_DMA_CH4_Device_Xb_B_type (isp_dma_DMA_CH4_Device_Xb_B)—Offset 41610h

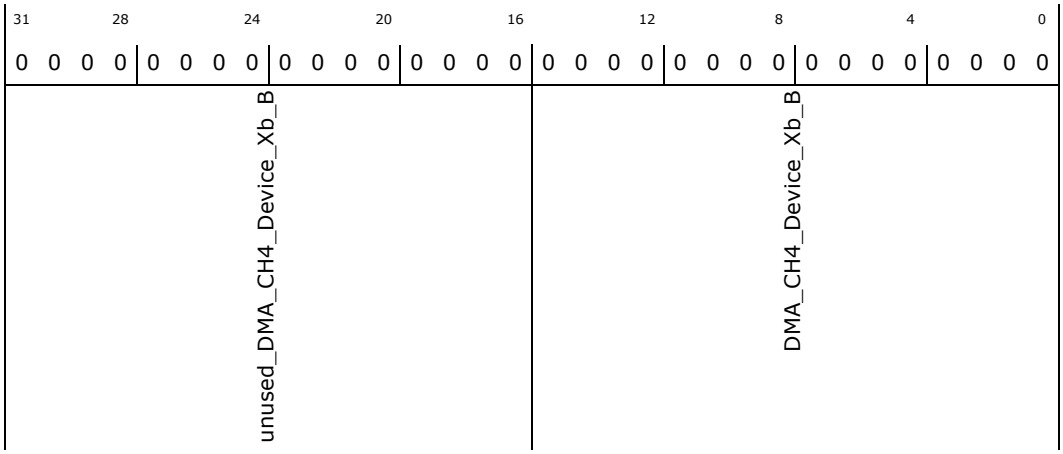
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_Device_Xb_B: [ISPMMADR] + 41610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH4_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH4_Device_Xb_B:** DMA CH 4 PARAM 6: Device B block width (Xb)

3.7.441 reg_isp_dma_DMA_CH5_Device_Xb_B_type (isp_dma_DMA_CH5_Device_Xb_B)—Offset 41614h

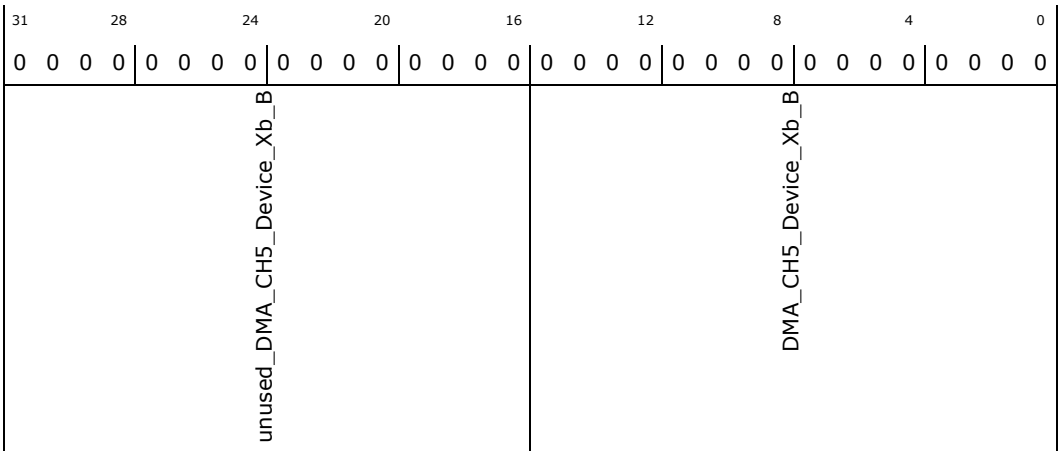
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_Device_Xb_B: [ISPMMADR] + 41614h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH5_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH5_Device_Xb_B:** DMA CH 5 PARAM 6: Device B block width (Xb)

3.7.442 reg_isp_dma_DMA_CH6_Device_Xb_B_type (isp_dma_DMA_CH6_Device_Xb_B)—Offset 41618h

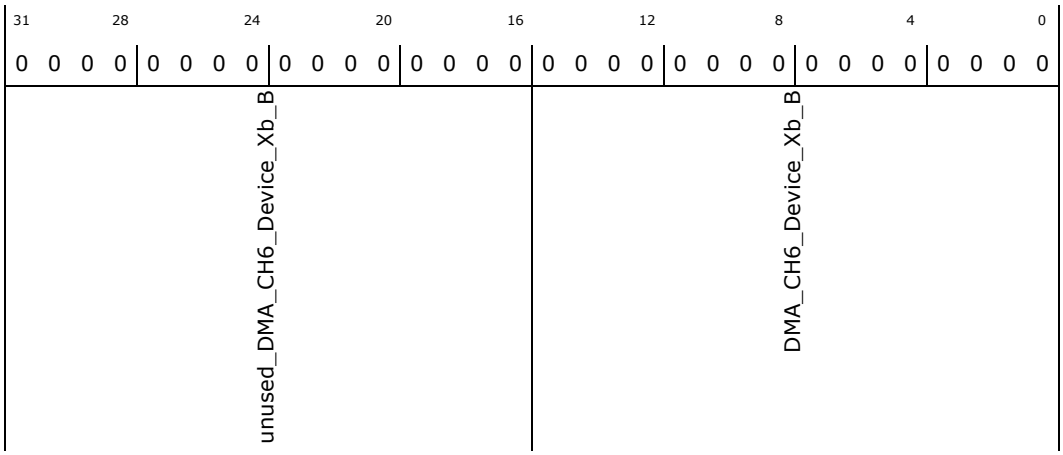
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_Device_Xb_B: [ISPMMADR] + 41618h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH6_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH6_Device_Xb_B:** DMA CH 6 PARAM 6: Device B block width (Xb)

3.7.443 reg_isp_dma_DMA_CH7_Device_Xb_B_type (isp_dma_DMA_CH7_Device_Xb_B)—Offset 4161Ch

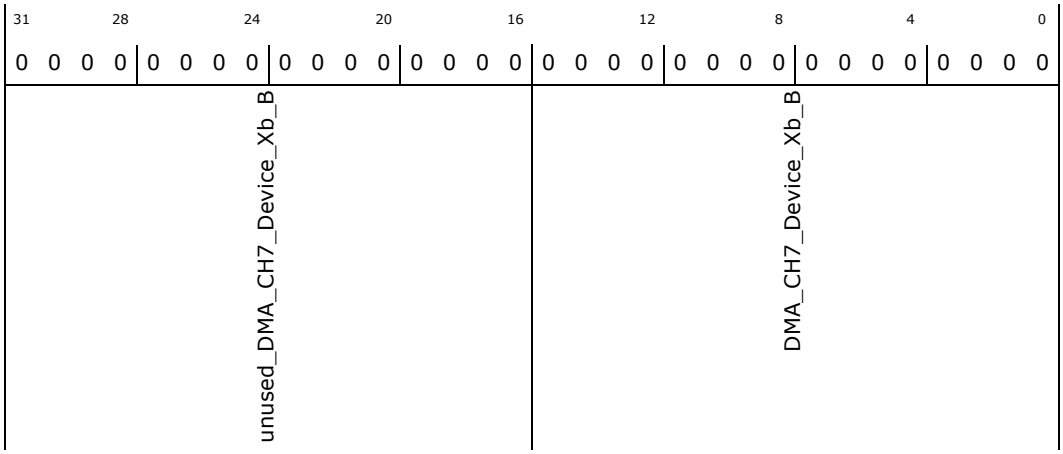
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_Device_Xb_B: [ISPMMADR] + 4161Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH7_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH7_Device_Xb_B:** DMA CH 7 PARAM 6: Device B block width (Xb)

3.7.444 reg_isp_dma_DMA_CH8_Device_Xb_B_type (isp_dma_DMA_CH8_Device_Xb_B)—Offset 41620h

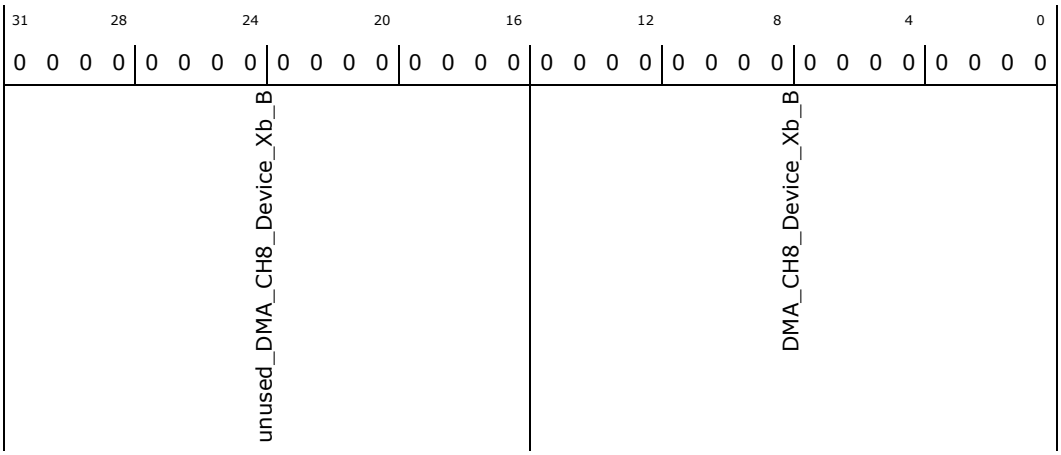
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_Device_Xb_B: [ISPMMADR] + 41620h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH8_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH8_Device_Xb_B:** DMA CH 8 PARAM 6: Device B block width (Xb)

3.7.445 reg_isp_dma_DMA_CH9_Device_Xb_B_type (isp_dma_DMA_CH9_Device_Xb_B)—Offset 41624h

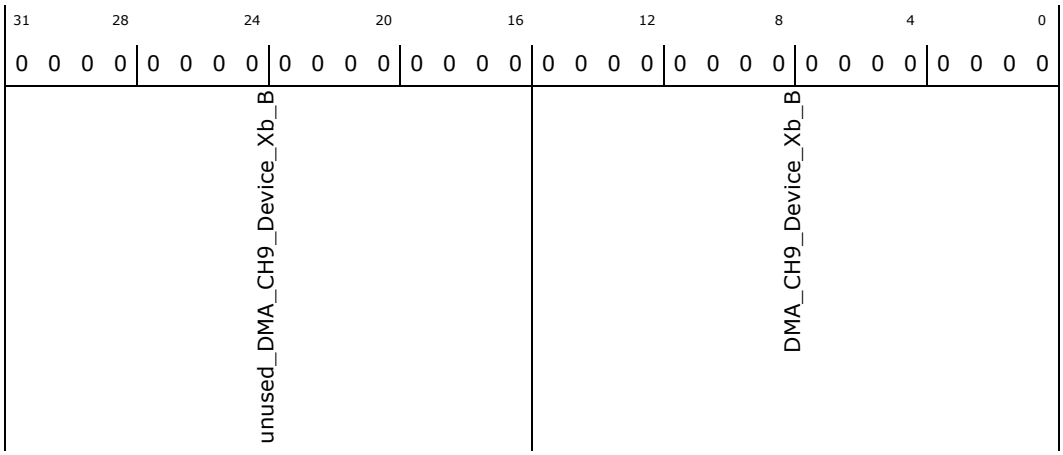
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_Device_Xb_B: [ISPMMADR] + 41624h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH9_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH9_Device_Xb_B:** DMA CH 9 PARAM 6: Device B block width (Xb)

3.7.446 reg_isp_dma_DMA_CH10_Device_Xb_B_type (isp_dma_DMA_CH10_Device_Xb_B)—Offset 41628h

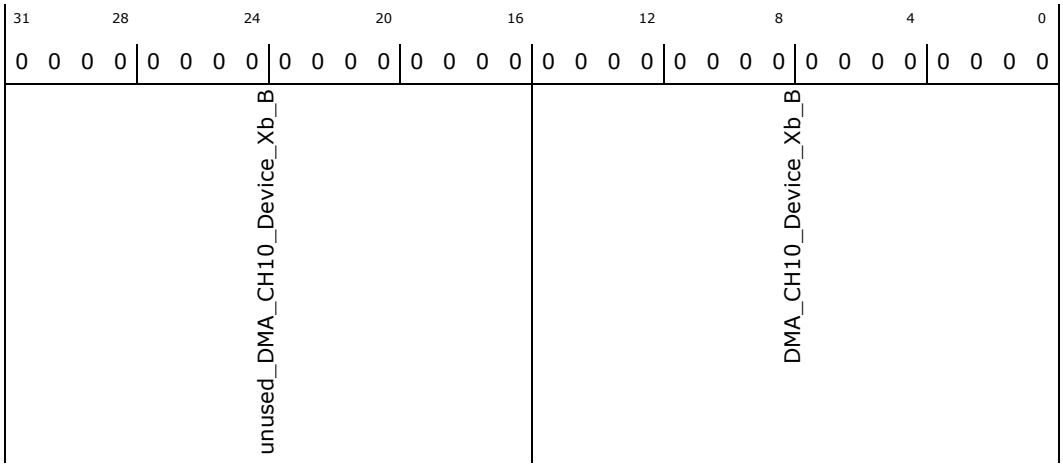
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_Device_Xb_B: [ISPMMADR] + 41628h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH10_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH10_Device_Xb_B:** DMA CH 10 PARAM 6: Device B block width (Xb)

3.7.447 reg_isp_dma_DMA_CH11_Device_Xb_B_type (isp_dma_DMA_CH11_Device_Xb_B)—Offset 4162Ch

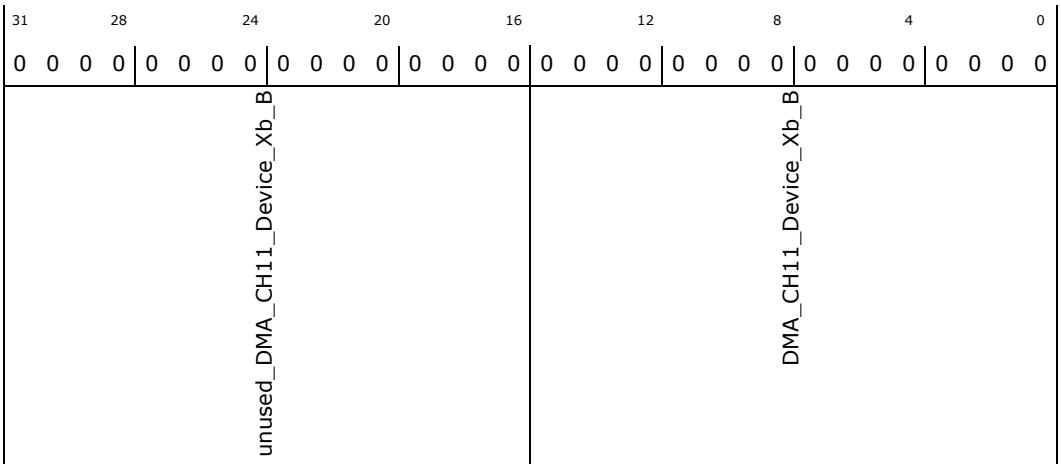
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_Device_Xb_B: [ISPMMADR] + 4162Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH11_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH11_Device_Xb_B:** DMA CH 11 PARAM 6: Device B block width (Xb)

3.7.448 reg_isp_dma_DMA_CH12_Device_Xb_B_type (isp_dma_DMA_CH12_Device_Xb_B)—Offset 41630h

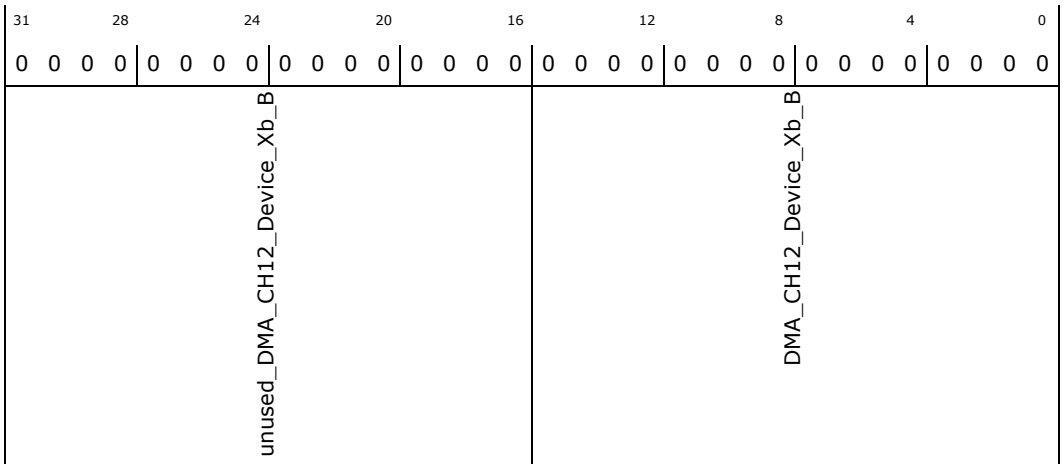
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_Device_Xb_B: [ISPMMADR] + 41630h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH12_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH12_Device_Xb_B:** DMA CH 12 PARAM 6: Device B block width (Xb)

3.7.449 reg_isp_dma_DMA_CH13_Device_Xb_B_type (isp_dma_DMA_CH13_Device_Xb_B)—Offset 41634h

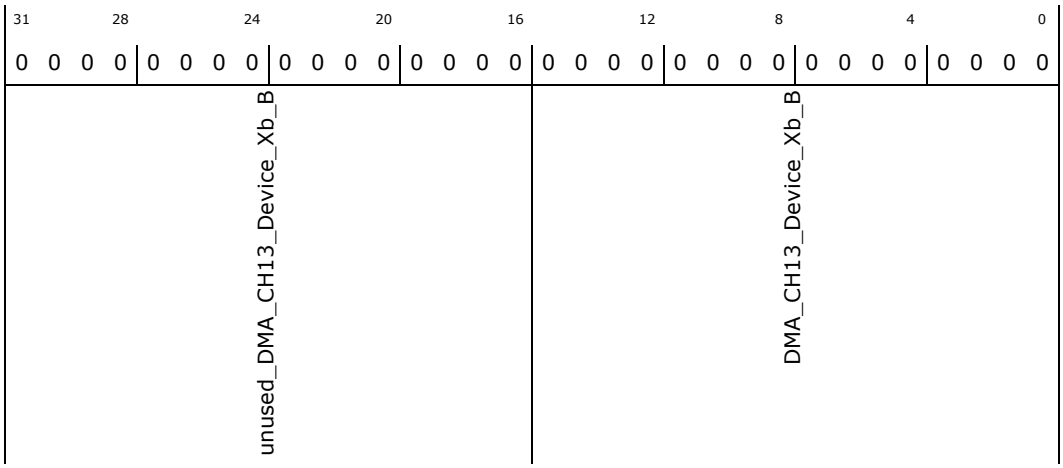
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_Device_Xb_B: [ISPMMADR] + 41634h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH13_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH13_Device_Xb_B:** DMA CH 13 PARAM 6: Device B block width (Xb)

3.7.450 reg_isp_dma_DMA_CH14_Device_Xb_B_type (isp_dma_DMA_CH14_Device_Xb_B)—Offset 41638h

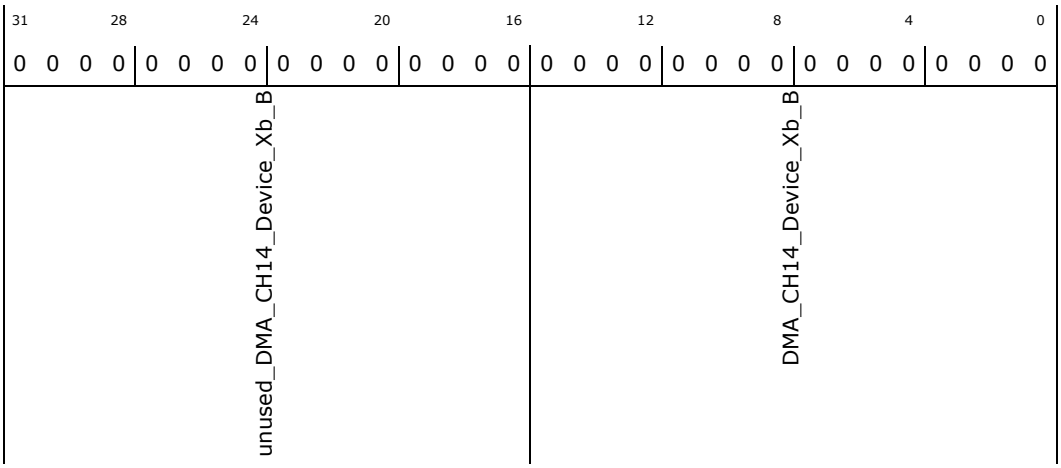
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_Device_Xb_B: [ISPMMADR] + 41638h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH14_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH14_Device_Xb_B:** DMA CH 14 PARAM 6: Device B block width (Xb)

3.7.451 reg_isp_dma_DMA_CH15_Device_Xb_B_type (isp_dma_DMA_CH15_Device_Xb_B)—Offset 4163Ch

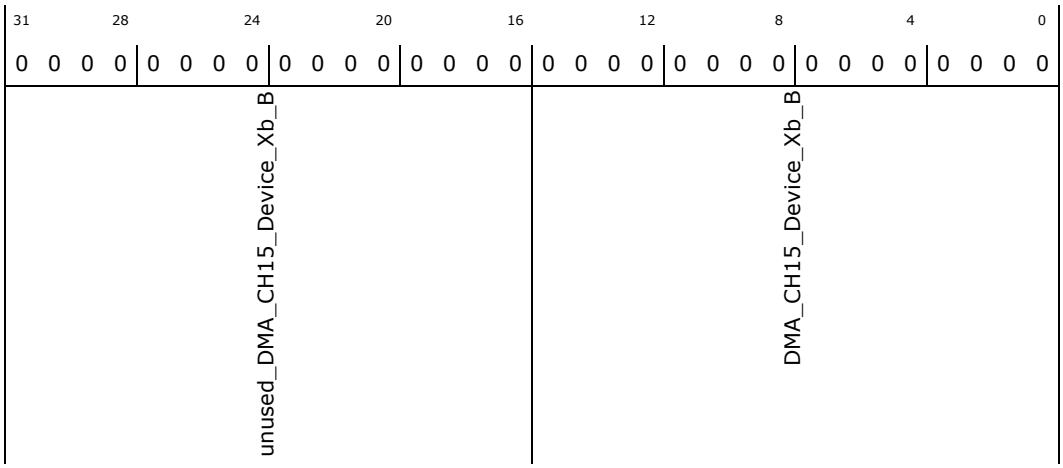
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_Device_Xb_B: [ISPMMADR] + 4163Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH15_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH15_Device_Xb_B:** DMA CH 15 PARAM 6: Device B block width (Xb)

3.7.452 reg_isp_dma_DMA_CH16_Device_Xb_B_type (isp_dma_DMA_CH16_Device_Xb_B)—Offset 41640h

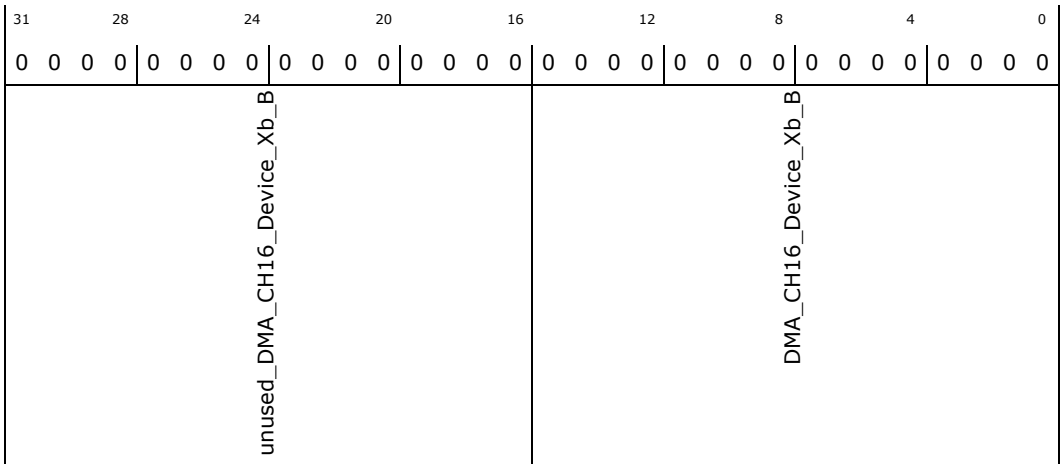
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_Device_Xb_B: [ISPMMADR] + 41640h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH16_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH16_Device_Xb_B:** DMA CH 16 PARAM 6: Device B block width (Xb)

3.7.453 reg_isp_dma_DMA_CH17_Device_Xb_B_type (isp_dma_DMA_CH17_Device_Xb_B)—Offset 41644h

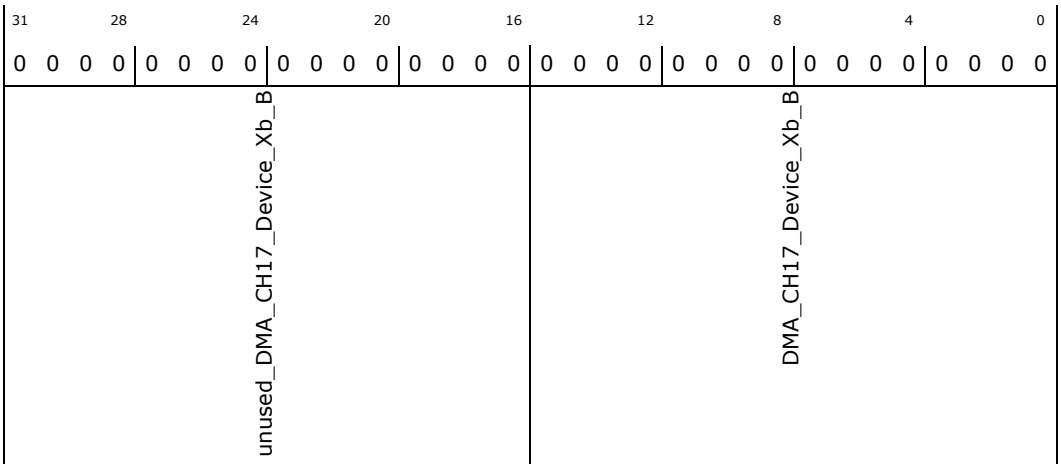
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_Device_Xb_B: [ISPMMADR] + 41644h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH17_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH17_Device_Xb_B:** DMA CH 17 PARAM 6: Device B block width (Xb)

3.7.454 reg_isp_dma_DMA_CH18_Device_Xb_B_type (isp_dma_DMA_CH18_Device_Xb_B)—Offset 41648h

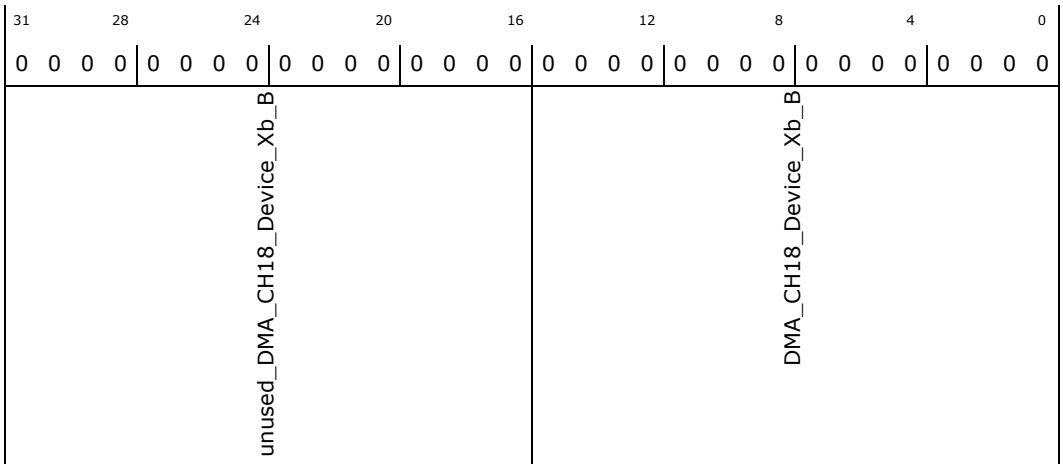
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_Device_Xb_B: [ISPMMADR] + 41648h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH18_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH18_Device_Xb_B:** DMA CH 18 PARAM 6: Device B block width (Xb)

3.7.455 reg_isp_dma_DMA_CH19_Device_Xb_B_type (isp_dma_DMA_CH19_Device_Xb_B)—Offset 4164Ch

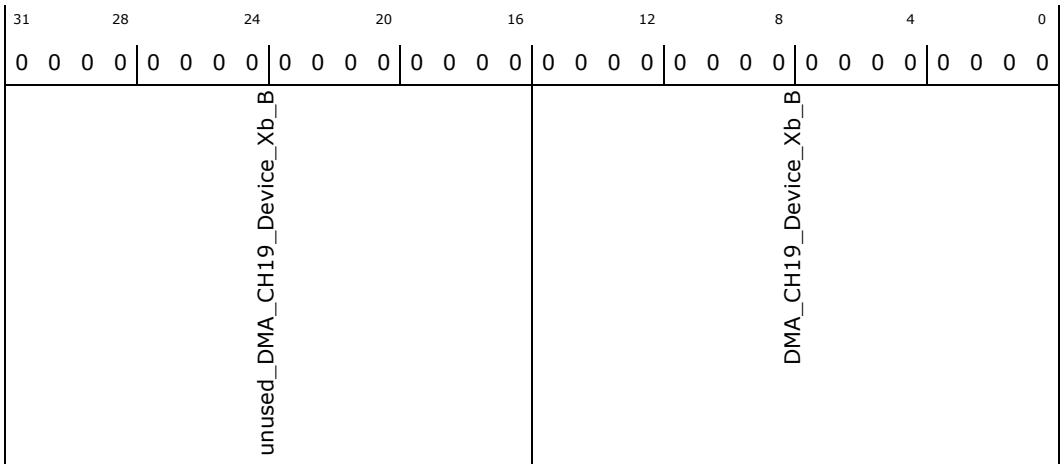
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_Device_Xb_B: [ISPMMADR] + 4164Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH19_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH19_Device_Xb_B:** DMA CH 19 PARAM 6: Device B block width (Xb)

3.7.456 reg_isp_dma_DMA_CH20_Device_Xb_B_type (isp_dma_DMA_CH20_Device_Xb_B)—Offset 41650h

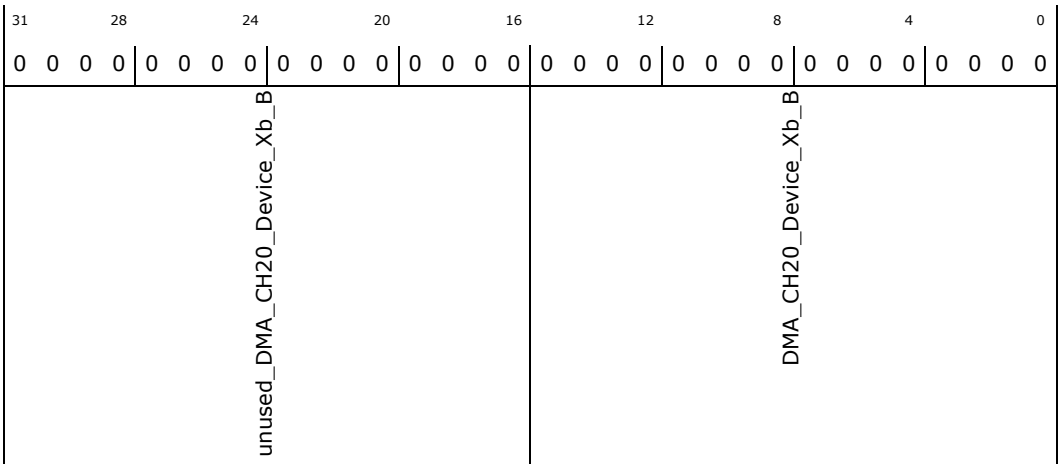
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_Device_Xb_B: [ISPMMADR] + 41650h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH20_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH20_Device_Xb_B:** DMA CH 20 PARAM 6: Device B block width (Xb)

3.7.457 reg_isp_dma_DMA_CH21_Device_Xb_B_type (isp_dma_DMA_CH21_Device_Xb_B)—Offset 41654h

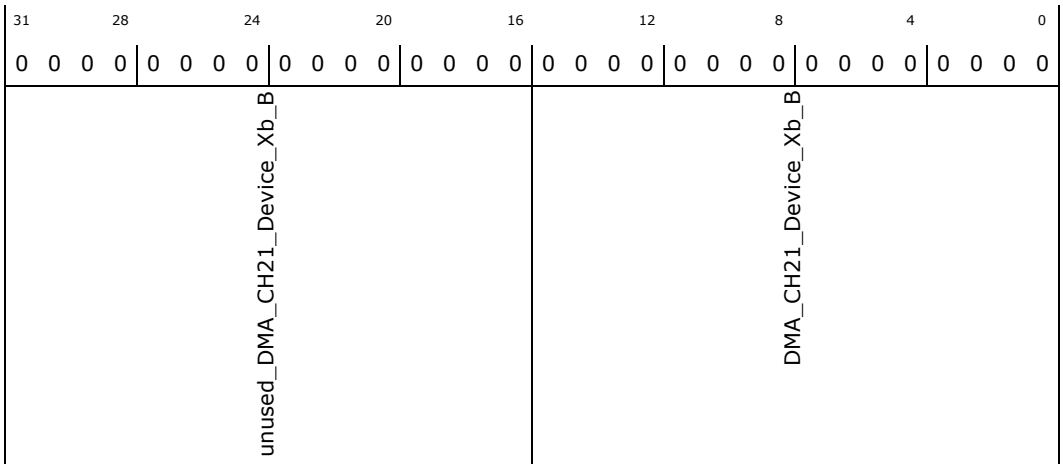
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_Device_Xb_B: [ISPMMADR] + 41654h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH21_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH21_Device_Xb_B:** DMA CH 21 PARAM 6: Device B block width (Xb)

3.7.458 reg_isp_dma_DMA_CH22_Device_Xb_B_type (isp_dma_DMA_CH22_Device_Xb_B)—Offset 41658h

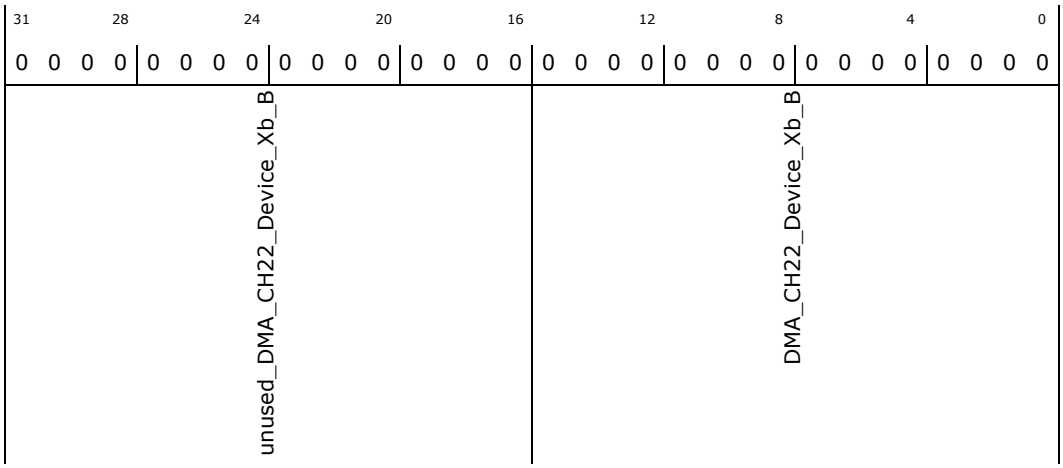
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_Device_Xb_B: [ISPMMADR] + 41658h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH22_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH22_Device_Xb_B:** DMA CH 22 PARAM 6: Device B block width (Xb)

3.7.459 reg_isp_dma_DMA_CH23_Device_Xb_B_type (isp_dma_DMA_CH23_Device_Xb_B)—Offset 4165Ch

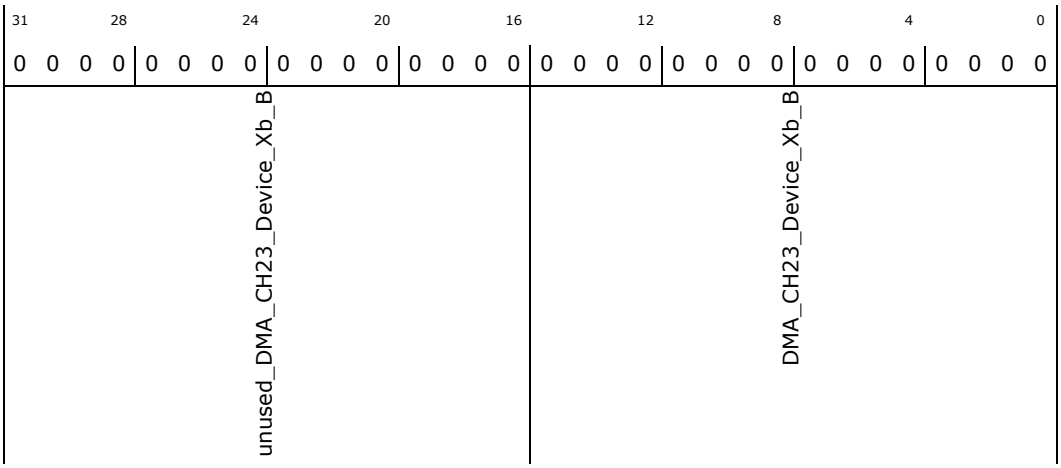
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_Device_Xb_B: [ISPMMADR] + 4165Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH23_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH23_Device_Xb_B:** DMA CH 23 PARAM 6: Device B block width (Xb)

3.7.460 reg_isp_dma_DMA_CH24_Device_Xb_B_type (isp_dma_DMA_CH24_Device_Xb_B)—Offset 41660h

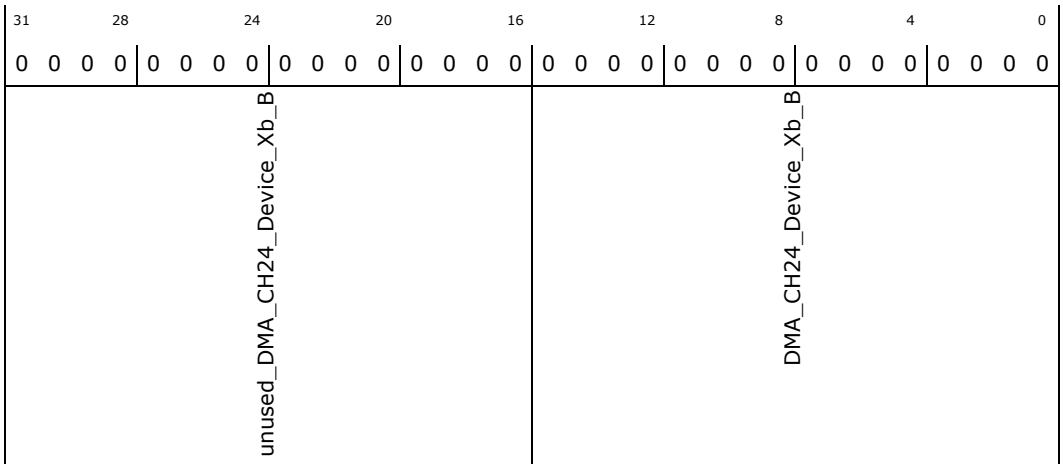
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_Device_Xb_B: [ISPMMADR] + 41660h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH24_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH24_Device_Xb_B:** DMA CH 24 PARAM 6: Device B block width (Xb)

3.7.461 reg_isp_dma_DMA_CH25_Device_Xb_B_type (isp_dma_DMA_CH25_Device_Xb_B)—Offset 41664h

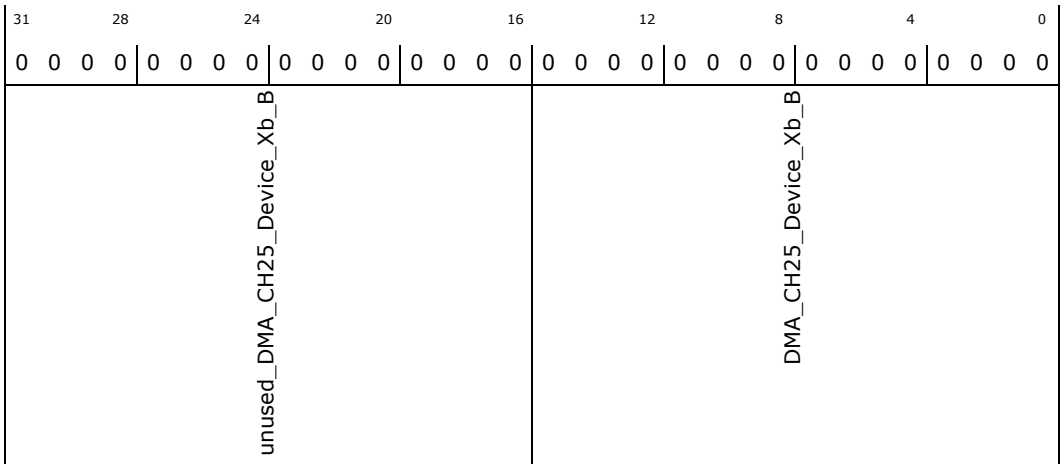
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_Device_Xb_B: [ISPMMADR] + 41664h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH25_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH25_Device_Xb_B:** DMA CH 25 PARAM 6: Device B block width (Xb)

3.7.462 reg_isp_dma_DMA_CH26_Device_Xb_B_type (isp_dma_DMA_CH26_Device_Xb_B)—Offset 41668h

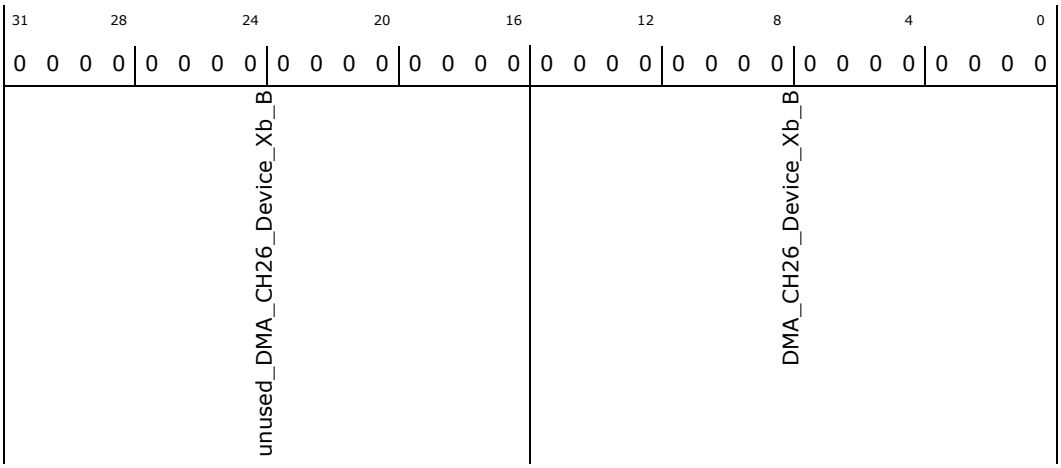
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_Device_Xb_B: [ISPMMADR] + 41668h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH26_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH26_Device_Xb_B:** DMA CH 26 PARAM 6: Device B block width (Xb)

3.7.463 reg_isp_dma_DMA_CH27_Device_Xb_B_type (isp_dma_DMA_CH27_Device_Xb_B)—Offset 4166Ch

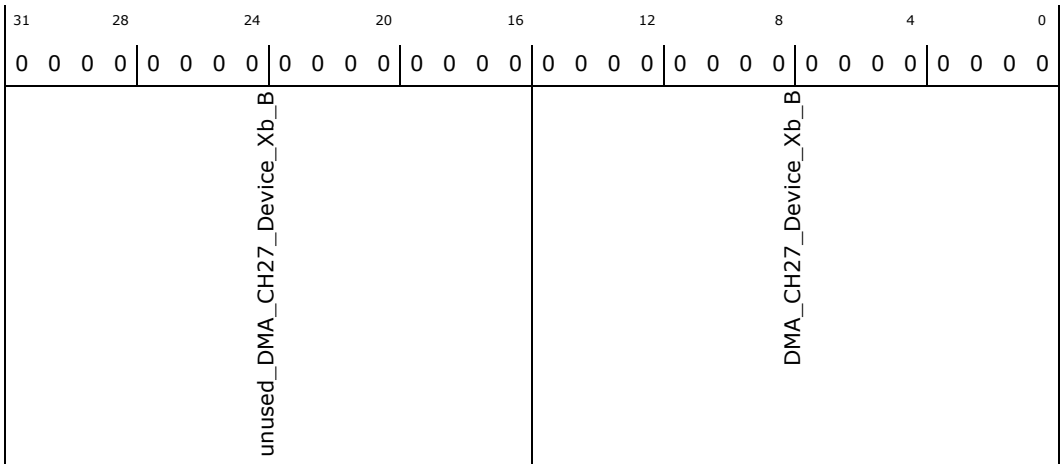
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_Device_Xb_B: [ISPMMADR] + 4166Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH27_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH27_Device_Xb_B:** DMA CH 27 PARAM 6: Device B block width (Xb)

3.7.464 reg_isp_dma_DMA_CH28_Device_Xb_B_type (isp_dma_DMA_CH28_Device_Xb_B)—Offset 41670h

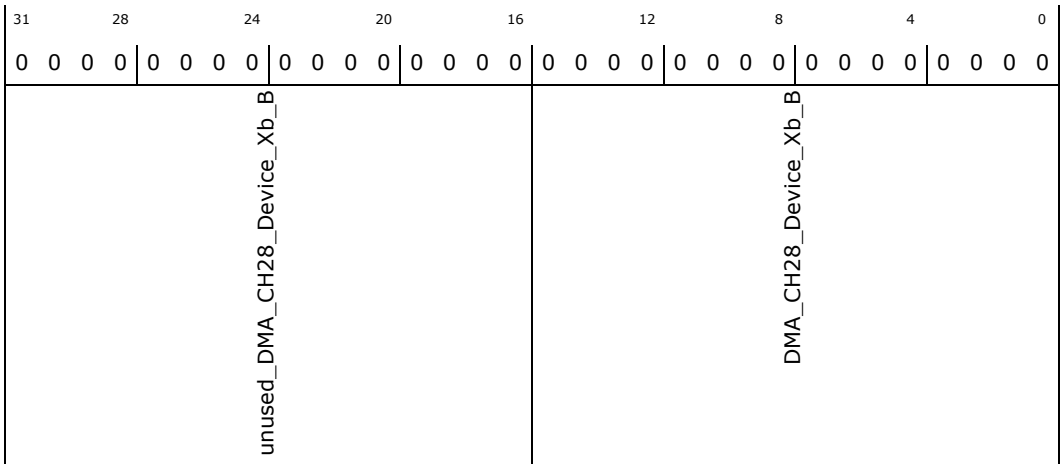
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_Device_Xb_B: [ISPMMADR] + 41670h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH28_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH28_Device_Xb_B:** DMA CH 28 PARAM 6: Device B block width (Xb)

3.7.465 reg_isp_dma_DMA_CH29_Device_Xb_B_type (isp_dma_DMA_CH29_Device_Xb_B)—Offset 41674h

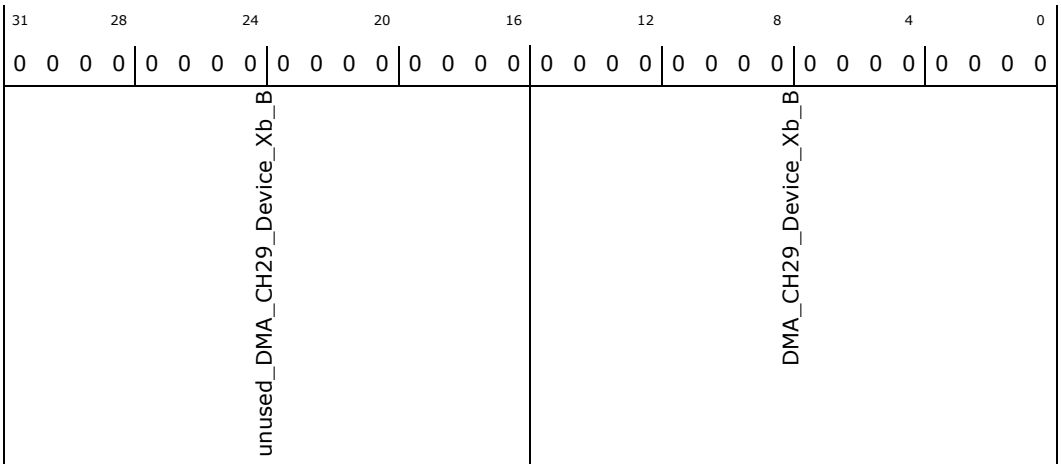
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_Device_Xb_B: [ISPMMADR] + 41674h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH29_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH29_Device_Xb_B:** DMA CH 29 PARAM 6: Device B block width (Xb)

3.7.466 reg_isp_dma_DMA_CH31_Device_Xb_B_type (isp_dma_DMA_CH31_Device_Xb_B)—Offset 41678h

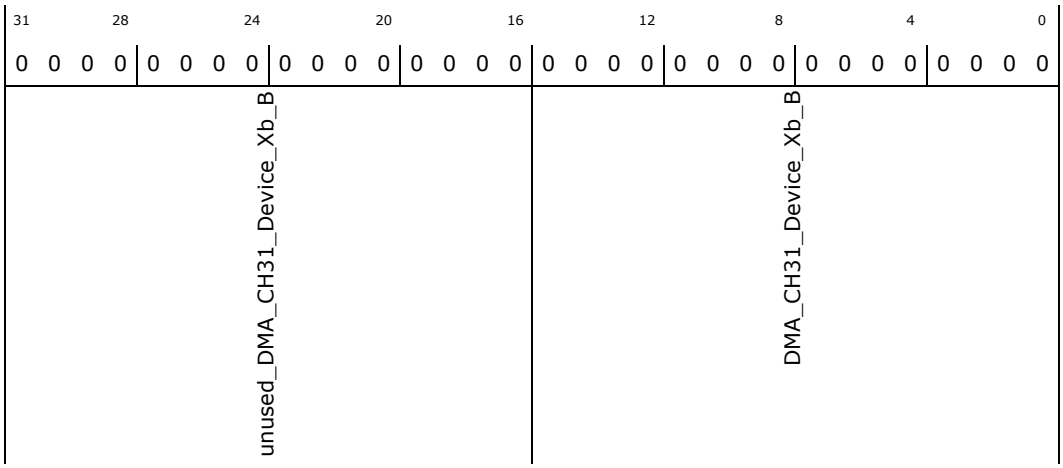
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_Device_Xb_B: [ISPMMADR] + 41678h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH31_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH31_Device_Xb_B:** DMA CH 31 PARAM 6: Device B block width (Xb)

3.7.467 reg_isp_dma_DMA_CH0_Yb_type (isp_dma_DMA_CH0_Yb)—Offset 41700h

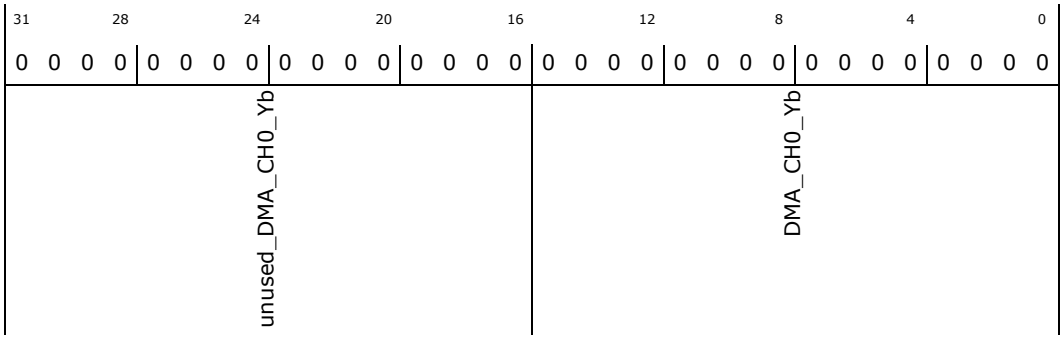
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_Yb: [ISPMMADR] + 41700h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Yb:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH0_Yb:** DMA CH 0 PARAM 7: block Height (Yb)

3.7.468 reg_isp_dma_DMA_CH1_Yb_type (isp_dma_DMA_CH1_Yb)—Offset 41704h

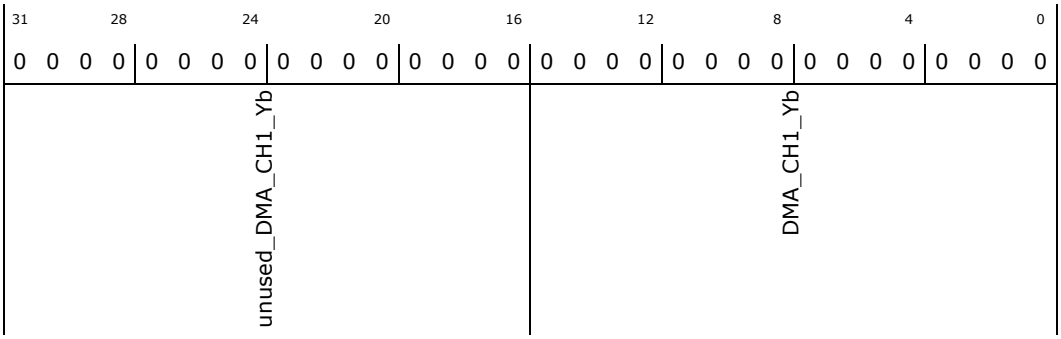
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_Yb: [ISPMMADR] + 41704h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH1_Yb:** Unused
15:0	0h RO	**DMA_CH1_Yb:** DMA CH 1 PARAM 7: block Height (Yb)

3.7.469 reg_isp_dma_DMA_CH2_Yb_type (isp_dma_DMA_CH2_Yb)—Offset 41708h

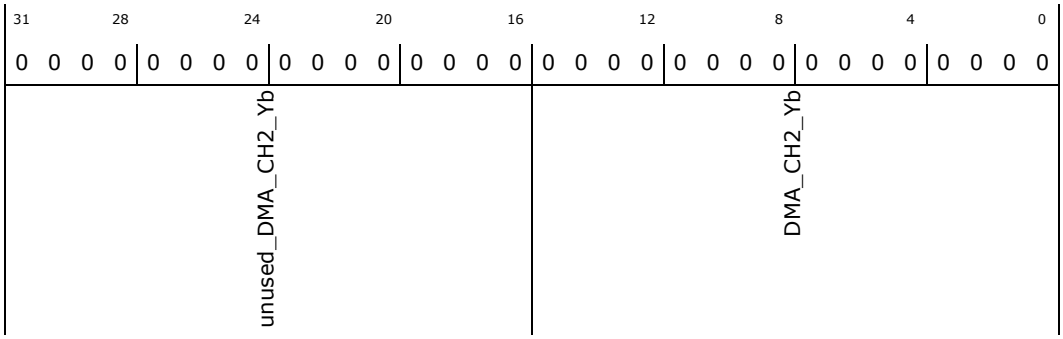
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_Yb: [ISPMMADR] + 41708h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH2_Yb:** Unused
15:0	0h RO	**DMA_CH2_Yb:** DMA CH 2 PARAM 7: block Height (Yb)

3.7.470 reg_isp_dma_DMA_CH3_Yb_type (isp_dma_DMA_CH3_Yb)—Offset 4170Ch

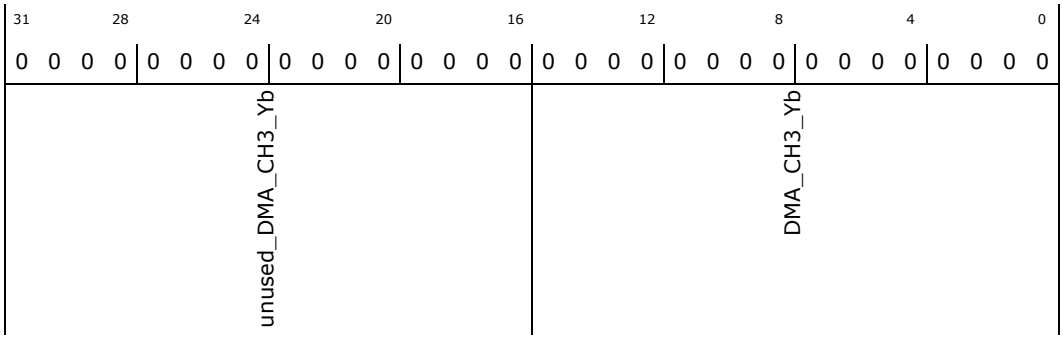
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_Yb: [ISPMMADR] + 4170Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH3_Yb:** Unused
15:0	0h RO	**DMA_CH3_Yb:** DMA CH 3 PARAM 7: block Height (Yb)

3.7.471 reg_isp_dma_DMA_CH4_Yb_type (isp_dma_DMA_CH4_Yb)—Offset 41710h

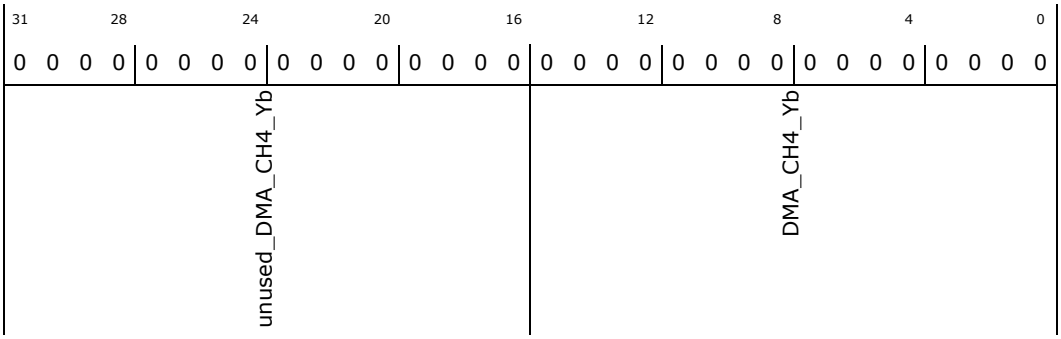
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_Yb: [ISPMMADR] + 41710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH4_Yb:** Unused
15:0	0h RO	**DMA_CH4_Yb:** DMA CH 4 PARAM 7: block Height (Yb)

3.7.472 reg_isp_dma_DMA_CH5_Yb_type (isp_dma_DMA_CH5_Yb)—Offset 41714h

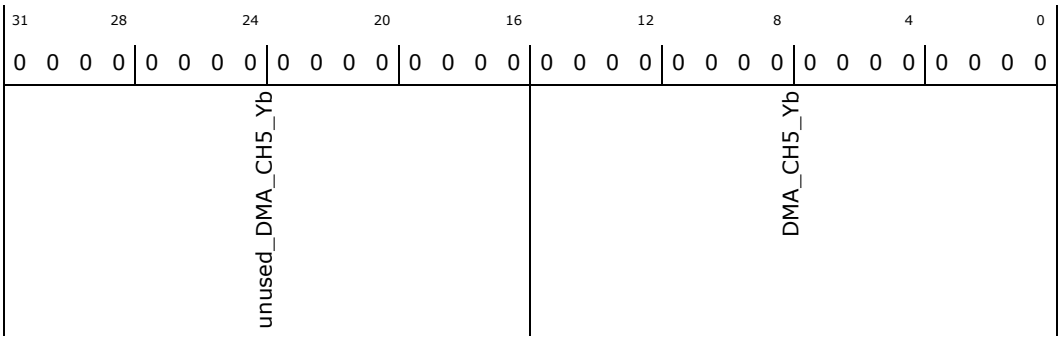
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_Yb: [ISPMMADR] + 41714h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH5_Yb:** Unused
15:0	0h RO	**DMA_CH5_Yb:** DMA CH 5 PARAM 7: block Height (Yb)

3.7.473 reg_isp_dma_DMA_CH6_Yb_type (isp_dma_DMA_CH6_Yb)—Offset 41718h

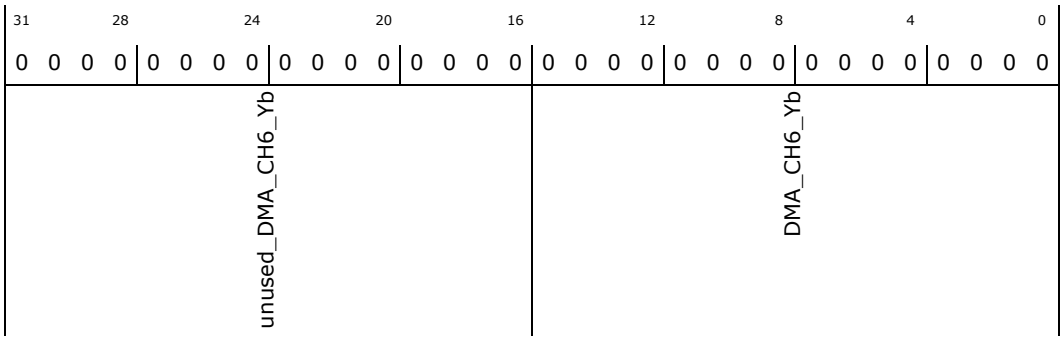
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_Yb: [ISPMMADR] + 41718h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH6_Yb:** Unused
15:0	0h RO	**DMA_CH6_Yb:** DMA CH 6 PARAM 7: block Height (Yb)

3.7.474 reg_isp_dma_DMA_CH7_Yb_type (isp_dma_DMA_CH7_Yb)—Offset 4171Ch

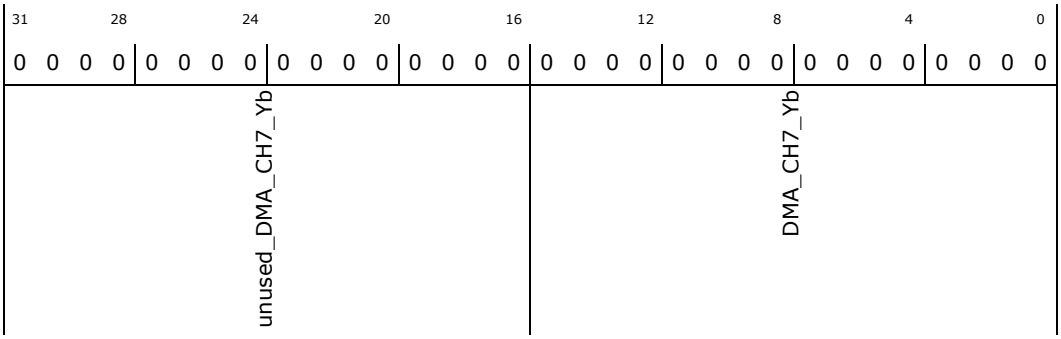
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_Yb: [ISPMMADR] + 4171Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH7_Yb:** Unused
15:0	0h RO	**DMA_CH7_Yb:** DMA CH 7 PARAM 7: block Height (Yb)

3.7.475 reg_isp_dma_DMA_CH8_Yb_type (isp_dma_DMA_CH8_Yb)—Offset 41720h

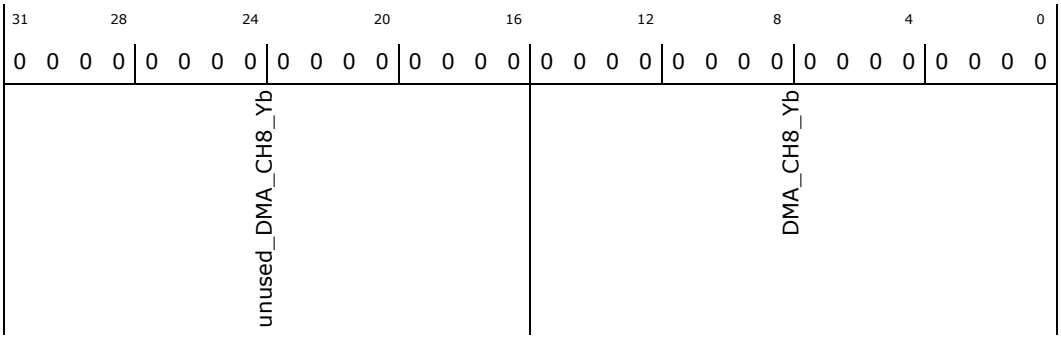
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_Yb: [ISPMMADR] + 41720h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH8_Yb:** Unused
15:0	0h RO	**DMA_CH8_Yb:** DMA CH 8 PARAM 7: block Height (Yb)

3.7.476 reg_isp_dma_DMA_CH9_Yb_type (isp_dma_DMA_CH9_Yb)—Offset 41724h

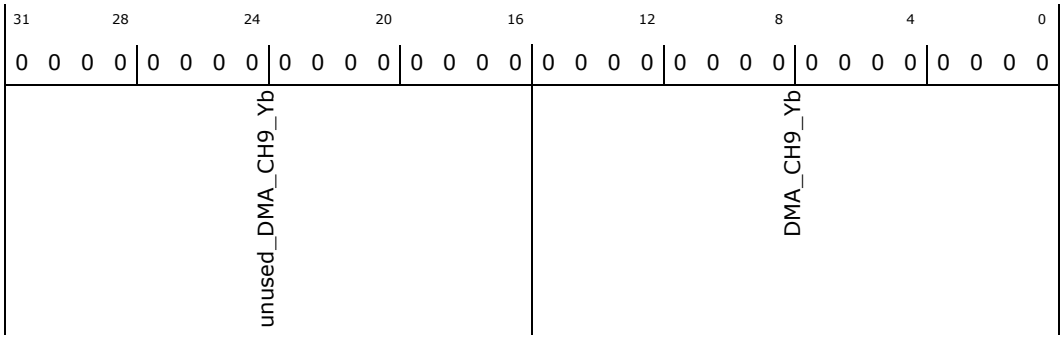
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_Yb: [ISPMMADR] + 41724h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH9_Yb:** Unused
15:0	0h RO	**DMA_CH9_Yb:** DMA CH 9 PARAM 7: block Height (Yb)

3.7.477 reg_isp_dma_DMA_CH10_Yb_type (isp_dma_DMA_CH10_Yb)—Offset 41728h

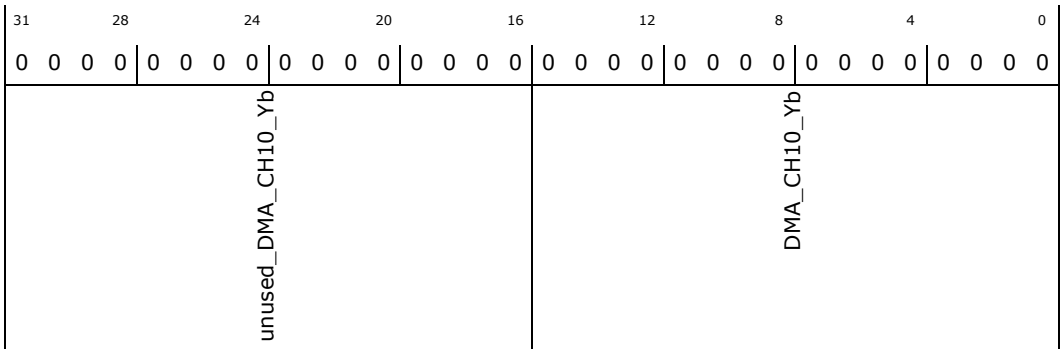
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_Yb: [ISPMMADR] + 41728h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH10_Yb:** Unused
15:0	0h RO	**DMA_CH10_Yb:** DMA CH 10 PARAM 7: block Height (Yb)

3.7.478 reg_isp_dma_DMA_CH11_Yb_type (isp_dma_DMA_CH11_Yb)—Offset 4172Ch

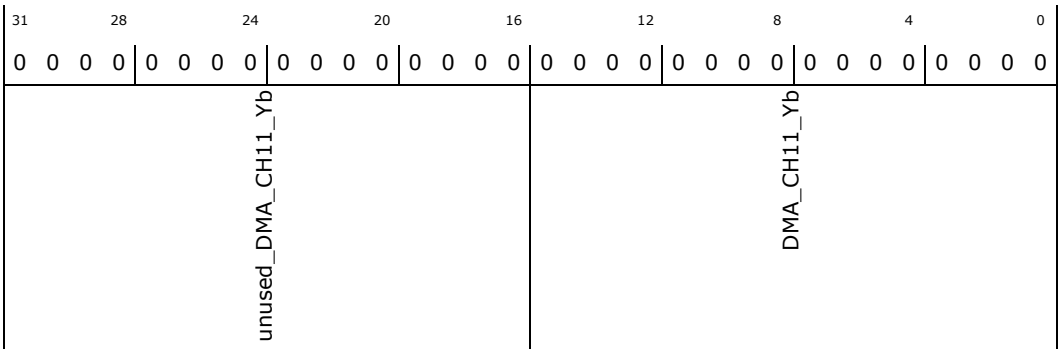
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_Yb: [ISPMMADR] + 4172Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH11_Yb:** Unused
15:0	0h RO	**DMA_CH11_Yb:** DMA CH 11 PARAM 7: block Height (Yb)

3.7.479 reg_isp_dma_DMA_CH12_Yb_type (isp_dma_DMA_CH12_Yb)—Offset 41730h

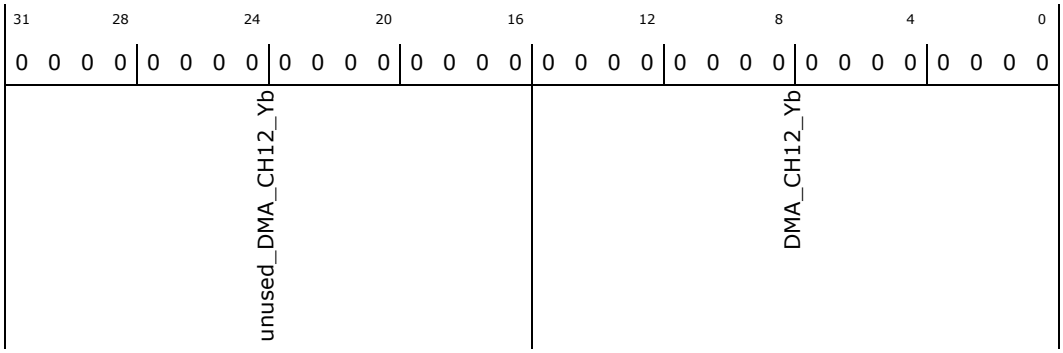
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_Yb: [ISPMMADR] + 41730h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH12_Yb:** Unused
15:0	0h RO	**DMA_CH12_Yb:** DMA CH 12 PARAM 7: block Height (Yb)

3.7.480 reg_isp_dma_DMA_CH13_Yb_type (isp_dma_DMA_CH13_Yb)—Offset 41734h

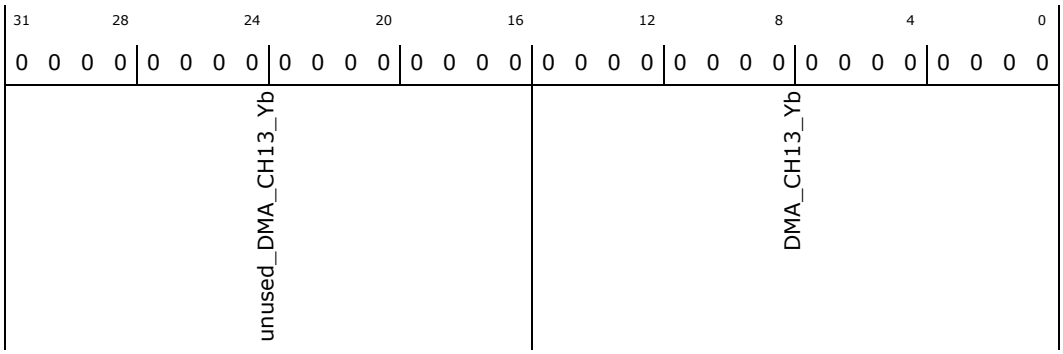
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_Yb: [ISPMMADR] + 41734h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH13_Yb:** Unused
15:0	0h RO	**DMA_CH13_Yb:** DMA CH 13 PARAM 7: block Height (Yb)

3.7.481 reg_isp_dma_DMA_CH14_Yb_type (isp_dma_DMA_CH14_Yb)—Offset 41738h

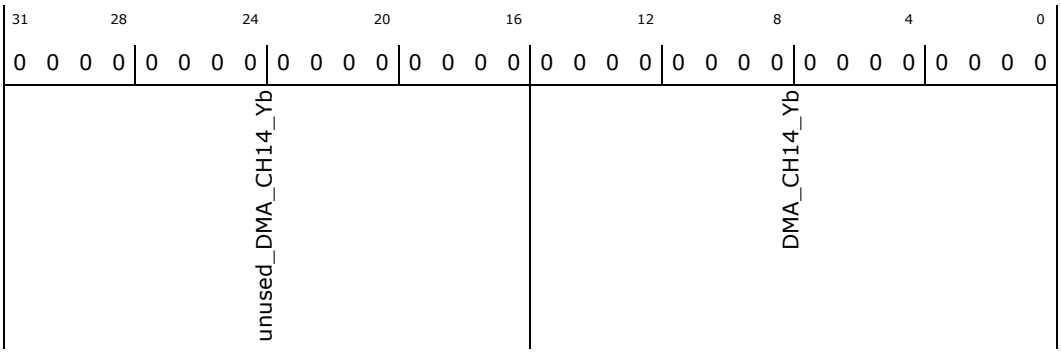
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_Yb: [ISPMMADR] + 41738h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH14_Yb:** Unused
15:0	0h RO	**DMA_CH14_Yb:** DMA CH 14 PARAM 7: block Height (Yb)

3.7.482 reg_isp_dma_DMA_CH15_Yb_type (isp_dma_DMA_CH15_Yb)—Offset 4173Ch

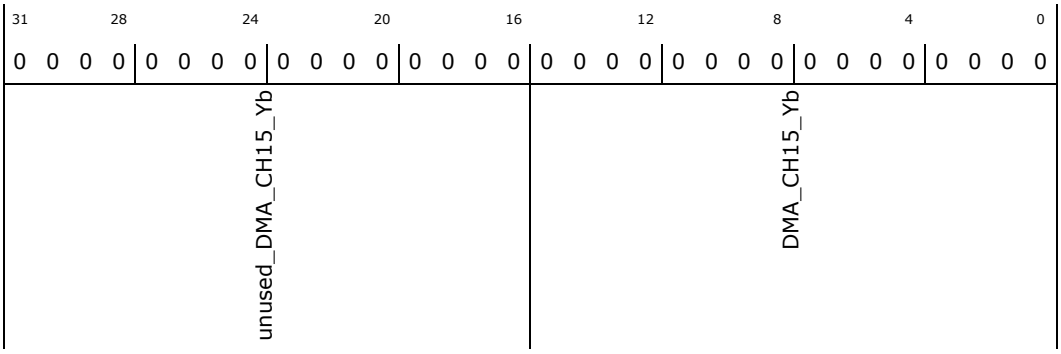
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_Yb: [ISPMMADR] + 4173Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH15_Yb:** Unused
15:0	0h RO	**DMA_CH15_Yb:** DMA CH 15 PARAM 7: block Height (Yb)

3.7.483 reg_isp_dma_DMA_CH16_Yb_type (isp_dma_DMA_CH16_Yb)—Offset 41740h

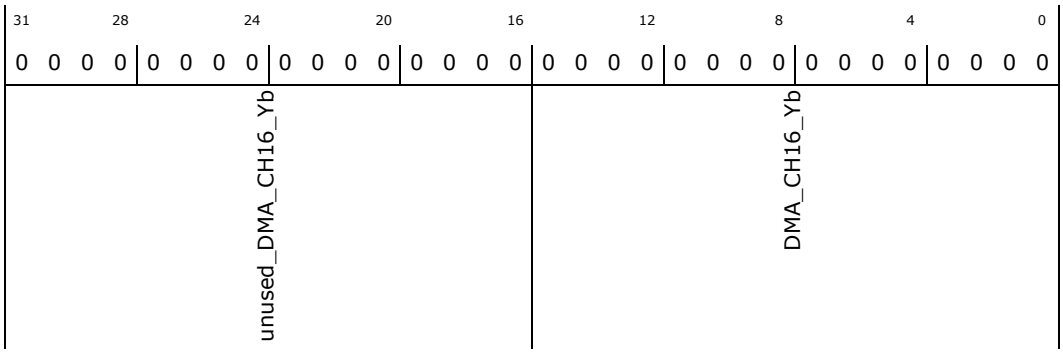
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_Yb: [ISPMMADR] + 41740h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH16_Yb:** Unused
15:0	0h RO	**DMA_CH16_Yb:** DMA CH 16 PARAM 7: block Height (Yb)

3.7.484 reg_isp_dma_DMA_CH17_Yb_type (isp_dma_DMA_CH17_Yb)—Offset 41744h

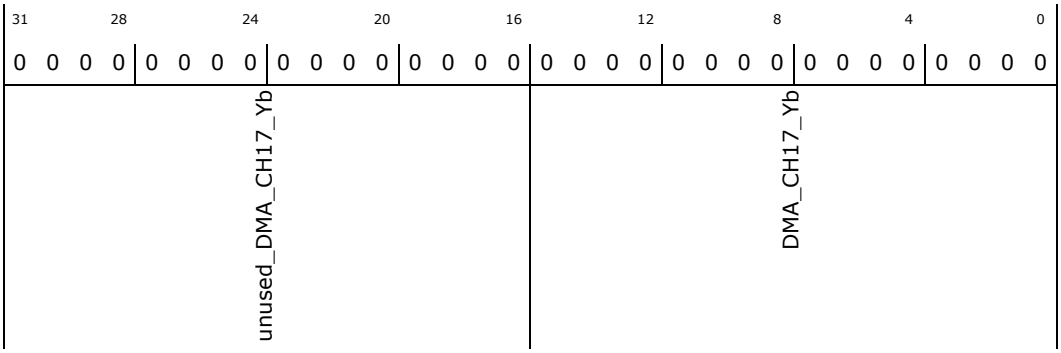
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_Yb: [ISPMMADR] + 41744h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH17_Yb:** Unused
15:0	0h RO	**DMA_CH17_Yb:** DMA CH 17 PARAM 7: block Height (Yb)

3.7.485 reg_isp_dma_DMA_CH18_Yb_type (isp_dma_DMA_CH18_Yb)—Offset 41748h

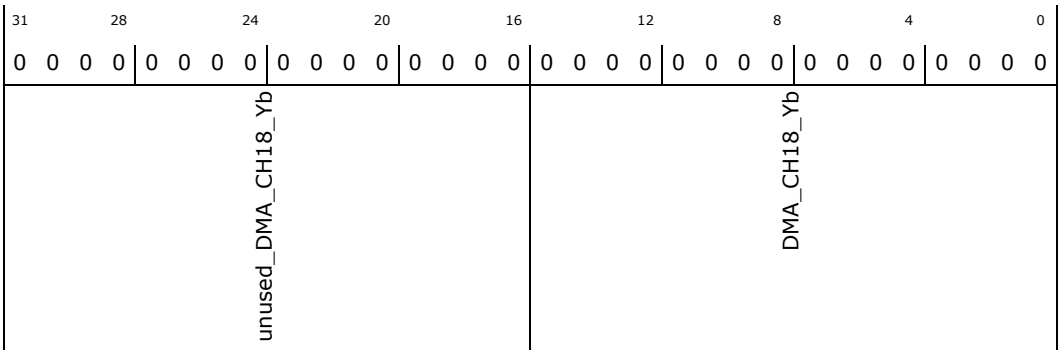
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_Yb: [ISPMMADR] + 41748h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH18_Yb:** Unused
15:0	0h RO	**DMA_CH18_Yb:** DMA CH 18 PARAM 7: block Height (Yb)

3.7.486 reg_isp_dma_DMA_CH19_Yb_type (isp_dma_DMA_CH19_Yb)—Offset 4174Ch

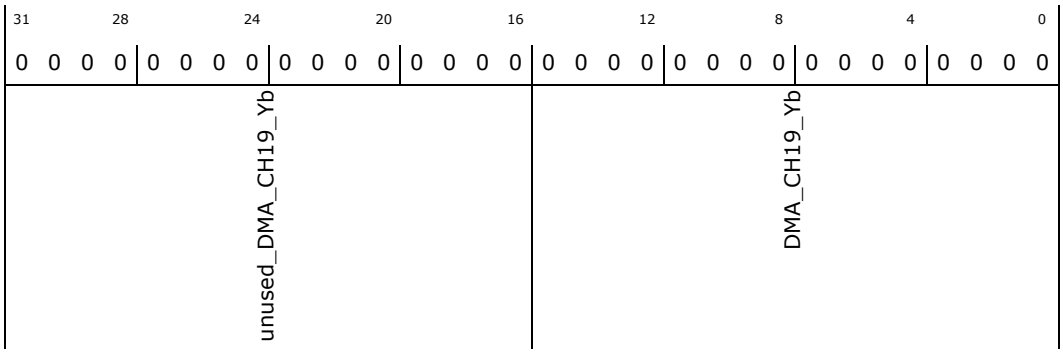
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_Yb: [ISPMMADR] + 4174Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH19_Yb:** Unused
15:0	0h RO	**DMA_CH19_Yb:** DMA CH 19 PARAM 7: block Height (Yb)

3.7.487 reg_isp_dma_DMA_CH20_Yb_type (isp_dma_DMA_CH20_Yb)—Offset 41750h

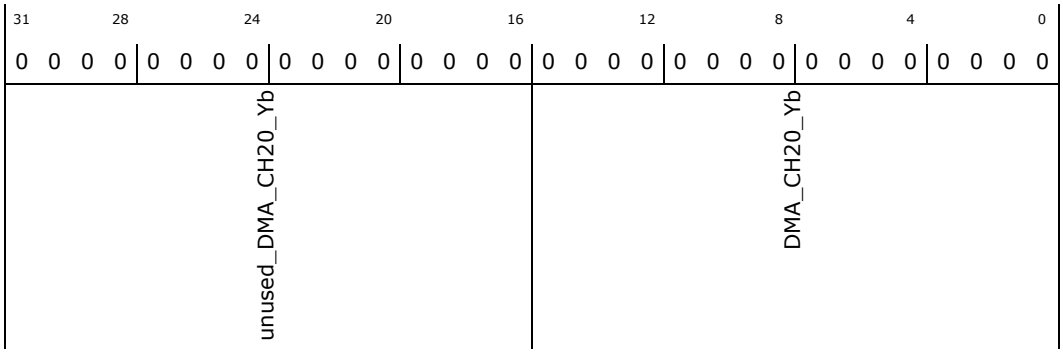
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_Yb: [ISPMMADR] + 41750h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH20_Yb:** Unused
15:0	0h RO	**DMA_CH20_Yb:** DMA CH 20 PARAM 7: block Height (Yb)

3.7.488 reg_isp_dma_DMA_CH21_Yb_type (isp_dma_DMA_CH21_Yb)—Offset 41754h

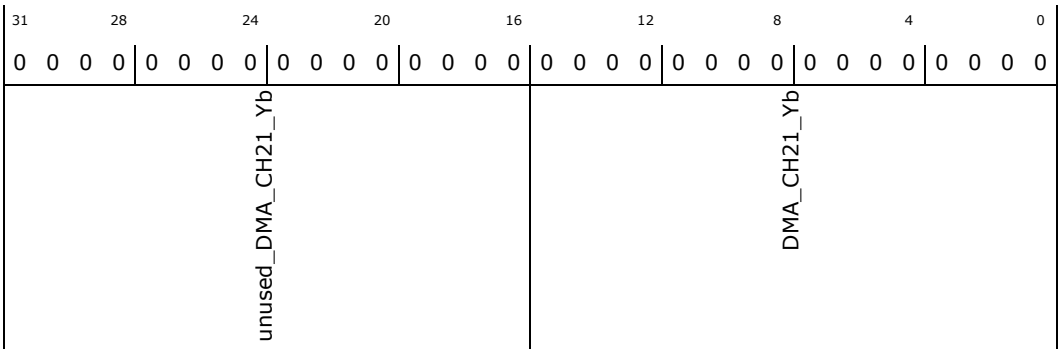
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_Yb: [ISPMMADR] + 41754h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH21_Yb:** Unused
15:0	0h RO	**DMA_CH21_Yb:** DMA CH 21 PARAM 7: block Height (Yb)

3.7.489 reg_isp_dma_DMA_CH22_Yb_type (isp_dma_DMA_CH22_Yb)—Offset 41758h

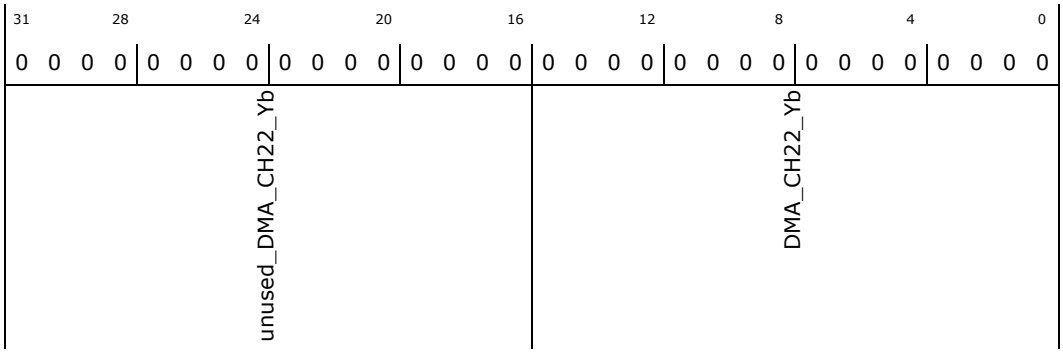
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_Yb: [ISPMMADR] + 41758h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH22_Yb:** Unused
15:0	0h RO	**DMA_CH22_Yb:** DMA CH 22 PARAM 7: block Height (Yb)

3.7.490 reg_isp_dma_DMA_CH23_Yb_type (isp_dma_DMA_CH23_Yb)—Offset 4175Ch

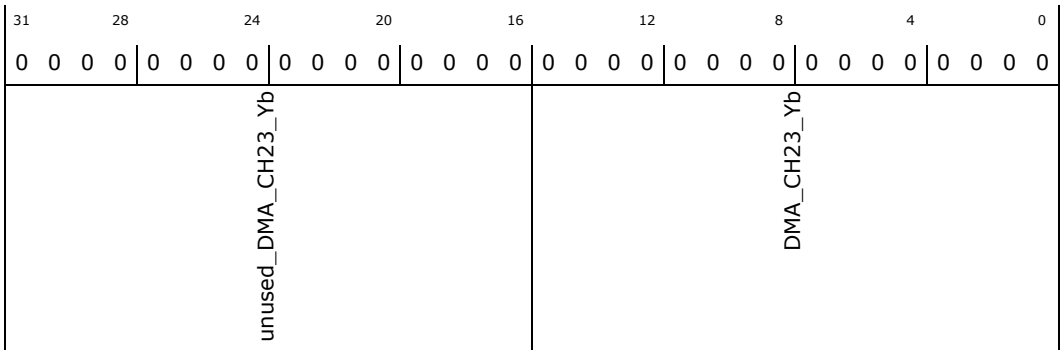
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_Yb: [ISPMMADR] + 4175Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH23_Yb:** Unused
15:0	0h RO	**DMA_CH23_Yb:** DMA CH 23 PARAM 7: block Height (Yb)

3.7.491 reg_isp_dma_DMA_CH24_Yb_type (isp_dma_DMA_CH24_Yb)—Offset 41760h

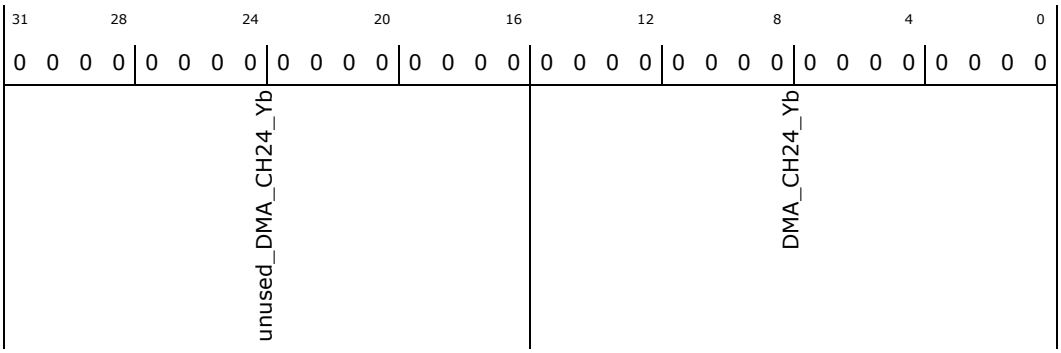
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_Yb: [ISPMMADR] + 41760h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH24_Yb:** Unused
15:0	0h RO	**DMA_CH24_Yb:** DMA CH 24 PARAM 7: block Height (Yb)

3.7.492 reg_isp_dma_DMA_CH25_Yb_type (isp_dma_DMA_CH25_Yb)—Offset 41764h

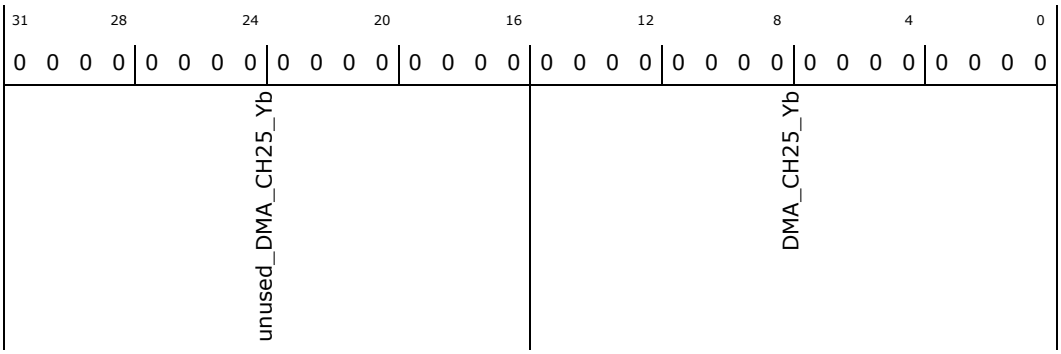
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_Yb: [ISPMMADR] + 41764h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH25_Yb:** Unused
15:0	0h RO	**DMA_CH25_Yb:** DMA CH 25 PARAM 7: block Height (Yb)

3.7.493 reg_isp_dma_DMA_CH26_Yb_type (isp_dma_DMA_CH26_Yb)—Offset 41768h

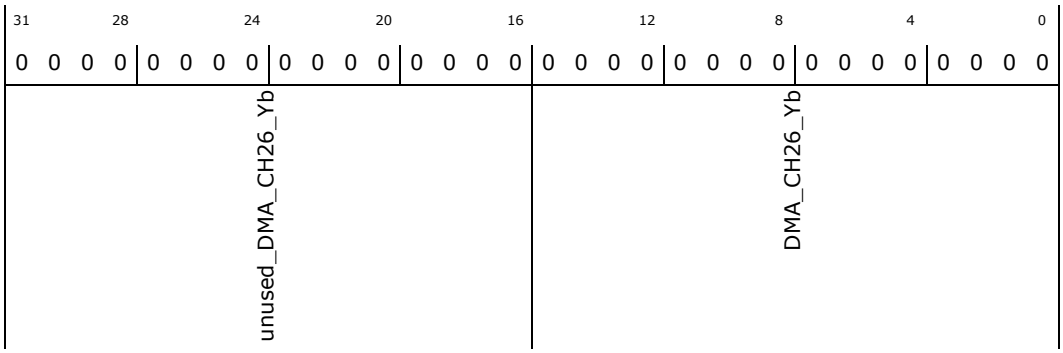
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_Yb: [ISPMMADR] + 41768h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH26_Yb:** Unused
15:0	0h RO	**DMA_CH26_Yb:** DMA CH 26 PARAM 7: block Height (Yb)

3.7.494 reg_isp_dma_DMA_CH27_Yb_type (isp_dma_DMA_CH27_Yb)—Offset 4176Ch

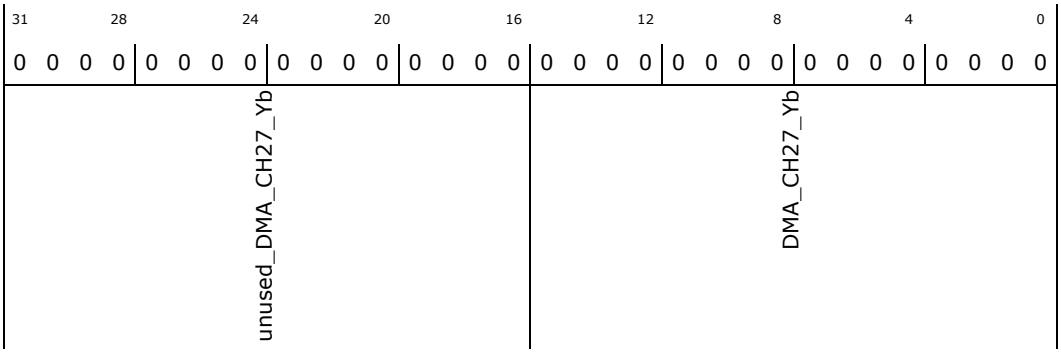
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_Yb: [ISPMMADR] + 4176Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH27_Yb:** Unused
15:0	0h RO	**DMA_CH27_Yb:** DMA CH 27 PARAM 7: block Height (Yb)

3.7.495 reg_isp_dma_DMA_CH28_Yb_type (isp_dma_DMA_CH28_Yb)—Offset 41770h

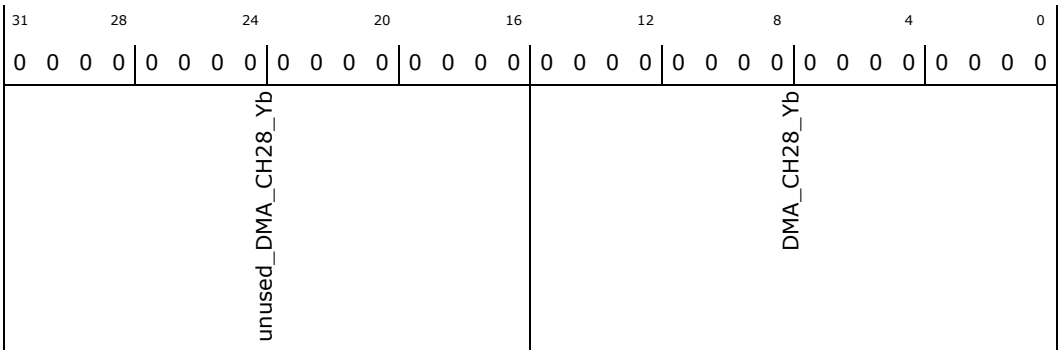
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_Yb: [ISPMMADR] + 41770h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH28_Yb:** Unused
15:0	0h RO	**DMA_CH28_Yb:** DMA CH 28 PARAM 7: block Height (Yb)

3.7.496 reg_isp_dma_DMA_CH29_Yb_type (isp_dma_DMA_CH29_Yb)—Offset 41774h

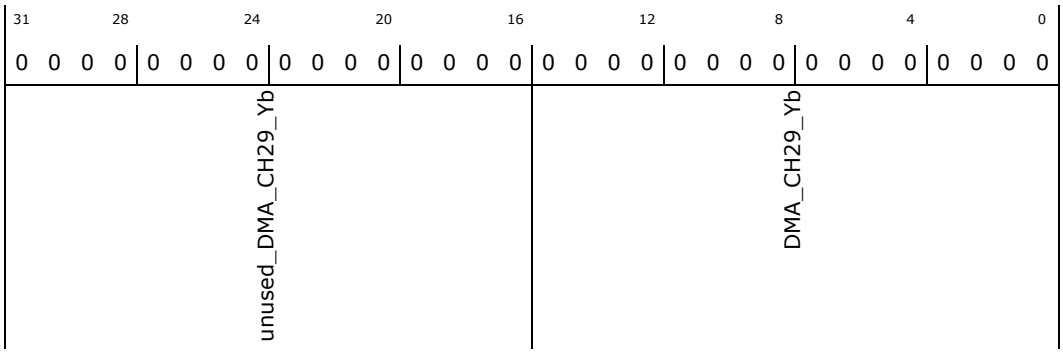
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_Yb: [ISPMMADR] + 41774h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH29_Yb:** Unused
15:0	0h RO	**DMA_CH29_Yb:** DMA CH 29 PARAM 7: block Height (Yb)

3.7.497 reg_isp_dma_DMA_CH31_Yb_type (isp_dma_DMA_CH31_Yb)—Offset 4177Ch

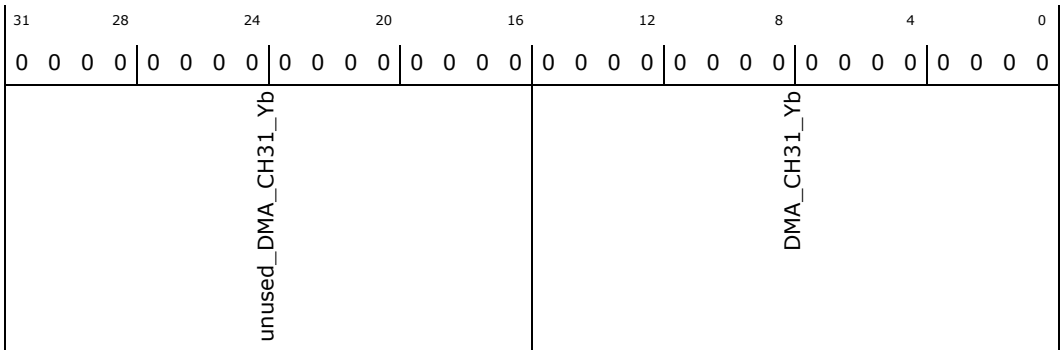
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_Yb: [ISPMMADR] + 4177Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH31_Yb:** Unused
15:0	0h RO	**DMA_CH31_Yb:** DMA CH 31 PARAM 7: block Height (Yb)

3.7.498 reg_isp_dma_DMA_CH0_pending_command_type (isp_dma_DMA_CH0_pending_command)—Offset 41800h

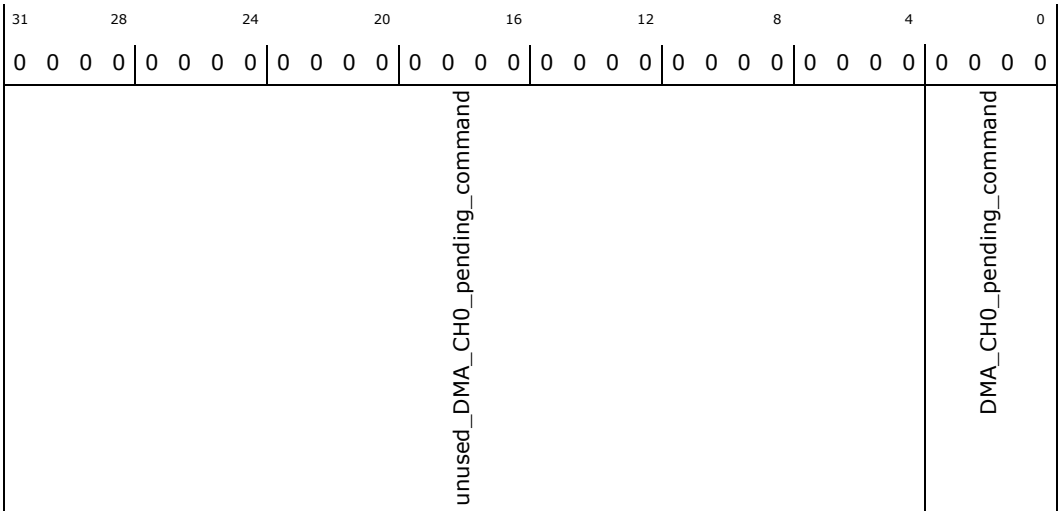
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_pending_command: [ISPMMADR] + 41800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH0_pending_command:** Unused
3:0	0h RO	**DMA_CH0_pending_command:** DMA CH 0 PARAM 8: Pending commands which will use channel 0

3.7.499 reg_isp_dma_DMA_CH1_pending_command_type (isp_dma_DMA_CH1_pending_command)—Offset 41804h

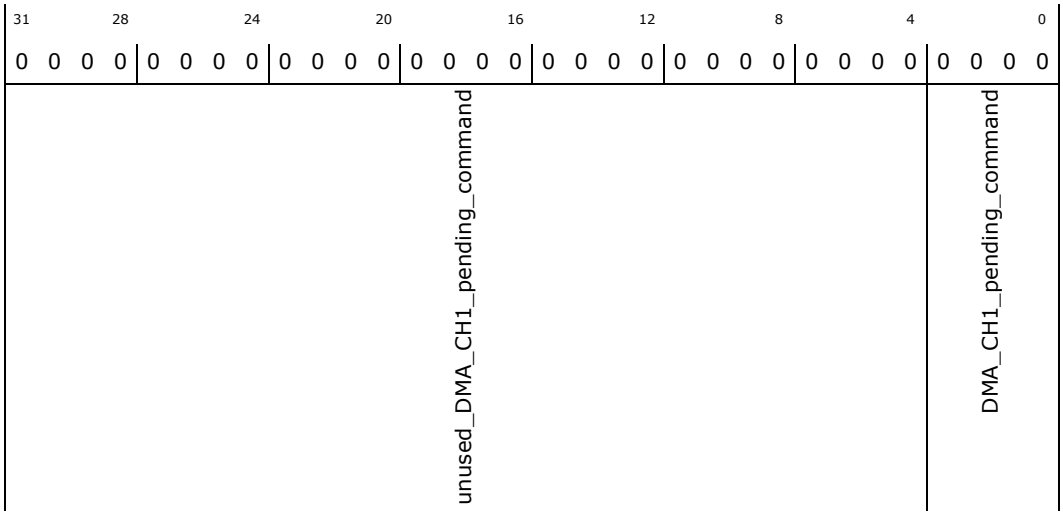
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_pending_command: [ISPMMADR] + 41804h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH1_pending_command:** Unused
3:0	0h RO	**DMA_CH1_pending_command:** DMA CH 1 PARAM 8: Pending commands which will use channel 1

3.7.500 reg_isp_dma_DMA_CH2_pending_command_type (isp_dma_DMA_CH2_pending_command)—Offset 41808h

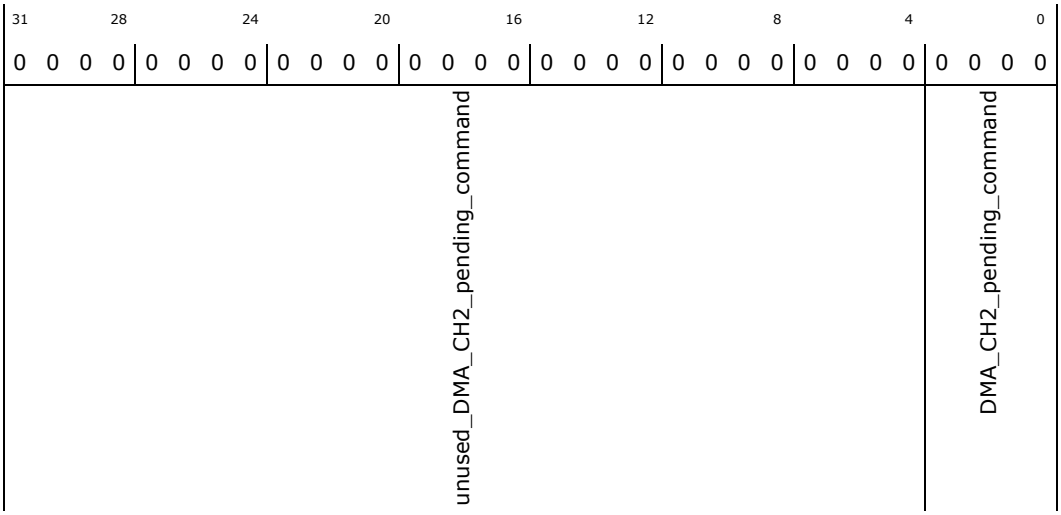
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_pending_command: [ISPMMADR] + 41808h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH2_pending_command:** Unused
3:0	0h RO	**DMA_CH2_pending_command:** DMA CH 2 PARAM 8: Pending commands which will use channel 2

3.7.501 reg_isp_dma_DMA_CH3_pending_command_type (isp_dma_DMA_CH3_pending_command)—Offset 4180Ch

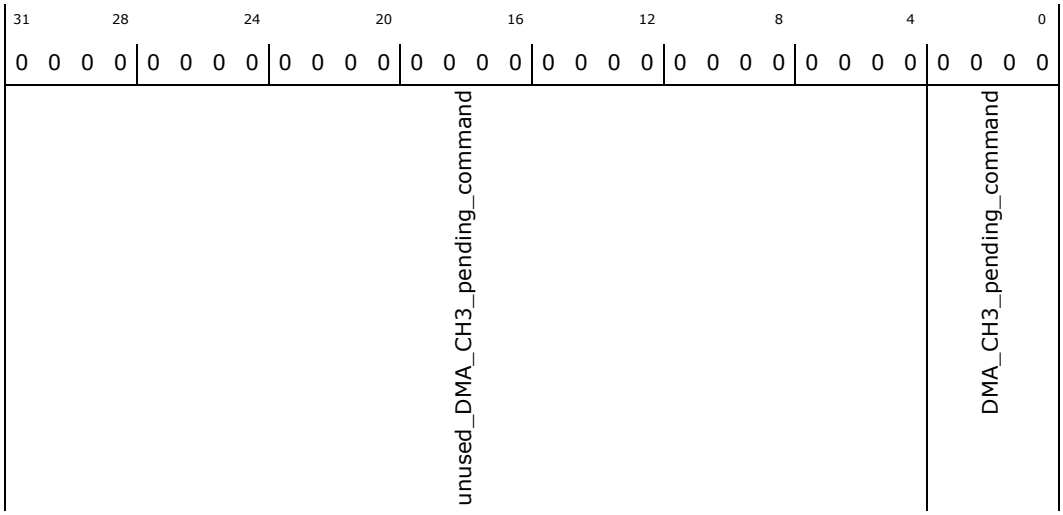
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_pending_command: [ISPMMADR] + 4180Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH3_pending_command:** Unused
3:0	0h RO	**DMA_CH3_pending_command:** DMA CH 0 PARAM 8: Pending commands which will use channel 3

3.7.502 reg_isp_dma_DMA_CH4_pending_command_type (isp_dma_DMA_CH4_pending_command)—Offset 41810h

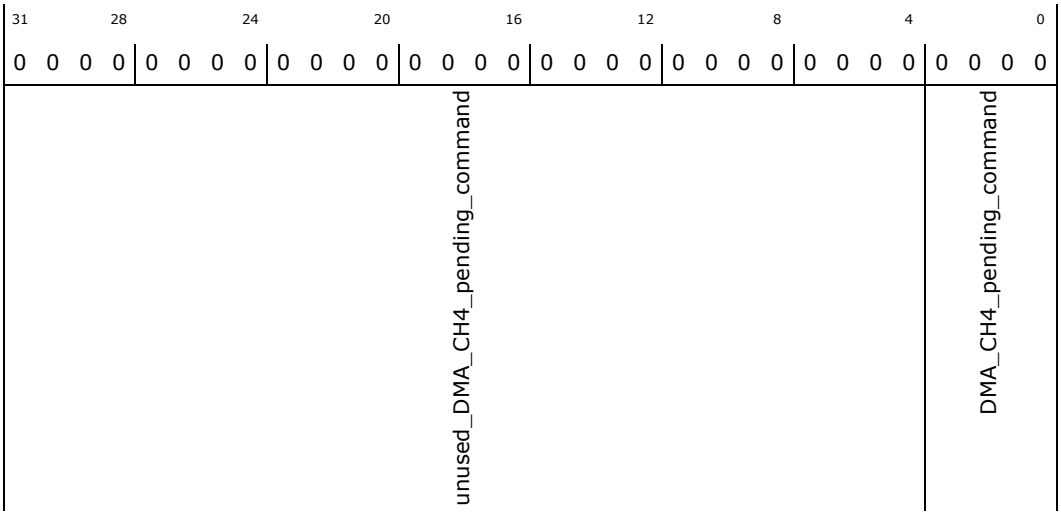
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_pending_command: [ISPMMADR] + 41810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH4_pending_command:** Unused
3:0	0h RO	**DMA_CH4_pending_command:** DMA CH 4 PARAM 8: Pending commands which will use channel 4

3.7.503 reg_isp_dma_DMA_CH5_pending_command_type (isp_dma_DMA_CH5_pending_command)—Offset 41814h

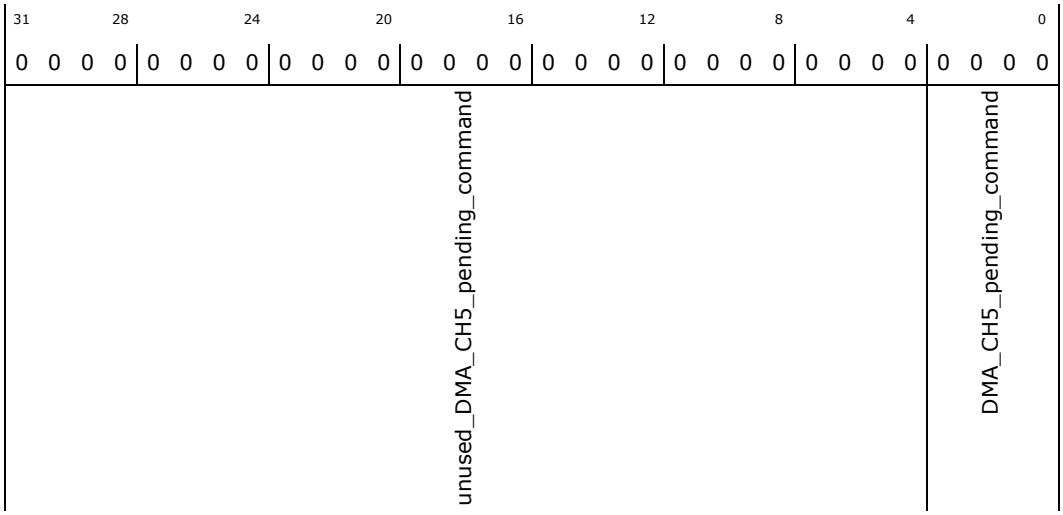
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_pending_command: [ISPMMADR] + 41814h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH5_pending_command:** Unused
3:0	0h RO	**DMA_CH5_pending_command:** DMA CH 5 PARAM 8: Pending commands which will use channel 5

3.7.504 reg_isp_dma_DMA_CH6_pending_command_type (isp_dma_DMA_CH6_pending_command)—Offset 41818h

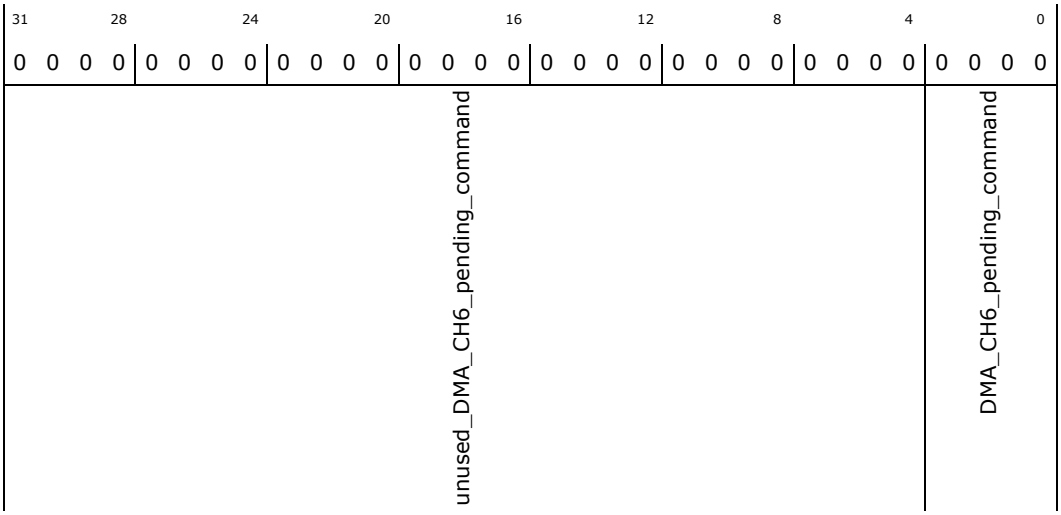
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_pending_command: [ISPMMADR] + 41818h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH6_pending_command:** Unused
3:0	0h RO	**DMA_CH6_pending_command:** DMA CH 6 PARAM 8: Pending commands which will use channel 6

3.7.505 reg_isp_dma_DMA_CH7_pending_command_type (isp_dma_DMA_CH7_pending_command)—Offset 4181Ch

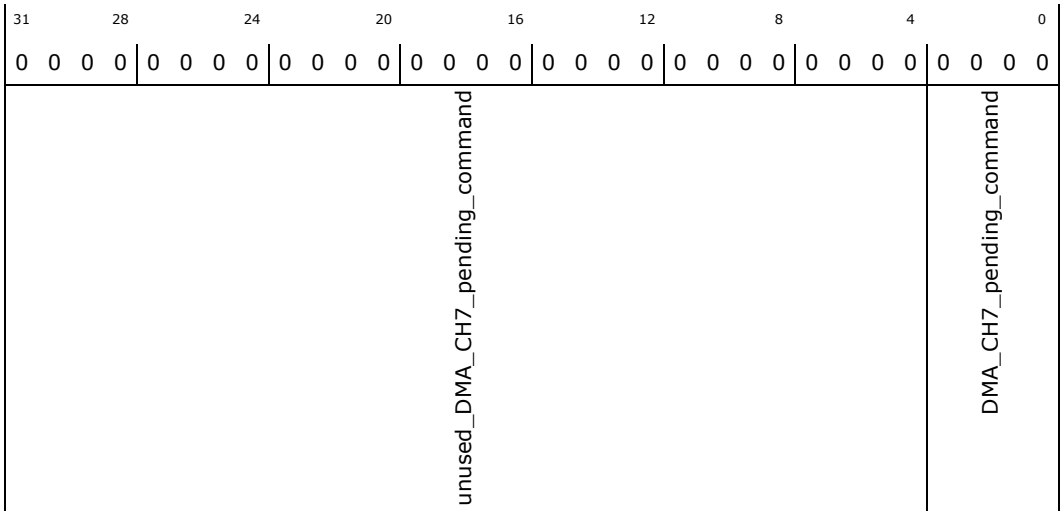
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_pending_command: [ISPMMADR] + 4181Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH7_pending_command:** Unused
3:0	0h RO	**DMA_CH7_pending_command:** DMA CH 7 PARAM 8: Pending commands which will use channel 7

3.7.506 reg_isp_dma_DMA_CH8_pending_command_type (isp_dma_DMA_CH8_pending_command)—Offset 41820h

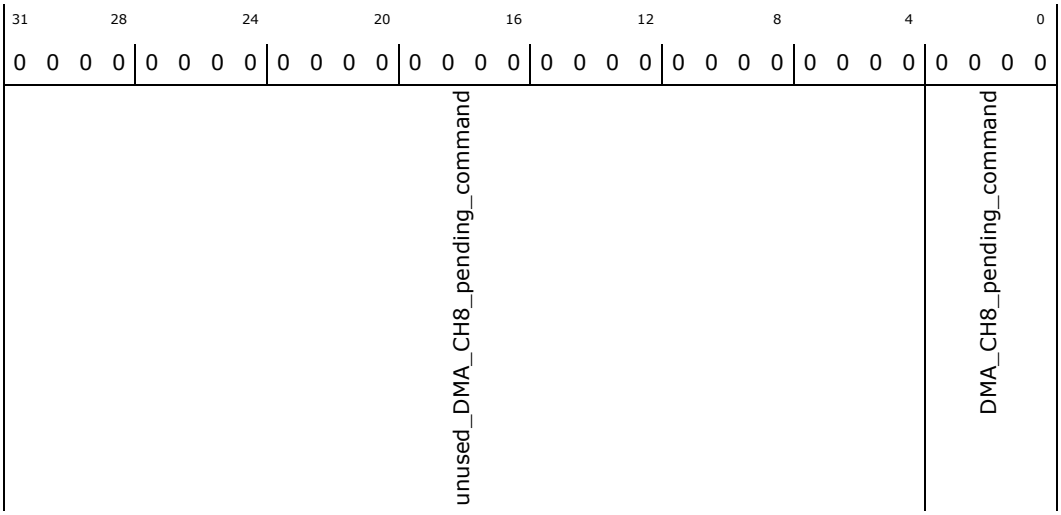
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_pending_command: [ISPMMADR] + 41820h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH8_pending_command:** Unused
3:0	0h RO	**DMA_CH8_pending_command:** DMA CH 8 PARAM 8: Pending commands which will use channel 6

3.7.507 reg_isp_dma_DMA_CH9_pending_command_type (isp_dma_DMA_CH9_pending_command)—Offset 41824h

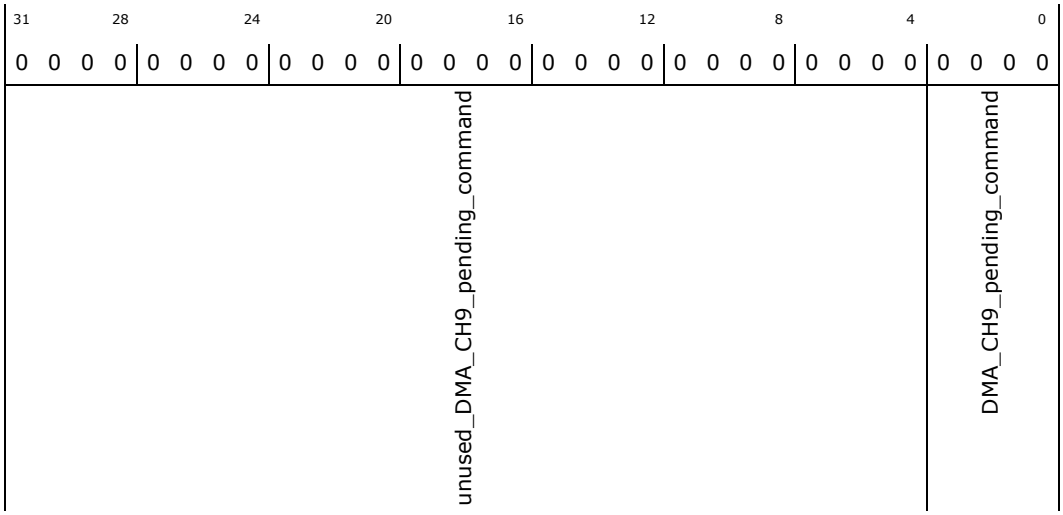
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_pending_command: [ISPMMADR] + 41824h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH9_pending_command:** Unused
3:0	0h RO	**DMA_CH9_pending_command:** DMA CH 9 PARAM 8: Pending commands which will use channel 7

3.7.508 reg_isp_dma_DMA_CH10_pending_command_type (isp_dma_DMA_CH10_pending_command)—Offset 41828h

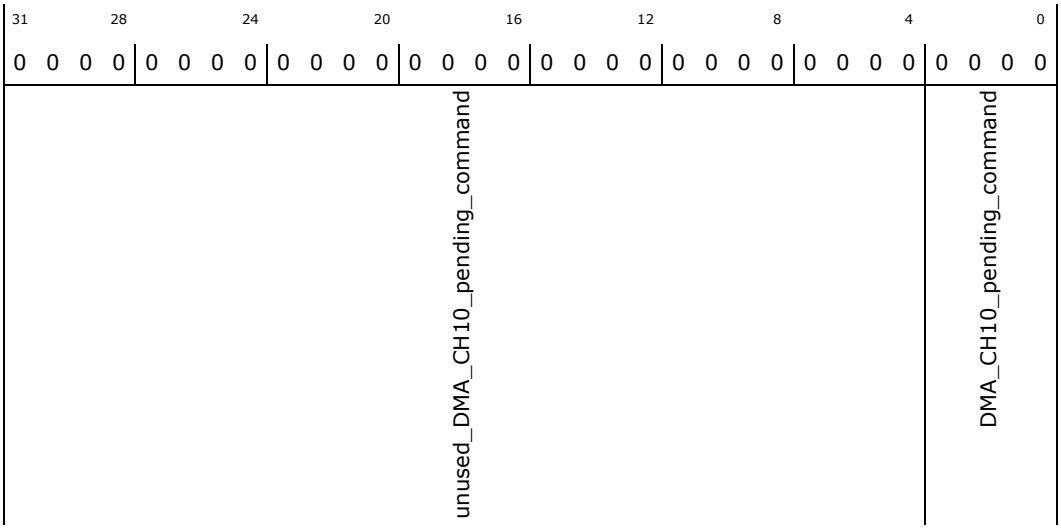
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_pending_command: [ISPMMADR] + 41828h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH10_pending_command:** Unused
3:0	0h RO	**DMA_CH10_pending_command:** DMA CH 10 PARAM 8: Pending commands which will use channel 0

3.7.509 reg_isp_dma_DMA_CH11_pending_command_type (isp_dma_DMA_CH11_pending_command)—Offset 4182Ch

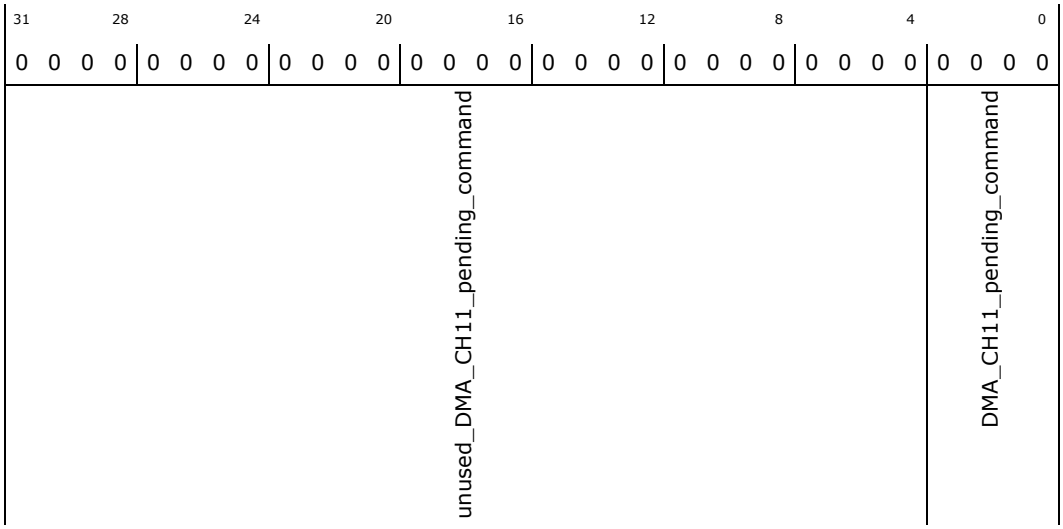
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_pending_command: [ISPMMADR] + 4182Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH11_pending_command:** Unused
3:0	0h RO	**DMA_CH11_pending_command:** DMA CH 11 PARAM 8: Pending commands which will use channel 1

3.7.510 reg_isp_dma_DMA_CH12_pending_command_type (isp_dma_DMA_CH12_pending_command)—Offset 41830h

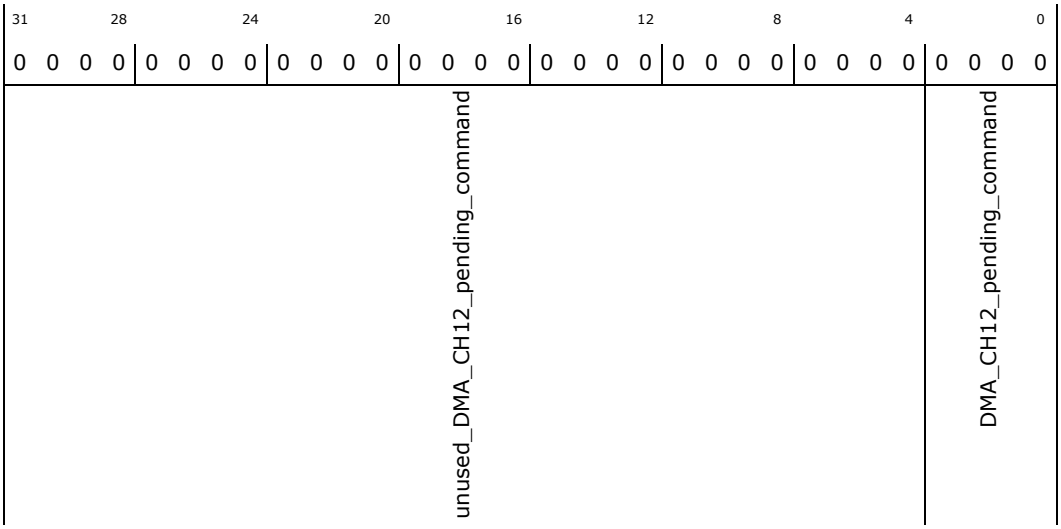
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_pending_command: [ISPMMADR] + 41830h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH12_pending_command:** Unused
3:0	0h RO	**DMA_CH12_pending_command:** DMA CH 12 PARAM 8: Pending commands which will use channel 2

3.7.511 reg_isp_dma_DMA_CH13_pending_command_type (isp_dma_DMA_CH13_pending_command)—Offset 41834h

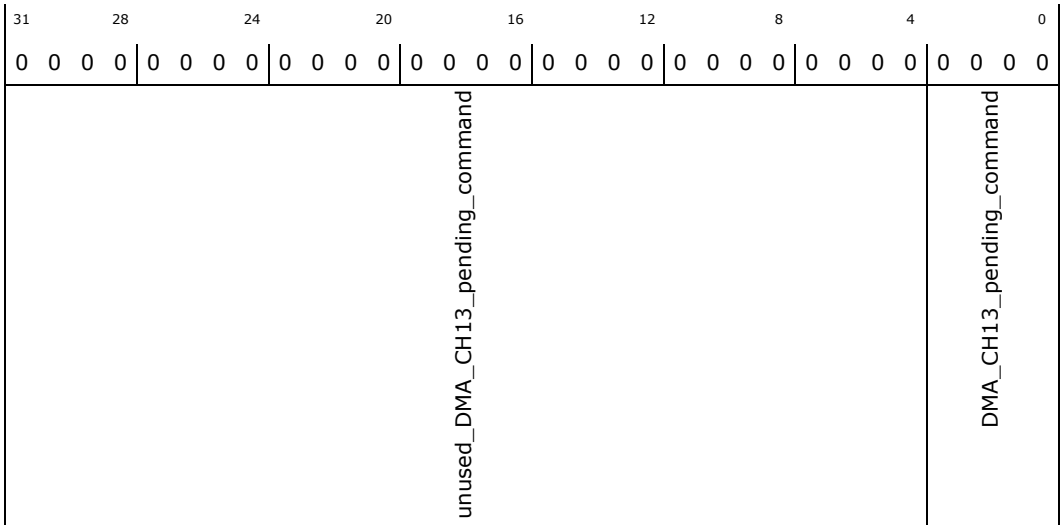
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_pending_command: [ISPMMADR] + 41834h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH13_pending_command:** Unused
3:0	0h RO	**DMA_CH13_pending_command:** DMA CH 10 PARAM 8: Pending commands which will use channel 3

3.7.512 reg_isp_dma_DMA_CH14_pending_command_type (isp_dma_DMA_CH14_pending_command)—Offset 41838h

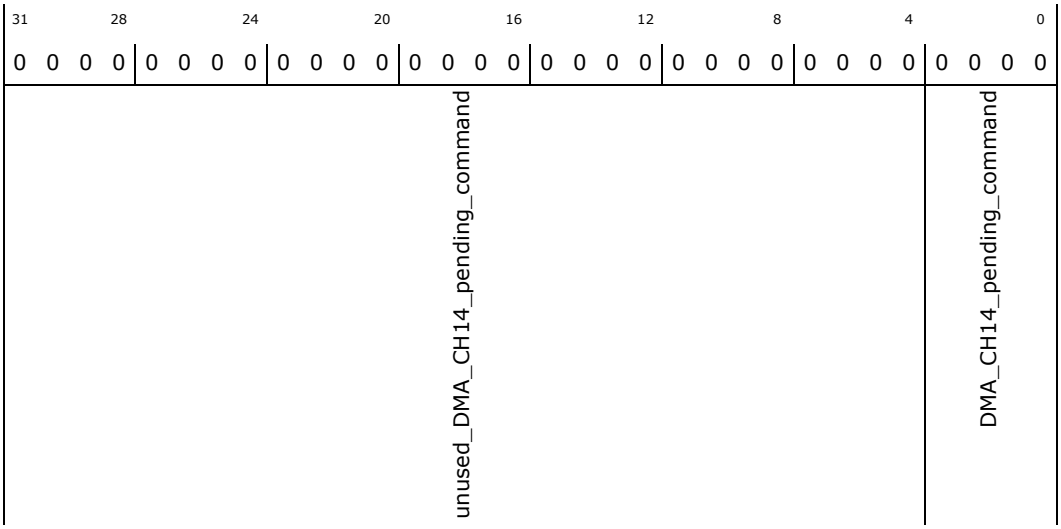
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_pending_command: [ISPMMADR] + 41838h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH14_pending_command:** Unused
3:0	0h RO	**DMA_CH14_pending_command:** DMA CH 14 PARAM 8: Pending commands which will use channel 4

3.7.513 reg_isp_dma_DMA_CH15_pending_command_type (isp_dma_DMA_CH15_pending_command)—Offset 4183Ch

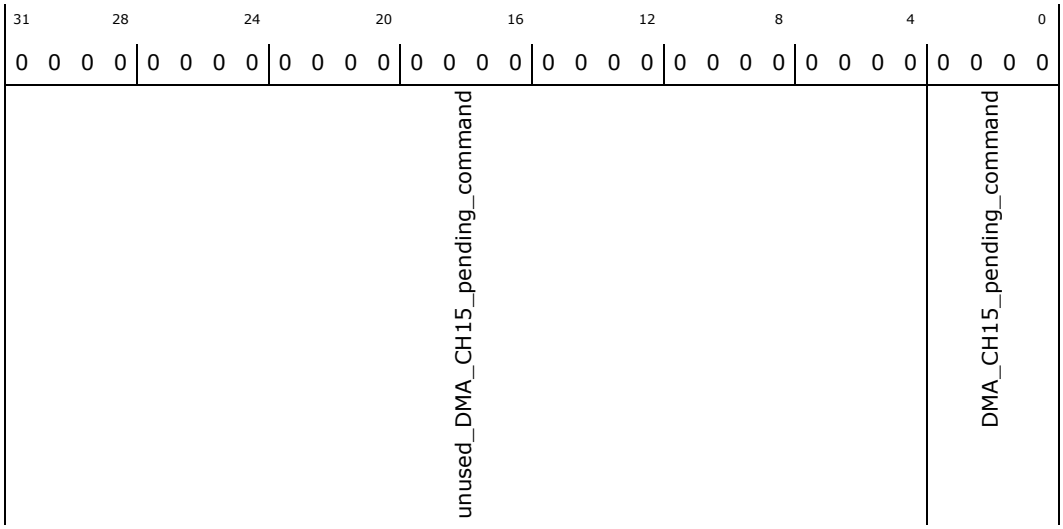
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_pending_command: [ISPMMADR] + 4183Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH15_pending_command:** Unused
3:0	0h RO	**DMA_CH15_pending_command:** DMA CH 15 PARAM 8: Pending commands which will use channel 5

3.7.514 reg_isp_dma_DMA_CH16_pending_command_type (isp_dma_DMA_CH16_pending_command)—Offset 41840h

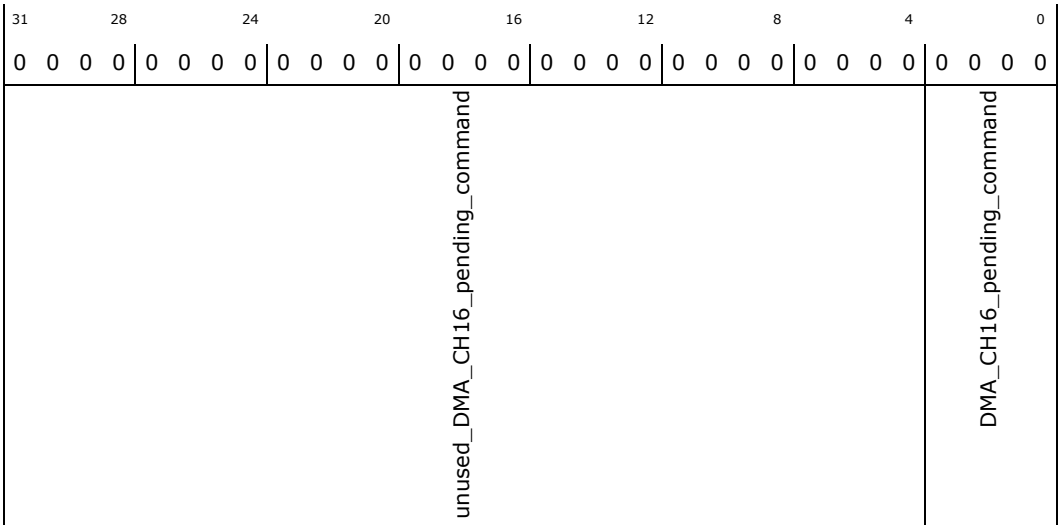
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_pending_command: [ISPMMADR] + 41840h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH16_pending_command:** Unused
3:0	0h RO	**DMA_CH16_pending_command:** DMA CH 16 PARAM 8: Pending commands which will use channel 6

3.7.515 reg_isp_dma_DMA_CH17_pending_command_type (isp_dma_DMA_CH17_pending_command)—Offset 41844h

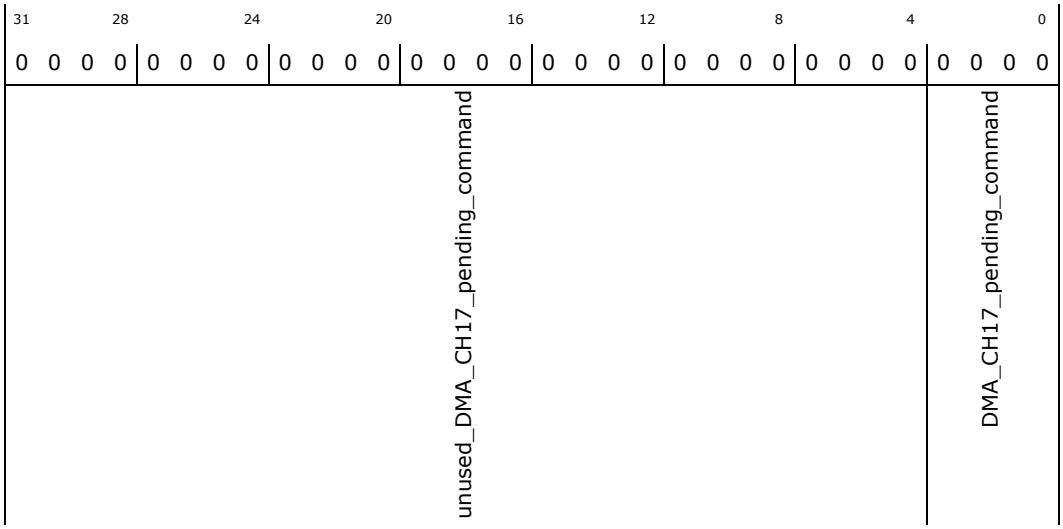
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_pending_command: [ISPMMADR] + 41844h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH17_pending_command:** Unused
3:0	0h RO	**DMA_CH17_pending_command:** DMA CH 17 PARAM 8: Pending commands which will use channel 7

3.7.516 reg_isp_dma_DMA_CH18_pending_command_type (isp_dma_DMA_CH18_pending_command)—Offset 41848h

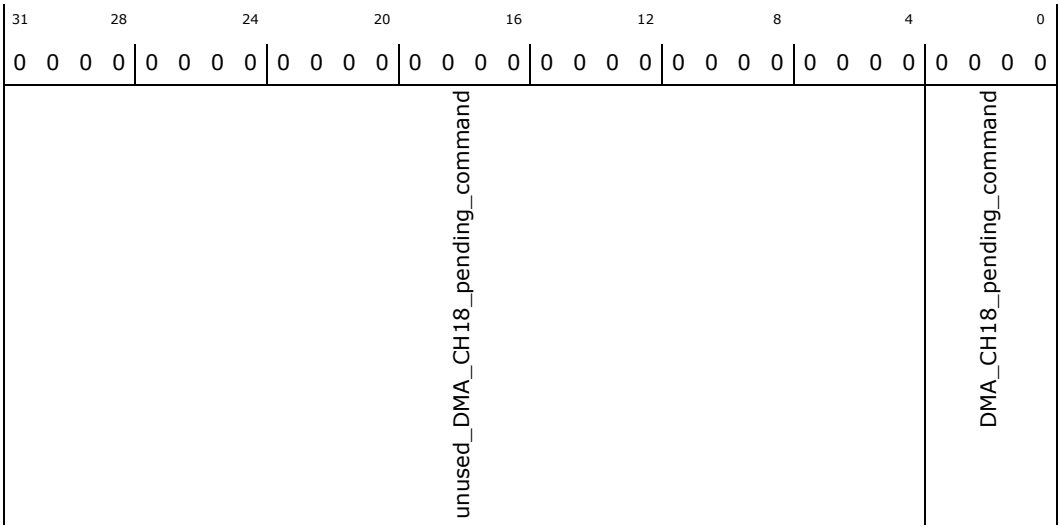
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_pending_command: [ISPMMADR] + 41848h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH18_pending_command:** Unused
3:0	0h RO	**DMA_CH18_pending_command:** DMA CH 18 PARAM 8: Pending commands which will use channel 6

3.7.517 reg_isp_dma_DMA_CH19_pending_command_type (isp_dma_DMA_CH19_pending_command)—Offset 4184Ch

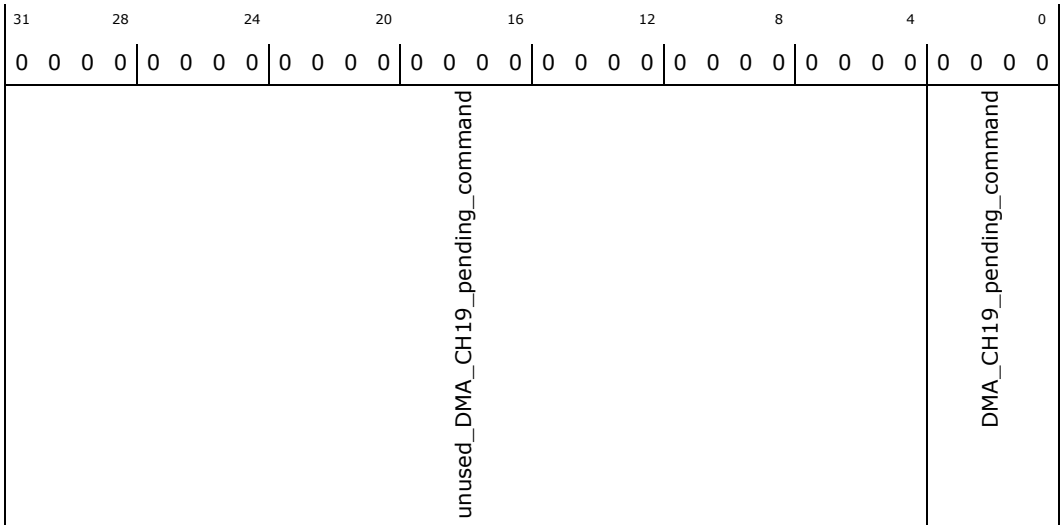
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_pending_command: [ISPMMADR] + 4184Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH19_pending_command:** Unused
3:0	0h RO	**DMA_CH19_pending_command:** DMA CH 19 PARAM 8: Pending commands which will use channel 7

3.7.518 reg_isp_dma_DMA_CH20_pending_command_type (isp_dma_DMA_CH20_pending_command)—Offset 41850h

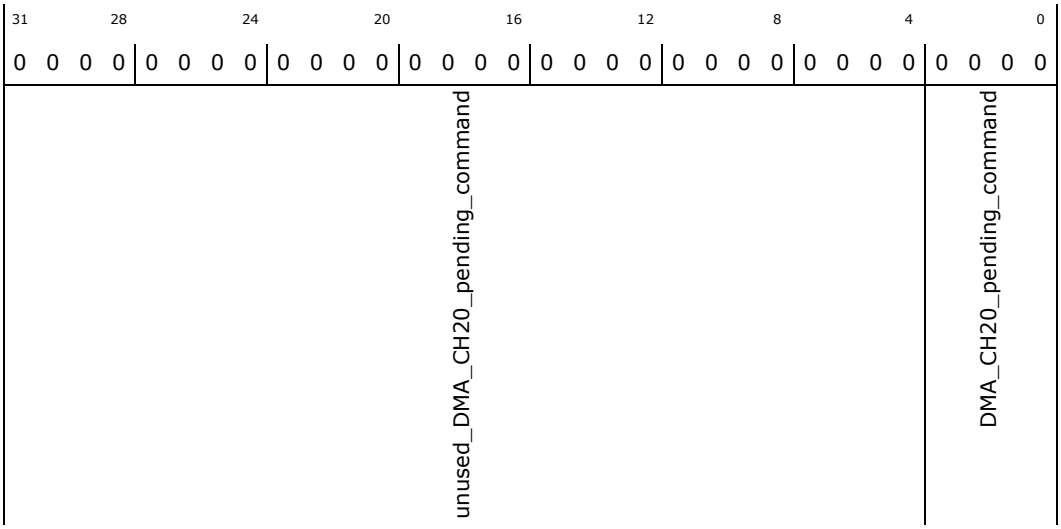
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_pending_command: [ISPMMADR] + 41850h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH20_pending_command:** Unused
3:0	0h RO	**DMA_CH20_pending_command:** DMA CH 20 PARAM 8: Pending commands which will use channel 0

3.7.519 reg_isp_dma_DMA_CH21_pending_command_type (isp_dma_DMA_CH21_pending_command)—Offset 41854h

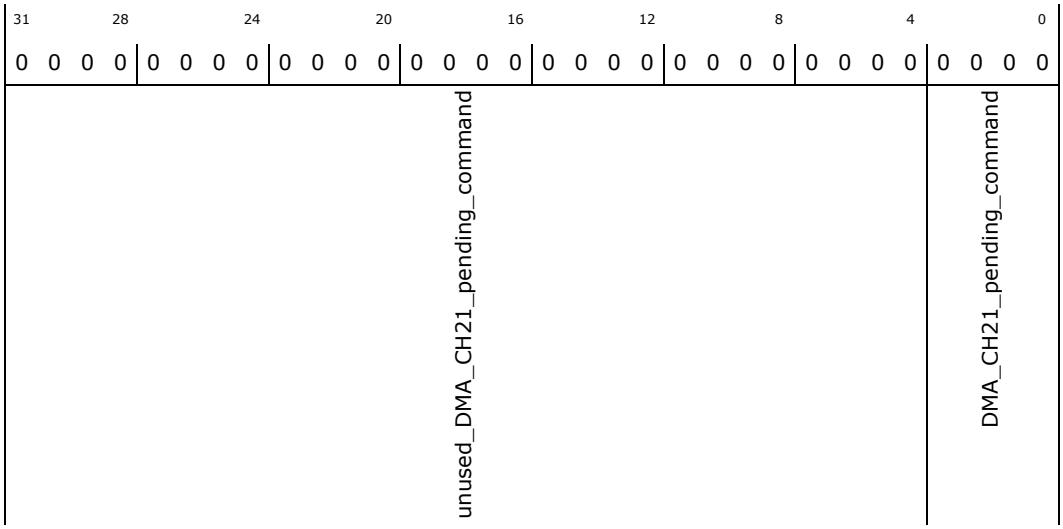
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_pending_command: [ISPMMADR] + 41854h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH21_pending_command:** Unused
3:0	0h RO	**DMA_CH21_pending_command:** DMA CH 21 PARAM 8: Pending commands which will use channel 1

3.7.520 reg_isp_dma_DMA_CH22_pending_command_type (isp_dma_DMA_CH22_pending_command)—Offset 41858h

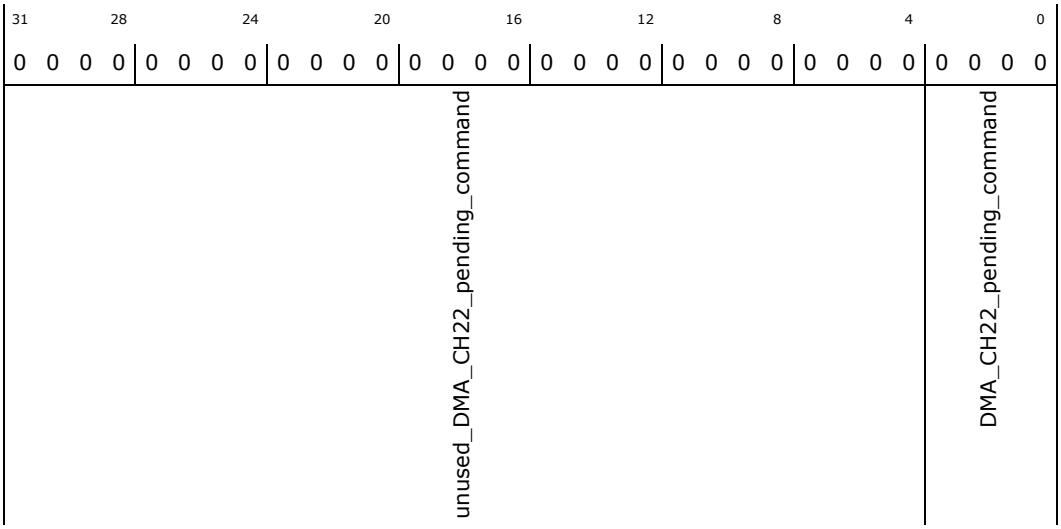
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_pending_command: [ISPMMADR] + 41858h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH22_pending_command:** Unused
3:0	0h RO	**DMA_CH22_pending_command:** DMA CH 22 PARAM 8: Pending commands which will use channel 2

3.7.521 reg_isp_dma_DMA_CH23_pending_command_type (isp_dma_DMA_CH23_pending_command)—Offset 4185Ch

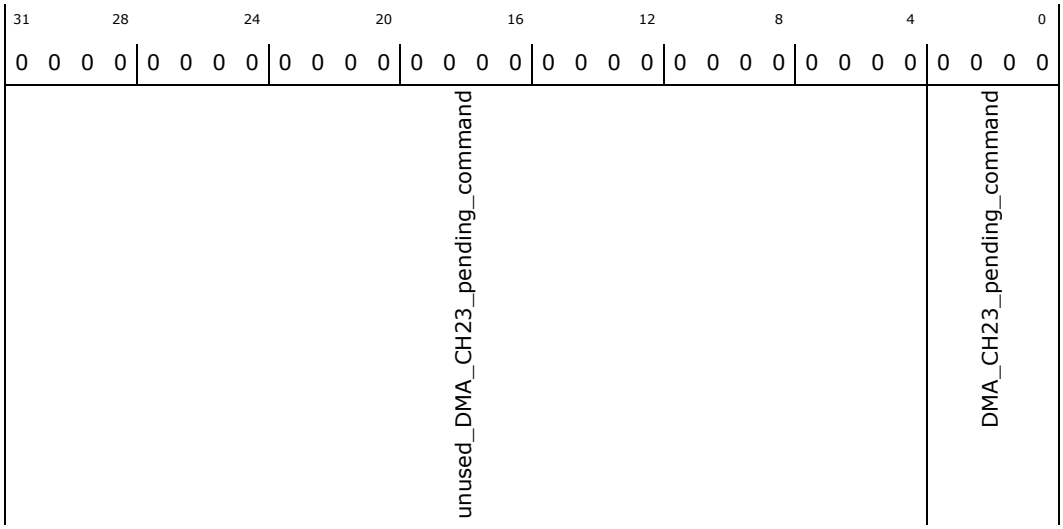
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_pending_command: [ISPMMADR] + 4185Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH23_pending_command:** Unused
3:0	0h RO	**DMA_CH23_pending_command:** DMA CH 20 PARAM 8: Pending commands which will use channel 3

3.7.522 reg_isp_dma_DMA_CH24_pending_command_type (isp_dma_DMA_CH24_pending_command)—Offset 41860h

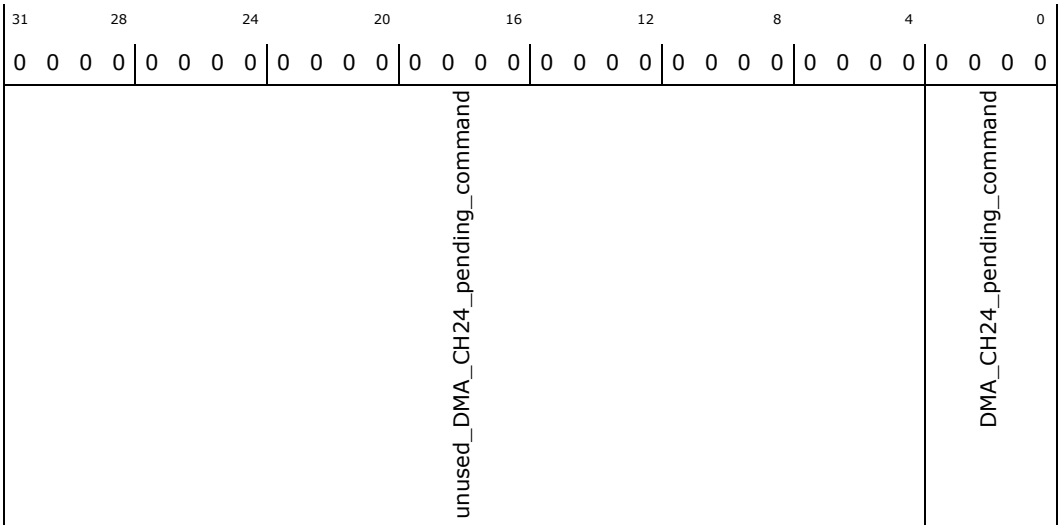
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_pending_command: [ISPMMADR] + 41860h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH24_pending_command:** Unused
3:0	0h RO	**DMA_CH24_pending_command:** DMA CH 24 PARAM 8: Pending commands which will use channel 4

3.7.523 reg_isp_dma_DMA_CH25_pending_command_type (isp_dma_DMA_CH25_pending_command)—Offset 41864h

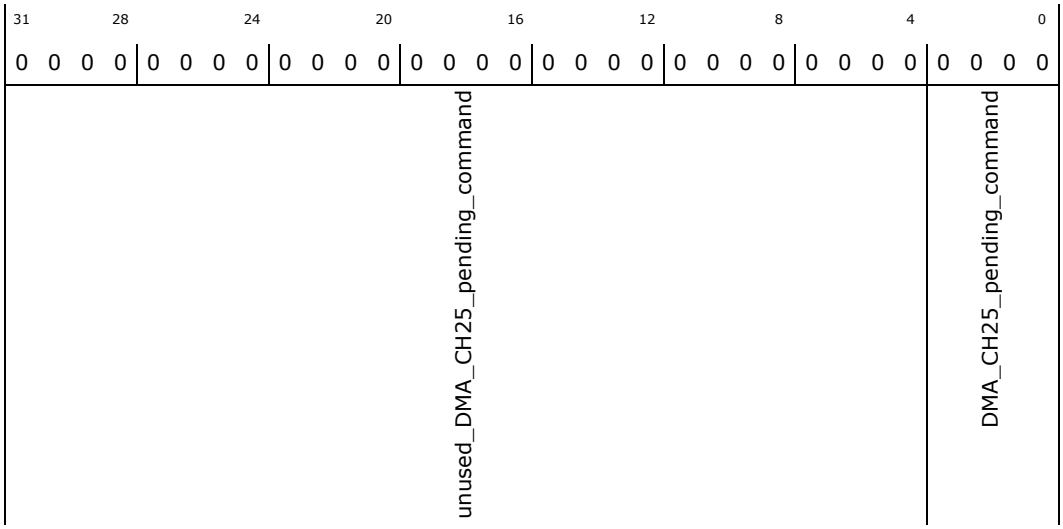
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_pending_command: [ISPMMADR] + 41864h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH25_pending_command:** Unused
3:0	0h RO	**DMA_CH25_pending_command:** DMA CH 25 PARAM 8: Pending commands which will use channel 5

3.7.524 reg_isp_dma_DMA_CH26_pending_command_type (isp_dma_DMA_CH26_pending_command)—Offset 41868h

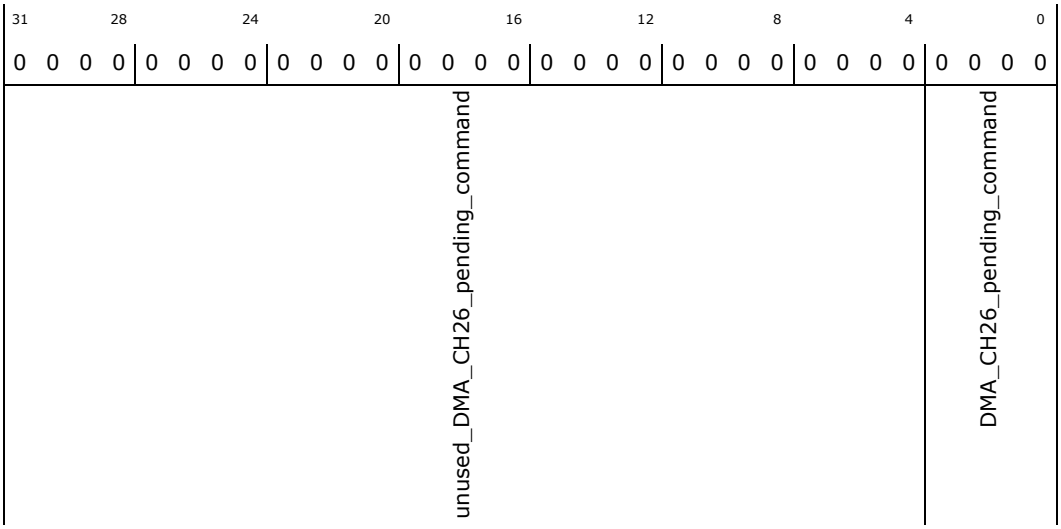
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_pending_command: [ISPMMADR] + 41868h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH26_pending_command:** Unused
3:0	0h RO	**DMA_CH26_pending_command:** DMA CH 26 PARAM 8: Pending commands which will use channel 6

3.7.525 reg_isp_dma_DMA_CH27_pending_command_type (isp_dma_DMA_CH27_pending_command)—Offset 4186Ch

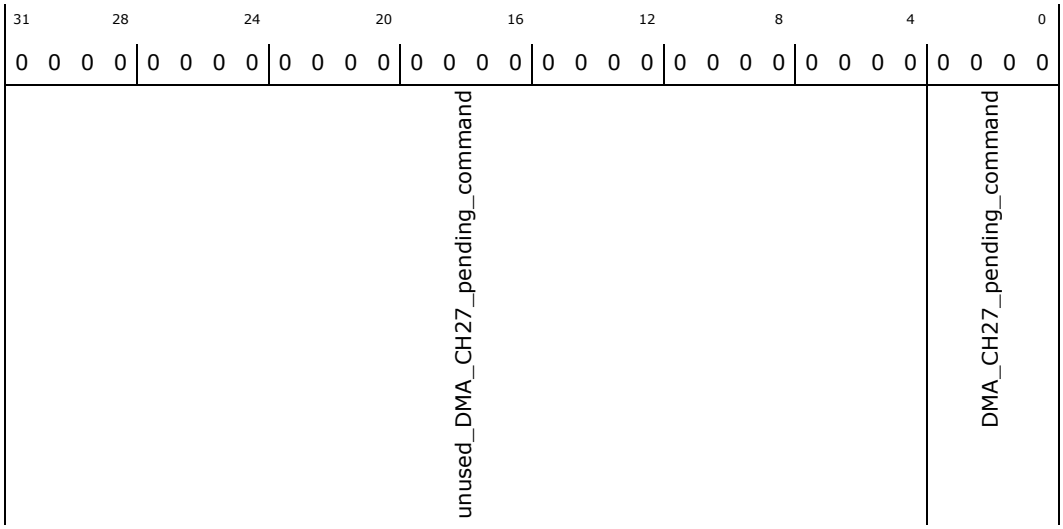
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_pending_command: [ISPMMADR] + 4186Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH27_pending_command:** Unused
3:0	0h RO	**DMA_CH27_pending_command:** DMA CH 27 PARAM 8: Pending commands which will use channel 7

3.7.526 reg_isp_dma_DMA_CH28_pending_command_type (isp_dma_DMA_CH28_pending_command)—Offset 41870h

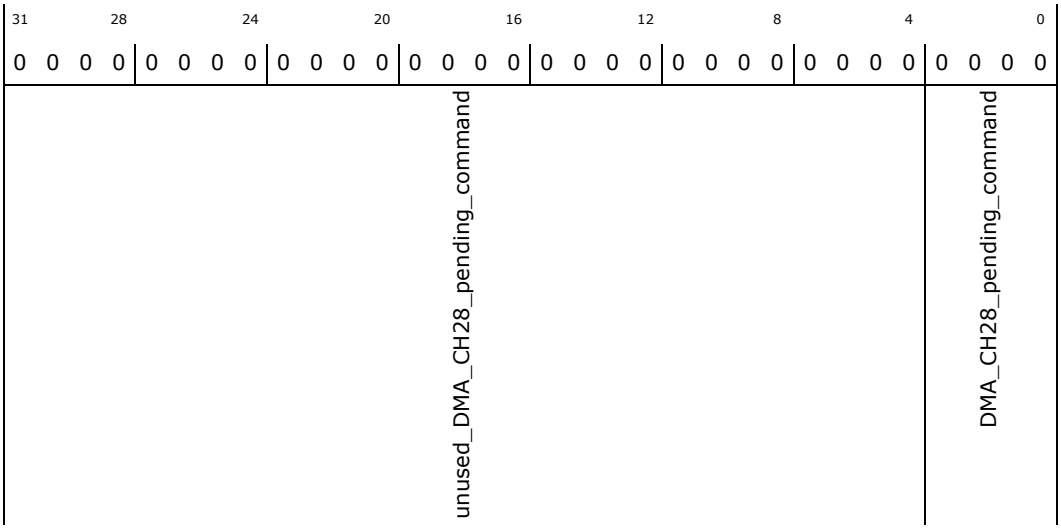
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_pending_command: [ISPMMADR] + 41870h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH28_pending_command:** Unused
3:0	0h RO	**DMA_CH28_pending_command:** DMA CH 28 PARAM 8: Pending commands which will use channel 6

3.7.527 reg_isp_dma_DMA_CH29_pending_command_type (isp_dma_DMA_CH29_pending_command)—Offset 41874h

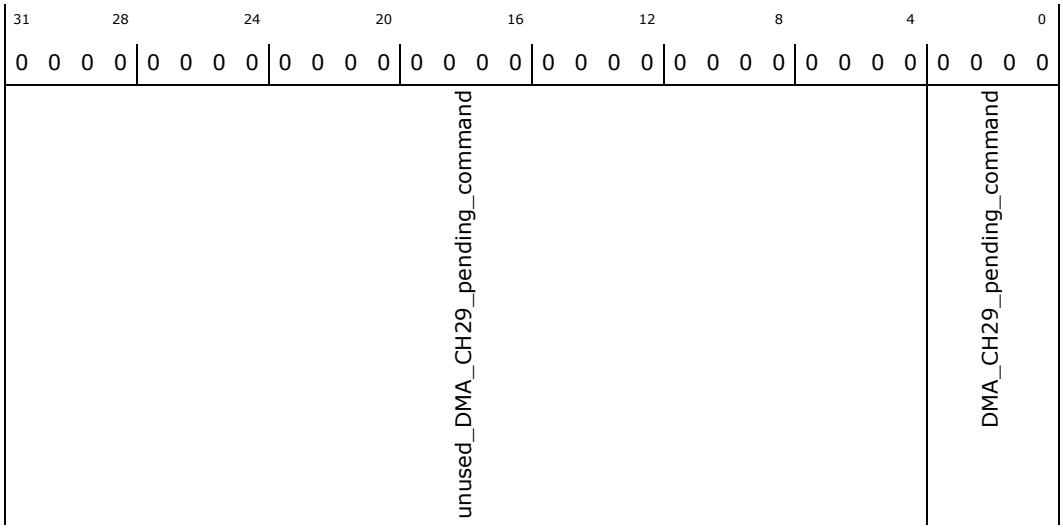
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_pending_command: [ISPMMADR] + 41874h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH29_pending_command:** Unused
3:0	0h RO	**DMA_CH29_pending_command:** DMA CH 29 PARAM 8: Pending commands which will use channel 7

3.7.528 reg_isp_dma_DMA_CH30_pending_command_type (isp_dma_DMA_CH30_pending_command)—Offset 41878h

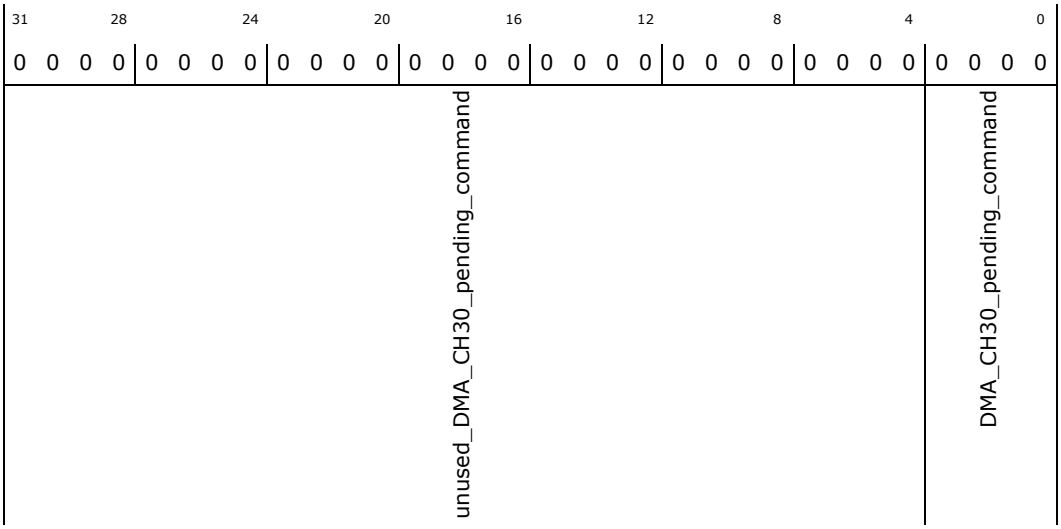
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH30_pending_command: [ISPMMADR] + 41878h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH30_pending_command:** Unused
3:0	0h RO	**DMA_CH30_pending_command:** DMA CH 30 PARAM 8: Pending commands which will use channel 6

3.7.529 reg_isp_dma_DMA_CH31_pending_command_type (isp_dma_DMA_CH31_pending_command)—Offset 4187Ch

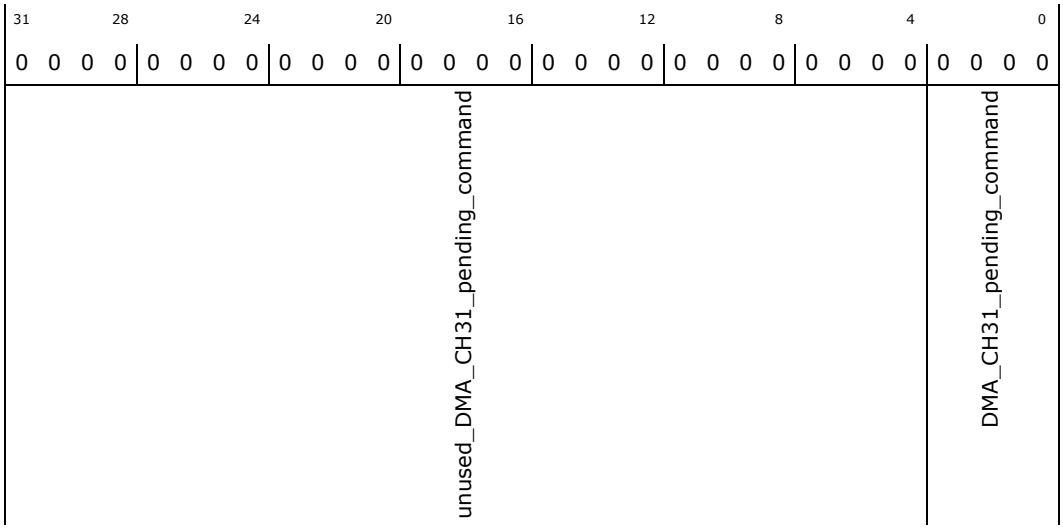
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_pending_command: [ISPMMADR] + 4187Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH31_pending_command:** Unused
3:0	0h RO	**DMA_CH31_pending_command:** DMA CH 30 PARAM 8: Pending commands which will use channel 7

3.7.530 reg_isp_dma_DMA_command_token_type (isp_dma_DMA_command_token)—Offset 42000h

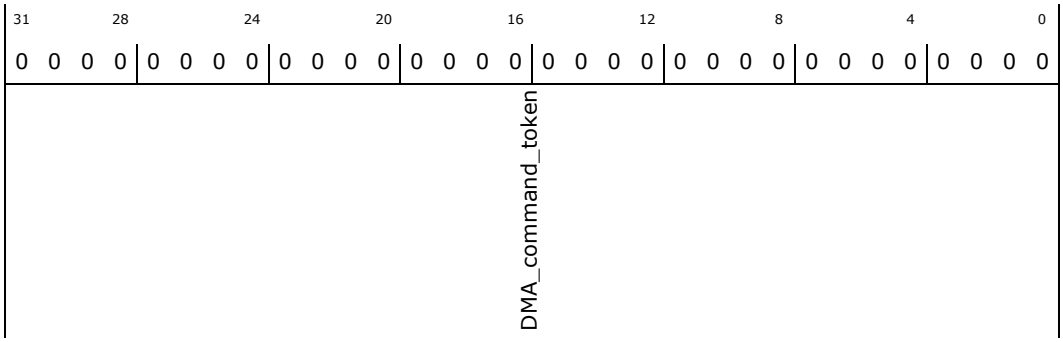
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_command_token: [ISPMMADR] + 42000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_token:** Pending or last executed command token

3.7.531 reg_isp_dma_DMA_command_src_addr_type (isp_dma_DMA_command_src_addr)—Offset 42004h

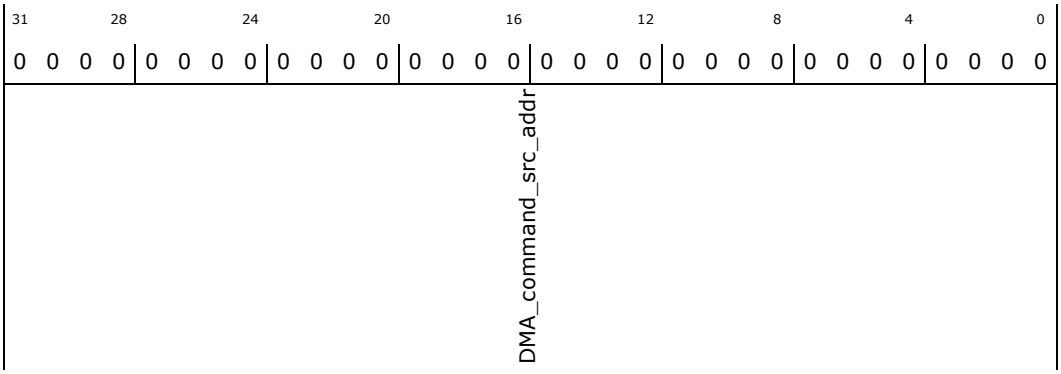
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_command_src_addr: [ISPMMADR] + 42004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_src_addr:** Source address of the pending or last executed command token

3.7.532 reg_isp_dma_DMA_command_dst_addr_type (isp_dma_DMA_command_dst_addr)—Offset 42008h

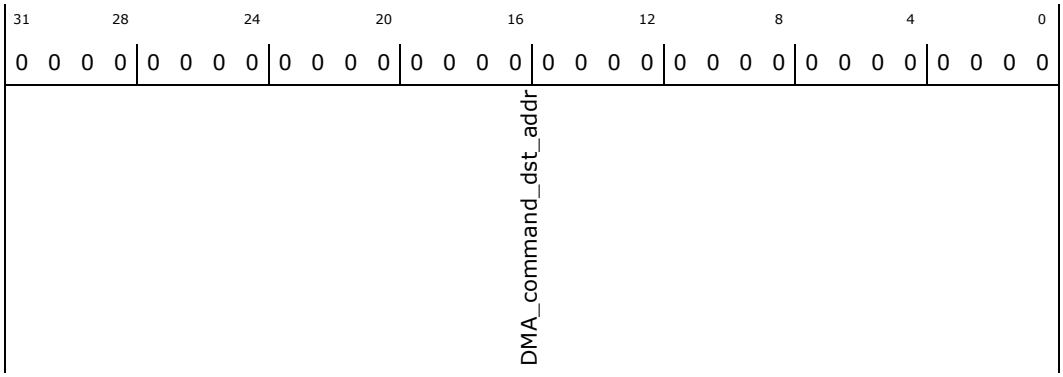
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_command_dst_addr: [ISPMMADR] + 42008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_dst_addr:** Destination address of the pending or last executed command token

3.7.533 reg_isp_dma_DMA_command_ctrl_id_type (isp_dma_DMA_command_ctrl_id)—Offset 4200Ch

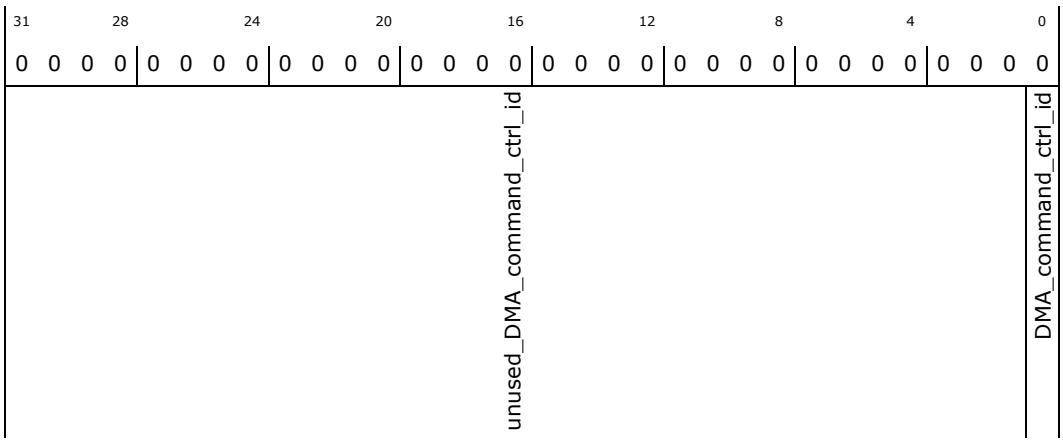
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_command_ctrl_id: [ISPMMADR] + 4200Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_DMA_command_ctrl_id:** Unused
0	0h RO	**DMA_command_ctrl_id:** Controller id of the pending or last executed command token

3.7.534 reg_isp_dma_DMA_FSM_Ctrl_status_type (isp_dma_DMA_FSM_Ctrl_status)—Offset 42010h

DMA FSM Control state and flags

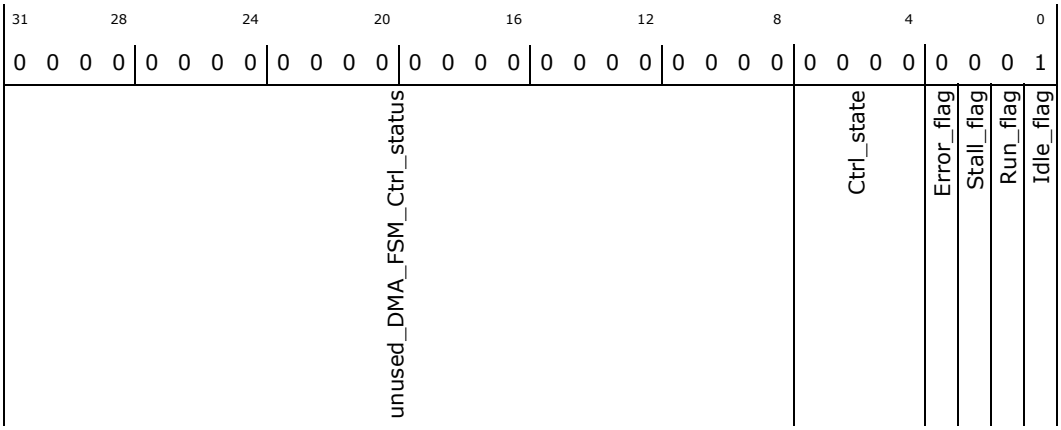
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_status: [ISPMMADR] + 42010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_DMA_FSM_Ctrl_status:** Unused
7:4	0h RO	**Ctrl_state:** FSM control state: 0)Idle -- 1)req_rcv -- 2)rcv -- 3)rcv_req -- 4)init
3	0h RO	**Error_flag:** Error flag
2	0h RO	**Stall_flag:** Stall flag
1	0h RO	**Run_flag:** Run flag
0	1h RO	**Idle_flag:** Idle flag

3.7.535 reg_isp_dma_DMA_FSM_Pack_status_type (isp_dma_DMA_FSM_Pack_status)—Offset 42014h

DMA FSM Pack state

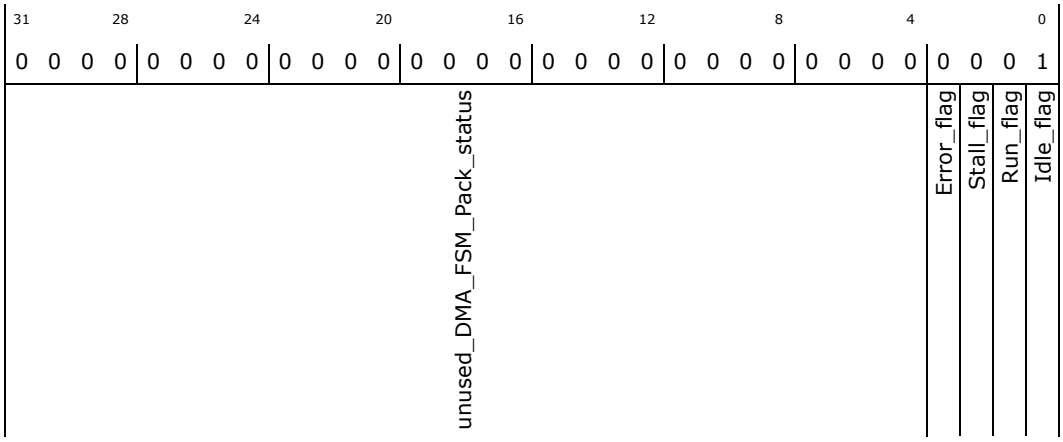
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Pack_status: [ISPMMADR] + 42014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_FSM_Pack_status:** Unused
3	0h RO	**Error_flag:** Error flag
2	0h RO	**Stall_flag:** Stall flag
1	0h RO	**Run_flag:** Run flag
0	1h RO	**Idle_flag:** Idle flag

3.7.536 reg_isp_dma_DMA_FSM_request_status_type (isp_dma_DMA_FSM_request_status)—Offset 42018h

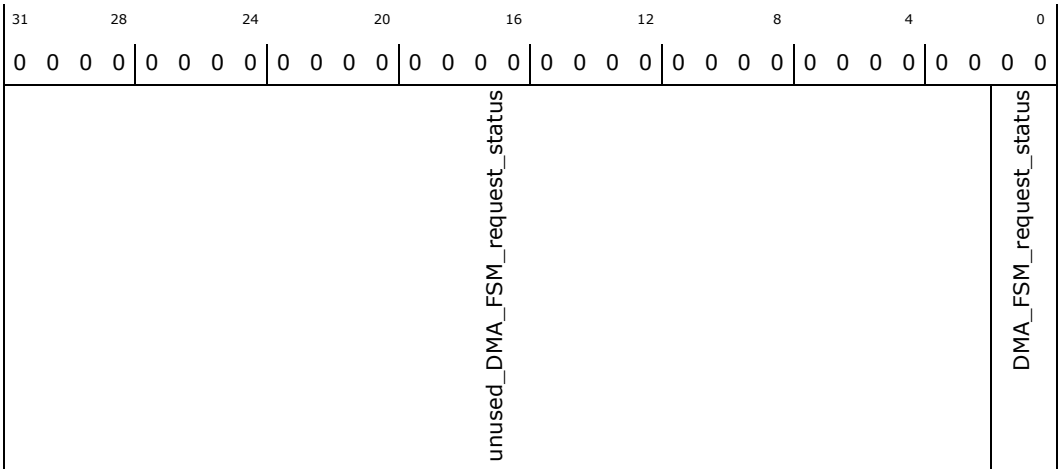
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_request_status: [ISPMMADR] + 42018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_request_status:** Unused
1:0	0h RO	**DMA_FSM_request_status:** DMA FSM Request state: 0)Idle -- 1)req -- 2)Next line

3.7.537 reg_isp_dma_DMA_FSM_write_status_type (isp_dma_DMA_FSM_write_status)—Offset 4201Ch

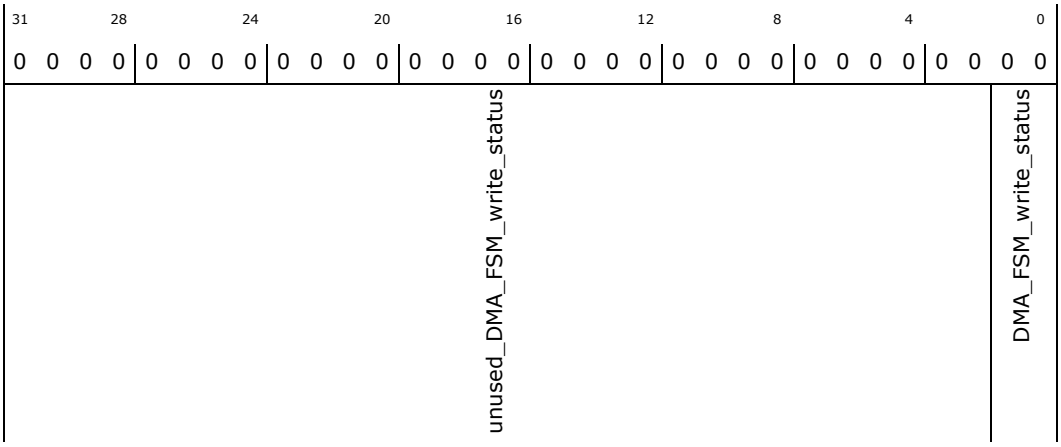
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_write_status: [ISPMMADR] + 4201Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_write_status:** Unused
1:0	0h RO	**DMA_FSM_write_status:** DMA FSM Write state: 0)Idle -- 1)req -- 2)Next line

3.7.538 reg_isp_dma_DMA_FSM_Ctrl_dev_idx_type (isp_dma_DMA_FSM_Ctrl_dev_idx)—Offset 42110h

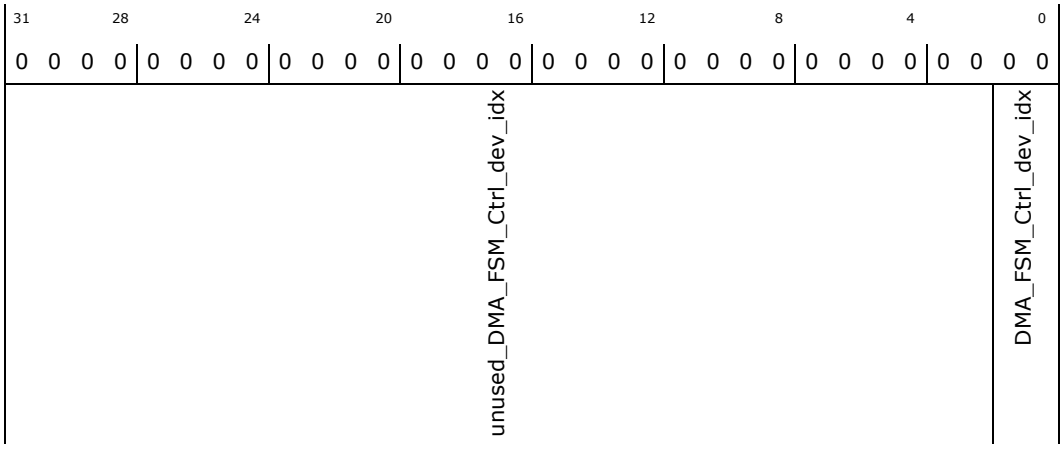
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_dev_idx: [ISPMMADR] + 42110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_Ctrl_dev_idx:** Unused
1:0	0h RO	**DMA_FSM_Ctrl_dev_idx:** DMA FSM Control request device idx

3.7.539 reg_isp_dma_DMA_FSM_Pack_cnt_Yb_type (isp_dma_DMA_FSM_Pack_cnt_Yb)—Offset 42114h

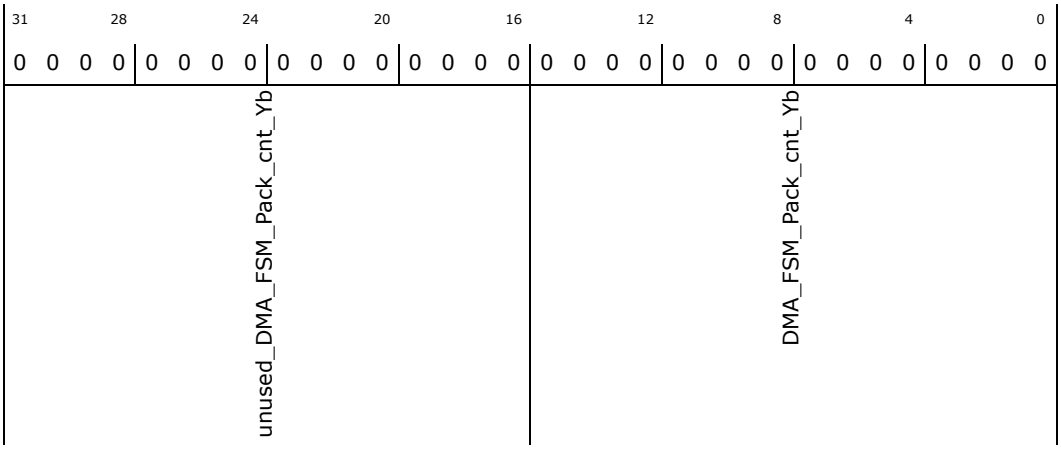
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Pack_cnt_Yb: [ISPMMADR] + 42114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_cnt_Yb:** Unused
15:0	0h RO	**DMA_FSM_Pack_cnt_Yb:** DMA FSM pack counter height (Yb)

3.7.540 reg_isp_dma_DMA_FSM_Request_cnt_Yb_type (isp_dma_DMA_FSM_Request_cnt_Yb)—Offset 42118h

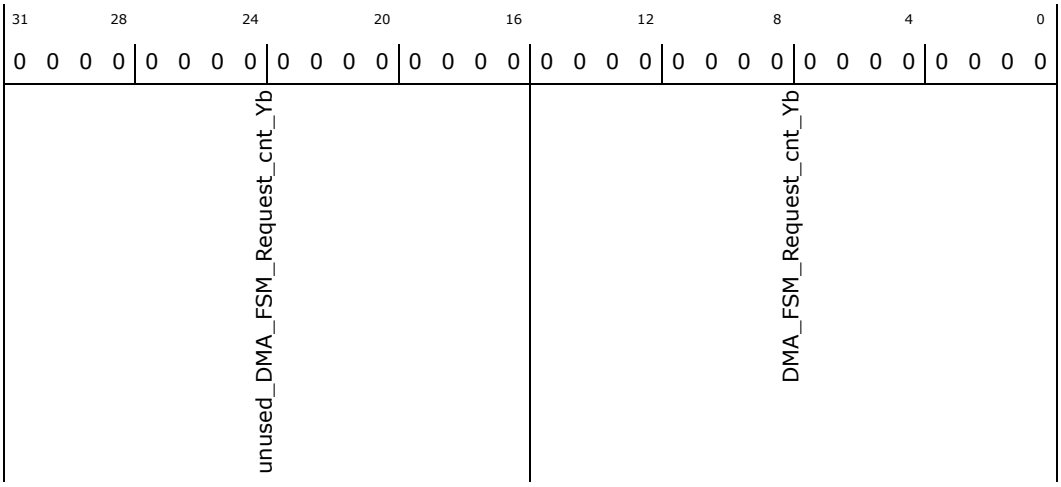
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Request_cnt_Yb: [ISPMMADR] + 42118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Request_cnt_Yb:** Unused
15:0	0h RO	**DMA_FSM_Request_cnt_Yb:** DMA FSM request counter height (Yb)

3.7.541 reg_isp_dma_DMA_FSM_Write_cnt_Y_type (isp_dma_DMA_FSM_Write_cnt_Y)—Offset 4211Ch

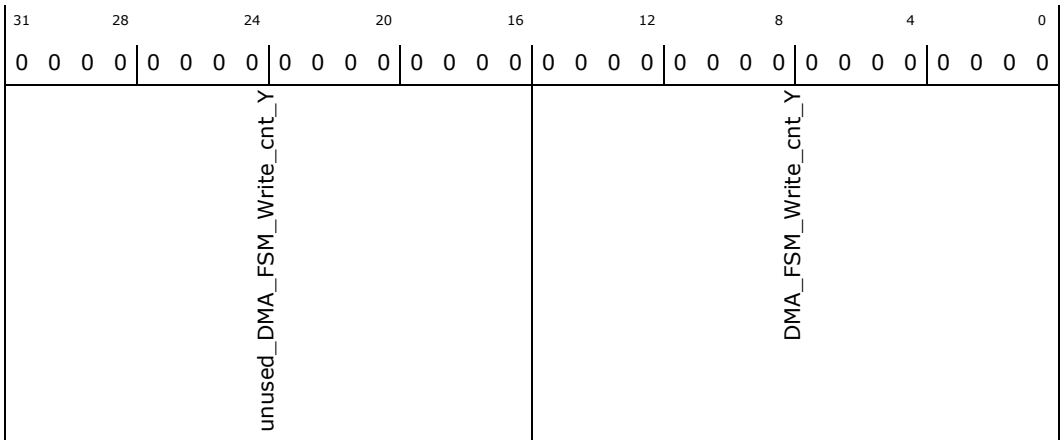
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Write_cnt_Y: [ISPMMADR] + 4211Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Write_cnt_Y:** Unused
15:0	0h RO	**DMA_FSM_Write_cnt_Y:** DMA FSM Write counter height (Yb)

3.7.542 reg_isp_dma_DMA_FSM_Ctrl_req_addr_type (isp_dma_DMA_FSM_Ctrl_req_addr)—Offset 42210h

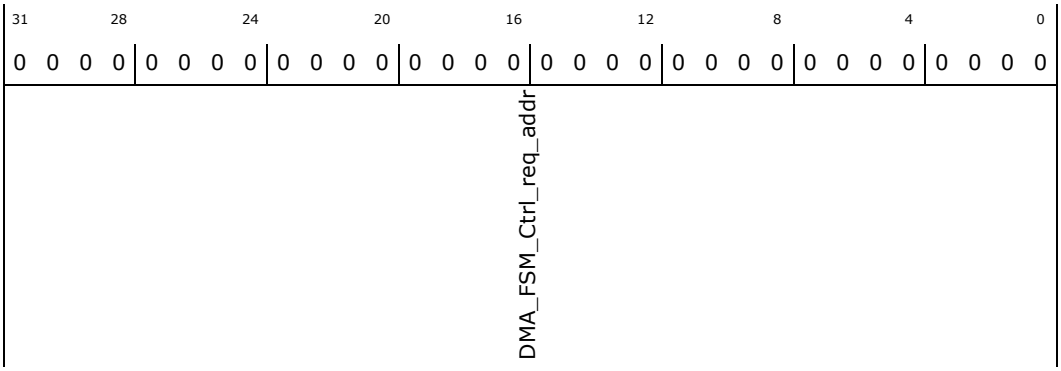
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_req_addr: [ISPMMADR] + 42210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_req_addr:** DMA FSM Control request address

3.7.543 reg_isp_dma_DMA_FSM_Pack_req_cnt_Xb_type (isp_dma_DMA_FSM_Pack_req_cnt_Xb)—Offset 42214h

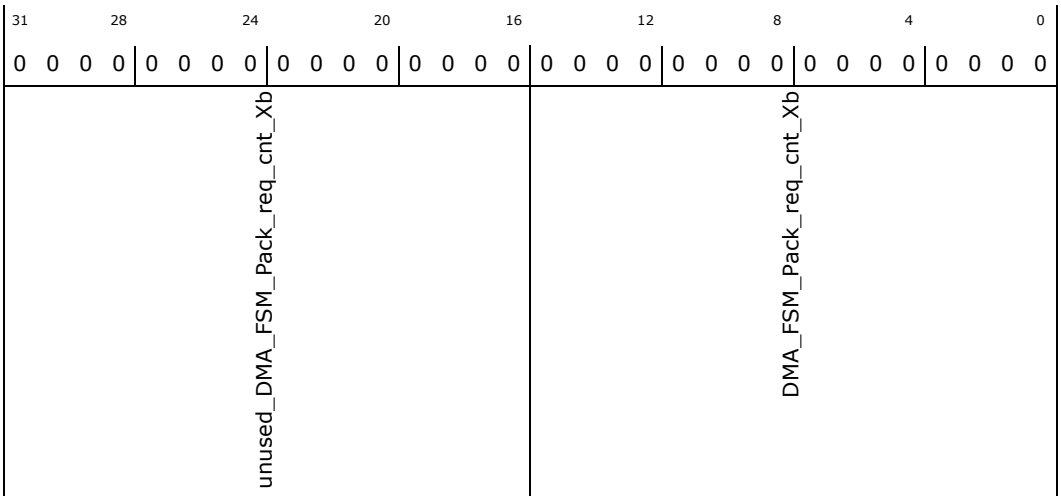
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Pack_req_cnt_Xb: [ISPMMADR] + 42214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_req_cnt_Xb:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_FSM_Pack_req_cnt_Xb:** DMA FSM pack request counter width (Xb)

3.7.544 reg_isp_dma_DMA_FSM_Request_cnt_Xb_type (isp_dma_DMA_FSM_Request_cnt_Xb)—Offset 42218h

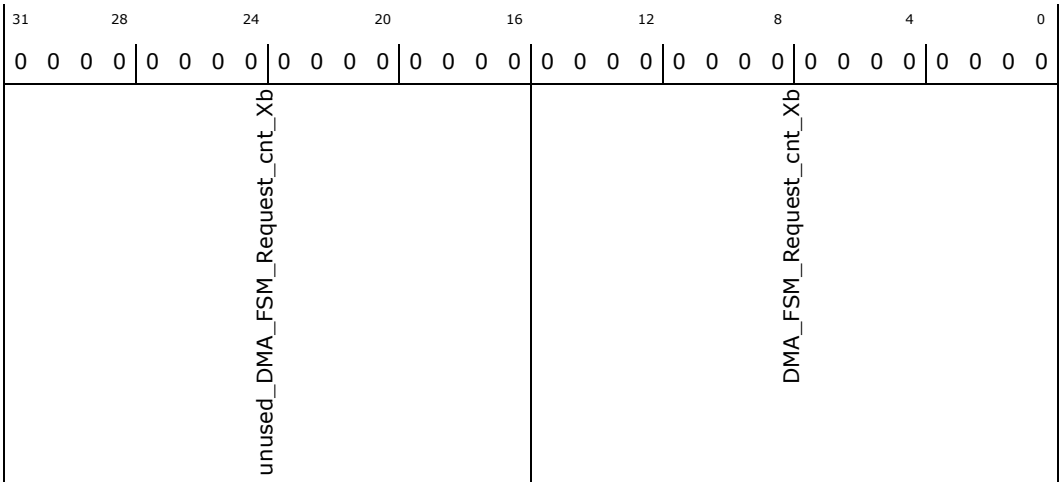
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Request_cnt_Xb: [ISPMMADR] + 42218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Request_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Request_cnt_Xb:** DMA FSM Request counter width (Xb)

3.7.545 reg_isp_dma_DMA_FSM_Write_cnt_Xb_type (isp_dma_DMA_FSM_Write_cnt_Xb)—Offset 4221Ch

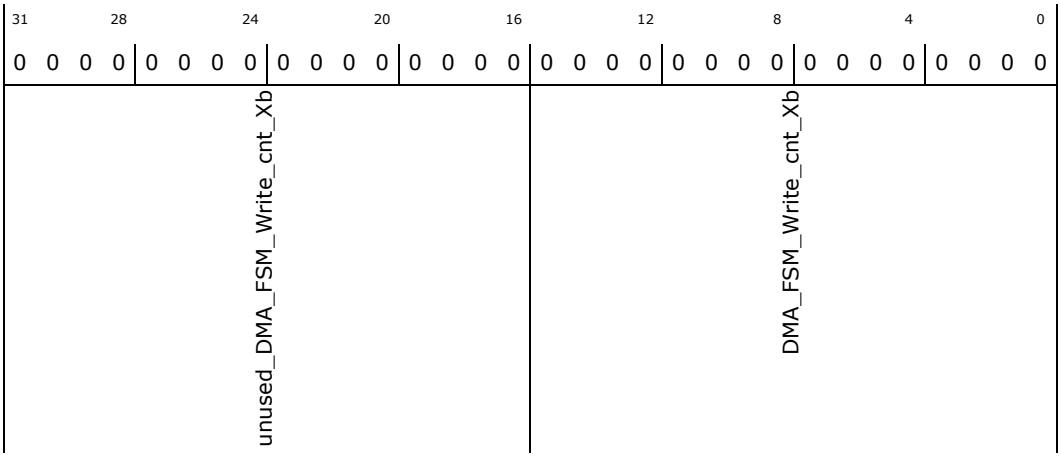
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Write_cnt_Xb: [ISPMMADR] + 4221Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Write_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Write_cnt_Xb:** DMA FSM Write counter width (Xb)

3.7.546 reg_isp_dma_DMA_FSM_Ctrl_req_stride_type (isp_dma_DMA_FSM_Ctrl_req_stride)—Offset 42310h

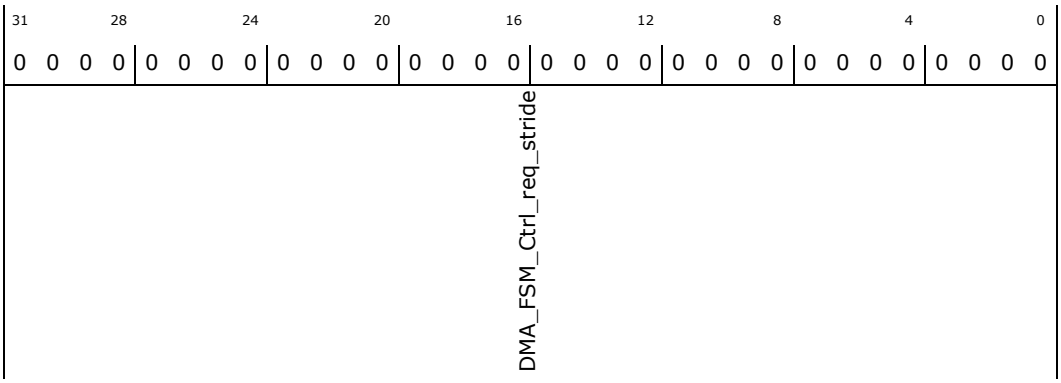
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_req_stride: [ISPMMADR] + 42310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_req_stride:** DMA FSM Control request stride

3.7.547 reg_isp_dma_DMA_FSM_Pack_wr_cnt_Xb_type (isp_dma_DMA_FSM_Pack_wr_cnt_Xb)—Offset 42314h

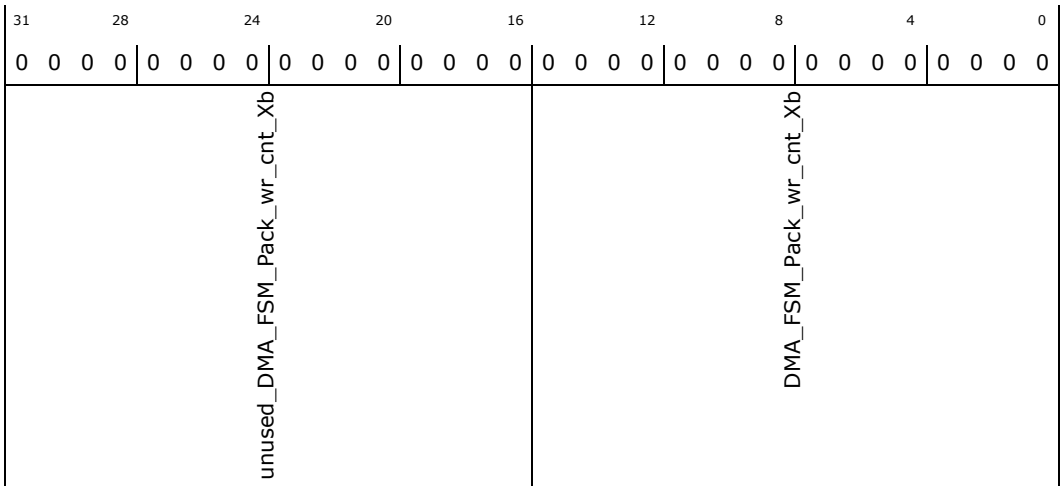
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Pack_wr_cnt_Xb: [ISPMMADR] + 42314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_wr_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Pack_wr_cnt_Xb:** DMA FSM pack write counter width (Xb)

3.7.548 reg_isp_dma_DMA_FSM_Req_remining_Xb_type (isp_dma_DMA_FSM_Req_remining_Xb)—Offset 42318h

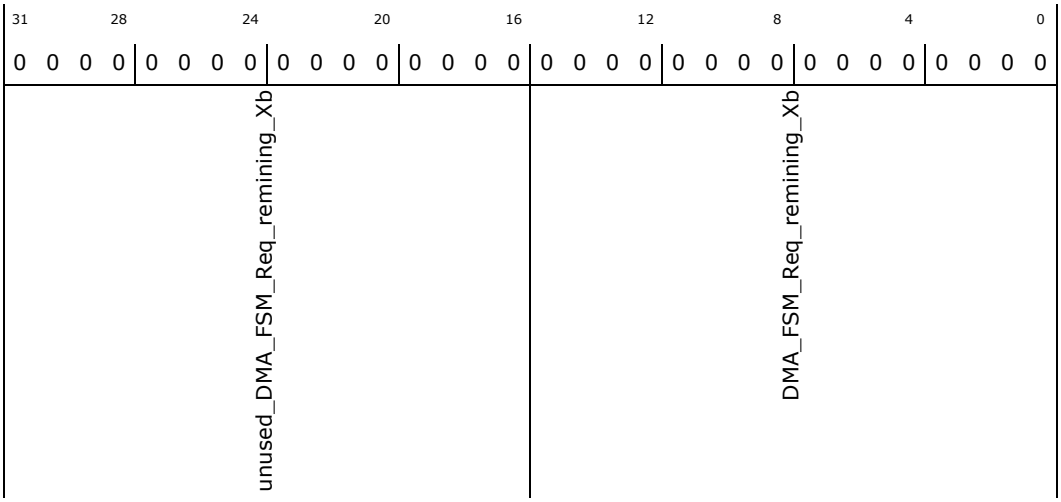
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Req_remining_Xb: [ISPMMADR] + 42318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Req_remining_Xb:** Unused
15:0	0h RO	**DMA_FSM_Req_remining_Xb:** DMA FSM Request counter remaining word width

3.7.549 reg_isp_dma_DMA_FSM_Wr_remining_Xb_type (isp_dma_DMA_FSM_Wr_remining_Xb)—Offset 4231Ch

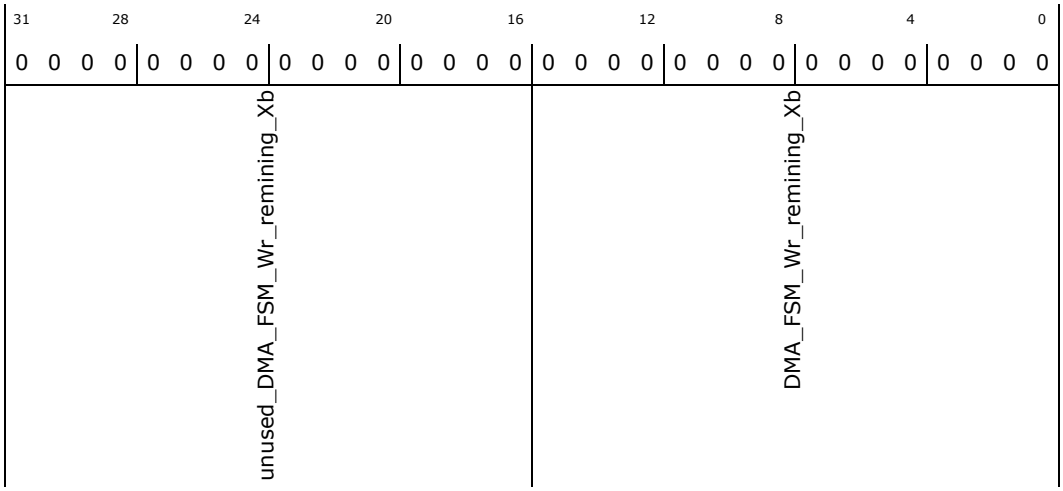
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Wr_remining_Xb: [ISPMMADR] + 4231Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Wr_remining_Xb:** Unused
15:0	0h RO	**DMA_FSM_Wr_remining_Xb:** DMA FSM Write counter remaining word width

3.7.550 reg_isp_dma_DMA_FSM_Ctrl_req_Xb_type (isp_dma_DMA_FSM_Ctrl_req_Xb)—Offset 42410h

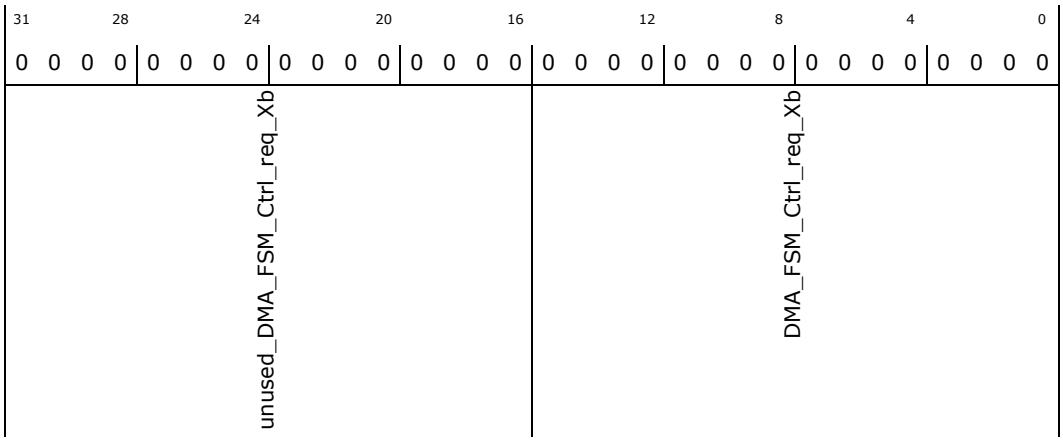
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_req_Xb: [ISPMMADR] + 42410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_req_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_req_Xb:** DMA FSM Control request width (Xb)

3.7.551 reg_isp_dma_DMA_FSM_Req_burst_cnt_type (isp_dma_DMA_FSM_Req_burst_cnt)—Offset 42418h

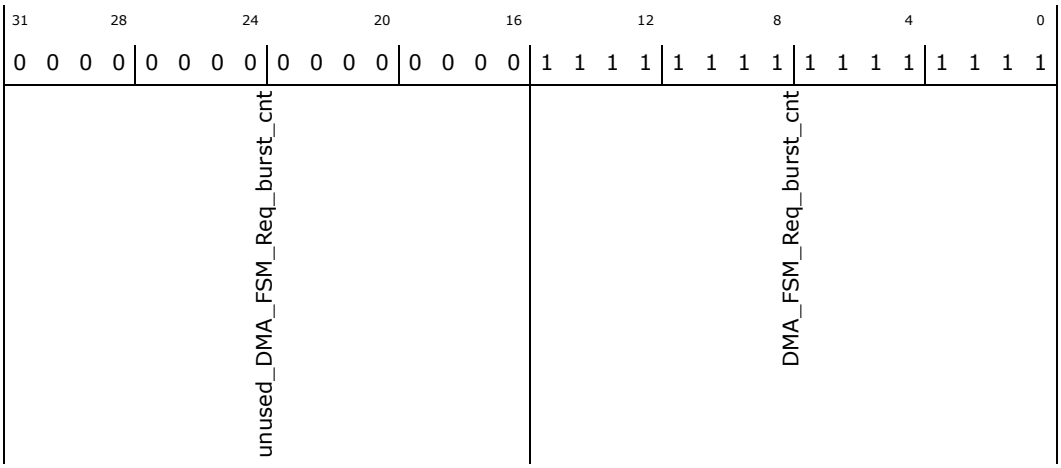
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Req_burst_cnt: [ISPMMADR] + 42418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Req_burst_cnt:** Unused
15:0	FFFFh RO	**DMA_FSM_Req_burst_cnt:** DMA FSM Request word burst counter

3.7.552 reg_isp_dma_DMA_FSM_Wr_burst_cnt_type (isp_dma_DMA_FSM_Wr_burst_cnt)—Offset 4241Ch

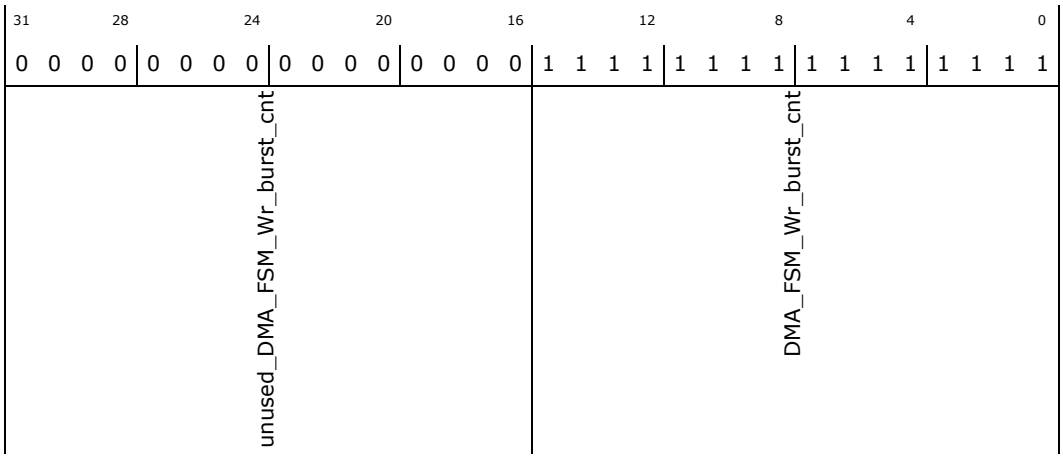
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Wr_burst_cnt: [ISPMMADR] + 4241Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Wr_burst_cnt:** Unused
15:0	FFFFh RO	**DMA_FSM_Wr_burst_cnt:** DMA FSM Write word burst counter

3.7.553 reg_isp_dma_DMA_FSM_Ctrl_req_Yb_type (isp_dma_DMA_FSM_Ctrl_req_Yb)—Offset 42510h

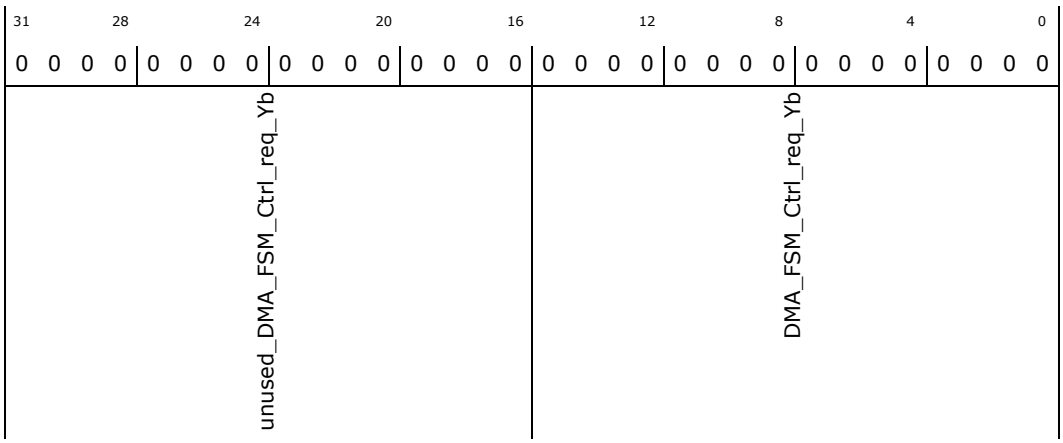
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_req_Yb: [ISPMMADR] + 42510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_req_Yb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_req_Yb:** DMA FSM Control request height (Yb)

3.7.554 reg_isp_dma_DMA_FSM_Ctrl_Pack_req_dev_idx_type (isp_dma_DMA_FSM_Ctrl_Pack_req_dev_idx)—Offset 42610h

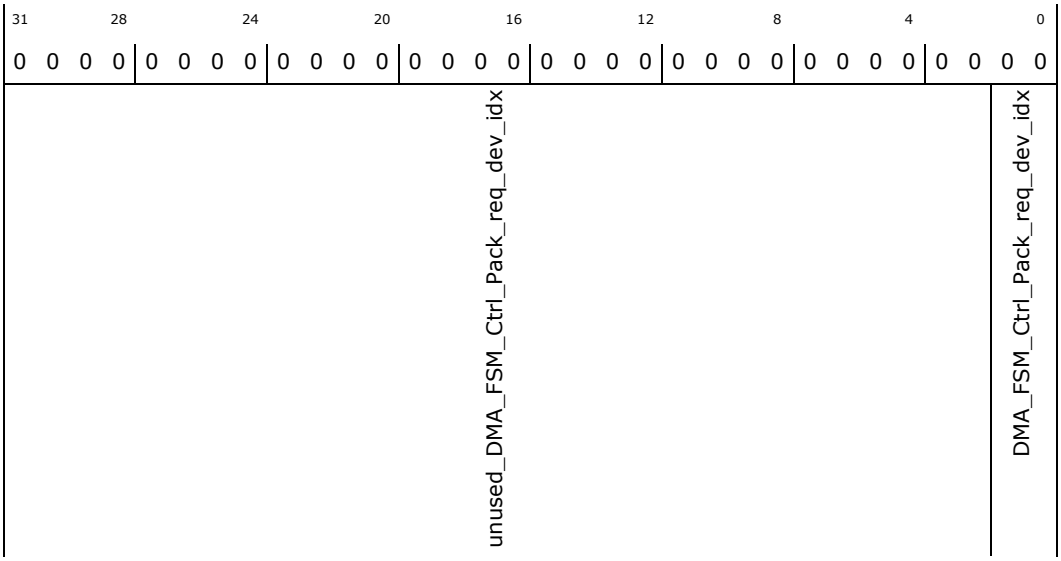
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_Pack_req_dev_idx: [ISPMMADR] + 42610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_Ctrl_Pack_req_dev_idx:** Unused
1:0	0h RO	**DMA_FSM_Ctrl_Pack_req_dev_idx:** DMA FSM Control pack request device idx

3.7.555 reg_isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx_type (isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx)—Offset 42710h

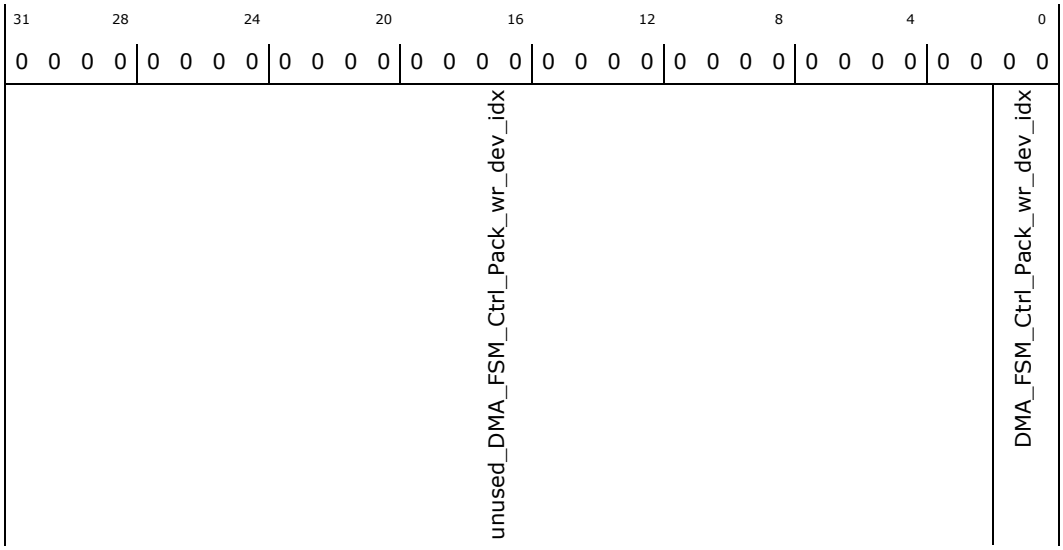
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx: [ISPMMADR] + 42710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_Ctrl_Pack_wr_dev_idx:** Unused
1:0	0h RO	**DMA_FSM_Ctrl_Pack_wr_dev_idx:** DMA FSM Control pack write device idx

3.7.556 reg_isp_dma_DMA_FSM_Ctrl_Wr_addr_type (isp_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 42810h

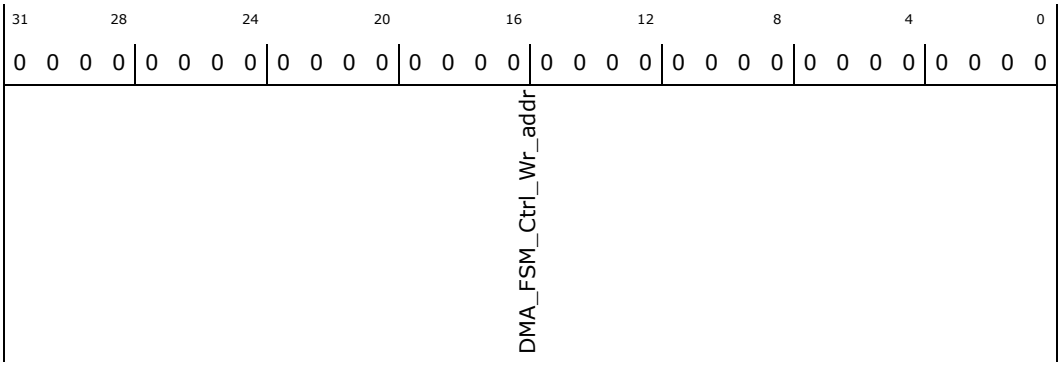
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_Wr_addr: [ISPMMADR] + 42810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_Wr_addr:** DMA FSM Control write address

3.7.557 reg_isp_dma_DMA_FSM_Ctrl_Wr_stride_type (isp_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 42910h

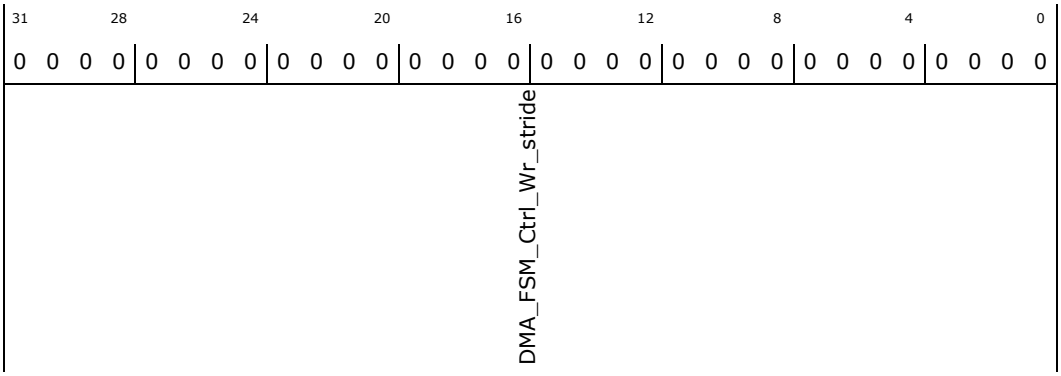
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_Wr_stride: [ISPMMADR] + 42910h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_Wr_stride:** DMA FSM Control write stride

3.7.558 reg_isp_dma_DMA_FSM_Ctrl_pack_req_Xb_type (isp_dma_DMA_FSM_Ctrl_pack_req_Xb)—Offset 42A10h

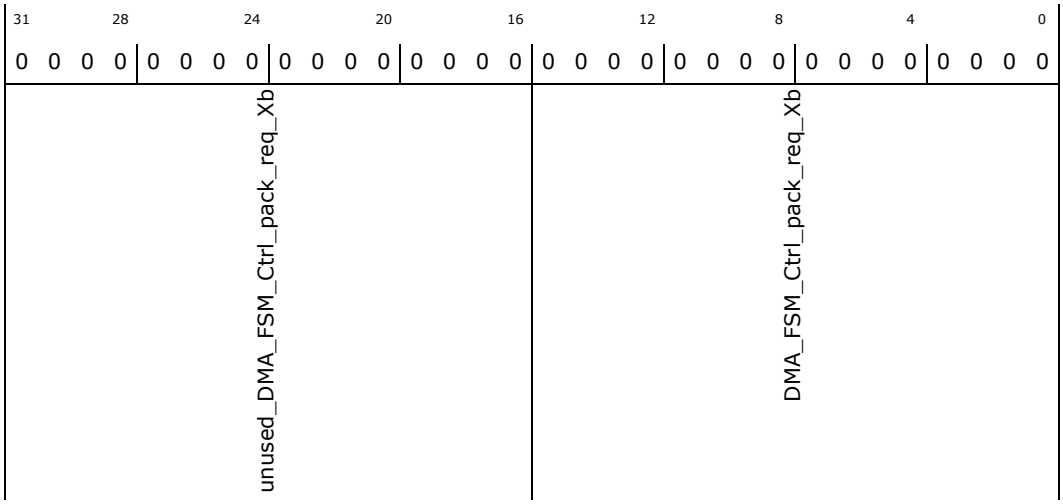
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_req_Xb: [ISPMMADR] + 42A10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_req_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_req_Xb:** DMA FSM Control FSM Pack request width (Xb)

3.7.559 reg_isp_dma_DMA_FSM_Ctrl_pack_Yb_type (isp_dma_DMA_FSM_Ctrl_pack_Yb)—Offset 42B10h

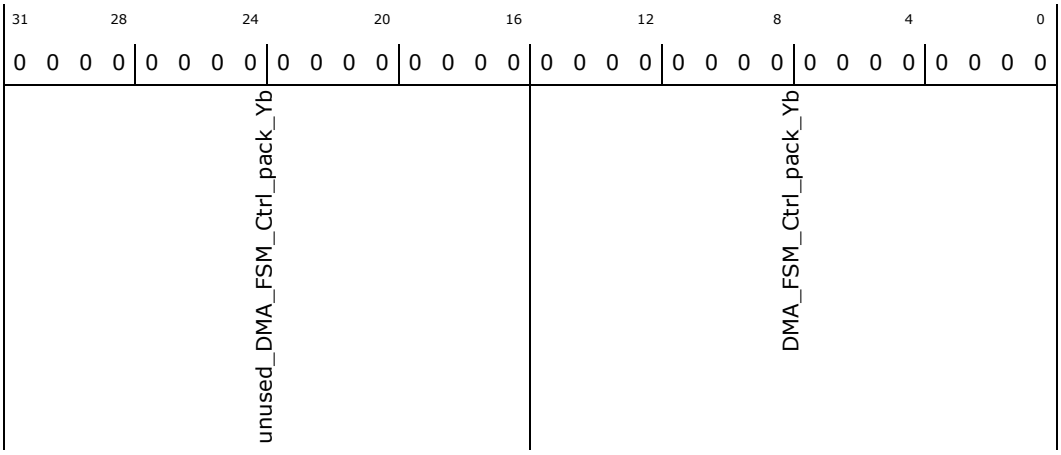
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_Yb: [ISPMMADR] + 42B10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_Yb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_Yb:** DMA FSM Control FSM Pack height (Yb)

3.7.560 reg_isp_dma_DMA_FSM_Ctrl_pack_wr_Xb_type (isp_dma_DMA_FSM_Ctrl_pack_wr_Xb)—Offset 42C10h

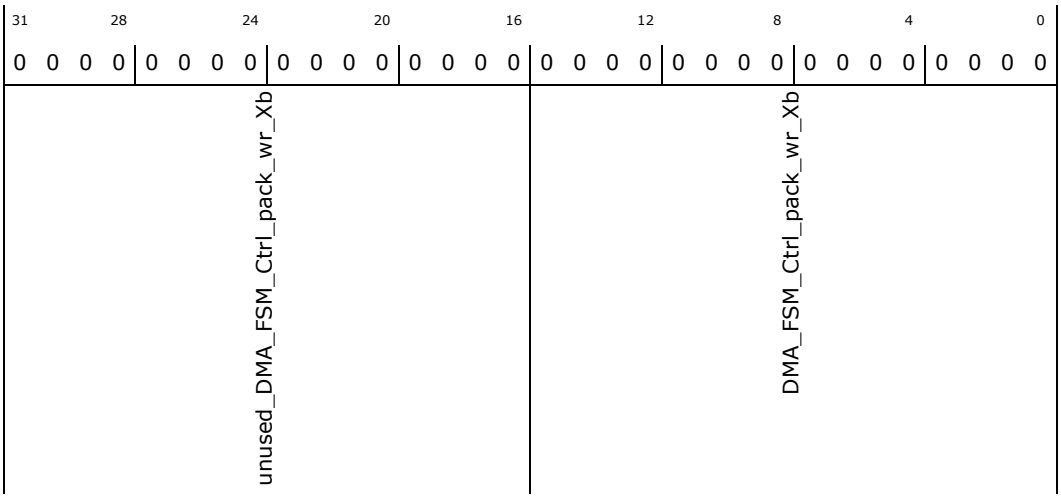
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_wr_Xb: [ISPMMADR] + 42C10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_wr_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_wr_Xb:** DMA FSM Control FSM Pack write width (Xb)

3.7.561 reg_isp_dma_DMA_FSM_Ctrl_pack_req_elem_type (isp_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 42D10h

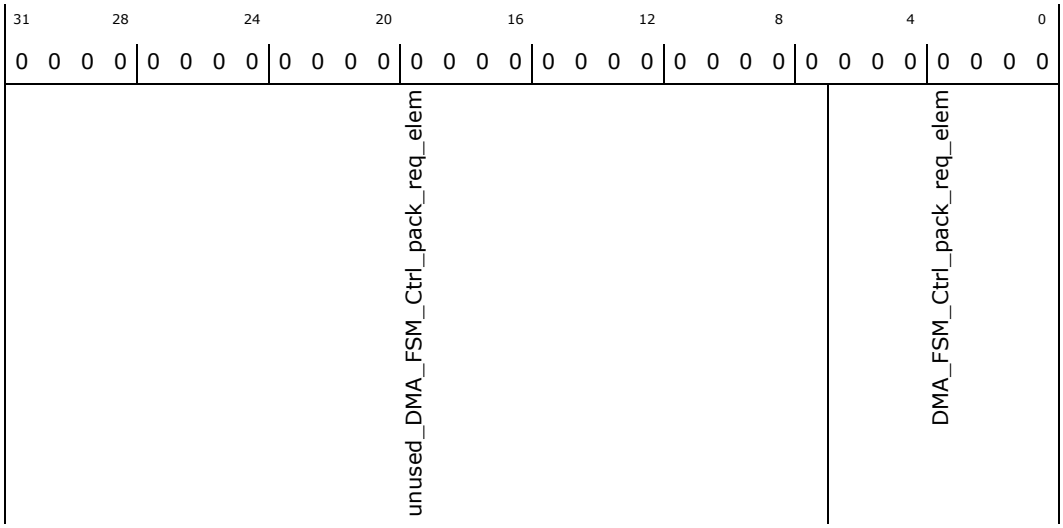
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_req_elem: [ISPMMADR] + 42D10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**unused_DMA_FSM_Ctrl_pack_req_elem:** Unused
6:0	0h RO	**DMA_FSM_Ctrl_pack_req_elem:** DMA FSM Control pack request element per word

3.7.562 reg_isp_dma_DMA_FSM_Ctrl_pack_wr_elem_type (isp_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 42E10h

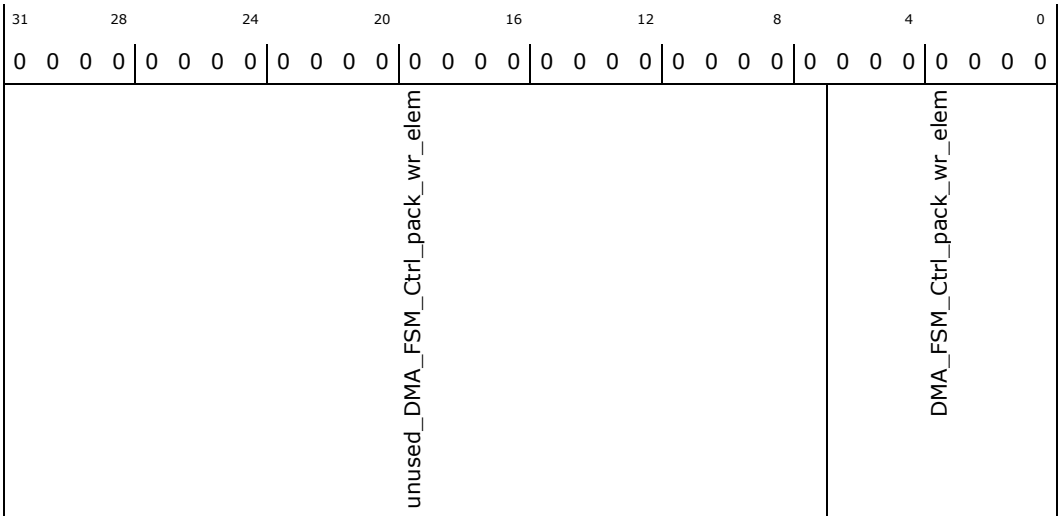
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_wr_elem: [ISPMMADR] + 42E10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**unused_DMA_FSM_Ctrl_pack_wr_elem:** Unused
6:0	0h RO	**DMA_FSM_Ctrl_pack_wr_elem:** DMA FSM Control pack write element per word

3.7.563 reg_isp_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id_type (isp_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id)—Offset 42F10h

DMA FSM Control pack element sign zero extension and controller ID

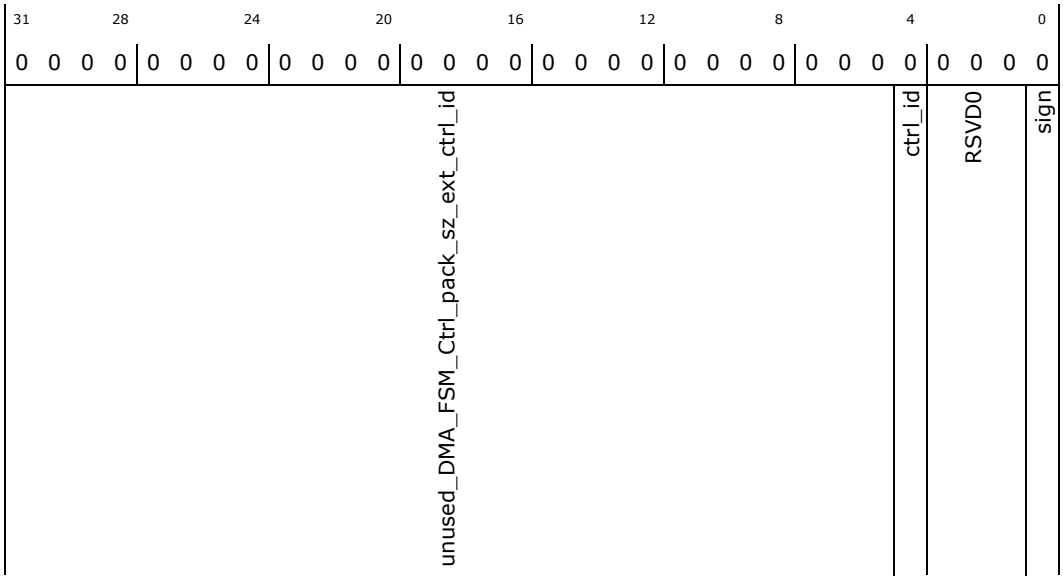
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id: [ISPMMADR] + 42F10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id:** Unused
4	0h RO	**ctrl_id:** Controller ID
3:1	0b RO	**RSVD0:** Reserved
0	0h RO	**sign:** element sign(1)/zero(0) extension

3.7.564 reg_isp_dma_Dev_Interf_0_req_side_type (isp_dma_Dev_Interf_0_req_side)—Offset 43000h

DMA Device interface 0 internal side status

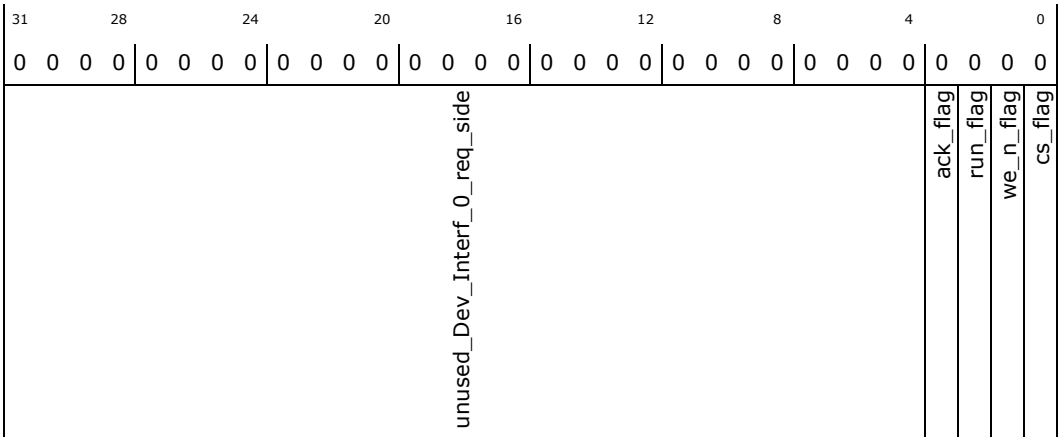
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_0_req_side: [ISPMMADR] + 43000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_0_req_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	0h RO	**run_flag:** Run flag
1	0h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

3.7.565 reg_isp_dma_Dev_Interf_1_req_side_type (isp_dma_Dev_Interf_1_req_side)—Offset 43004h

DMA Device interface 1 internal side status

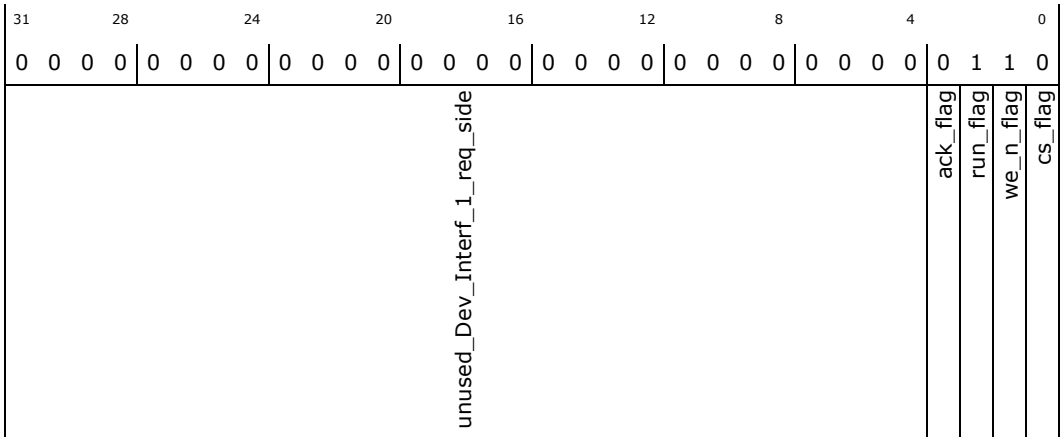
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_1_req_side: [ISPMMADR] + 43004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_1_req_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	1h RO	**run_flag:** Run flag
1	1h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

3.7.566 reg_isp_dma_Dev_Interf_2_req_side_type (isp_dma_Dev_Interf_2_req_side)—Offset 43008h

DMA Device interface 2 internal side status

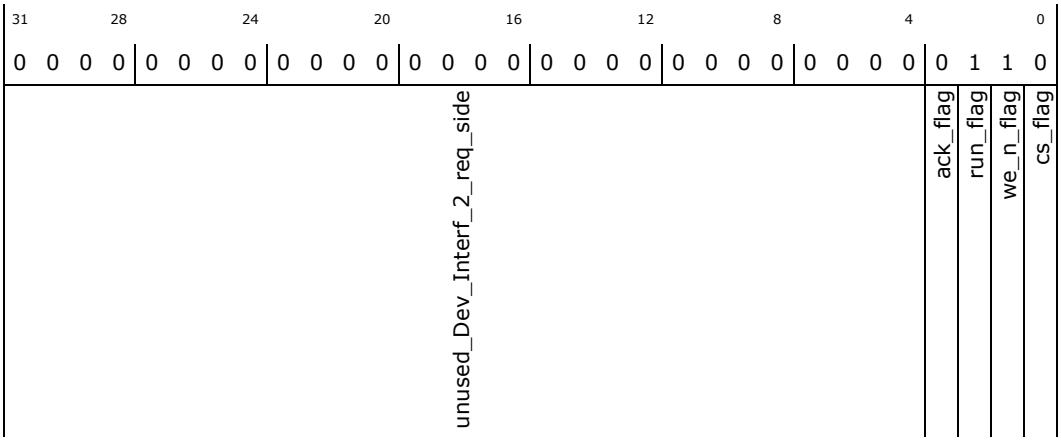
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_2_req_side: [ISPMMADR] + 43008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_2_req_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	1h RO	**run_flag:** Run flag
1	1h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

3.7.567 reg_isp_dma_Dev_Interf_0_snd_side_type (isp_dma_Dev_Interf_0_snd_side)—Offset 43100h

DMA Device interface 0 output side status

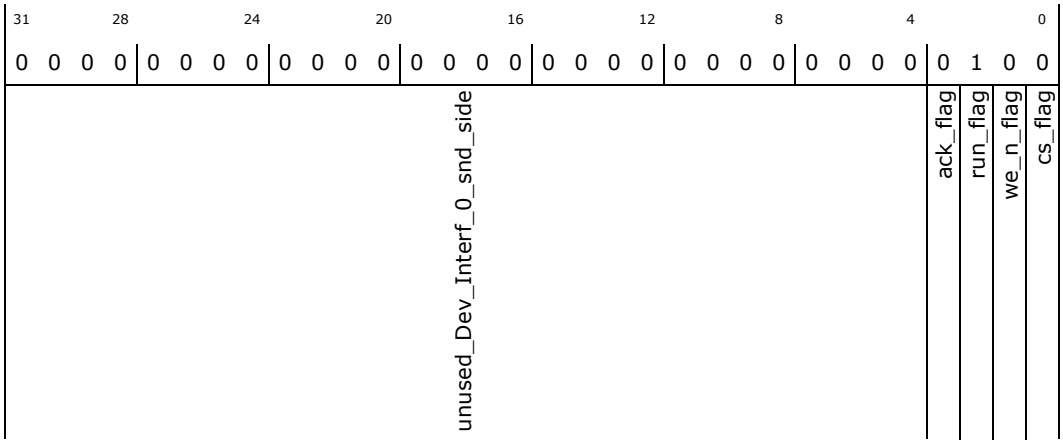
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_0_snd_side: [ISPMMADR] + 43100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_0_snd_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	1h RO	**run_flag:** Run flag
1	0h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

3.7.568 reg_isp_dma_Dev_Interf_1_snd_side_type (isp_dma_Dev_Interf_1_snd_side)—Offset 43104h

DMA Device interface 1 output side status

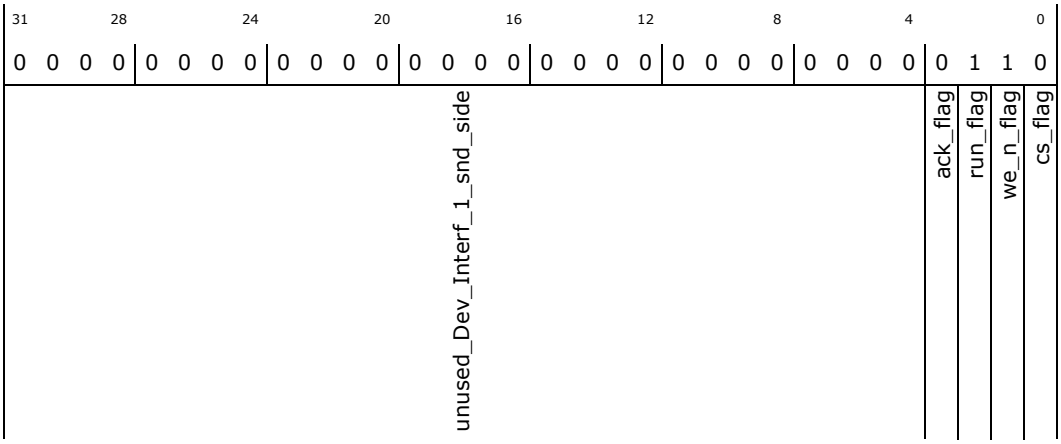
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_1_snd_side: [ISPMMADR] + 43104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_1_snd_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	1h RO	**run_flag:** Run flag
1	1h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

3.7.569 reg_isp_dma_Dev_Interf_2_snd_side_type (isp_dma_Dev_Interf_2_snd_side)—Offset 43108h

DMA Device interface 2 output side status

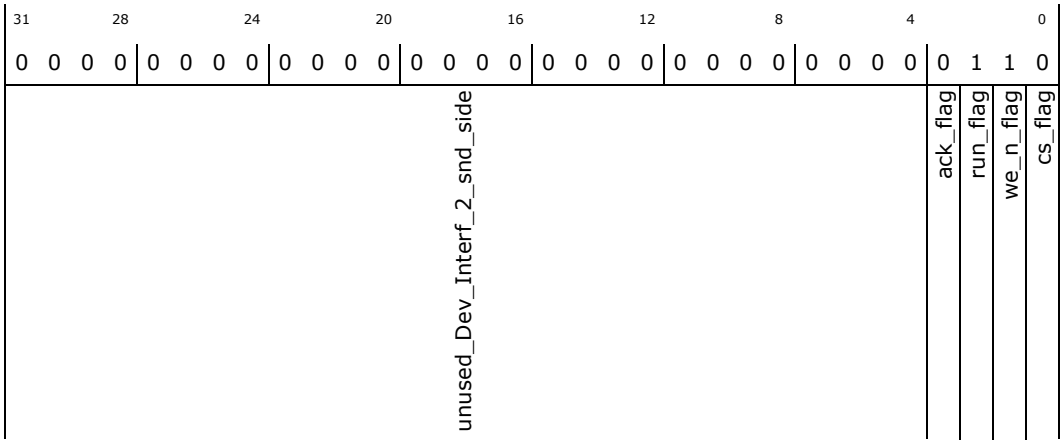
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_2_snd_side: [ISPMMADR] + 43108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_2_snd_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	1h RO	**run_flag:** Run flag
1	1h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

3.7.570 reg_isp_dma_Dev_Interf_0_Fifo_status_type (isp_dma_Dev_Interf_0_Fifo_status)—Offset 43200h

Device Interface 0 Fifo status

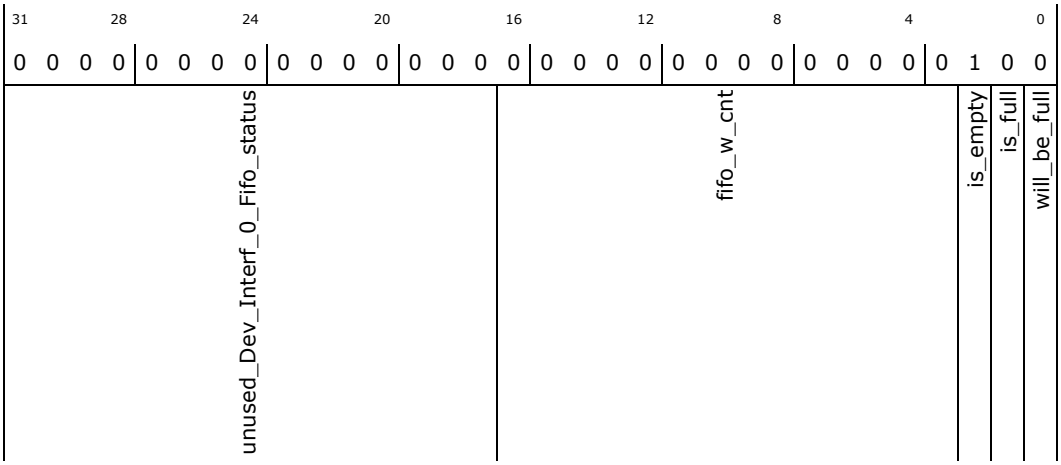
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_0_Fifo_status: [ISPMMADR] + 43200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_Dev_Interf_0_Fifo_status:** Unused
16:3	0h RO	**fifo_w_cnt:** Fifo word counter
2	1h RO	**is_empty:** Fifo is empty
1	0h RO	**is_full:** Fifo is full
0	0h RO	**will_be_full:** Fifo will be full

3.7.571 reg_isp_dma_Dev_Interf_1_Fifo_status_type (isp_dma_Dev_Interf_1_Fifo_status)—Offset 43204h

Device Interface 1 Fifo status

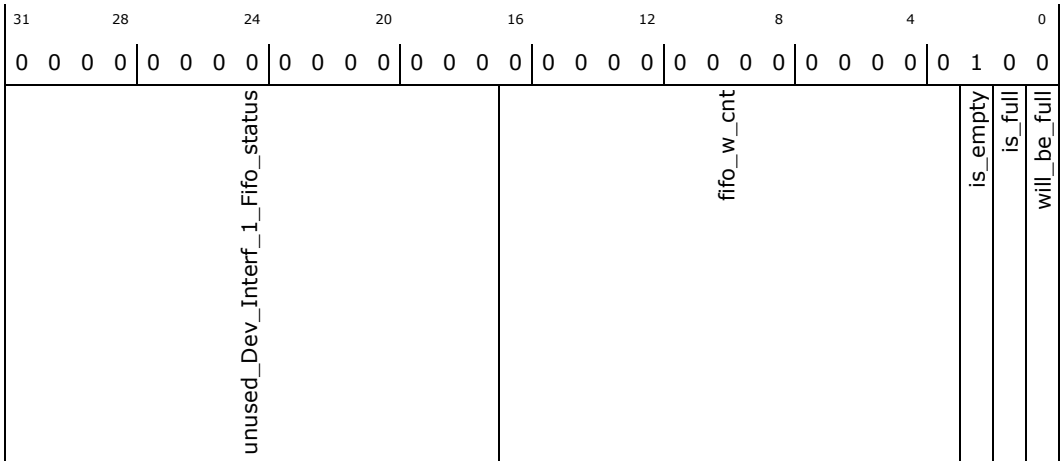
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_1_Fifo_status: [ISPMMADR] + 43204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_Dev_Interf_1_Fifo_status:** Unused
16:3	0h RO	**fifo_w_cnt:** Fifo word counter
2	1h RO	**is_empty:** Fifo is empty
1	0h RO	**is_full:** Fifo is full
0	0h RO	**will_be_full:** Fifo will be full

3.7.572 reg_isp_dma_Dev_Interf_2_Fifo_status_type (isp_dma_Dev_Interf_2_Fifo_status)—Offset 43208h

Device Interface 2 Fifo status

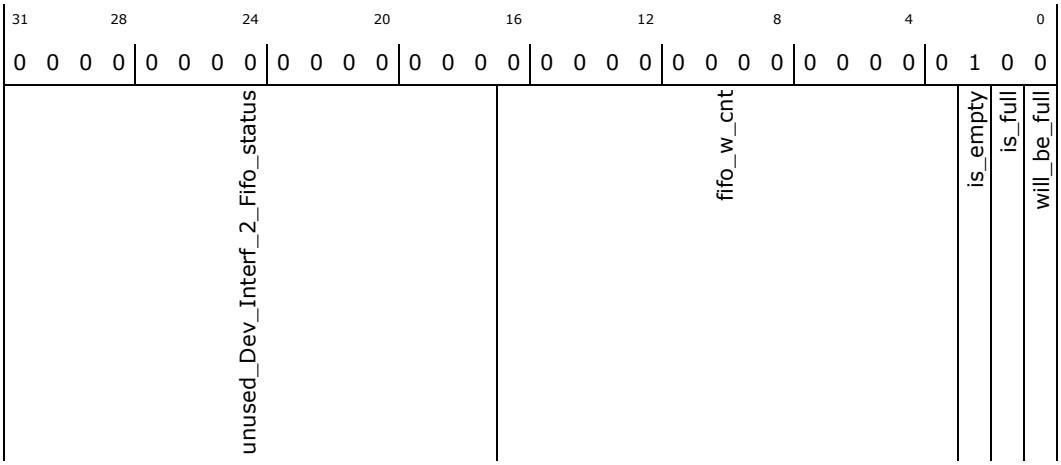
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_2_Fifo_status: [ISPMMADR] + 43208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_Dev_Interf_2_Fifo_status:** Unused
16:3	0h RO	**fifo_w_cnt:** Fifo word counter
2	1h RO	**is_empty:** Fifo is empty
1	0h RO	**is_full:** Fifo is full
0	0h RO	**will_be_full:** Fifo will be full

3.7.573 reg_isp_dma_Dev_Interf_0_Req_complete_bust_type (isp_dma_Dev_Interf_0_Req_complete_bust)—Offset 43300h

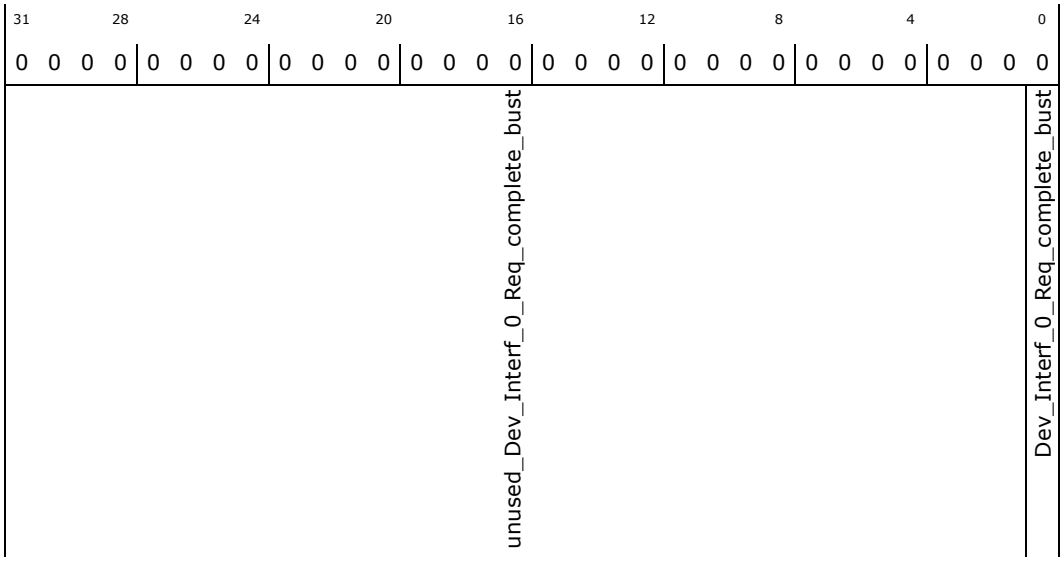
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_0_Req_complete_bust: [ISPMMADR] + 43300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_Dev_Interf_0_Req_complete_bust:** Unused
0	0h RW	**Dev_Interf_0_Req_complete_bust:** DMA Device interface 0 Request only complete burst

3.7.574 reg_isp_dma_Dev_Interf_1_Req_complete_bust_type (isp_dma_Dev_Interf_1_Req_complete_bust)—Offset 43304h

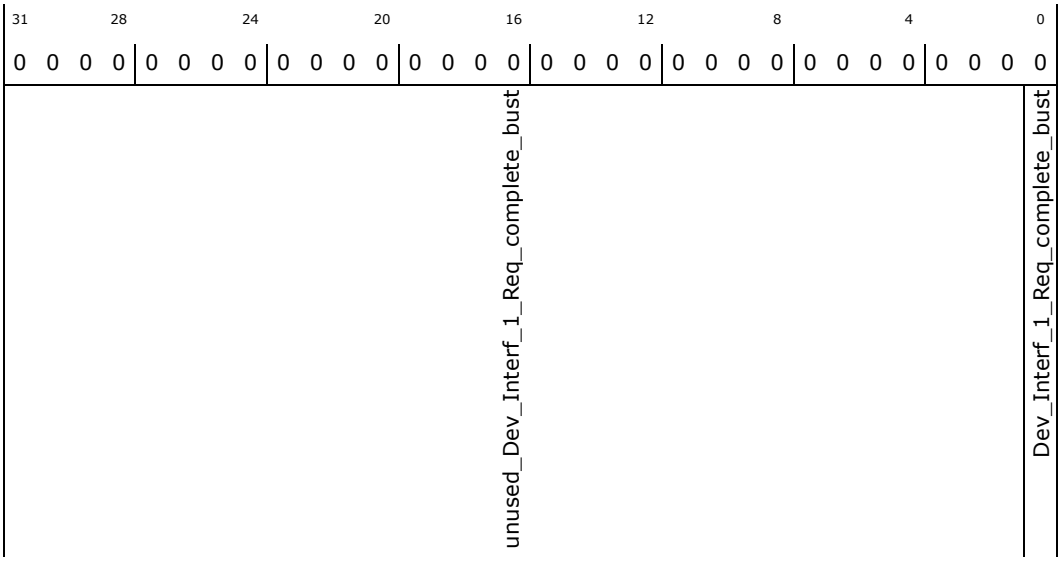
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_1_Req_complete_bust: [ISPMMADR] + 43304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_Dev_Interf_1_Req_complete_bust:** Unused
0	0h RW	**Dev_Interf_1_Req_complete_bust:** DMA Device interface 1 Request only complete burst

3.7.575 reg_isp_dma_Dev_Interf_2_Req_complete_bust_type (isp_dma_Dev_Interf_2_Req_complete_bust)—Offset 43308h

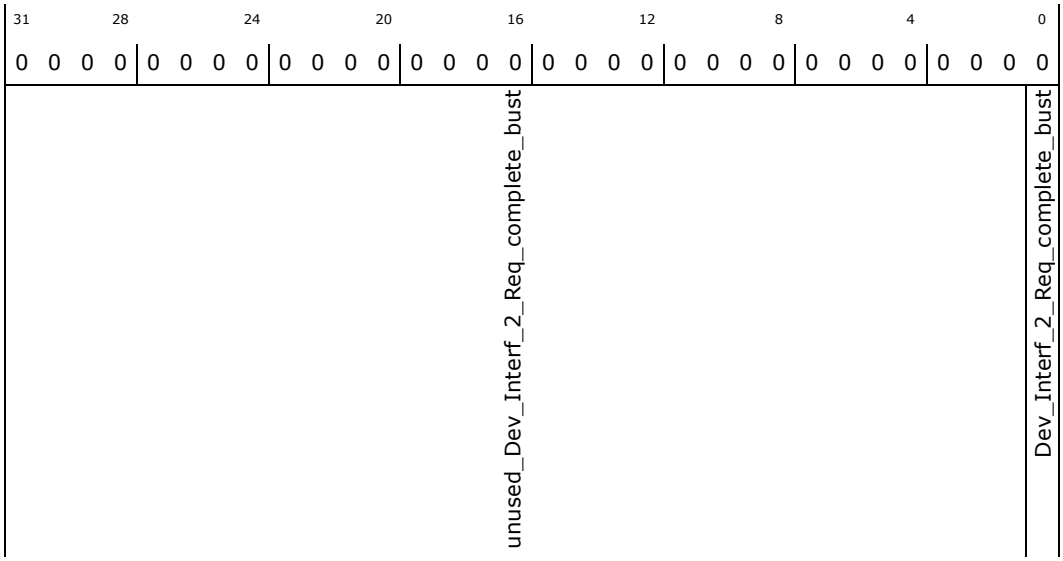
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_2_Req_complete_bust: [ISPMMADR] + 43308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_Dev_Interf_2_Req_complete_bust:** Unused
0	0h RW	**Dev_Interf_2_Req_complete_bust:** DMA Device interface 2 Request only complete burst

3.7.576 reg_isp_dma_Dev_Interf_2_Max_burst_Size_type (isp_dma_Dev_Interf_2_Max_burst_Size)—Offset 43408h

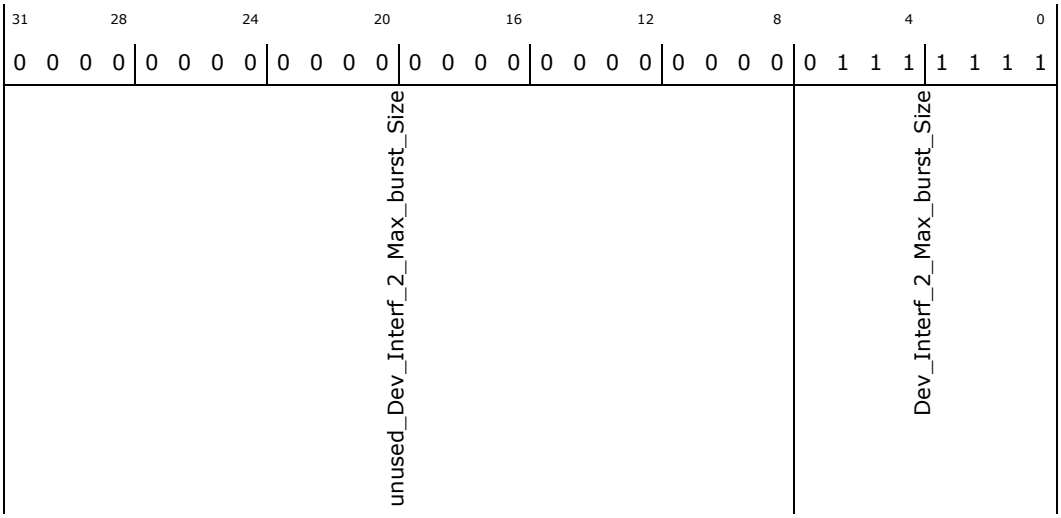
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_2_Max_burst_Size: [ISPMMADR] + 43408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:8	0h RW	**unused_Dev_Interf_2_Max_burst_Size:** Unused
7:0	7Fh RW	**Dev_Interf_2_Max_burst_Size:** DMA Device interface 2 max burst size

3.7.577 reg_gdc1_reg0_type (gdc1_reg0)—Offset 50000h

Status register: Current opx, opy, top-level FSM state

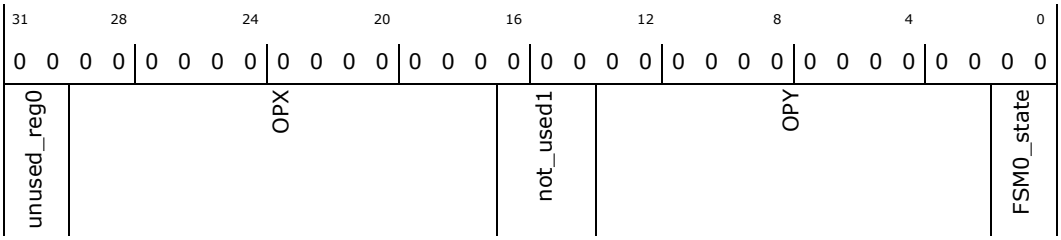
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_reg0: [ISPMMADR] + 50000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**unused_reg0:** Unused

Bit Range	Default & Access	Description
29:17	0h RO	**OPX:** OPX value
16:14	0h RO	**not_used1:** N/A
13:2	0h RO	**OPY:** OPY value
1:0	0h RO	**FSM0_state:** FSM0 state: 00=Idle ; 01=Busy-receiving data needed to kick the device ; 10=Busy-wait state ; 11=Busy-run state

3.7.578 reg_gdc1_woi_x_type (gdc1_woi_x)—Offset 50004h

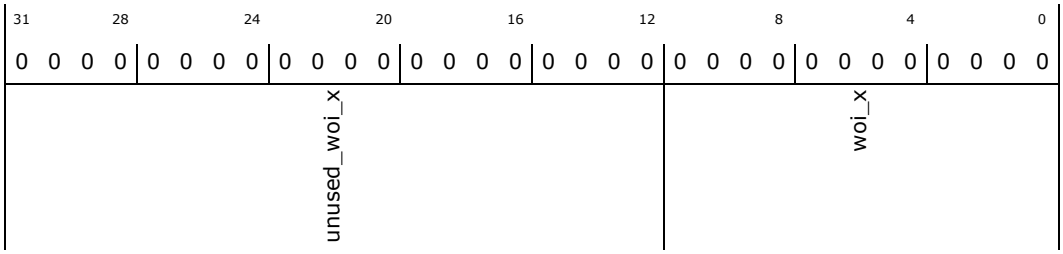
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_woi_x: [ISPMMADR] + 50004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_woi_x:** Unused
11:0	0h RO	**woi_x:** Configured X dimension of the internal window-of-interest (local memory)

3.7.579 reg_gdc1_woi_y_type (gdc1_woi_y)—Offset 50008h

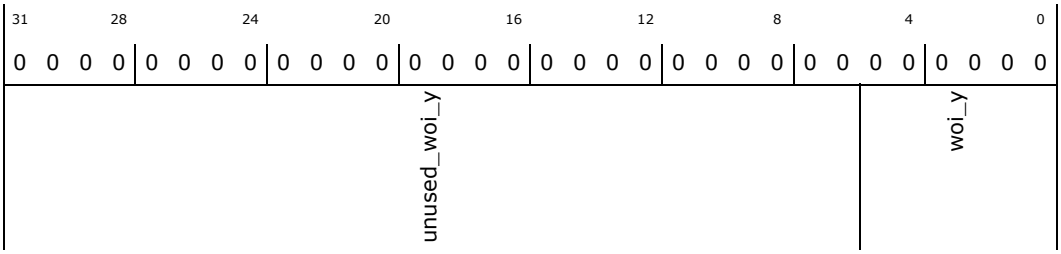
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_woi_y: [ISPMMADR] + 50008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_woi_y:** Unused
5:0	0h RO	**woi_y:** Configured Y dimension of the internal window-of-interest (local memory)

3.7.580 reg_gdc1_bpp_type (gdc1_bpp)—Offset 5000Ch

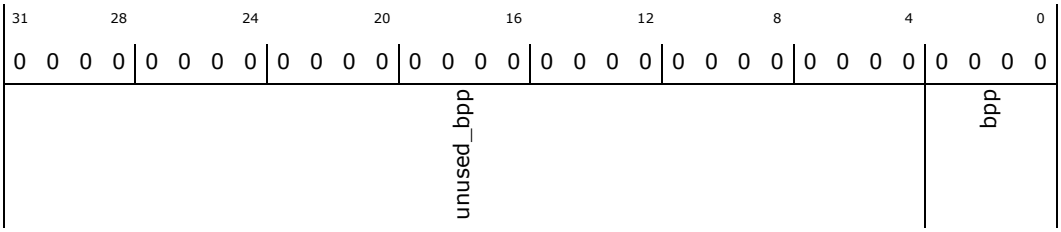
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_bpp: [ISPMMADR] + 5000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_bpp:** Unused
3:0	0h RW	**bpp:** Bits per input/output pixel, allowed: 8, 10, 12, 14

3.7.581 reg_gdc1_fryipxfrx_start_type (gdc1_fryipxfrx_start)—Offset 50010h

Fractional component of the starting X and Y position for scaling given in fixed point notation

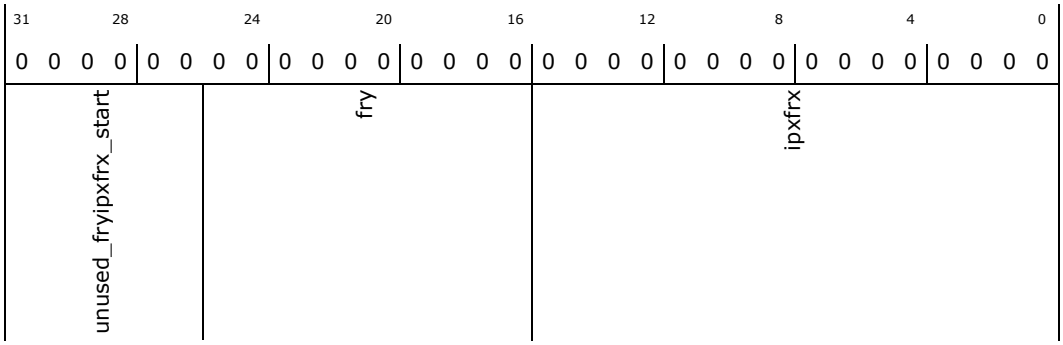
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_fryipxfrx_start: [ISPMMADR] + 50010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0h RW	**unused_fryipxfrx_start:** Unused
25:16	0h RW	**fry:** Fractional component of the Y start
15:0	0h RW	**ipxfrx:** Integer (6) and Fractional (10) component of the X start

3.7.582 reg_gdc1_oxdim_type (gdc1_oxdim)—Offset 50014h

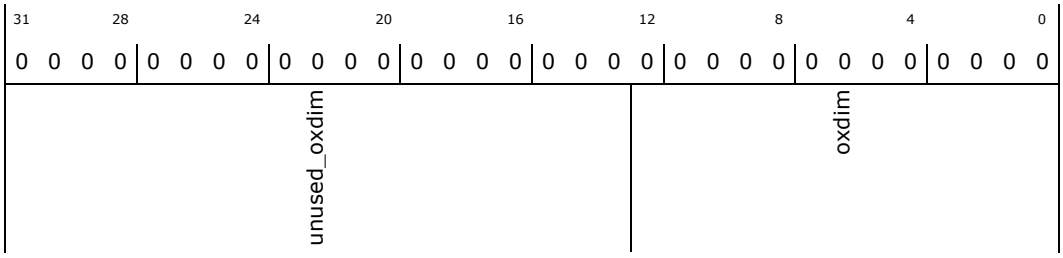
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_oxdim: [ISPMMADR] + 50014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:13	0h RW	**unused_oxdim:** Unused

Bit Range	Default & Access	Description
12:0	0h RW	**oxdim:** Output X dimension of the produced block of pixels

3.7.583 reg_gdc1_oydim_type (gdc1_oydim)—Offset 50018h

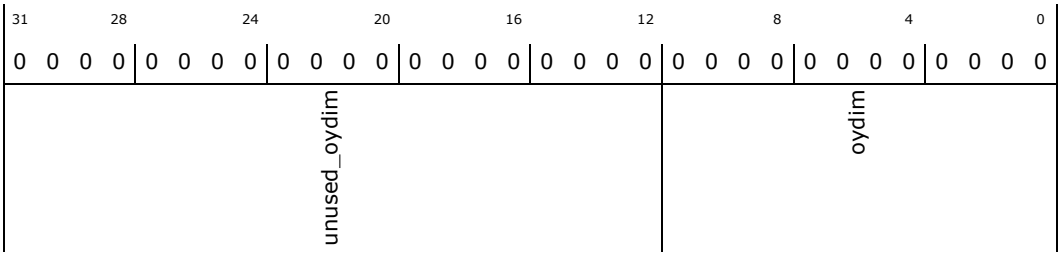
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_oydim: [ISPMMADR] + 50018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_oydim:** Unused
11:0	0h RW	**oydim:** Output Y dimension of the produced block of pixels

3.7.584 reg_gdc1_src_addr_type (gdc1_src_addr)—Offset 5001Ch

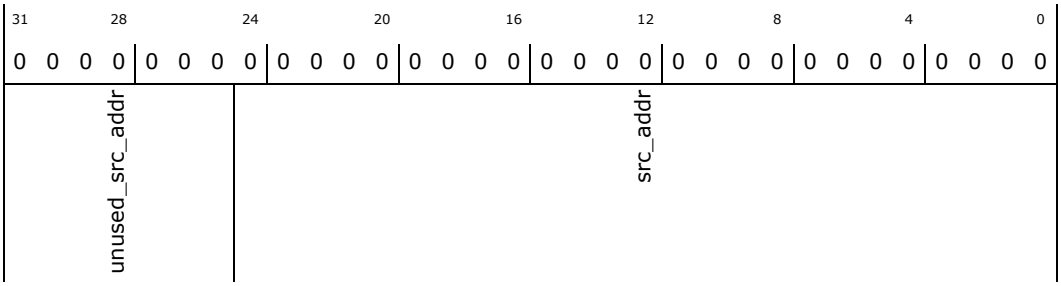
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_src_addr: [ISPMMADR] + 5001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_addr:** Unused
24:0	0h RW	**src_addr:** Source (input) pixel base address [byte-based]

3.7.585 reg_gdc1_src_end_type (gdc1_src_end)—Offset 50020h

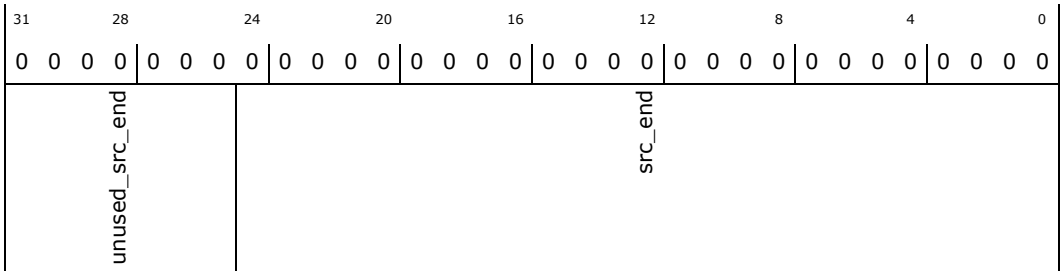
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_src_end: [ISPMMADR] + 50020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_end:** Unused
24:0	0h RW	**src_end:** End address. When reached wrap around. [byte-based]

3.7.586 reg_gdc1_src_wrap_type (gdc1_src_wrap)—Offset 50024h

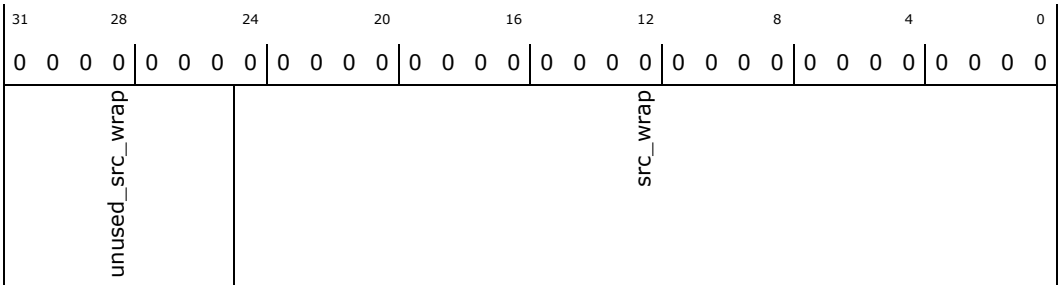
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_src_wrap: [ISPMMADR] + 50024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_wrap:** Unused
24:0	0h RW	**src_wrap:** Wrap addr. Wrap here when src_end reached [byte-based]

3.7.587 reg_gdc1_src_stride_type (gdc1_src_stride)—Offset 50028h

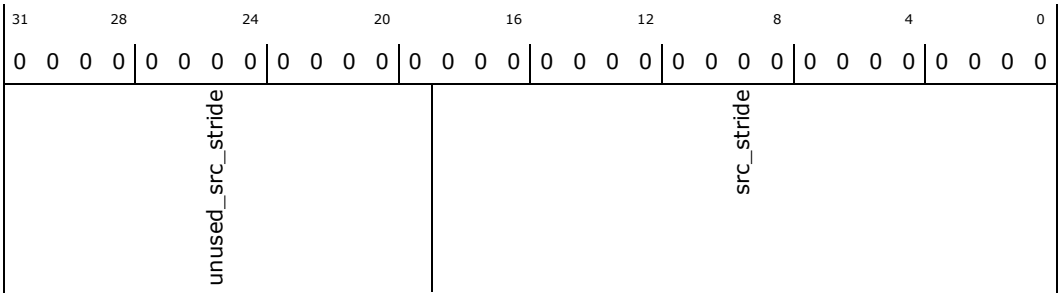
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_src_stride: [ISPMMADR] + 50028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_src_stride:** Unused
18:0	0h RW	**src_stride:** Source (input) pixel stride [byte-based]

3.7.588 reg_gdc1_dst_addr_type (gdc1_dst_addr)—Offset 5002Ch

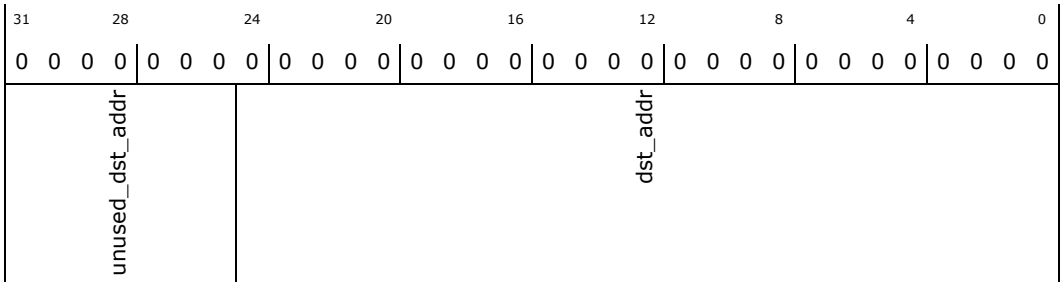
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_dst_addr: [ISPMMADR] + 5002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RW	**unused_dst_addr:** Unused
24:0	0h RW	**dst_addr:** Destination (output) pixel base address [byte-based]

3.7.589 reg_gdc1_dst_stride_type (gdc1_dst_stride)—Offset 50030h

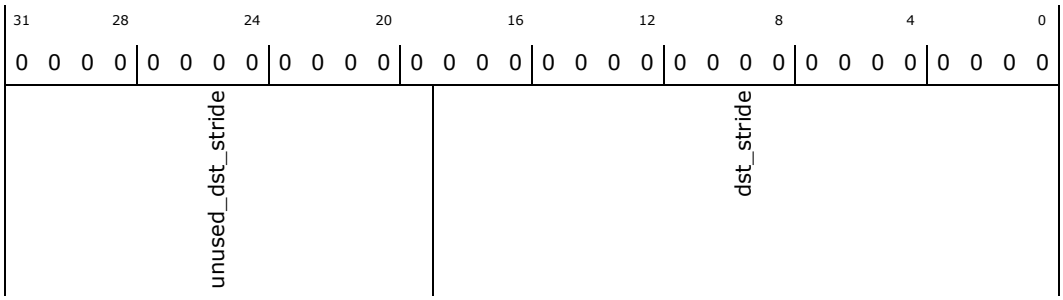
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_dst_stride: [ISPMMADR] + 50030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_dst_stride:** Unused
18:0	0h RW	**dst_stride:** Destination (output) pixel stride [byte-based]

3.7.590 reg_gdc1_dx_type (gdc1_dx)—Offset 50034h

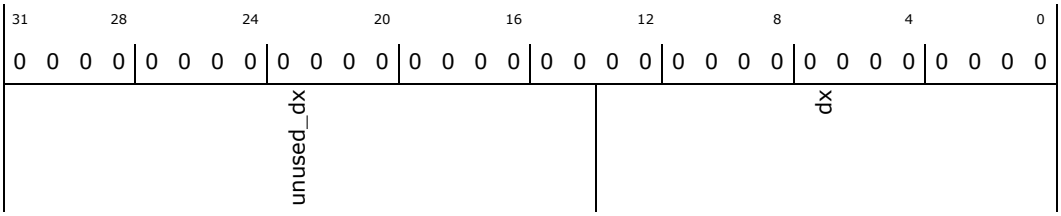
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_dx: [ISPMMADR] + 50034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_dx:** Unused
13:0	0h RW	**dx:** Scaling only: Horizontal scaling factor

3.7.591 reg_gdc1_dy_type (gdc1_dy)—Offset 50038h

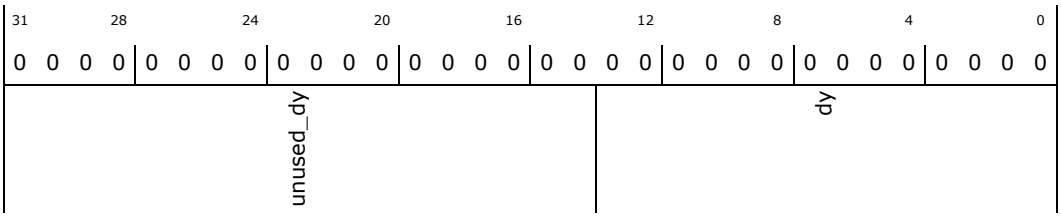
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_dy: [ISPMMADR] + 50038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_dy:** Unused
13:0	0h RW	**dy:** Scaling only: Vertical scaling factor

3.7.592 reg_gdc1_P0_primX_ixdim_type (gdc1_P0_primX_ixdim)—Offset 5003Ch

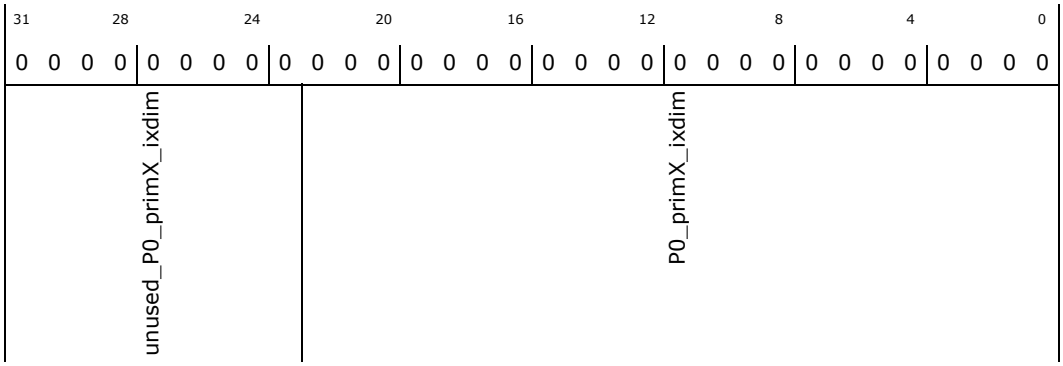
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_P0_primX_ixdim: [ISPMMADR] + 5003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RW	**unused_P0_primX_ixdim:** Unused
22:0	0h RW	**P0_primX_ixdim:** P0(X) Tetragon mode: top-left coordinate (X), Scaling mode: dimension of the input region (X), fixed point notation, 13.10

3.7.593 reg_gdc1_P0_primY_iydim_type (gdc1_P0_primY_iydim)—Offset 50040h

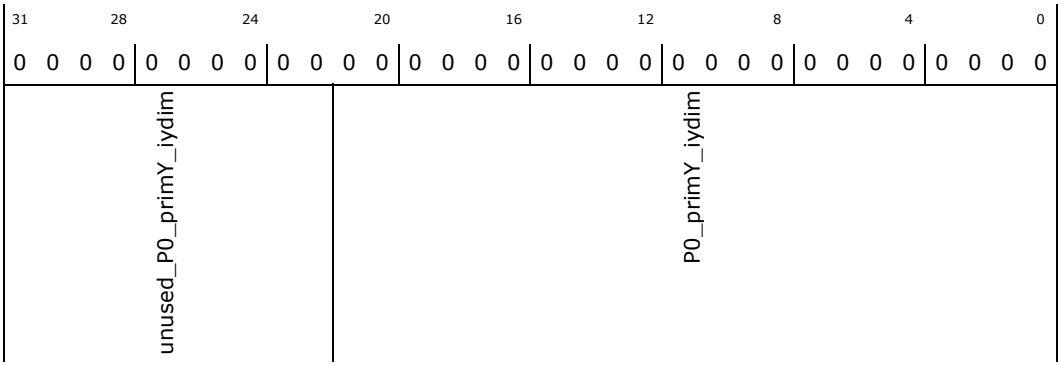
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_P0_primY_iydim: [ISPMMADR] + 50040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_P0_primY_iydim:** Unused
21:0	0h RW	**P0_primY_iydim:** P0(Y) Tetragon mode: top-left coordinate (Y), Scaling mode: dimension of the input region (Y), fixed point notation, 12.10

3.7.594 reg_gdc1_P1_primX_type (gdc1_P1_primX)—Offset 50044h

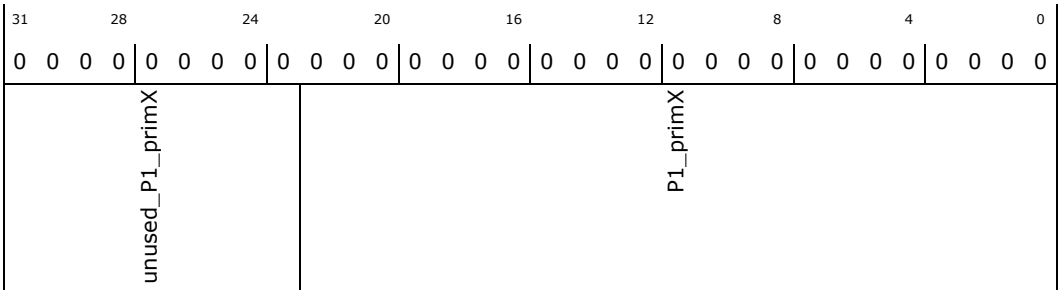
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_P1_primX: [ISPMMADR] + 50044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RW	**unused_P1_primX:** Unused
22:0	0h RW	**P1_primX:** P1(X) Tetragon mode only: top-right coordinate (X), fixed point notation, 13.10

3.7.595 reg_gdc1_P1_primY_type (gdc1_P1_primY)—Offset 50048h

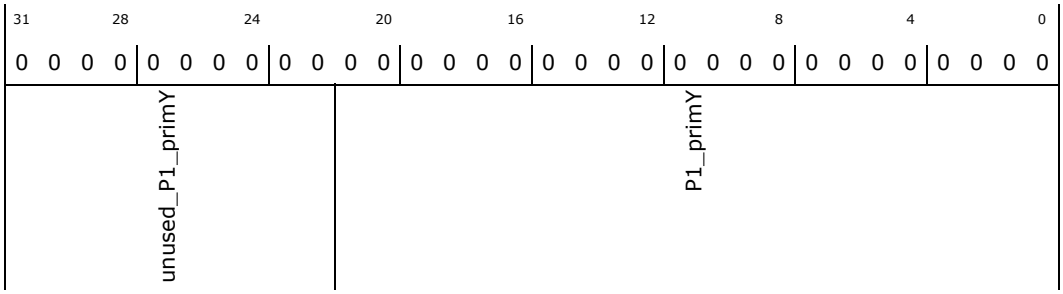
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_P1_primY: [ISPMMADR] + 50048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_P1_primY:** Unused
21:0	0h RW	**P1_primY:** P1(Y) Tetragon mode only: top-right coordinate (Y), fixed point notation, 12.10

3.7.596 reg_gdc1_P2_primX_type (gdc1_P2_primX)—Offset 5004Ch

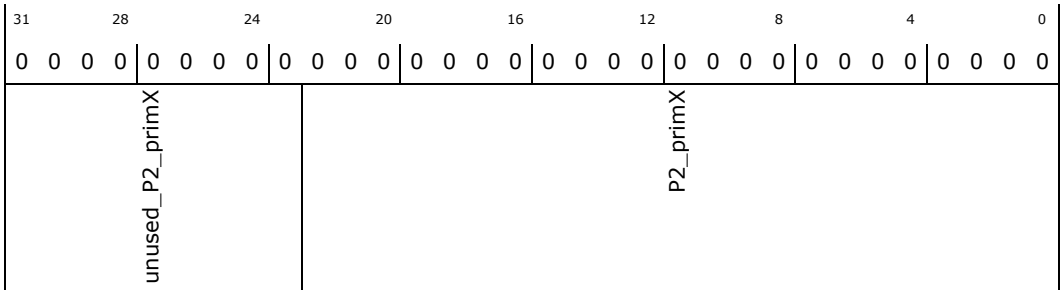
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_P2_primX: [ISPMMADR] + 5004Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RW	**unused_P2_primX:** Unused
22:0	0h RW	**P2_primX:** P2(X) Tetragon mode only: bottom-left coordinate (X), fixed point notation, 13.10

3.7.597 reg_gdc1_P2_primY_type (gdc1_P2_primY)—Offset 50050h

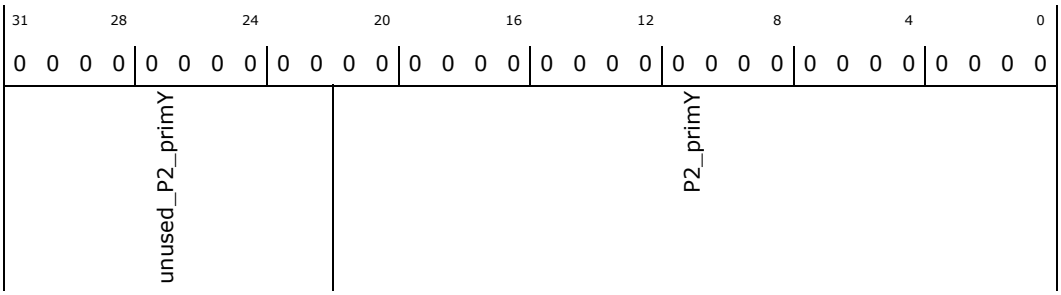
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_P2_primY: [ISPMMADR] + 50050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_P2_primY:** Unused
21:0	0h RW	**P2_primY:** P2(Y) Tetragon mode only: bottom-left coordinate (Y), fixed point notation, 12.10

3.7.598 reg_gdc1_P3_primX_type (gdc1_P3_primX)—Offset 50054h

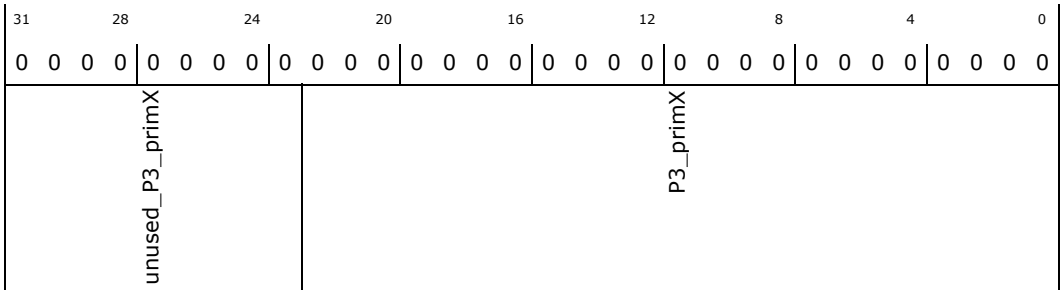
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_P3_primX: [ISPMMADR] + 50054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RW	**unused_P3_primX:** Unused
22:0	0h RW	**P3_primX:** P3(X) Tetragon mode only: bottom-right coordinate (X), fixed point notation, 13.10

3.7.599 reg_gdc1_P3_primY_type (gdc1_P3_primY)—Offset 50058h

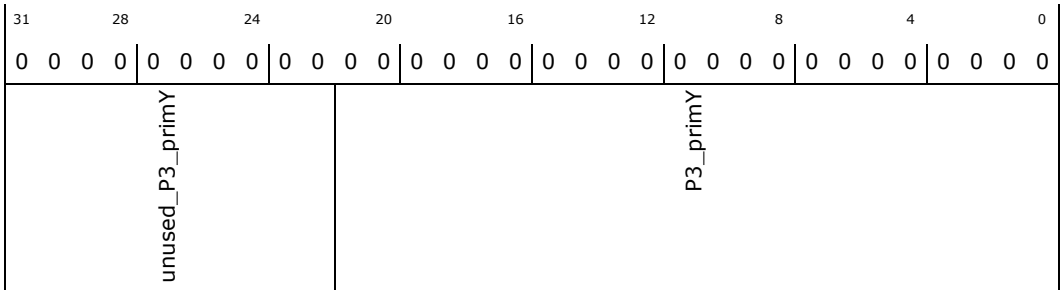
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_P3_primY: [ISPMMADR] + 50058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_P3_primY:** Unused
21:0	0h RW	**P3_primY:** P3(Y) Tetragon mode only: bottom-right coordinate (Y), fixed point notation, 12.10

3.7.600 reg_gdc1_perf_mode_type (gdc1_perf_mode)—Offset 5005Ch

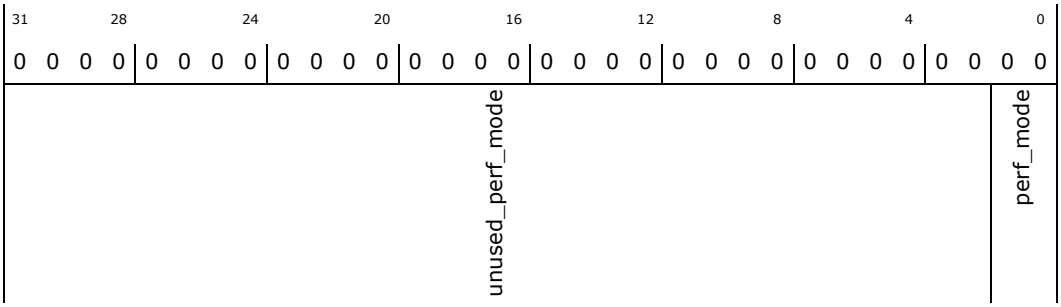
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_perf_mode: [ISPMMADR] + 5005Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_perf_mode:** Unused
1:0	0h RW	**perf_mode:** Number and location of pixels produced per clock cycle: 00=1x1 pixels ; 01=2x1 pixels ; 10=1x2 pixels ; 11=2x2 pixels

3.7.601 reg_gdc1_interp_type_type (gdc1_interp_type)—Offset 50060h

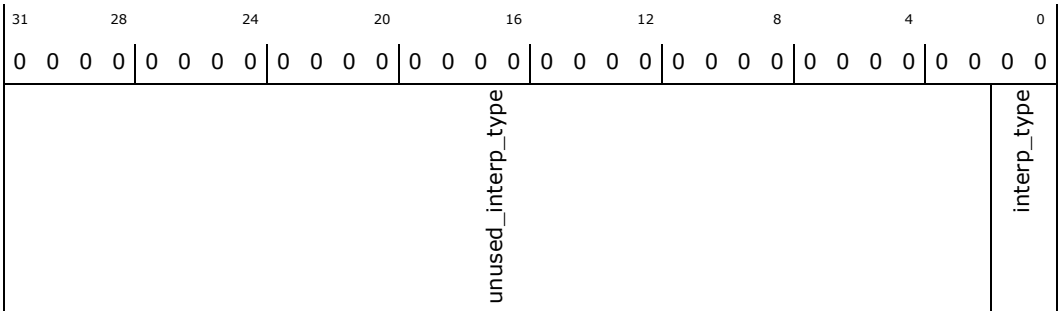
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_interp_type: [ISPMMADR] + 50060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_interp_type:** Unused

Bit Range	Default & Access	Description
1:0	0h RW	**interp_type:** Type of interpolation: 00=NND ; 01=BLI ; 10=BCI ; 11=LUT

3.7.602 reg_gdc1_scan_mode_type (gdc1_scan_mode)—Offset 50064h

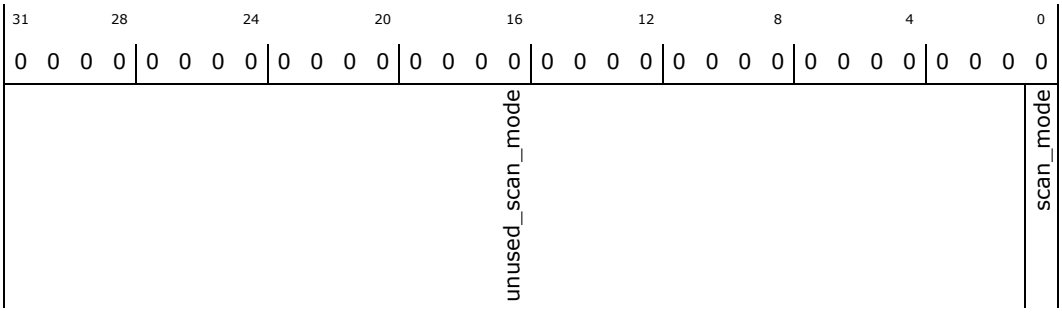
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_scan_mode: [ISPMMADR] + 50064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_scan_mode:** Unused
0	0h RW	**scan_mode:** Scanning mode: 0 = STB (Slide To Bottom) ; 1 = STR (Slide To Right)

3.7.603 reg_gdc1_proc_mode_type (gdc1_proc_mode)—Offset 50068h

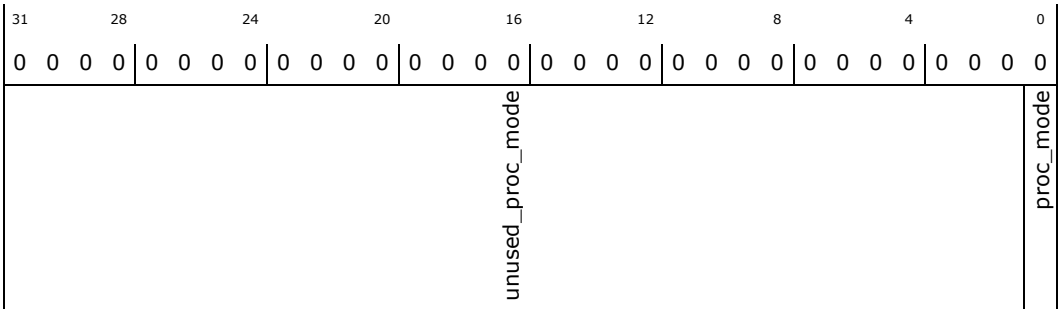
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_proc_mode: [ISPMMADR] + 50068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_proc_mode:** Unused
0	0h RW	**proc_mode:** Processing mode: 0 = Rectangular-based scaling ; 1 = Tetragon-based scaling

3.7.604 reg_gdc2_reg0_type (gdc2_reg0)—Offset 60000h

Status register: Current opx, opy, top-level FSM state

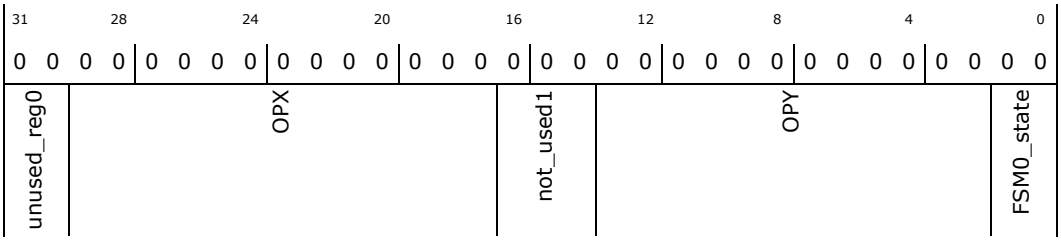
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_reg0: [ISPMMADR] + 60000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**unused_reg0:** Unused
29:17	0h RO	**OPX:** OPX value
16:14	0h RO	**not_used1:** N/A
13:2	0h RO	**OPY:** OPY value
1:0	0h RO	**FSM0_state:** FSM0 state: 00=Idle ; 01=Busy-receiving data needed to kick the device ; 10=Busy-wait state ; 11=Busy-run state

3.7.605 reg_gdc2_woi_x_type (gdc2_woi_x)—Offset 60004h

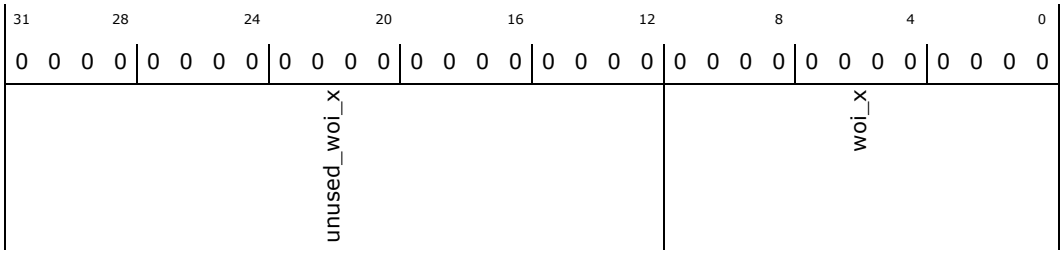
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_woi_x: [ISPMMADR] + 60004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_woi_x:** Unused
11:0	0h RO	**woi_x:** Configured X dimension of the internal window-of-interest (local memory)

3.7.606 reg_gdc2_woi_y_type (gdc2_woi_y)—Offset 60008h

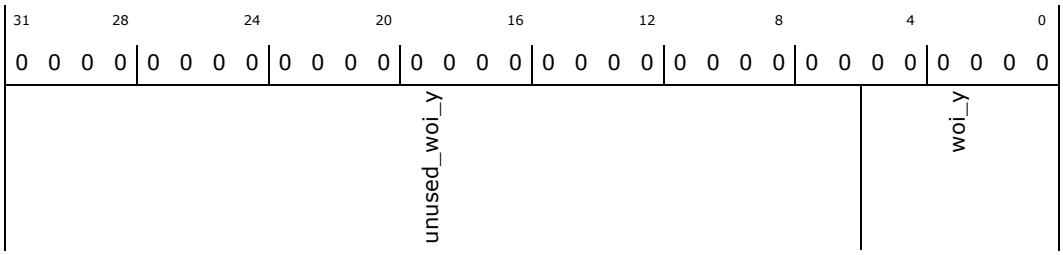
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_woi_y: [ISPMMADR] + 60008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_woi_y:** Unused
5:0	0h RO	**woi_y:** Configured Y dimension of the internal window-of-interest (local memory)

3.7.607 reg_gdc2_bpp_type (gdc2_bpp)—Offset 6000Ch

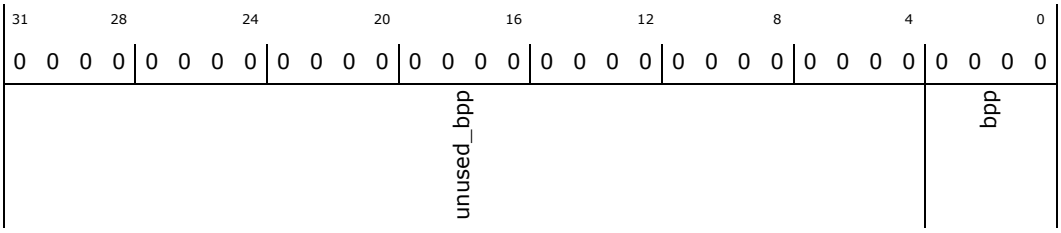
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_bpp: [ISPMMADR] + 6000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_bpp:** Unused
3:0	0h RW	**bpp:** Bits per input/output pixel, allowed: 8, 10, 12, 14

3.7.608 reg_gdc2_fryipxfrx_start_type (gdc2_fryipxfrx_start)—Offset 60010h

Fractional component of the starting X and Y position for scaling given in fixed point notation

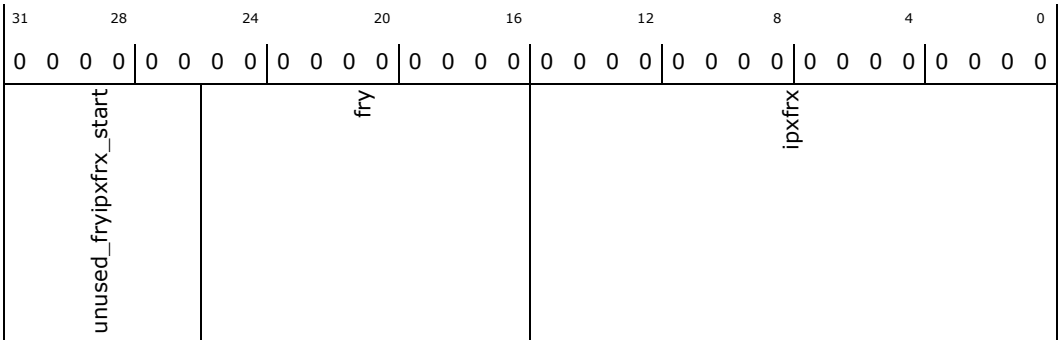
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_fryipxfrx_start: [ISPMMADR] + 60010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0h RW	**unused_fryipxfrx_start:** Unused
25:16	0h RW	**fry:** Fractional component of the Y start
15:0	0h RW	**ipxfrx:** Integer (6) and Fractional (10) component of the X start

3.7.609 reg_gdc2_oxdim_type (gdc2_oxdim)—Offset 60014h

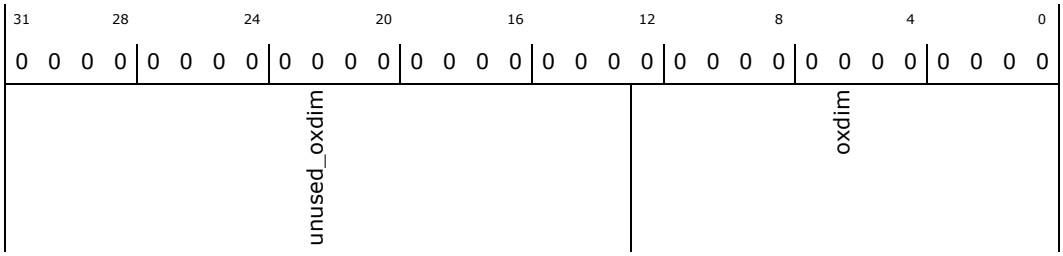
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_oxdim: [ISPMMADR] + 60014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:13	0h RW	**unused_oxdim:** Unused
12:0	0h RW	**oxdim:** Output X dimension of the produced block of pixels

3.7.610 reg_gdc2_oydim_type (gdc2_oydim)—Offset 60018h

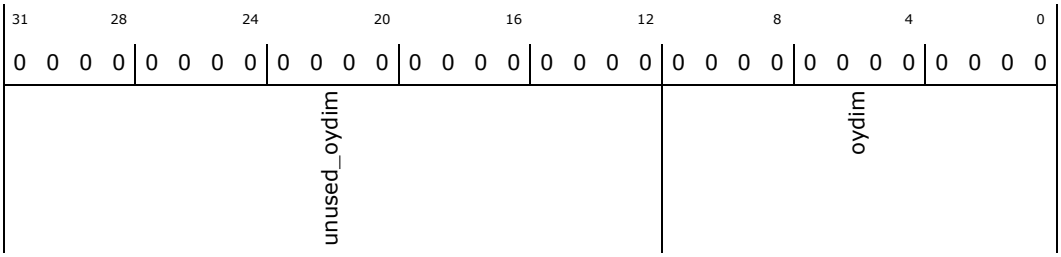
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_oydim: [ISPMMADR] + 60018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_oydim:** Unused
11:0	0h RW	**oydim:** Output Y dimension of the produced block of pixels

3.7.611 reg_gdc2_src_addr_type (gdc2_src_addr)—Offset 6001Ch

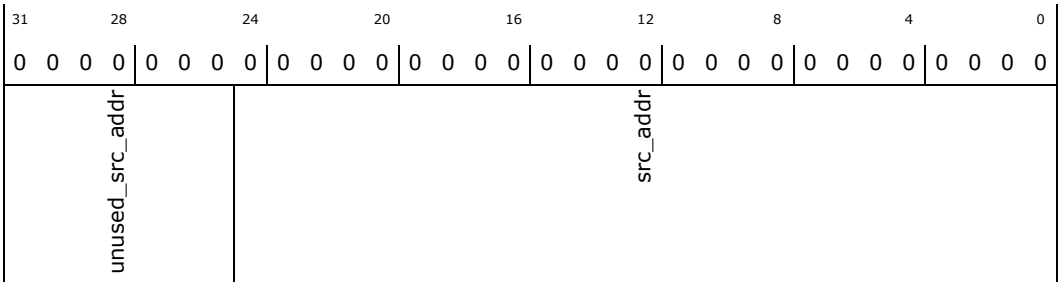
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_src_addr: [ISPMMADR] + 6001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_addr:** Unused
24:0	0h RW	**src_addr:** Source (input) pixel base address [byte-based]

3.7.612 reg_gdc2_src_end_type (gdc2_src_end)—Offset 60020h

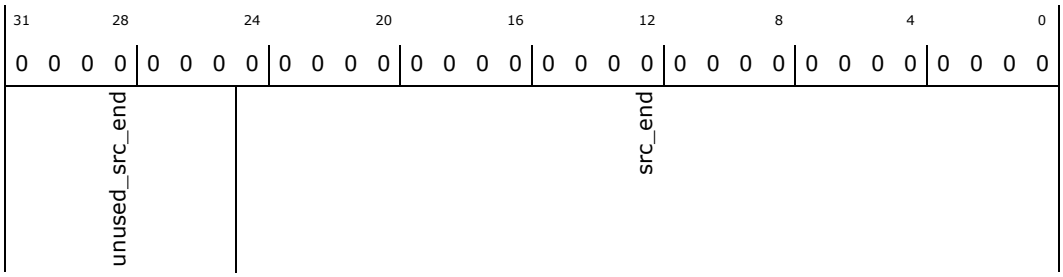
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_src_end: [ISPMMADR] + 60020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_end:** Unused
24:0	0h RW	**src_end:** End address. When reached wrap around. [byte-based]

3.7.613 reg_gdc2_src_wrap_type (gdc2_src_wrap)—Offset 60024h

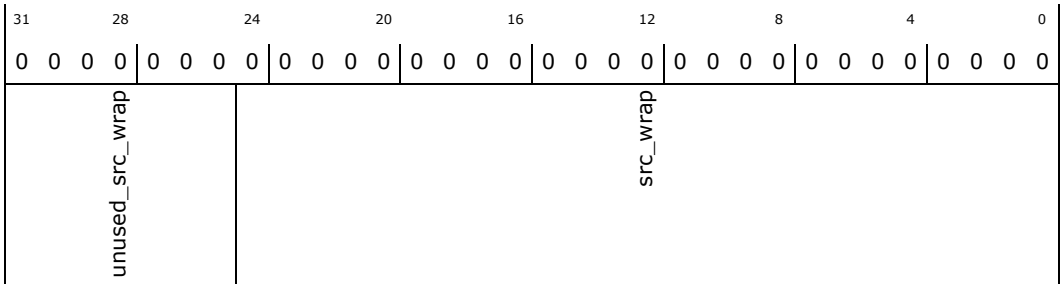
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_src_wrap: [ISPMMADR] + 60024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_wrap:** Unused
24:0	0h RW	**src_wrap:** Wrap addr. Wrap here when src_end reached [byte-based]

3.7.614 reg_gdc2_src_stride_type (gdc2_src_stride)—Offset 60028h

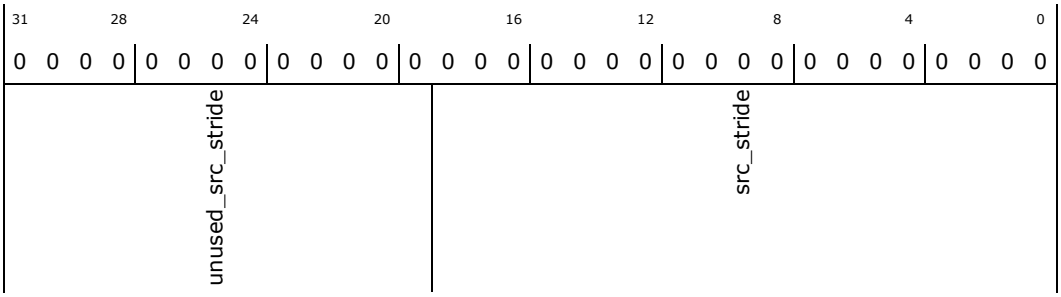
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_src_stride: [ISPMMADR] + 60028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_src_stride:** Unused
18:0	0h RW	**src_stride:** Source (input) pixel stride [byte-based]

3.7.615 reg_gdc2_dst_addr_type (gdc2_dst_addr)—Offset 6002Ch

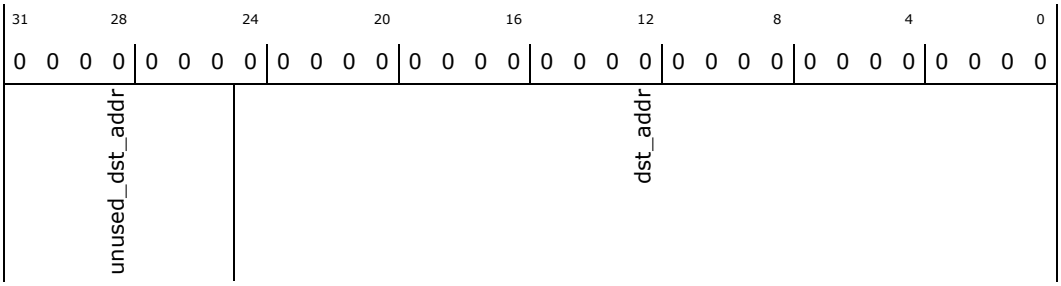
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_dst_addr: [ISPMMADR] + 6002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RW	**unused_dst_addr:** Unused
24:0	0h RW	**dst_addr:** Destination (output) pixel base address [byte-based]

3.7.616 reg_gdc2_dst_stride_type (gdc2_dst_stride)—Offset 60030h

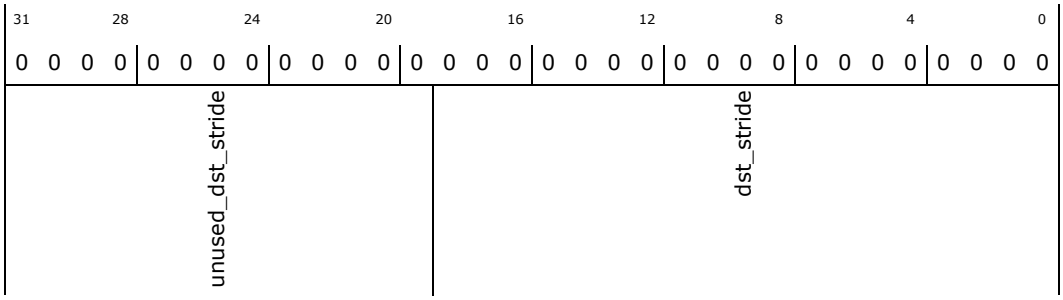
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_dst_stride: [ISPMMADR] + 60030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_dst_stride:** Unused
18:0	0h RW	**dst_stride:** Destination (output) pixel stride [byte-based]

3.7.617 reg_gdc2_dx_type (gdc2_dx)—Offset 60034h

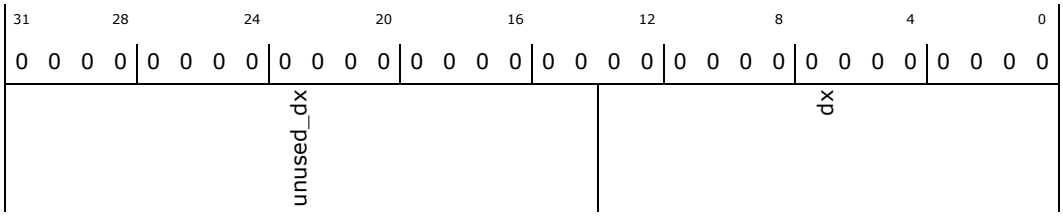
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_dx: [ISPMMADR] + 60034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_dx:** Unused
13:0	0h RW	**dx:** Scaling only: Horizontal scaling factor

3.7.618 reg_gdc2_dy_type (gdc2_dy)—Offset 60038h

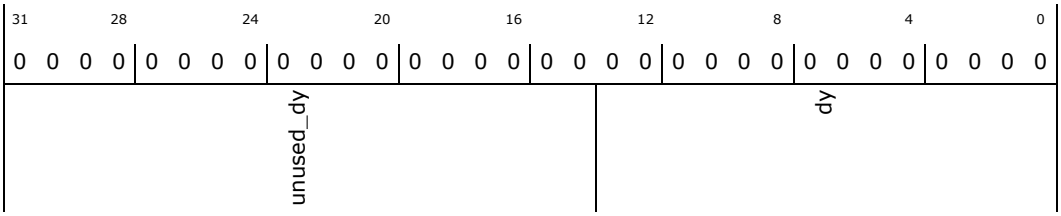
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_dy: [ISPMMADR] + 60038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_dy:** Unused
13:0	0h RW	**dy:** Scaling only: Vertical scaling factor

3.7.619 reg_gdc2_P0_primX_ixdim_type (gdc2_P0_primX_ixdim)—Offset 6003Ch

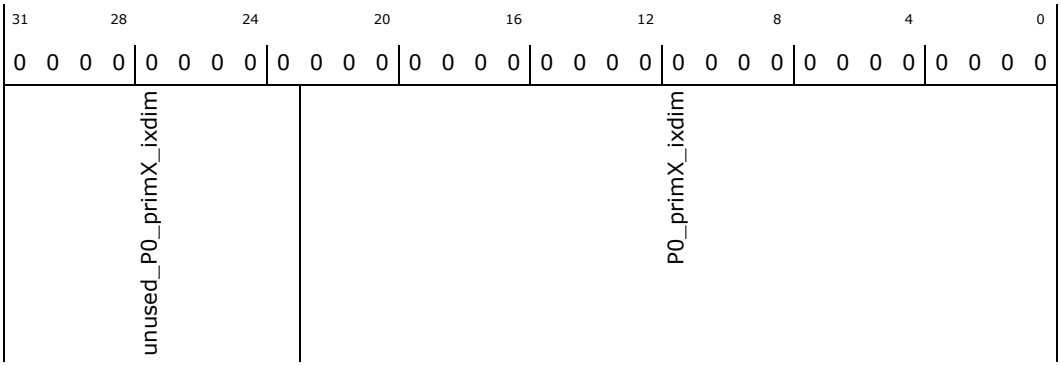
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P0_primX_ixdim: [ISPMMADR] + 6003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RW	**unused_P0_primX_ixdim:** Unused
22:0	0h RW	**P0_primX_ixdim:** P0(X) Tetragon mode: top-left coordinate (X), Scaling mode: dimension of the input region (X), fixed point notation, 13.10

3.7.620 reg_gdc2_P0_primY_iydim_type (gdc2_P0_primY_iydim)—Offset 60040h

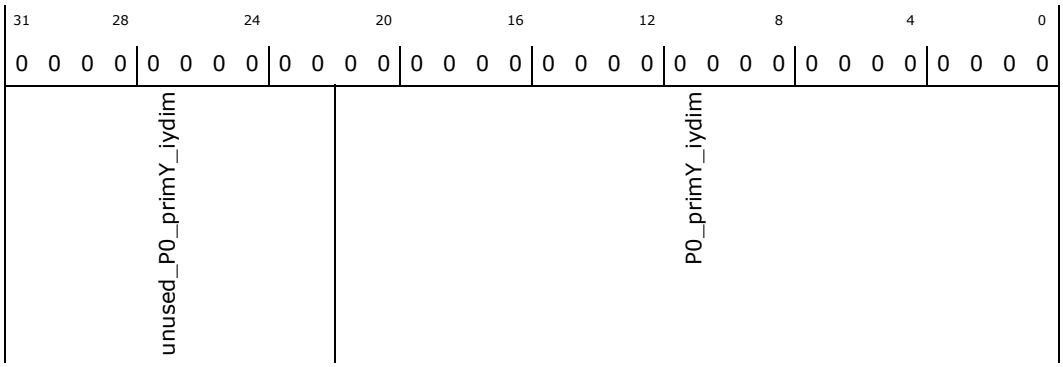
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P0_primY_iydim: [ISPMMADR] + 60040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_P0_primY_iydim:** Unused
21:0	0h RW	**P0_primY_iydim:** P0(Y) Tetragon mode: top-left coordinate (Y), Scaling mode: dimension of the input region (Y), fixed point notation, 12.10

3.7.621 reg_gdc2_P1_primX_type (gdc2_P1_primX)—Offset 60044h

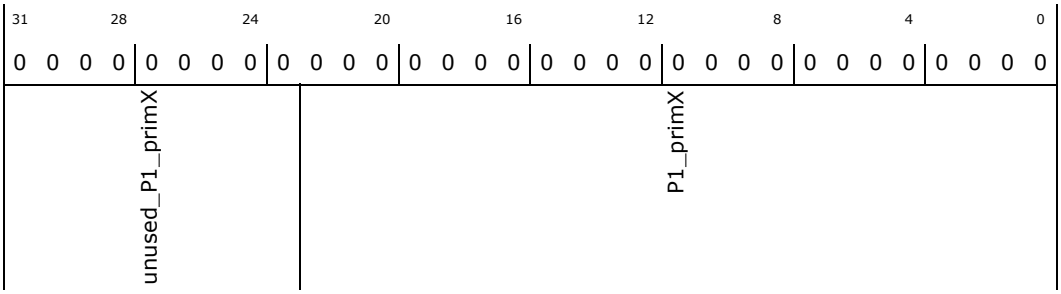
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P1_primX: [ISPMMADR] + 60044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RW	**unused_P1_primX:** Unused
22:0	0h RW	**P1_primX:** P1(X) Tetragon mode only: top-right coordinate (X), fixed point notation, 13.10

3.7.622 reg_gdc2_P1_primY_type (gdc2_P1_primY)—Offset 60048h

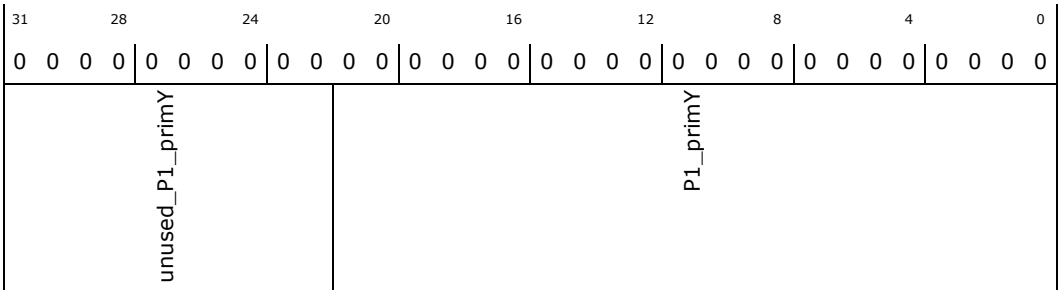
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P1_primY: [ISPMMADR] + 60048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_P1_primY:** Unused
21:0	0h RW	**P1_primY:** P1(Y) Tetragon mode only: top-right coordinate (Y), fixed point notation, 12.10

3.7.623 reg_gdc2_P2_primX_type (gdc2_P2_primX)—Offset 6004Ch

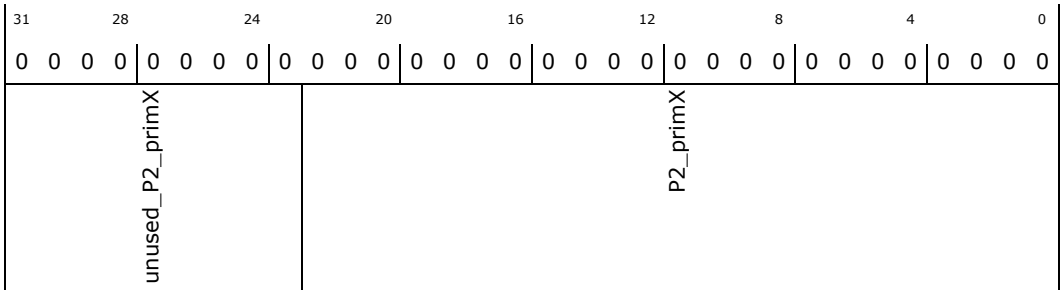
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P2_primX: [ISPMMADR] + 6004Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RW	**unused_P2_primX:** Unused
22:0	0h RW	**P2_primX:** P2(X) Tetragon mode only: bottom-left coordinate (X), fixed point notation, 13.10

3.7.624 reg_gdc2_P2_primY_type (gdc2_P2_primY)—Offset 60050h

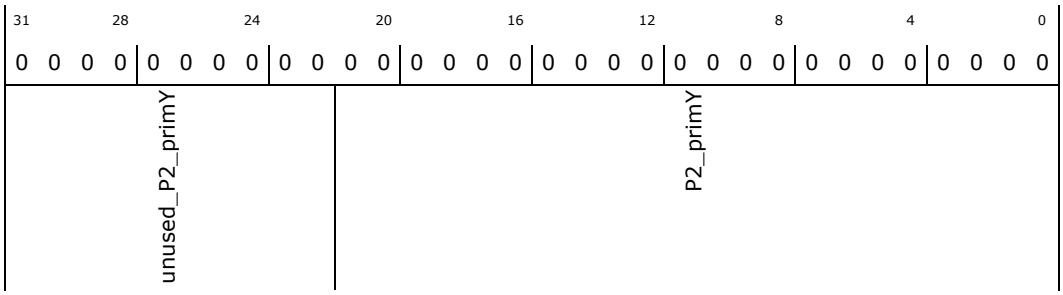
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P2_primY: [ISPMMADR] + 60050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_P2_primY:** Unused
21:0	0h RW	**P2_primY:** P2(Y) Tetragon mode only: bottom-left coordinate (Y), fixed point notation, 12.10

3.7.625 reg_gdc2_P3_primX_type (gdc2_P3_primX)—Offset 60054h

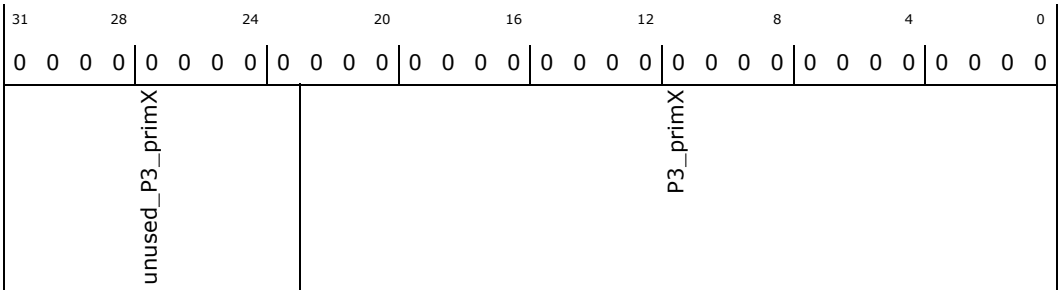
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P3_primX: [ISPMMADR] + 60054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RW	**unused_P3_primX:** Unused
22:0	0h RW	**P3_primX:** P3(X) Tetragon mode only: bottom-right coordinate (X), fixed point notation, 13.10

3.7.626 reg_gdc2_P3_primY_type (gdc2_P3_primY)—Offset 60058h

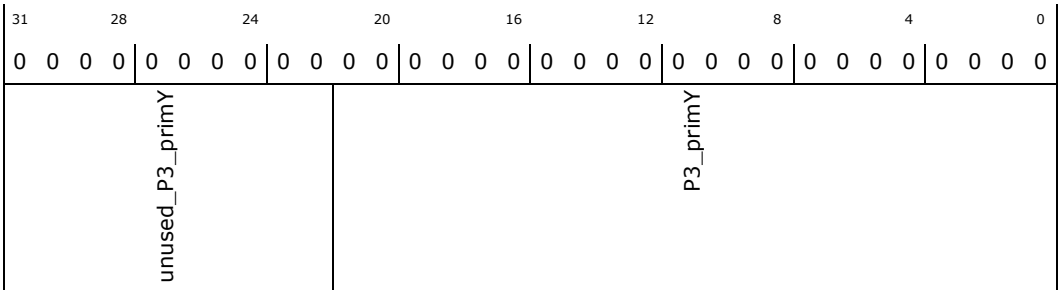
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P3_primY: [ISPMMADR] + 60058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_P3_primY:** Unused
21:0	0h RW	**P3_primY:** P3(Y) Tetragon mode only: bottom-right coordinate (Y), fixed point notation, 12.10

3.7.627 reg_gdc2_perf_mode_type (gdc2_perf_mode)—Offset 6005Ch

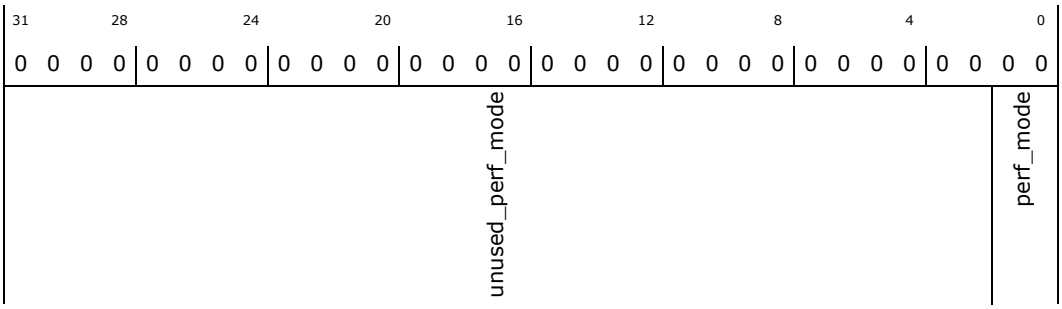
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_perf_mode: [ISPMMADR] + 6005Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_perf_mode:** Unused
1:0	0h RW	**perf_mode:** Number and location of pixels produced per clock cycle: 00=1x1 pixels ; 01=2x1 pixels ; 10=1x2 pixels ; 11=2x2 pixels

3.7.628 reg_gdc2_interp_type_type (gdc2_interp_type)—Offset 60060h

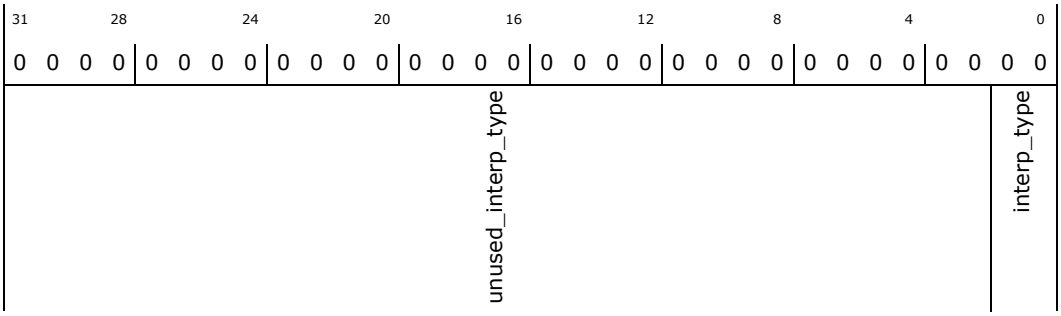
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_interp_type: [ISPMMADR] + 60060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_interp_type:** Unused
1:0	0h RW	**interp_type:** Type of interpolation: 00=NND ; 01=BLI ; 10=BCI ; 11=LUT

3.7.629 reg_gdc2_scan_mode_type (gdc2_scan_mode)—Offset 60064h

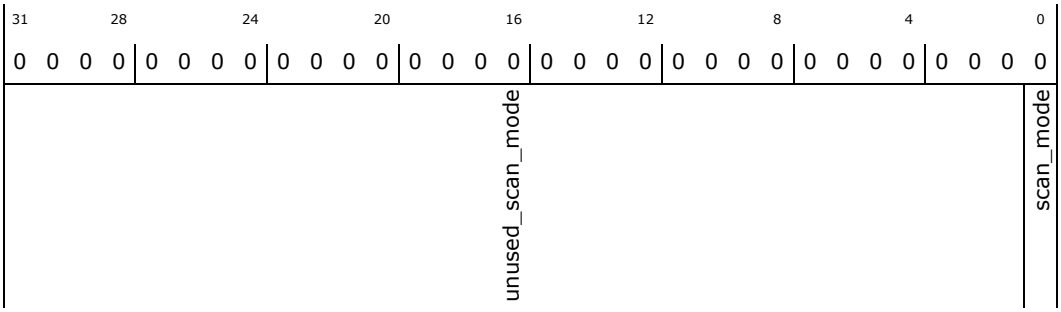
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_scan_mode: [ISPMMADR] + 60064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_scan_mode:** Unused
0	0h RW	**scan_mode:** Scanning mode: 0 = STB (Slide To Bottom) ; 1 = STR (Slide To Right)

3.7.630 reg_gdc2_proc_mode_type (gdc2_proc_mode)—Offset 60068h

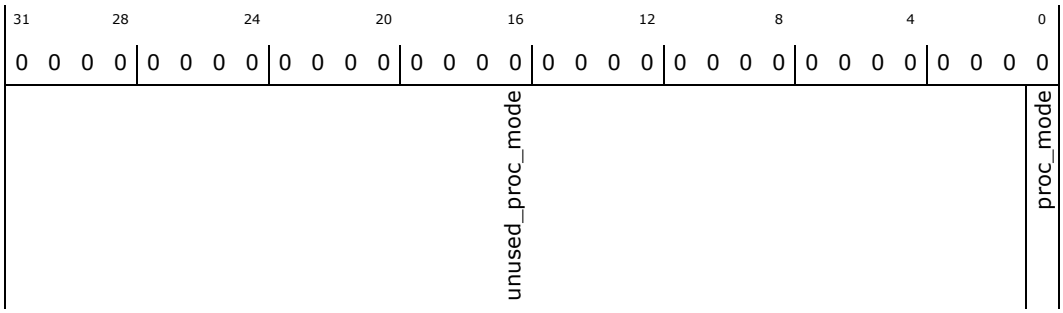
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_proc_mode: [ISPMMADR] + 60068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_proc_mode:** Unused
0	0h RW	**proc_mode:** Processing mode: 0 = Rectangular-based scaling ; 1 = Tetragon-based scaling

3.7.631 reg_data_out_sys_c_mmu_MMU_invalidate_cache_type (data_out_sys_c_mmu_MMU_invalidate_cache)—Offset 70000h

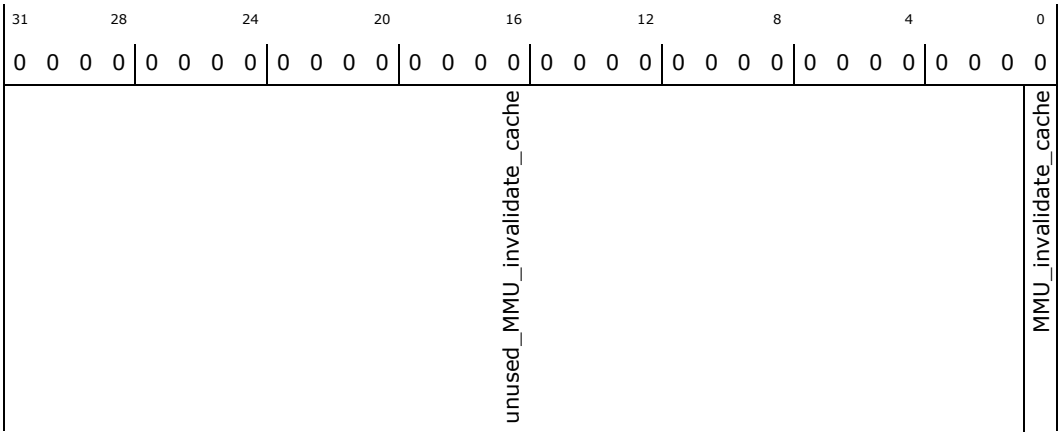
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

data_out_sys_c_mmu_MMU_invalidate_cache: [ISPMMADR] + 70000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MMU_invalidate_cache:** Unused
0	0h WO	**MMU_invalidate_cache:** MMU invalidate cache. When '1', the MMUs TLB is invalidated.

3.7.632 reg_data_out_sys_c_mmu_MMU_page_table_base_type (data_out_sys_c_mmu_MMU_page_table_base)—Offset 70004h

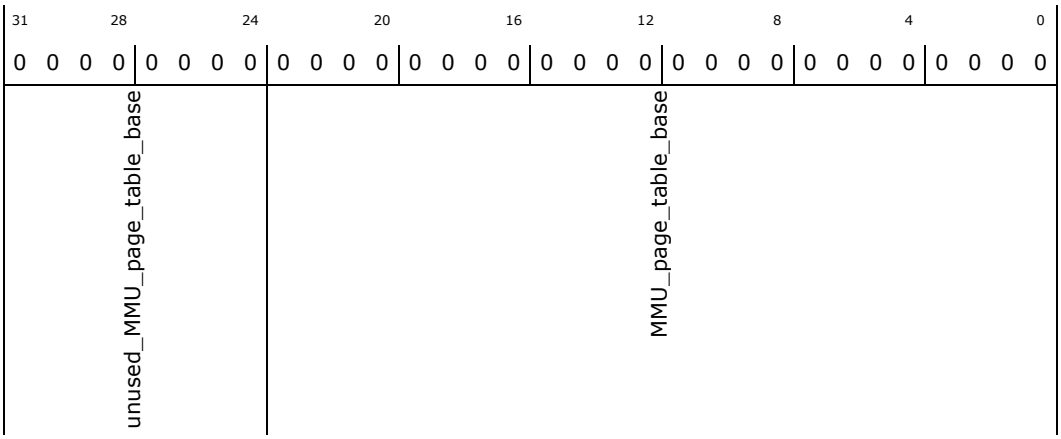
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

data_out_sys_c_mmu_MMU_page_table_base: [ISPMMADR] + 70004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_MMU_page_table_base:** Unused
23:0	0h RW	**MMU_page_table_base:** Defines the physical page number of the page tables

3.7.633 reg_inp_sys_csi_receiver_csi1_dev_ready_type (inp_sys_csi_receiver_csi1_dev_ready)—Offset 80100h

Set after programming operational registers to enable receiver

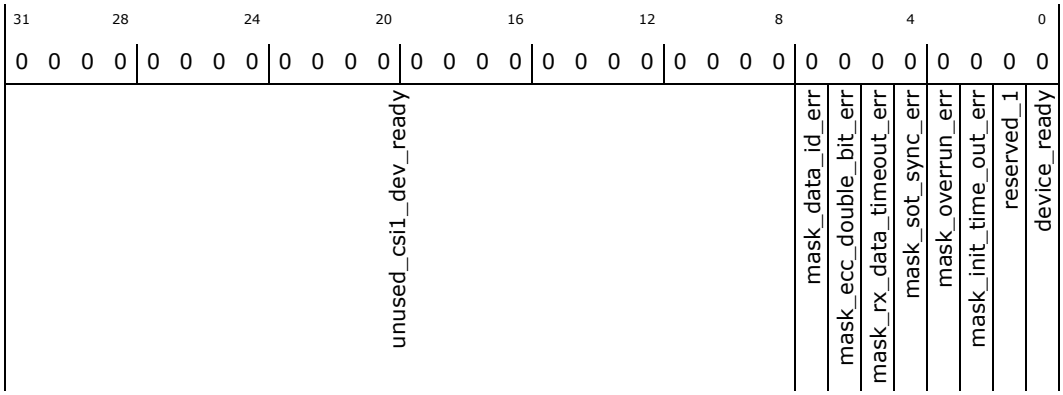
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_dev_ready: [ISPMMADR] + 80100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi1_dev_ready:** Unused
7	0h RW	**mask_data_id_err:** Set to mask error recovery when data ID error is detected
6	0h RW	**mask_ecc_double_bit_err:** Set to mask error recovery when ECC double bit error is detected
5	0h RW	**mask_rx_data_timeout_err:** Set to mask error recovery when receive data time out error is detected
4	0h RW	**mask_sot_sync_err:** Set to mask error recovery when start of transmission sync error is detected
3	0h RW	**mask_overrun_err:** set to mask overrun: NOT used now, can be discarded

Bit Range	Default & Access	Description
2	0h RW	**mask_init_time_out_err:** Set to mask error recovery when initialization time out error is detected
1	0h RO	**reserved_1:** Reserved
0	0h RW	**device_ready:** Set to indicate that device is ready for reception

3.7.634 reg_inp_sys_csi_receiver_csi1_int_status_type (inp_sys_csi_receiver_csi1_int_status)—Offset 80104h

Interrupt Status

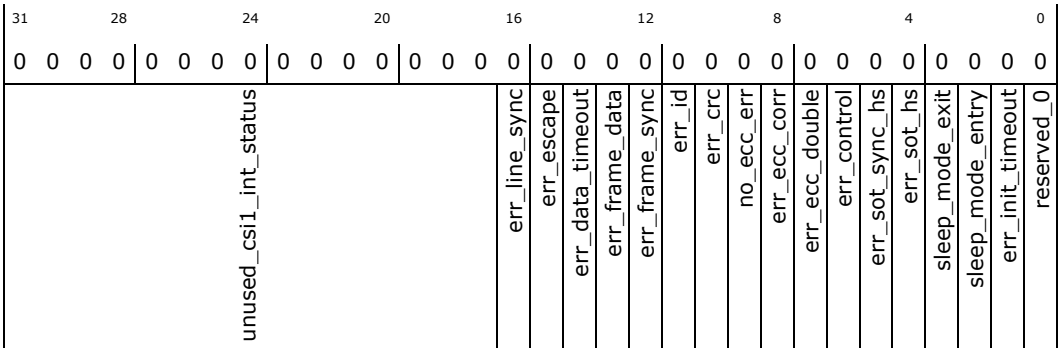
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_int_status: [ISPMMADR] + 80104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi1_int_status:** Unused
16	0h RW/1C	**err_line_sync:** Set if line number for line start and line end packets do not match
15	0h RW/1C	**err_escape:** Set if an unrecognised escape entry command is received
14	0h RW/1C	**err_data_timeout:** Set if time taken to receive a packet exceeds programmed timeout value
13	0h RW/1C	**err_frame_data:** Set if data packets within a frame has errors
12	0h RW/1C	**err_frame_sync:** Set if frame start is not paired with frame end for same virtual channel

Bit Range	Default & Access	Description
11	0h RW/1C	**err_id:** Set if packet header has a unrecognised data id
10	0h RW/1C	**err_crc:** Set if computed CRC differs from received value
9	0h RW/1C	**no_ecc_err:** Set if no ECC error detected in packet
8	0h RW/1C	**err_ecc_corr:** Set if ECC error detected and corrected for one bit
7	0h RW/1C	**err_ecc_double:** Set if ECC error detected for two or more bits
6	0h RW/1C	**err_control:** Set if DPHY flags a control error
5	0h RW/1C	**err_sot_sync_hs:** Set if DPHY flags start of transmission synchronisation error
4	0h RW/1C	**err_sot_hs:** Set if DPHY flags start of transmission error
3	0h RW/1C	**sleep_mode_exit:** Set if DPHY exits ultra low power state
2	0h RW/1C	**sleep_mode_entry:** Set if DPHY enters ultra low power state
1	0h RW/1C	**err_init_timeout:** Set if Initialization timeout error occurs on DPHY data lanes
0	0h RO	**reserved_0:** Always set to 0

3.7.635 reg_inp_sys_csi_receiver_csi1_int_enable_type (inp_sys_csi_receiver_csi1_int_enable)—Offset 80108h

Interrupt Enable

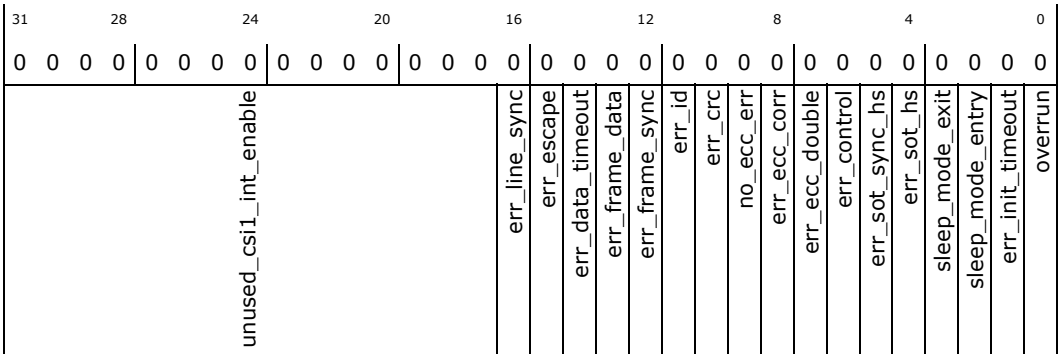
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_int_enable: [ISPMMADR] + 80108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi1_int_enable:** Unused
16	0h RW	**err_line_sync:** Enable line sync error interrupt
15	0h RW	**err_escape:** Enable escape entry error interrupt
14	0h RW	**err_data_timeout:** Enable timeout error interrupt
13	0h RW	**err_frame_data:** Enable frame data error interrupt
12	0h RW	**err_frame_sync:** Enable frame sync error interrupt
11	0h RW	**err_id:** Enable data id error interrupt
10	0h RW	**err_crc:** Enable CRC error interrupt
9	0h RW	**no_ecc_err:** Enable no ECC error interrupt
8	0h RW	**err_ecc_corr:** Enable ECC error detected and corrected for one bit interrupt
7	0h RW	**err_ecc_double:** Enable ECC error detected for two or more bits interrupt
6	0h RW	**err_control:** Enable control error interrupt
5	0h RW	**err_sot_sync_hs:** Enable start of transmission synchronisation error interrupt
4	0h RW	**err_sot_hs:** Enable start of transmission error interrupt
3	0h RW	**sleep_mode_exit:** Enable sleep mode exit interrupt
2	0h RW	**sleep_mode_entry:** Enable sleep mode entry interrupt
1	0h RW	**err_init_timeout:** Enable Initialization timeout error interrupt

Bit Range	Default & Access	Description
0	0h RW	**overrun:** Enable FIFO overrun interrupt: NOT available now, can be discarded

3.7.636 reg_inp_sys_csi_receiver_csi1_func_prg_type (inp_sys_csi_receiver_csi1_func_prg)—Offset 8010Ch

Functional Programming

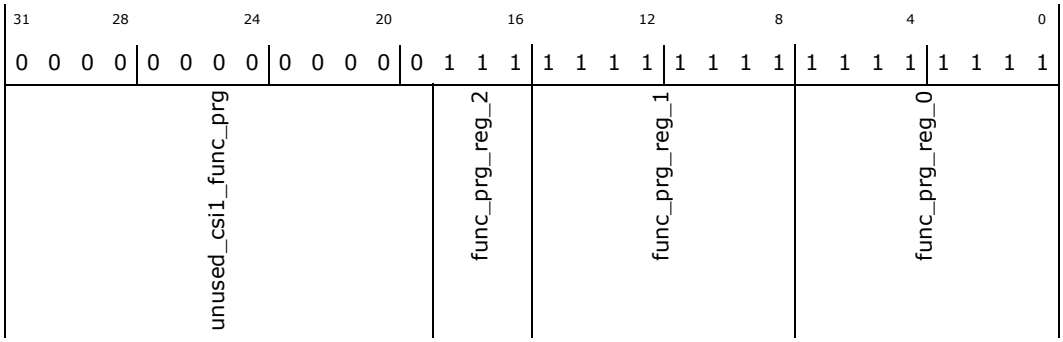
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_func_prg: [ISPMMADR] + 8010Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0007FFFFh



Bit Range	Default & Access	Description
31:19	0h RW	**unused_csi1_func_prg:** Unused
18:16	7h RW	**func_prg_reg_2:** Byte 2 for functional programming
15:8	FFh RW	**func_prg_reg_1:** Byte 1 for functional programming
7:0	FFh RW	**func_prg_reg_0:** Byte 0 for functional programming

3.7.637 reg_inp_sys_csi_receiver_csi1_init_cnt_type (inp_sys_csi_receiver_csi1_init_cnt)—Offset 80110h

Duration after power up when DPHY lanes will not be observed

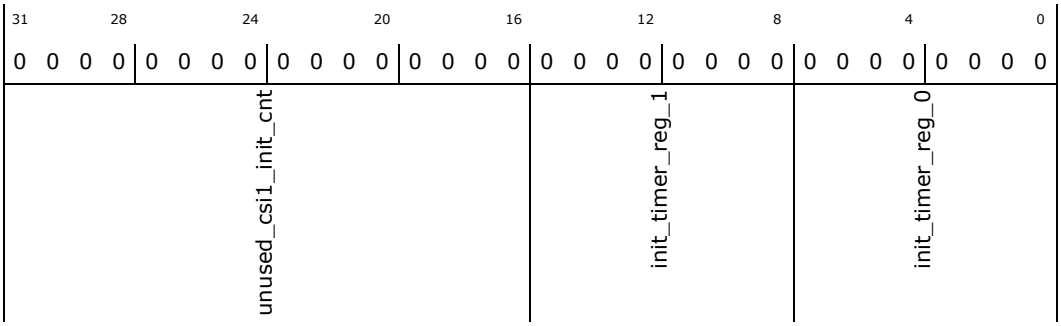
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_init_cnt: [ISPMMADR] + 80110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi1_init_cnt:** Unused
15:8	0h RW	**init_timer_reg_1:** Byte 1 for power up timer
7:0	0h RW	**init_timer_reg_0:** Byte 0 for power up timer

3.7.638 reg_inp_sys_csi_receiver_csi_backend_fs_ls_type (inp_sys_csi_receiver_csi_backend_fs_ls)—Offset 8011Ch

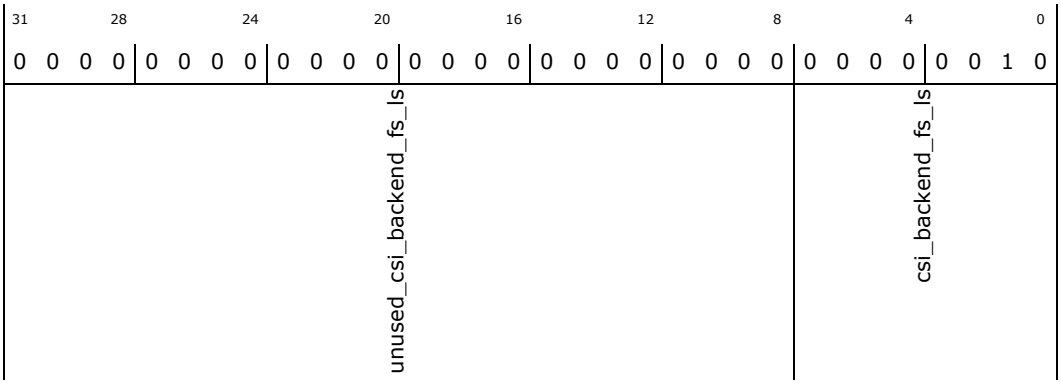
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_fs_ls: [ISPMMADR] + 8011Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_fs_ls:** Unused
7:0	02h RW	**csi_backend_fs_ls:** Minimum interval between frame start and line start syncs

3.7.639 reg_inp_sys_csi_receiver_csi_backend_ls_dvalid_type (inp_sys_csi_receiver_csi_backend_ls_dvalid)—Offset 80120h

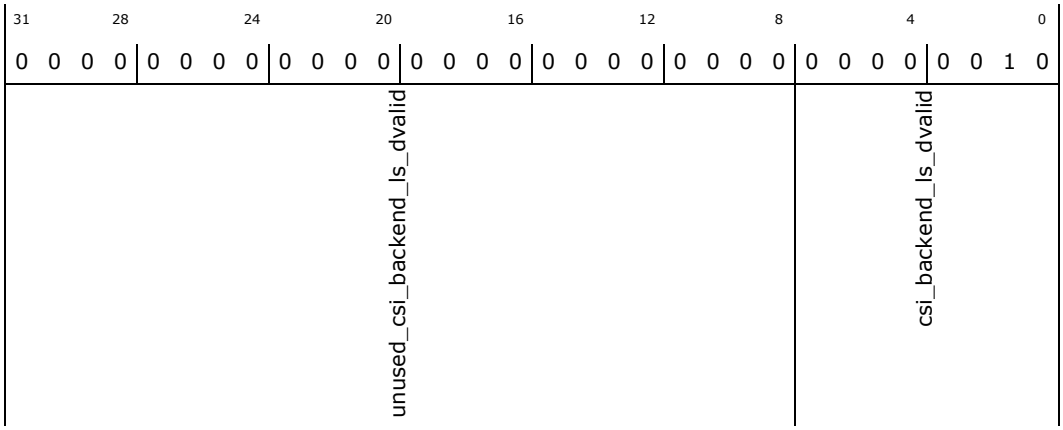
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_ls_dvalid: [ISPMMADR] + 80120h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_ls_dvalid:** Unused
7:0	02h RW	**csi_backend_ls_dvalid:** Minimum interval between line start sync and valid data

3.7.640 reg_inp_sys_csi_receiver_csi_backend_dvalid_le_type (inp_sys_csi_receiver_csi_backend_dvalid_le)—Offset 80124h

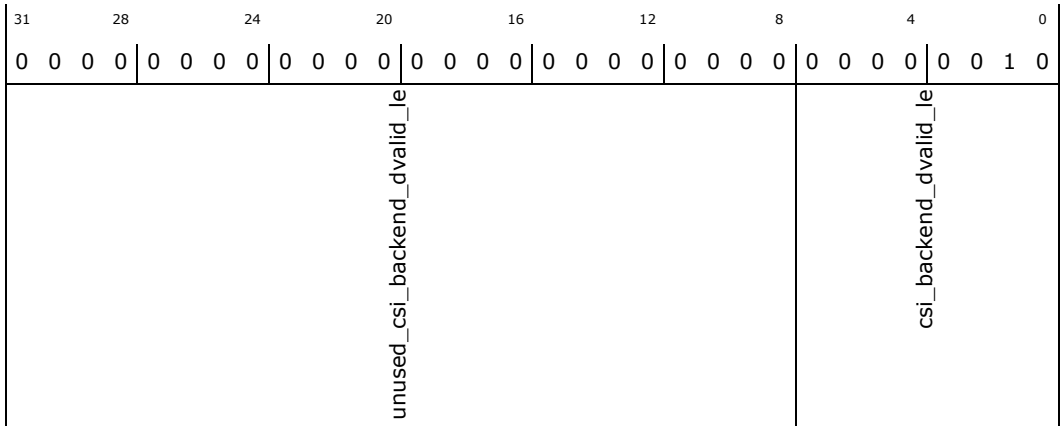
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_dvalid_le: [ISPMMADR] + 80124h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_dvalid_le:** Unused
7:0	02h RW	**csi_backend_dvalid_le:** Minimum interval between valid data and line end sync

3.7.641 reg_inp_sys_csi_receiver_csi_backend_le_fe_type (inp_sys_csi_receiver_csi_backend_le_fe)—Offset 80128h

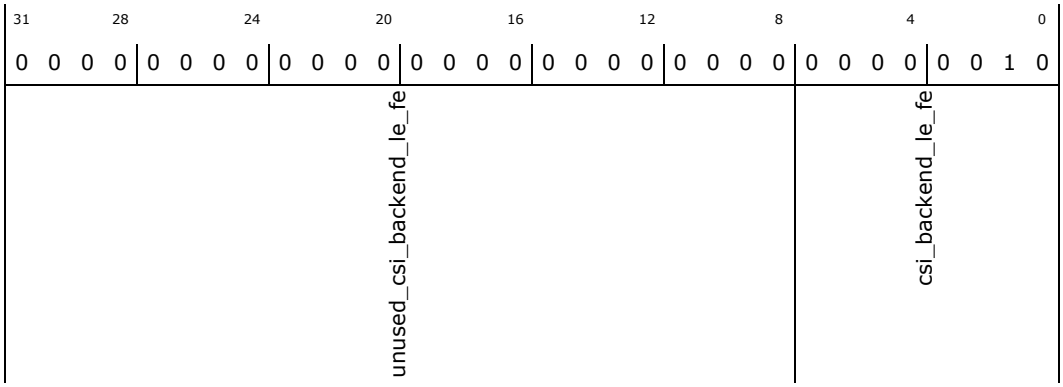
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_le_fe: [ISPMMADR] + 80128h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_le_fe:** Unused
7:0	02h RW	**csi_backend_le_fe:** Minimum interval between line end and frame end syncs

3.7.642 reg_inp_sys_csi_receiver_csi_backend_fe_fs_type (inp_sys_csi_receiver_csi_backend_fe_fs)—Offset 8012Ch

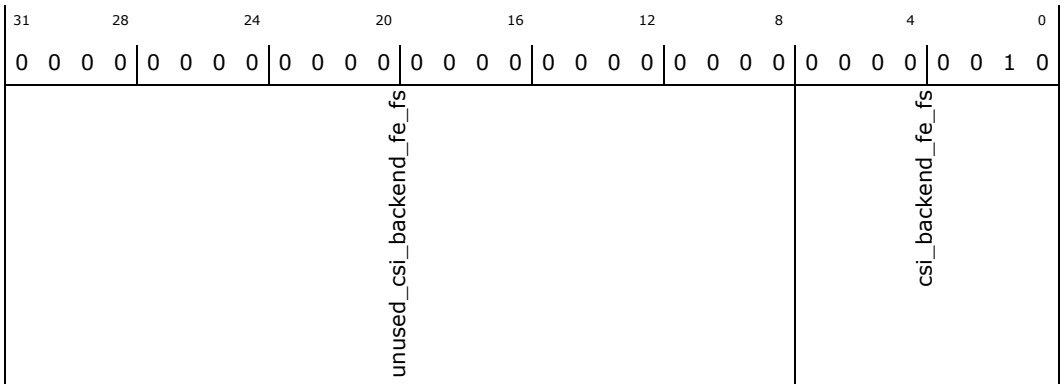
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_fe_fs: [ISPMMADR] + 8012Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_fe_fs:** Unused

Bit Range	Default & Access	Description
7:0	02h RW	**csi_backend_fe_fs:** Minimum interval between frame end and frame start syncs

3.7.643 reg_inp_sys_csi_receiver_csi_backend_le_ls_type (inp_sys_csi_receiver_csi_backend_le_ls)—Offset 80130h

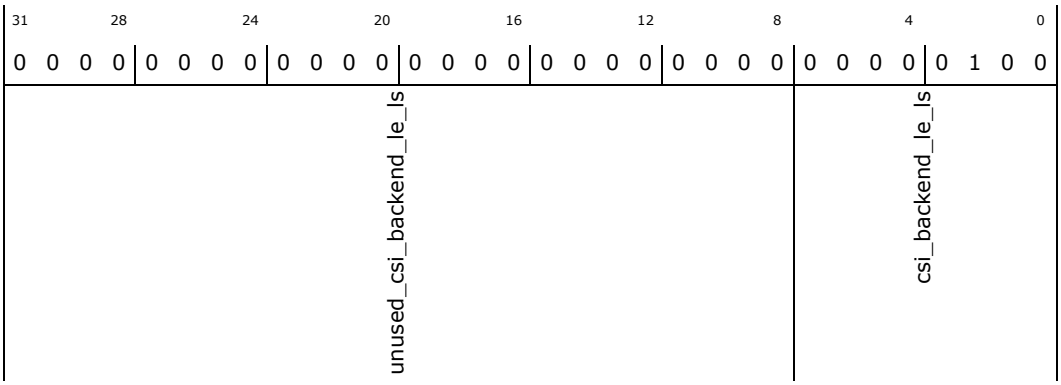
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_le_ls: [ISPMMADR] + 80130h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_le_ls:** Unused
7:0	04h RW	**csi_backend_le_ls:** Minimum interval between line end and line start syncs

3.7.644 reg_inp_sys_csi_receiver_csi_backend_two_pixel_en_type (inp_sys_csi_receiver_csi_backend_two_pixel_en)—Offset 80134h

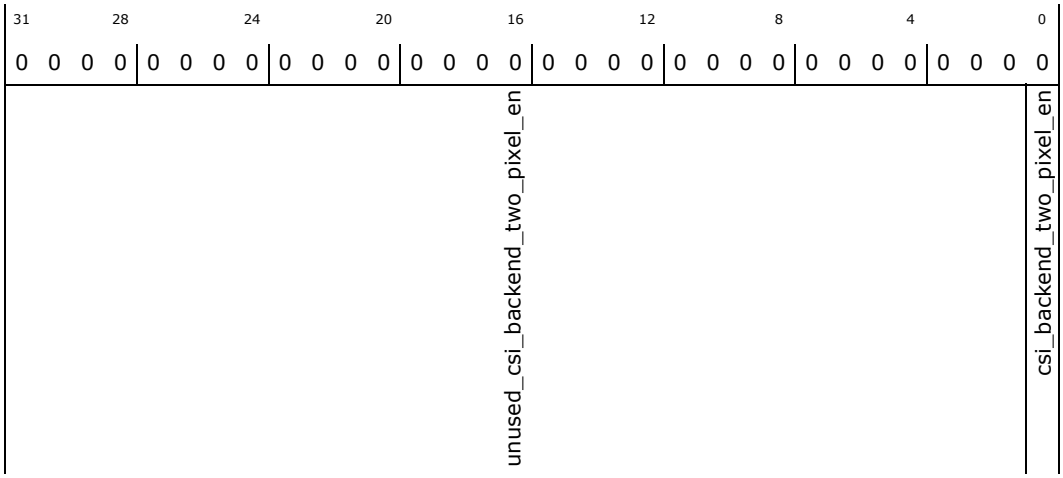
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_two_pixel_en: [ISPMMADR] + 80134h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_csi_backend_two_pixel_en:** Unused
0	0h RW	**csi_backend_two_pixel_en:** Enable two pixels per clock mode

3.7.645 reg_inp_sys_csi_receiver_csi1_raw16_18_data_id_type (inp_sys_csi_receiver_csi1_raw16_18_data_id)—Offset 80138h

RAW 16 and RAW 18 data ID register

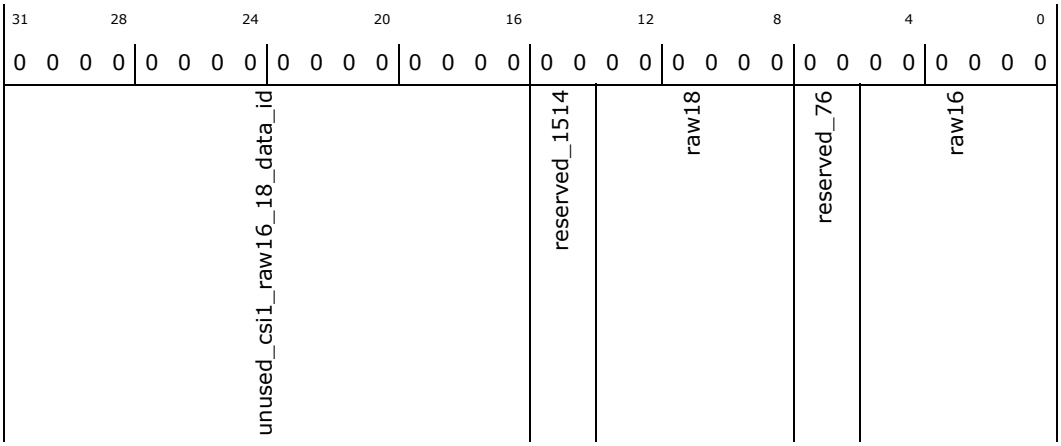
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_raw16_18_data_id: [ISPMMADR] + 80138h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi1_raw16_18_data_id:** Unused
15:14	0h RO	**reserved_1514:** Reserved
13:8	0h RW	**raw18:** RAW 18 data ID
7:6	0h RO	**reserved_76:** Reserved
5:0	0h RW	**raw16:** RAW 16 data ID

3.7.646 reg_inp_sys_csi_receiver_csi1_sync_cnt_type (inp_sys_csi_receiver_csi1_sync_cnt)—Offset 8013Ch

Synchronisation count value in terms of MIPI high speed byte clock

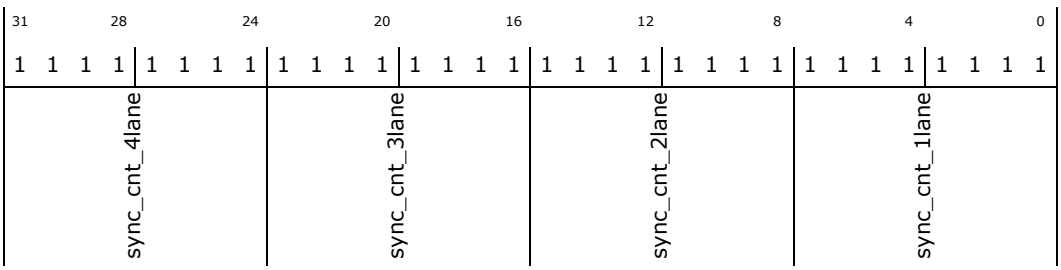
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_sync_cnt: [ISPMMADR] + 8013Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:24	FFh RW	**sync_cnt_4lane:** Synchronisation count value for 4 lane
23:16	FFh RW	**sync_cnt_3lane:** Synchronisation count value for 3 lane
15:8	FFh RW	**sync_cnt_2lane:** Synchronisation count value for 2 lane
7:0	FFh RW	**sync_cnt_1lane:** Synchronisation count value for 1 lane

3.7.647 reg_inp_sys_csi_receiver_csi1_rx_cnt_type (inp_sys_csi_receiver_csi1_rx_cnt)—Offset 80140h

Receive count value in terms of MIPI high speed byte clock

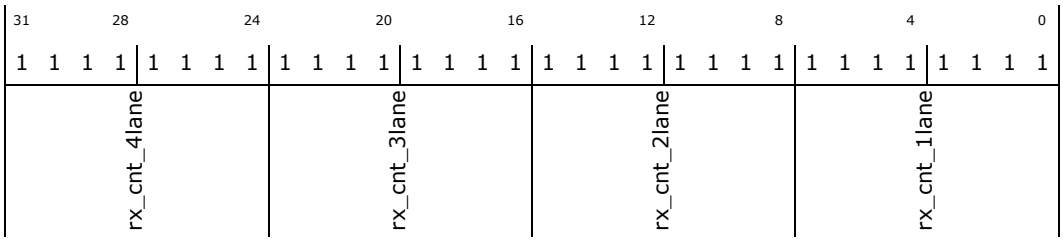
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_rx_cnt: [ISPMMADR] + 80140h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:24	FFh RW	**rx_cnt_4lane:** Receive count value for 4 lane
23:16	FFh RW	**rx_cnt_3lane:** Receive count value for 3 lane
15:8	FFh RW	**rx_cnt_2lane:** Receive count value for 2 lane
7:0	FFh RW	**rx_cnt_1lane:** Receive count value for 1 lane

3.7.648 reg_inp_sys_csi_receiver_csi_backend_rst_type (inp_sys_csi_receiver_csi_backend_rst)—Offset 80144h

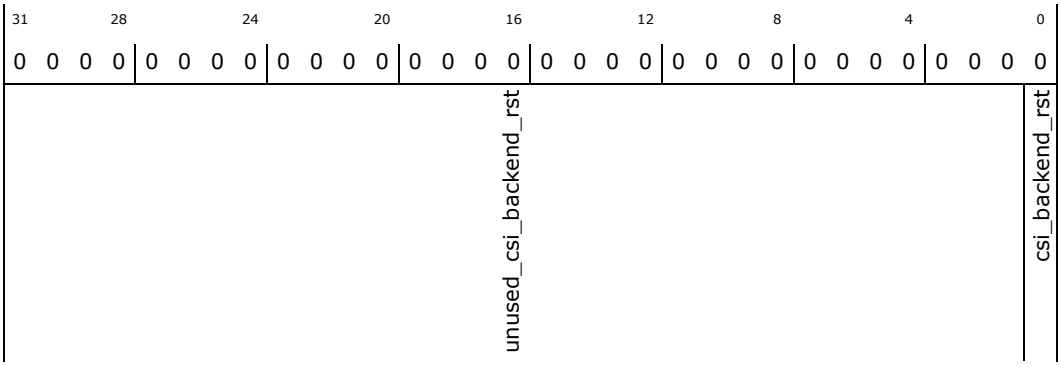
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_rst: [ISPMMADR] + 80144h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_csi_backend_rst:** Unused
0	0h RW	**csi_backend_rst:** Reset CSI Rx backend block

3.7.649 reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0)—Offset 80148h

Compression and Prediction scheme register 0 for virtual channel 0

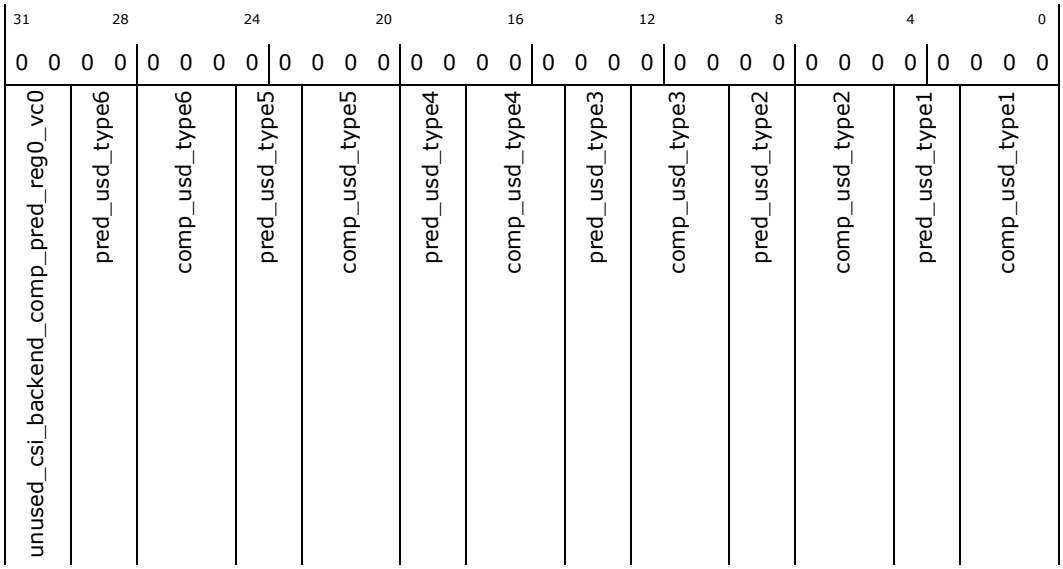
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0: [ISPMMADR] + 80148h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**unused_csi_backend_comp_pred_reg0_vc0:** Unused
29:28	0h RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0h RW	**comp_usd_type6:** compression format for user defined type 6 data: value between 1 to 6
24:23	0h RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0h RW	**comp_usd_type5:** compression format for user defined type 5 data: value between 1 to 6
19:18	0h RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2
17:15	0h RW	**comp_usd_type4:** compression format for user defined type 4 data: value between 1 to 6
14:13	0h RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0h RW	**comp_usd_type3:** compression format for user defined type 3 data: value between 1 to 6
9:8	0h RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type2:** compression format for user defined type 2 data: value between 1 to 6
4:3	0h RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for user defined type 1 data: value between 1 to 6

3.7.650 reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc0_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc0)—Offset 8014Ch

Compression scheme register 1 for virtual channel 0

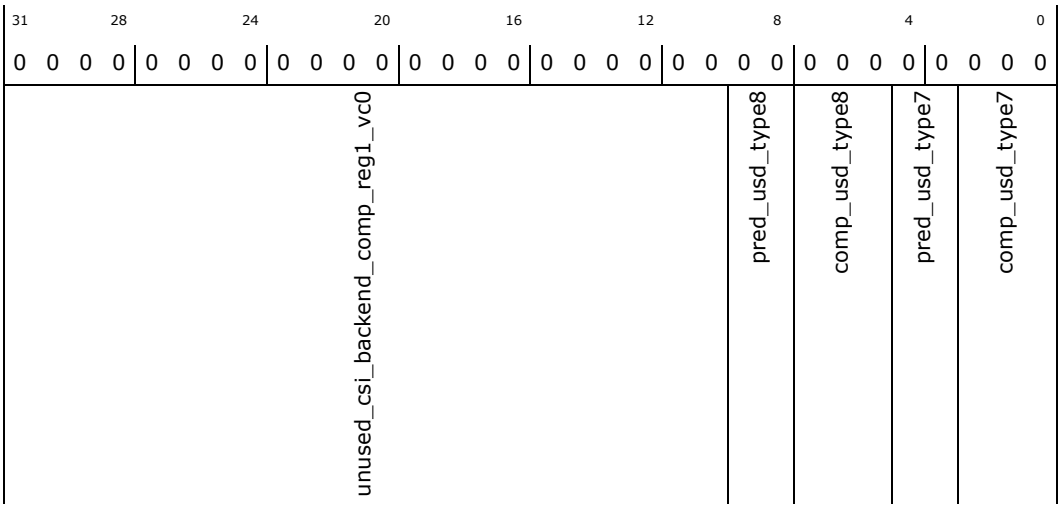
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_reg1_vc0: [ISPMMADR] + 8014Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0h RW	**unused_csi_backend_comp_reg1_vc0:** Unused
9:8	0h RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type8:** compression format for user defined type 8 data: value between 1 to 6
4:3	0h RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type7:** compression format for user defined type 7 data: value between 1 to 6

3.7.651 reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1)—Offset 80150h

Compression and Prediction scheme register 0 for virtual channel 1

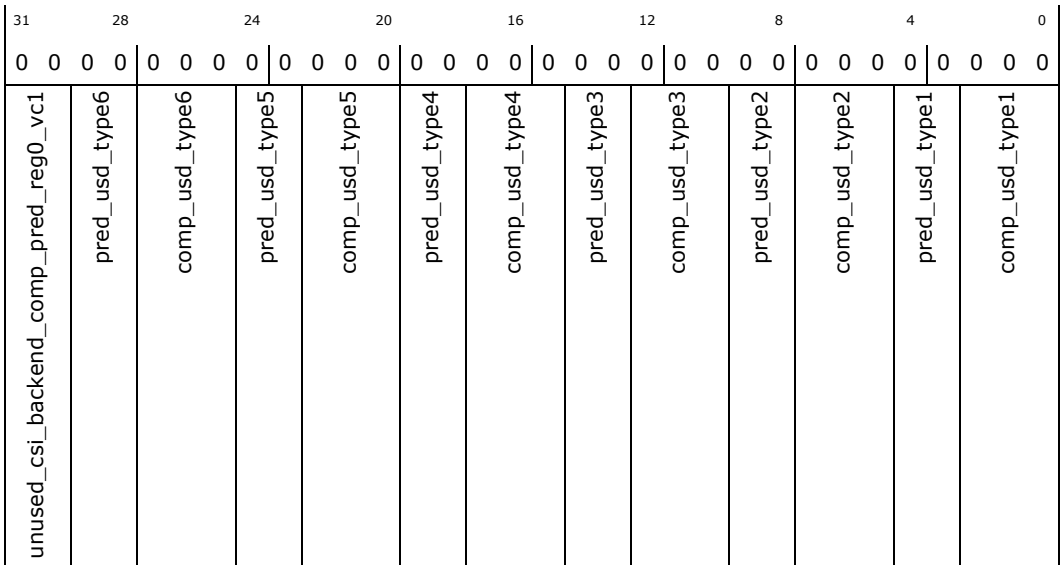
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1: [ISPMMADR] + 80150h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**unused_csi_backend_comp_pred_reg0_vc1:** Unused
29:28	0h RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0h RW	**comp_usd_type6:** compression format for user defined type 6 data: value between 1 to 6
24:23	0h RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0h RW	**comp_usd_type5:** compression format for user defined type 5 data: value between 1 to 6
19:18	0h RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2
17:15	0h RW	**comp_usd_type4:** compression format for user defined type 4 data: value between 1 to 6
14:13	0h RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0h RW	**comp_usd_type3:** compression format for user defined type 3 data: value between 1 to 6
9:8	0h RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2

Bit Range	Default & Access	Description
7:5	0h RW	**comp_usd_type2:** compression format for user defined type 2 data: value between 1 to 6
4:3	0h RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for user defined type 1 data: value between 1 to 6

3.7.652 reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc1_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc1)—Offset 80154h

Compression scheme register 1 for virtual channel 1

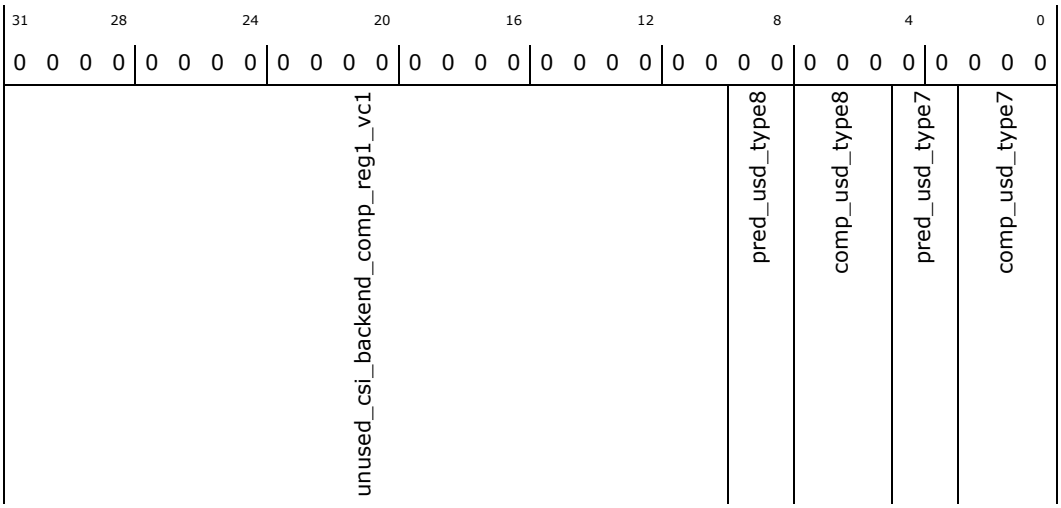
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_reg1_vc1: [ISPMMADR] + 80154h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0h RW	**unused_csi_backend_comp_reg1_vc1:** Unused
9:8	0h RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type8:** compression format for user defined type 8 data: value between 1 to 6

Bit Range	Default & Access	Description
4:3	0h RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type7:** compression format for user defined type 7 data: value between 1 to 6

3.7.653 reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2)—Offset 80158h

Compression and Prediction scheme register 0 for virtual channel 2

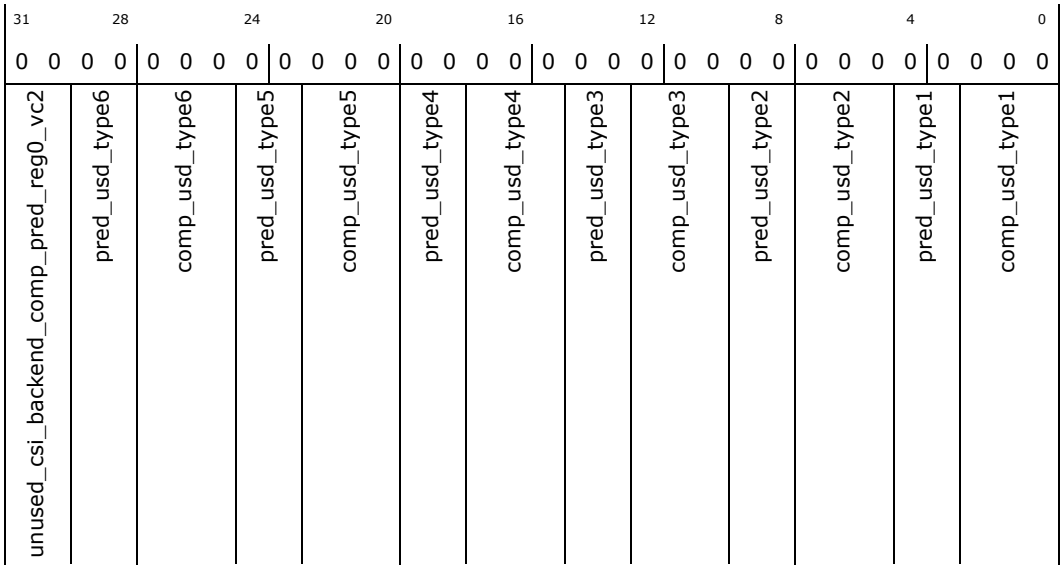
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2: [ISPMMADR] + 80158h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**unused_csi_backend_comp_pred_reg0_vc2:** Unused
29:28	0h RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0h RW	**comp_usd_type6:** compression format for user defined type 6 data: value between 1 to 6

Bit Range	Default & Access	Description
24:23	0h RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0h RW	**comp_usd_type5:** compression format for user defined type 5 data: value between 1 to 6
19:18	0h RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2
17:15	0h RW	**comp_usd_type4:** compression format for user defined type 4 data: value between 1 to 6
14:13	0h RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0h RW	**comp_usd_type3:** compression format for user defined type 3 data: value between 1 to 6
9:8	0h RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type2:** compression format for user defined type 2 data: value between 1 to 6
4:3	0h RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for user defined type 1 data: value between 1 to 6

3.7.654 reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc2_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc2)—Offset 8015Ch

Compression scheme register 1 for virtual channel 2

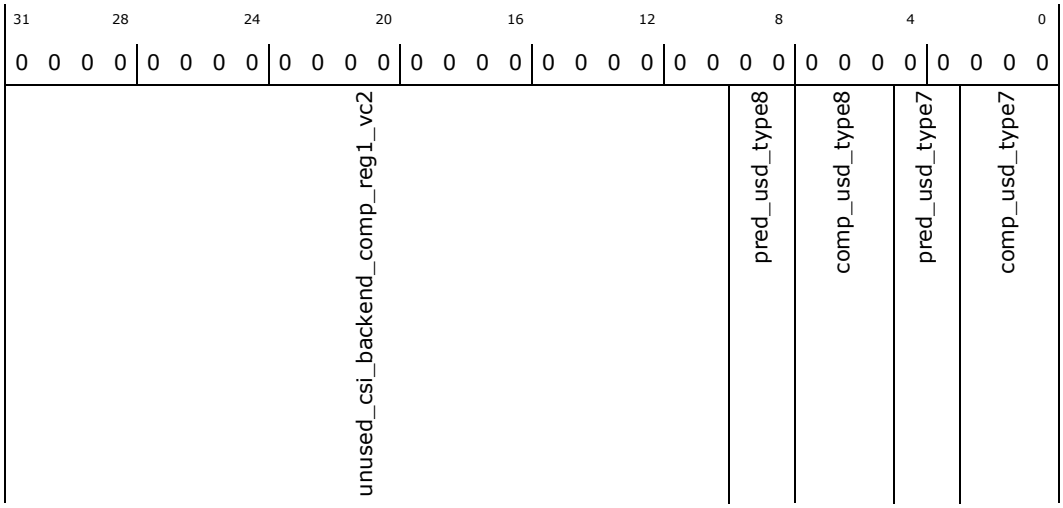
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_reg1_vc2: [ISPMMADR] + 8015Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0h RW	**unused_csi_backend_comp_reg1_vc2:** Unused
9:8	0h RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type8:** compression format for user defined type 8 data: value between 1 to 6
4:3	0h RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type7:** compression format for user defined type 7 data: value between 1 to 6

3.7.655 reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3)—Offset 80160h

Compression and Prediction scheme register 0 for virtual channel 3

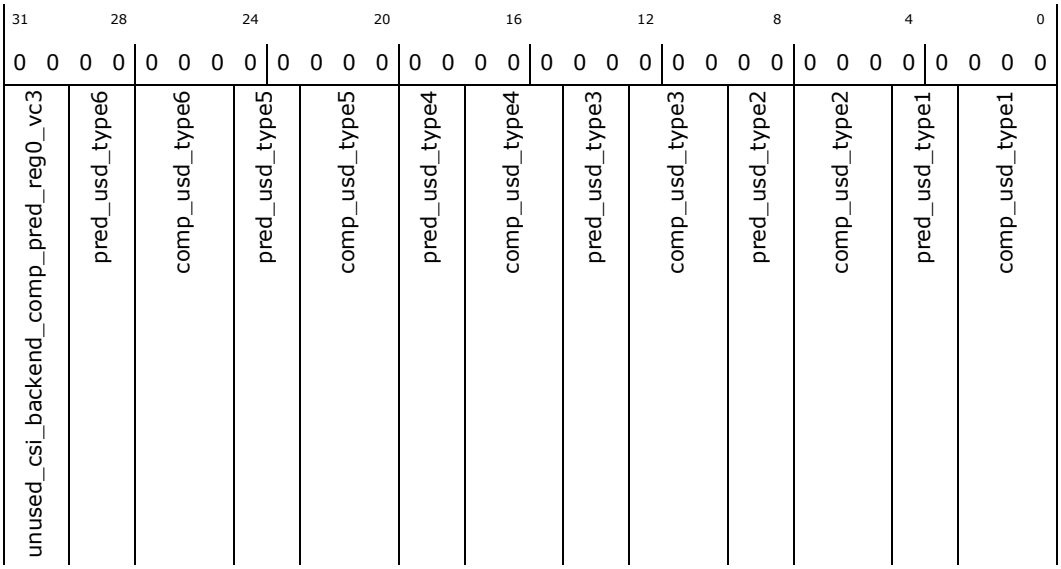
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3: [ISPMMADR] + 80160h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**unused_csi_backend_comp_pred_reg0_vc3:** Unused
29:28	0h RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0h RW	**comp_usd_type6:** compression format for user defined type 6 data: value between 1 to 6
24:23	0h RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0h RW	**comp_usd_type5:** compression format for user defined type 5 data: value between 1 to 6
19:18	0h RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2
17:15	0h RW	**comp_usd_type4:** compression format for user defined type 4 data: value between 1 to 6
14:13	0h RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0h RW	**comp_usd_type3:** compression format for user defined type 3 data: value between 1 to 6
9:8	0h RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type2:** compression format for user defined type 2 data: value between 1 to 6
4:3	0h RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for user defined type 1 data: value between 1 to 6

3.7.656 reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc3_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc3)—Offset 80164h

Compression scheme register 1 for virtual channel 3

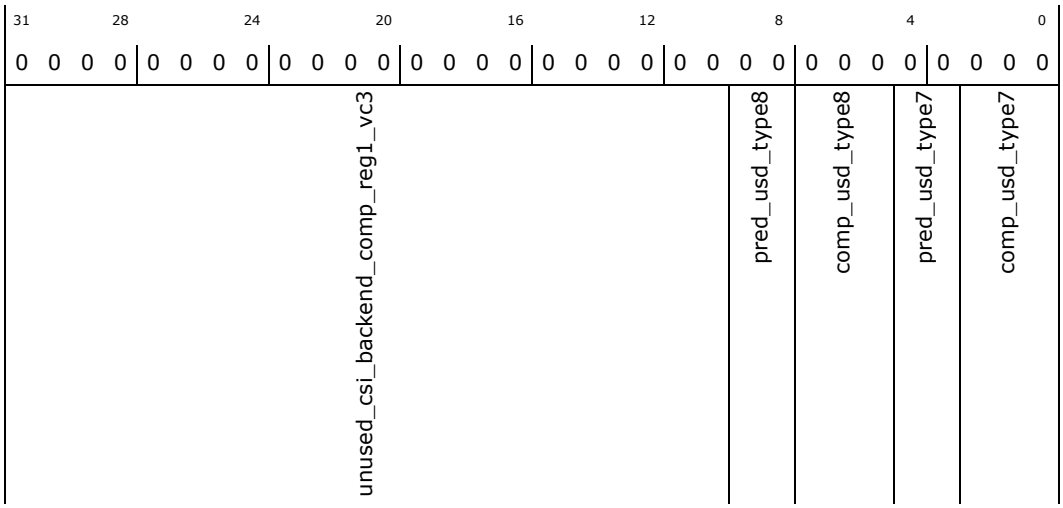
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_reg1_vc3: [ISPMMADR] + 80164h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0h RW	**unused_csi_backend_comp_reg1_vc3:** Unused
9:8	0h RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type8:** compression format for user defined type 8 data: value between 1 to 6
4:3	0h RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type7:** compression format for user defined type 7 data: value between 1 to 6

3.7.657 reg_inp_sys_csi_receiver_csi_backend_raw18_reg_type (inp_sys_csi_receiver_csi_backend_raw18_reg)—Offset 80168h

Configuration register for RAW 18 data type decode

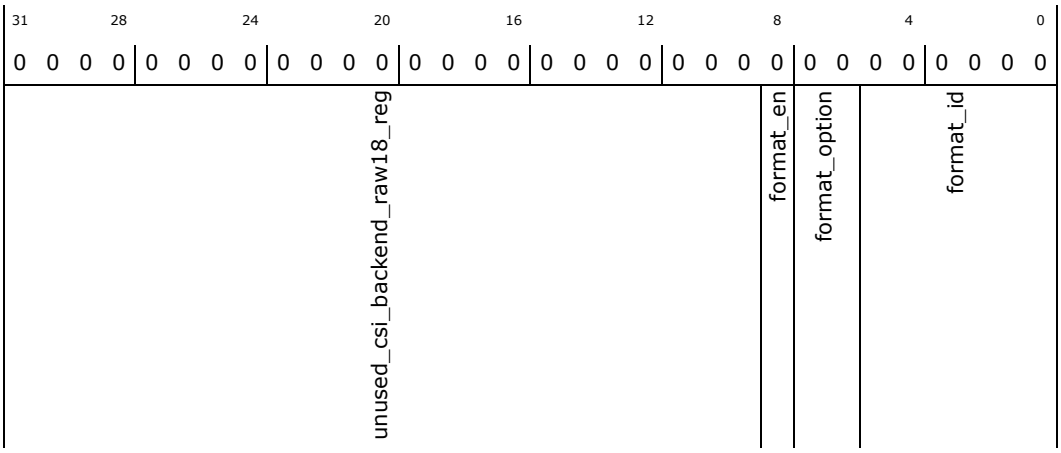
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_raw18_reg: [ISPMMADR] + 80168h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_csi_backend_raw18_reg:** Unused
8	0h RW	**format_en:** enable RAW 18 type decode
7:6	0h RW	**format_option:** format option for RAW 18 data type: 3 options possible (1,2,3)
5:0	0h RW	**format_id:** data id for RAW 18

3.7.658 reg_inp_sys_csi_receiver_csi_backend_force_raw8_reg_type (inp_sys_csi_receiver_csi_backend_force_raw8_reg)—Offset 8016Ch

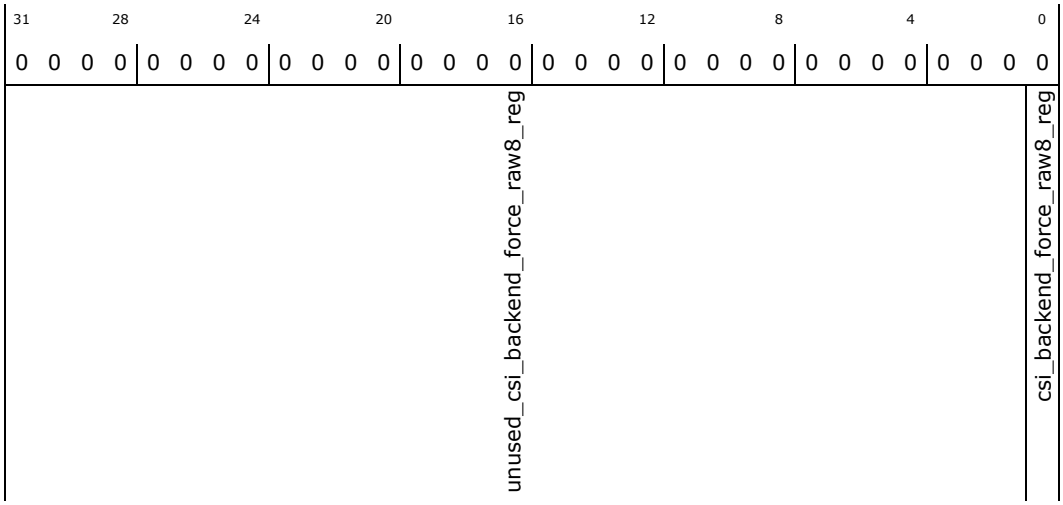
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_force_raw8_reg: [ISPMMADR] + 8016Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_csi_backend_force_raw8_reg:** Unused
0	0h RW	**csi_backend_force_raw8_reg:** Force RAW8(byte) decoding for LONG data packets

3.7.659 reg_inp_sys_csi_receiver_csi_backend_raw16_reg_type (inp_sys_csi_receiver_csi_backend_raw16_reg)—Offset 80170h

Configuration register for RAW 16 data type decode

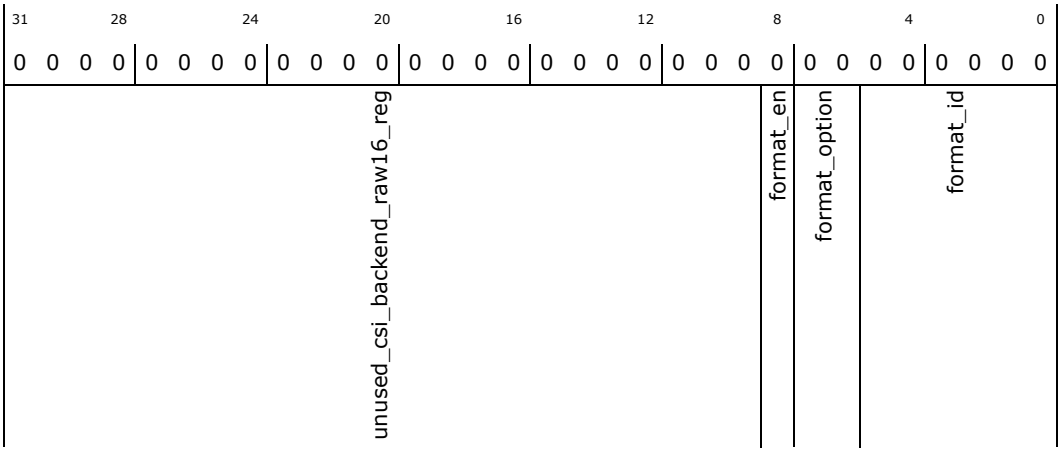
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_raw16_reg: [ISPMMADR] + 80170h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_csi_backend_raw16_reg:** Unused
8	0h RW	**format_en:** enable RAW 16 type decode
7:6	0h RW	**format_option:** format option for RAW 16 data type: ONLY 1 option possible (1)
5:0	0h RW	**format_id:** data id for RAW 16

3.7.660 reg_inp_sys_csi_receiver_csi2_dev_ready_type (inp_sys_csi_receiver_csi2_dev_ready)—Offset 80200h

Set after programming operational registers to enable receiver

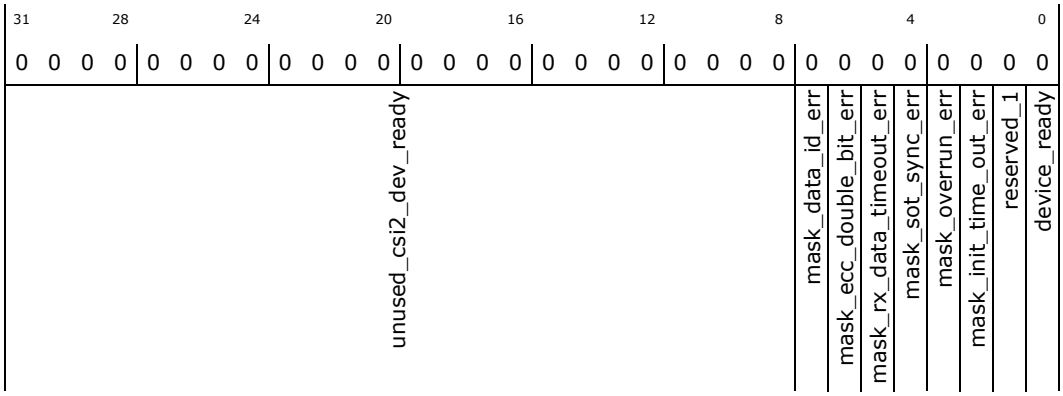
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi2_dev_ready: [ISPMMADR] + 80200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi2_dev_ready:** Unused
7	0h RW	**mask_data_id_err:** Set to mask error recovery when data ID error is detected
6	0h RW	**mask_ecc_double_bit_err:** Set to mask error recovery when ECC double bit error is detected
5	0h RW	**mask_rx_data_timeout_err:** Set to mask error recovery when receive data time out error is detected
4	0h RW	**mask_sot_sync_err:** Set to mask error recovery when start of transmission sync error is detected
3	0h RW	**mask_overrun_err:** set to mask overrun: NOT used now, can be discarded
2	0h RW	**mask_init_time_out_err:** Set to mask error recovery when initialization time out error is detected
1	0h RO	**reserved_1:** Reserved
0	0h RW	**device_ready:** Set to indicate that device is ready for reception

3.7.661 reg_inp_sys_csi_receiver_csi2_int_status_type (inp_sys_csi_receiver_csi2_int_status)—Offset 80204h

Interrupt Status

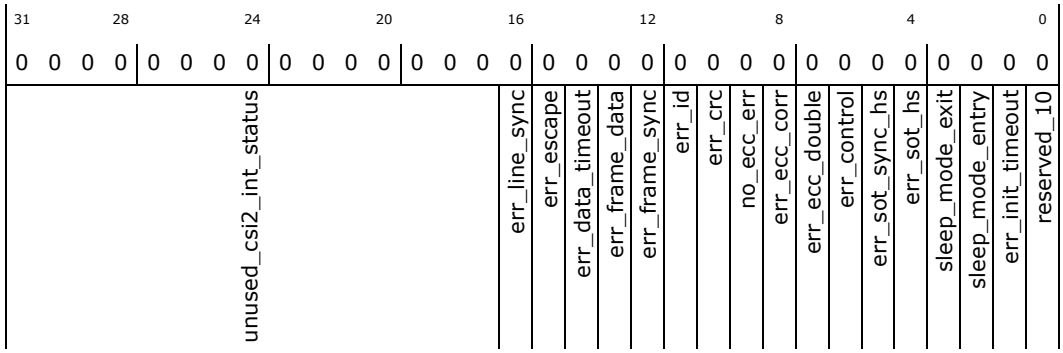
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi2_int_status: [ISPMMADR] + 80204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi2_int_status:** Unused
16	0h RW/1C	**err_line_sync:** Set if line number for line start and line end packets do not match
15	0h RW/1C	**err_escape:** Set if an unrecognised escape entry command is received
14	0h RW/1C	**err_data_timeout:** Set if time taken to receive a packet exceeds programmed timeout value
13	0h RW/1C	**err_frame_data:** Set if data packets within a frame has errors
12	0h RW/1C	**err_frame_sync:** Set if frame start is not paired with frame end for same virtual channel
11	0h RW/1C	**err_id:** Set if packet header has a unrecognised data id
10	0h RW/1C	**err_crc:** Set if computed CRC differs from received value
9	0h RW/1C	**no_ecc_err:** Set if no ECC error detected in packet
8	0h RW/1C	**err_ecc_corr:** Set if ECC error detected and corrected for one bit
7	0h RW/1C	**err_ecc_double:** Set if ECC error detected for two or more bits
6	0h RW/1C	**err_control:** Set if DPHY flags a control error
5	0h RW/1C	**err_sot_sync_hs:** Set if DPHY flags start of transmission synchronisation error
4	0h RW/1C	**err_sot_hs:** Set if DPHY flags start of transmission error
3	0h RW/1C	**sleep_mode_exit:** Set if DPHY exits ultra low power state
2	0h RW/1C	**sleep_mode_entry:** Set if DPHY enters ultra low power state
1	0h RW/1C	**err_init_timeout:** Set if Initialization timeout error occurs on DPHY data lanes

Bit Range	Default & Access	Description
0	0h RO	**reserved_10:** Always set to 0

3.7.662 reg_inp_sys_csi_receiver_csi2_int_enable_type (inp_sys_csi_receiver_csi2_int_enable)—Offset 80208h

Interrupt Enable

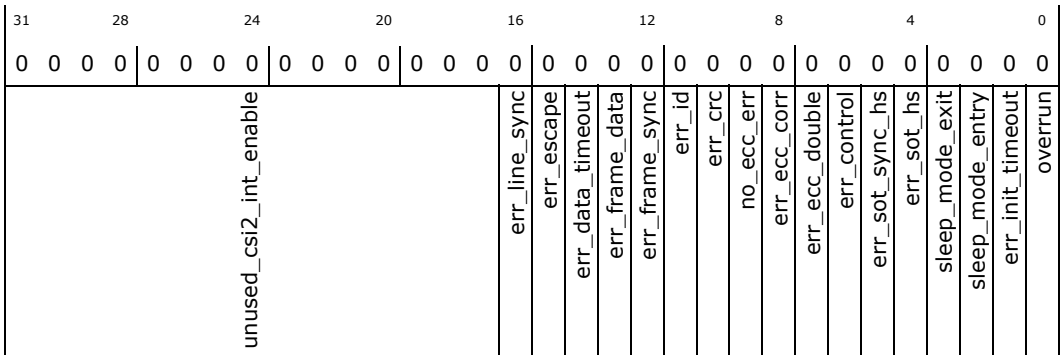
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi2_int_enable: [ISPMMADR] + 80208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi2_int_enable:** Unused
16	0h RW	**err_line_sync:** Enable line sync error interrupt
15	0h RW	**err_escape:** Enable escape entry error interrupt
14	0h RW	**err_data_timeout:** Enable timeout error interrupt
13	0h RW	**err_frame_data:** Enable frame data error interrupt
12	0h RW	**err_frame_sync:** Enable frame sync error interrupt
11	0h RW	**err_id:** Enable data id error interrupt
10	0h RW	**err_crc:** Enable CRC error interrupt

Bit Range	Default & Access	Description
9	0h RW	**no_ecc_err:** Enable no ECC error interrupt
8	0h RW	**err_ecc_corr:** Enable ECC error detected and corrected for one bit interrupt
7	0h RW	**err_ecc_double:** Enable ECC error detected for two or more bits interrupt
6	0h RW	**err_control:** Enable control error interrupt
5	0h RW	**err_sot_sync_hs:** Enable start of transmission synchronisation error interrupt
4	0h RW	**err_sot_hs:** Enable start of transmission error interrupt
3	0h RW	**sleep_mode_exit:** Enable sleep mode exit interrupt
2	0h RW	**sleep_mode_entry:** Enable sleep mode entry interrupt
1	0h RW	**err_init_timeout:** Enable Initialization timeout error interrupt
0	0h RW	**overrun:** Enable FIFO overrun interrupt: NOT available now, can be discarded

3.7.663 reg_inp_sys_csi_receiver_csi2_func_prg_type (inp_sys_csi_receiver_csi2_func_prg)—Offset 8020Ch

Functional Programming

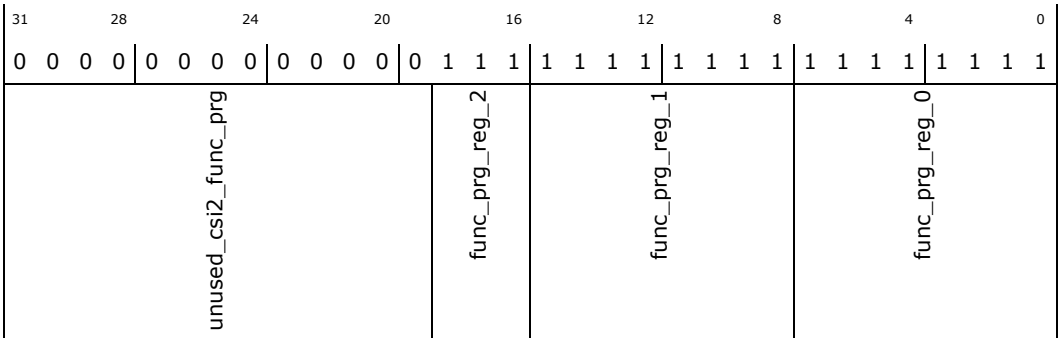
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi2_func_prg: [ISPMMADR] + 8020Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0007FFFFh



Bit Range	Default & Access	Description
31:19	0h RW	**unused_csi2_func_prg:** Unused
18:16	7h RW	**func_prg_reg_2:** Byte 2 for functional programming
15:8	FFh RW	**func_prg_reg_1:** Byte 1 for functional programming
7:0	FFh RW	**func_prg_reg_0:** Byte 0 for functional programming

3.7.664 reg_inp_sys_csi_receiver_csi2_init_cnt_type (inp_sys_csi_receiver_csi2_init_cnt)—Offset 80210h

Duration after power up when DPHY lanes will not be observed

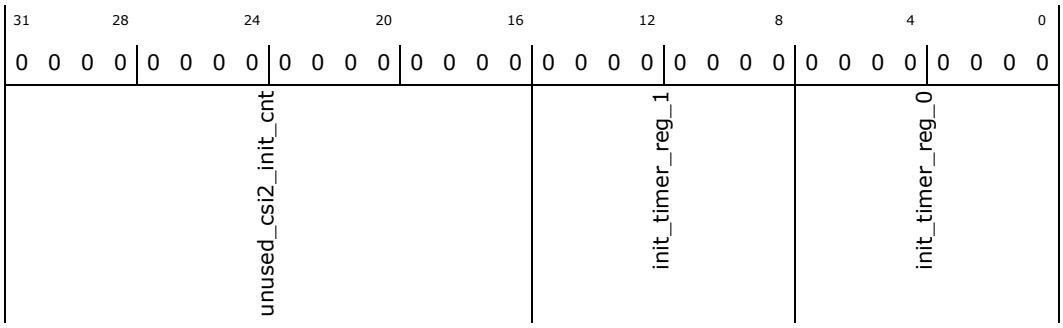
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi2_init_cnt: [ISPMMADR] + 80210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi2_init_cnt:** Unused
15:8	0h RW	**init_timer_reg_1:** Byte 1 for power up timer
7:0	0h RW	**init_timer_reg_0:** Byte 0 for power up timer

3.7.665 reg_inp_sys_csi_receiver_csi2_raw16_18_data_id_type (inp_sys_csi_receiver_csi2_raw16_18_data_id)—Offset 80238h

RAW 16 and RAW 18 data ID register

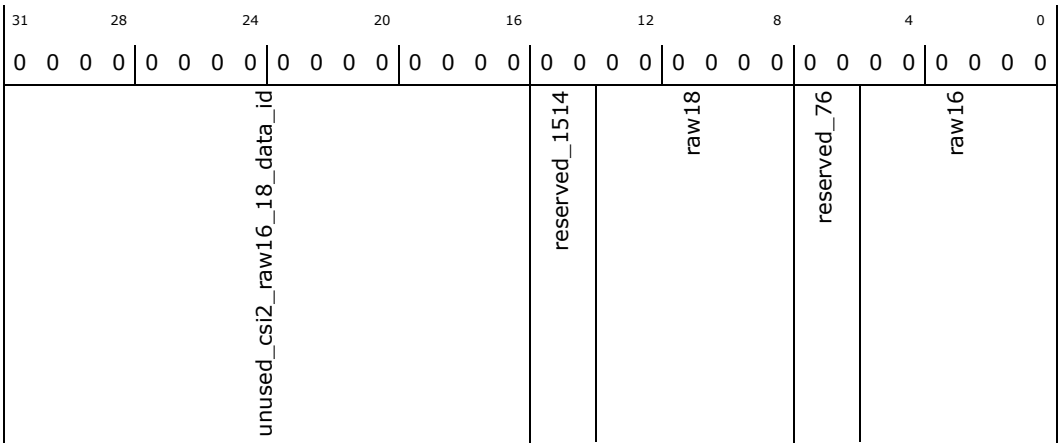
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi2_raw16_18_data_id: [ISPMMADR] + 80238h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi2_raw16_18_data_id:** Unused
15:14	0h RO	**reserved_1514:** Reserved
13:8	0h RW	**raw18:** RAW 18 data ID
7:6	0h RO	**reserved_76:** Reserved
5:0	0h RW	**raw16:** RAW 16 data ID

3.7.666 reg_inp_sys_csi_receiver_csi2_sync_cnt_type (inp_sys_csi_receiver_csi2_sync_cnt)—Offset 8023Ch

Synchronisation count value in terms of MIPI high speed byte clock

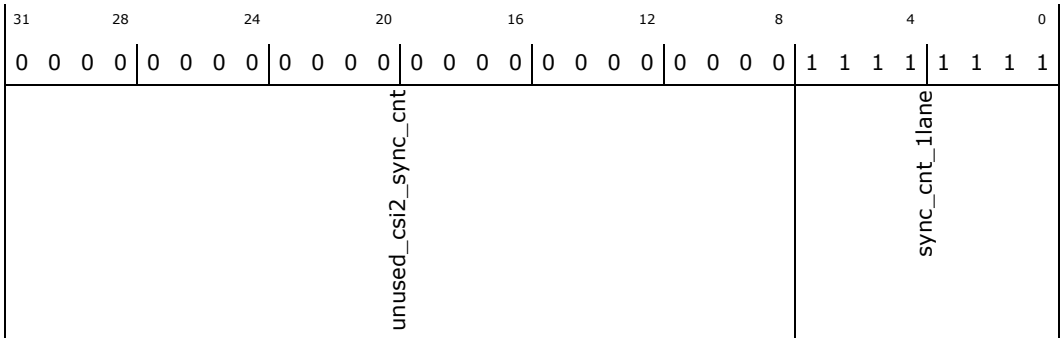
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi2_sync_cnt: [ISPMMADR] + 8023Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000FFh



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi2_sync_cnt:** Unused
7:0	FFh RW	**sync_cnt_1lane:** Synchronisation count value for 1 lane

3.7.667 reg_inp_sys_csi_receiver_csi2_rx_cnt_type (inp_sys_csi_receiver_csi2_rx_cnt)—Offset 80240h

Receive count value in terms of MIPI high speed byte clock

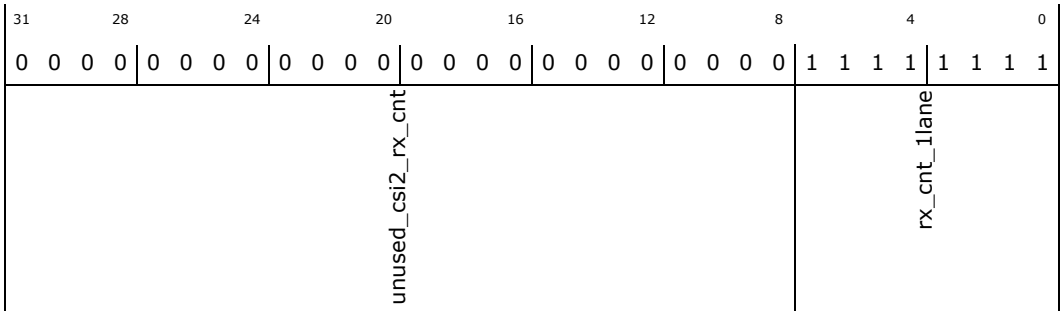
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi2_rx_cnt: [ISPMMADR] + 80240h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000FFh



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi2_rx_cnt:** Unused
7:0	FFh RW	**rx_cnt_1lane:** Receive count value for 1 lane

3.7.668 reg_inp_sys_csi_receiver_csi3_dev_ready_type (inp_sys_csi_receiver_csi3_dev_ready)—Offset 80300h

Set after programming operational registers to enable receiver

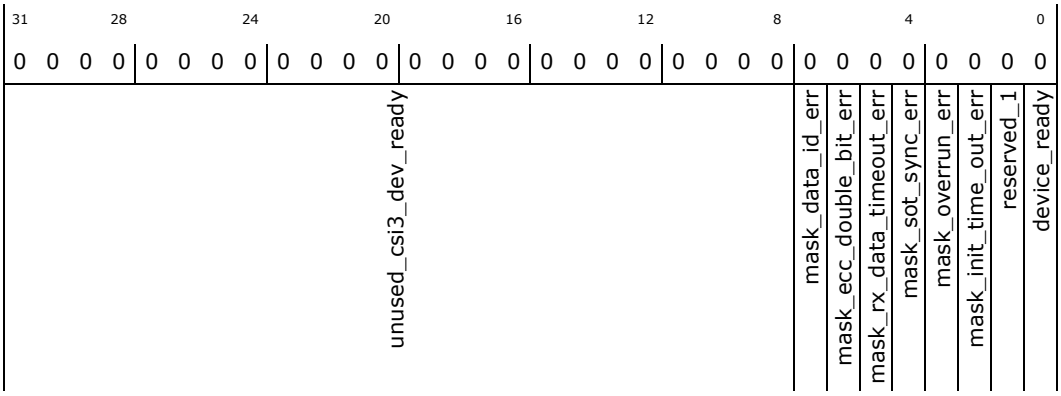
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_dev_ready: [ISPMMADR] + 80300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi3_dev_ready:** Unused
7	0h RW	**mask_data_id_err:** Set to mask error recovery when data ID error is detected
6	0h RW	**mask_ecc_double_bit_err:** Set to mask error recovery when ECC double bit error is detected
5	0h RW	**mask_rx_data_timeout_err:** Set to mask error recovery when receive data time out error is detected
4	0h RW	**mask_sot_sync_err:** Set to mask error recovery when start of transmission sync error is detected
3	0h RW	**mask_overrun_err:** set to mask overrun: NOT used now, can be discarded
2	0h RW	**mask_init_time_out_err:** Set to mask error recovery when initialization time out error is detected
1	0h RO	**reserved_1:** Reserved
0	0h RW	**device_ready:** Set to indicate that device is ready for reception

3.7.669 reg_inp_sys_csi_receiver_csi3_int_status_type (inp_sys_csi_receiver_csi3_int_status)—Offset 80304h

Interrupt Status

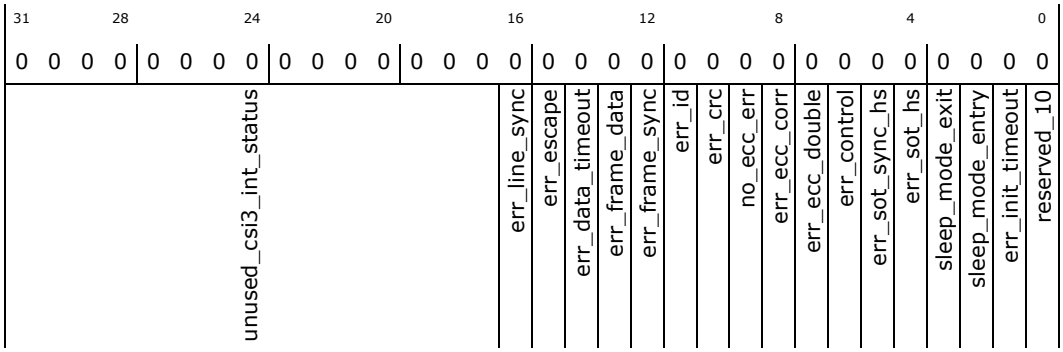
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_int_status: [ISPMMADR] + 80304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi3_int_status:** Unused
16	0h RW/1C	**err_line_sync:** Set if line number for line start and line end packets do not match
15	0h RW/1C	**err_escape:** Set if an unrecognised escape entry command is received
14	0h RW/1C	**err_data_timeout:** Set if time taken to receive a packet exceeds programmed timeout value
13	0h RW/1C	**err_frame_data:** Set if data packets within a frame has errors
12	0h RW/1C	**err_frame_sync:** Set if frame start is not paired with frame end for same virtual channel
11	0h RW/1C	**err_id:** Set if packet header has a unrecognised data id
10	0h RW/1C	**err_crc:** Set if computed CRC differs from received value
9	0h RW/1C	**no_ecc_err:** Set if no ECC error detected in packet
8	0h RW/1C	**err_ecc_corr:** Set if ECC error detected and corrected for one bit
7	0h RW/1C	**err_ecc_double:** Set if ECC error detected for two or more bits

Bit Range	Default & Access	Description
6	0h RW/1C	**err_control:** Set if DPHY flags a control error
5	0h RW/1C	**err_sot_sync_hs:** Set if DPHY flags start of transmission synchronisation error
4	0h RW/1C	**err_sot_hs:** Set if DPHY flags start of transmission error
3	0h RW/1C	**sleep_mode_exit:** Set if DPHY exits ultra low power state
2	0h RW/1C	**sleep_mode_entry:** Set if DPHY enters ultra low power state
1	0h RW/1C	**err_init_timeout:** Set if Initialization timeout error occurs on DPHY data lanes
0	0h RO	**reserved_10:** Always set to 0

3.7.670 reg_inp_sys_csi_receiver_csi3_int_enable_type (inp_sys_csi_receiver_csi3_int_enable)—Offset 80308h

Interrupt Enable

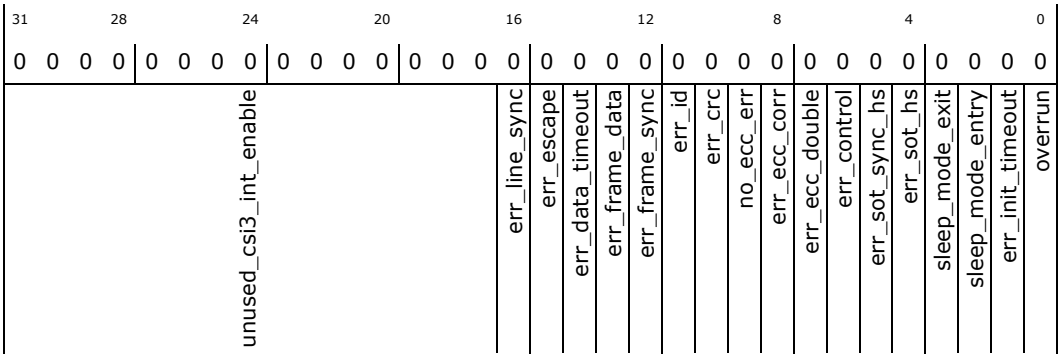
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_int_enable: [ISPMMADR] + 80308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi3_int_enable:** Unused
16	0h RW	**err_line_sync:** Enable line sync error interrupt

Bit Range	Default & Access	Description
15	0h RW	**err_escape:** Enable escape entry error interrupt
14	0h RW	**err_data_timeout:** Enable timeout error interrupt
13	0h RW	**err_frame_data:** Enable frame data error interrupt
12	0h RW	**err_frame_sync:** Enable frame sync error interrupt
11	0h RW	**err_id:** Enable data id error interrupt
10	0h RW	**err_crc:** Enable CRC error interrupt
9	0h RW	**no_ecc_err:** Enable no ECC error interrupt
8	0h RW	**err_ecc_corr:** Enable ECC error detected and corrected for one bit interrupt
7	0h RW	**err_ecc_double:** Enable ECC error detected for two or more bits interrupt
6	0h RW	**err_control:** Enable control error interrupt
5	0h RW	**err_sot_sync_hs:** Enable start of transmission synchronisation error interrupt
4	0h RW	**err_sot_hs:** Enable start of transmission error interrupt
3	0h RW	**sleep_mode_exit:** Enable sleep mode exit interrupt
2	0h RW	**sleep_mode_entry:** Enable sleep mode entry interrupt
1	0h RW	**err_init_timeout:** Enable Initialization timeout error interrupt
0	0h RW	**overrun:** Enable FIFO overrun interrupt: NOT available now, can be discarded

3.7.671 reg_inp_sys_csi_receiver_csi3_func_prg_type (inp_sys_csi_receiver_csi3_func_prg)—Offset 8030Ch

Functional Programming

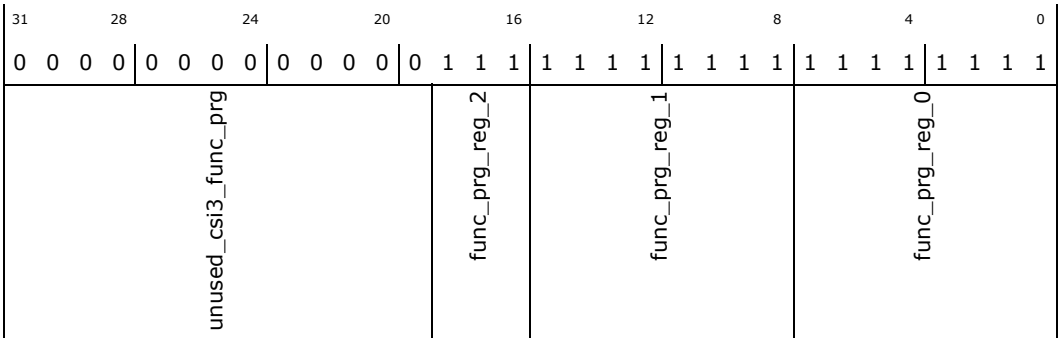
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_func_prg: [ISPMMADR] + 8030Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0007FFFFh



Bit Range	Default & Access	Description
31:19	0h RW	**unused_csi3_func_prg:** Unused
18:16	7h RW	**func_prg_reg_2:** Byte 2 for functional programming
15:8	FFh RW	**func_prg_reg_1:** Byte 1 for functional programming
7:0	FFh RW	**func_prg_reg_0:** Byte 0 for functional programming

3.7.672 reg_inp_sys_csi_receiver_csi3_init_cnt_type (inp_sys_csi_receiver_csi3_init_cnt)—Offset 80310h

Duration after power up when DPHY lanes will not be observed

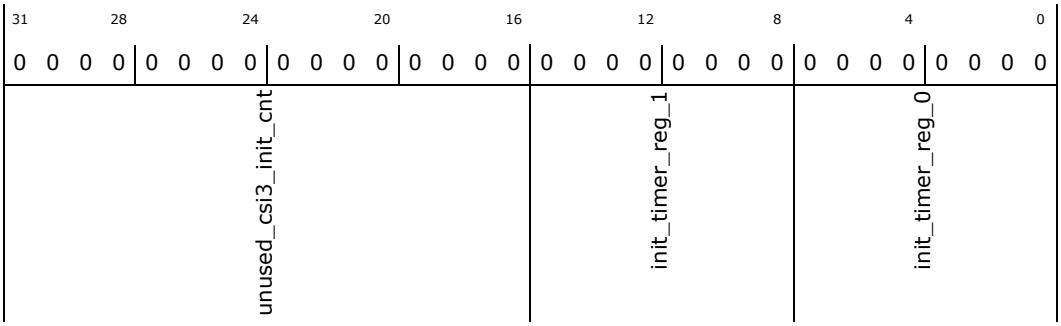
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_init_cnt: [ISPMMADR] + 80310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi3_init_cnt:** Unused
15:8	0h RW	**init_timer_reg_1:** Byte 1 for power up timer
7:0	0h RW	**init_timer_reg_0:** Byte 0 for power up timer

3.7.673 reg_inp_sys_csi_receiver_csi3_raw16_18_data_id_type (inp_sys_csi_receiver_csi3_raw16_18_data_id)—Offset 80338h

RAW 16 and RAW 18 data ID register

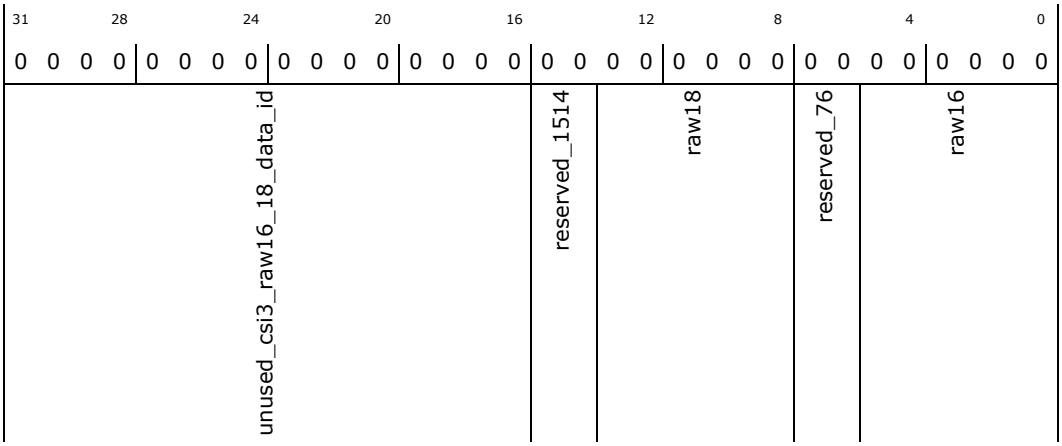
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_raw16_18_data_id: [ISPMMADR] + 80338h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi3_raw16_18_data_id:** Unused
15:14	0h RO	**reserved_1514:** Reserved
13:8	0h RW	**raw18:** RAW 18 data ID
7:6	0h RO	**reserved_76:** Reserved

Bit Range	Default & Access	Description
5:0	0h RW	**raw16:** RAW 16 data ID

3.7.674 reg_inp_sys_csi_receiver_csi3_sync_cnt_type (inp_sys_csi_receiver_csi3_sync_cnt)—Offset 8033Ch

Synchronisation count value in terms of MIPI high speed byte clock

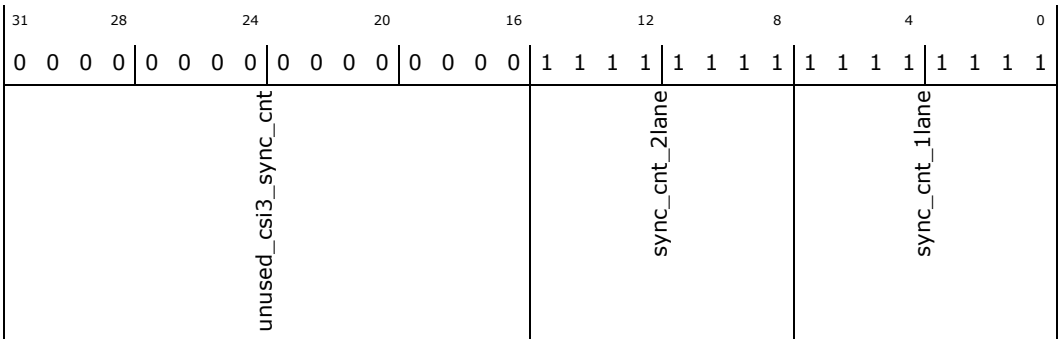
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_sync_cnt: [ISPMMADR] + 8033Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh



Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi3_sync_cnt:** Unused
15:8	FFh RW	**sync_cnt_2lane:** Synchronisation count value for 2 lane
7:0	FFh RW	**sync_cnt_1lane:** Synchronisation count value for 1 lane

3.7.675 reg_inp_sys_csi_receiver_csi3_rx_cnt_type (inp_sys_csi_receiver_csi3_rx_cnt)—Offset 80340h

Receive count value in terms of MIPI high speed byte clock

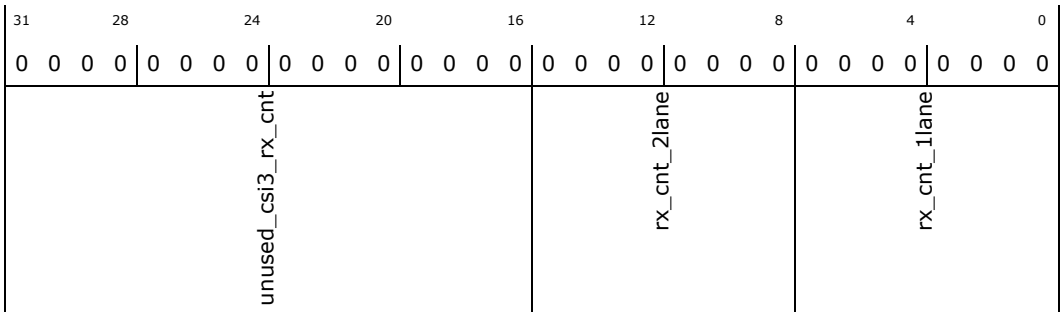
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_rx_cnt: [ISPMMADR] + 80340h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi3_rx_cnt:** Unused
15:8	0h RW	**rx_cnt_2lane:** Receive count value for 2 lane
7:0	0h RW	**rx_cnt_1lane:** Receive count value for 1 lane

3.7.676 reg_inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl_type (inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl)—Offset 80800h

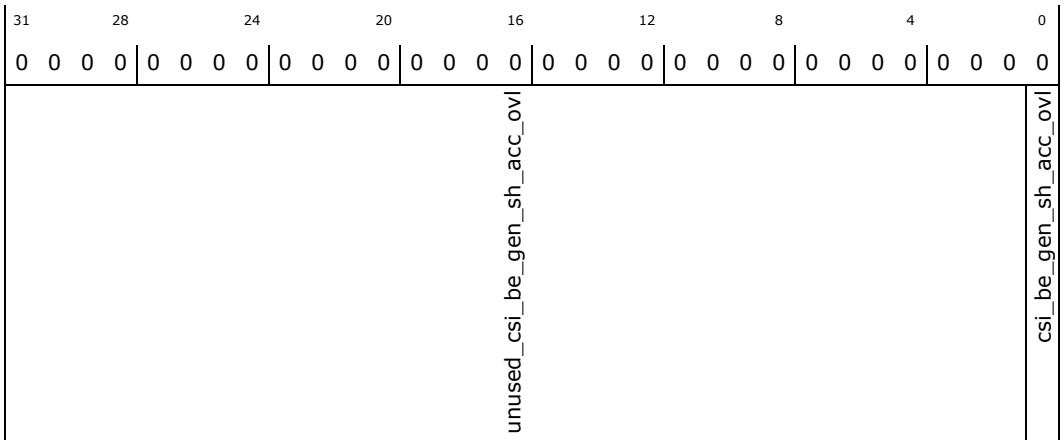
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl: [ISPMMADR] + 80800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_csi_be_gen_sh_acc_ovl:** Unused
0	0h RW	**csi_be_gen_sh_acc_ovl:** Allows for overruling the accept signal generated by the generic short packet FIFO, going to the CSI receiver backend.

3.7.677 reg_inp_sys_csi_receiver_csi_sh_be_srst_type (inp_sys_csi_receiver_csi_sh_be_srst)—Offset 80804h

soft reset modules of the SH CSI receiver Back End

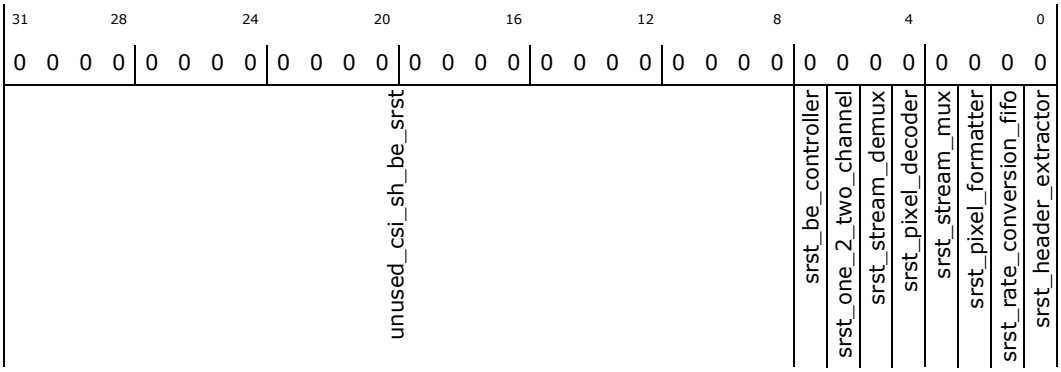
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_srst: [ISPMMADR] + 80804h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_sh_be_srst:** Unused
7	0h RW	**srst_be_controller:** Soft resets the backend controller module
6	0h RW	**srst_one_2_two_channel:** Soft resets the one 2 two channel module
5	0h RW	**srst_stream_demux:** Soft resets the stream demux module
4	0h RW	**srst_pixel_decoder:** Soft resets the pixel decoder module
3	0h RW	**srst_stream_mux:** Soft resets the stream mux module
2	0h RW	**srst_pixel_formatter:** Soft resets the pixel formatter module

Bit Range	Default & Access	Description
1	0h RW	**srst_rate_conversion_fifo:** Soft resets the rate conversion FIFO module
0	0h RW	**srst_header_extractor:** Soft resets the header extractor module

3.7.678 reg_inp_sys_csi_receiver_csi_sh_be_two_ppc_type (inp_sys_csi_receiver_csi_sh_be_two_ppc)—Offset 80808h

Sets the output rate of the backend and the precision

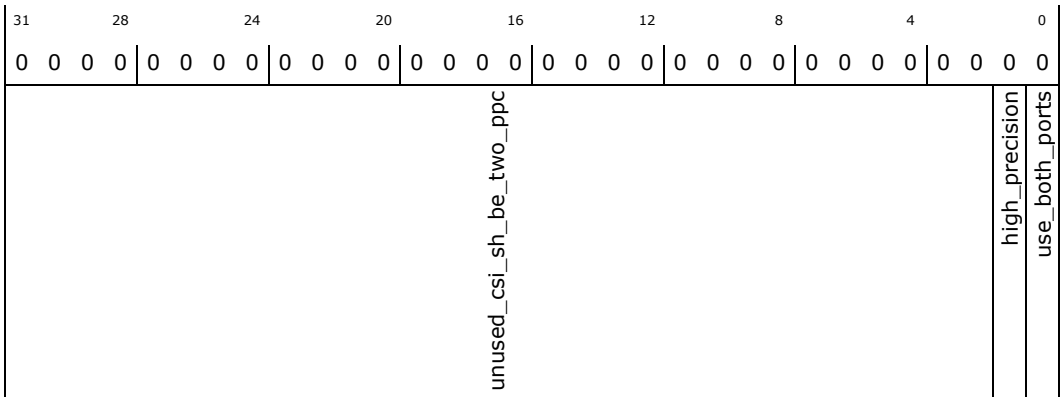
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_two_ppc: [ISPMMADR] + 80808h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_csi_sh_be_two_ppc:** Unused
1	0h RW	**high_precision:** When '1', (and use_both_ports='1' as well) both ports A and B are used to output one high precision pixel, when '0', high_precision pixels are saturated to fit on one port.
0	0h RW	**use_both_ports:** When '1', both ports A and B are active. When '0' only port A is active

3.7.679 reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0)—Offset 8080Ch

Compression scheme register for virtual channel 0

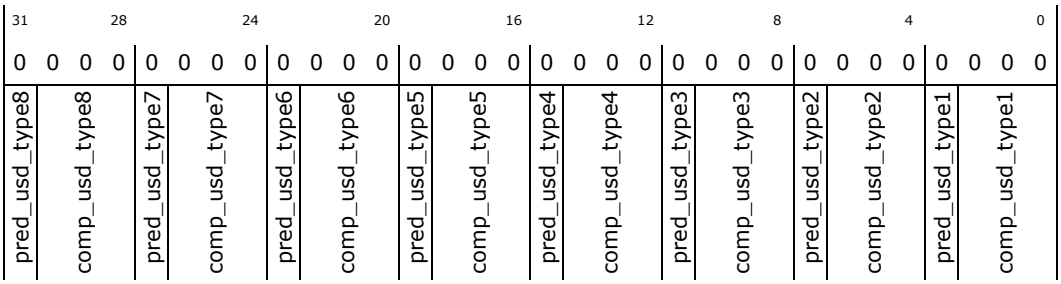
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0: [ISPMMADR] + 8080Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**pred_usd_type8:** prediction algorithm for vc=0, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0h RW	**comp_usd_type8:** compression format for vc=0, user defined type 8 data: value between 0 to 6. 0-no compression
27	0h RW	**pred_usd_type7:** prediction algorithm for vc=0, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0h RW	**comp_usd_type7:** compression format for vc=0, user defined type 7 data: value between 0 to 6. 0-no compression
23	0h RW	**pred_usd_type6:** prediction algorithm for vc=0, user defined type 6 data: 0 -) pred1, 1 -) pred2
22:20	0h RW	**comp_usd_type6:** compression format for vc=0, user defined type 6 data: value between 0 to 6. 0-no compression
19	0h RW	**pred_usd_type5:** prediction algorithm for vc=0, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0h RW	**comp_usd_type5:** compression format for vc=0, user defined type 5 data: value between 0 to 6. 0-no compression
15	0h RW	**pred_usd_type4:** prediction algorithm for vc=0, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0h RW	**comp_usd_type4:** compression format for vc=0, user defined type 4 data: value between 0 to 6. 0-no compression
11	0h RW	**pred_usd_type3:** prediction algorithm for vc=0, user defined type 3 data: 0 -) pred1, 1 -) pred2

Bit Range	Default & Access	Description
10:8	0h RW	**comp_usd_type3:** compression format for vc=0, user defined type 3 data: value between 0 to 6. 0-no compression
7	0h RW	**pred_usd_type2:** prediction algorithm for vc=0, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0h RW	**comp_usd_type2:** compression format for vc=0, user defined type 2 data: value between 0 to 6. 0-no compression
3	0h RW	**pred_usd_type1:** prediction algorithm for vc=0, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for vc=0, user defined type 1 data: value between 0 to 6. 0-no compression

3.7.680 reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1)—Offset 80810h

Compression scheme register for virtual channel 1

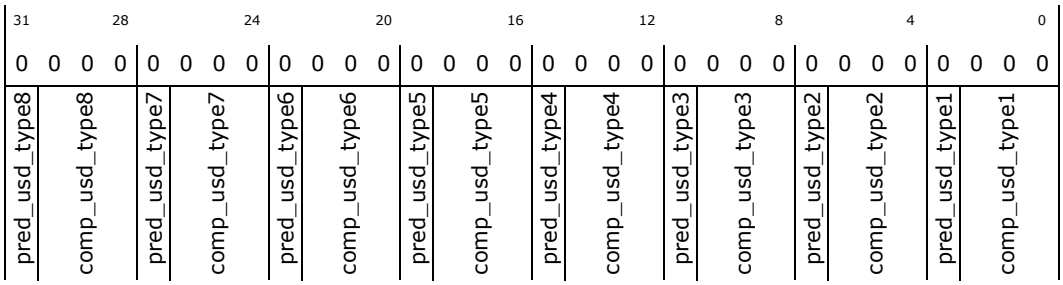
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1: [ISPMMADR] + 80810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**pred_usd_type8:** prediction algorithm for vc=1, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0h RW	**comp_usd_type8:** compression format for vc=1, user defined type 8 data: value between 0 to 6. 0-no compression
27	0h RW	**pred_usd_type7:** prediction algorithm for vc=1, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0h RW	**comp_usd_type7:** compression format for vc=1, user defined type 7 data: value between 0 to 6. 0-no compression

Bit Range	Default & Access	Description
23	0h RW	**pred_usd_type6:** prediction algorithm for vc=1, user defined type 6 data: 0 -) pred1, 1 -) pred2
22:20	0h RW	**comp_usd_type6:** compression format for vc=1, user defined type 6 data: value between 0 to 6. 0-no compression
19	0h RW	**pred_usd_type5:** prediction algorithm for vc=1, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0h RW	**comp_usd_type5:** compression format for vc=1, user defined type 5 data: value between 0 to 6. 0-no compression
15	0h RW	**pred_usd_type4:** prediction algorithm for vc=1, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0h RW	**comp_usd_type4:** compression format for vc=1, user defined type 4 data: value between 0 to 6. 0-no compression
11	0h RW	**pred_usd_type3:** prediction algorithm for vc=1, user defined type 3 data: 0 -) pred1, 1 -) pred2
10:8	0h RW	**comp_usd_type3:** compression format for vc=1, user defined type 3 data: value between 0 to 6. 0-no compression
7	0h RW	**pred_usd_type2:** prediction algorithm for vc=1, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0h RW	**comp_usd_type2:** compression format for vc=1, user defined type 2 data: value between 0 to 6. 0-no compression
3	0h RW	**pred_usd_type1:** prediction algorithm for vc=1, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for vc=1, user defined type 1 data: value between 0 to 6. 0-no compression

3.7.681 reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2)—Offset 80814h

Compression scheme register for virtual channel 0

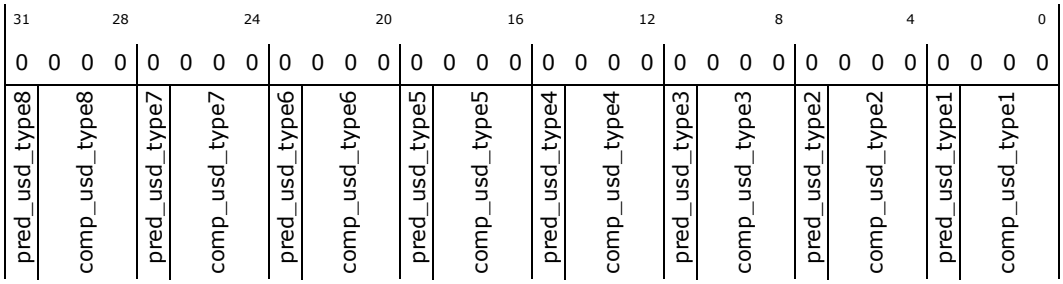
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2: [ISPMMADR] + 80814h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**pred_usd_type8:** prediction algorithm for vc=2, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0h RW	**comp_usd_type8:** compression format for vc=2, user defined type 8 data: value between 0 to 6. 0-no compression
27	0h RW	**pred_usd_type7:** prediction algorithm for vc=2, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0h RW	**comp_usd_type7:** compression format for vc=2, user defined type 7 data: value between 0 to 6. 0-no compression
23	0h RW	**pred_usd_type6:** prediction algorithm for vc=2, user defined type 6 data: 0 -) pred1, 1 -) pred2
22:20	0h RW	**comp_usd_type6:** compression format for vc=2, user defined type 6 data: value between 0 to 6. 0-no compression
19	0h RW	**pred_usd_type5:** prediction algorithm for vc=2, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0h RW	**comp_usd_type5:** compression format for vc=2, user defined type 5 data: value between 0 to 6. 0-no compression
15	0h RW	**pred_usd_type4:** prediction algorithm for vc=2, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0h RW	**comp_usd_type4:** compression format for vc=2, user defined type 4 data: value between 0 to 6. 0-no compression
11	0h RW	**pred_usd_type3:** prediction algorithm for vc=2, user defined type 3 data: 0 -) pred1, 1 -) pred2
10:8	0h RW	**comp_usd_type3:** compression format for vc=2, user defined type 3 data: value between 0 to 6. 0-no compression
7	0h RW	**pred_usd_type2:** prediction algorithm for vc=2, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0h RW	**comp_usd_type2:** compression format for vc=2, user defined type 2 data: value between 0 to 6. 0-no compression
3	0h RW	**pred_usd_type1:** prediction algorithm for vc=2, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for vc=2, user defined type 1 data: value between 0 to 6. 0-no compression

3.7.682 reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3)—Offset 80818h

Compression scheme register for virtual channel 0

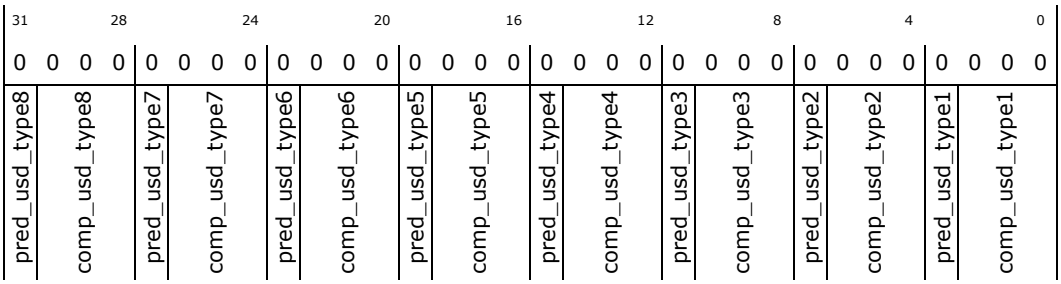
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3: [ISPMMADR] + 80818h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**pred_usd_type8:** prediction algorithm for vc=3, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0h RW	**comp_usd_type8:** compression format for vc=3, user defined type 8 data: value between 0 to 6. 0-no compression
27	0h RW	**pred_usd_type7:** prediction algorithm for vc=3, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0h RW	**comp_usd_type7:** compression format for vc=3, user defined type 7 data: value between 0 to 6. 0-no compression
23	0h RW	**pred_usd_type6:** prediction algorithm for vc=3, user defined type 6 data: 0 -) pred1, 1 -) pred2
22:20	0h RW	**comp_usd_type6:** compression format for vc=3, user defined type 6 data: value between 0 to 6. 0-no compression
19	0h RW	**pred_usd_type5:** prediction algorithm for vc=3, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0h RW	**comp_usd_type5:** compression format for vc=3, user defined type 5 data: value between 0 to 6. 0-no compression
15	0h RW	**pred_usd_type4:** prediction algorithm for vc=3, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0h RW	**comp_usd_type4:** compression format for vc=3, user defined type 4 data: value between 0 to 6. 0-no compression
11	0h RW	**pred_usd_type3:** prediction algorithm for vc=3, user defined type 3 data: 0 -) pred1, 1 -) pred2

Bit Range	Default & Access	Description
10:8	0h RW	**comp_usd_type3:** compression format for vc=3, user defined type 3 data: value between 0 to 6. 0-no compression
7	0h RW	**pred_usd_type2:** prediction algorithm for vc=3, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0h RW	**comp_usd_type2:** compression format for vc=3, user defined type 2 data: value between 0 to 6. 0-no compression
3	0h RW	**pred_usd_type1:** prediction algorithm for vc=3, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for vc=3, user defined type 1 data: value between 0 to 6. 0-no compression

3.7.683 reg_inp_sys_csi_receiver_csi_sh_be_sel_be_type (inp_sys_csi_receiver_csi_sh_be_sel_be)—Offset 8081Ch

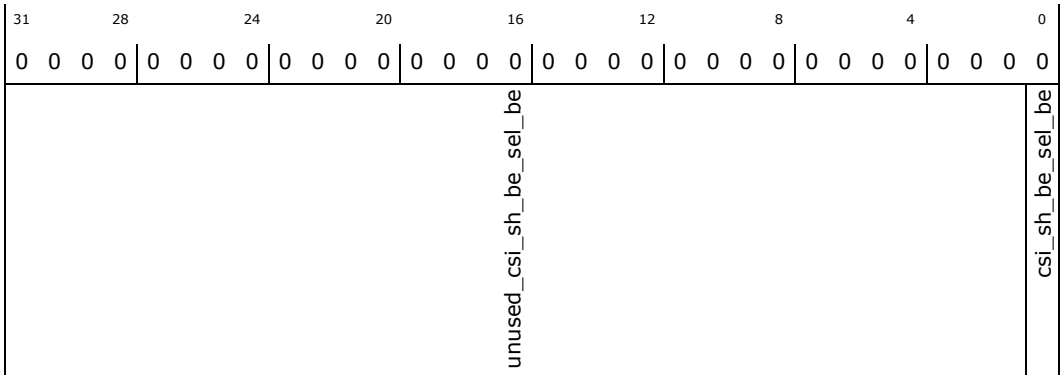
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_sel_be: [ISPMMADR] + 8081Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_csi_sh_be_sel_be:** Unused
0	0h RW	**csi_sh_be_sel_be:** Selects which CSI Receiver Backend to use 0-Arasan Backend, 1-Silicon Hive Backend

3.7.684 reg_inp_sys_csi_receiver_csi_sh_be_raw16_reg_type (inp_sys_csi_receiver_csi_sh_be_raw16_reg)—Offset 80820h

Configuration register for RAW 16 data type decode

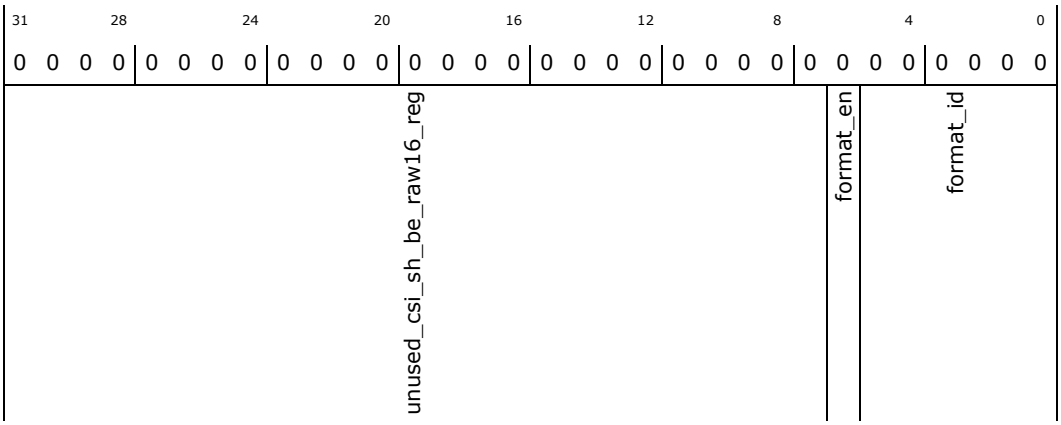
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_raw16_reg: [ISPMMADR] + 80820h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**unused_csi_sh_be_raw16_reg:** Unused
6	0h RW	**format_en:** enable RAW 16 type decode
5:0	0h RW	**format_id:** data id for RAW 16

3.7.685 reg_inp_sys_csi_receiver_csi_sh_be_raw18_reg_type (inp_sys_csi_receiver_csi_sh_be_raw18_reg)—Offset 80824h

Configuration register for RAW 18 data type decode

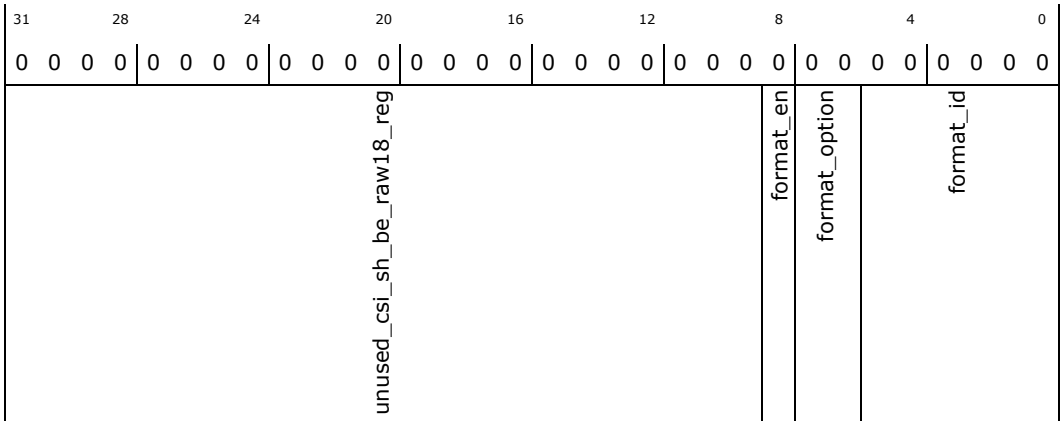
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_raw18_reg: [ISPMMADR] + 80824h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_csi_sh_be_raw18_reg:** Unused
8	0h RW	**format_en:** enable RAW 16 type decode
7:6	0h RW	**format_option:** format option for RAW 18 data type: 3 options possible (1,2,3)
5:0	0h RW	**format_id:** data id for RAW 16

3.7.686 reg_inp_sys_csi_receiver_csi_sh_be_force_raw8_reg_type (inp_sys_csi_receiver_csi_sh_be_force_raw8_reg)—Offset 80828h

Force RAW8(byte) decoding for LONG data packets

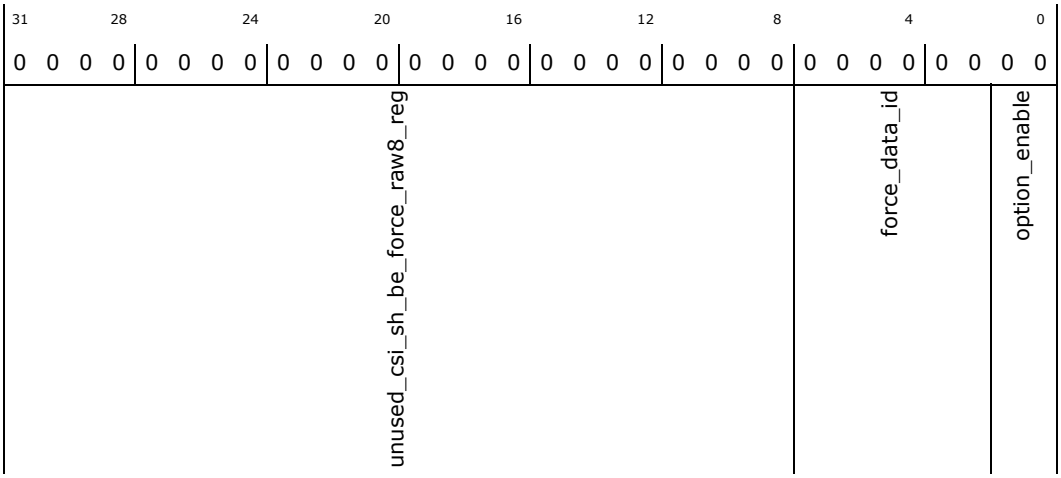
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_force_raw8_reg: [ISPMMADR] + 80828h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_sh_be_force_raw8_reg:** Unused
7:2	0h RW	**force_data_id:** Data_id that should be forced to RAW8
1:0	0h RW	**option_enable:** 00-Do not force anything in RAW8 mode. 01-force all data types in RAW8 mode, 11-force only packets with data_id force_data_id to RAW8 mode

3.7.687 reg_inp_sys_csi_receiver_csi_sh_be_irq_stat_reg_type (inp_sys_csi_receiver_csi_sh_be_irq_stat_reg)—Offset 8082Ch

IRQ status register

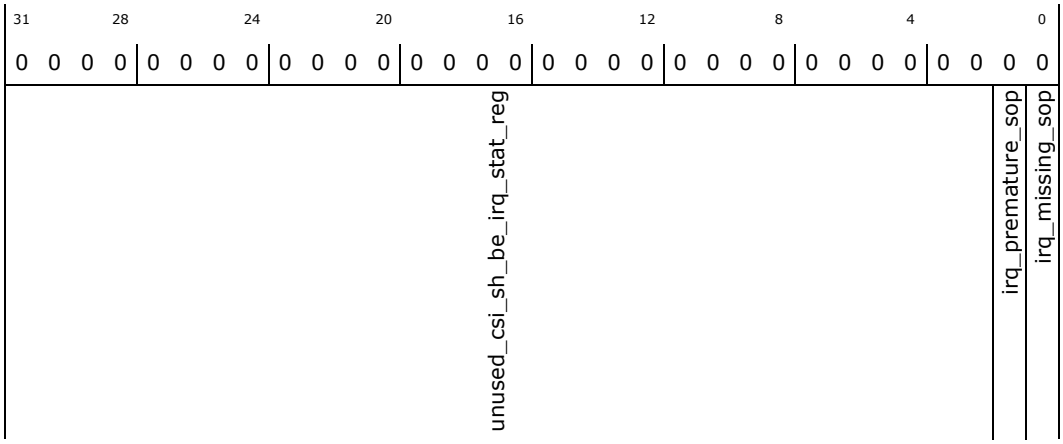
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_irq_stat_reg: [ISPMMADR] + 8082Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_csi_sh_be_irq_stat_reg:** Unused
1	0h RO	**irq_premature_sop:** If '1', sh_be has detected a premature sop
0	0h RO	**irq_missing_sop:** If '1', sh_be has detected a missing sop

3.7.688 reg_inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg_type (inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg)—Offset 80830h

IRQ status clear register

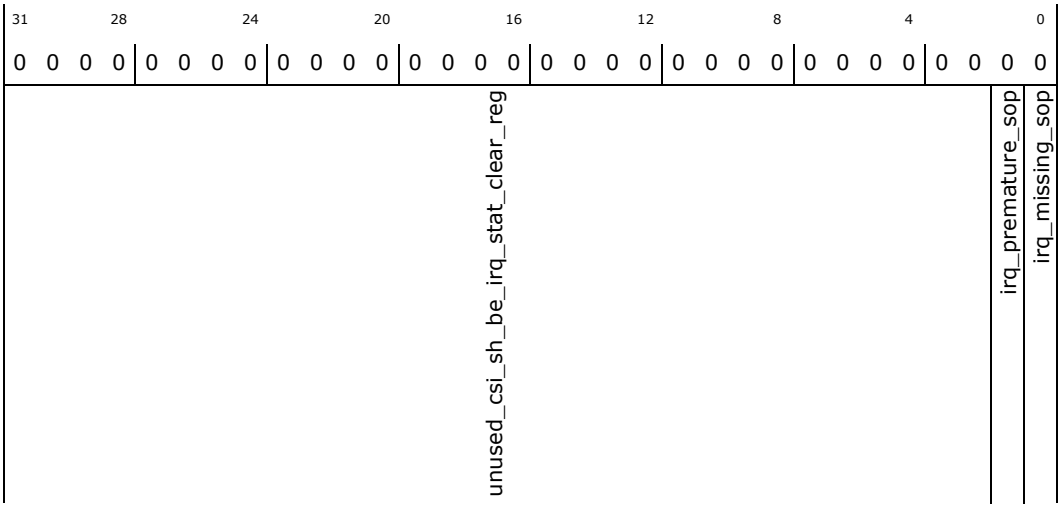
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg: [ISPMMADR] + 80830h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_csi_sh_be_irq_stat_clear_reg:** Unused
1	0h WO	**irq_premature_sop:** A '1' written into this field, clears the premature_sop field to '0'
0	0h WO	**irq_missing_sop:** A '1' written into this field, clears the irq_missing_sop field to '0'

3.7.689 reg_inp_sys_csi_receiver_csi_sh_be_custom_enable_reg_type (inp_sys_csi_receiver_csi_sh_be_custom_enable_reg)—Offset 80834h

Enable custom mode decoding for LONG data packets

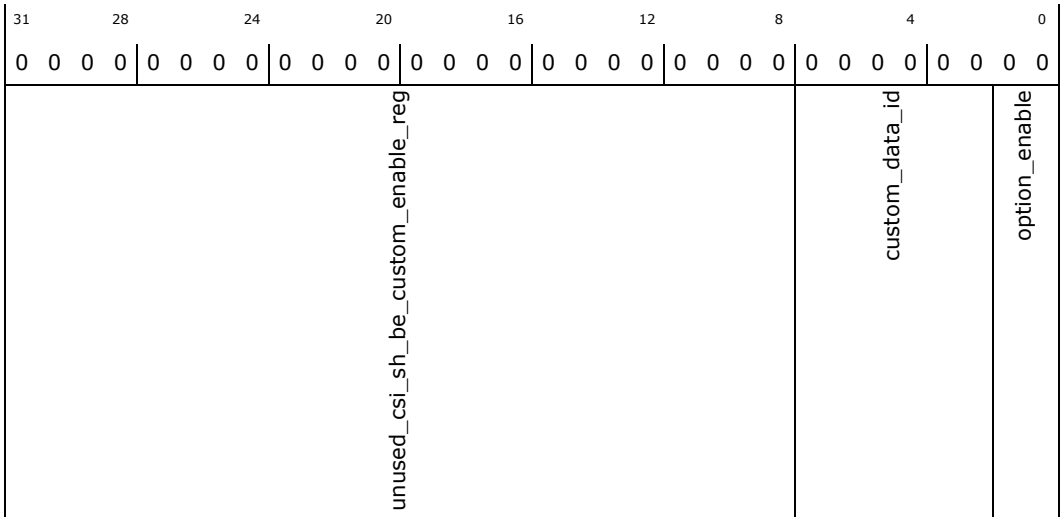
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_custom_enable_reg: [ISPMMADR] + 80834h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_sh_be_custom_enable_reg:** Unused
7:2	0h RW	**custom_data_id:** Data_id that should be processed in custom mode
1:0	0h RW	**option_enable:** 00-Custom mode switched off. 01-all data types in custom mode, 11-only packets with data id custom_data_id are processed in custom mode

3.7.690 reg_inp_sys_capt_unit_a_reg_CaptStartMode_type (inp_sys_capt_unit_a_reg_CaptStartMode)—Offset 81000h

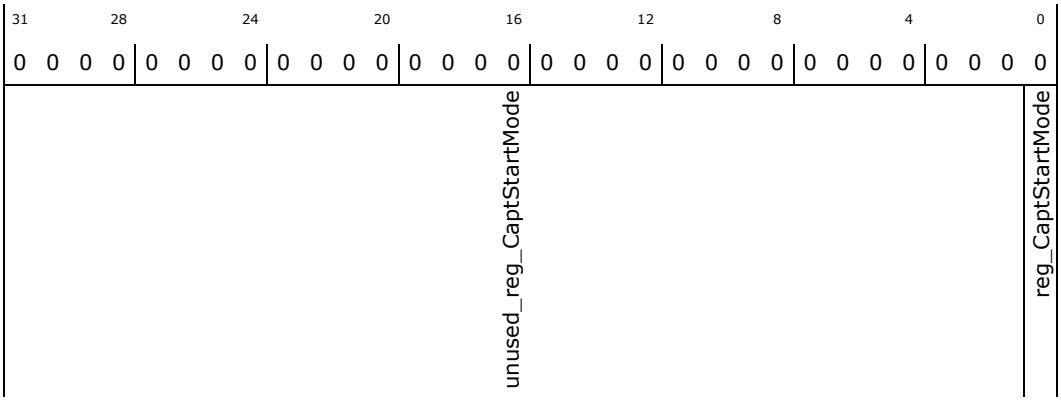
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_CaptStartMode: [ISPMMADR] + 81000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_CaptStartMode:** Unused
0	0h RW	**reg_CaptStartMode:** Synchronize on any packet header or on a frame start

3.7.691 reg_inp_sys_capt_unit_a_reg_Capt_Start_Addr_type (inp_sys_capt_unit_a_reg_Capt_Start_Addr)—Offset 81004h

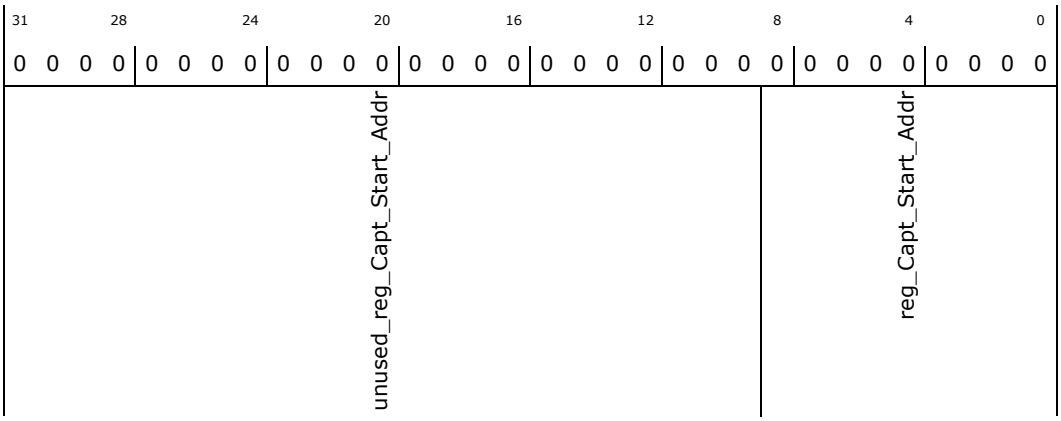
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Start_Addr: [ISPMMADR] + 81004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Start_Addr:** Unused
8:0	0h RW	**reg_Capt_Start_Addr:** Start Address of first memory region

3.7.692 reg_inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size)—Offset 81008h

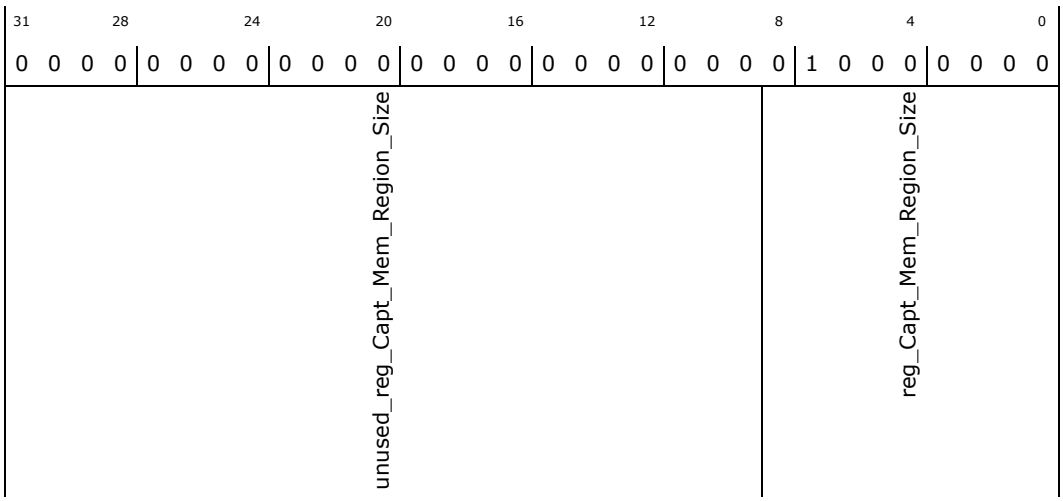
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size: [ISPMMADR] + 81008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Mem_Region_Size:** Unused
8:0	080h RW	**reg_Capt_Mem_Region_Size:** Memory region size

3.7.693 reg_inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions)—Offset 8100Ch

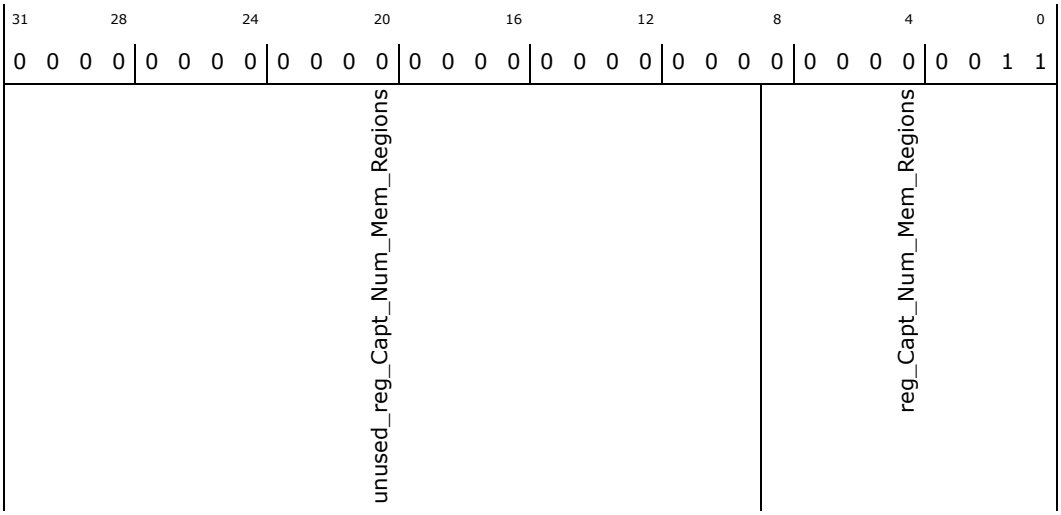
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions: [ISPMMADR] + 8100Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Num_Mem_Regions:** Unused
8:0	003h RW	**reg_Capt_Num_Mem_Regions:** Number of memory regions

3.7.694 reg_inp_sys_capt_unit_a_reg_Capt_Init_type (inp_sys_capt_unit_a_reg_Capt_Init)—Offset 81010h

Initialize Capture Unit

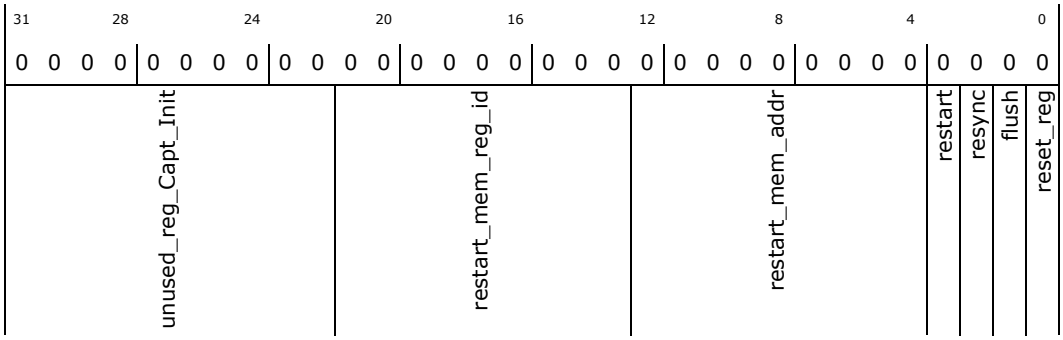
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Init: [ISPMMADR] + 81010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_reg_Capt_Init:** Unused
21:13	0h WO	**restart_mem_reg_id:** Restart Memory Region ID
12:4	0h WO	**restart_mem_addr:** Restart Memory Address
3	0h WO	**restart:** Restart Capture Unit
2	0h WO	**resync:** Resynchronize Capture Unit
1	0h WO	**flush:** Flush Internal Buffers
0	0h WO	**reset_reg:** Reset Status Registers

3.7.695 reg_inp_sys_capt_unit_a_reg_Capt_Start_type (inp_sys_capt_unit_a_reg_Capt_Start)—Offset 81014h

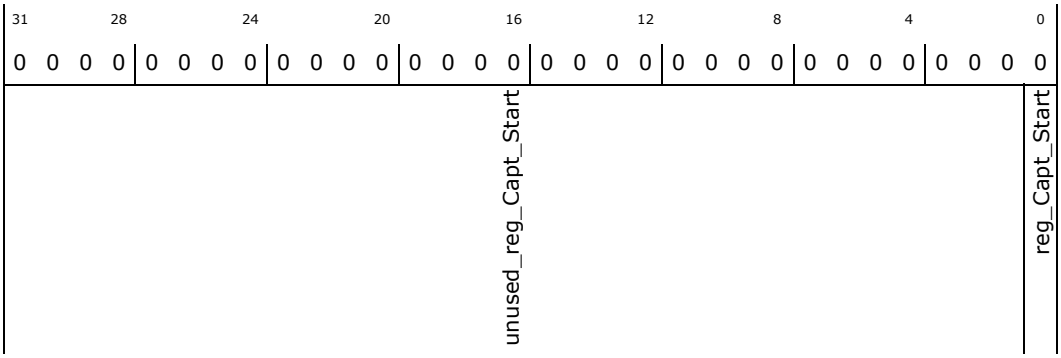
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Start: [ISPMMADR] + 81014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Start:** Unused
0	0h WO	**reg_Capt_Start:** Start Capturing

3.7.696 reg_inp_sys_capt_unit_a_reg_Capt_Stop_type (inp_sys_capt_unit_a_reg_Capt_Stop)—Offset 81018h

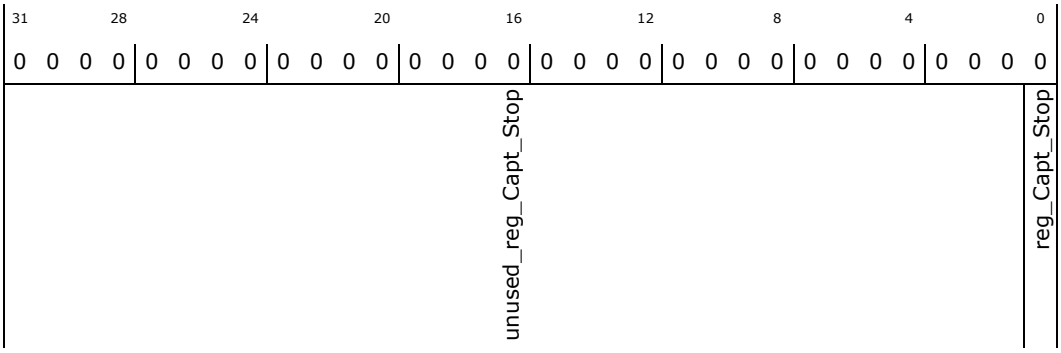
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Stop: [ISPMMADR] + 81018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Stop:** Unused
0	0h WO	**reg_Capt_Stop:** Stop Capturing

3.7.697 reg_inp_sys_capt_unit_a_reg_Capt_Packet_Length_type (inp_sys_capt_unit_a_reg_Capt_Packet_Length)—Offset 8101Ch

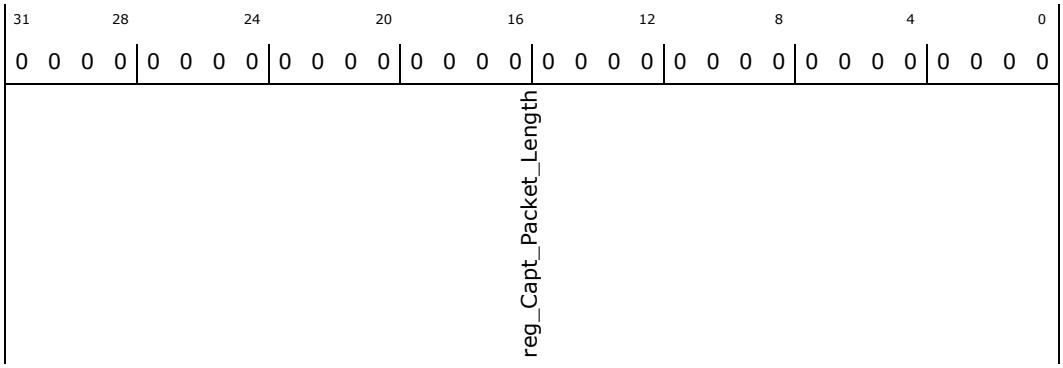
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Packet_Length: [ISPMMADR] + 8101Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Packet_Length:** Packet length of multi_word packet (MWP) as decoded from packet header

3.7.698 reg_inp_sys_capt_unit_a_reg_Capt_Received_Length_type (inp_sys_capt_unit_a_reg_Capt_Received_Length)—Offset 81020h

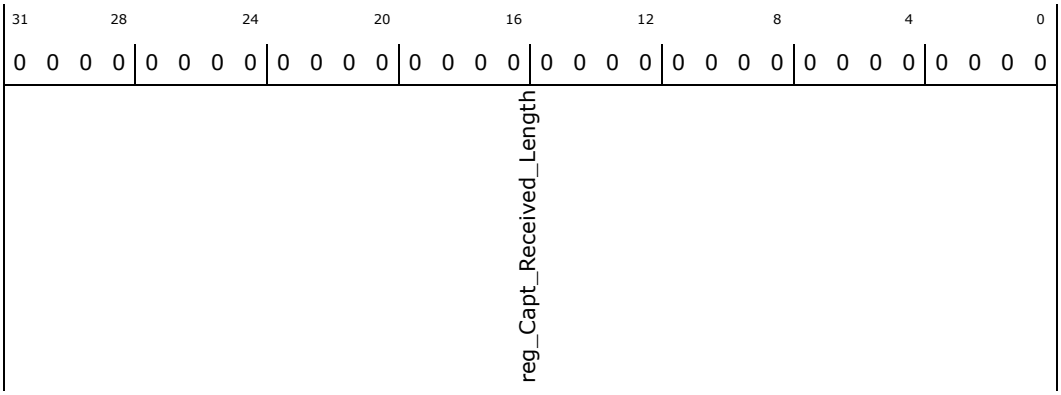
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Received_Length: [ISPMMADR] + 81020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Length:** (Incremental) received packet length of current multi-word packet (MWP)

3.7.699 reg_inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets)—Offset 81024h

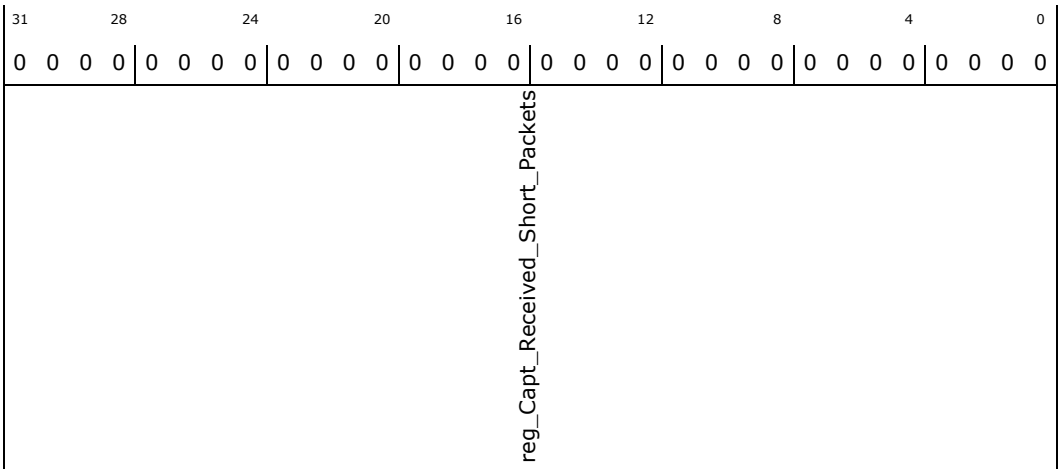
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets: [ISPMMADR] + 81024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Short_Packets:** Number of received short packets

3.7.700 reg_inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets)—Offset 81028h

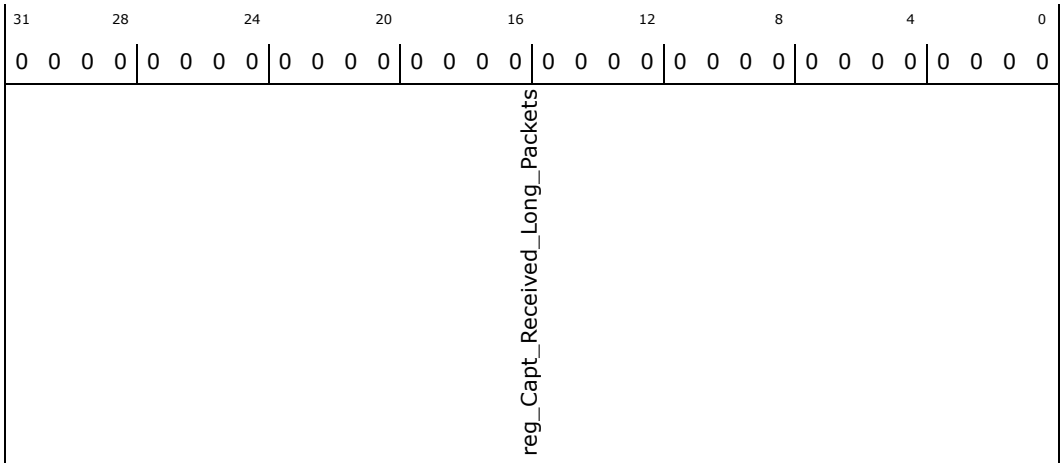
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets: [ISPMMADR] + 81028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Long_Packets:** Number of received long packets

3.7.701 reg_inp_sys_capt_unit_a_reg_Capt_Last_Command_type (inp_sys_capt_unit_a_reg_Capt_Last_Command)—Offset 8102Ch

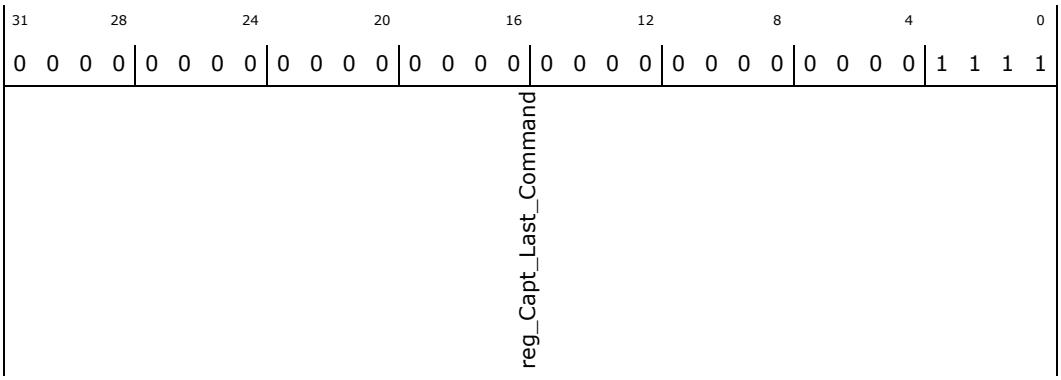
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Last_Command: [ISPMMADR] + 8102Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Command:** Last command token accepted

3.7.702 reg_inp_sys_capt_unit_a_reg_Capt_Next_Command_type (inp_sys_capt_unit_a_reg_Capt_Next_Command)—Offset 81030h

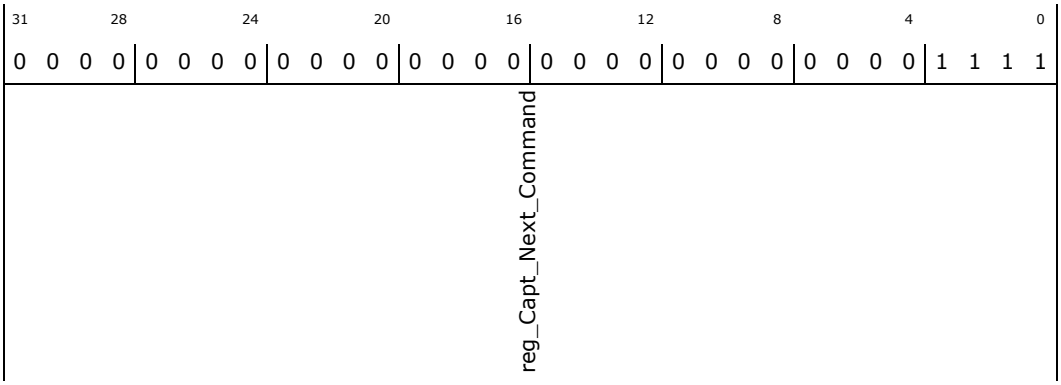
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Next_Command: [ISPMMADR] + 81030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Command:** Next command token to be accepted

3.7.703 reg_inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge)—Offset 81034h

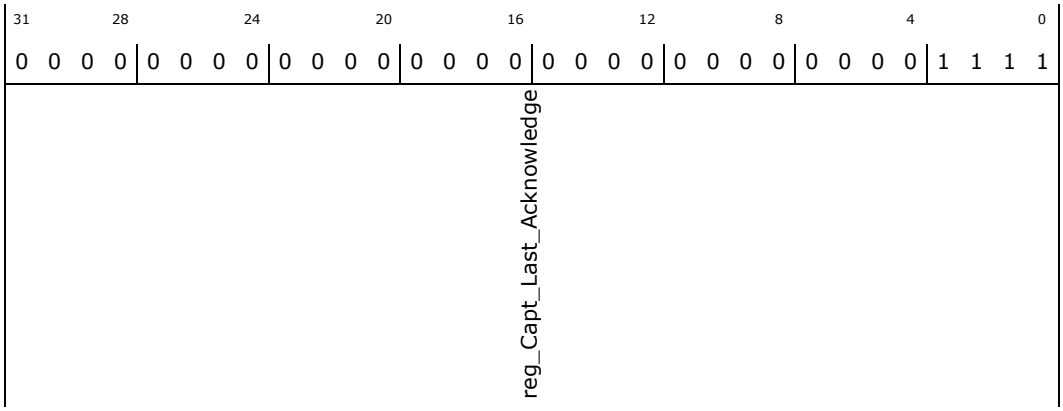
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge: [ISPMMADR] + 81034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Acknowledge:** Last acknowledge token send

3.7.704 reg_inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge)—Offset 81038h

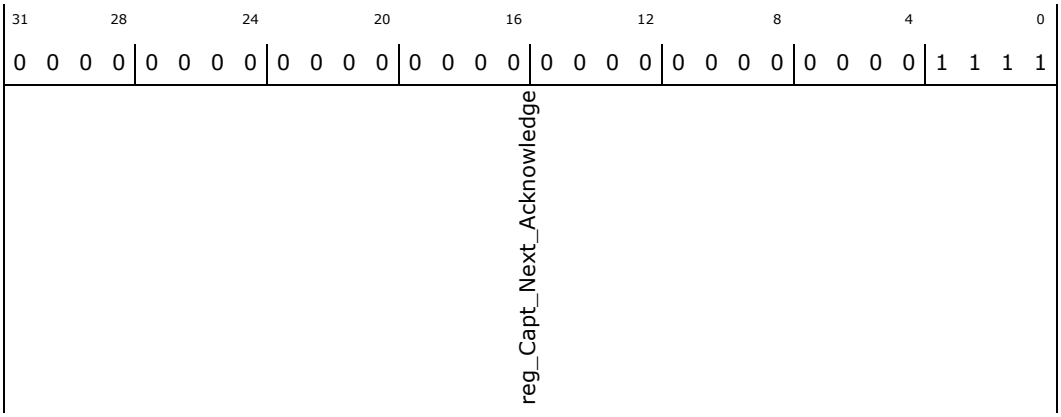
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge: [ISPMMADR] + 81038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Acknowledge:** Next acknowledge token to be send

3.7.705 reg_inp_sys_capt_unit_a_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_a_reg_Capt_FSM_State_Info)—Offset 8103Ch

Capture Unit State Machine Information

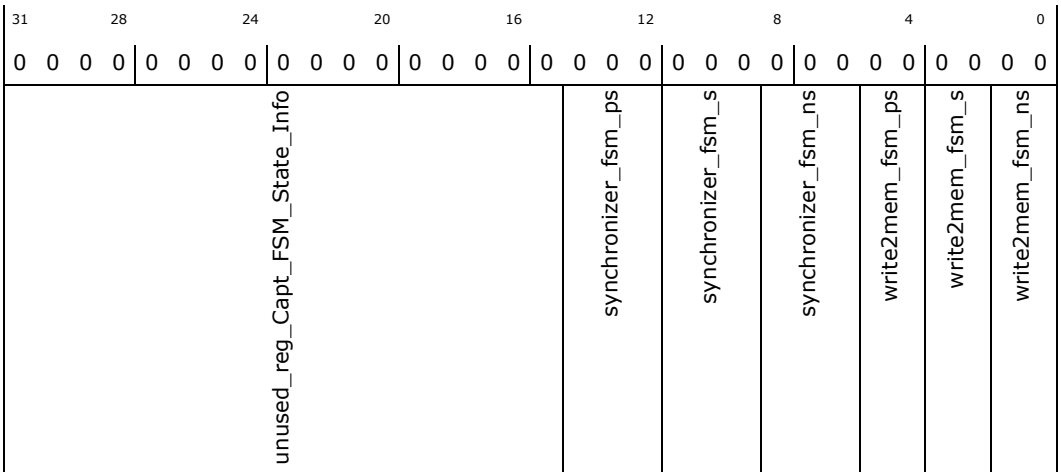
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_FSM_State_Info: [ISPMMADR] + 8103Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RW	**unused_reg_Capt_FSM_State_Info:** Unused
14:12	0h RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine
11:9	0h RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine
8:6	0h RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine
5:4	0h RO	**write2mem_fsm_ps:** Previous state of Write2Mem State Machine
3:2	0h RO	**write2mem_fsm_s:** Current state of Write2Mem State Machine
1:0	0h RO	**write2mem_fsm_ns:** Next state of Write2Mem State Machine

3.7.706 reg_inp_sys_capt_unit_b_reg_CaptStartMode_type (inp_sys_capt_unit_b_reg_CaptStartMode)—Offset 82000h

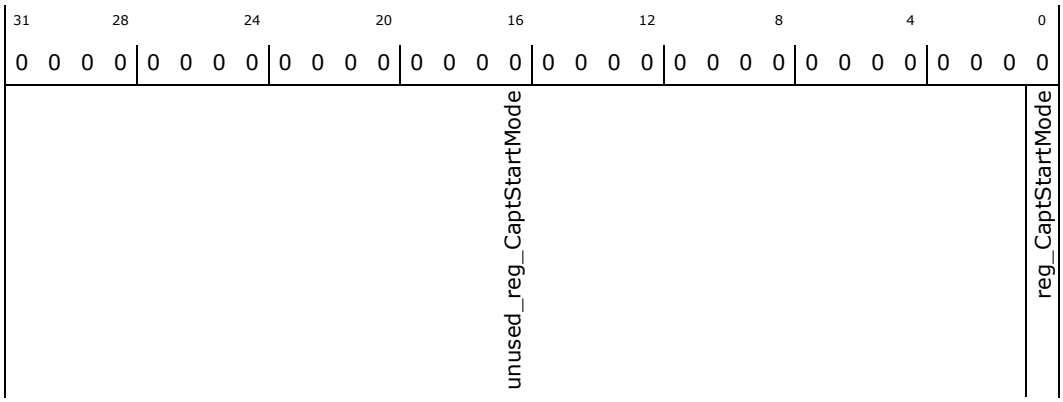
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_CaptStartMode: [ISPMMADR] + 82000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_CaptStartMode:** Unused
0	0h RW	**reg_CaptStartMode:** Synchronize on any packet header or on a frame start

3.7.707 reg_inp_sys_capt_unit_b_reg_Capt_Start_Addr_type (inp_sys_capt_unit_b_reg_Capt_Start_Addr)—Offset 82004h

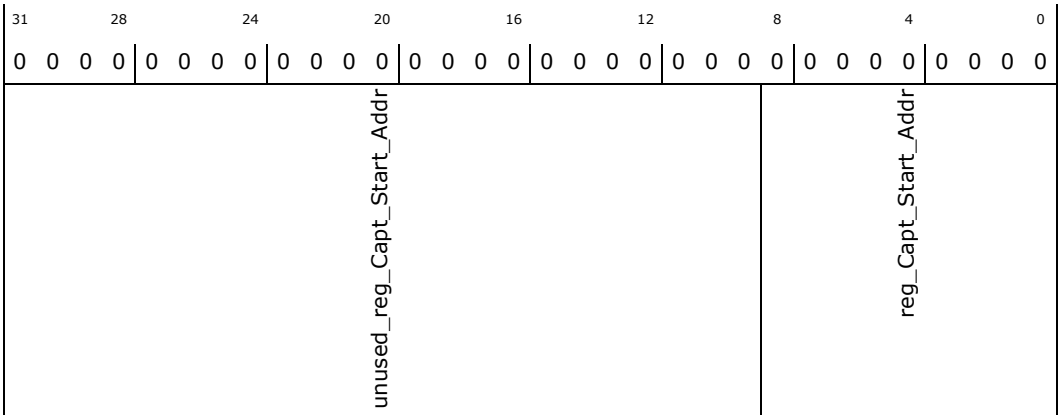
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Start_Addr: [ISPMMADR] + 82004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Start_Addr:** Unused
8:0	0h RW	**reg_Capt_Start_Addr:** Start Address of first memory region

3.7.708 reg_inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size)—Offset 82008h

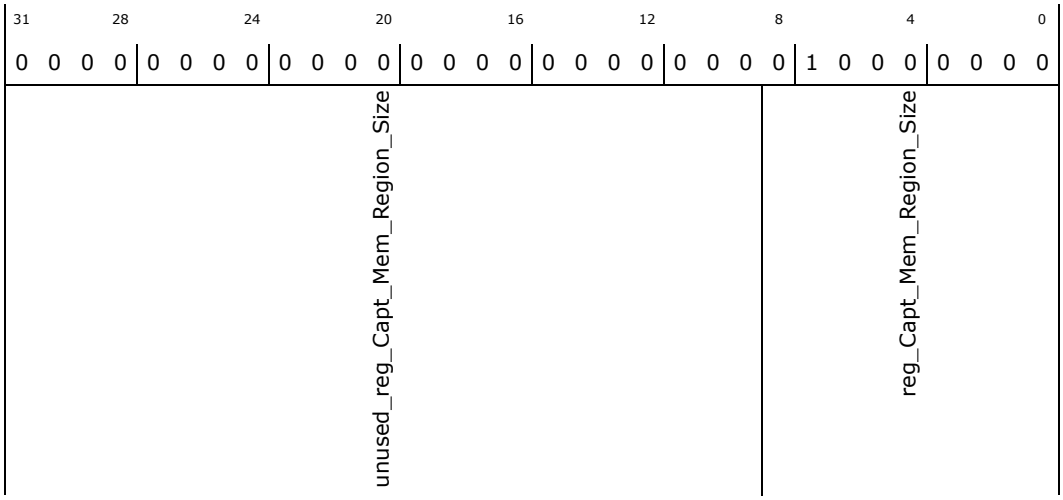
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size: [ISPMMADR] + 82008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Mem_Region_Size:** Unused
8:0	080h RW	**reg_Capt_Mem_Region_Size:** Memory region size

3.7.709 reg_inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions)—Offset 8200Ch

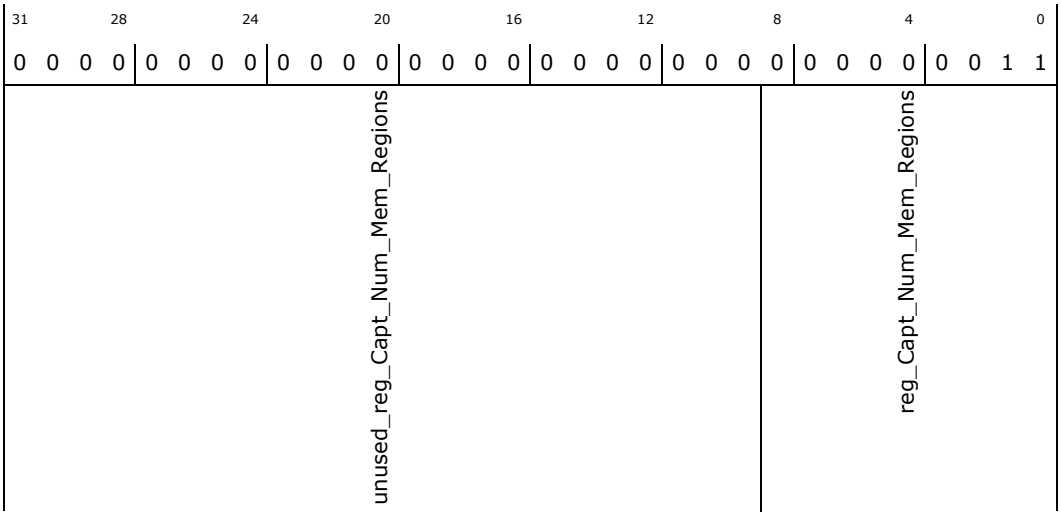
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions: [ISPMMADR] + 8200Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Num_Mem_Regions:** Unused
8:0	003h RW	**reg_Capt_Num_Mem_Regions:** Number of memory regions

3.7.710 reg_inp_sys_capt_unit_b_reg_Capt_Init_type (inp_sys_capt_unit_b_reg_Capt_Init)—Offset 82010h

Initialize Capture Unit

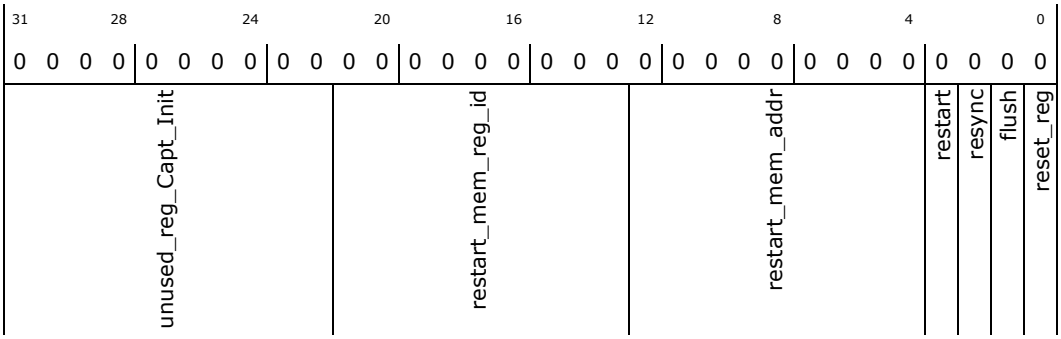
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Init: [ISPMMADR] + 82010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_reg_Capt_Init:** Unused
21:13	0h WO	**restart_mem_reg_id:** Restart Memory Region ID
12:4	0h WO	**restart_mem_addr:** Restart Memory Address
3	0h WO	**restart:** Restart Capture Unit
2	0h WO	**resync:** Resynchronize Capture Unit
1	0h WO	**flush:** Flush Internal Buffers
0	0h WO	**reset_reg:** Reset Status Registers

3.7.711 reg_inp_sys_capt_unit_b_reg_Capt_Start_type (inp_sys_capt_unit_b_reg_Capt_Start)—Offset 82014h

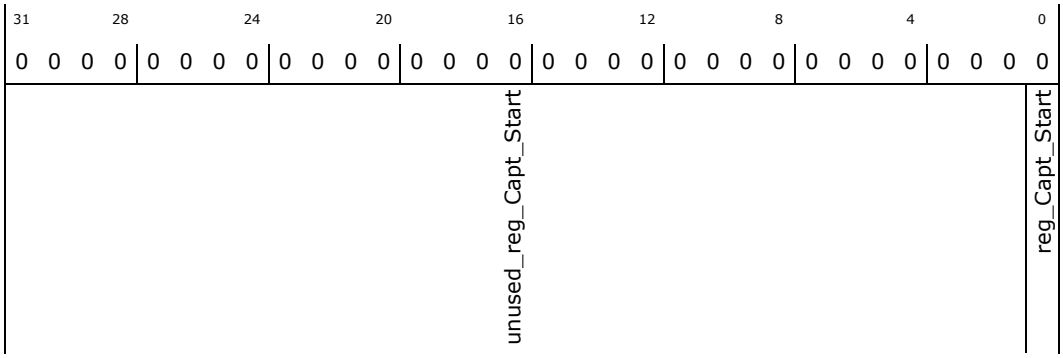
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Start: [ISPMMADR] + 82014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Start:** Unused
0	0h WO	**reg_Capt_Start:** Start Capturing

3.7.712 reg_inp_sys_capt_unit_b_reg_Capt_Stop_type (inp_sys_capt_unit_b_reg_Capt_Stop)—Offset 82018h

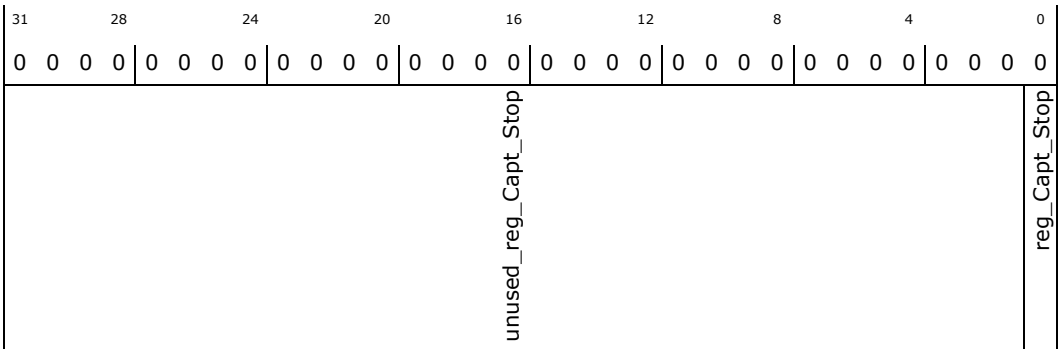
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Stop: [ISPMMADR] + 82018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Stop:** Unused
0	0h WO	**reg_Capt_Stop:** Stop Capturing

3.7.713 reg_inp_sys_capt_unit_b_reg_Capt_Packet_Length_type (inp_sys_capt_unit_b_reg_Capt_Packet_Length)—Offset 8201Ch

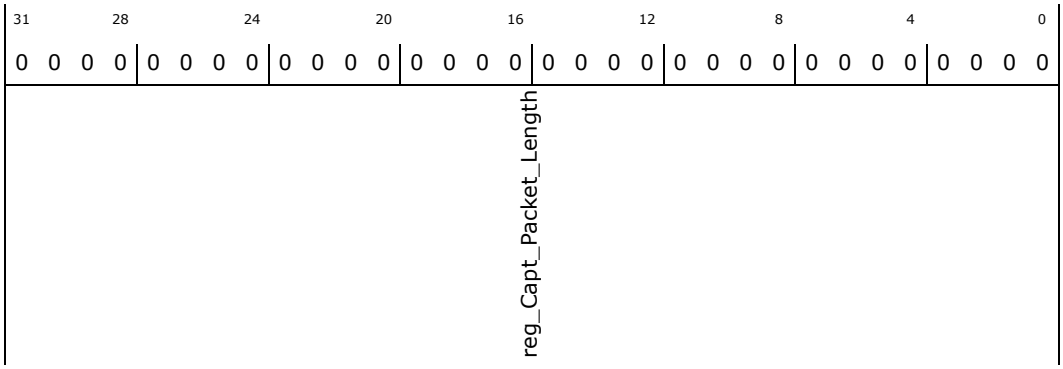
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Packet_Length: [ISPMMADR] + 8201Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Packet_Length:** Packet length of multi_word packet (MWP) as decoded from packet header

3.7.714 reg_inp_sys_capt_unit_b_reg_Capt_Received_Length_type (inp_sys_capt_unit_b_reg_Capt_Received_Length)—Offset 82020h

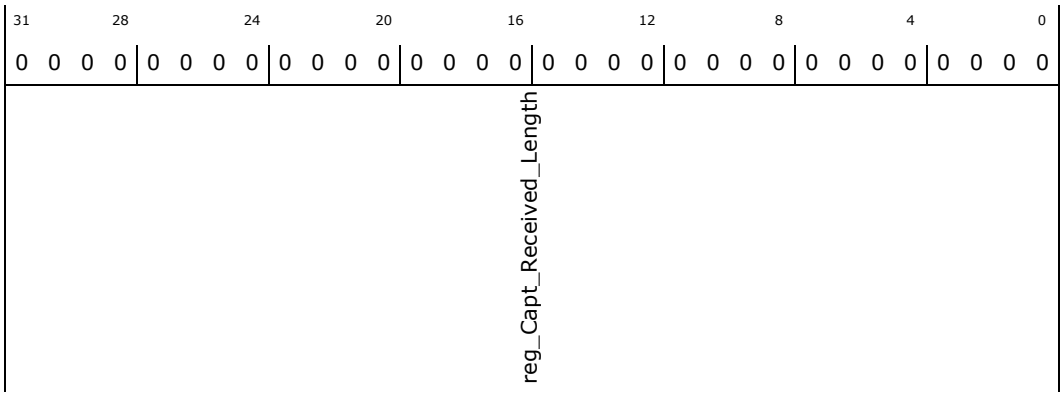
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Received_Length: [ISPMMADR] + 82020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Length:** (Incremental) received packet length of current multi-word packet (MWP)

3.7.715 reg_inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets)—Offset 82024h

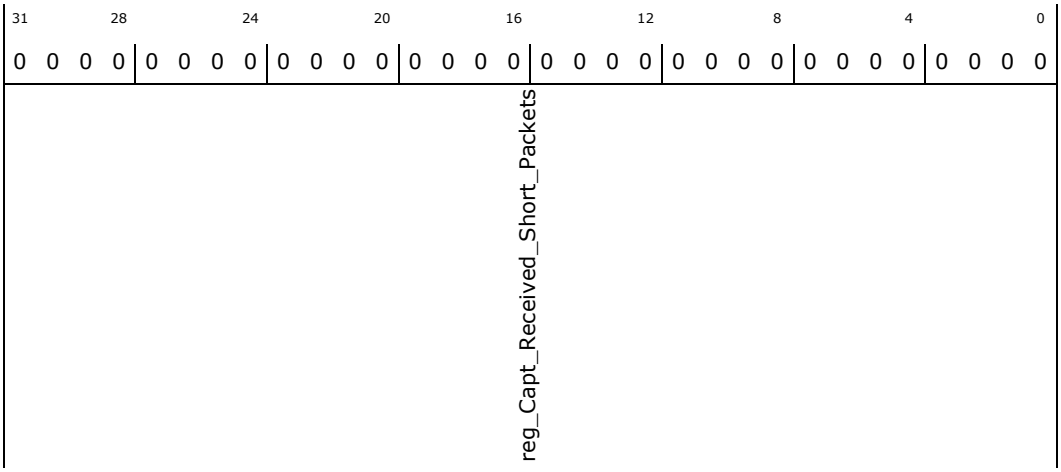
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets: [ISPMMADR] + 82024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Short_Packets:** Number of received short packets

3.7.716 reg_inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets)—Offset 82028h

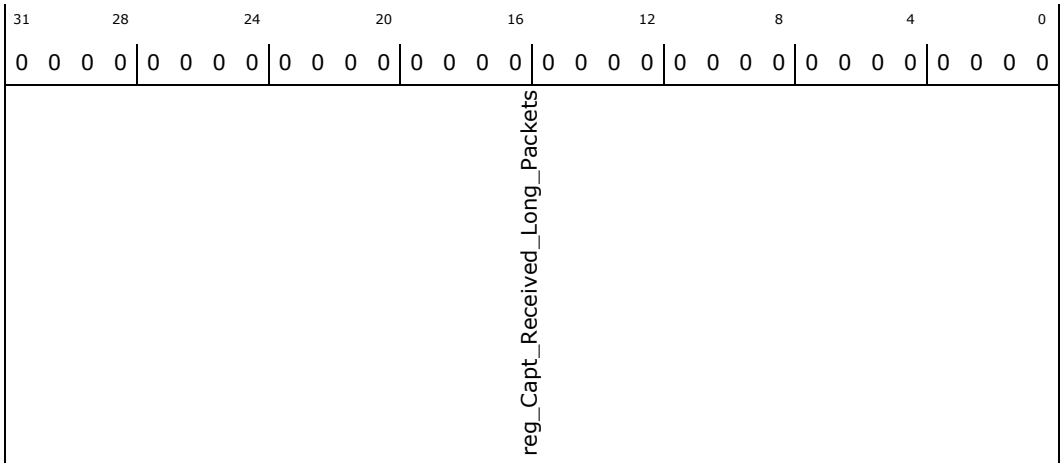
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets: [ISPMMADR] + 82028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Long_Packets:** Number of received long packets

3.7.717 reg_inp_sys_capt_unit_b_reg_Capt_Last_Command_type (inp_sys_capt_unit_b_reg_Capt_Last_Command)—Offset 8202Ch

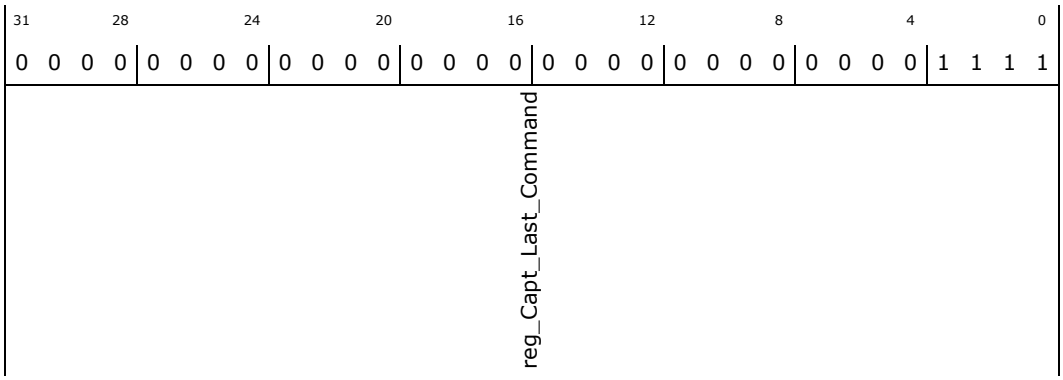
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Last_Command: [ISPMMADR] + 8202Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Command:** Last command token accepted

3.7.718 reg_inp_sys_capt_unit_b_reg_Capt_Next_Command_type (inp_sys_capt_unit_b_reg_Capt_Next_Command)—Offset 82030h

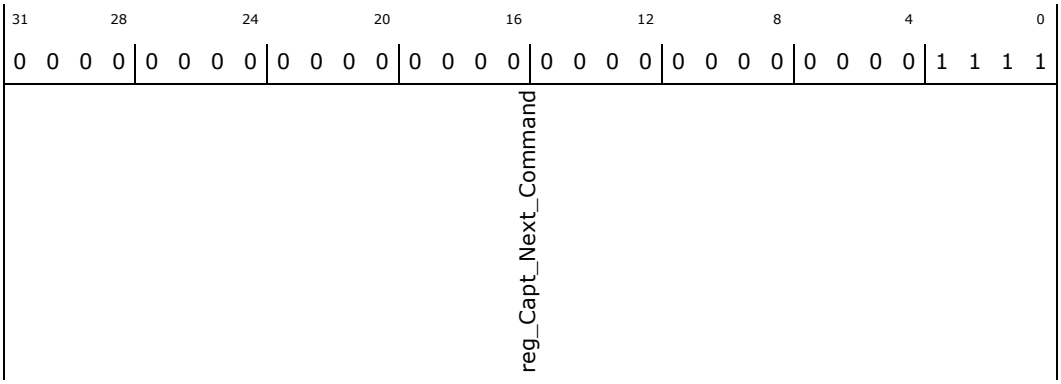
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Next_Command: [ISPMMADR] + 82030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Command:** Next command token to be accepted

3.7.719 reg_inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge)—Offset 82034h

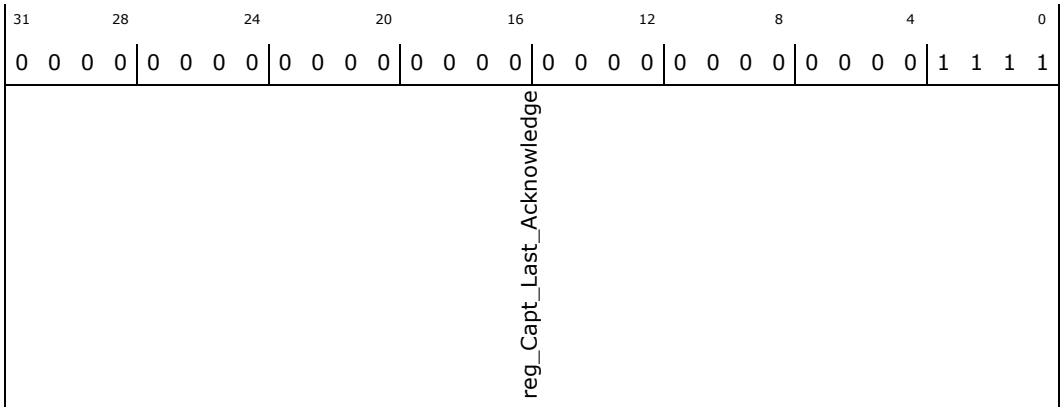
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge: [ISPMMADR] + 82034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Acknowledge:** Last acknowledge token send

3.7.720 reg_inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge)—Offset 82038h

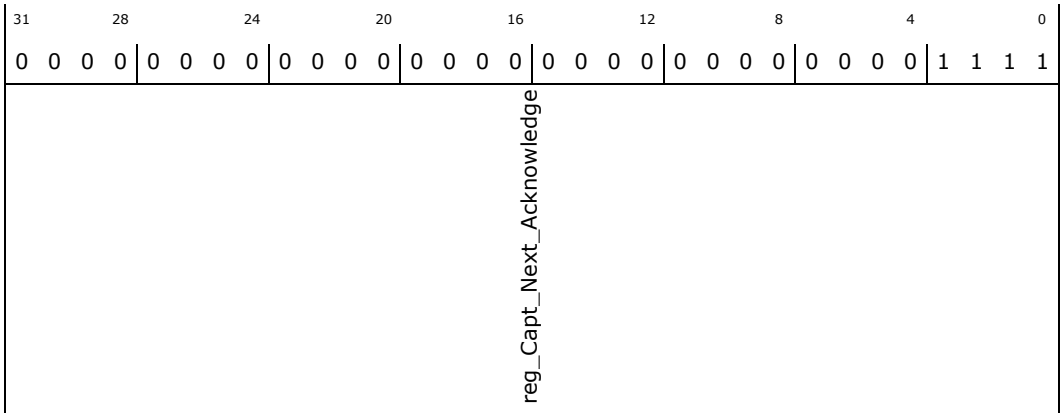
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge: [ISPMMADR] + 82038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Acknowledge:** Next acknowledge token to be send

3.7.721 reg_inp_sys_capt_unit_b_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_b_reg_Capt_FSM_State_Info)—Offset 8203Ch

Capture Unit State Machine Information

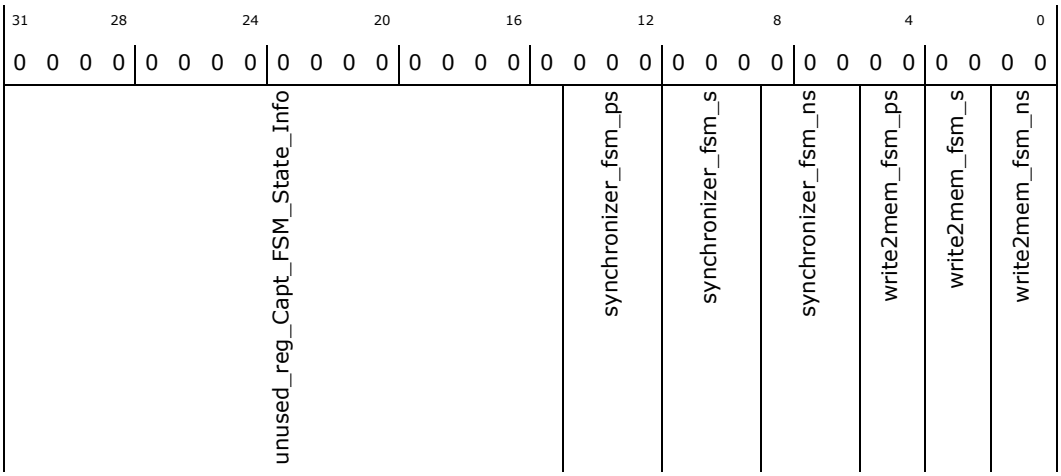
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_FSM_State_Info: [ISPMMADR] + 8203Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RW	**unused_reg_Capt_FSM_State_Info:** Unused
14:12	0h RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine
11:9	0h RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine
8:6	0h RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine
5:4	0h RO	**write2mem_fsm_ps:** Previous state of Write2Mem State Machine
3:2	0h RO	**write2mem_fsm_s:** Current state of Write2Mem State Machine
1:0	0h RO	**write2mem_fsm_ns:** Next state of Write2Mem State Machine

3.7.722 reg_inp_sys_capt_unit_c_reg_CaptStartMode_type (inp_sys_capt_unit_c_reg_CaptStartMode)—Offset 83000h

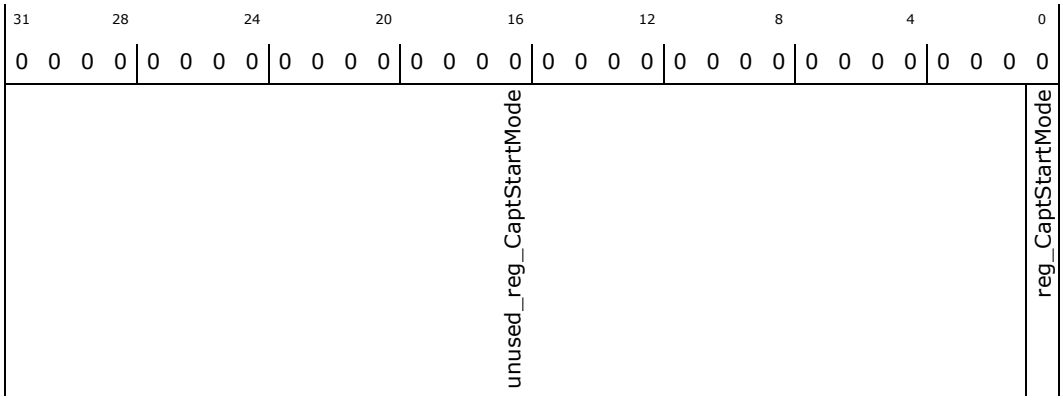
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_CaptStartMode: [ISPMMADR] + 83000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_CaptStartMode:** Unused
0	0h RW	**reg_CaptStartMode:** Synchronize on any packet header or on a frame start

3.7.723 reg_inp_sys_capt_unit_c_reg_Capt_Start_Addr_type (inp_sys_capt_unit_c_reg_Capt_Start_Addr)—Offset 83004h

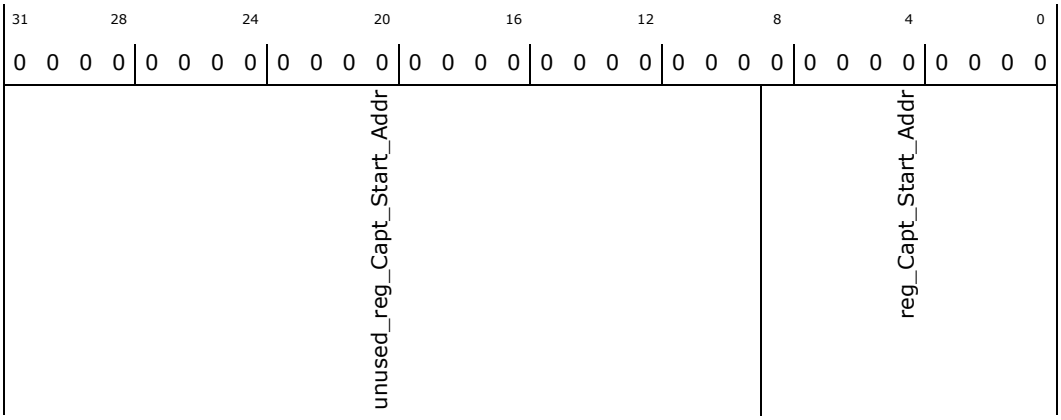
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Start_Addr: [ISPMMADR] + 83004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Start_Addr:** Unused
8:0	0h RW	**reg_Capt_Start_Addr:** Start Address of first memory region

3.7.724 reg_inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size)—Offset 83008h

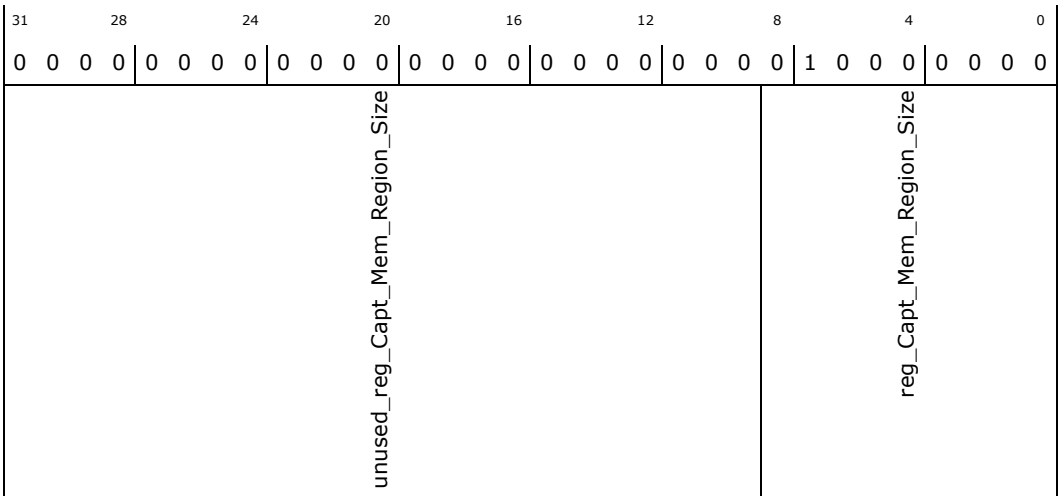
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size: [ISPMMADR] + 83008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Mem_Region_Size:** Unused
8:0	080h RW	**reg_Capt_Mem_Region_Size:** Memory region size

3.7.725 reg_inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions)—Offset 8300Ch

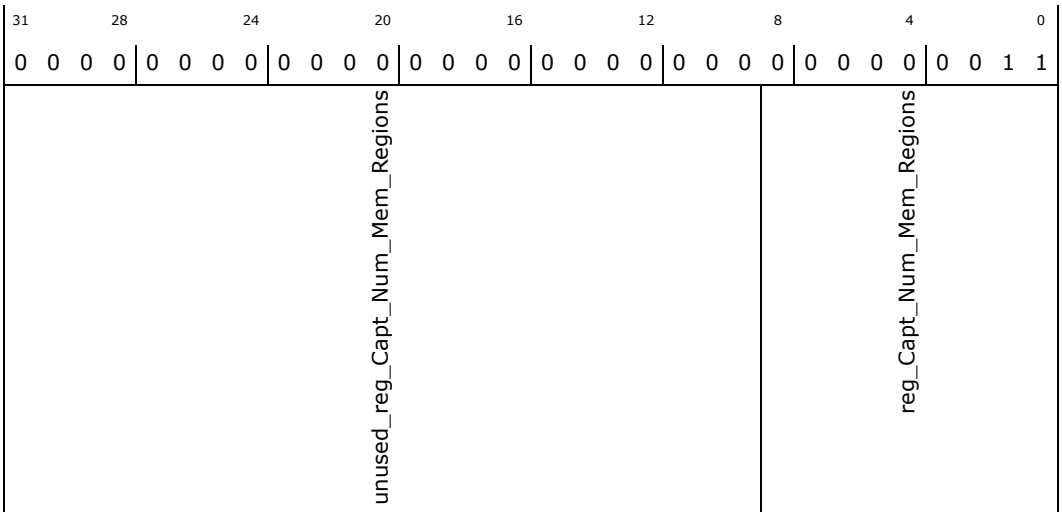
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions: [ISPMMADR] + 8300Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Num_Mem_Regions:** Unused
8:0	003h RW	**reg_Capt_Num_Mem_Regions:** Number of memory regions

3.7.726 reg_inp_sys_capt_unit_c_reg_Capt_Init_type (inp_sys_capt_unit_c_reg_Capt_Init)—Offset 83010h

Initialize Capture Unit

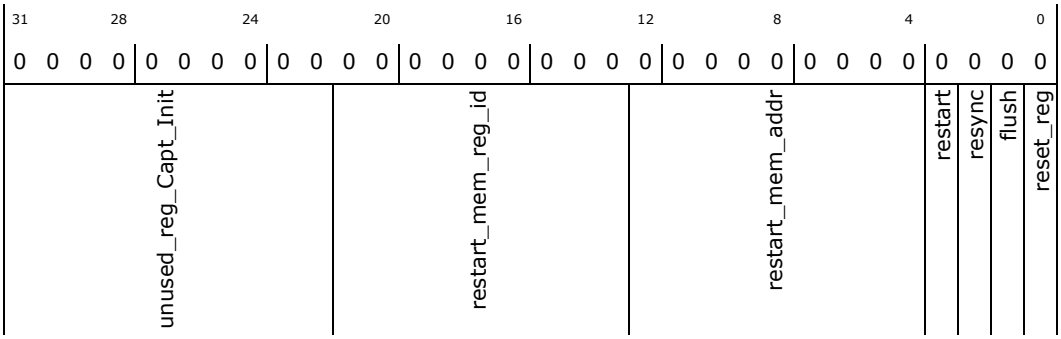
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Init: [ISPMMADR] + 83010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_reg_Capt_Init:** Unused
21:13	0h WO	**restart_mem_reg_id:** Restart Memory Region ID
12:4	0h WO	**restart_mem_addr:** Restart Memory Address
3	0h WO	**restart:** Restart Capture Unit
2	0h WO	**resync:** Resynchronize Capture Unit
1	0h WO	**flush:** Flush Internal Buffers
0	0h WO	**reset_reg:** Reset Status Registers

3.7.727 reg_inp_sys_capt_unit_c_reg_Capt_Start_type (inp_sys_capt_unit_c_reg_Capt_Start)—Offset 83014h

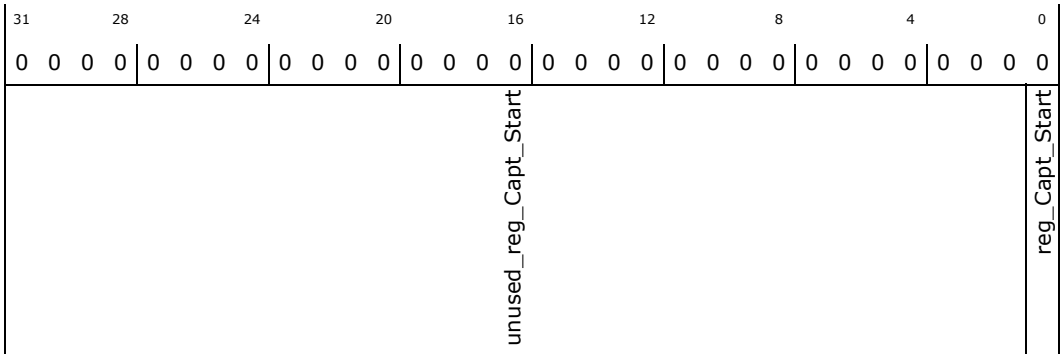
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Start: [ISPMMADR] + 83014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Start:** Unused
0	0h WO	**reg_Capt_Start:** Start Capturing

3.7.728 reg_inp_sys_capt_unit_c_reg_Capt_Stop_type (inp_sys_capt_unit_c_reg_Capt_Stop)—Offset 83018h

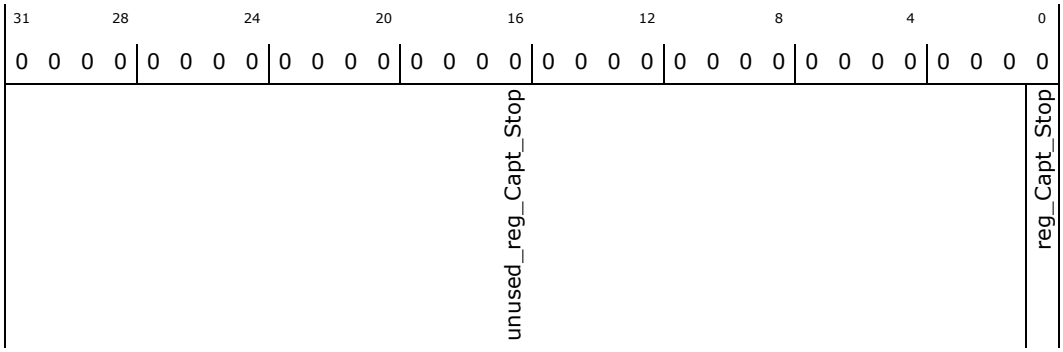
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Stop: [ISPMMADR] + 83018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Stop:** Unused
0	0h WO	**reg_Capt_Stop:** Stop Capturing

3.7.729 reg_inp_sys_capt_unit_c_reg_Capt_Packet_Length_type (inp_sys_capt_unit_c_reg_Capt_Packet_Length)—Offset 8301Ch

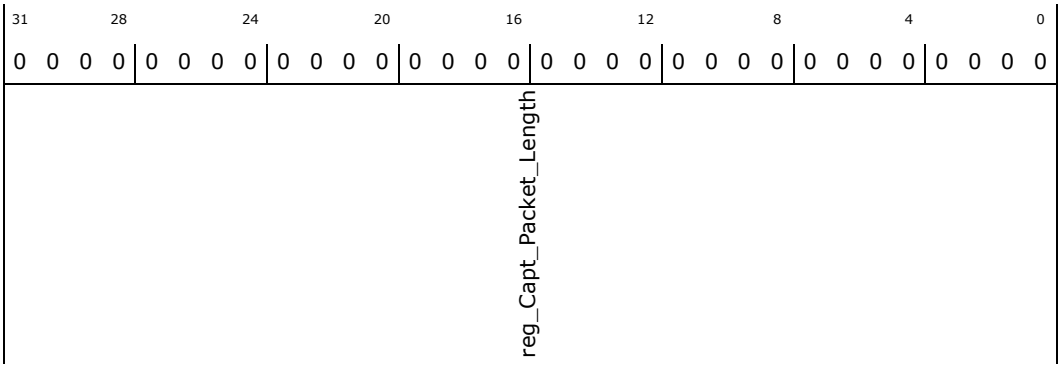
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Packet_Length: [ISPMMADR] + 8301Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Packet_Length:** Packet length of multi_word packet (MWP) as decoded from packet header

3.7.730 reg_inp_sys_capt_unit_c_reg_Capt_Received_Length_type (inp_sys_capt_unit_c_reg_Capt_Received_Length)—Offset 83020h

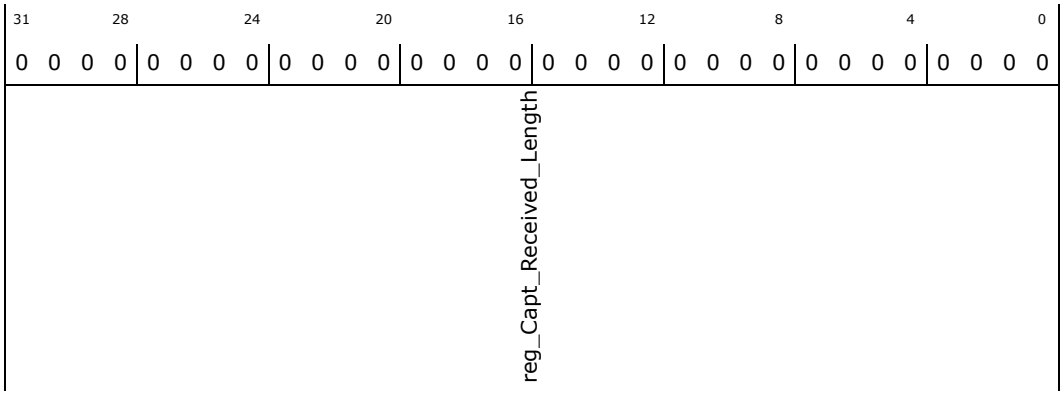
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Received_Length: [ISPMMADR] + 83020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Length:** (Incremental) received packet length of current multi-word packet (MWP)

3.7.731 reg_inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets)—Offset 83024h

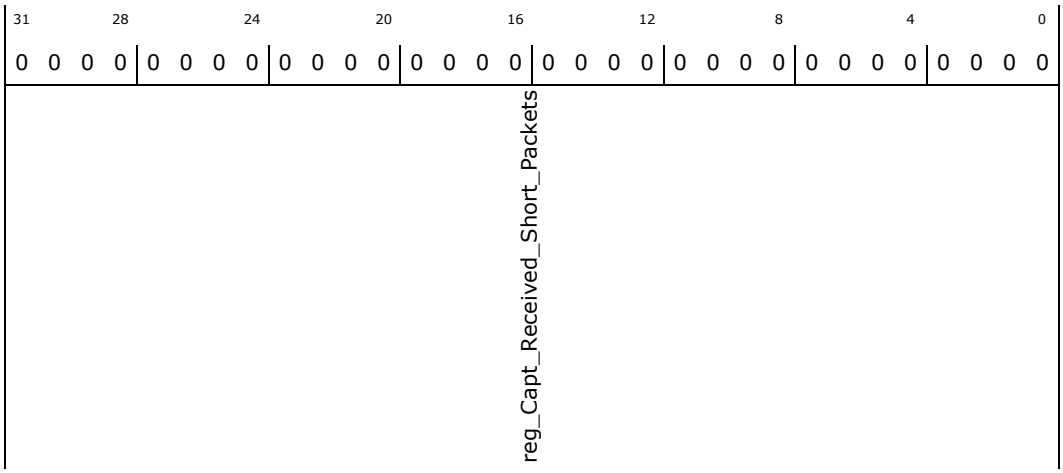
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets: [ISPMMADR] + 83024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Short_Packets:** Number of received short packets

3.7.732 reg_inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets)—Offset 83028h

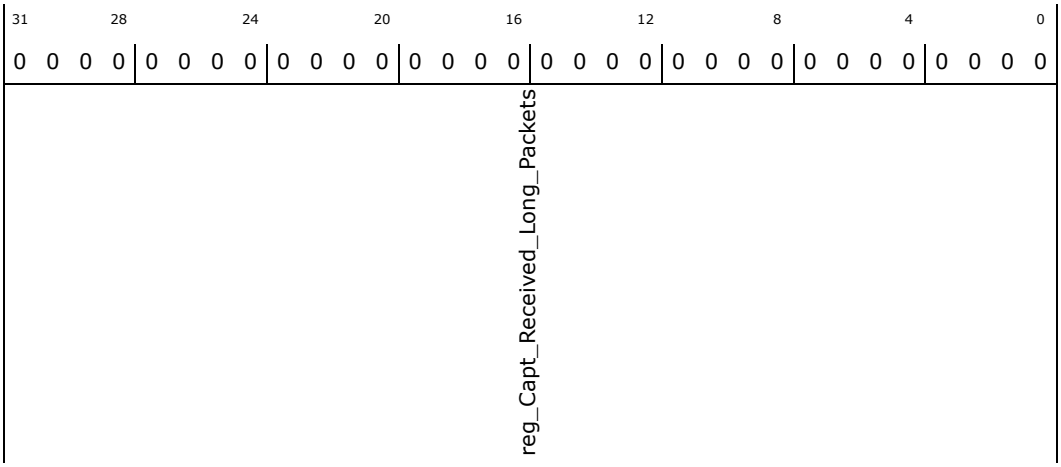
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets: [ISPMMADR] + 83028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Long_Packets:** Number of received long packets

3.7.733 reg_inp_sys_capt_unit_c_reg_Capt_Last_Command_type (inp_sys_capt_unit_c_reg_Capt_Last_Command)—Offset 8302Ch

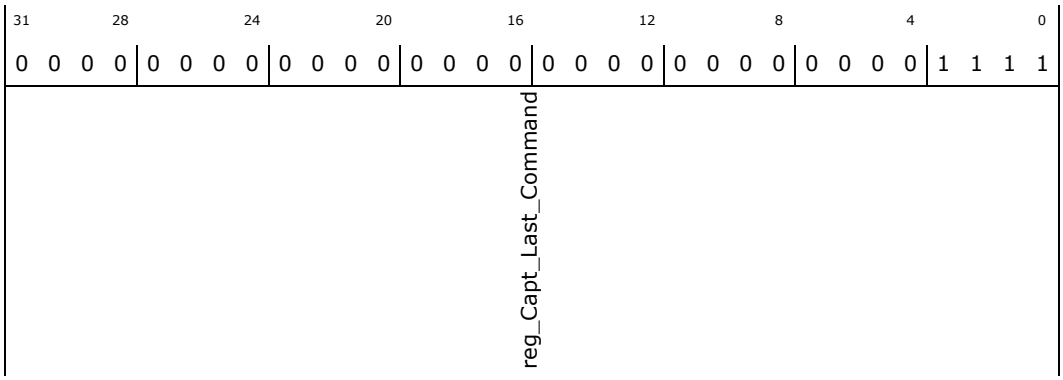
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Last_Command: [ISPMMADR] + 8302Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Command:** Last command token accepted

3.7.734 reg_inp_sys_capt_unit_c_reg_Capt_Next_Command_type (inp_sys_capt_unit_c_reg_Capt_Next_Command)—Offset 83030h

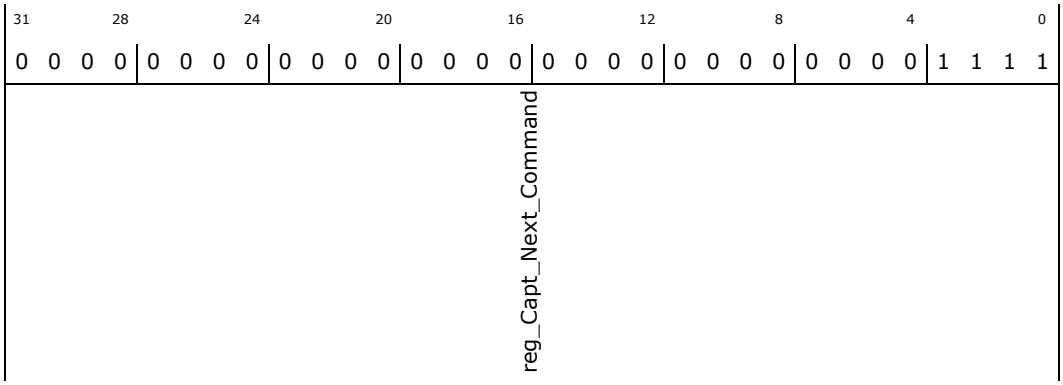
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Next_Command: [ISPMMADR] + 83030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Command:** Next command token to be accepted

3.7.735 reg_inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge)—Offset 83034h

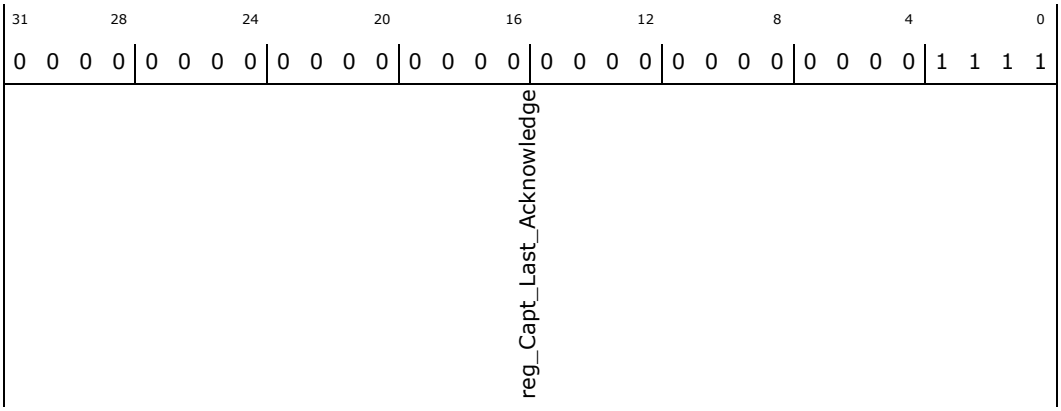
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge: [ISPMMADR] + 83034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Acknowledge:** Last acknowledge token send

3.7.736 reg_inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge)—Offset 83038h

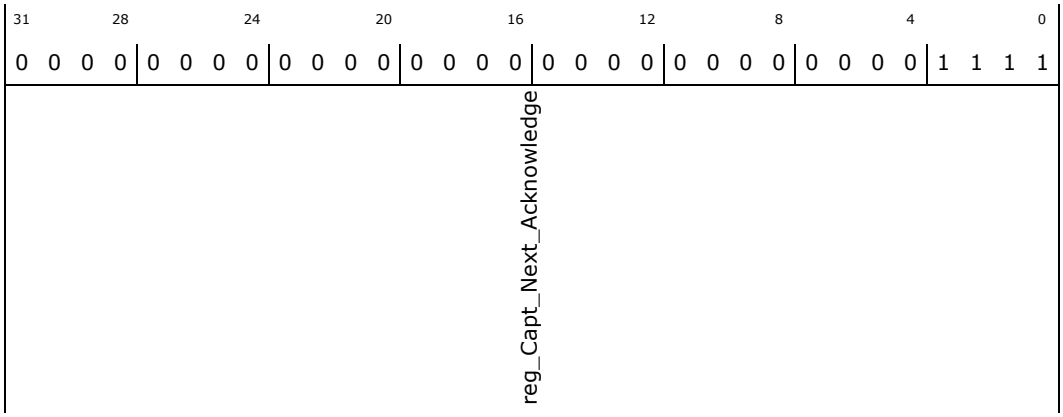
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge: [ISPMMADR] + 83038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Acknowledge:** Next acknowledge token to be send

3.7.737 reg_inp_sys_capt_unit_c_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_c_reg_Capt_FSM_State_Info)—Offset 8303Ch

Capture Unit State Machine Information

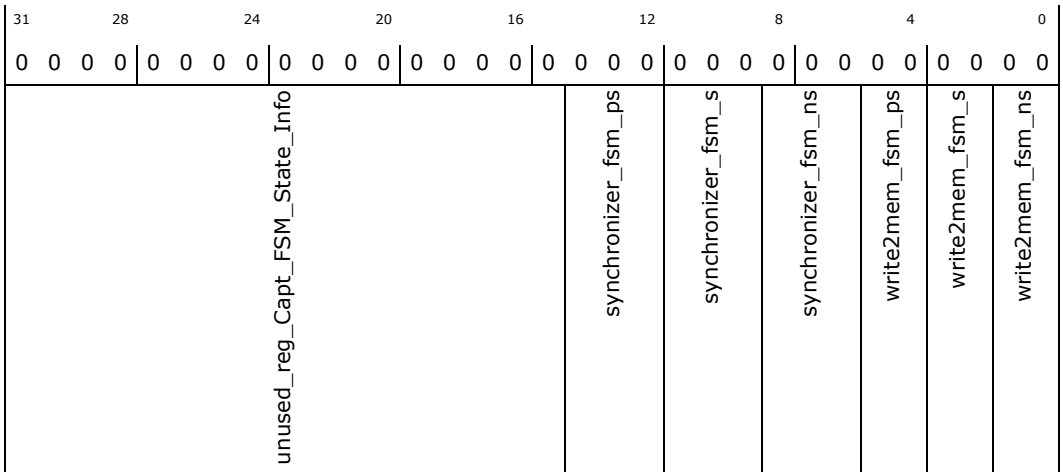
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_FSM_State_Info: [ISPMMADR] + 8303Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RW	**unused_reg_Capt_FSM_State_Info:** Unused
14:12	0h RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine
11:9	0h RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine
8:6	0h RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine
5:4	0h RO	**write2mem_fsm_ps:** Previous state of Write2Mem State Machine
3:2	0h RO	**write2mem_fsm_s:** Current state of Write2Mem State Machine
1:0	0h RO	**write2mem_fsm_ns:** Next state of Write2Mem State Machine

3.7.738 reg_inp_sys_acq_unit_reg_Acq_Start_Addr_type (inp_sys_acq_unit_reg_Acq_Start_Addr)—Offset 84000h

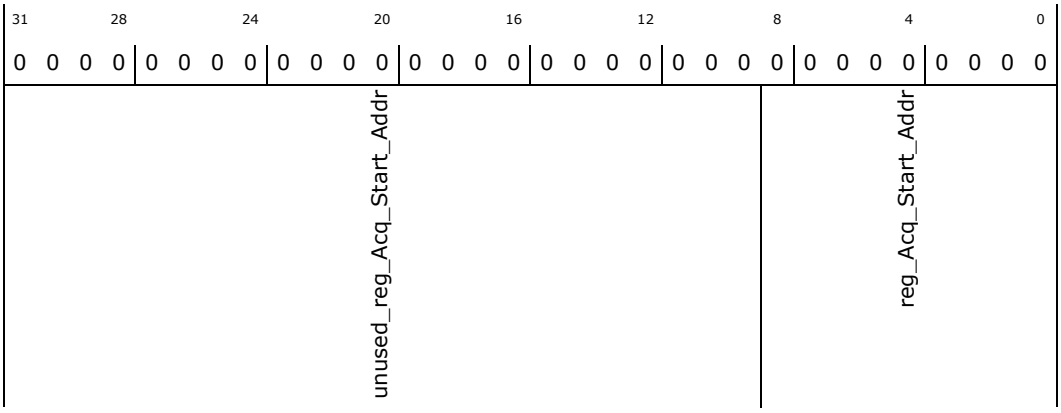
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Start_Addr: [ISPMMADR] + 84000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Acq_Start_Addr:** Unused
8:0	0h RW	**reg_Acq_Start_Addr:** Start Address of first memory region

3.7.739 reg_inp_sys_acq_unit_reg_Acq_Mem_Region_Size_type (inp_sys_acq_unit_reg_Acq_Mem_Region_Size)—Offset 84004h

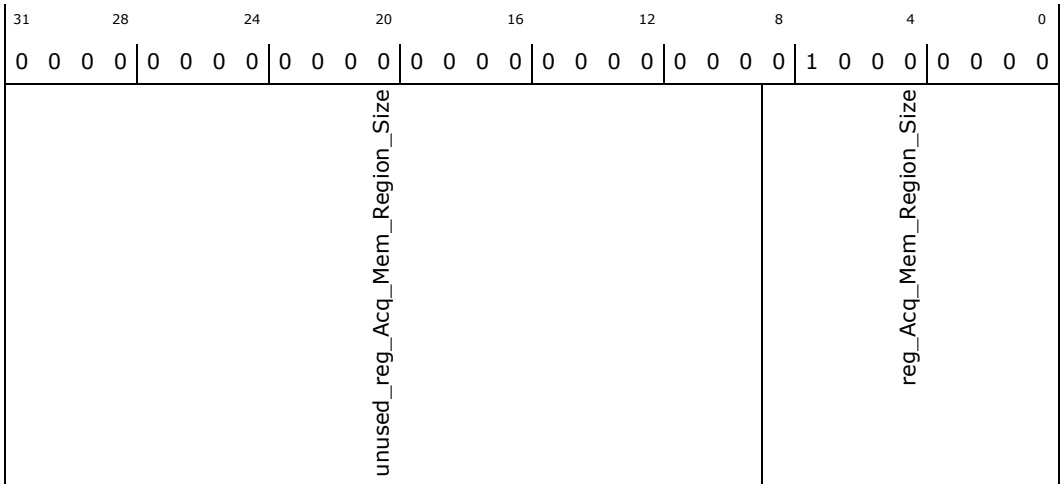
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Mem_Region_Size: [ISPMMADR] + 84004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Acq_Mem_Region_Size:** Unused
8:0	080h RW	**reg_Acq_Mem_Region_Size:** Memory region size

3.7.740 reg_inp_sys_acq_unit_reg_Acq_Num_Mem_Regions_type (inp_sys_acq_unit_reg_Acq_Num_Mem_Regions)—Offset 84008h

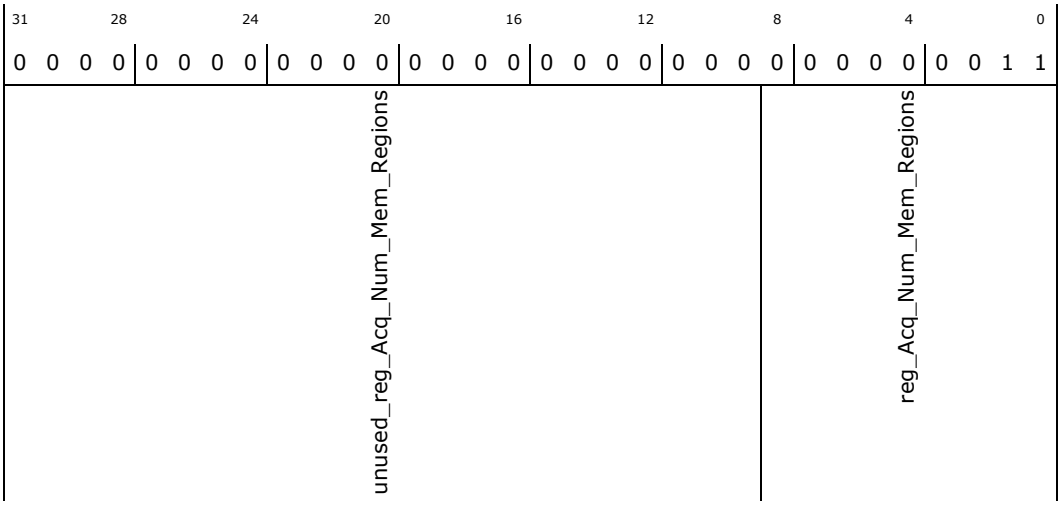
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Num_Mem_Regions: [ISPMMADR] + 84008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Acq_Num_Mem_Regions:** Unused
8:0	003h RW	**reg_Acq_Num_Mem_Regions:** Number of memory regions

3.7.741 reg_inp_sys_acq_unit_reg_Acq_Init_type (inp_sys_acq_unit_reg_Acq_Init)—Offset 8400Ch

Initialize Acquisition Unit

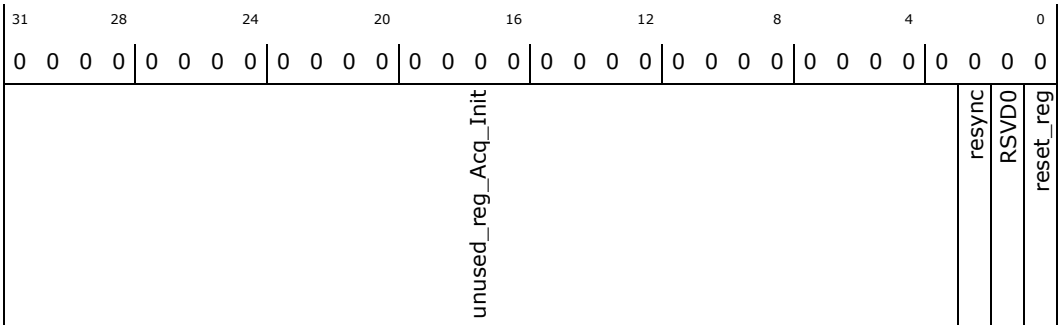
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Init: [ISPMMADR] + 8400Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_reg_Acq_Init:** Unused
2	0h WO	**resync:** Resynchronize the Acquisition Unit
1	0b RO	**RSVD0:** Reserved
0	0h WO	**reset_reg:** Reset Status Registers

3.7.742 reg_inp_sys_acq_unit_reg_Acq_Received_Short_Packets_type (inp_sys_acq_unit_reg_Acq_Received_Short_Packets)—Offset 84010h

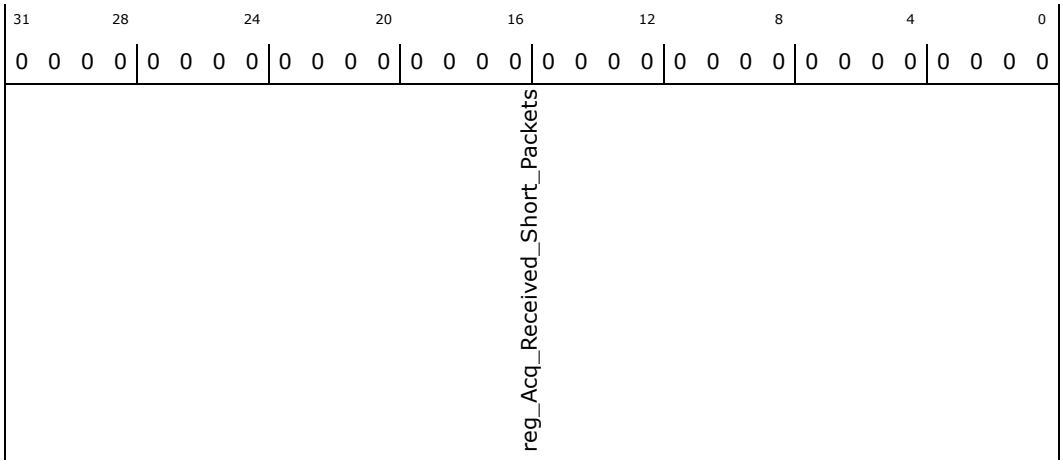
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Received_Short_Packets: [ISPMMADR] + 84010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Acq_Received_Short_Packets:** Number of received short packets

3.7.743 reg_inp_sys_acq_unit_reg_Acq_Received_Long_Packets_type (inp_sys_acq_unit_reg_Acq_Received_Long_Packets)—Offset 84014h

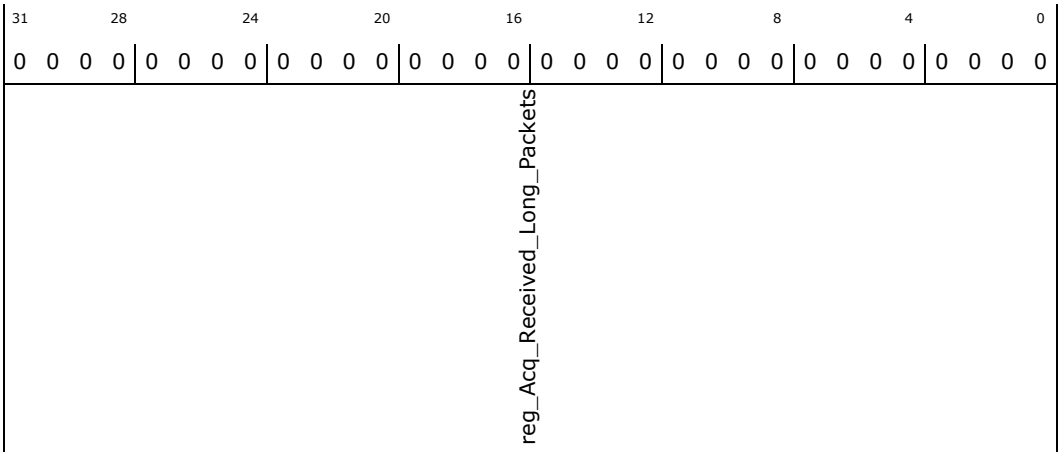
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Received_Long_Packets: [ISPMMADR] + 84014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**reg_Acq_Received_Long_Packets:** Number of received long packets

3.7.744 reg_inp_sys_acq_unit_reg_Acq_Last_Command_type (inp_sys_acq_unit_reg_Acq_Last_Command)—Offset 84018h

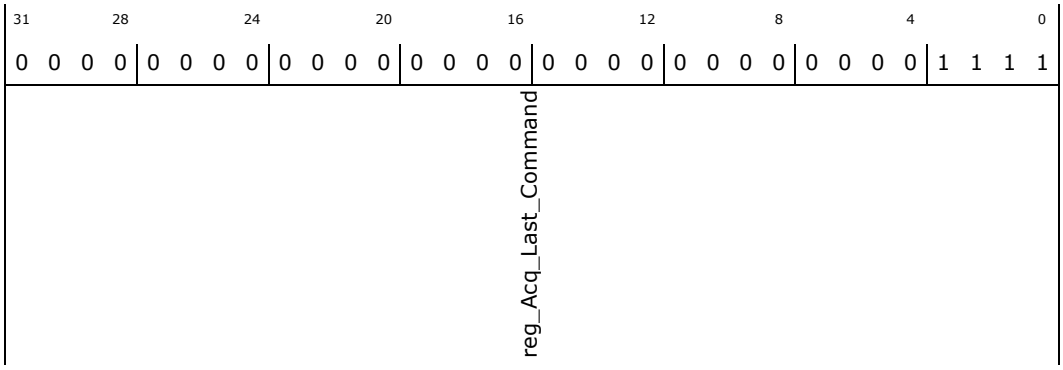
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Last_Command: [ISPMMADR] + 84018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Acq_Last_Command:** Last command token accepted

3.7.745 reg_inp_sys_acq_unit_reg_Acq_Next_Command_type (inp_sys_acq_unit_reg_Acq_Next_Command)—Offset 8401Ch

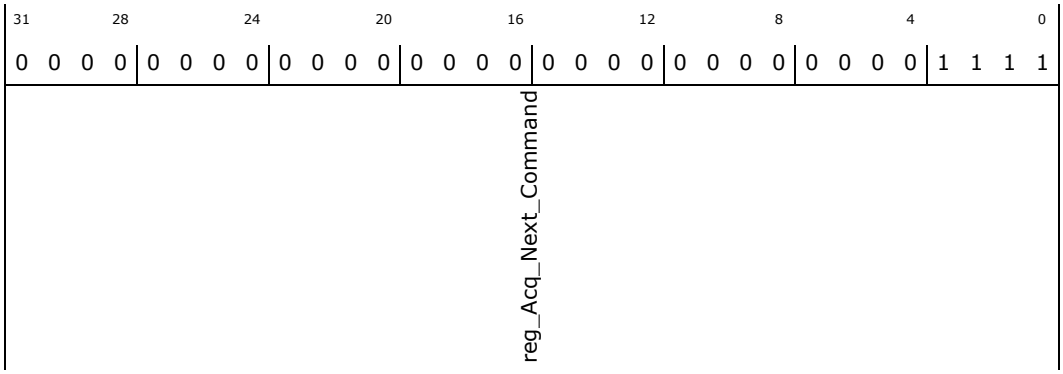
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Next_Command: [ISPMMADR] + 8401Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Acq_Next_Command:** Next command token to be accepted

3.7.746 reg_inp_sys_acq_unit_reg_Acq_Last_Acknowledge_type (inp_sys_acq_unit_reg_Acq_Last_Acknowledge)—Offset 84020h

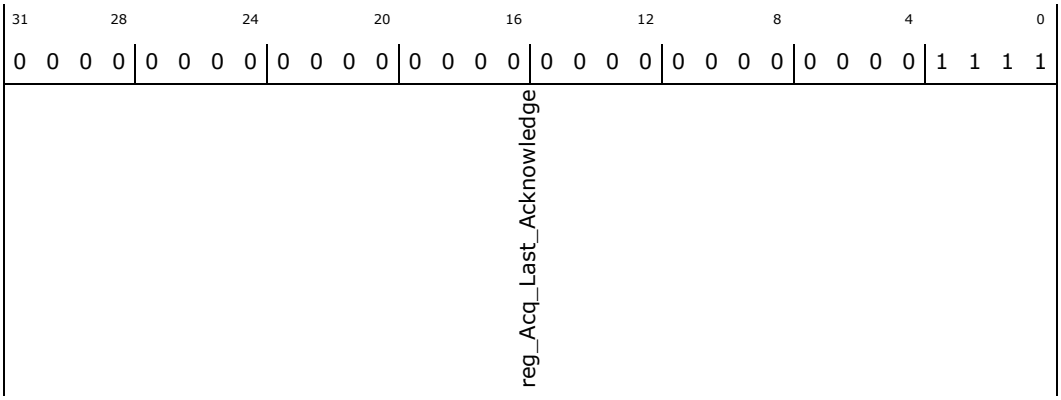
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Last_Acknowledge: [ISPMMADR] + 84020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Acq_Last_Acknowledge:** Last acknowledge token send

3.7.747 reg_inp_sys_acq_unit_reg_Acq_Next_Acknowledge_type (inp_sys_acq_unit_reg_Acq_Next_Acknowledge)—Offset 84024h

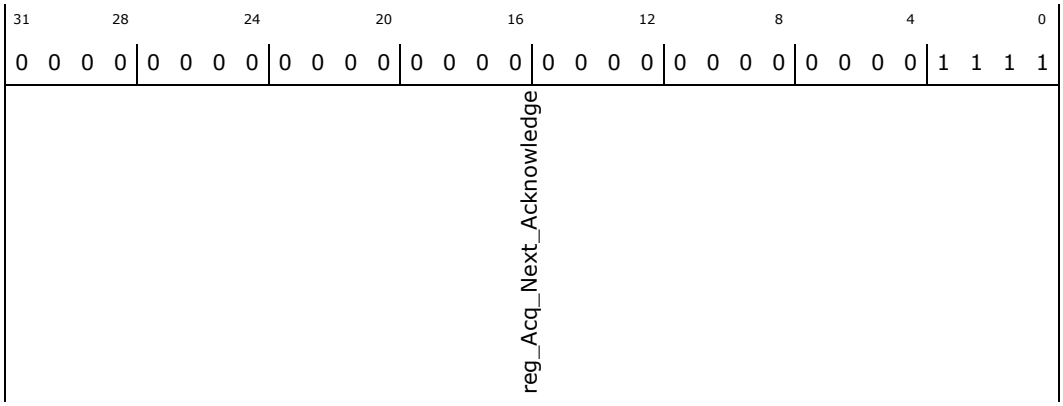
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Next_Acknowledge: [ISPMMADR] + 84024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Acq_Next_Acknowledge:** Next acknowledge token to be send

3.7.748 reg_inp_sys_acq_unit_reg_Acq_FSM_State_Info_type (inp_sys_acq_unit_reg_Acq_FSM_State_Info)—Offset 84028h

Acquisition unit State Machine information

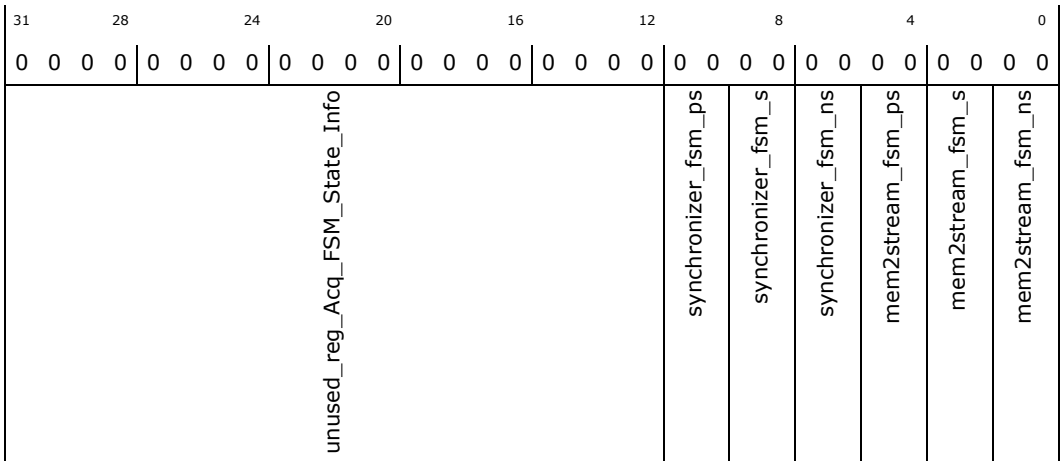
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_FSM_State_Info: [ISPMMADR] + 84028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_Acq_FSM_State_Info:** Unused
11:10	0h RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine
9:8	0h RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine
7:6	0h RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine
5:4	0h RO	**mem2stream_fsm_ps:** Previous state of Mem2Stream State Machine
3:2	0h RO	**mem2stream_fsm_s:** Current state of Mem2Stream State Machine
1:0	0h RO	**mem2stream_fsm_ns:** Next state of Mem2Stream State Machine

3.7.749 reg_inp_sys_acq_unit_reg_Acq_Int_Cntr_Info_type (inp_sys_acq_unit_reg_Acq_Int_Cntr_Info)—Offset 8402Ch

Acq_Int_Cntr_Info

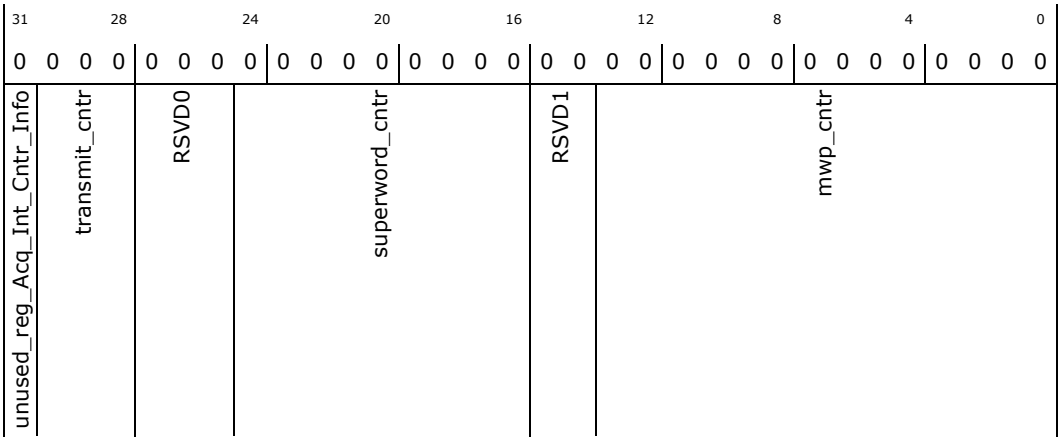
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Int_Cntr_Info: [ISPMMADR] + 8402Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**unused_reg_Acq_Int_Cntr_Info:** Unused
30:28	0h RO	**transmit_cntr:** Counter used for determining which word (part of a superword) to be send
27:25	0b RO	**RSVD0:** Reserved
24:16	0h RO	**superword_cntr:** Counts number of superwords read from wide bus (input buffer)
15:14	0b RO	**RSVD1:** Reserved
13:0	0h RO	**mwp_cntr:** Counts words in multi word packet

3.7.750 reg_inp_sys_dma_DMA_FSM_Command_type (inp_sys_dma_DMA_FSM_Command)—Offset 85000h

FSM Command: Last command and State

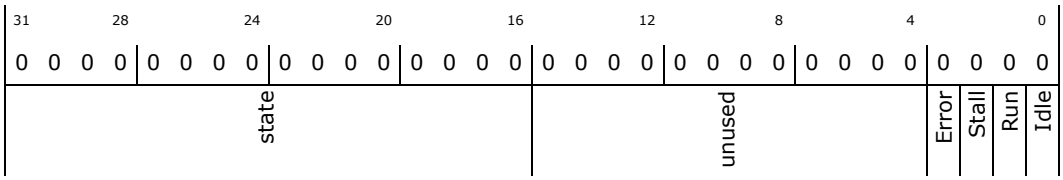
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Command: [ISPMMADR] + 85000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**state:** Lower 16 bits of the last command received and processed
15:4	0h RO	**unused:** unused
3	0h RO	**Error:** Error flag
2	0h RO	**Stall:** Stall flag
1	0h RO	**Run:** Run flag
0	0h RO	**Idle:** Idle flag

3.7.751 reg_inp_sys_dma_DMA_CH0_Packing_setup_type (inp_sys_dma_DMA_CH0_Packing_setup)—Offset 86000h

DMA CH 0 PARAM 0: Packing setup

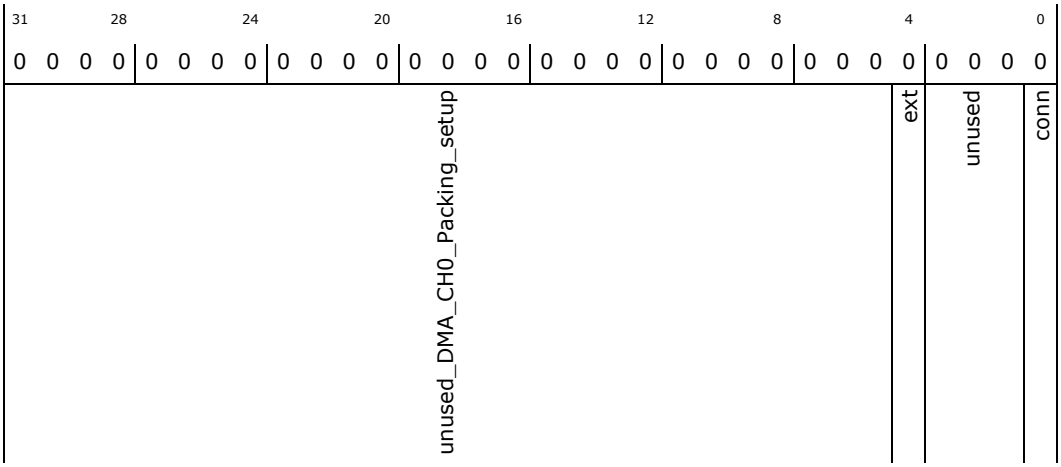
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_Packing_setup: [ISPMMADR] + 86000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH0_Packing_setup:** Unused
4	0h RO	**ext:** Zero(0)/Sign(1) extension
3:1	0h RO	**unused:** unused
0	0h RO	**conn:** Connection ID

3.7.752 reg_inp_sys_dma_DMA_CH0_dev_stride_A_type (inp_sys_dma_DMA_CH0_dev_stride_A)—Offset 86100h

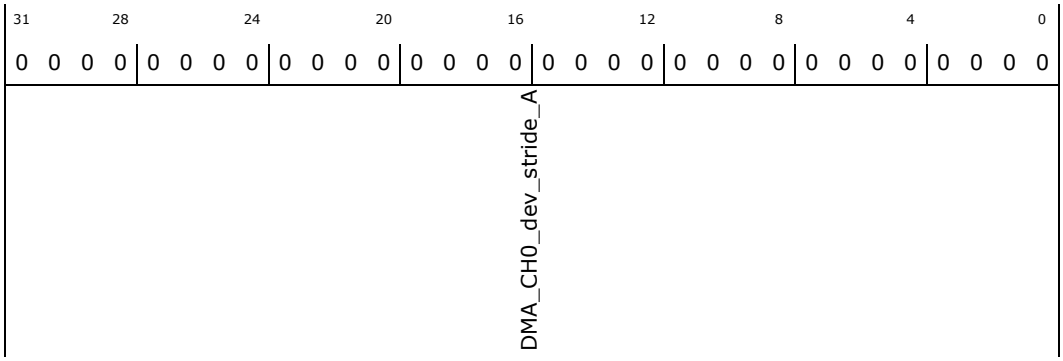
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_dev_stride_A: [ISPMMADR] + 86100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH0_dev_stride_A:** DMA CH 0 PARAM 1: Device A stride

3.7.753 reg_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A_type (inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A)—Offset 86200h

DMA CH 0 PARAM 2: Device A Packing LSE cropping/Elements

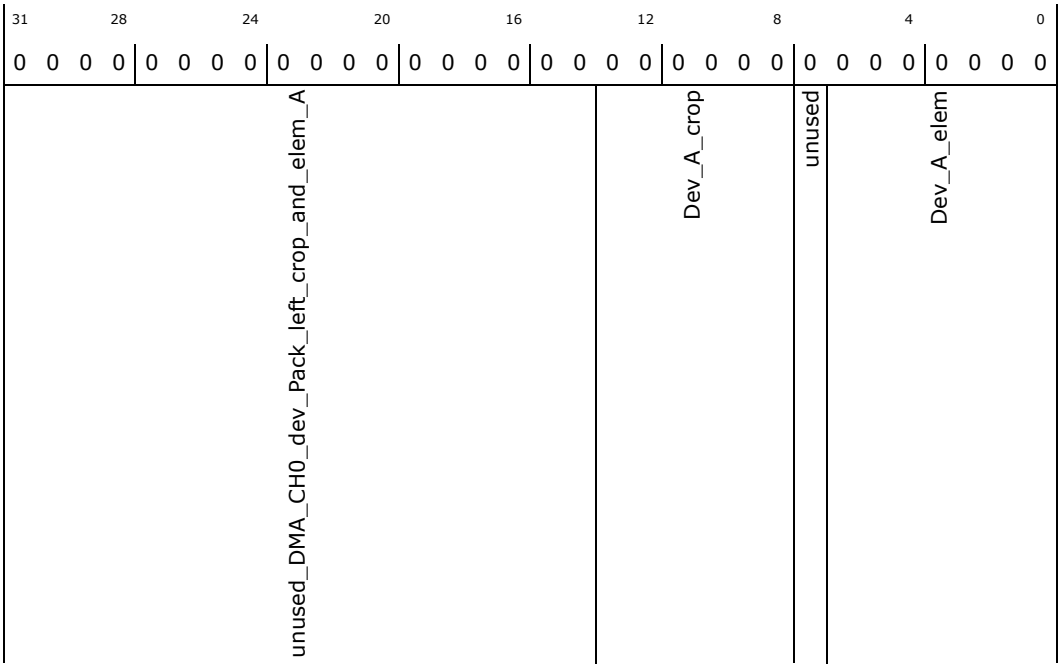
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A : [ISPMMADR] + 86200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH0_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0h RO	**unused:** unused
6:0	0h RO	**Dev_A_elem:** Device A element per word

3.7.754 reg_inp_sys_dma_DMA_CH0_Device_Xb_A_type (inp_sys_dma_DMA_CH0_Device_Xb_A)—Offset 86300h

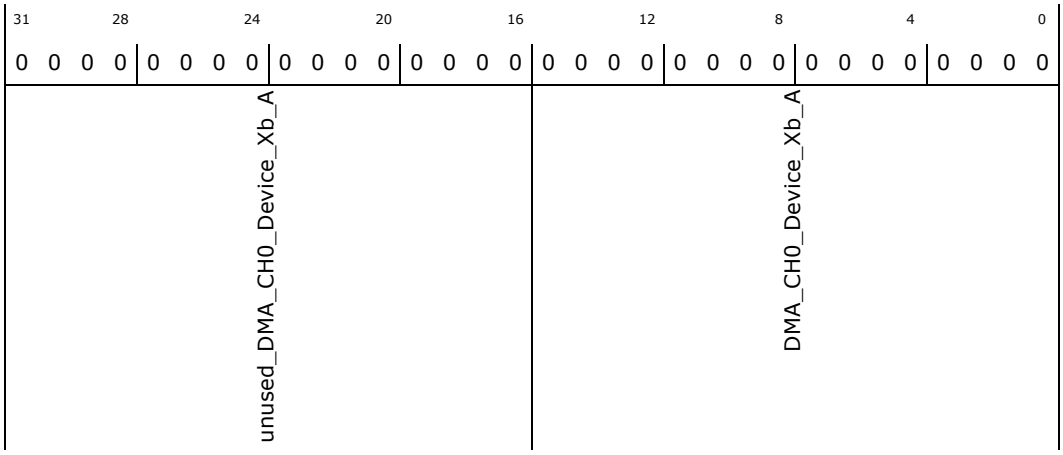
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_Device_Xb_A: [ISPMMADR] + 86300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH0_Device_Xb_A:** DMA CH 0 PARAM 3: Device A block width (Xb)

3.7.755 reg_inp_sys_dma_DMA_CH0_dev_stride_B_type (inp_sys_dma_DMA_CH0_dev_stride_B)—Offset 86400h

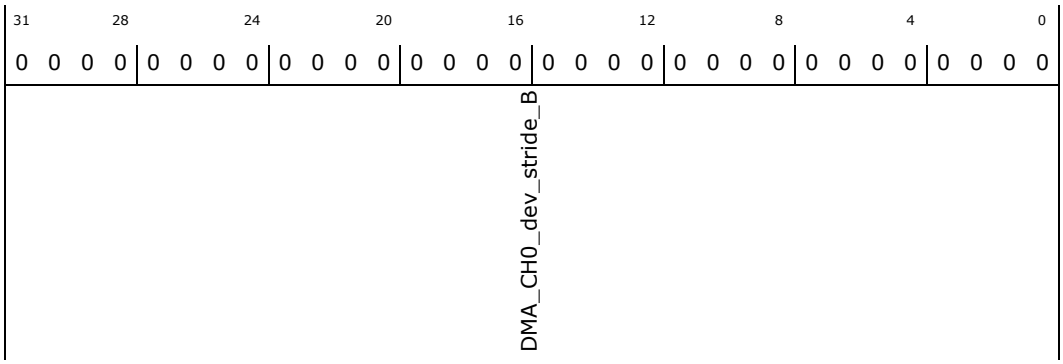
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_dev_stride_B: [ISPMMADR] + 86400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH0_dev_stride_B:** DMA CH 0 PARAM 4: Device B stride

3.7.756 reg_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B_type (inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B)—Offset 86500h

DMA CH 0 PARAM 5: Device B Packing LSE cropping/Elements

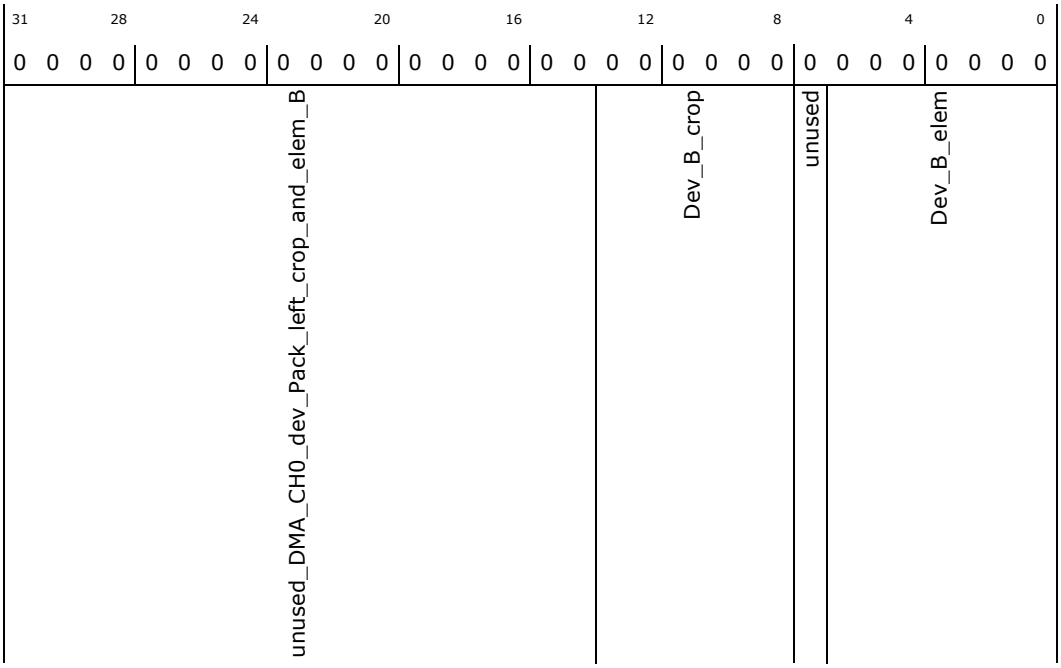
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B : [ISPMMADR] + 86500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH0_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0h RO	**unused:** unused
6:0	0h RO	**Dev_B_elem:** Device B element per word

3.7.757 reg_inp_sys_dma_DMA_CH0_Device_Xb_B_type (inp_sys_dma_DMA_CH0_Device_Xb_B)—Offset 86600h

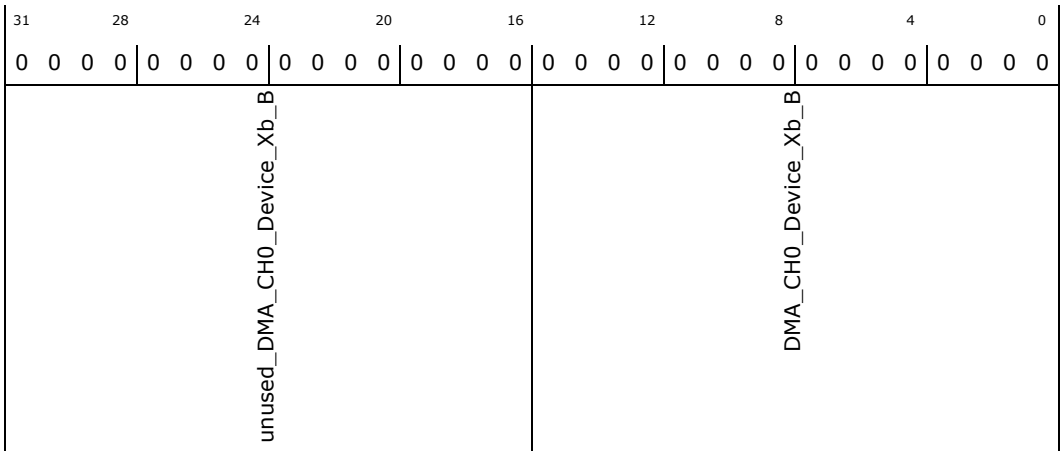
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_Device_Xb_B: [ISPMMADR] + 86600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH0_Device_Xb_B:** DMA CH 0 PARAM 6: Device B block width (Xb)

3.7.758 reg_inp_sys_dma_DMA_CH0_Yb_type (inp_sys_dma_DMA_CH0_Yb)—Offset 86700h

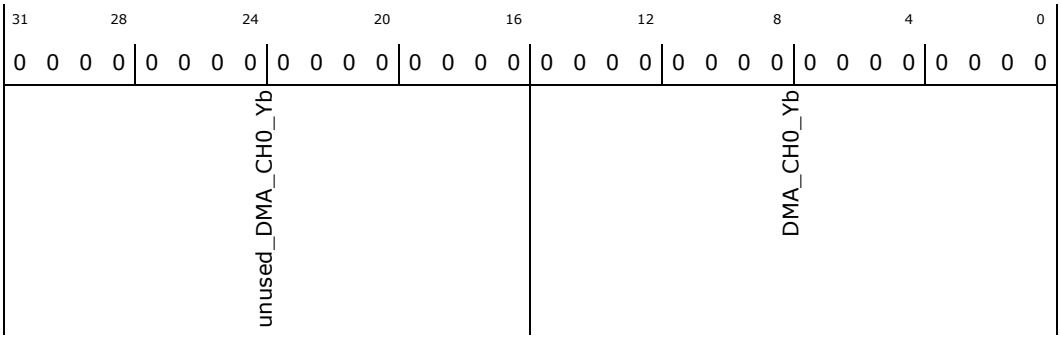
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_Yb: [ISPMMADR] + 86700h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Yb:** Unused
15:0	0h RO	**DMA_CH0_Yb:** DMA CH 0 PARAM 7: block Height (Yb)

3.7.759 reg_inp_sys_dma_DMA_CH0_pending_command_type (inp_sys_dma_DMA_CH0_pending_command)—Offset 86800h

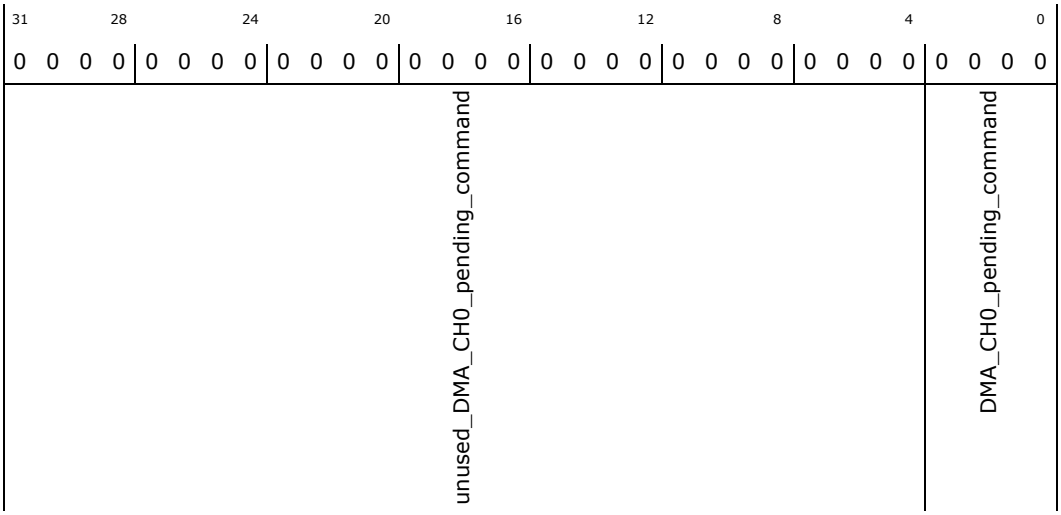
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_pending_command: [ISPMMADR] + 86800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH0_pending_command:** Unused
3:0	0h RO	**DMA_CH0_pending_command:** DMA CH 0 PARAM 8: Pending commands which will use channel 0

3.7.760 reg_inp_sys_dma_DMA_command_token_type (inp_sys_dma_DMA_command_token)—Offset 87000h

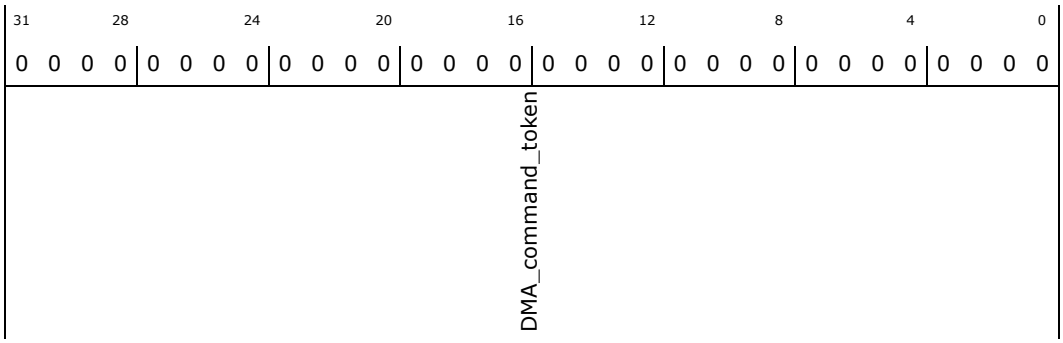
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_command_token: [ISPMMADR] + 87000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_token:** Pending or last executed command token

3.7.761 reg_inp_sys_dma_DMA_command_src_addr_type (inp_sys_dma_DMA_command_src_addr)—Offset 87004h

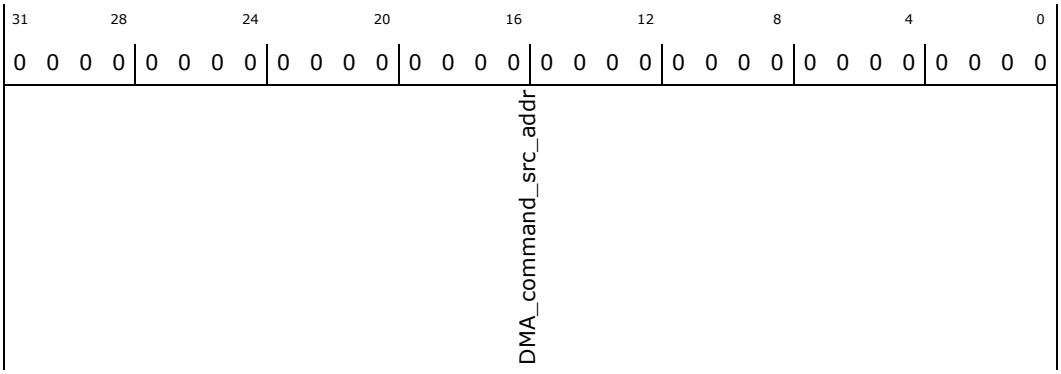
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_command_src_addr: [ISPMMADR] + 87004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_src_addr:** Source address of the pending or last executed command token

3.7.762 reg_inp_sys_dma_DMA_command_dst_addr_type (inp_sys_dma_DMA_command_dst_addr)—Offset 87008h

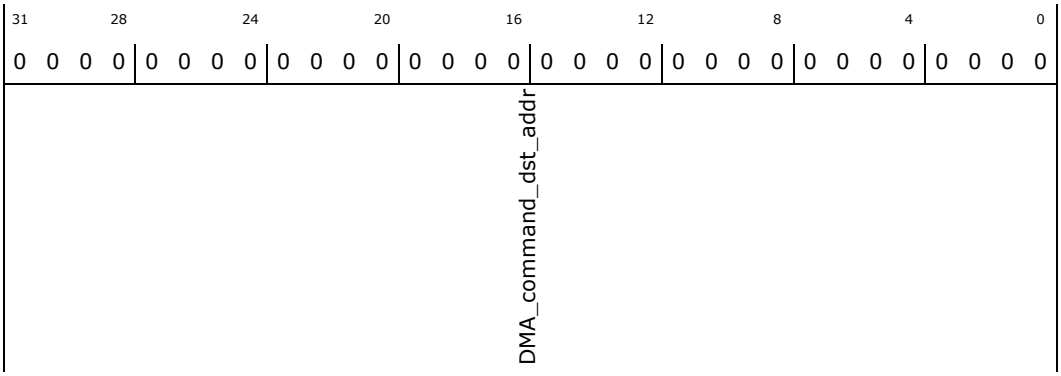
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_command_dst_addr: [ISPMMADR] + 87008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_dst_addr:** Destination address of the pending or last executed command token

3.7.763 reg_inp_sys_dma_DMA_command_ctrl_id_type (inp_sys_dma_DMA_command_ctrl_id)—Offset 8700Ch

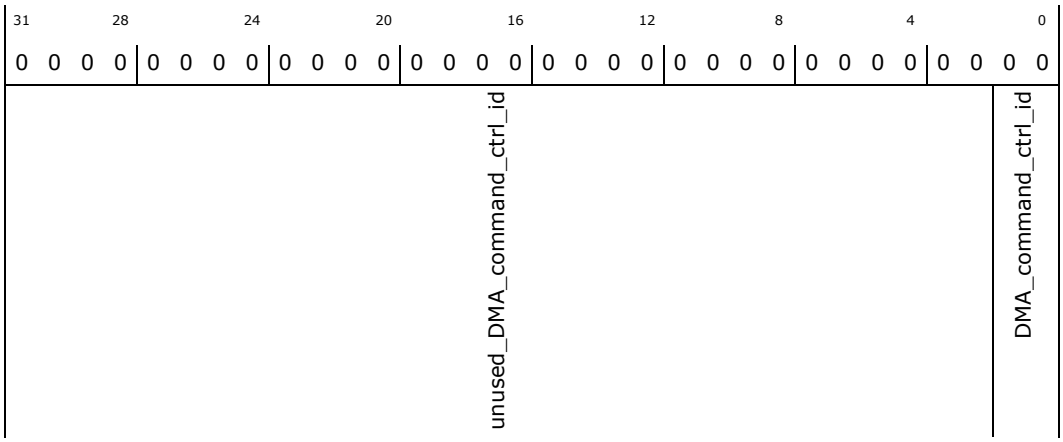
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_command_ctrl_id: [ISPMMADR] + 8700Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_command_ctrl_id:** Unused
1:0	0h RO	**DMA_command_ctrl_id:** Controller id of the pending or last executed command token

3.7.764 reg_inp_sys_dma_DMA_FSM_Ctrl_status_type (inp_sys_dma_DMA_FSM_Ctrl_status)—Offset 87010h

DMA FSM Control state and flags

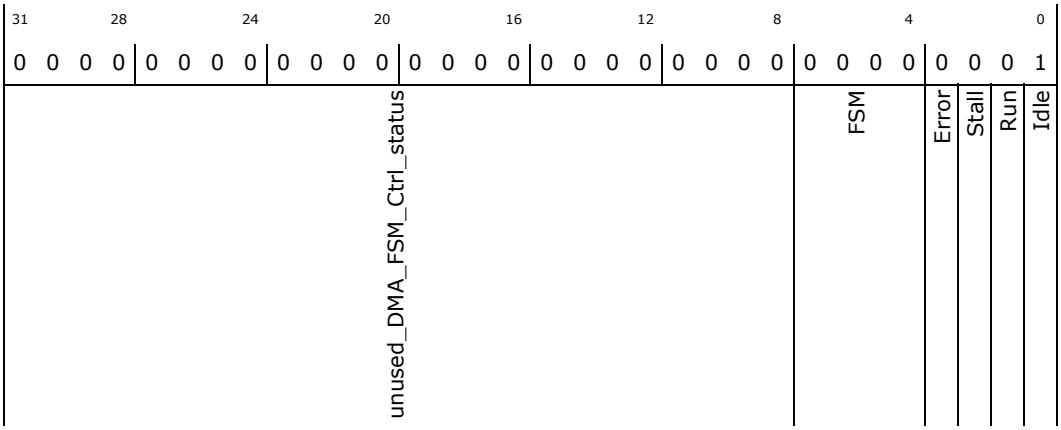
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_status: [ISPMMADR] + 87010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:8	0h RW	**unused_DMA_FSM_Ctrl_status:** Unused
7:4	0h RO	**FSM:** FSM control state: 0)Idle -- 1)req_rcv -- 2)rcv -- 3)rcv_req -- 4)init
3	0h RO	**Error:** Error flag
2	0h RO	**Stall:** Stall flag
1	0h RO	**Run:** Run flag
0	1h RO	**Idle:** Idle flag

3.7.765 reg_inp_sys_dma_DMA_FSM_Pack_status_type (inp_sys_dma_DMA_FSM_Pack_status)—Offset 87014h

DMA FSM Pack state

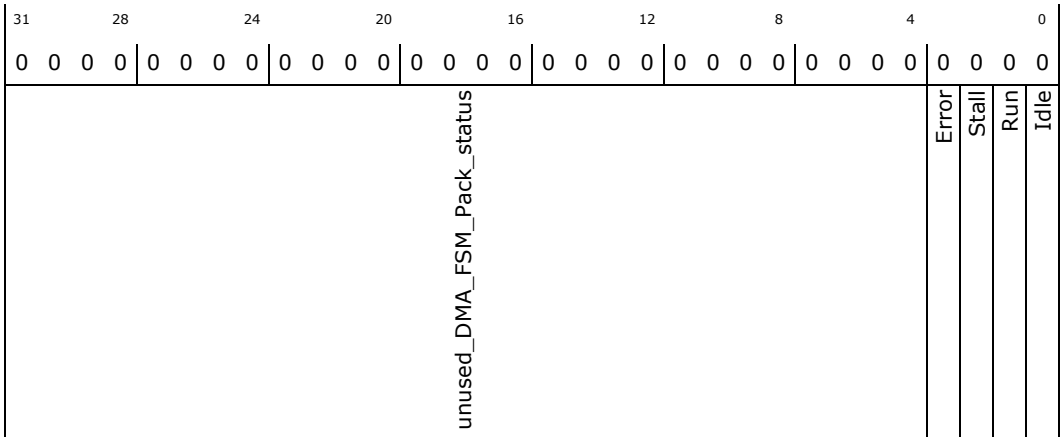
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Pack_status: [ISPMMADR] + 87014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_FSM_Pack_status:** Unused
3	0h RO	**Error:** Error flag
2	0h RO	**Stall:** Stall flag
1	0h RO	**Run:** Run flag
0	0h RO	**Idle:** Idle flag

3.7.766 reg_inp_sys_dma_DMA_FSM_request_status_type (inp_sys_dma_DMA_FSM_request_status)—Offset 87018h

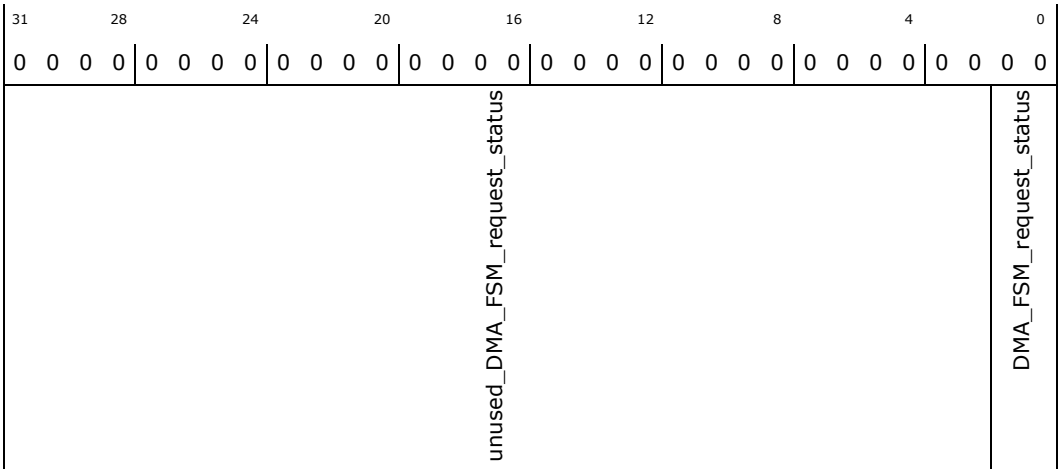
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_request_status: [ISPMMADR] + 87018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_request_status:** Unused
1:0	0h RO	**DMA_FSM_request_status:** DMA FSM Request state: 0)Idle -- 1)req -- 2)Next line

3.7.767 reg_inp_sys_dma_DMA_FSM_write_status_type (inp_sys_dma_DMA_FSM_write_status)—Offset 8701Ch

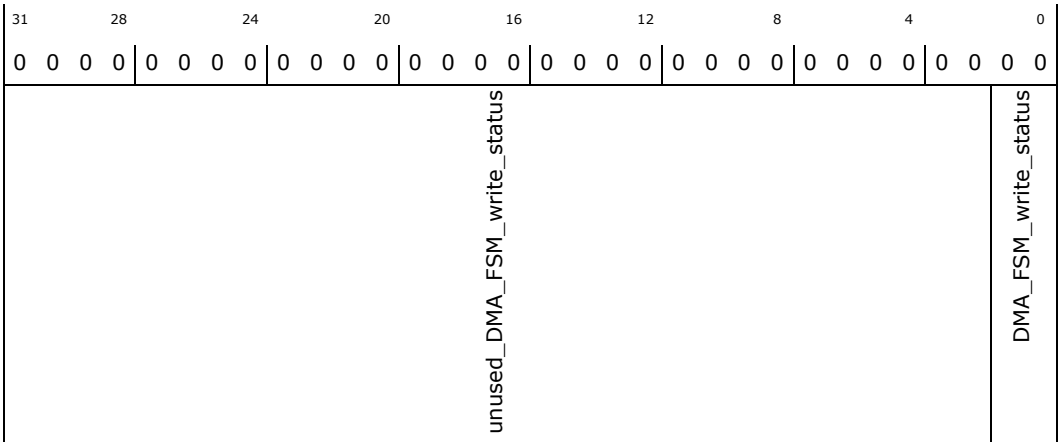
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_write_status: [ISPMMADR] + 8701Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_write_status:** Unused
1:0	0h RO	**DMA_FSM_write_status:** DMA FSM Write state: 0)Idle -- 1)req -- 2)Next line

3.7.768 reg_inp_sys_dma_DMA_FSM_Ctrl_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_dev_idx)—Offset 87110h

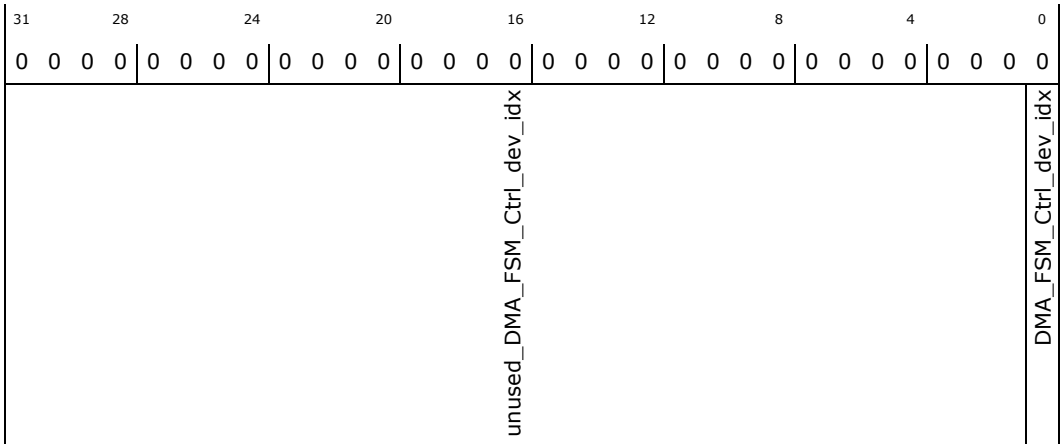
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_dev_idx: [ISPMMADR] + 87110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_DMA_FSM_Ctrl_dev_idx:** Unused
0	0h RO	**DMA_FSM_Ctrl_dev_idx:** DMA FSM Control request device idx

3.7.769 reg_inp_sys_dma_DMA_FSM_Pack_cnt_Yb_type (inp_sys_dma_DMA_FSM_Pack_cnt_Yb)—Offset 87114h

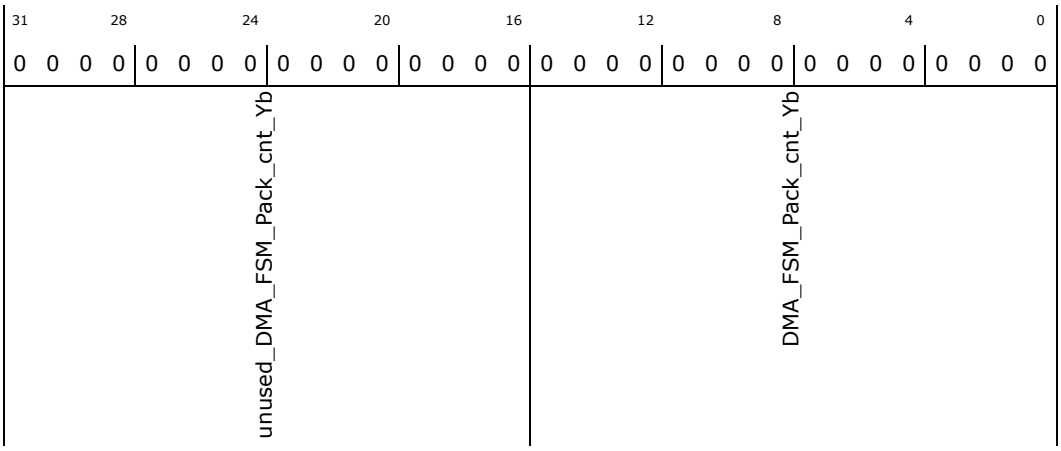
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Pack_cnt_Yb: [ISPMMADR] + 87114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_cnt_Yb:** Unused
15:0	0h RO	**DMA_FSM_Pack_cnt_Yb:** DMA FSM pack counter height (Yb)

3.7.770 reg_inp_sys_dma_DMA_FSM_Request_cnt_Yb_type (inp_sys_dma_DMA_FSM_Request_cnt_Yb)—Offset 87118h

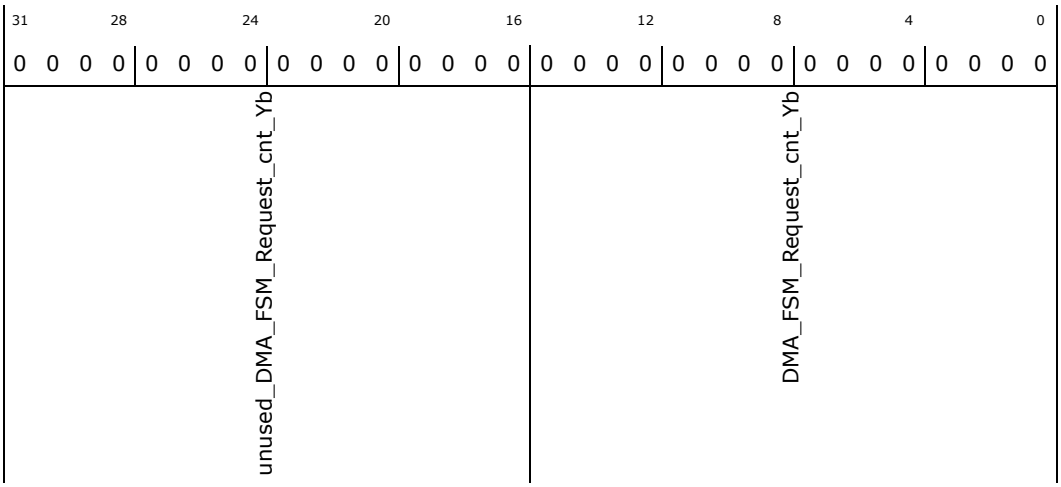
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Request_cnt_Yb: [ISPMMADR] + 87118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Request_cnt_Yb:** Unused
15:0	0h RO	**DMA_FSM_Request_cnt_Yb:** DMA FSM request counter height (Yb)

3.7.771 reg_inp_sys_dma_DMA_FSM_Write_cnt_Y_type (inp_sys_dma_DMA_FSM_Write_cnt_Y)—Offset 8711Ch

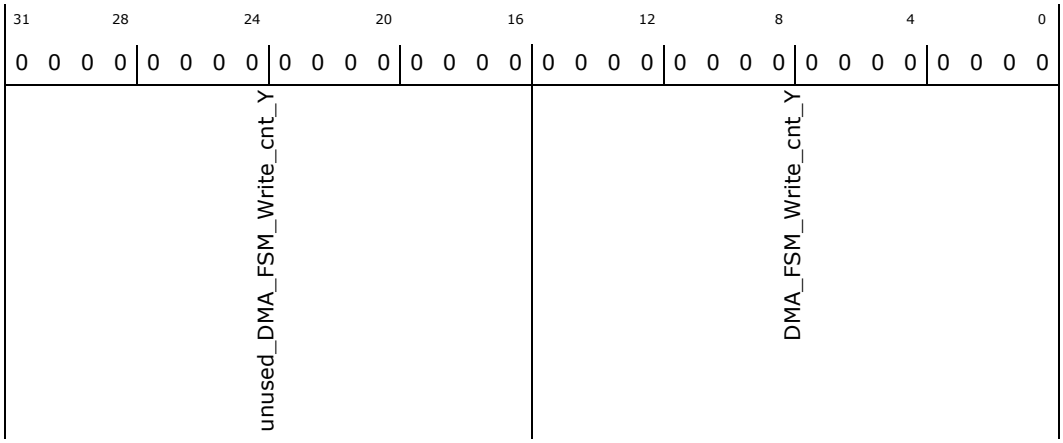
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Write_cnt_Y: [ISPMMADR] + 8711Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Write_cnt_Y:** Unused
15:0	0h RO	**DMA_FSM_Write_cnt_Y:** DMA FSM Write counter height (Yb)

3.7.772 reg_inp_sys_dma_DMA_FSM_Ctrl_req_addr_type (inp_sys_dma_DMA_FSM_Ctrl_req_addr)—Offset 87210h

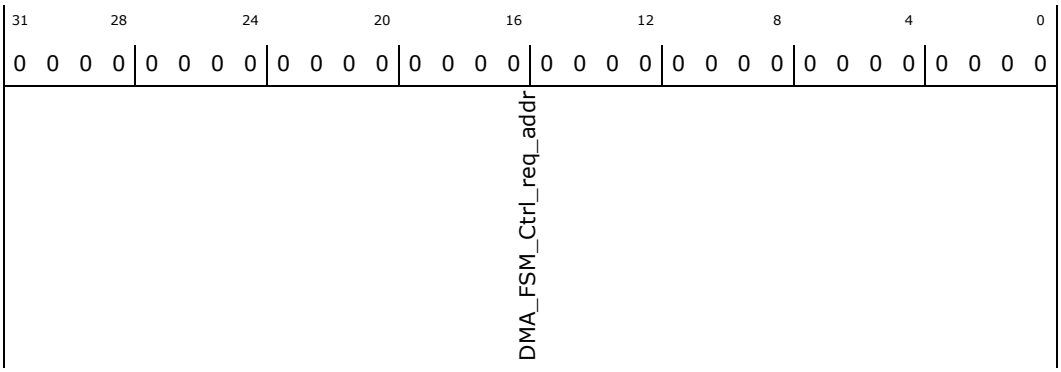
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_req_addr: [ISPMMADR] + 87210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_req_addr:** DMA FSM Control request address

3.7.773 reg_inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb_type (inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb)—Offset 87214h

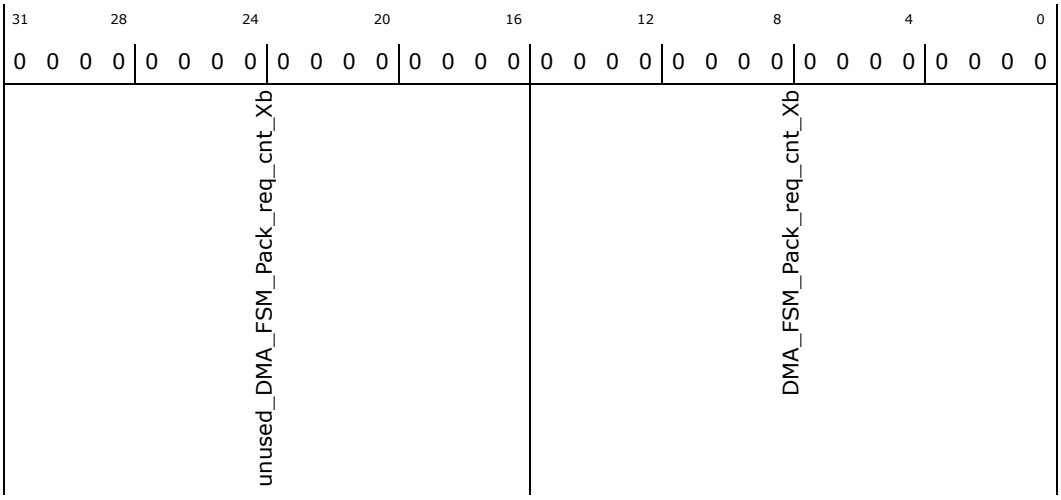
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb: [ISPMMADR] + 87214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_req_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Pack_req_cnt_Xb:** DMA FSM pack request counter width (Xb)

3.7.774 reg_inp_sys_dma_DMA_FSM_Request_cnt_Xb_type (inp_sys_dma_DMA_FSM_Request_cnt_Xb)—Offset 87218h

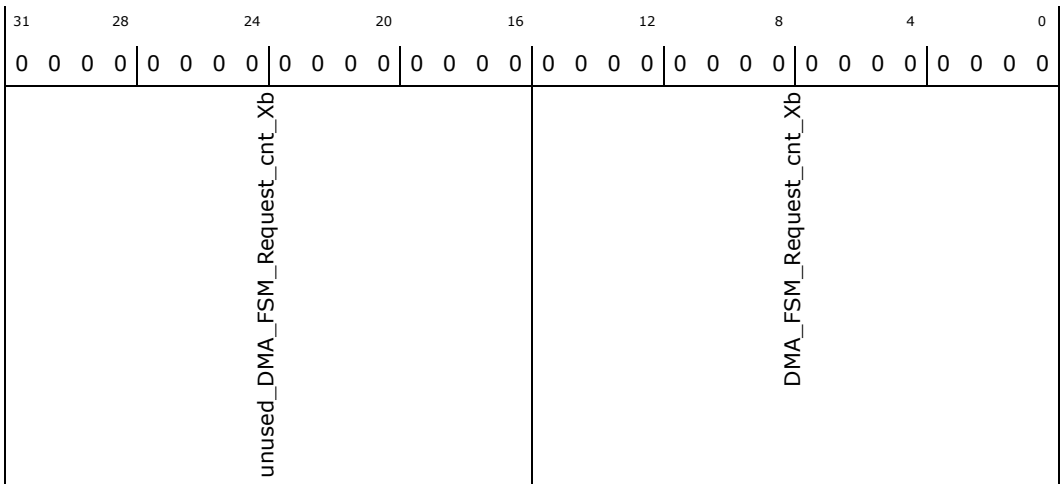
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Request_cnt_Xb: [ISPMMADR] + 87218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Request_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Request_cnt_Xb:** DMA FSM Request counter width (Xb)

3.7.775 reg_inp_sys_dma_DMA_FSM_Write_cnt_Xb_type (inp_sys_dma_DMA_FSM_Write_cnt_Xb)—Offset 8721Ch

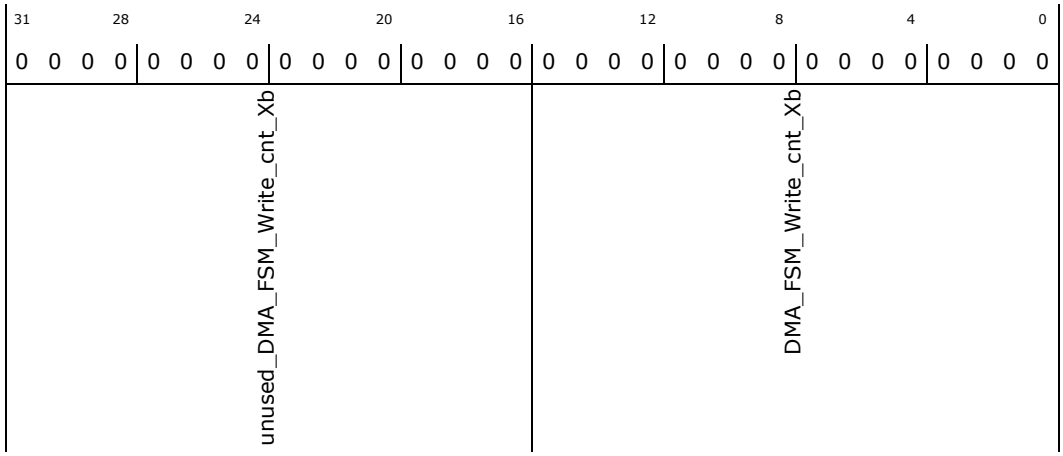
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Write_cnt_Xb: [ISPMMADR] + 8721Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Write_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Write_cnt_Xb:** DMA FSM Write counter width (Xb)

3.7.776 reg_inp_sys_dma_DMA_FSM_Ctrl_req_stride_type (inp_sys_dma_DMA_FSM_Ctrl_req_stride)—Offset 87310h

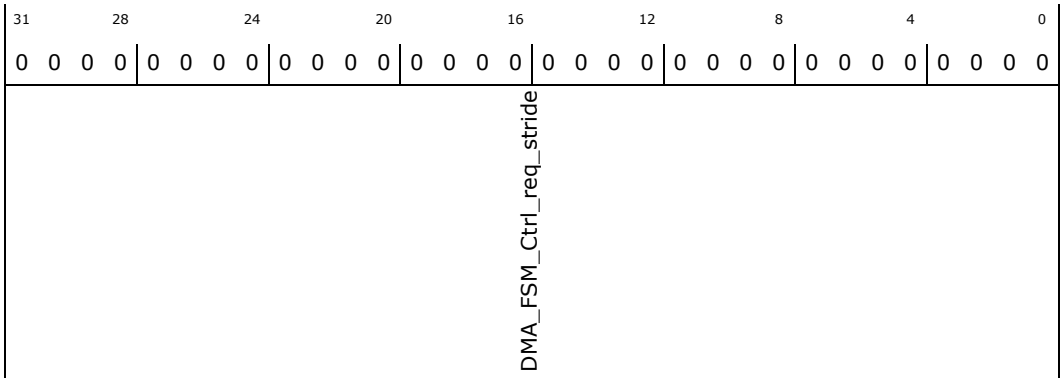
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_req_stride: [ISPMMADR] + 87310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_req_stride:** DMA FSM Control request stride

3.7.777 reg_inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb_type (inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb)—Offset 87314h

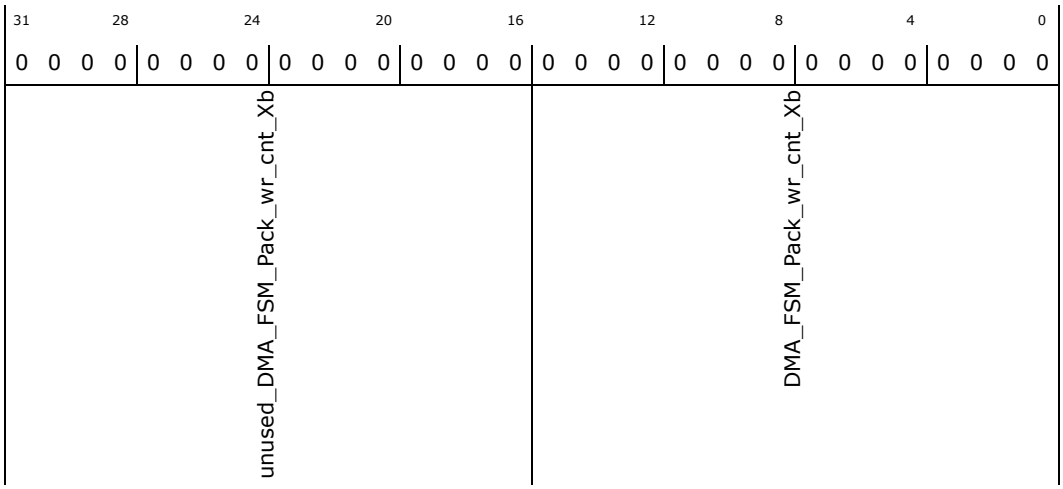
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb: [ISPMMADR] + 87314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_wr_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Pack_wr_cnt_Xb:** DMA FSM pack write counter width (Xb)

3.7.778 reg_inp_sys_dma_DMA_FSM_Req_remining_Xb_type (inp_sys_dma_DMA_FSM_Req_remining_Xb)—Offset 87318h

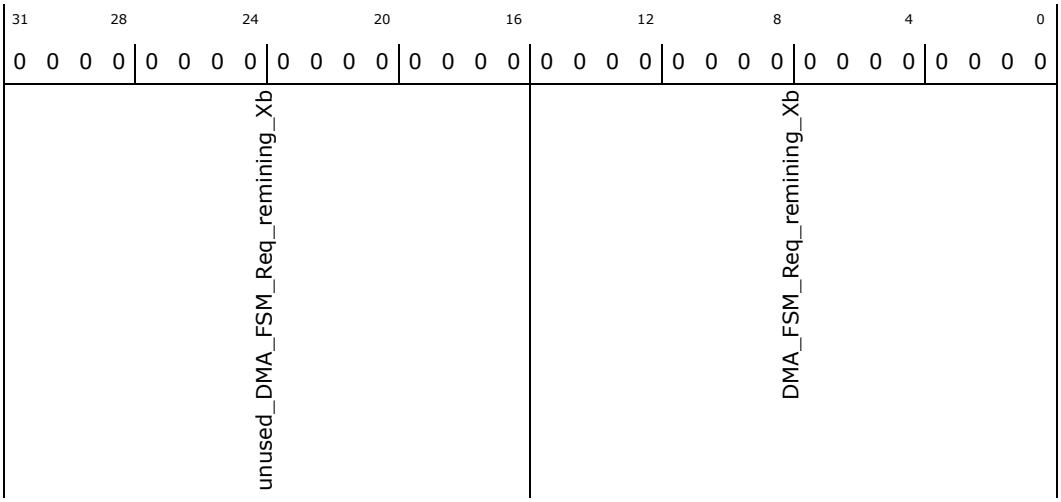
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Req_remining_Xb: [ISPMMADR] + 87318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Req_remining_Xb:** Unused
15:0	0h RO	**DMA_FSM_Req_remining_Xb:** DMA FSM Request counter remaining word width

3.7.779 reg_inp_sys_dma_DMA_FSM_Wr_remining_Xb_type (inp_sys_dma_DMA_FSM_Wr_remining_Xb)—Offset 8731Ch

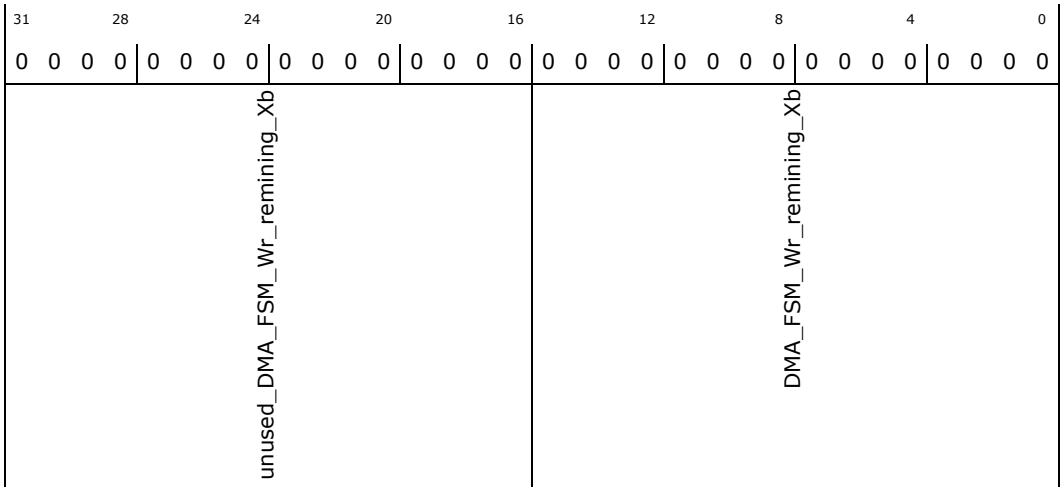
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Wr_remining_Xb: [ISPMMADR] + 8731Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Wr_remining_Xb:** Unused
15:0	0h RO	**DMA_FSM_Wr_remining_Xb:** DMA FSM Write counter remaining word width

3.7.780 reg_inp_sys_dma_DMA_FSM_Ctrl_req_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_req_Xb)—Offset 87410h

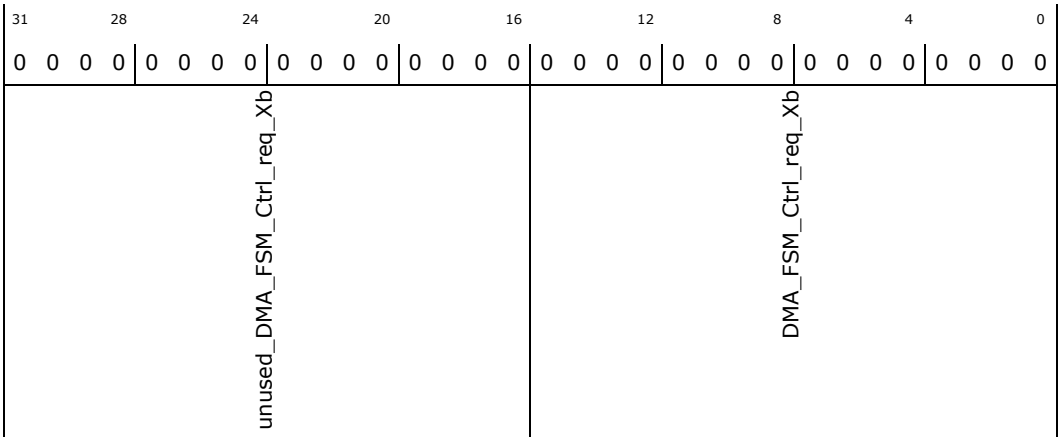
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_req_Xb: [ISPMMADR] + 87410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_req_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_req_Xb:** DMA FSM Control request width (Xb)

3.7.781 reg_inp_sys_dma_DMA_FSM_Req_burst_cnt_type (inp_sys_dma_DMA_FSM_Req_burst_cnt)—Offset 87418h

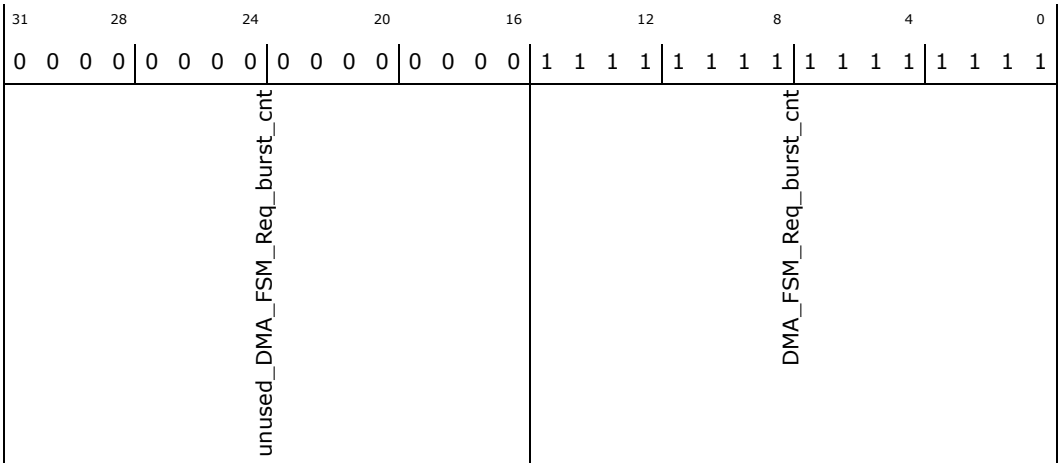
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Req_burst_cnt: [ISPMMADR] + 87418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Req_burst_cnt:** Unused
15:0	FFFFh RO	**DMA_FSM_Req_burst_cnt:** DMA FSM Request word burst counter

3.7.782 reg_inp_sys_dma_DMA_FSM_Wr_burst_cnt_type (inp_sys_dma_DMA_FSM_Wr_burst_cnt)—Offset 8741Ch

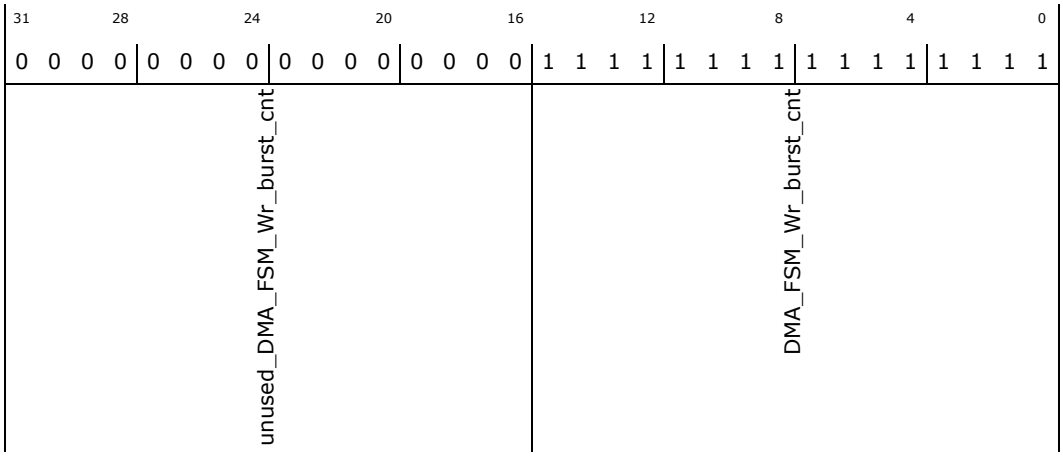
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Wr_burst_cnt: [ISPMMADR] + 8741Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Wr_burst_cnt:** Unused
15:0	FFFFh RO	**DMA_FSM_Wr_burst_cnt:** DMA FSM Write word burst counter

3.7.783 reg_inp_sys_dma_DMA_FSM_Ctrl_req_Yb_type (inp_sys_dma_DMA_FSM_Ctrl_req_Yb)—Offset 87510h

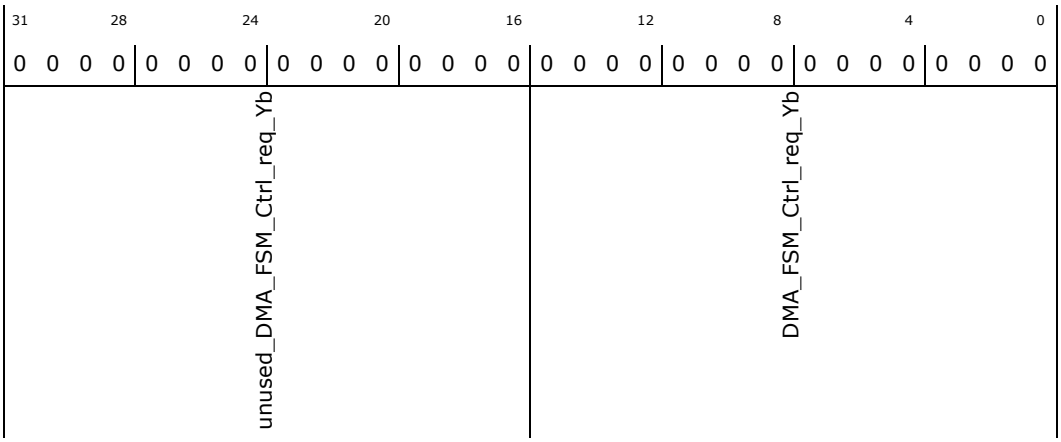
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_req_Yb: [ISPMMADR] + 87510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_req_Yb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_req_Yb:** DMA FSM Control request height (Yb)

3.7.784 reg_inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx)—Offset 87610h

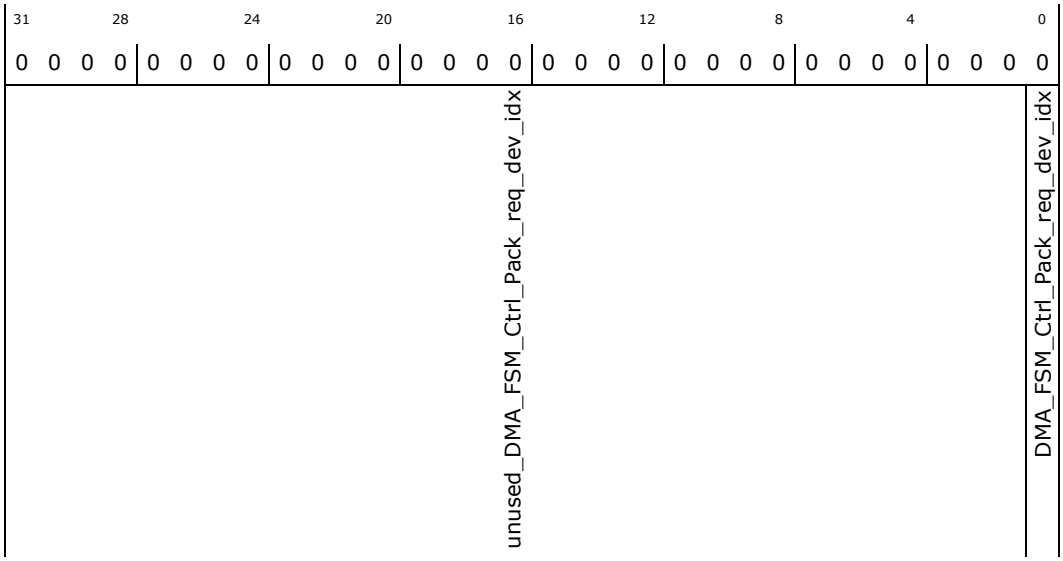
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx: [ISPMMADR] + 87610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_DMA_FSM_Ctrl_Pack_req_dev_idx:** Unused
0	0h RO	**DMA_FSM_Ctrl_Pack_req_dev_idx:** DMA FSM Control pack request device idx

3.7.785 reg_inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx)—Offset 87710h

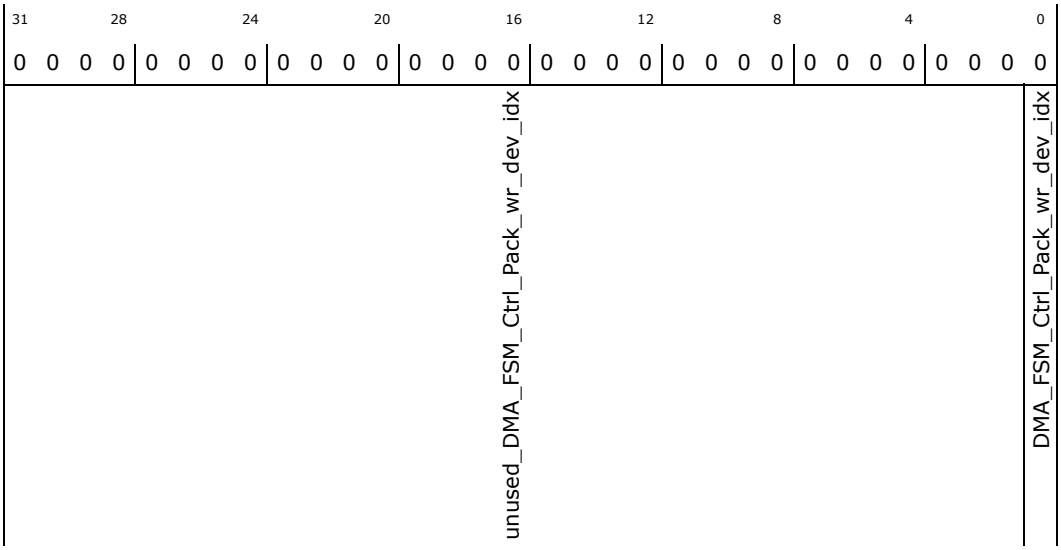
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx: [ISPMMADR] + 87710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_DMA_FSM_Ctrl_Pack_wr_dev_idx:** Unused
0	0h RO	**DMA_FSM_Ctrl_Pack_wr_dev_idx:** DMA FSM Control pack write device idx

3.7.786 reg_inp_sys_dma_DMA_FSM_Ctrl_Wr_addr_type (inp_sys_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 87810h

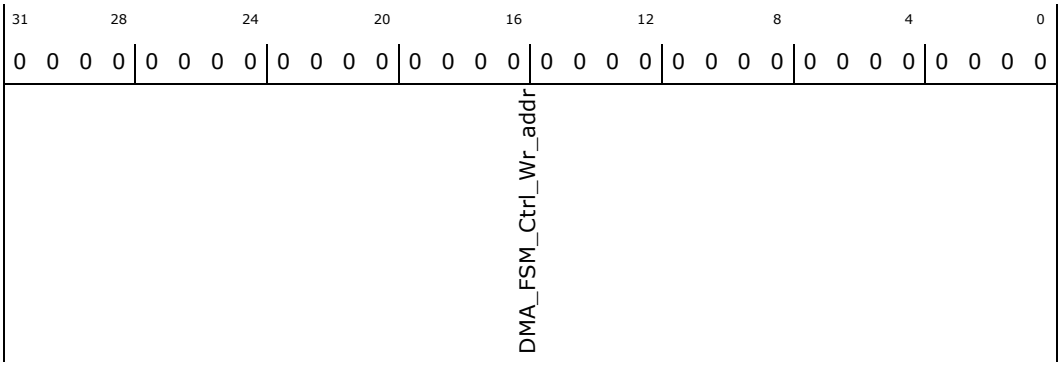
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_Wr_addr: [ISPMMADR] + 87810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_Wr_addr:** DMA FSM Control write address

3.7.787 reg_inp_sys_dma_DMA_FSM_Ctrl_Wr_stride_type (inp_sys_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 87910h

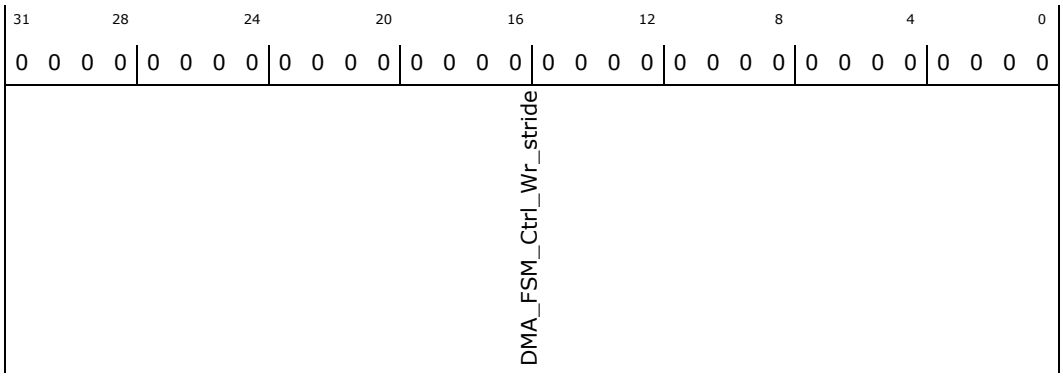
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_Wr_stride: [ISPMMADR] + 87910h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_Wr_stride:** DMA FSM Control write stride

3.7.788 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb)—Offset 87A10h

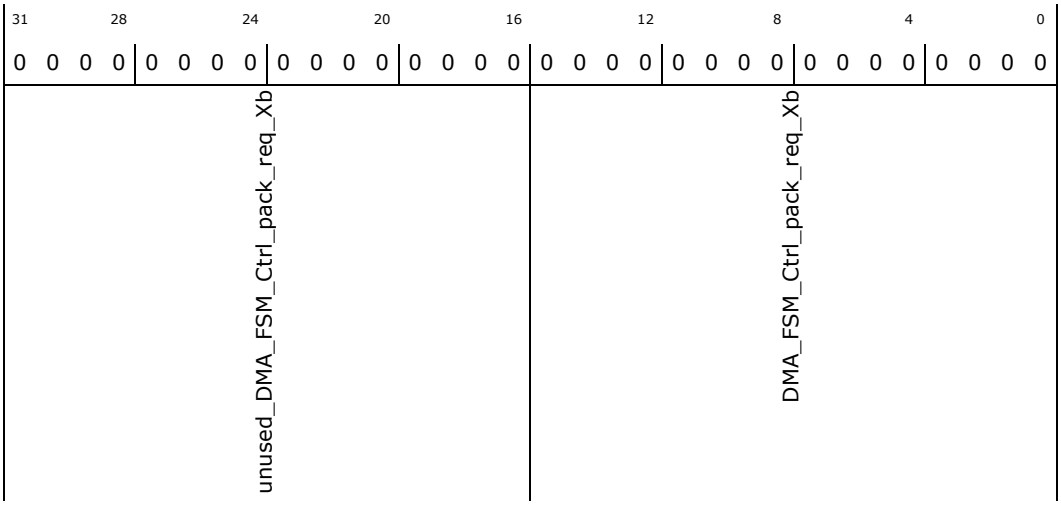
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb: [ISPMMADR] + 87A10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_req_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_req_Xb:** DMA FSM Control FSM Pack request width (Xb)

3.7.789 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_Yb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_Yb)—Offset 87B10h

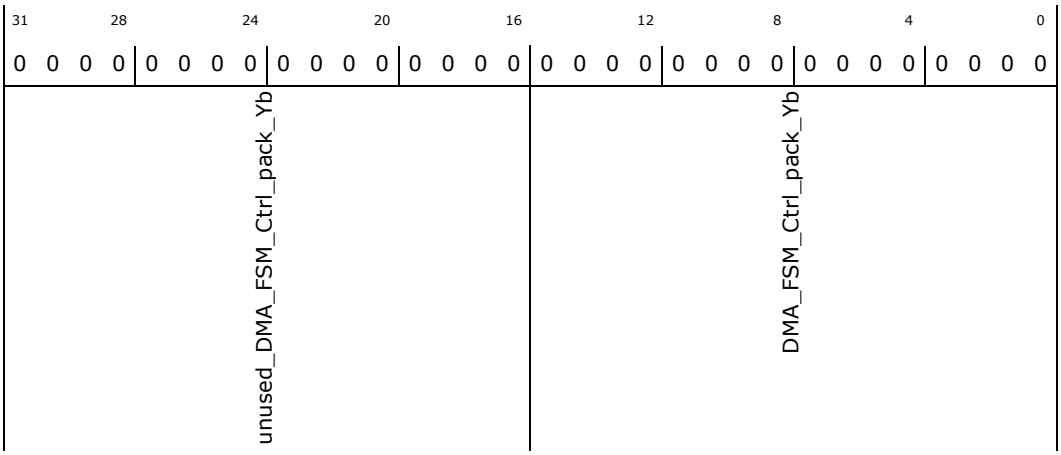
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_Yb: [ISPMMADR] + 87B10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_Yb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_Yb:** DMA FSM Control FSM Pack height (Yb)

3.7.790 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb)—Offset 87C10h

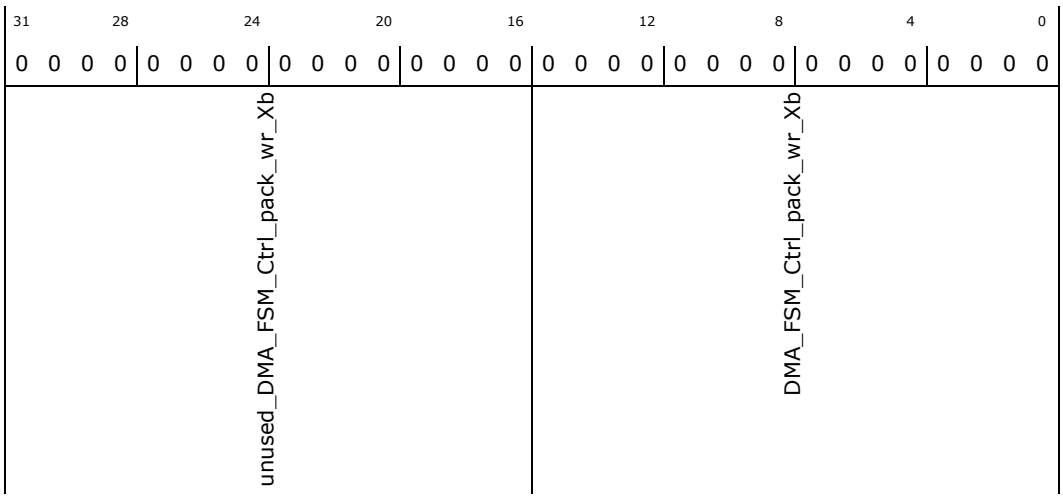
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb: [ISPMMADR] + 87C10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_wr_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_wr_Xb:** DMA FSM Control FSM Pack write width (Xb)

3.7.791 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem_type (inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 87D10h

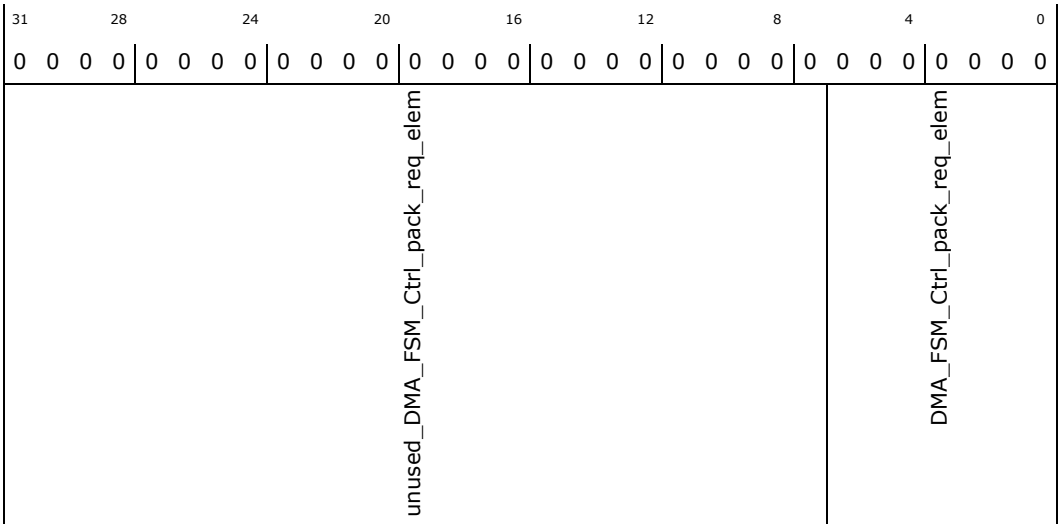
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem: [ISPMMADR] + 87D10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**unused_DMA_FSM_Ctrl_pack_req_elem:** Unused
6:0	0h RO	**DMA_FSM_Ctrl_pack_req_elem:** DMA FSM Control pack request element per word

3.7.792 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem_type (inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 87E10h

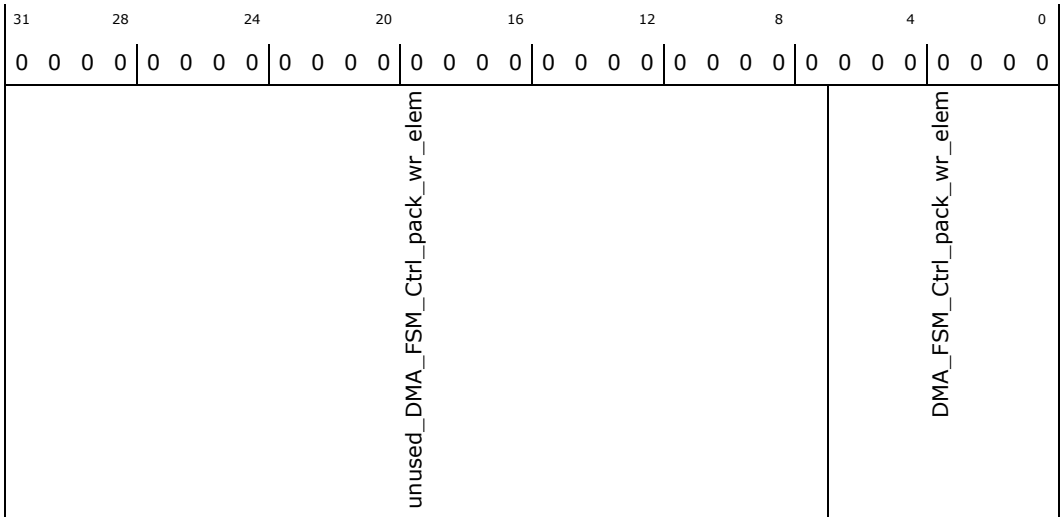
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem: [ISPMMADR] + 87E10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**unused_DMA_FSM_Ctrl_pack_wr_elem:** Unused
6:0	0h RO	**DMA_FSM_Ctrl_pack_wr_elem:** DMA FSM Control pack write element per word

3.7.793 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id_type (inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id)—Offset 87F10h

DMA FSM Control pack element sign zero extension and controller ID

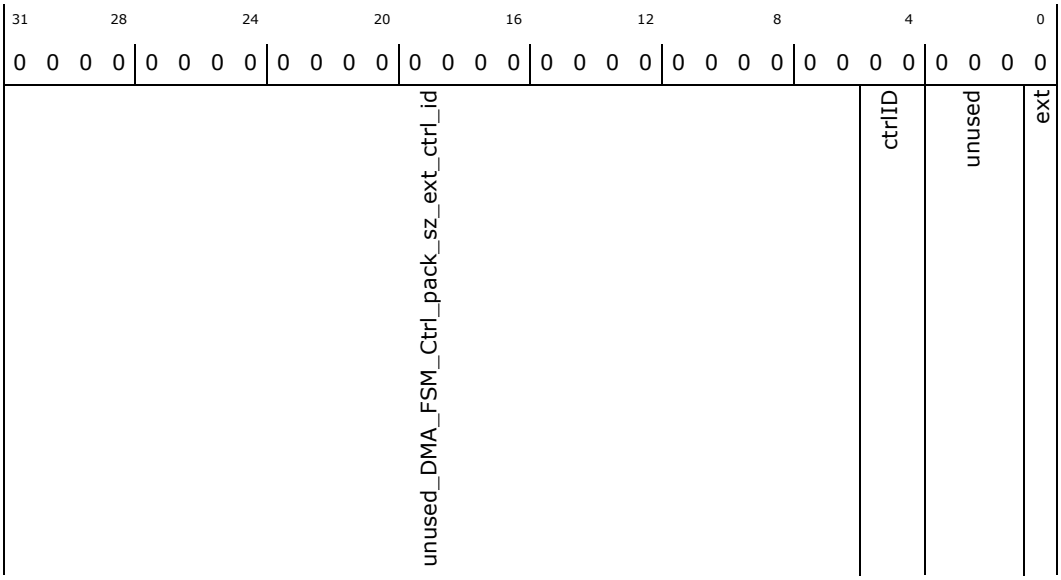
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id: [ISPMMADR] + 87F10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id:** Unused
5:4	0h RO	**ctrlID:** Controller ID
3:1	0h RO	**unused:** unused
0	0h RO	**ext:** element sign(1)/zero(0) extension

3.7.794 reg_inp_sys_dma_Dev_Interf_0_req_side_type (inp_sys_dma_Dev_Interf_0_req_side)—Offset 88000h

DMA Device interface 0 internal side status

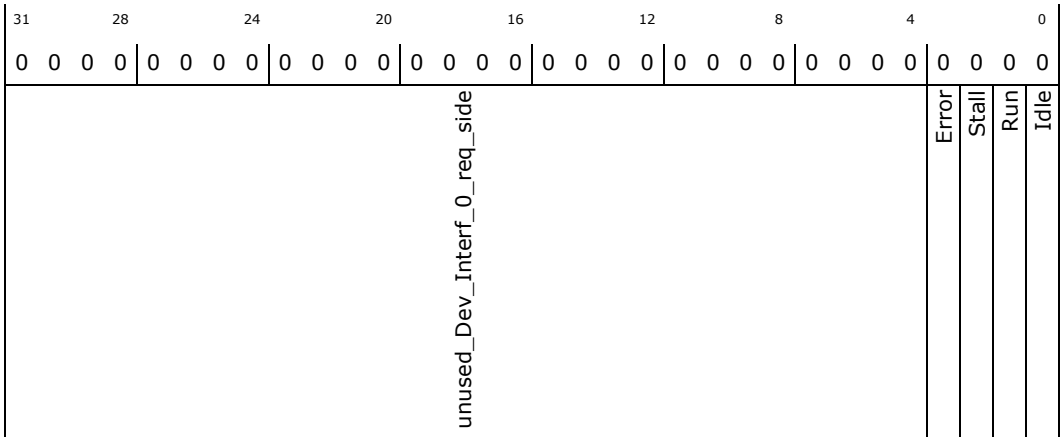
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_0_req_side: [ISPMMADR] + 88000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_0_req_side:** Unused
3	0h RO	**Error:** Ack flag
2	0h RO	**Stall:** Run flag
1	0h RO	**Run:** We_n flag
0	0h RO	**Idle:** CS flag

3.7.795 reg_inp_sys_dma_Dev_Interf_1_req_side_type (inp_sys_dma_Dev_Interf_1_req_side)—Offset 88004h

DMA Device interface 1 internal side status

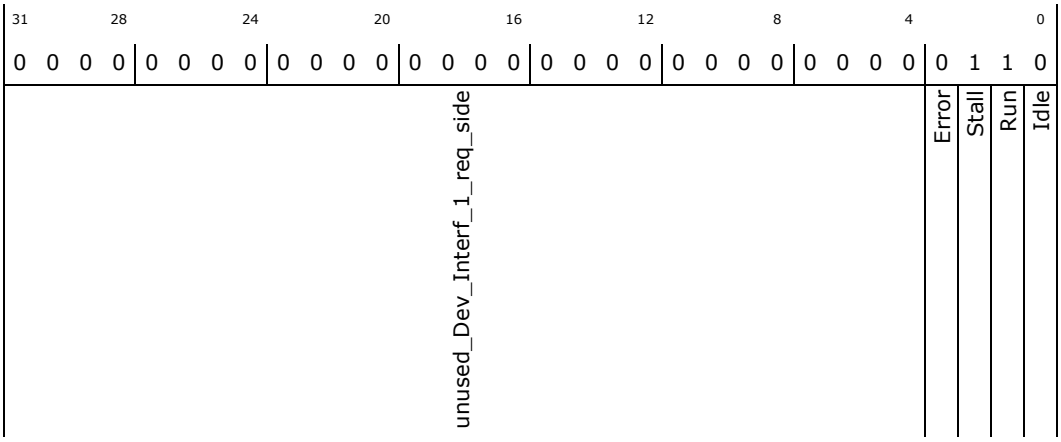
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_1_req_side: [ISPMMADR] + 88004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_1_req_side:** Unused
3	0h RO	**Error:** Ack flag
2	1h RO	**Stall:** Run flag
1	1h RO	**Run:** We_n flag
0	0h RO	**Idle:** CS flag

3.7.796 reg_inp_sys_dma_Dev_Interf_0_snd_side_type (inp_sys_dma_Dev_Interf_0_snd_side)—Offset 88100h

DMA Device interface 0 output side status

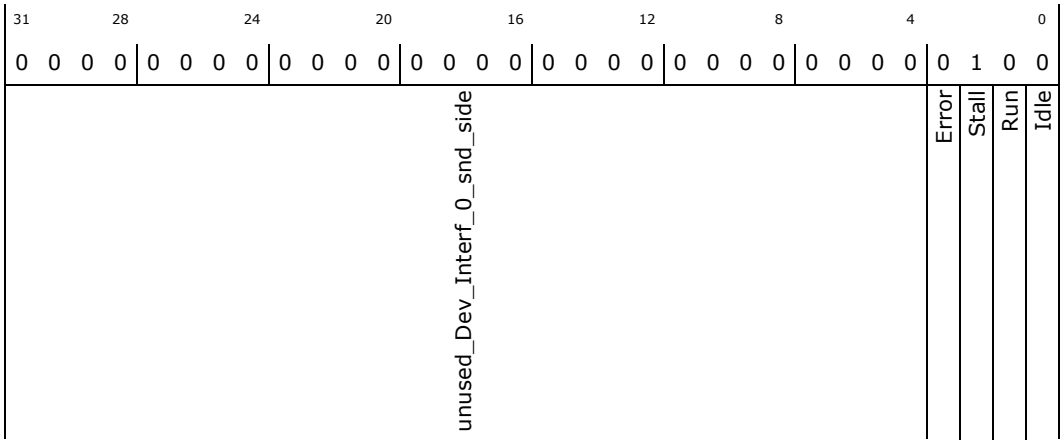
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_0_snd_side: [ISPMMADR] + 88100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_0_snd_side:** Unused
3	0h RO	**Error:** Ack flag
2	1h RO	**Stall:** Run flag
1	0h RO	**Run:** We_n flag
0	0h RO	**Idle:** CS flag

3.7.797 reg_inp_sys_dma_Dev_Interf_1_snd_side_type (inp_sys_dma_Dev_Interf_1_snd_side)—Offset 88104h

DMA Device interface 1 output side status

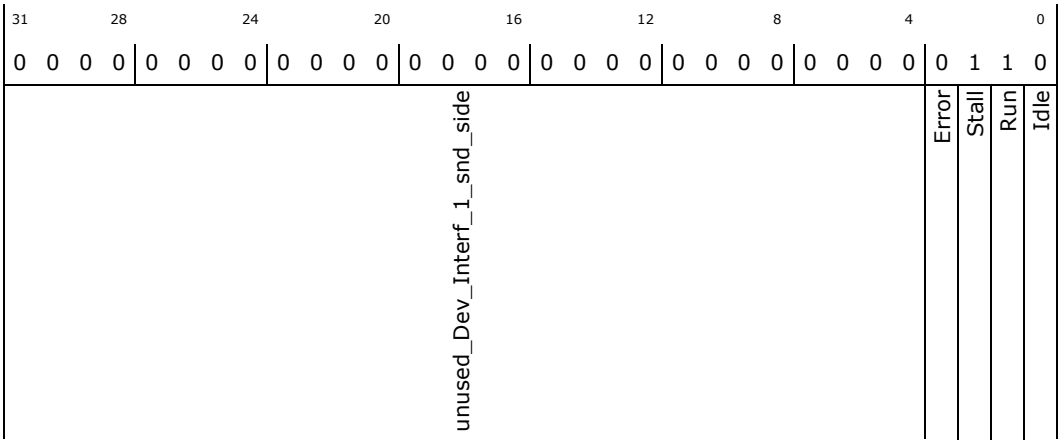
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_1_snd_side: [ISPMMADR] + 88104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_1_snd_side:** Unused
3	0h RO	**Error:** Ack flag
2	1h RO	**Stall:** Run flag
1	1h RO	**Run:** We_n flag
0	0h RO	**Idle:** CS flag

3.7.798 reg_inp_sys_dma_Dev_Interf_0_Fifo_status_type (inp_sys_dma_Dev_Interf_0_Fifo_status)—Offset 88200h

Device Interface 0 Fifo Status

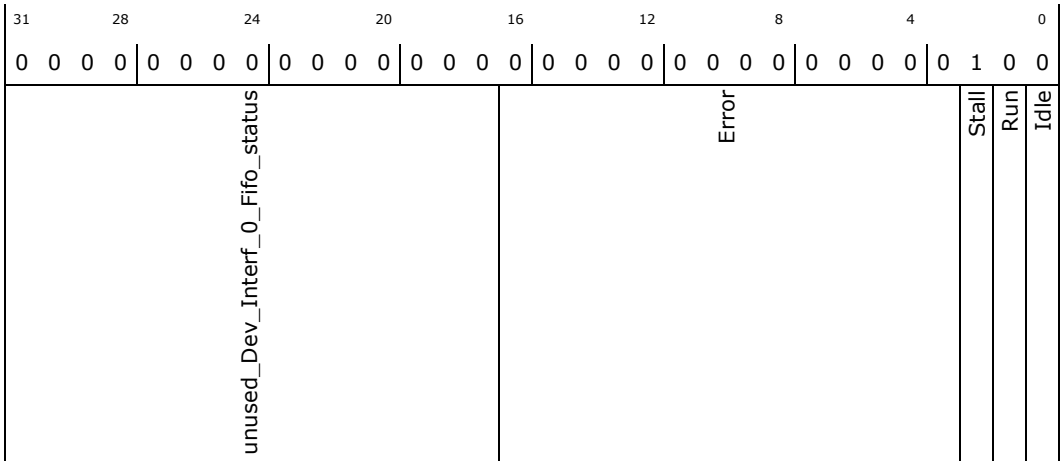
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_0_Fifo_status: [ISPMMADR] + 88200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_Dev_Interf_0_Fifo_status:** Unused
16:3	0h RO	**Error:** Fifo word counter
2	1h RO	**Stall:** Fifo is empty
1	0h RO	**Run:** Fifo is full
0	0h RO	**Idle:** Fifo will be full

3.7.799 reg_inp_sys_dma_Dev_Interf_1_Fifo_status_type (inp_sys_dma_Dev_Interf_1_Fifo_status)—Offset 88204h

Device Interface 1 Fifo Status

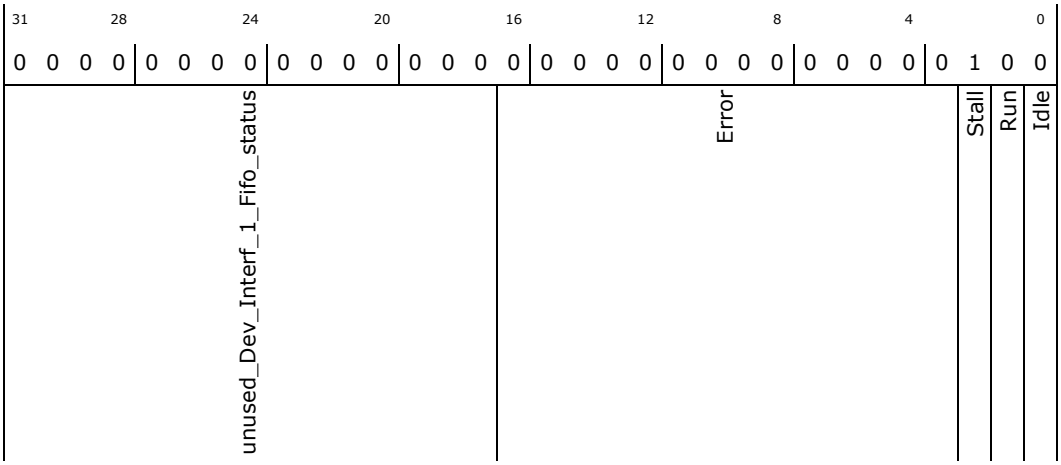
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_1_Fifo_status: [ISPMMADR] + 88204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:17	0h RW	**unused_Dev_Interf_1_Fifo_status:** Unused
16:3	0h RO	**Error:** Fifo word counter
2	1h RO	**Stall:** Fifo is empty
1	0h RO	**Run:** Fifo is full
0	0h RO	**Idle:** Fifo will be full

3.7.800 reg_inp_sys_dma_Dev_Interf_0_Req_complete_bust_type (inp_sys_dma_Dev_Interf_0_Req_complete_bust)—Offset 88300h

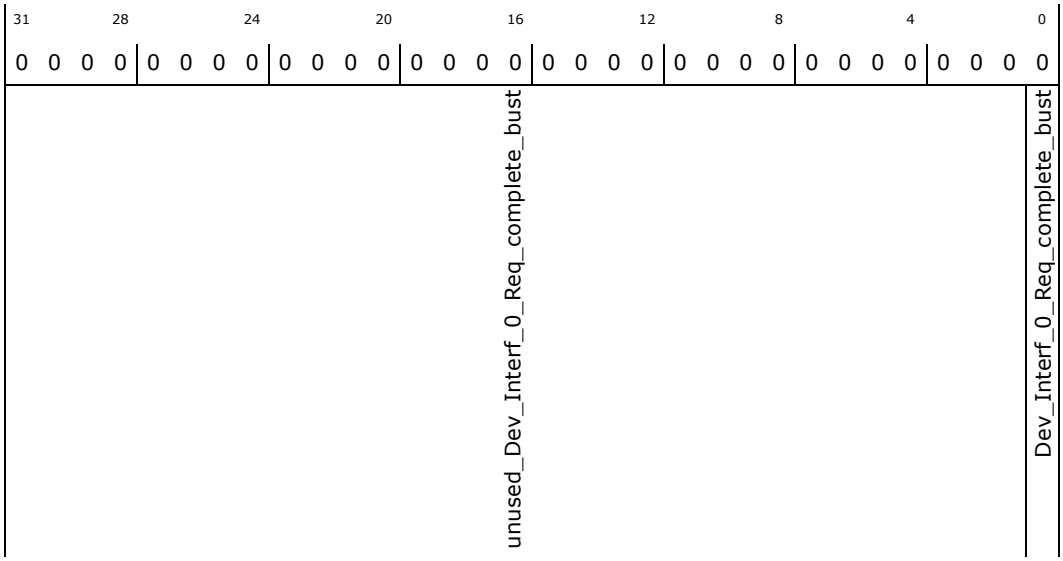
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_0_Req_complete_bust: [ISPMMADR] + 88300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_Dev_Interf_0_Req_complete_bust:** Unused
0	0h RW	**Dev_Interf_0_Req_complete_bust:** DMA Device interface 0 Request only complete burst

3.7.801 reg_inp_sys_dma_Dev_Interf_1_Req_complete_bust_type (inp_sys_dma_Dev_Interf_1_Req_complete_bust)—Offset 88304h

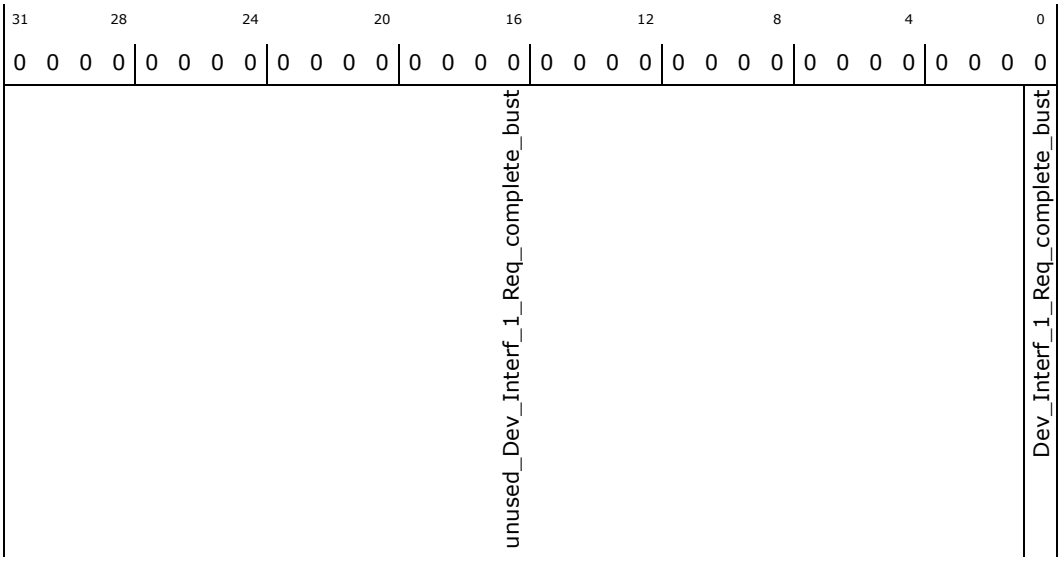
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_1_Req_complete_bust: [ISPMMADR] + 88304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_Dev_Interf_1_Req_complete_bust:** Unused
0	0h RW	**Dev_Interf_1_Req_complete_bust:** DMA Device interface 1 Request only complete burst

3.7.802 reg_inp_sys_dma_Dev_Interf_1_Max_burst_Size_type (inp_sys_dma_Dev_Interf_1_Max_burst_Size)—Offset 88400h

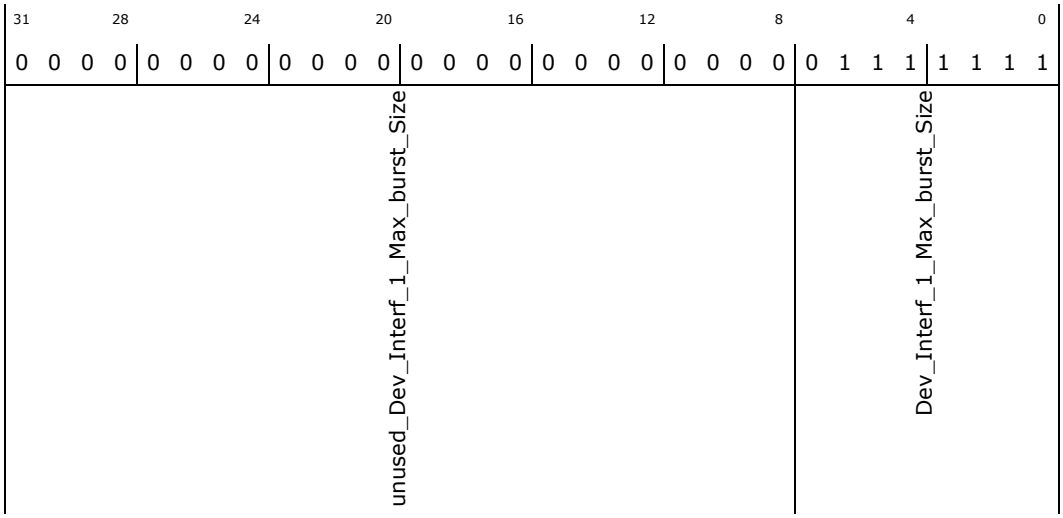
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_1_Max_burst_Size: [ISPMMADR] + 88400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:8	0h RW	**unused_Dev_Interf_1_Max_burst_Size:** Unused
7:0	7Fh RW	**Dev_Interf_1_Max_burst_Size:** DMA Device interface 1 max burst size

3.7.803 reg_inp_sys_inp_ctrl_inpsys_captA_start_addr_type (inp_sys_inp_ctrl_inpsys_captA_start_addr)—Offset 89000h

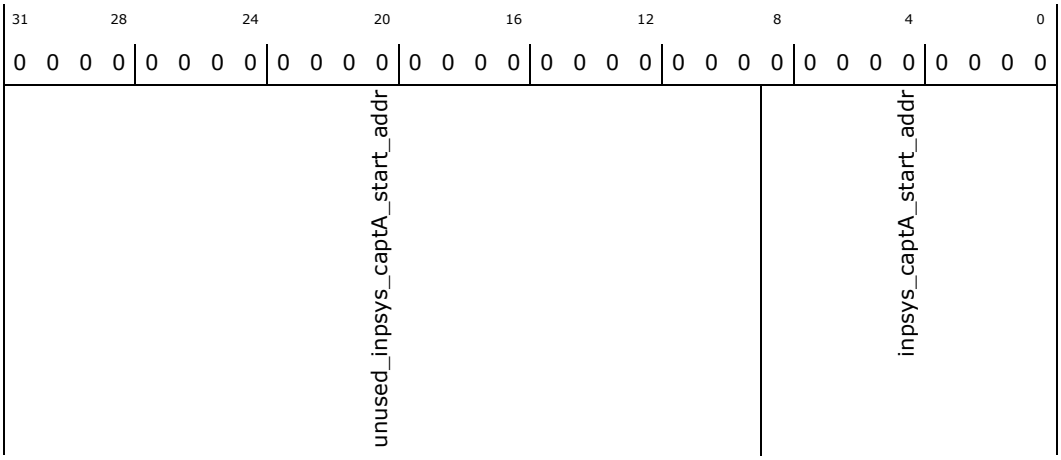
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captA_start_addr: [ISPMMADR] + 89000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captA_start_addr:** Unused
8:0	0h RW	**inpsys_captA_start_addr:** Input System Controller Capt A mem region start address

3.7.804 reg_inp_sys_inp_ctrl_inpsys_captB_start_addr_type (inp_sys_inp_ctrl_inpsys_captB_start_addr)—Offset 89004h

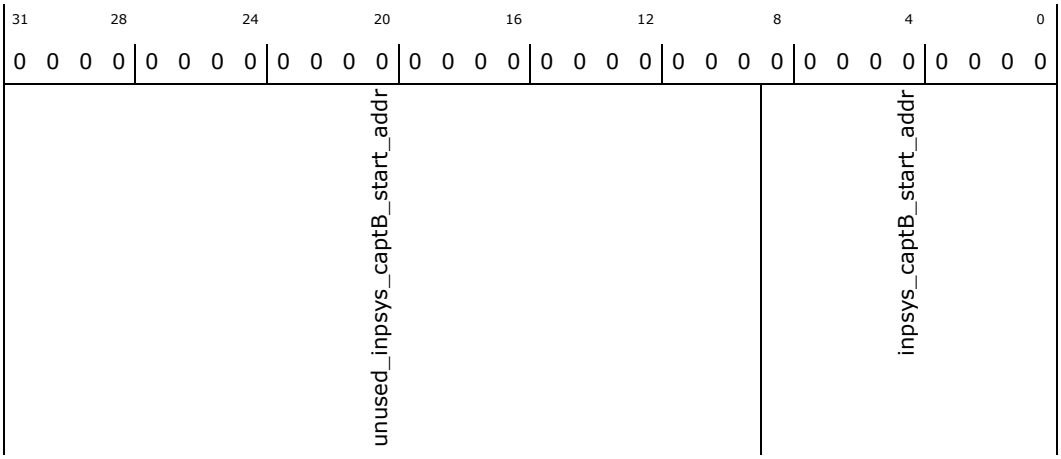
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captB_start_addr: [ISPMMADR] + 89004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captB_start_addr:** Unused
8:0	0h RW	**inpsys_captB_start_addr:** Input System Controller Capt B mem region start address

3.7.805 reg_inp_sys_inp_ctrl_inpsys_captC_start_addr_type (inp_sys_inp_ctrl_inpsys_captC_start_addr)—Offset 89008h

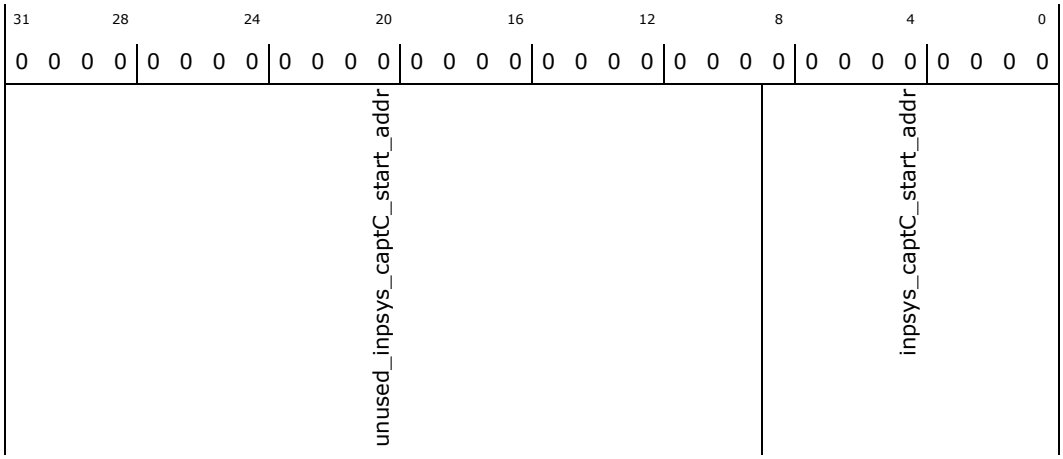
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captC_start_addr: [ISPMMADR] + 89008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captC_start_addr:** Unused
8:0	0h RW	**inpsys_captC_start_addr:** Input System Controller Capt C mem region start address

3.7.806 reg_inp_sys_inp_ctrl_inpsys_captA_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captA_mem_region_size)—Offset 8900Ch

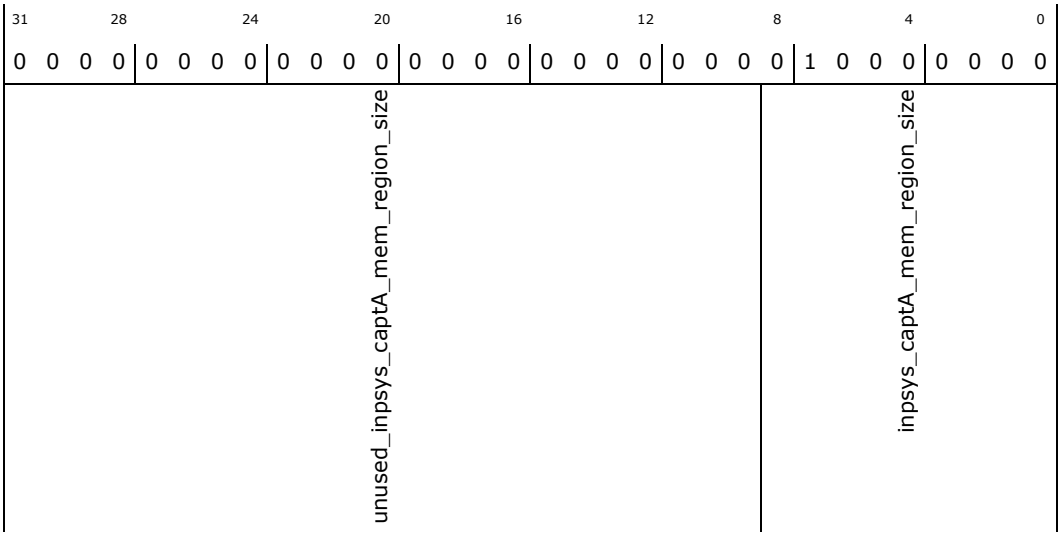
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captA_mem_region_size: [ISPMMADR] + 8900Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captA_mem_region_size:** Unused
8:0	080h RW	**inpsys_captA_mem_region_size:** Input System Controller Capt A mem region size

3.7.807 reg_inp_sys_inp_ctrl_inpsys_captB_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captB_mem_region_size)—Offset 89010h

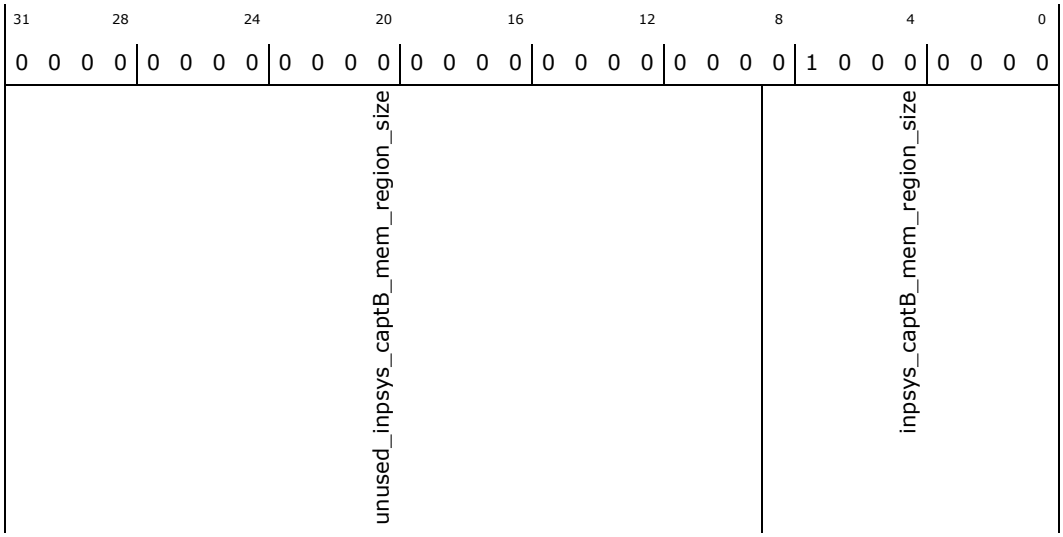
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captB_mem_region_size: [ISPMMADR] + 89010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captB_mem_region_size:** Unused
8:0	080h RW	**inpsys_captB_mem_region_size:** Input System Controller Capt B mem region size

3.7.808 reg_inp_sys_inp_ctrl_inpsys_captC_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captC_mem_region_size)—Offset 89014h

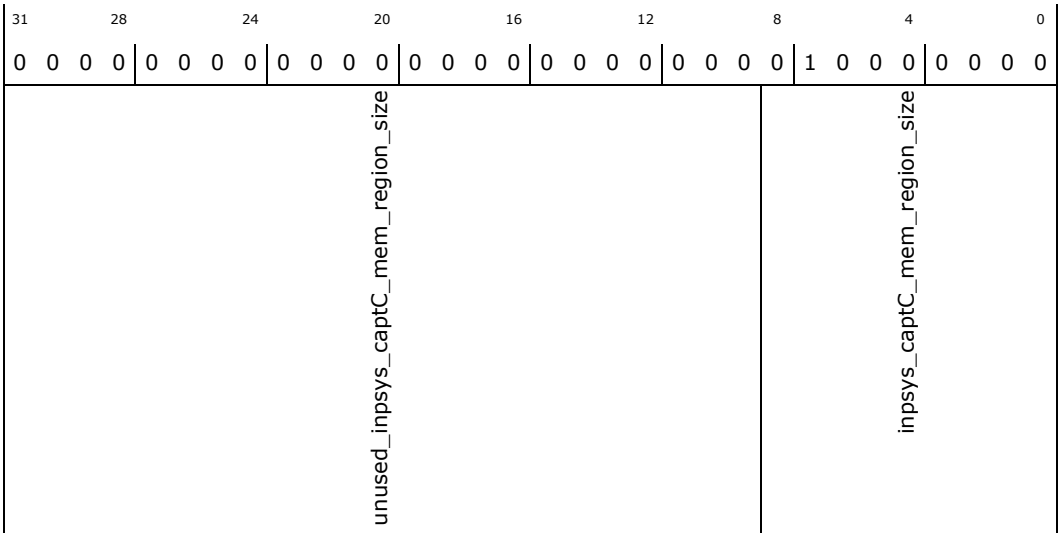
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captC_mem_region_size: [ISPMMADR] + 89014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captC_mem_region_size:** Unused
8:0	080h RW	**inpsys_captC_mem_region_size:** Input System Controller Capt C mem region size

3.7.809 reg_inp_sys_inp_ctrl_inpsys_captA_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captA_num_mem_regions)—Offset 89018h

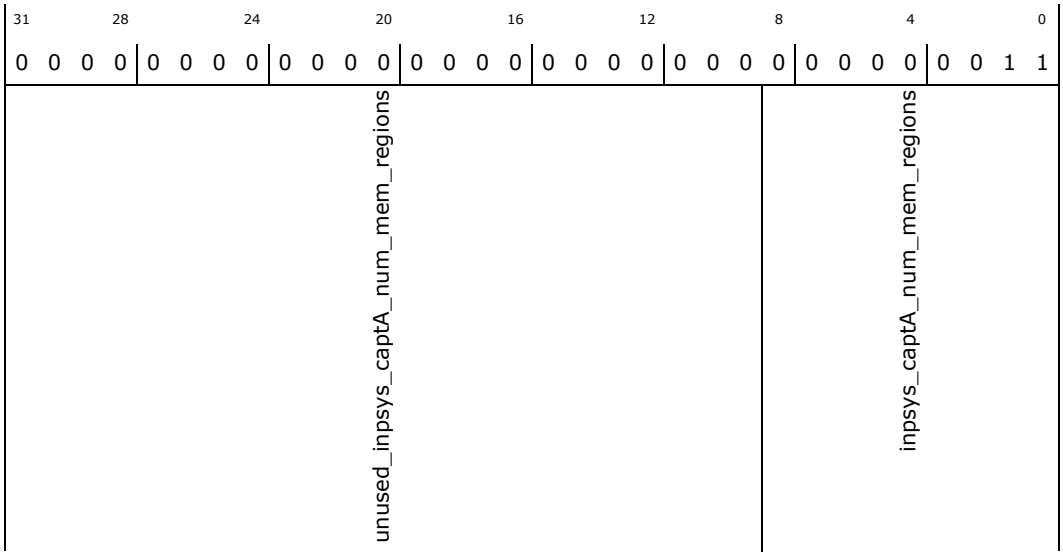
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captA_num_mem_regions: [ISPMMADR] + 89018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captA_num_mem_regions:** Unused
8:0	003h RW	**inpsys_captA_num_mem_regions:** Input System Controller Capt A number of mem regions

3.7.810 reg_inp_sys_inp_ctrl_inpsys_captB_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captB_num_mem_regions)—Offset 8901Ch

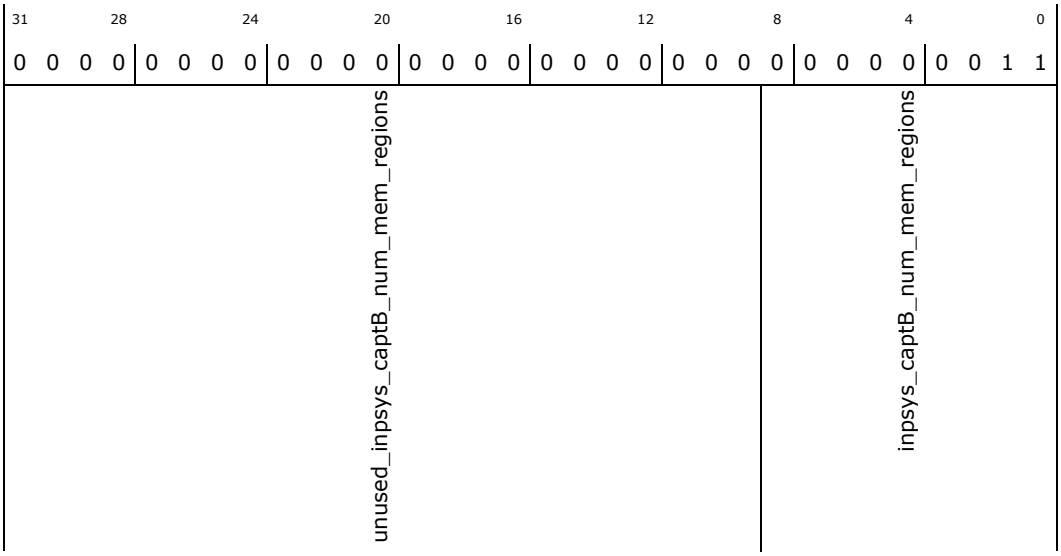
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captB_num_mem_regions: [ISPMMADR] + 8901Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captB_num_mem_regions:** Unused
8:0	003h RW	**inpsys_captB_num_mem_regions:** Input System Controller Capt B number of mem regions

3.7.811 reg_inp_sys_inp_ctrl_inpsys_captC_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captC_num_mem_regions)—Offset 89020h

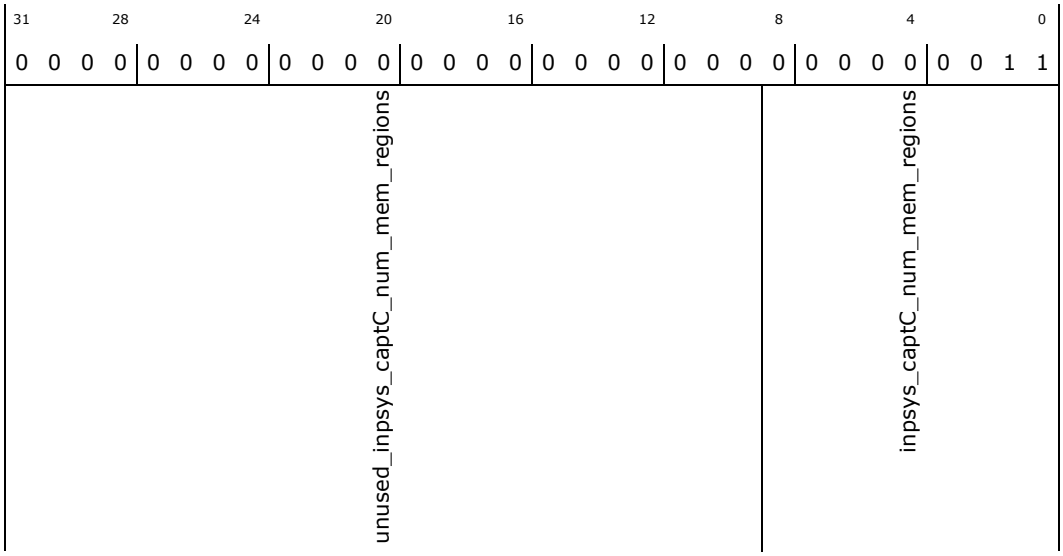
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captC_num_mem_regions: [ISPMMADR] + 89020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captC_num_mem_regions:** Unused
8:0	003h RW	**inpsys_captC_num_mem_regions:** Input System Controller Capt C number of mem regions

3.7.812 reg_inp_sys_inp_ctrl_inpsys_acq_start_addr_type (inp_sys_inp_ctrl_inpsys_acq_start_addr)—Offset 89024h

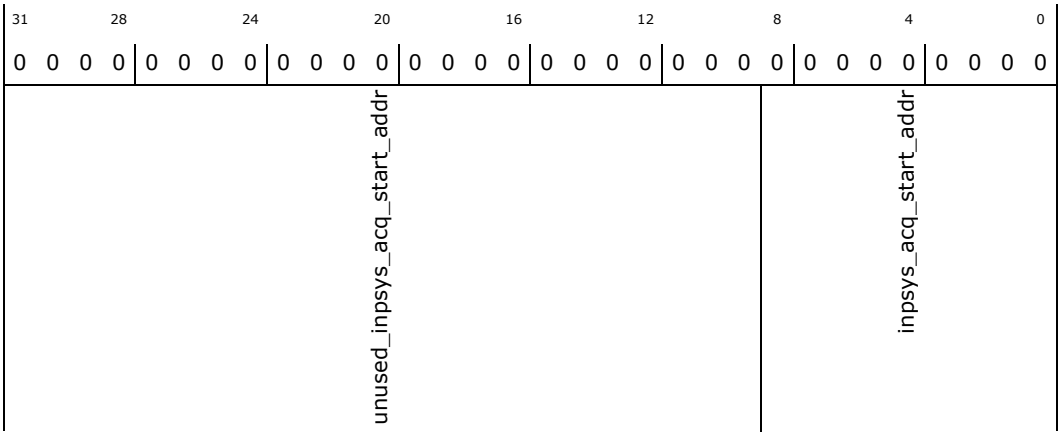
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_acq_start_addr: [ISPMMADR] + 89024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_acq_start_addr:** Unused
8:0	0h RW	**inpsys_acq_start_addr:** Input System Controller Acquisition mem region start address

3.7.813 reg_inp_sys_inp_ctrl_inpsys_acq_mem_region_size_type (inp_sys_inp_ctrl_inpsys_acq_mem_region_size)—Offset 89028h

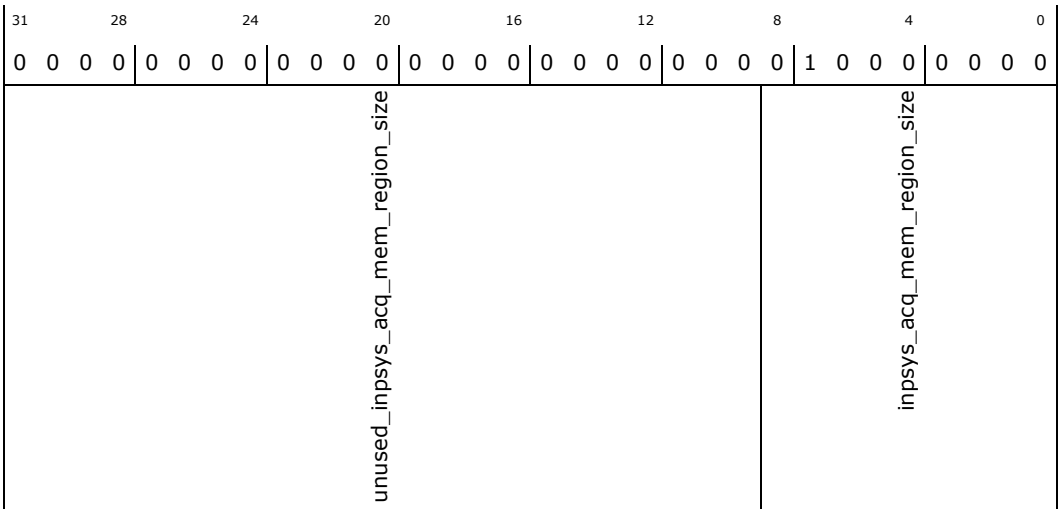
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_acq_mem_region_size: [ISPMMADR] + 89028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_acq_mem_region_size:** Unused
8:0	080h RW	**inpsys_acq_mem_region_size:** Input System Controller Acquisition mem region size

3.7.814 reg_inp_sys_inp_ctrl_inpsys_acq_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_acq_num_mem_regions)—Offset 8902Ch

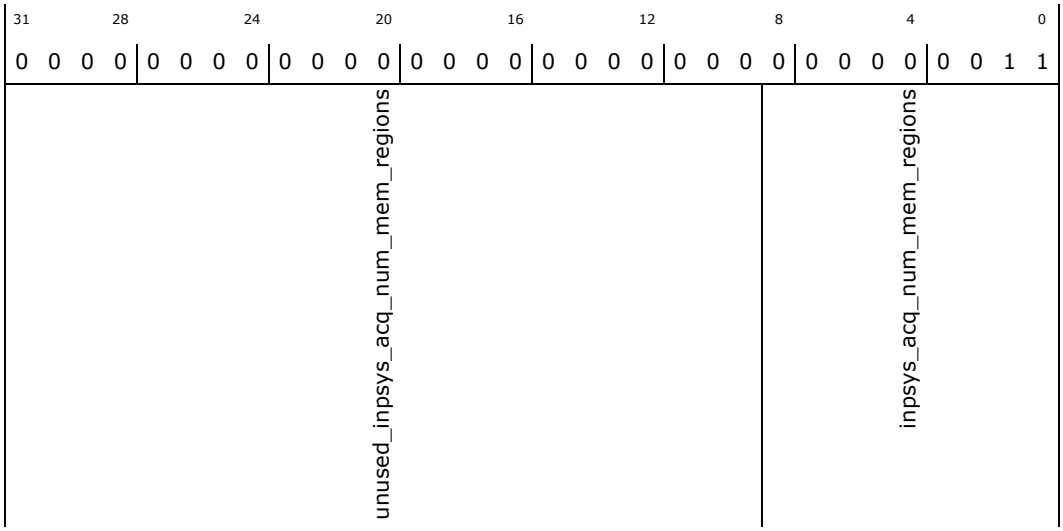
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_acq_num_mem_regions: [ISPMMADR] + 8902Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_acq_num_mem_regions:** Unused
8:0	003h RW	**inpsys_acq_num_mem_regions:** Input System Controller Acquisition number of mem regions

3.7.815 reg_inp_sys_inp_ctrl_inpsys_ctrl_init_type (inp_sys_inp_ctrl_inpsys_ctrl_init)—Offset 89030h

Input System Controller initialization register

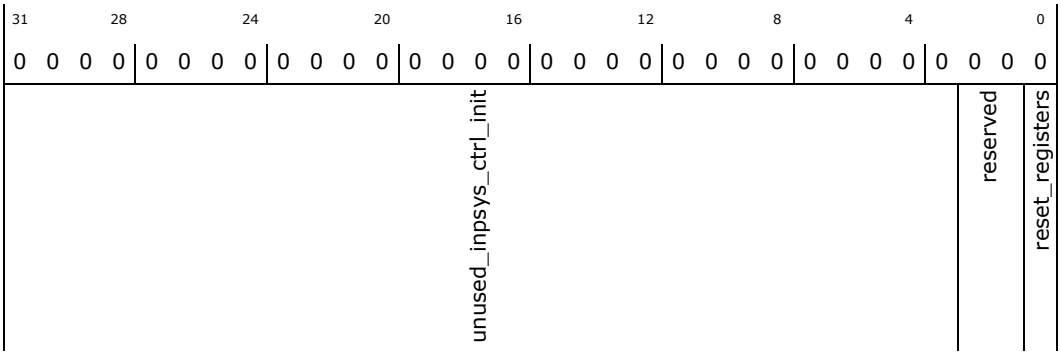
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_ctrl_init: [ISPMMADR] + 89030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RW	**unused_inpsys_ctrl_init:** Unused
2:1	0h RW	**reserved:** reserved bits, no action for now
0	0h RW	**reset_registers:** Reset all registers in Input System Controller

3.7.816 reg_inp_sys_inp_ctrl_inpsys_last_cmd_type (inp_sys_inp_ctrl_inpsys_last_cmd)—Offset 89034h

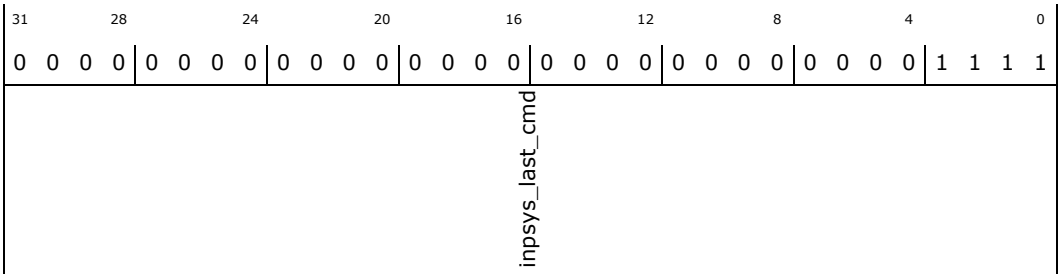
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_last_cmd: [ISPMMADR] + 89034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**inpsys_last_cmd:** Input System Controller last command register

3.7.817 reg_inp_sys_inp_ctrl_inpsys_next_cmd_type (inp_sys_inp_ctrl_inpsys_next_cmd)—Offset 89038h

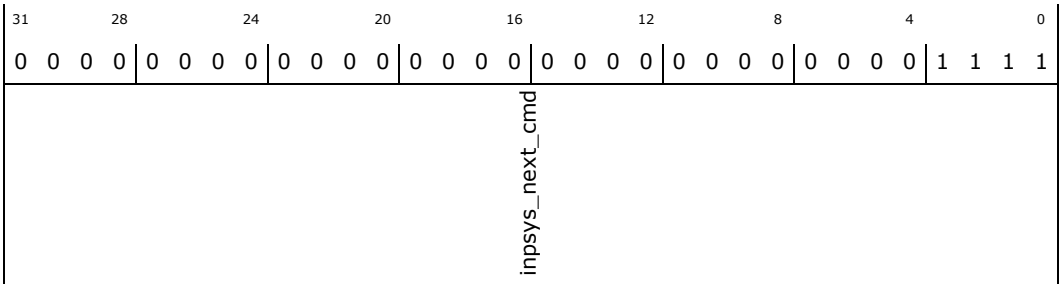
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_next_cmd: [ISPMMADR] + 89038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**inpsys_next_cmd:** Input System Controller next command register

3.7.818 reg_inp_sys_inp_ctrl_inpsys_last_ack_type (inp_sys_inp_ctrl_inpsys_last_ack)—Offset 8903Ch

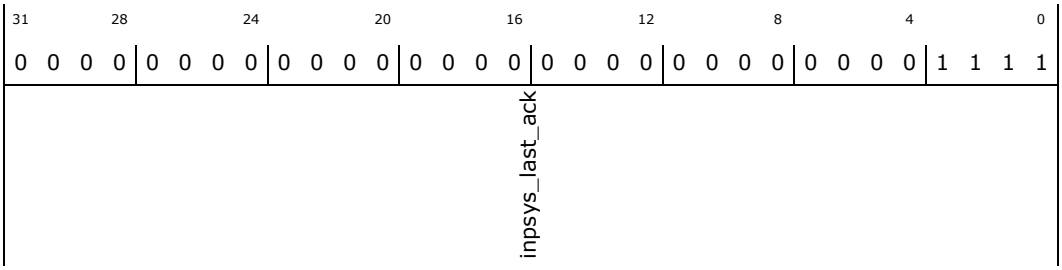
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_last_ack: [ISPMMADR] + 8903Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**inpsys_last_ack:** Input System Controller last acknowledge register

3.7.819 reg_inp_sys_inp_ctrl_inpsys_next_ack_type (inp_sys_inp_ctrl_inpsys_next_ack)—Offset 89040h

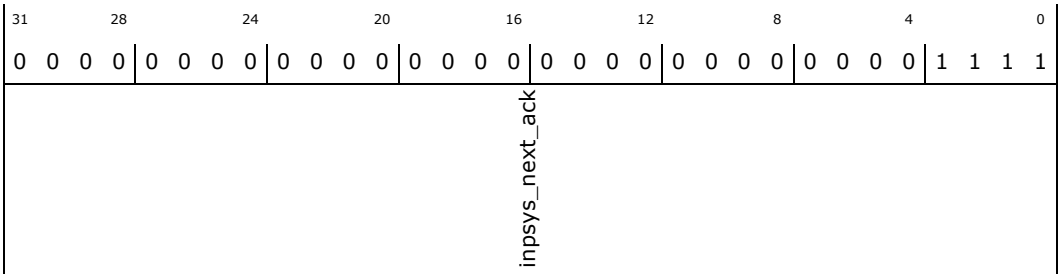
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_next_ack: [ISPMMADR] + 89040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default & Access	Description
31:0	0000000Fh RO	**inpsys_next_ack:** Input System Controller next acknowledge register

3.7.820 reg_inp_sys_inp_ctrl_inpsys_top_fsm_state_type (inp_sys_inp_ctrl_inpsys_top_fsm_state)—Offset 89044h

Input System Controller top-ctrl FSM current and next state info Register (both Cmd/ Ack FSM)

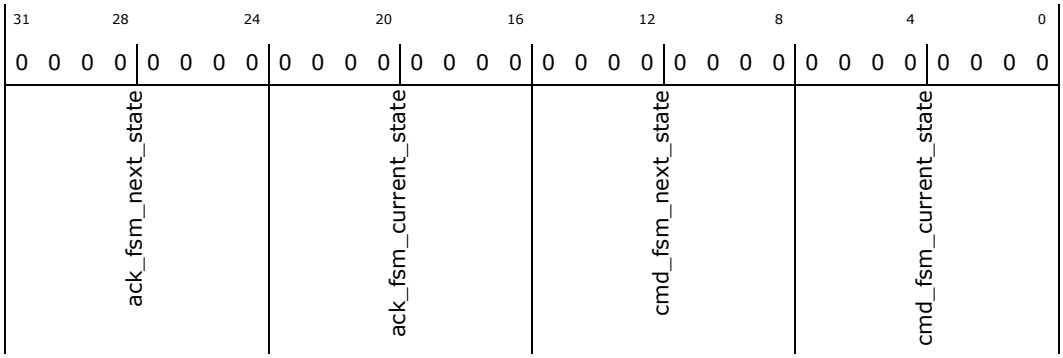
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_top_fsm_state: [ISPMMADR] + 89044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**ack_fsm_next_state:** Next state of top-ctrl Acknowledge FSM
23:16	0h RW	**ack_fsm_current_state:** Current state of top-ctrl Acknowledge FSM
15:8	0h RW	**cmd_fsm_next_state:** Next state of top-ctrl Command FSM
7:0	0h RW	**cmd_fsm_current_state:** Current state of top-ctrl Command FSM

3.7.821 reg_inp_sys_inp_ctrl_inpsys_captA_fsm_state_type (inp_sys_inp_ctrl_inpsys_captA_fsm_state)—Offset 89048h

Input System Controller captureA sub-ctrl current and next state info Register (FSM and DMA cmd state)

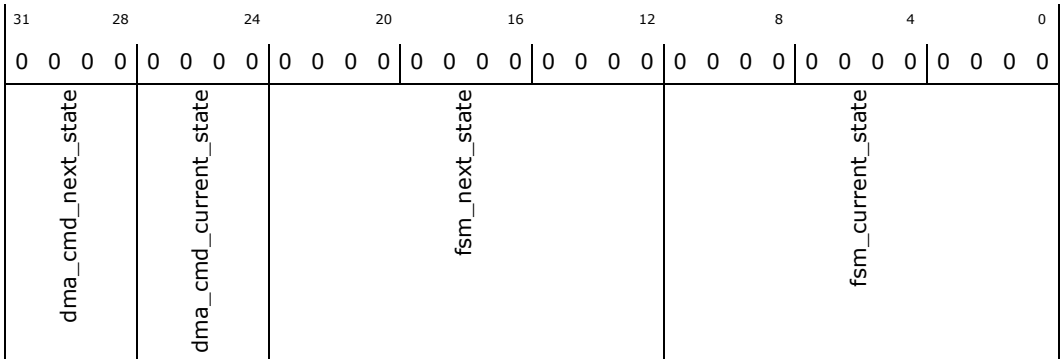
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captA_fsm_state: [ISPMMADR] + 89048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0h RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0h RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0h RW	**fsm_current_state:** Current state of sub-ctrl FSM

3.7.822 reg_inp_sys_inp_ctrl_inpsys_captB_fsm_state_type (inp_sys_inp_ctrl_inpsys_captB_fsm_state)—Offset 8904Ch

Input System Controller captureB sub-ctrl current and next state info Register (FSM and DMA cmd state)

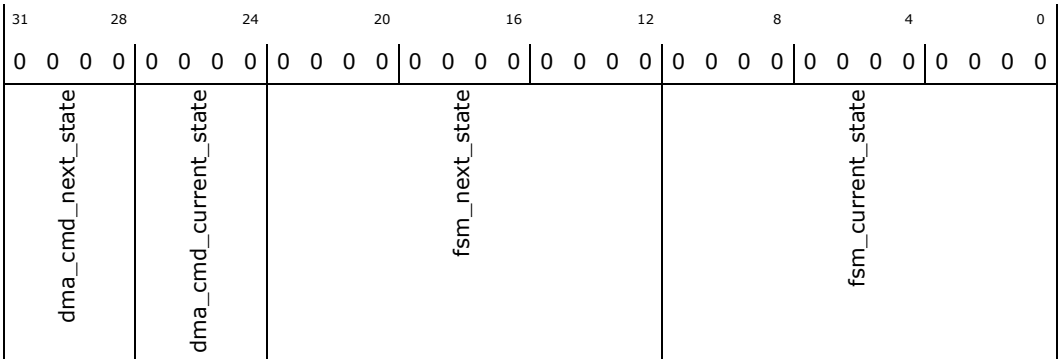
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captB_fsm_state: [ISPMMADR] + 8904Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0h RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0h RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0h RW	**fsm_current_state:** Current state of sub-ctrl FSM

3.7.823 reg_inp_sys_inp_ctrl_inpsys_captC_fsm_state_type (inp_sys_inp_ctrl_inpsys_captC_fsm_state)—Offset 89050h

Input System Controller captureC sub-ctrl current and next state info Register (FSM and DMA cmd state)

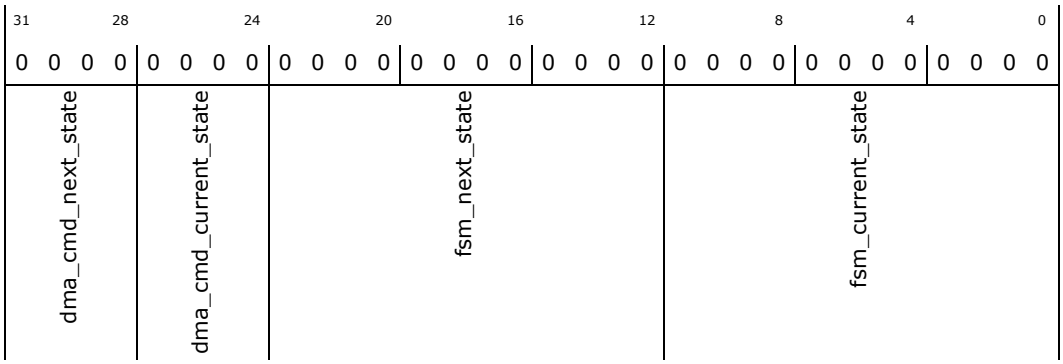
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captC_fsm_state: [ISPMMADR] + 89050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0h RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0h RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0h RW	**fsm_current_state:** Current state of sub-ctrl FSM

3.7.824 reg_inp_sys_inp_ctrl_inpsys_acq_fsm_state_type (inp_sys_inp_ctrl_inpsys_acq_fsm_state)—Offset 89054h

Input System Controller acquisition sub-ctrl current and next state info Register (FSM and DMA cmd state)

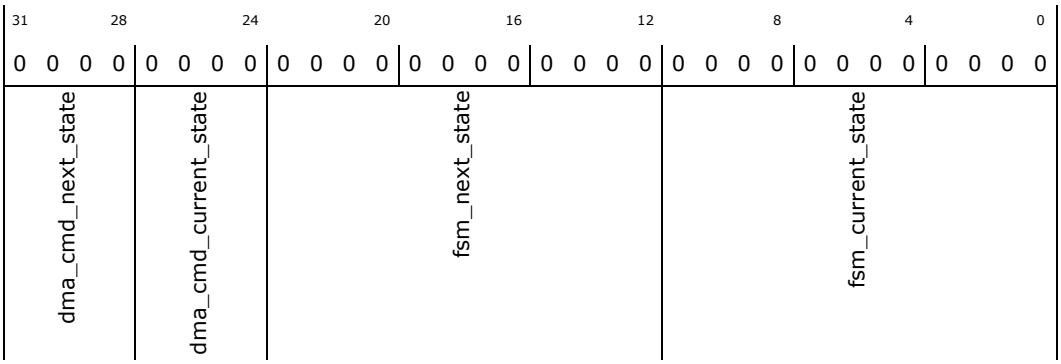
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_acq_fsm_state: [ISPMMADR] + 89054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0h RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0h RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0h RW	**fsm_current_state:** Current state of sub-ctrl FSM

3.7.825 reg_inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region_type (inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region)—Offset 89058h

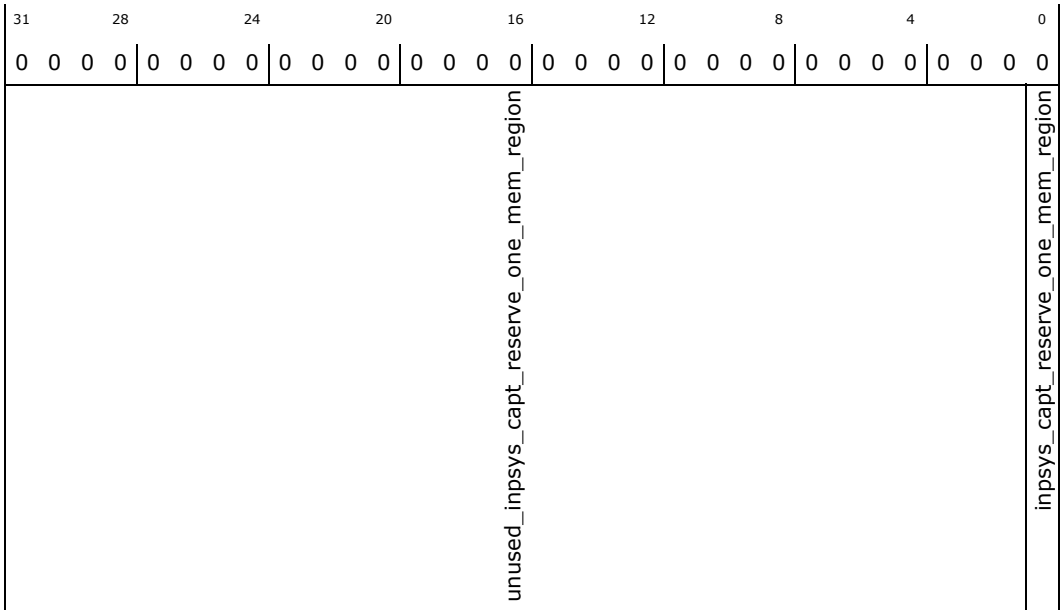
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region: [ISPMMADR] + 89058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_inpsys_capt_reserve_one_mem_region:** Unused
0	0h RW	**inpsys_capt_reserve_one_mem_region:** Reserve 1 or 0 mem region of capture units in input buffer to avoid overflow of captured data. 0: zero mem region reserved, 1: one mem region reserved

3.7.826 reg_inp_sys_gpreg_str_multicastA_sel_type (inp_sys_gpreg_str_multicastA_sel)—Offset 8A000h

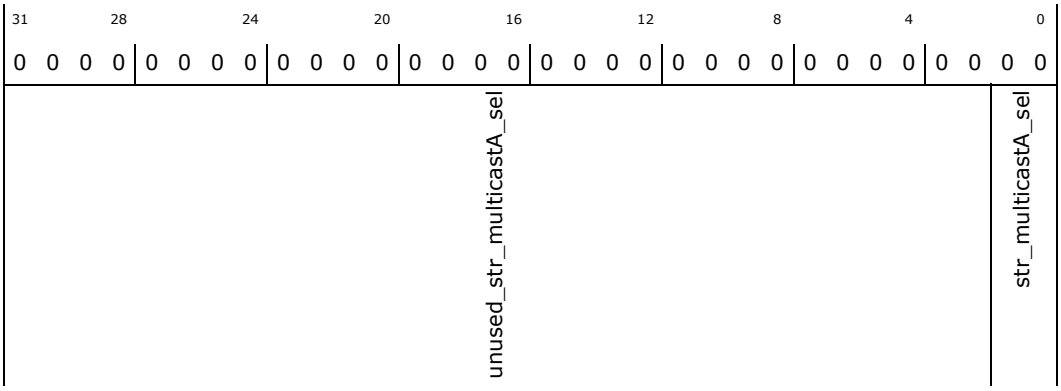
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_multicastA_sel: [ISPMMADR] + 8A000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_str_multicastA_sel:** Unused
1:0	0h RW	**str_multicastA_sel:** StreamMulticastA_select

3.7.827 reg_inp_sys_gpreg_str_multicastB_sel_type (inp_sys_gpreg_str_multicastB_sel)—Offset 8A004h

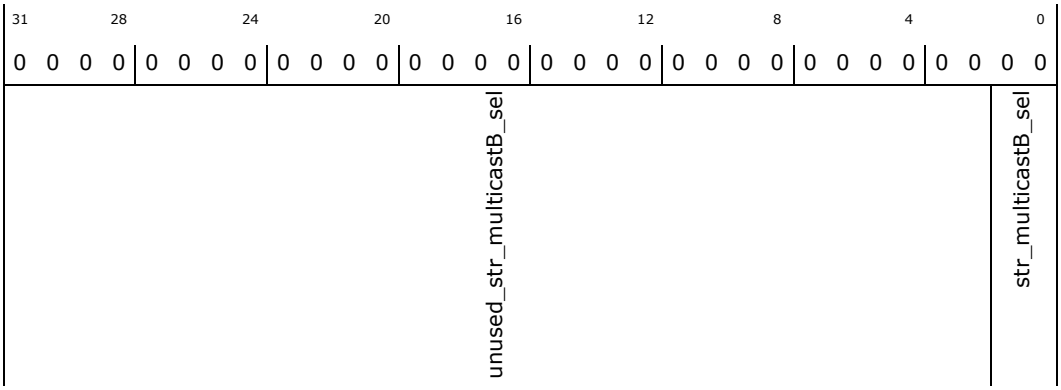
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_multicastB_sel: [ISPMMADR] + 8A004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_str_multicastB_sel:** Unused

Bit Range	Default & Access	Description
1:0	0h RW	**str_multicastB_sel:** StreamMulticastB_select

3.7.828 reg_inp_sys_gpreg_str_multicastC_sel_type (inp_sys_gpreg_str_multicastC_sel)—Offset 8A008h

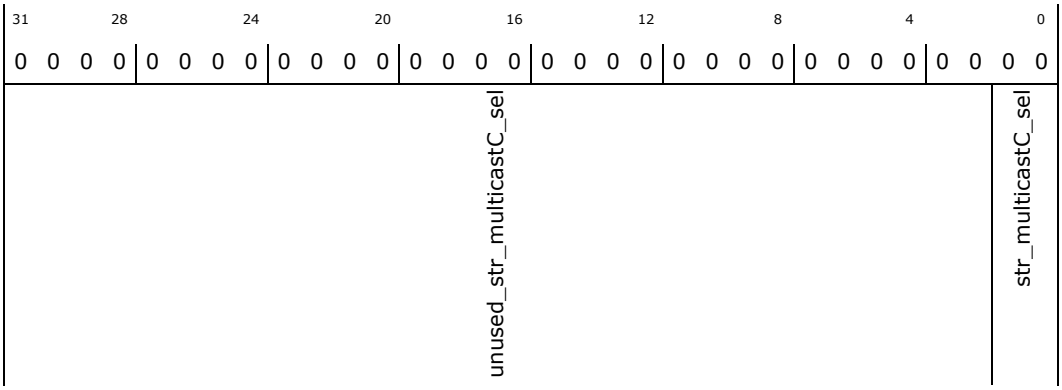
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_multicastC_sel: [ISPMMADR] + 8A008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_str_multicastC_sel:** Unused
1:0	0h RW	**str_multicastC_sel:** StreamMulticastC_select

3.7.829 reg_inp_sys_gpreg_str_mux_sel_type (inp_sys_gpreg_str_mux_sel)—Offset 8A00Ch

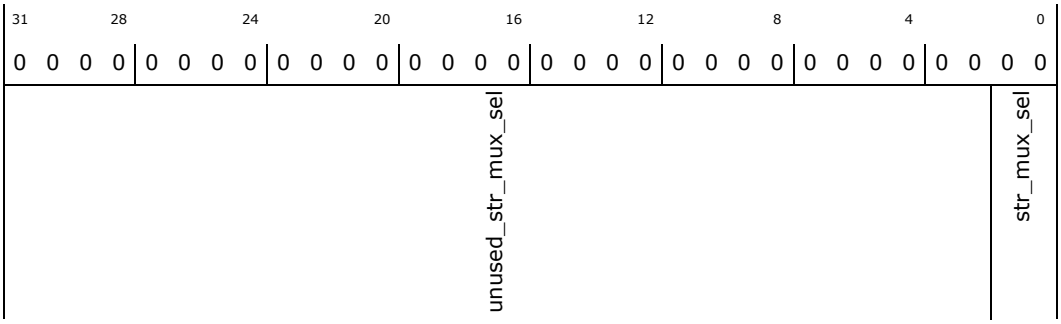
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_mux_sel: [ISPMMADR] + 8A00Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_str_mux_sel:** Unused
1:0	0h RW	**str_mux_sel:** StreamMux_select

3.7.830 reg_inp_sys_gpreg_str_mon_status_type (inp_sys_gpreg_str_mon_status)—Offset 8A010h

Streaming Monitor Status, [accept,valid] of streaming port

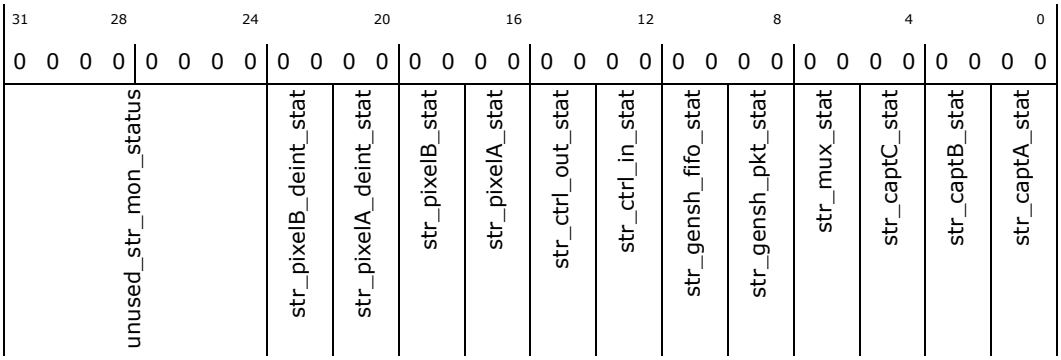
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_mon_status: [ISPMMADR] + 8A010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_str_mon_status:** Unused
23:22	0h RW	**str_pixelB_deint_stat:** Pixel B streaming output from Stream Deinterleaver

Bit Range	Default & Access	Description
21:20	0h RW	**str_pixelA_deint_stat:** Pixel A streaming output from Stream Deinterleaver
19:18	0h RW	**str_pixelB_stat:** Pixel B streaming output from CSI receiver
17:16	0h RW	**str_pixelA_stat:** Pixel A streaming output from CSI receiver
15:14	0h RW	**str_ctrl_out_stat:** Control streaming output
13:12	0h RW	**str_ctrl_in_stat:** Control streaming input
11:10	0h RW	**str_gensh_fifo_stat:** Generic short FIFO streaming output
9:8	0h RW	**str_gensh_pkt_stat:** Generic short packet streaming output from CSI receiver
7:6	0h RW	**str_mux_stat:** Stream Mux streaming output
5:4	0h RW	**str_captC_stat:** Capture port C streaming output from CSI receiver
3:2	0h RW	**str_captB_stat:** Capture port B streaming output from CSI receiver
1:0	0h RW	**str_captA_stat:** Capture port A streaming output from CSI receiver

3.7.831 reg_inp_sys_gpreg_str_mon_irq_cond_type (inp_sys_gpreg_str_mon_irq_cond)—Offset 8A014h

Streaming Monitor IRQ condition, [accept,valid] for streaming port

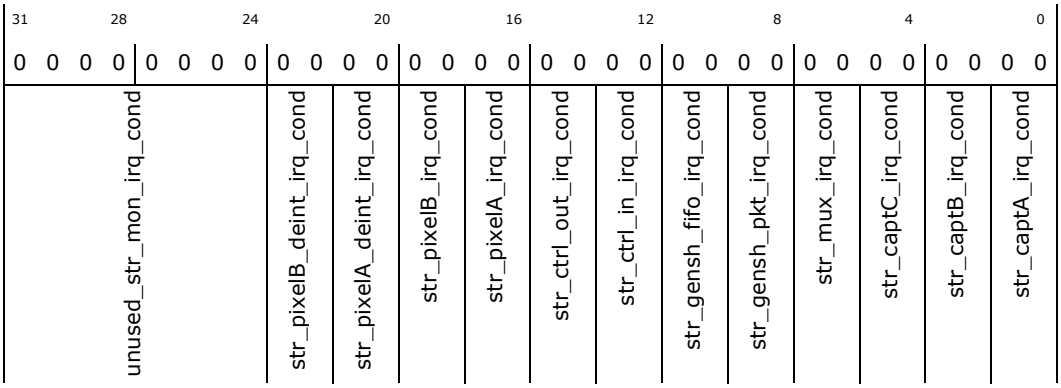
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_mon_irq_cond: [ISPMMADR] + 8A014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_str_mon_irq_cond:** Unused
23:22	0h RW	**str_pixelB_deint_irq_cond:** Pixel B streaming output from Stream Deinterleaver
21:20	0h RW	**str_pixelA_deint_irq_cond:** Pixel A streaming output from Stream Deinterleaver
19:18	0h RW	**str_pixelB_irq_cond:** Pixel B streaming output from CSI receiver
17:16	0h RW	**str_pixelA_irq_cond:** Pixel A streaming output from CSI receiver
15:14	0h RW	**str_ctrl_out_irq_cond:** Control streaming output
13:12	0h RW	**str_ctrl_in_irq_cond:** Control streaming input
11:10	0h RW	**str_gensh_fifo_irq_cond:** Generic short FIFO streaming output
9:8	0h RW	**str_gensh_pkt_irq_cond:** Generic short packet streaming output from CSI receiver
7:6	0h RW	**str_mux_irq_cond:** Stream Mux streaming output
5:4	0h RW	**str_captC_irq_cond:** Capture port C streaming output from CSI receiver
3:2	0h RW	**str_captB_irq_cond:** Capture port B streaming output from CSI receiver
1:0	0h RW	**str_captA_irq_cond:** Capture port A streaming output from CSI receiver

3.7.832 reg_inp_sys_gpreg_str_mon_irq_en_type (inp_sys_gpreg_str_mon_irq_en)—Offset 8A018h

Streaming Monitor IRQ enable

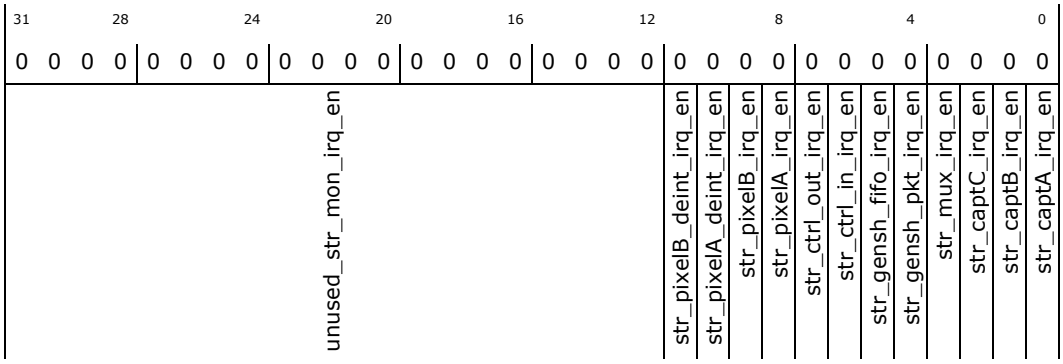
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_mon_irq_en: [ISPMMADR] + 8A018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_str_mon_irq_en:** Unused
11	0h RW	**str_pixelB_deint_irq_en:** Pixel B streaming output from Stream Deinterleaver
10	0h RW	**str_pixelA_deint_irq_en:** Pixel A streaming output from Stream Deinterleaver
9	0h RW	**str_pixelB_irq_en:** Pixel B streaming output from CSI receiver
8	0h RW	**str_pixelA_irq_en:** Pixel A streaming output from CSI receiver
7	0h RW	**str_ctrl_out_irq_en:** Control streaming output
6	0h RW	**str_ctrl_in_irq_en:** Control streaming input
5	0h RW	**str_gensh_fifo_irq_en:** Generic short FIFO streaming output
4	0h RW	**str_gensh_pkt_irq_en:** Generic short packet streaming output from CSI receiver
3	0h RW	**str_mux_irq_en:** Stream Mux streaming output
2	0h RW	**str_captC_irq_en:** Capture port C streaming output from CSI receiver
1	0h RW	**str_captB_irq_en:** Capture port B streaming output from CSI receiver
0	0h RW	**str_captA_irq_en:** Capture port A streaming output from CSI receiver

3.7.833 reg_inp_sys_gpreg_isys_srst_type (inp_sys_gpreg_isys_srst)—Offset 8A01Ch

Soft resets the modules of the input system. Writing a 1 to a field brings a module in reset, writing a 0 brings that module out of reset

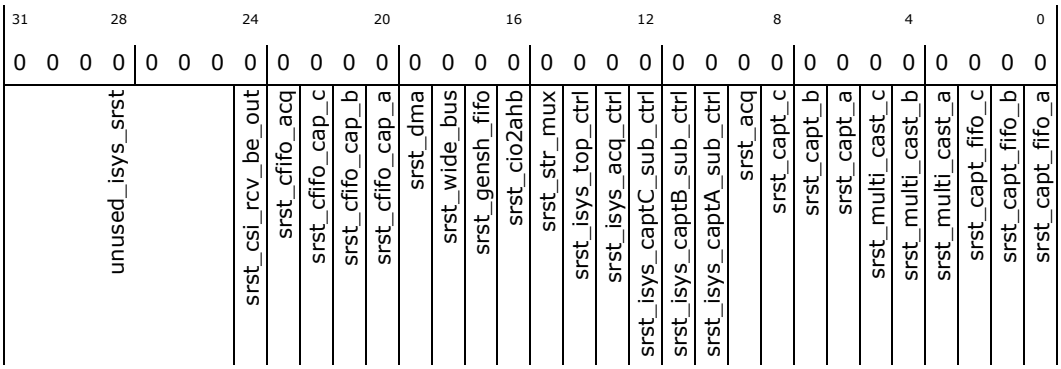
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_isys_srst: [ISPMMADR] + 8A01Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RW	**unused_isys_srst:** Unused
24	0h RW	**srst_csi_rcv_be_out:** Soft resets the output of the csi receiver backend
23	0h RW	**srst_cfifo_acq:** Soft resets the control and acknowledge FIFOs for the acquistion unit
22	0h RW	**srst_cfifo_cap_c:** Soft resets the control and acknowledge FIFOs for capture unit C
21	0h RW	**srst_cfifo_cap_b:** Soft resets the control and acknowledge FIFOs for capture unit B
20	0h RW	**srst_cfifo_cap_a:** Soft resets the control and acknowledge FIFOs for capture unit A
19	0h RW	**srst_dma:** Soft resets the DMA
18	0h RW	**srst_wide_bus:** Soft resets the wide bus including the CIO converter
17	0h RW	**srst_gensh_fifo:** Soft resets the generic short FIFO
16	0h RW	**srst_cio2ahb:** Soft resets the CIO2AHB adapter
15	0h RW	**srst_str_mux:** Soft resets the streaming mux

Bit Range	Default & Access	Description
14	0h RW	**srst_isys_top_ctrl:** Soft resets the input system Top controller
13	0h RW	**srst_isys_acq_ctrl:** Soft resets the input system Acquisition sub-controller (controls data-path from selected captA/captB/captC/dma_acq to acq)
12	0h RW	**srst_isys_captC_sub_ctrl:** Soft resets the input system CaptureC sub-controller (controls data-path from captC to dma_captC)
11	0h RW	**srst_isys_captB_sub_ctrl:** Soft resets the input system CaptureB sub-controller (controls data-path from captB to dma_captB)
10	0h RW	**srst_isys_captA_sub_ctrl:** Soft resets the input system CaptureA sub-controller (controls data-path from captA to dma_captA)
9	0h RW	**srst_acq:** Soft resets the acquision unit
8	0h RW	**srst_capt_c:** Soft resets the capture unit C
7	0h RW	**srst_capt_b:** Soft resets the capture unit B
6	0h RW	**srst_capt_a:** Soft resets the capture unit A
5	0h RW	**srst_multi_cast_c:** Soft resets multi cast C
4	0h RW	**srst_multi_cast_b:** Soft resets multi cast B
3	0h RW	**srst_multi_cast_a:** Soft resets multi cast A
2	0h RW	**srst_capt_fifo_c:** Soft resets the FIFO before multi cast C
1	0h RW	**srst_capt_fifo_b:** Soft resets the FIFO before multi cast B
0	0h RW	**srst_capt_fifo_a:** Soft resets the FIFO before multi cast A

3.7.834 reg_inp_sys_gpreg_isys_slv_reg_srst_type (inp_sys_gpreg_isys_slv_reg_srst)—Offset 8A020h

Soft resets the slave accessible registers of certain input system modules. Writing a 1 to a field brings the registers for a module to their default value, writing a 0 allows them to be overwritten

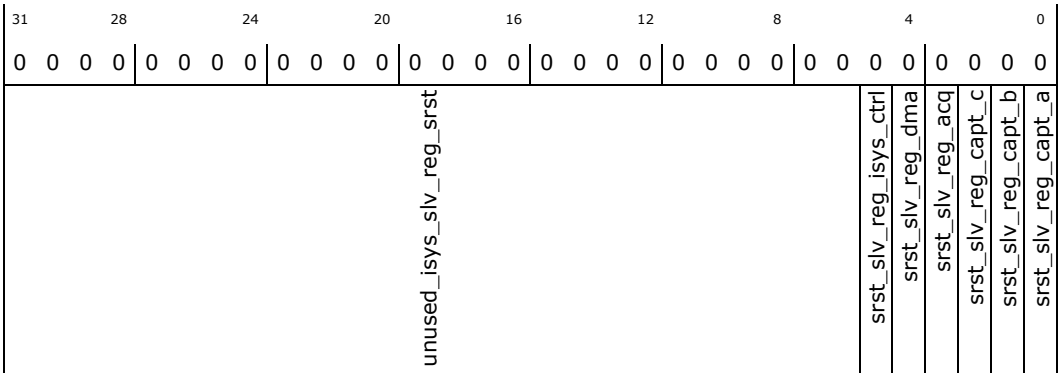
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_isys_slv_reg_srst: [ISPMMADR] + 8A020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_isys_slv_reg_srst:** Unused
5	0h RW	**srst_slv_reg_isys_ctrl:** Soft resets the slave accessible registers of the input system controller
4	0h RW	**srst_slv_reg_dma:** Soft resets the slave accessible registers of the DMA
3	0h RW	**srst_slv_reg_acq:** Soft resets the slave accessible registers of the acquisition unit
2	0h RW	**srst_slv_reg_capt_c:** Soft resets the slave accessible registers of capture unit C
1	0h RW	**srst_slv_reg_capt_b:** Soft resets the slave accessible registers of capture unit B
0	0h RW	**srst_slv_reg_capt_a:** Soft resets the slave accessible registers of capture unit A

3.7.835 reg_inp_sys_gpreg_str_deint_portA_cnt_type (inp_sys_gpreg_str_deint_portA_cnt)—Offset 8A024h

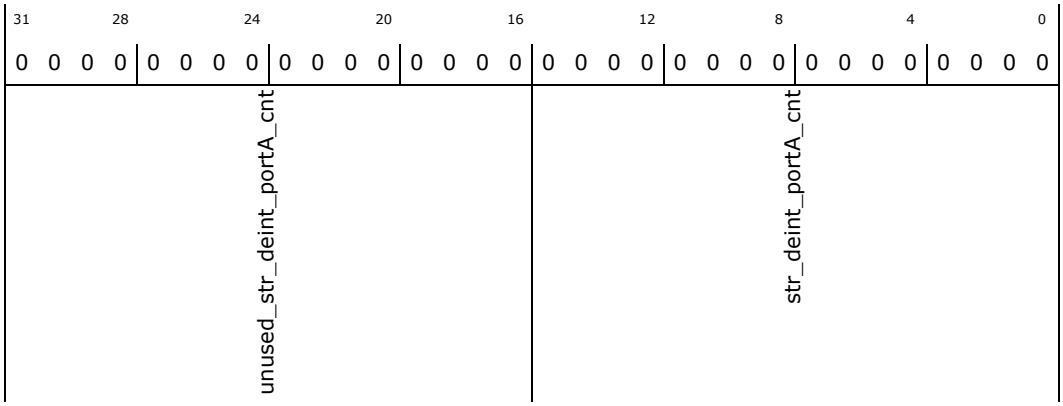
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_deint_portA_cnt: [ISPMMADR] + 8A024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_str_deint_portA_cnt:** Unused
15:0	0h RW	**str_deint_portA_cnt:** stream data count for portA of stream deinterleave block

3.7.836 reg_inp_sys_gpreg_str_deint_portB_cnt_type (inp_sys_gpreg_str_deint_portB_cnt)—Offset 8A028h

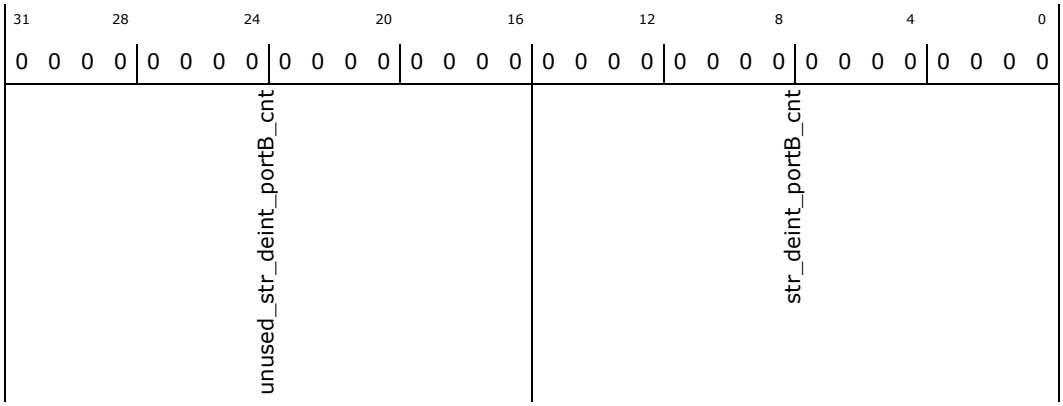
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_deint_portB_cnt: [ISPMMADR] + 8A028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_str_deint_portB_cnt:** Unused

Bit Range	Default & Access	Description
15:0	0h RW	**str_deint_portB_cnt:** stream data count for portB of stream deinterleave block

3.7.837 reg_inp_sys_fifo_adapter_CSI_generic_short_packet_available_type (inp_sys_fifo_adapter_CSI_generic_short_packet_available)—Offset 8B008h

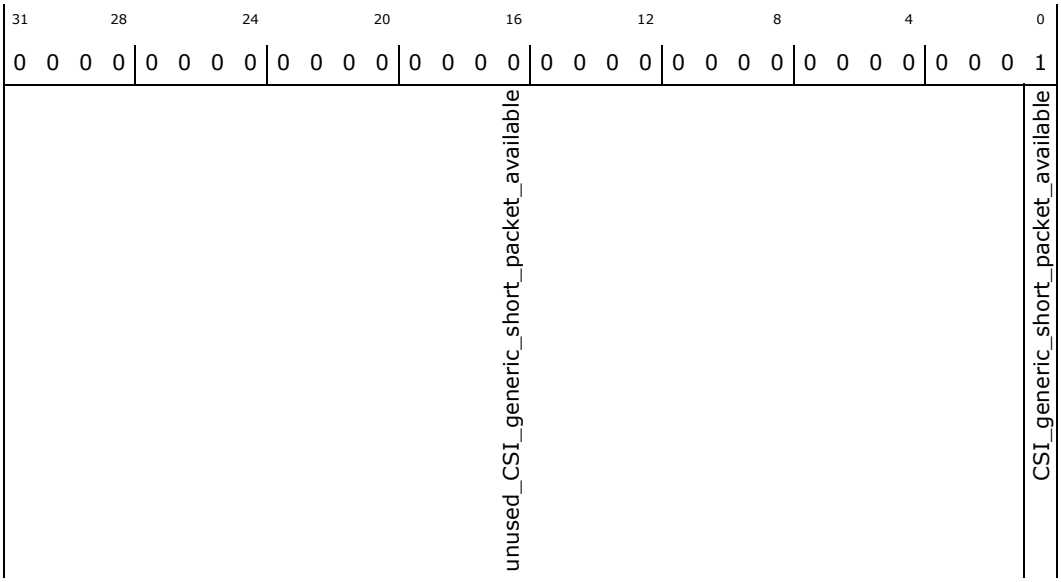
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_fifo_adapter_CSI_generic_short_packet_available : [ISPMMADR] + 8B008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_CSI_generic_short_packet_available:** Unused
0	1h RO	**CSI_generic_short_packet_available:** Returns 1 if there is a generic short packet available. Returns 0 is there is no generic short packet available.

3.7.838 reg_inp_sys_irq_ctrl_irq_edge_type (inp_sys_irq_ctrl_irq_edge)—Offset 8C000h

IRQ active edge select per interrupt input. Rising edge: 1, Falling edge: 0

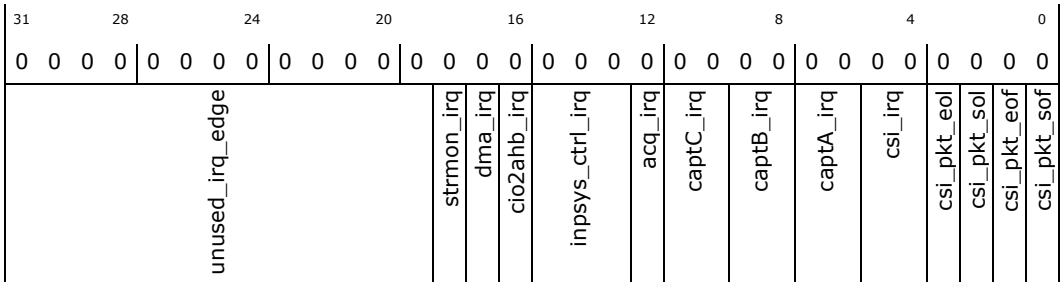
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_irq_ctrl_irq_edge: [ISPMMADR] + 8C000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_edge:** Unused
18	0h RW	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h RW	**acq_irq:** Acquisition unit interrupt request
11:10	0h RW	**captC_irq:** Capture unit C interrupt request
9:8	0h RW	**captB_irq:** Capture unit B interrupt request
7:6	0h RW	**captA_irq:** Capture unit A interrupt request
5:4	0h RW	**csi_irq:** CSI receiver interrupt request
3	0h RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

3.7.839 reg_inp_sys_irq_ctrl_irq_mask_type (inp_sys_irq_ctrl_irq_mask)—Offset 8C004h

IRQ mask per interrupt

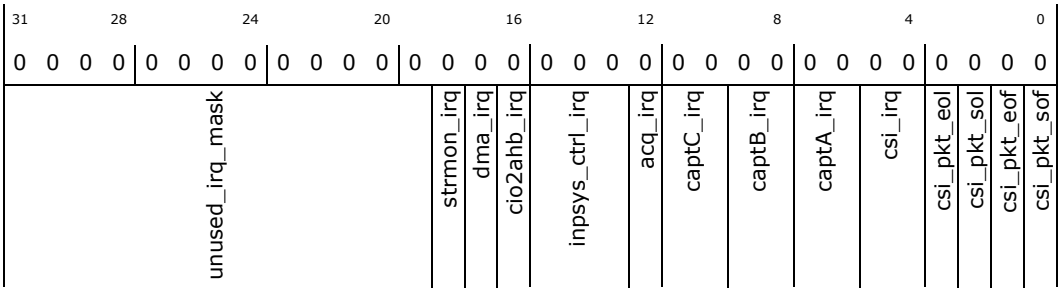
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_irq_ctrl_irq_mask: [ISPMMADR] + 8C004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_mask:** Unused
18	0h RW	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h RW	**acq_irq:** Acquisition unit interrupt request
11:10	0h RW	**captC_irq:** Capture unit C interrupt request
9:8	0h RW	**captB_irq:** Capture unit B interrupt request
7:6	0h RW	**captA_irq:** Capture unit A interrupt request
5:4	0h RW	**csi_irq:** CSI receiver interrupt request
3	0h RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h RW	**csi_pkt_sol:** Start of Line packet from CSI receiver

Bit Range	Default & Access	Description
1	0h RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

3.7.840 reg_inp_sys_irq_ctrl_irq_status_type (inp_sys_irq_ctrl_irq_status)—Offset 8C008h

IRQ status for each unmasked interrupt

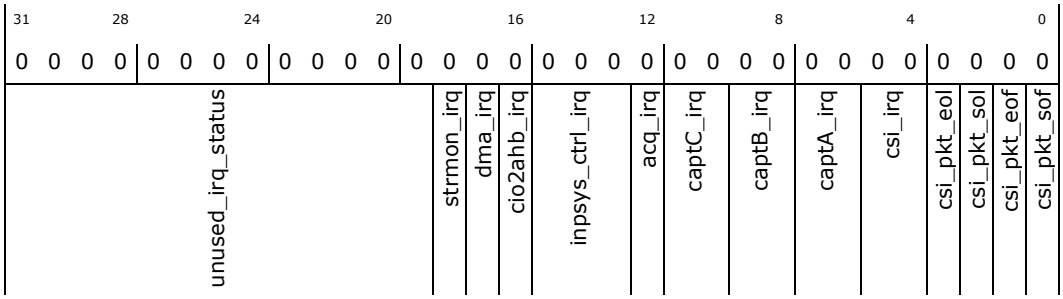
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_irq_ctrl_irq_status: [ISPMMADR] + 8C008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_status:** Unused
18	0h RO	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h RO	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h RO	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h RO	**acq_irq:** Acquisition unit interrupt request
11:10	0h RO	**captC_irq:** Capture unit C interrupt request
9:8	0h RO	**captB_irq:** Capture unit B interrupt request

Bit Range	Default & Access	Description
7:6	0h RO	**captA_irq:** Capture unit A interrupt request
5:4	0h RO	**csi_irq:** CSI receiver interrupt request
3	0h RO	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h RO	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h RO	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h RO	**csi_pkt_sof:** Start of Frame packet from CSI receiver

3.7.841 reg_inp_sys_irq_ctrl_irq_clear_type (inp_sys_irq_ctrl_irq_clear)—Offset 8C00Ch

IRQ clear for interrupt set in irq_status

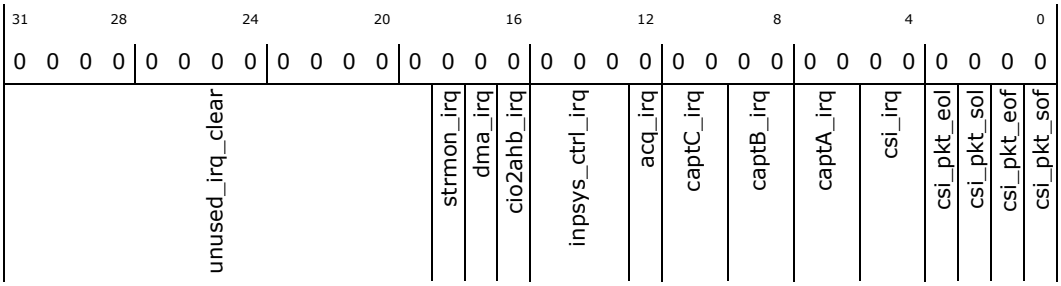
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_irq_ctrl_irq_clear: [ISPMMADR] + 8C00Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_clear:** Unused
18	0h WO	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h WO	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request

Bit Range	Default & Access	Description
15:13	0h WO	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h WO	**acq_irq:** Acquisition unit interrupt request
11:10	0h WO	**captC_irq:** Capture unit C interrupt request
9:8	0h WO	**captB_irq:** Capture unit B interrupt request
7:6	0h WO	**captA_irq:** Capture unit A interrupt request
5:4	0h WO	**csi_irq:** CSI receiver interrupt request
3	0h WO	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h WO	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h WO	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h WO	**csi_pkt_sof:** Start of Frame packet from CSI receiver

3.7.842 reg_inp_sys_irq_ctrl_irq_en_type (inp_sys_irq_ctrl_irq_en)—Offset 8C010h

IRQ enable per interrupt bit

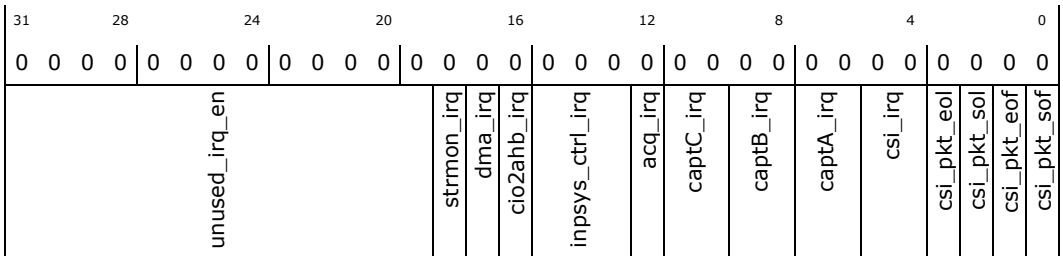
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

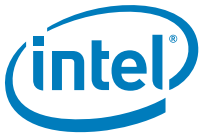
inp_sys_irq_ctrl_irq_en: [ISPMMADR] + 8C010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_en:** Unused



Bit Range	Default & Access	Description
18	0h RW	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h RW	**acq_irq:** Acquisition unit interrupt request
11:10	0h RW	**captC_irq:** Capture unit C interrupt request
9:8	0h RW	**captB_irq:** Capture unit B interrupt request
7:6	0h RW	**captA_irq:** Capture unit A interrupt request
5:4	0h RW	**csi_irq:** CSI receiver interrupt request
3	0h RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

3.7.843 reg_inp_sys_irq_ctrl_irq_level_not_pulse_type (inp_sys_irq_ctrl_irq_level_not_pulse)—Offset 8C014h

IRQ setting per interrupt bit for level or pulse irq generation at output pin. Level: 1, Pulse: 0

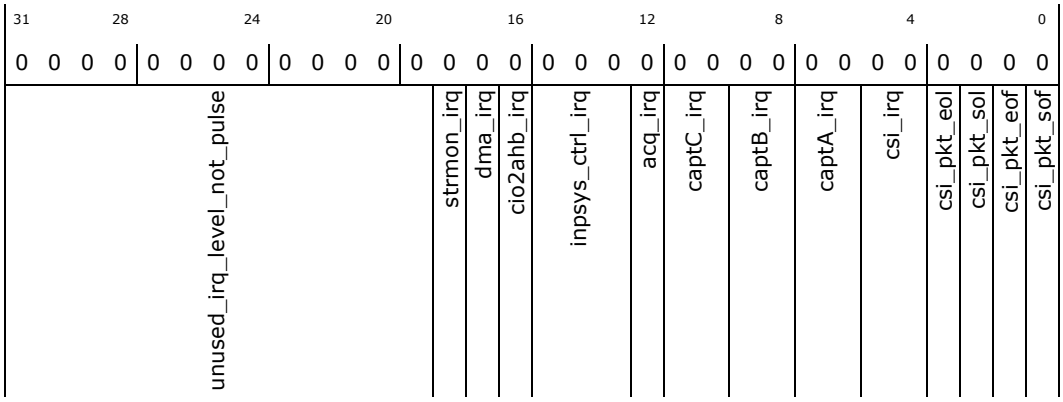
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_irq_ctrl_irq_level_not_pulse: [ISPMMADR] + 8C014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_level_not_pulse:** Unused
18	0h RW	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h RW	**acq_irq:** Acquisition unit interrupt request
11:10	0h RW	**captC_irq:** Capture unit C interrupt request
9:8	0h RW	**captB_irq:** Capture unit B interrupt request
7:6	0h RW	**captA_irq:** Capture unit A interrupt request
5:4	0h RW	**csi_irq:** CSI receiver interrupt request
3	0h RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

3.7.844 reg_isel_gpr_reg_gp_syncgen_enable_type (isel_gpr_reg_gp_syncgen_enable)—Offset 90000h

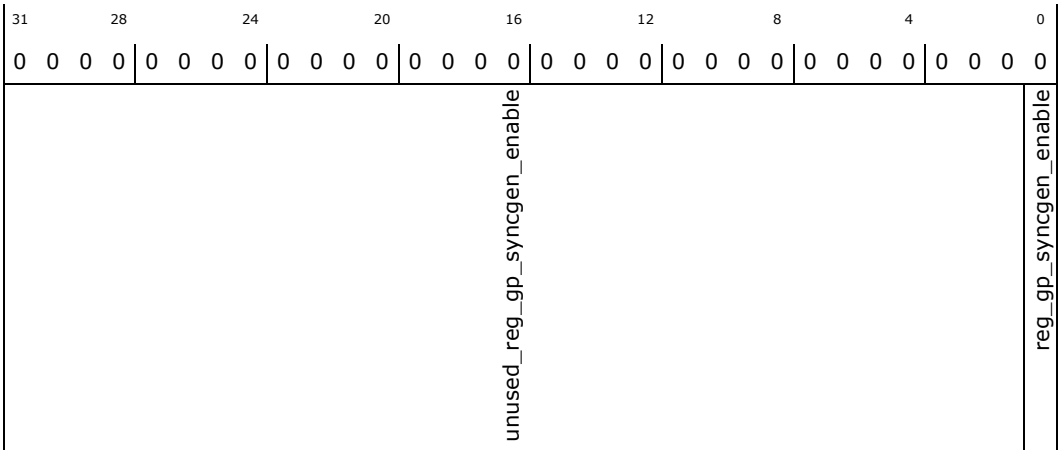
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syncgen_enable: [ISPMMADR] + 90000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_syncgen_enable:** Unused
0	0h RW	**reg_gp_syncgen_enable:** Enables (value=1) or disables (value=0) the Sync Generator.

3.7.845 reg_isel_gpr_reg_gp_syncgen_free_running_type (isel_gpr_reg_gp_syncgen_free_running)—Offset 90004h

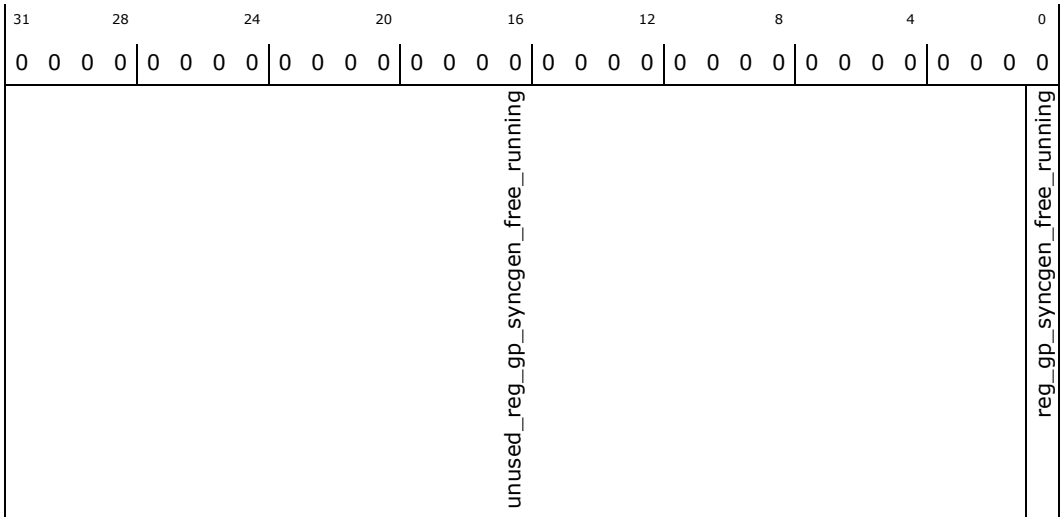
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syncgen_free_running: [ISPMMADR] + 90004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_syncgen_free_running:** Unused
0	0h RW	**reg_gp_syncgen_free_running:** Sets the sync generator in free running mode (value=1) or let it stall in sync with either the PRBS or TPG (value=0)

3.7.846 reg_isel_gpr_reg_gp_syncgen_pause_type (isel_gpr_reg_gp_syncgen_pause)—Offset 90008h

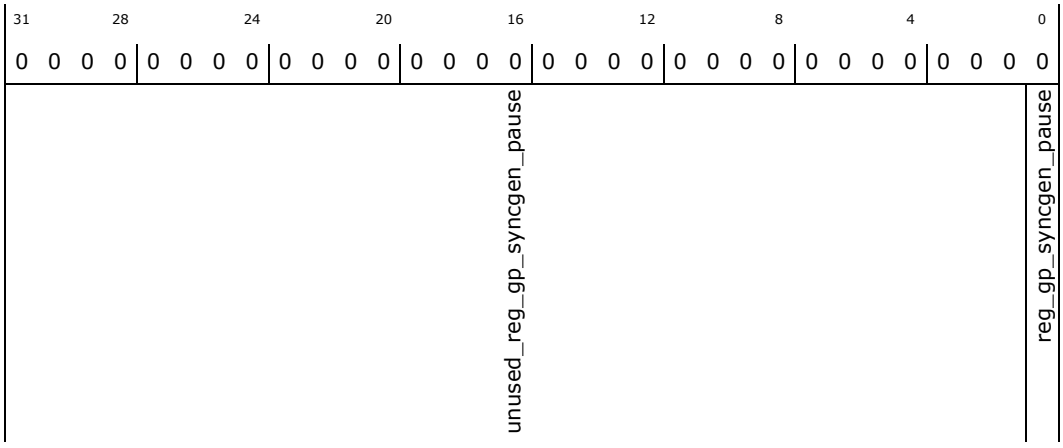
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syncgen_pause: [ISPMMADR] + 90008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_syncgen_pause:** Unused
0	0h RW	**reg_gp_syncgen_pause:** Sets the sync generator in pause mode (value=1) or not (value=0)

3.7.847 reg_isel_gpr_reg_gp_nr_frames_type (isel_gpr_reg_gp_nr_frames)—Offset 9000Ch

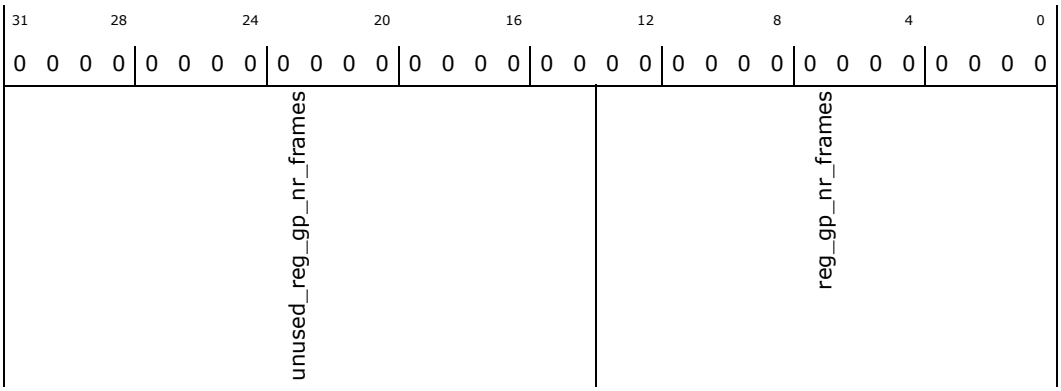
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_nr_frames: [ISPMMADR] + 9000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_nr_frames:** Unused
13:0	0h RW	**reg_gp_nr_frames:** Sets the sync generator parameter Number of Frames

3.7.848 reg_isel_gpr_reg_gp_syngen_nr_pix_type (isel_gpr_reg_gp_syngen_nr_pix)—Offset 90010h

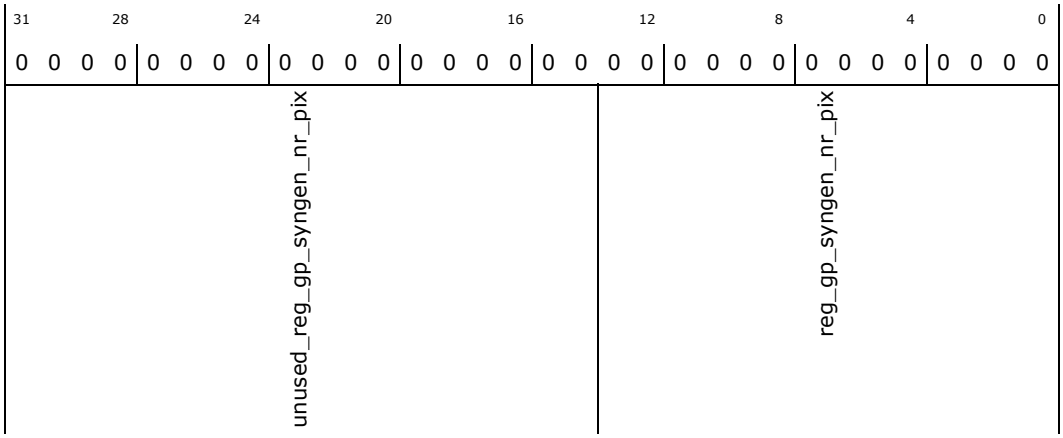
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syngen_nr_pix: [ISPMMADR] + 90010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syngen_nr_pix:** Unused
13:0	0h RW	**reg_gp_syngen_nr_pix:** Sets the number of active pixels per line in the Sync Generator

3.7.849 reg_isel_gpr_reg_gp_syngen_nr_lines_type (isel_gpr_reg_gp_syngen_nr_lines)—Offset 90014h

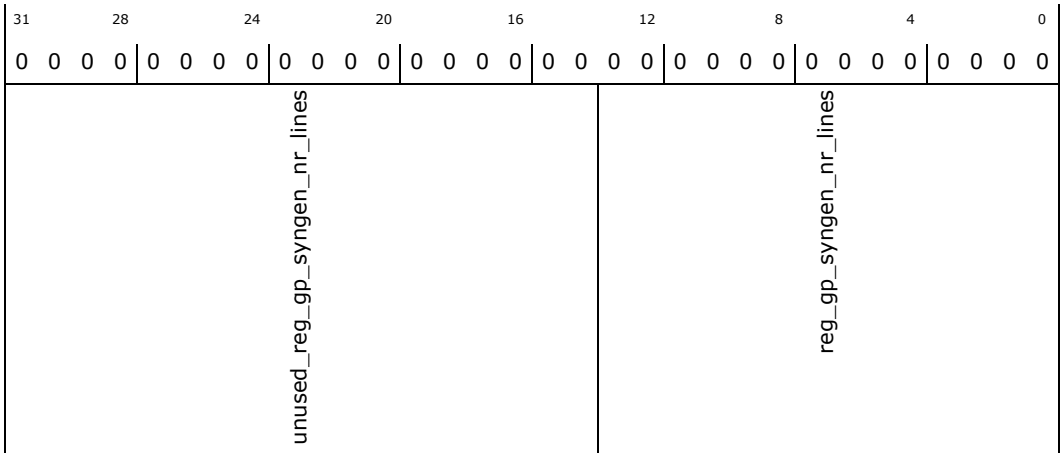
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syngen_nr_lines: [ISPMMADR] + 90014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syngen_nr_lines:** Unused
13:0	0h RW	**reg_gp_syngen_nr_lines:** Sets the number of lines per frame in the Sync generator

3.7.850 reg_isel_gpr_reg_gp_syngen_hblank_cycles_type (isel_gpr_reg_gp_syngen_hblank_cycles)—Offset 90018h

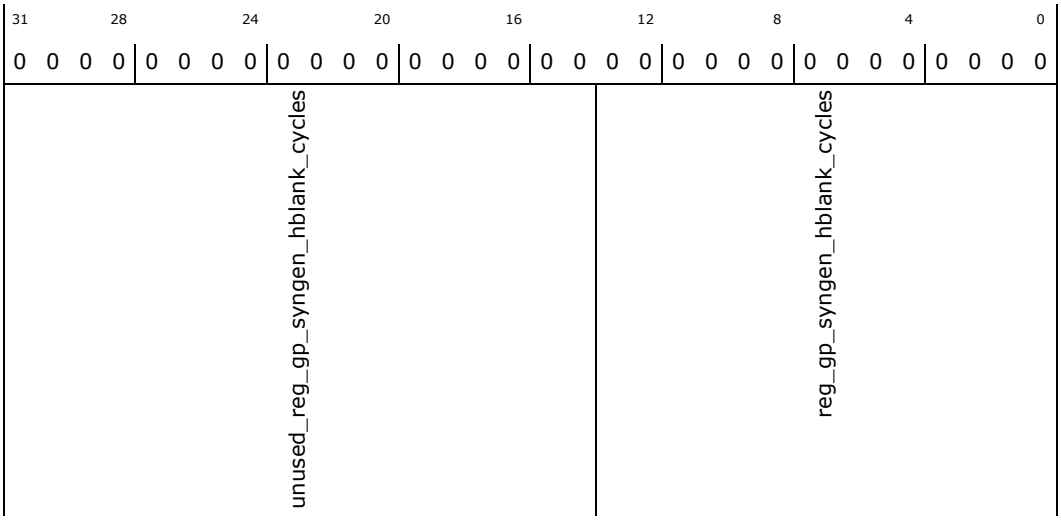
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syngen_hblank_cycles: [ISPMMADR] + 90018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syngen_hblank_cycles:** Unused
13:0	0h RW	**reg_gp_syngen_hblank_cycles:** Sets the number of cycles between the end-of-line and start-of-line pulses.

3.7.851 reg_isel_gpr_reg_gp_syngen_vblank_cycles_type (isel_gpr_reg_gp_syngen_vblank_cycles)—Offset 9001Ch

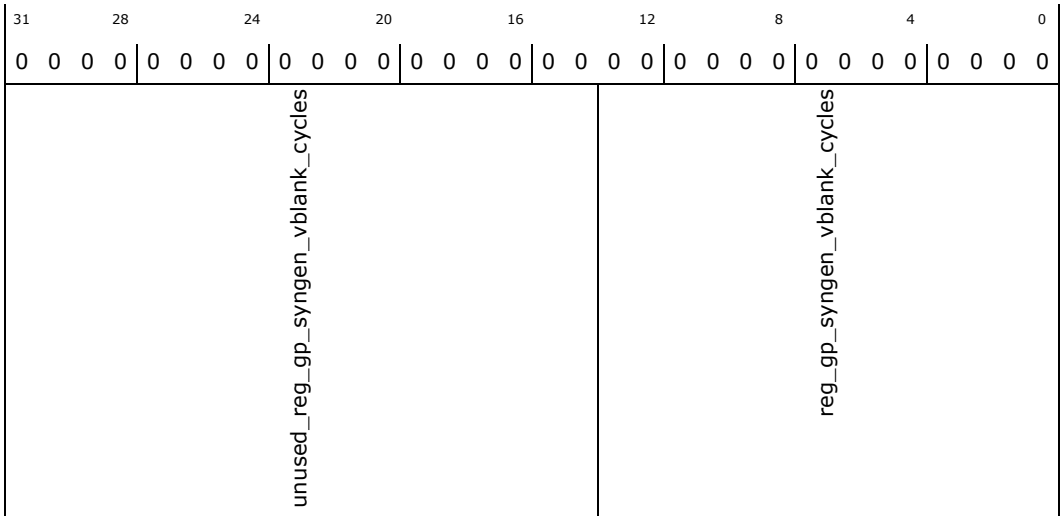
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syngen_vblank_cycles: [ISPMMADR] + 9001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syngen_vblank_cycles:** Unused
13:0	0h RW	**reg_gp_syngen_vblank_cycles:** Sets the number of cycles between the end-of-frame and start-of-frame pulses.

3.7.852 reg_isel_gpr_reg_gp_isel_sof_type (isel_gpr_reg_gp_isel_sof)—Offset 90020h

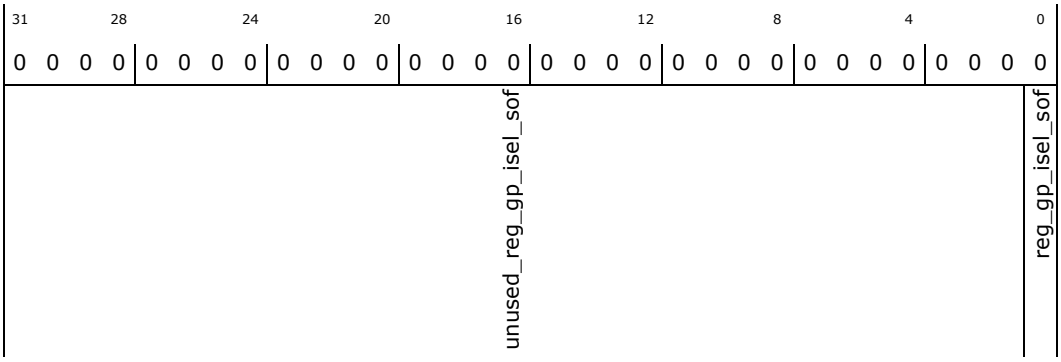
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_sof: [ISPMMADR] + 90020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_sof:** Unused
0	0h RW	**reg_gp_isel_sof:** Sets the input selector gp_sof input.

3.7.853 reg_isel_gpr_reg_gp_isel_eof_type (isel_gpr_reg_gp_isel_eof)—Offset 90024h

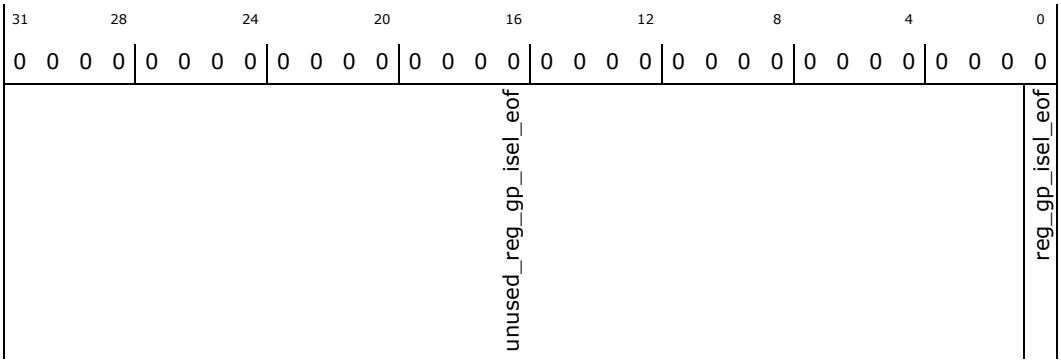
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_eof: [ISPMMADR] + 90024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_eof:** Unused
0	0h RW	**reg_gp_isel_eof:** Sets the input selector gp_eof input.

3.7.854 reg_isel_gpr_reg_gp_isel_sol_type (isel_gpr_reg_gp_isel_sol)—Offset 90028h

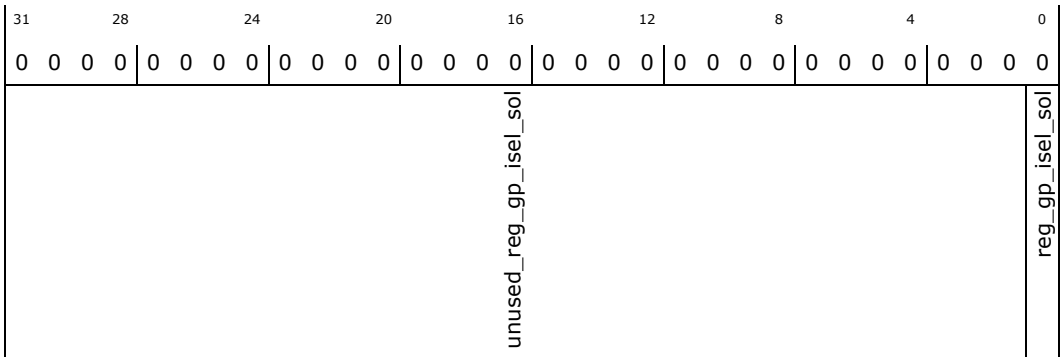
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_sol: [ISPMMADR] + 90028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_sol:** Unused
0	0h RW	**reg_gp_isel_sol:** Sets the input selector gp_sol input.

3.7.855 reg_isel_gpr_reg_gp_isel_eol_type (isel_gpr_reg_gp_isel_eol)—Offset 9002Ch

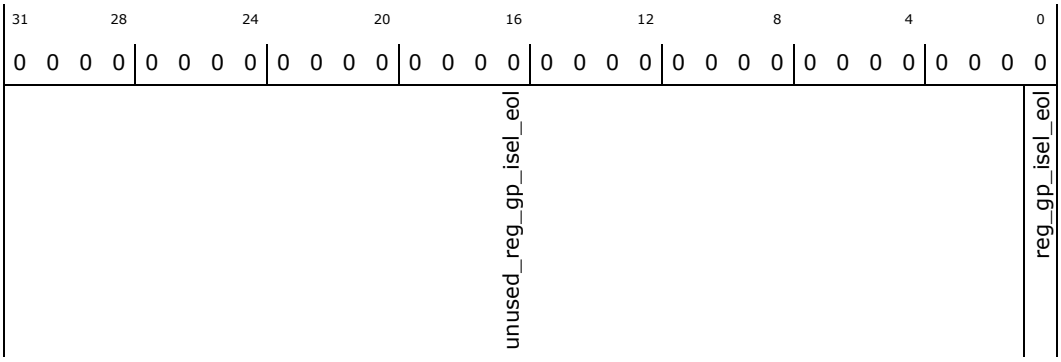
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_eol: [ISPMMADR] + 9002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_eol:** Unused
0	0h RW	**reg_gp_isel_eol:** Sets the input selector gp_eol input.

3.7.856 reg_isel_gpr_reg_gp_isel_lfsr_enable_type (isel_gpr_reg_gp_isel_lfsr_enable)—Offset 90030h

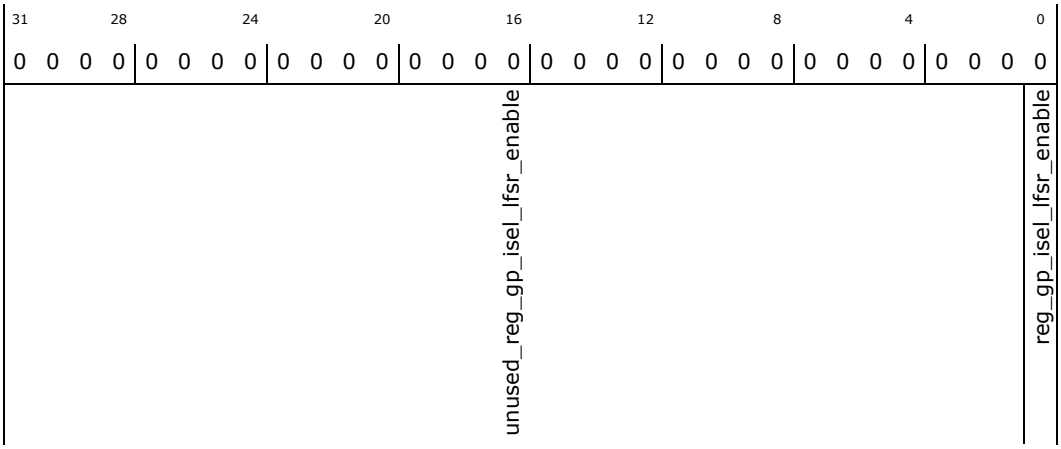
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_lfsr_enable: [ISPMMADR] + 90030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_lfsr_enable:** Unused

Bit Range	Default & Access	Description
0	0h RW	**reg_gp_isel_lfsr_enable:** Enables the PRBS

3.7.857 reg_isel_gpr_reg_gp_isel_lfsr_enable_b_type (isel_gpr_reg_gp_isel_lfsr_enable_b)—Offset 90034h

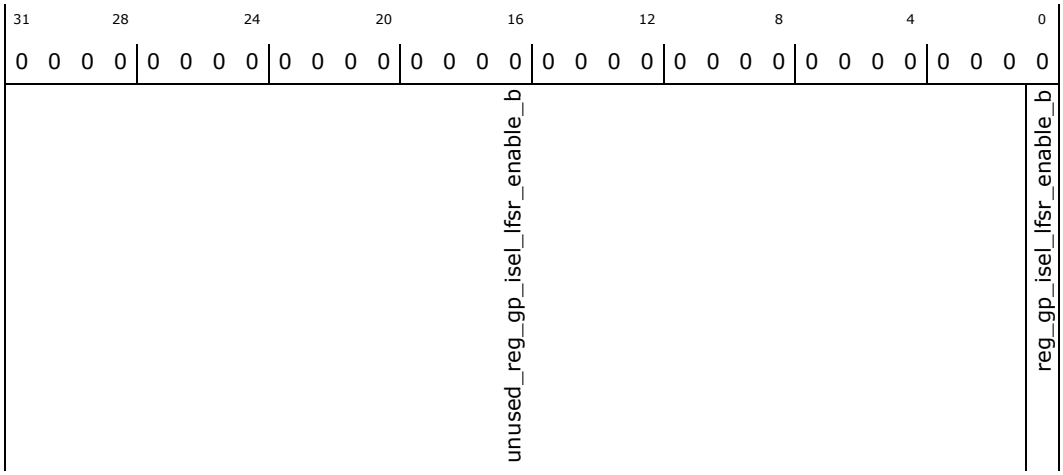
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_lfsr_enable_b: [ISPMMADR] + 90034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_lfsr_enable_b:** Unused
0	0h RW	**reg_gp_isel_lfsr_enable_b:** Enables the PRBS for port b

3.7.858 reg_isel_gpr_reg_gp_isel_lfsr_reset_value_type (isel_gpr_reg_gp_isel_lfsr_reset_value)—Offset 90038h

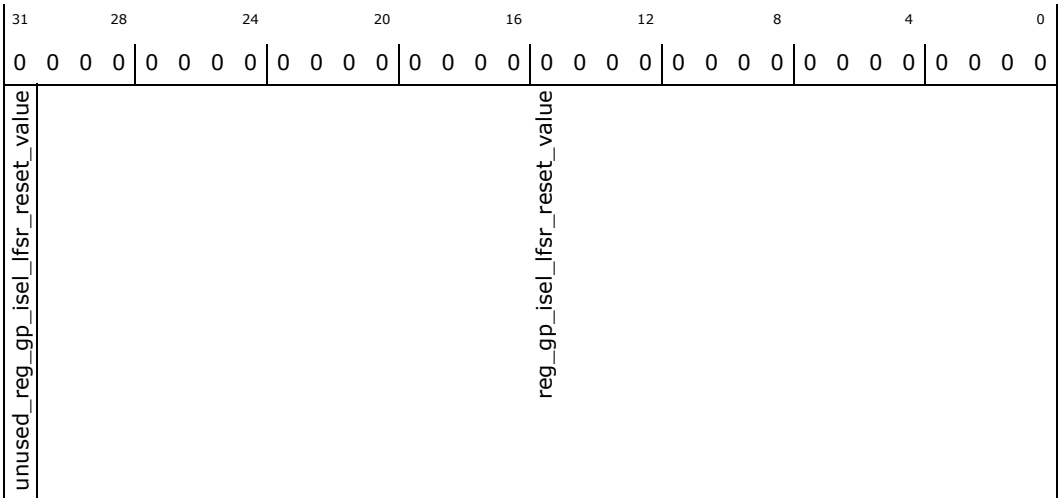
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_lfsr_reset_value: [ISPMMADR] + 90038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**unused_reg_gp_isel_lfsr_reset_value:** Unused
30:0	0h RW	**reg_gp_isel_lfsr_reset_value:** Set the reset value of the LFSR in the PRBS of the Input selector

3.7.859 reg_isel_gpr_reg_gp_isel_tpg_enable_type (isel_gpr_reg_gp_isel_tpg_enable)—Offset 9003Ch

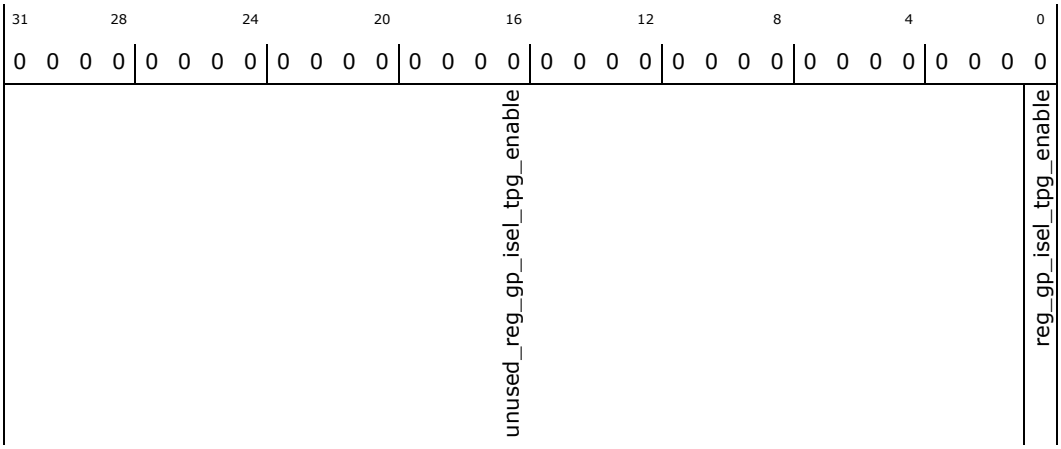
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_enable: [ISPMMADR] + 9003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_tpg_enable:** Unused
0	0h RW	**reg_gp_isel_tpg_enable:** Enables the test pattern generator

3.7.860 reg_isel_gpr_reg_gp_isel_tpg_enable_b_type (isel_gpr_reg_gp_isel_tpg_enable_b)—Offset 90040h

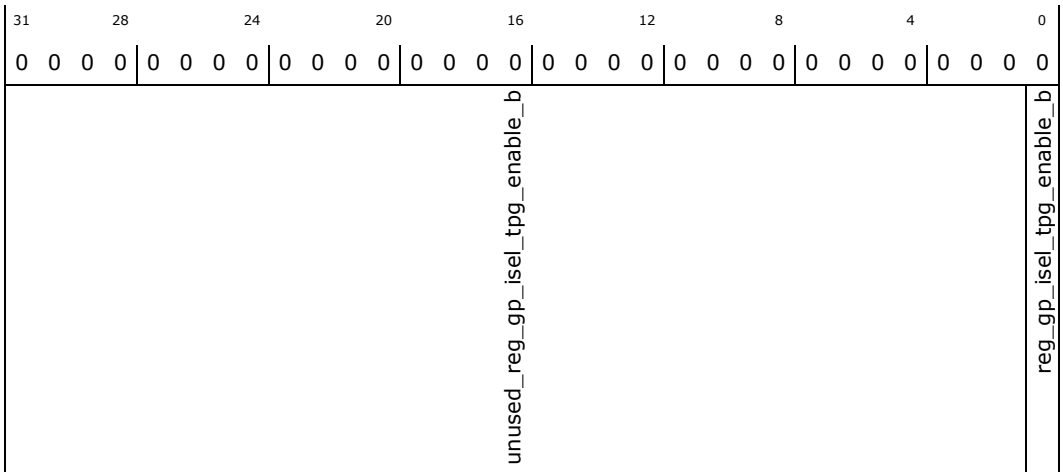
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_enable_b: [ISPMMADR] + 90040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_tpg_enable_b:** Unused
0	0h RW	**reg_gp_isel_tpg_enable_b:** Enables the test pattern generator for port b

3.7.861 reg_isel_gpr_reg_gp_isel_hor_cnt_mask_type (isel_gpr_reg_gp_isel_hor_cnt_mask)—Offset 90044h

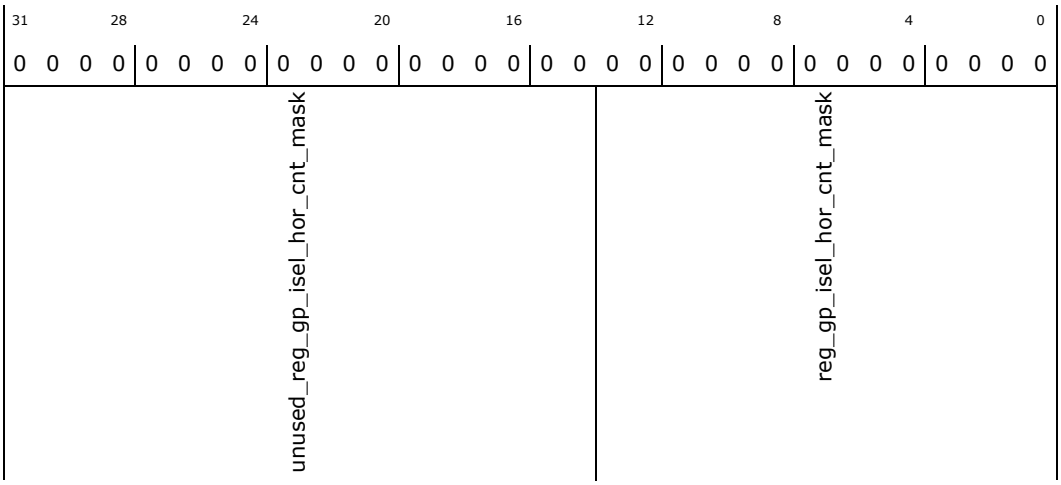
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_hor_cnt_mask: [ISPMMADR] + 90044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_isel_hor_cnt_mask:** Unused
13:0	0h RW	**reg_gp_isel_hor_cnt_mask:** Sets the horizontal counter mask in the Input selector

3.7.862 reg_isel_gpr_reg_gp_isel_ver_cnt_mask_type (isel_gpr_reg_gp_isel_ver_cnt_mask)—Offset 90048h

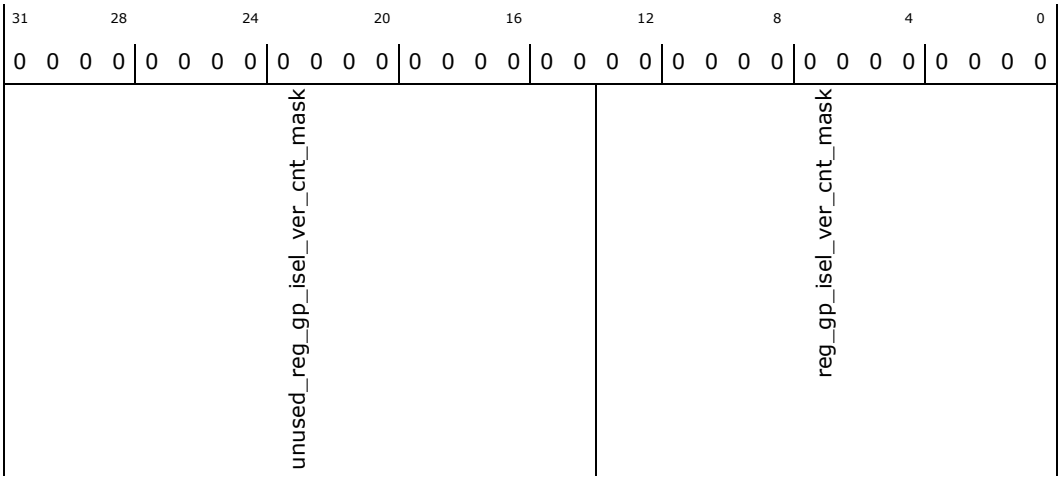
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_ver_cnt_mask: [ISPMMADR] + 90048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_isel_ver_cnt_mask:** Unused
13:0	0h RW	**reg_gp_isel_ver_cnt_mask:** Sets the vertical counter mask in the Input selector

3.7.863 reg_isel_gpr_reg_gp_isel_xy_cnt_mask_type (isel_gpr_reg_gp_isel_xy_cnt_mask)—Offset 9004Ch

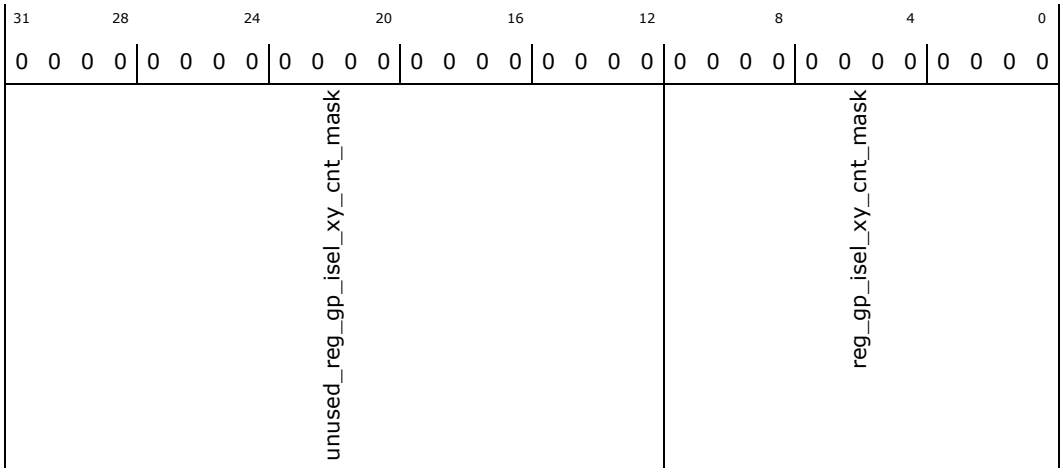
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_xy_cnt_mask: [ISPMMADR] + 9004Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_xy_cnt_mask:** Unused
11:0	0h RW	**reg_gp_isel_xy_cnt_mask:** Sets the xy counter mask in the Input selector

3.7.864 reg_isel_gpr_reg_gp_isel_hor_cnt_delta_type (isel_gpr_reg_gp_isel_hor_cnt_delta)—Offset 90050h

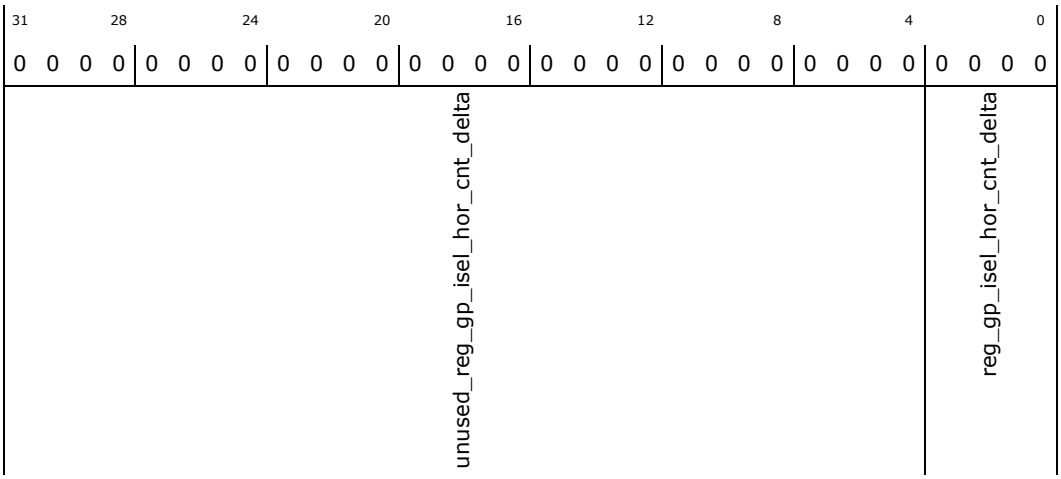
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_hor_cnt_delta: [ISPMMADR] + 90050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_gp_isel_hor_cnt_delta:** Unused
3:0	0h RW	**reg_gp_isel_hor_cnt_delta:** sets the horizontal counter delta in the Input selector

3.7.865 reg_isel_gpr_reg_gp_isel_ver_cnt_delta_type (isel_gpr_reg_gp_isel_ver_cnt_delta)—Offset 90054h

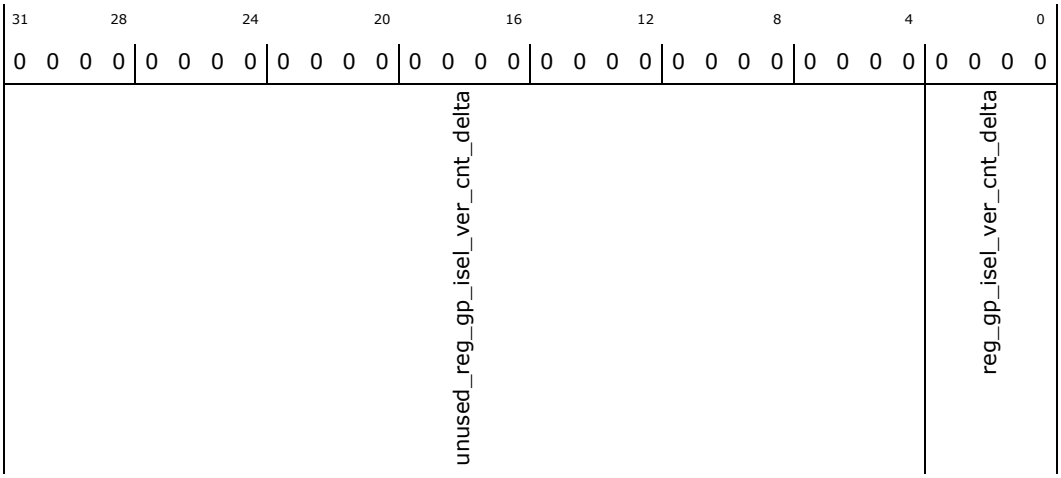
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_ver_cnt_delta: [ISPMMADR] + 90054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_gp_isel_ver_cnt_delta:** Unused
3:0	0h RW	**reg_gp_isel_ver_cnt_delta:** Sets the vertical counter delta in the Input selector

3.7.866 reg_isel_gpr_reg_gp_isel_tpg_mode_type (isel_gpr_reg_gp_isel_tpg_mode)—Offset 90058h

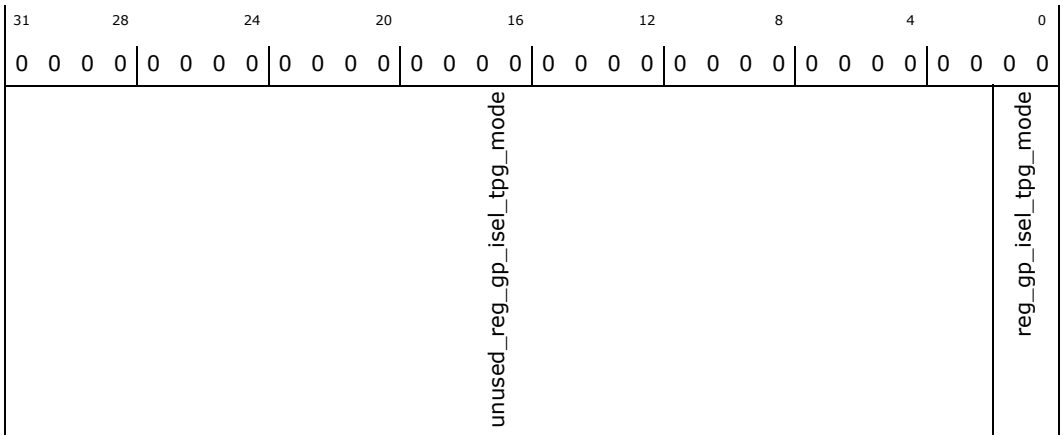
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_mode: [ISPMMADR] + 90058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_reg_gp_isel_tpg_mode:** Unused
1:0	0h RW	**reg_gp_isel_tpg_mode:** Sets the mode of the test pattern generator. 'b00-ramp mode, 'b01-checkerboard, 'b10-frame based color

3.7.867 reg_isel_gpr_reg_gp_isel_tpg_red1_type (isel_gpr_reg_gp_isel_tpg_red1)—Offset 9005Ch

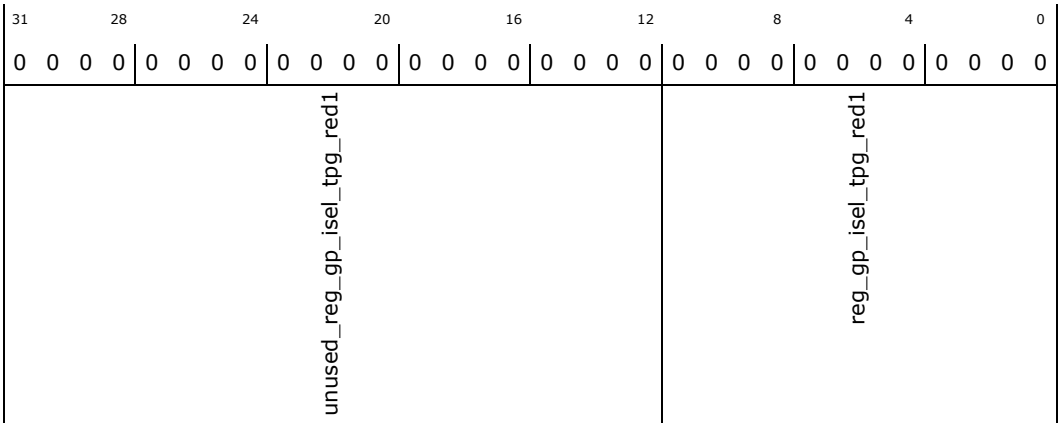
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_red1: [ISPMMADR] + 9005Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_red1:** Unused
11:0	0h RW	**reg_gp_isel_tpg_red1:** Defines the red1 color for test pattern generator

3.7.868 reg_isel_gpr_reg_gp_isel_tpg_green1_type (isel_gpr_reg_gp_isel_tpg_green1)—Offset 90060h

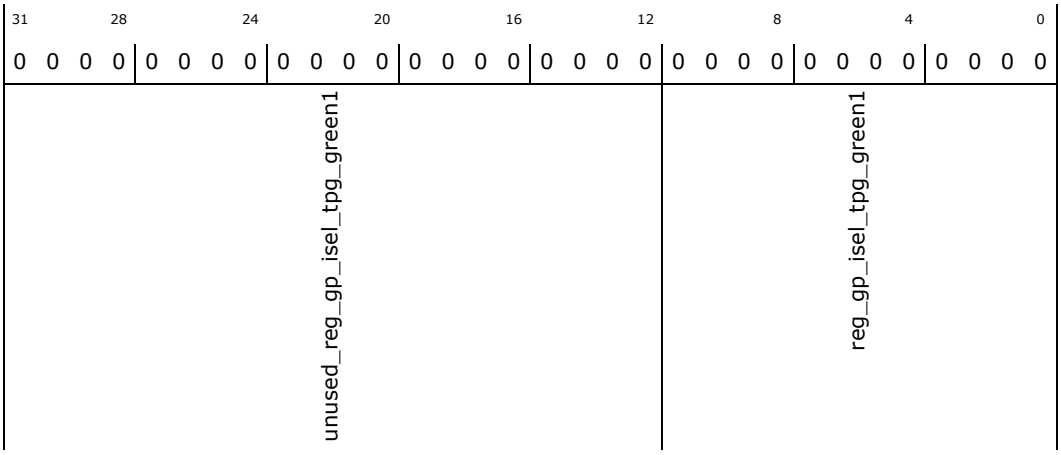
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_green1: [ISPMMADR] + 90060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_green1:** Unused
11:0	0h RW	**reg_gp_isel_tpg_green1:** Defines the green1 color for test pattern generator

3.7.869 reg_isel_gpr_reg_gp_isel_tpg_blue1_type (isel_gpr_reg_gp_isel_tpg_blue1)—Offset 90064h

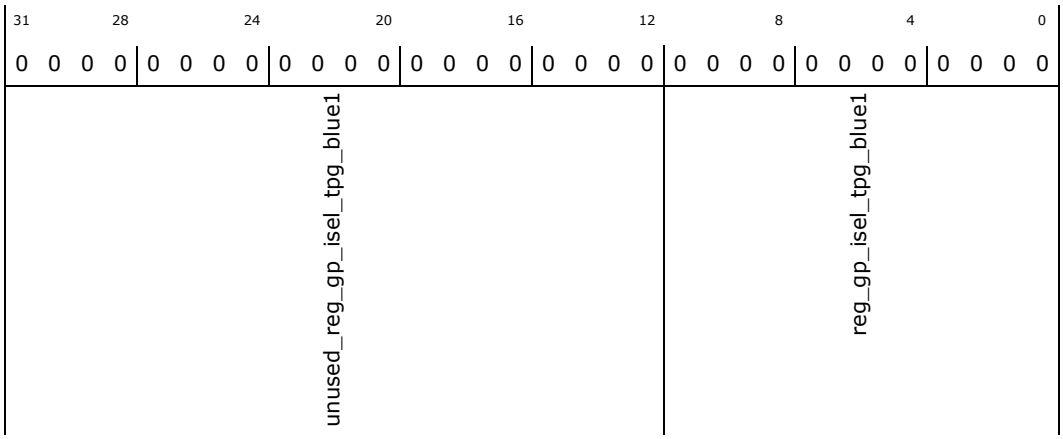
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_blue1: [ISPMMADR] + 90064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_blue1:** Unused
11:0	0h RW	**reg_gp_isel_tpg_blue1:** Defines the blue1 color for test pattern generator

3.7.870 reg_isel_gpr_reg_gp_isel_tpg_red2_type (isel_gpr_reg_gp_isel_tpg_red2)—Offset 90068h

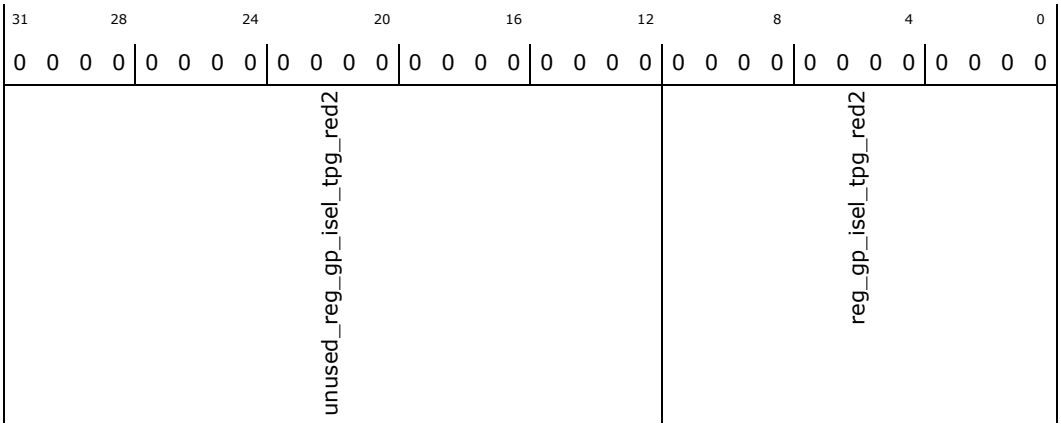
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_red2: [ISPMMADR] + 90068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_red2:** Unused
11:0	0h RW	**reg_gp_isel_tpg_red2:** Defines the red2 color for test pattern generator

3.7.871 reg_isel_gpr_reg_gp_isel_tpg_green2_type (isel_gpr_reg_gp_isel_tpg_green2)—Offset 9006Ch

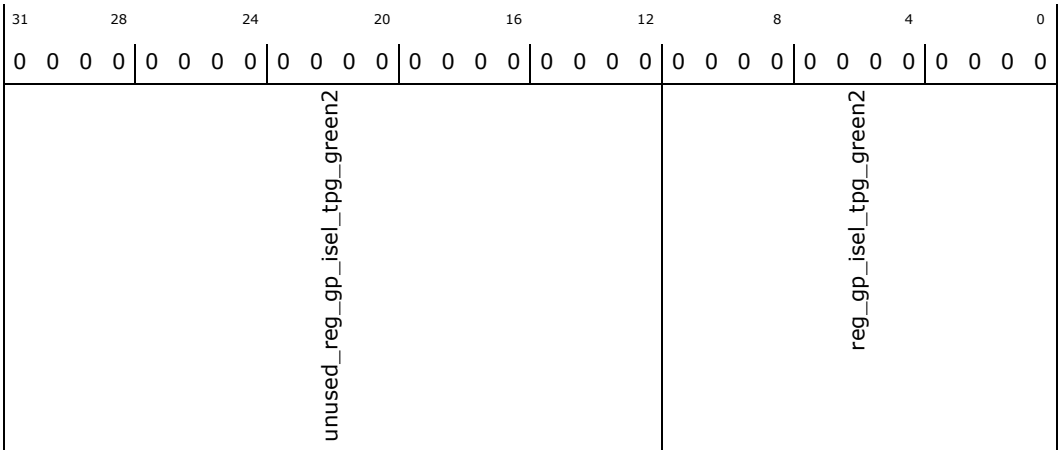
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_green2: [ISPMMADR] + 9006Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_green2:** Unused
11:0	0h RW	**reg_gp_isel_tpg_green2:** Defines the green2 color for test pattern generator

3.7.872 reg_isel_gpr_reg_gp_isel_tpg_blue2_type (isel_gpr_reg_gp_isel_tpg_blue2)—Offset 90070h

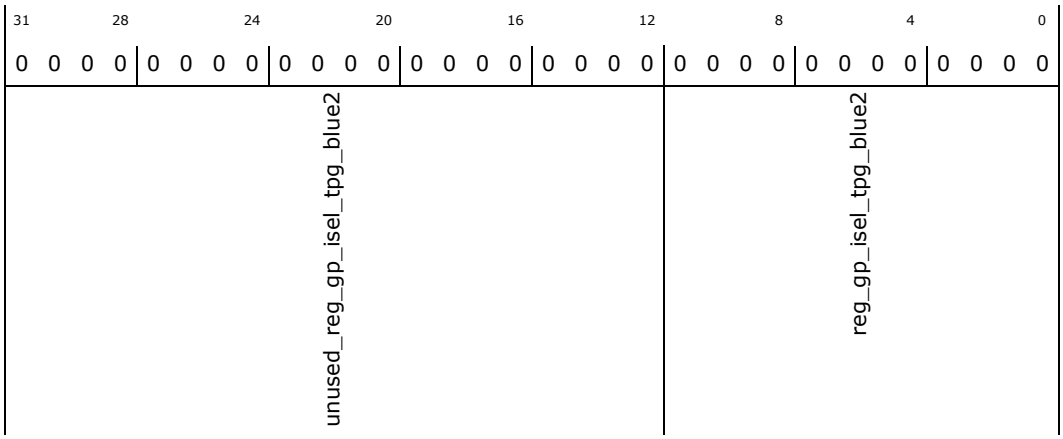
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_blue2: [ISPMMADR] + 90070h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_blue2:** Unused
11:0	0h RW	**reg_gp_isel_tpg_blue2:** Defines the blue2 color for test pattern generator

3.7.873 reg_isel_gpr_reg_gp_isel_ch_id_type (isel_gpr_reg_gp_isel_ch_id)—Offset 90074h

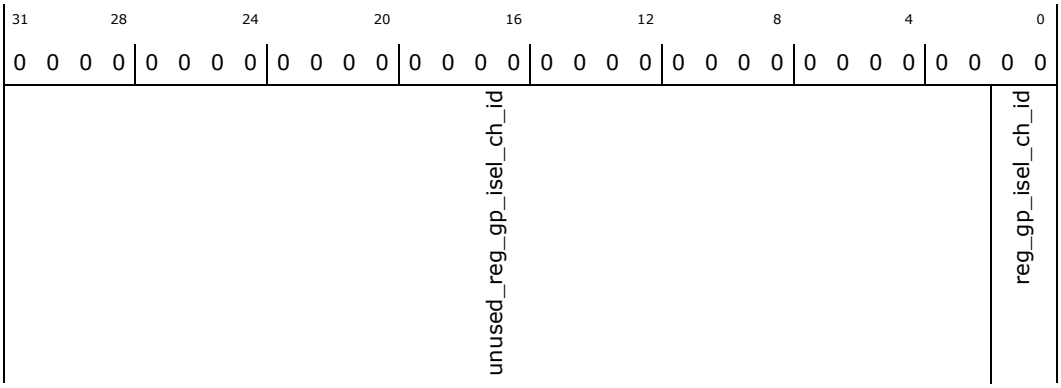
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_ch_id: [ISPMMADR] + 90074h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_reg_gp_isel_ch_id:** Unused
1:0	0h RW	**reg_gp_isel_ch_id:** Sets the channel id input for the Input selector

3.7.874 reg_isel_gpr_reg_gp_isel_fmt_type_type (isel_gpr_reg_gp_isel_fmt_type)—Offset 90078h

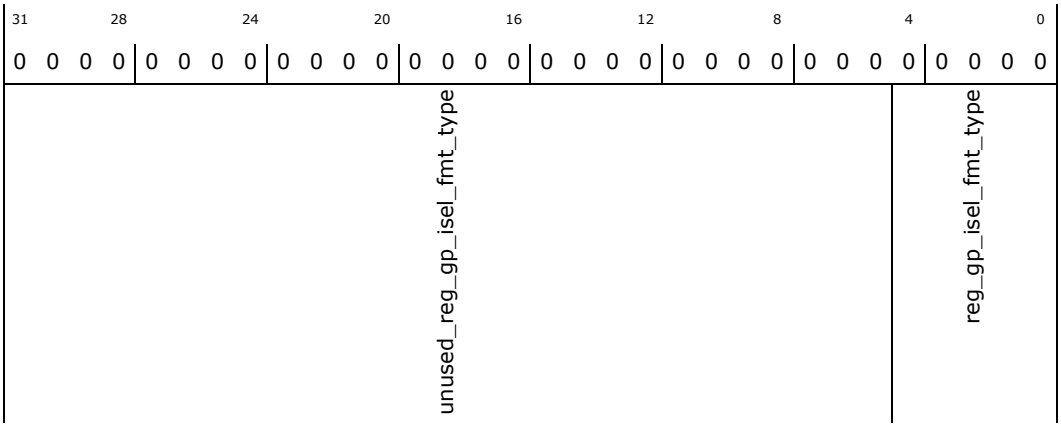
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_fmt_type: [ISPMMADR] + 90078h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**unused_reg_gp_isel_fmt_type:** Unused

Bit Range	Default & Access	Description
4:0	0h RW	**reg_gp_isel_fmt_type:** Sets the format type input for the Input selector

3.7.875 reg_isel_gpr_reg_gp_isel_data_sel_type (isel_gpr_reg_gp_isel_data_sel)—Offset 9007Ch

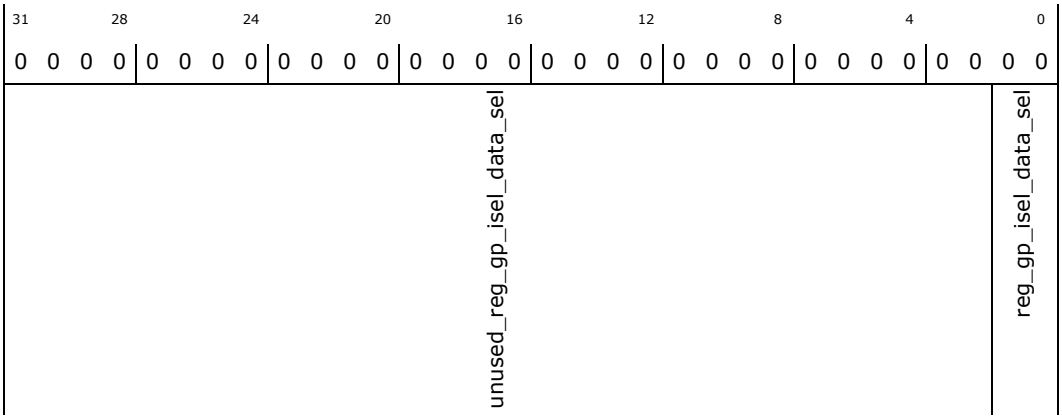
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_data_sel: [ISPMMADR] + 9007Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_reg_gp_isel_data_sel:** Unused
1:0	0h RW	**reg_gp_isel_data_sel:** Select value for the data multiplexer in the Input selector

3.7.876 reg_isel_gpr_reg_gp_isel_sband_sel_type (isel_gpr_reg_gp_isel_sband_sel)—Offset 90080h

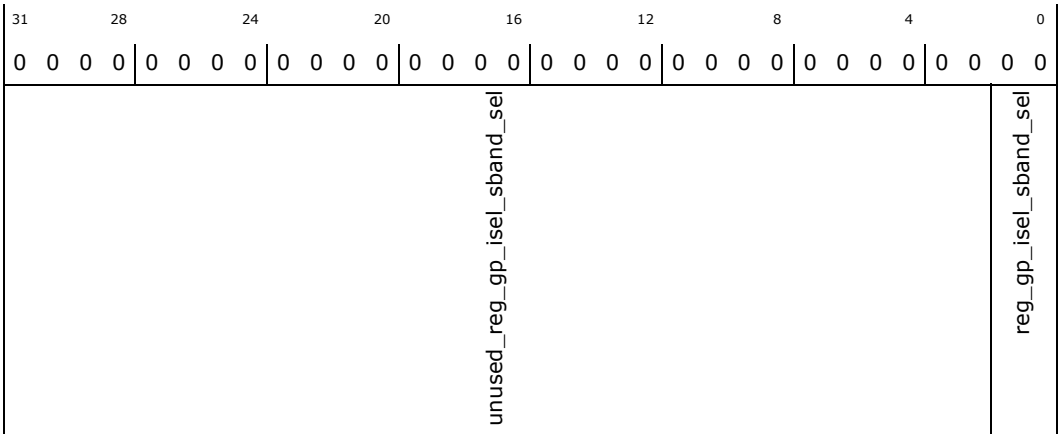
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_sband_sel: [ISPMMADR] + 90080h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_reg_gp_isel_sband_sel:** Unused
1:0	0h RW	**reg_gp_isel_sband_sel:** Select value for the side band multiplexer in the Input selector

3.7.877 reg_isel_gpr_reg_gp_isel_sync_sel_type (isel_gpr_reg_gp_isel_sync_sel)—Offset 90084h

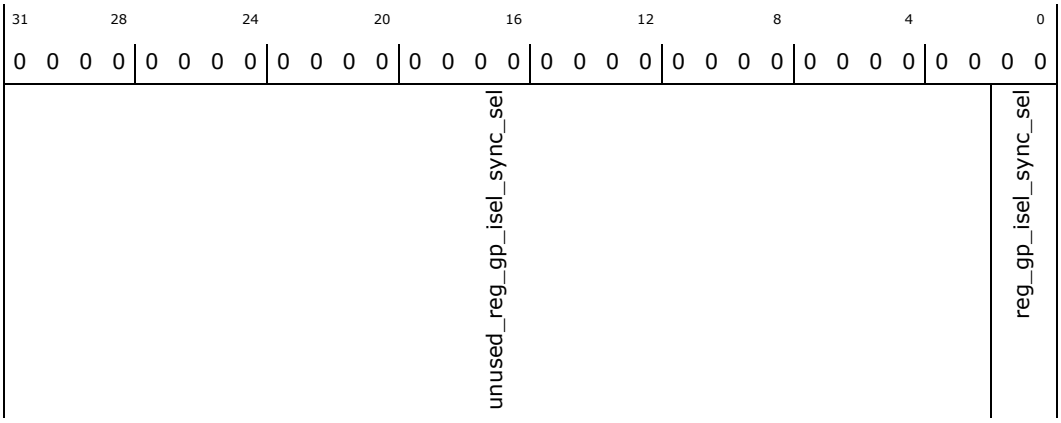
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_sync_sel: [ISPMMADR] + 90084h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**unused_reg_gp_isel_sync_sel:** Unused
1:0	0h RW	**reg_gp_isel_sync_sel:** Select value for the sync multiplexer in the Input selector

3.7.878 reg_isel_gpr_reg_gp_syncgen_hor_cnt_type (isel_gpr_reg_gp_syncgen_hor_cnt)—Offset 90088h

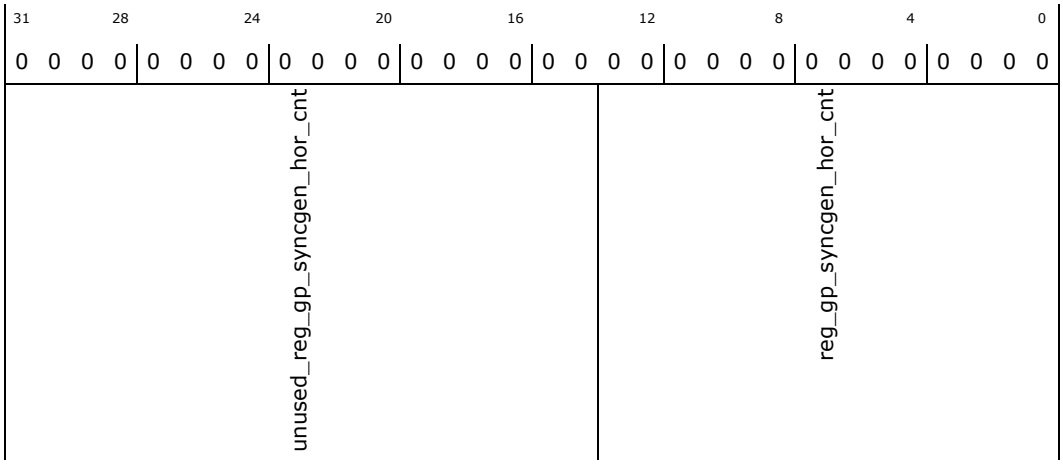
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syncgen_hor_cnt: [ISPMMADR] + 90088h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syncgen_hor_cnt:** Unused
13:0	0h RO	**reg_gp_syncgen_hor_cnt:** Returns the value of the horizontal counter in the sync generator

3.7.879 reg_isel_gpr_reg_gp_syncgen_ver_cnt_type (isel_gpr_reg_gp_syncgen_ver_cnt)—Offset 9008Ch

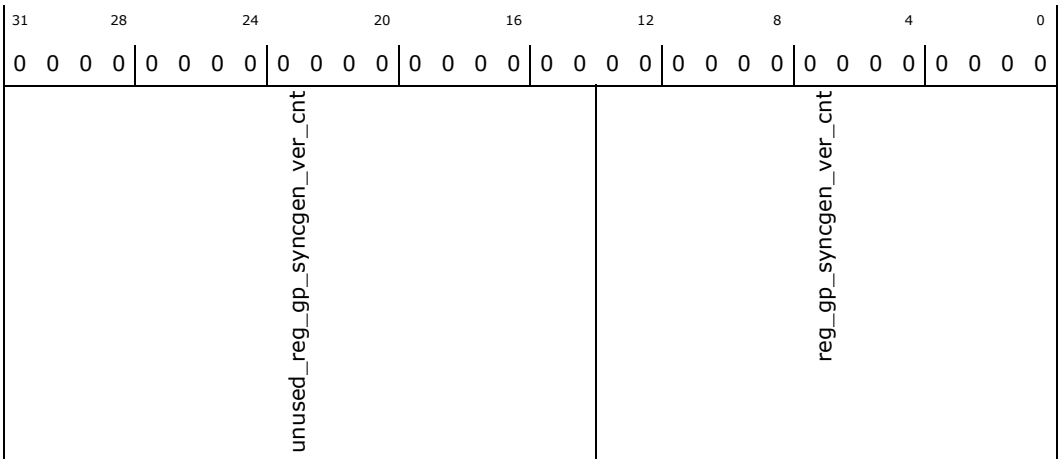
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syncgen_ver_cnt: [ISPMMADR] + 9008Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syncgen_ver_cnt:** Unused
13:0	0h RO	**reg_gp_syncgen_ver_cnt:** Returns the value of the vertical counter in the sync generator

3.7.880 reg_isel_gpr_reg_gp_syncgen_frame_cnt_type (isel_gpr_reg_gp_syncgen_frame_cnt)—Offset 90090h

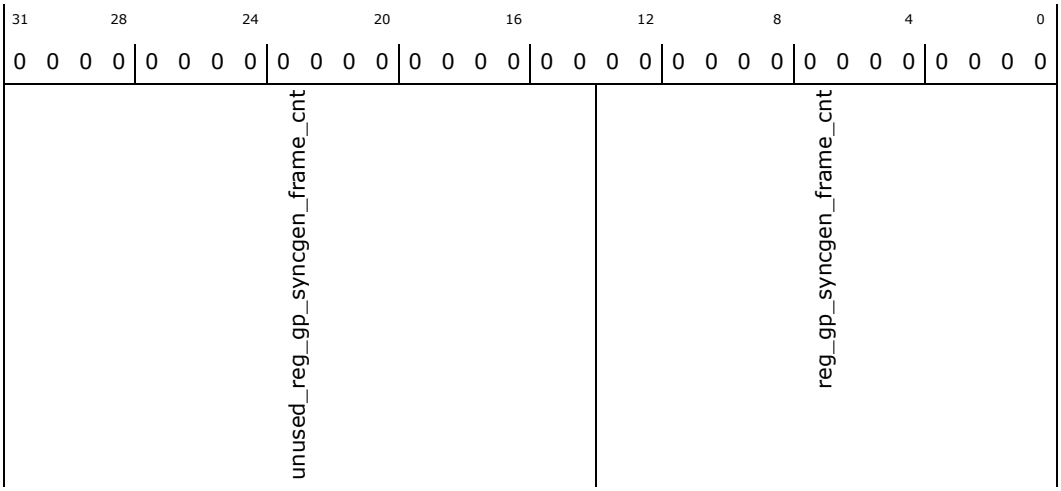
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syncgen_frame_cnt: [ISPMMADR] + 90090h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syncgen_frame_cnt:** Unused
13:0	0h RO	**reg_gp_syncgen_frame_cnt:** Returns the value of the frame counter in the sync generator

3.7.881 reg_isel_gpr_reg_gp_soft_reset_type (isel_gpr_reg_gp_soft_reset)—Offset 90094h

Soft resets the modules in the input selector cluster

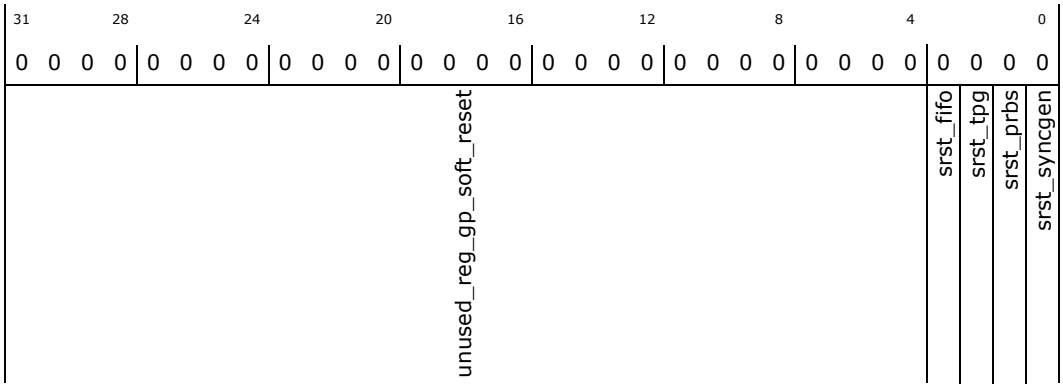
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_soft_reset: [ISPMMADR] + 90094h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_gp_soft_reset:** Unused
3	0h RW	**srst_fifo:** If 1, the fifo is held in reset mode. If 0, the fifo is not in reset state.
2	0h RW	**srst_tpg:** If 1, the TPG is held in reset mode. If 0, the TPG is not in reset state.
1	0h RW	**srst_prbs:** If 1, the PRBS is held in reset mode. If 0, the PRBS is not in reset state.
0	0h RW	**srst_syncgen:** If 1, the sync generator is held in reset mode. If 0, the sync generator is not in reset state.

3.7.882 reg_isel_fa_send_to_GP_FIFO_type (isel_fa_send_to_GP_FIFO)—Offset 90100h

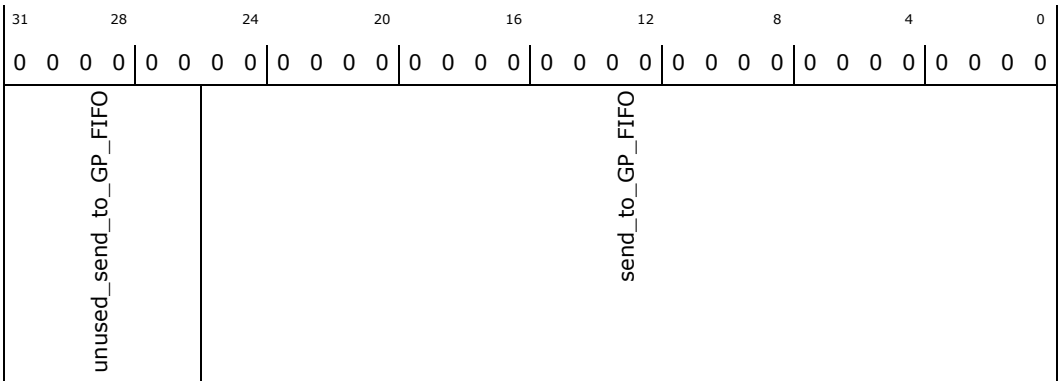
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_fa_send_to_GP_FIFO: [ISPMMADR] + 90100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0h RW	**unused_send_to_GP_FIFO:** Unused
25:0	0h WO	**send_to_GP_FIFO:** Send data to input selector GP FIFO

3.7.883 reg_isel_fa_check_send_to_GP_FIFO_type (isel_fa_check_send_to_GP_FIFO)—Offset 90108h

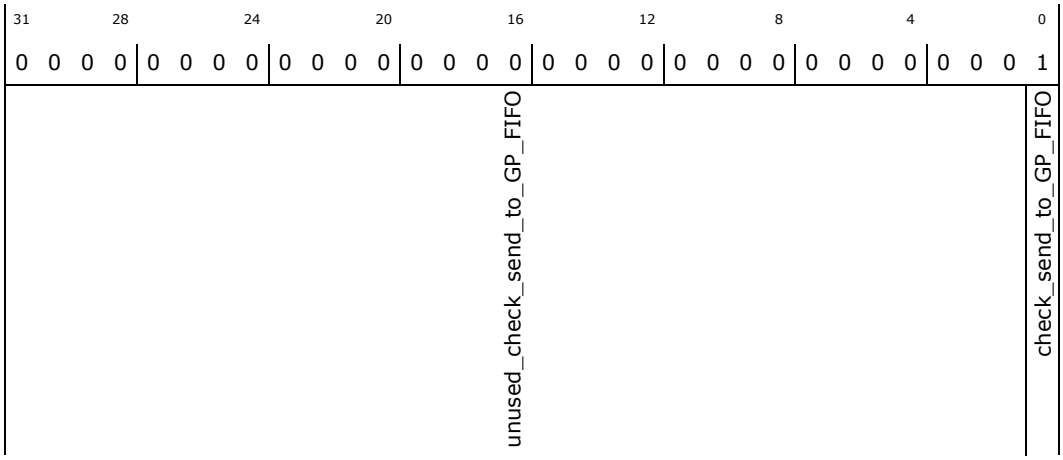
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_fa_check_send_to_GP_FIFO: [ISPMMADR] + 90108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_check_send_to_GP_FIFO:** Unused
0	1h WO	**check_send_to_GP_FIFO:** Check for availability of GP FIFO. Returns 1 if a word can be send to the input selector, without it being stalled

3.7.884 reg_isel_irq_ctrl_reg_irq_edge_type (isel_irq_ctrl_reg_irq_edge)—Offset 90200h

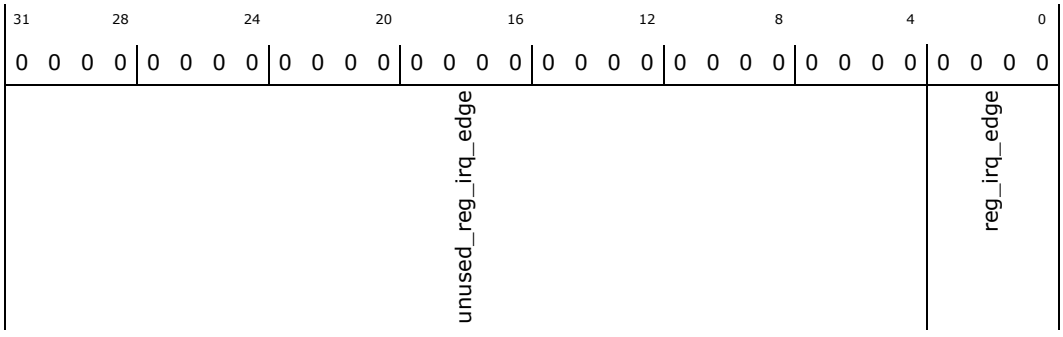
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_irq_ctrl_reg_irq_edge: [ISPMMADR] + 90200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_edge:** Unused

Bit Range	Default & Access	Description
3:0	0h RW	**reg_irq_edge:** indicates for each bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

3.7.885 reg_isel_irq_ctrl_reg_irq_mask_type (isel_irq_ctrl_reg_irq_mask)—Offset 90204h

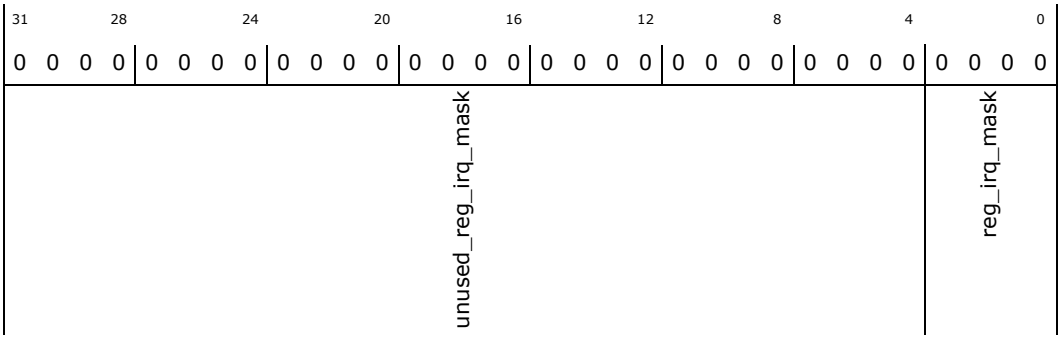
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_irq_ctrl_reg_irq_mask: [ISPMMADR] + 90204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_mask:** Unused
3:0	0h RW	**reg_irq_mask:** indicates for each bit of irq_di whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

3.7.886 reg_isel_irq_ctrl_reg_irq_status_type (isel_irq_ctrl_reg_irq_status)—Offset 90208h

Indicates for each bit whether a non-masked interrupt has been generated (value='1'). Can be cleared by writing a '1' into the the corresponding bit of the req_irq_clear register.

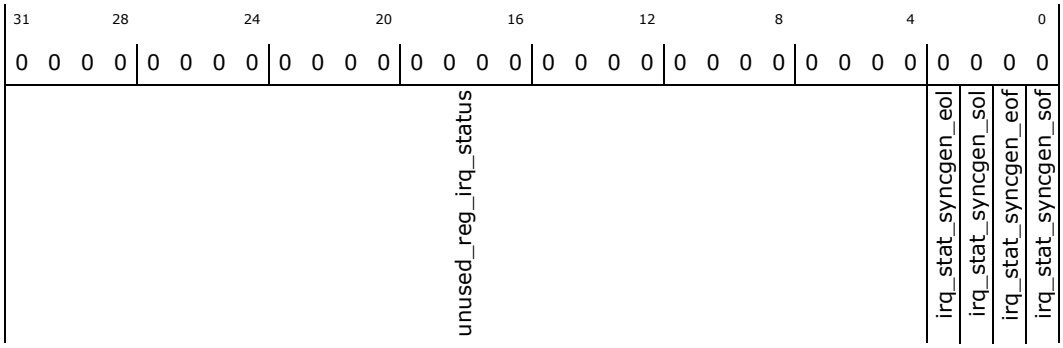
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_irq_ctrl_reg_irq_status: [ISPMMADR] + 90208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_status:** Unused
3	0h RO	**irq_stat_syncgen_eol:** Represents the irq status of the eol (end of line) bit generated by the sync generator
2	0h RO	**irq_stat_syncgen_sol:** Represents the irq status of the sol (start of line) bit generated by the sync generator
1	0h RO	**irq_stat_syncgen_eof:** Represents the irq status of the eof (end of frame) bit generated by the sync generator
0	0h RO	**irq_stat_syncgen_sof:** Represents the irq status of the sof (start of frame) bit generated by the sync generator

3.7.887 reg_isel_irq_ctrl_reg_irq_clear_type (isel_irq_ctrl_reg_irq_clear)—Offset 9020Ch

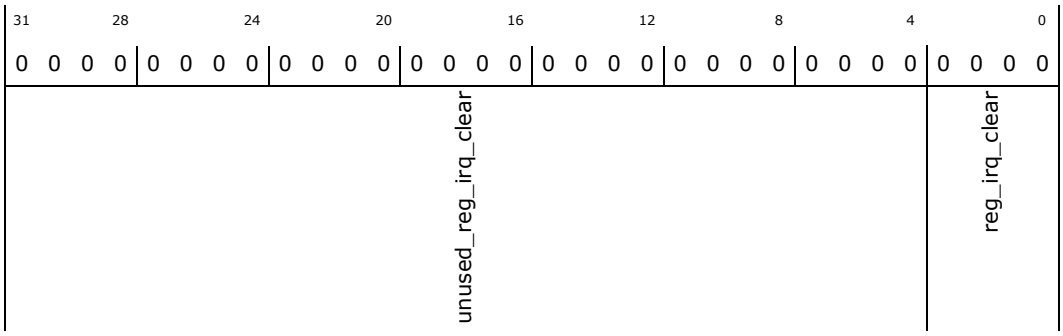
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_irq_ctrl_reg_irq_clear: [ISPMMADR] + 9020Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_clear:** Unused
3:0	0h WO	**reg_irq_clear:** Clears (set to '0') bits in reg_irq_status. When writing a '1' into a bit of this register, the corresponding bit in the req_irq_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the req_irq_status is not affected.

3.7.888 reg_isel_irq_ctrl_reg_irq_enable_type (isel_irq_ctrl_reg_irq_enable)—Offset 90210h

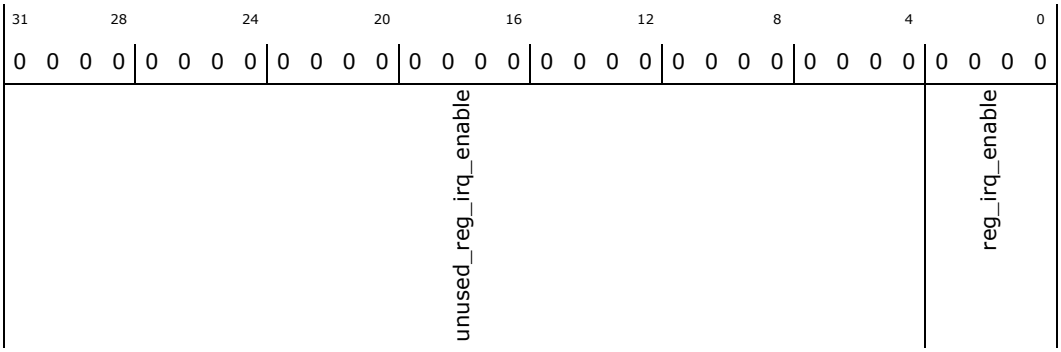
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_irq_ctrl_reg_irq_enable: [ISPMMADR] + 90210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_enable:** Unused
3:0	0h RW	**reg_irq_enable:** Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also affects the IRQ pin (value='1') or not (value='0')

3.7.889 reg_isel_irq_ctrl_reg_irq_level_not_pulse_type (isel_irq_ctrl_reg_irq_level_not_pulse)—Offset 90214h

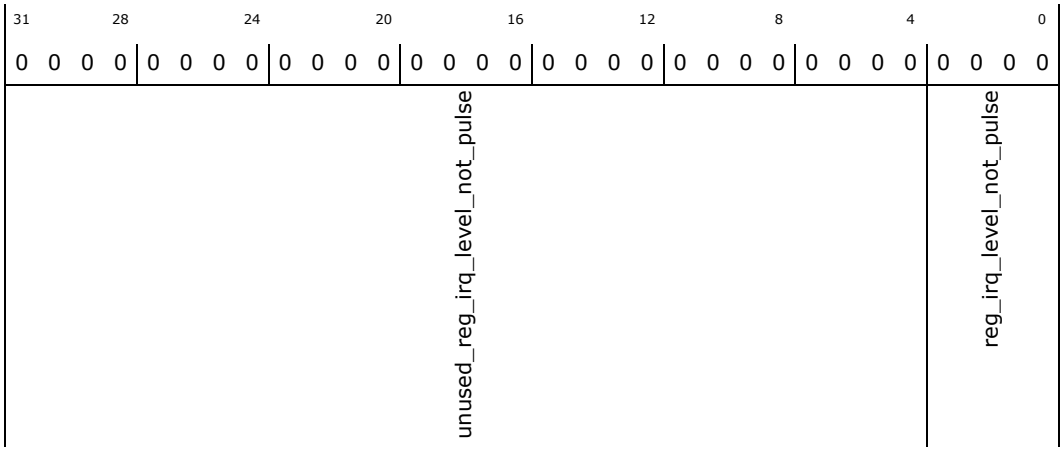
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_irq_ctrl_reg_irq_level_not_pulse: [ISPMMADR] + 90214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_level_not_pulse:** Unused
3:0	0h RW	**reg_irq_level_not_pulse:** Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

3.7.890 reg_icache_out_sys_c_mmu_MMU_invalidate_cache_type (icache_out_sys_c_mmu_MMU_invalidate_cache)—Offset A0000h

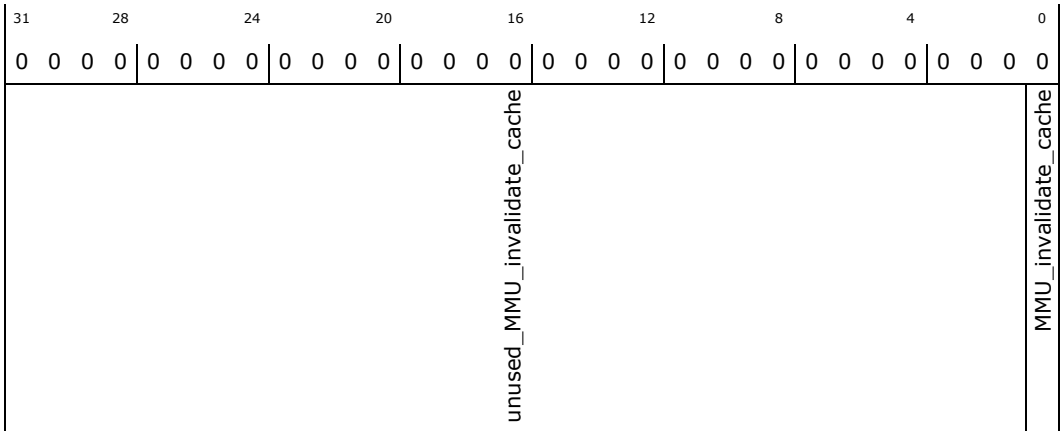
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

icache_out_sys_c_mmu_MMU_invalidate_cache: [ISPMMADR] + A0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_MMU_invalidate_cache:** Unused
0	0h WO	**MMU_invalidate_cache:** MMU invalidate cache. When '1', the MMUs TLB is invalidated.

3.7.891 reg_icache_out_sys_c_mmu_MMU_page_table_base_type (icache_out_sys_c_mmu_MMU_page_table_base)—Offset A0004h

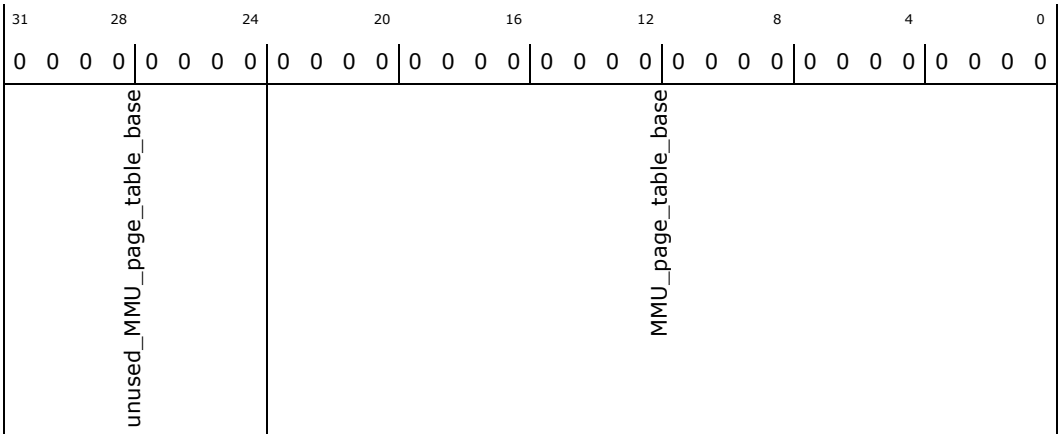
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

icache_out_sys_c_mmu_MMU_page_table_base: [ISPMMADR] + A0004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_MMU_page_table_base:** Unused
23:0	0h RW	**MMU_page_table_base:** Defines the physical page number of the page tables

3.7.892 mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first)—Offset B0000h

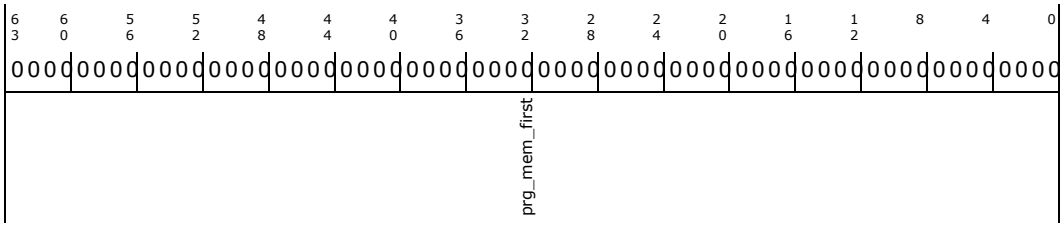
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first: [ISPMMADR] + B0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:0	0h RW	**prg_mem_first:** Read Latency of 1 cycles. Write latency of 0 cycles

3.7.893 mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last)—Offset B7FF8h

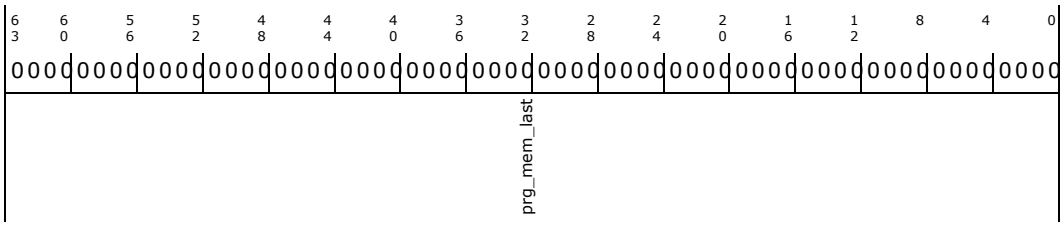
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last: [ISPMMADR] + B7FF8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:0	0h RW	**prg_mem_last:** Read Latency of 1 cycles. Write latency of 0 cycles

3.7.894 mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first_type

(isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first) —Offset 1C0000h

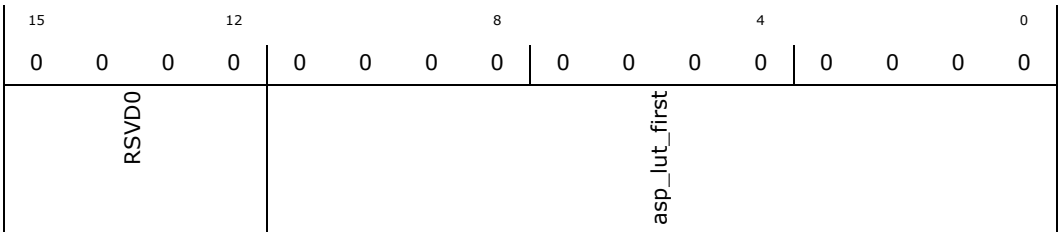
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first: [ISPMMADR] + 1C0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_first:** Read Latency of 67 cycles. Write latency of 0 cycles

3.7.895 mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1C0FFEh

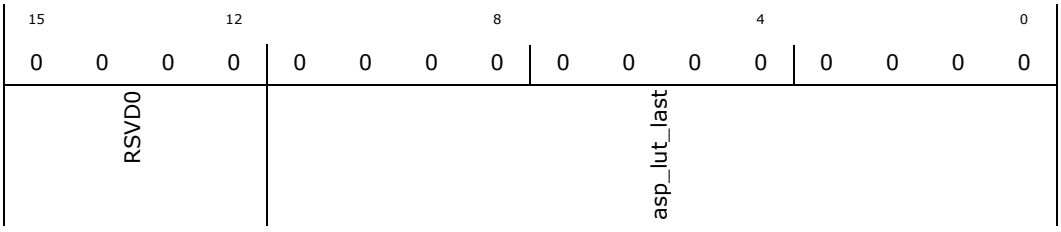
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last: [ISPMMADR] + 1C0FFEh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_last:** Read Latency of 67 cycles. Write latency of 0 cycles

3.7.896 mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1D0000h

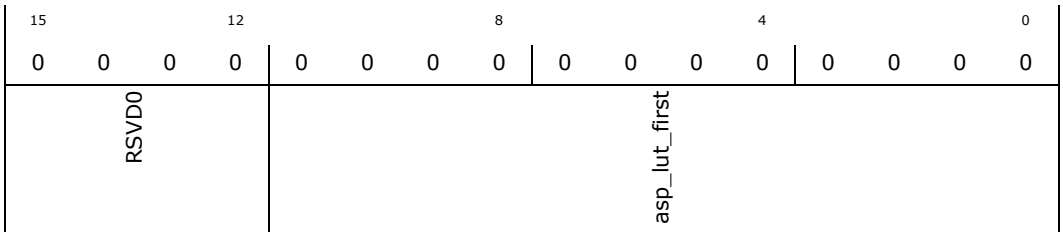
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first: [ISPMMADR] + 1D0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_first:** Read Latency of 67 cycles. Write latency of 0 cycles

3.7.897 mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1D0FFEh

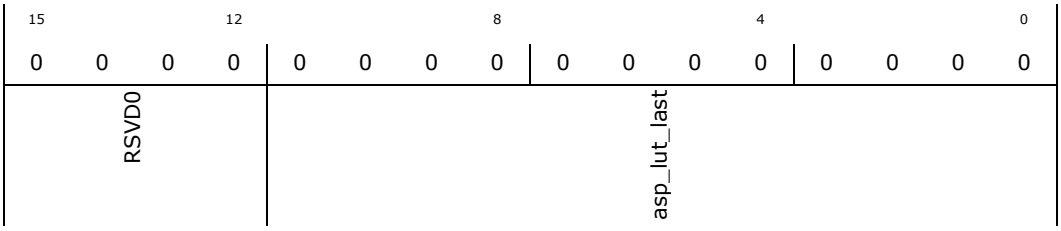
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last: [ISPMMADR] + 1D0FFEh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_last:** Read Latency of 67 cycles. Write latency of 0 cycles

3.7.898 mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1E0000h

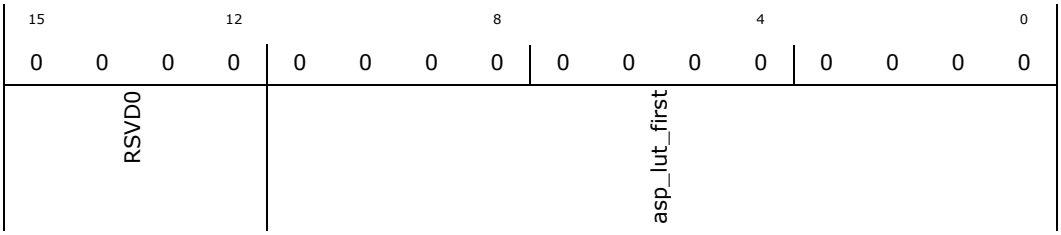
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first: [ISPMMADR] + 1E0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_first:** Read Latency of 67 cycles. Write latency of 0 cycles

3.7.899 mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1E0FFEh

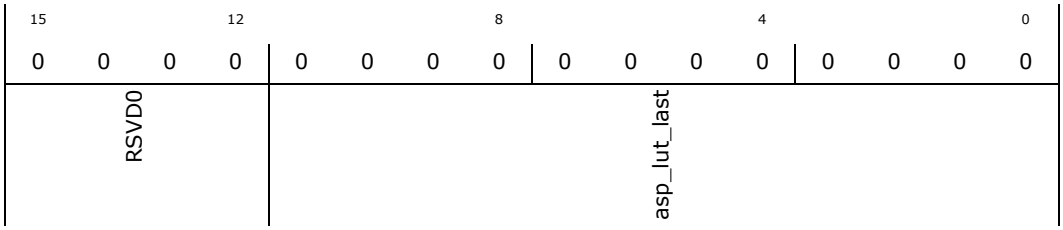
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last: [ISPMMADR] + 1E0FFEh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_last:** Read Latency of 67 cycles. Write latency of 0 cycles

3.7.900 mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first)—Offset 1F0000h

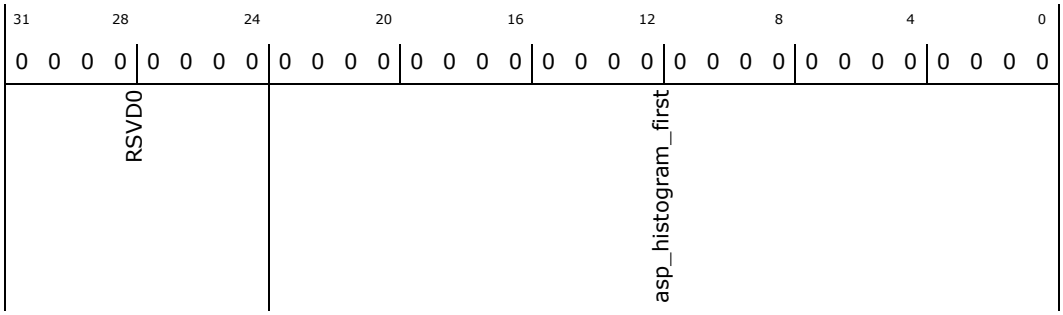
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first: [ISPMMADR] + 1F0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
23:0	0h RW	**asp_histogram_first:** Read Latency of 66 cycles. Write latency of 0 cycles

3.7.901 mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last)—Offset 1F0FFCh

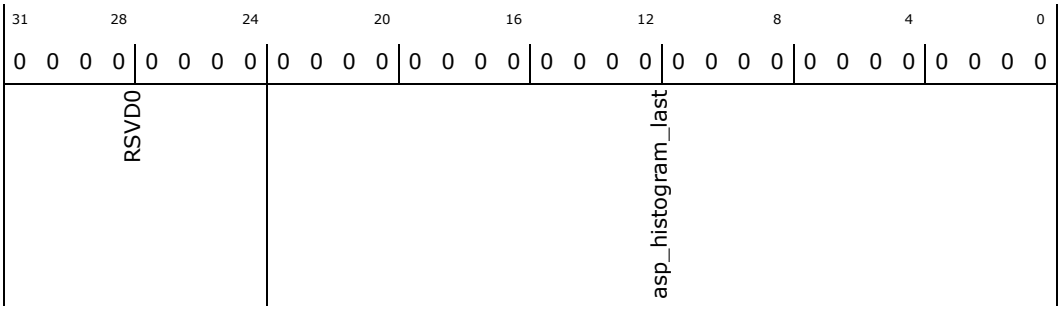
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last: [ISPMMADR] + 1F0FFCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved
23:0	0h RW	**asp_histogram_last:** Read Latency of 66 cycles. Write latency of 0 cycles

3.7.902 mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_first_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_first)—Offset 200000h

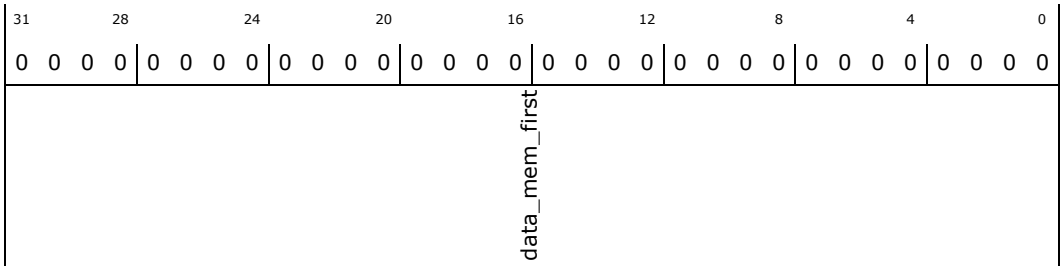
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_base_dmem_data_mem_sl_ipdmem_data_mem_first: [ISPMMADR] + 200000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**data_mem_first:** Read Latency of 2 cycles. Write latency of 0 cycles

3.7.903 mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_last_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_last)—Offset 203FFCh

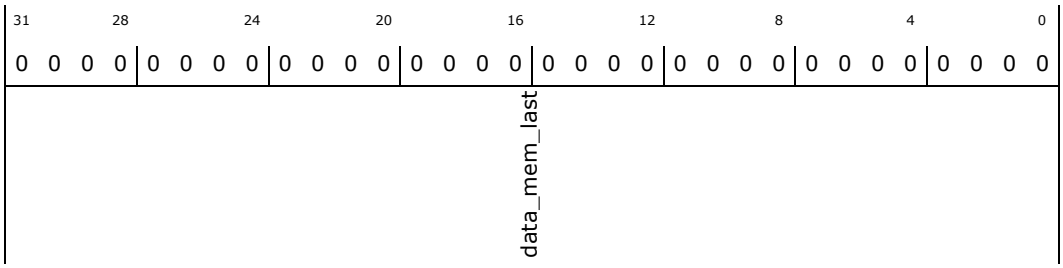
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_base_dmem_data_mem_sl_ipdmem_data_mem_last: [ISPMMADR] + 203FFCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**data_mem_last:** Read Latency of 2 cycles. Write latency of 0 cycles

3.7.904 mem_scp_dmem_mem_sl_ip_dmem_mem_first_type (scp_dmem_mem_sl_ip_dmem_mem_first)—Offset 300000h

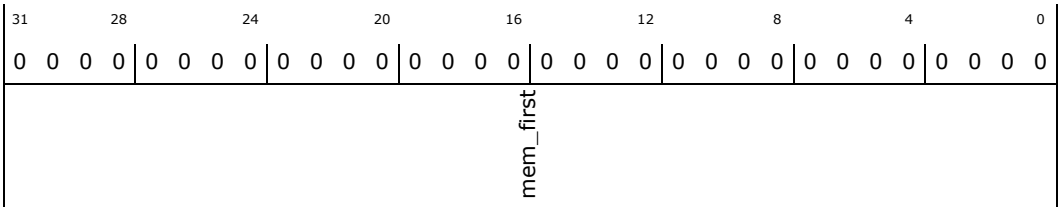
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_dmem_mem_sl_ip_dmem_mem_first: [ISPMMADR] + 300000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**mem_first:** Read Latency of 2 cycles. Write latency of 0 cycles

3.7.905 mem_scp_dmem_mem_sl_ip_dmem_mem_last_type (scp_dmem_mem_sl_ip_dmem_mem_last)—Offset 307FFCh

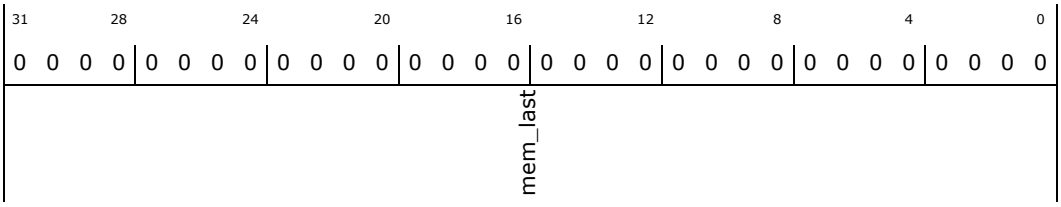
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_dmem_mem_sl_ip_dmem_mem_last: [ISPMMADR] + 307FFCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**mem_last:** Read Latency of 2 cycles. Write latency of 0 cycles

3.7.906 reg_fa_sp_isp_send_to_SP_type (fa_sp_isp_send_to_SP)—Offset 380008h

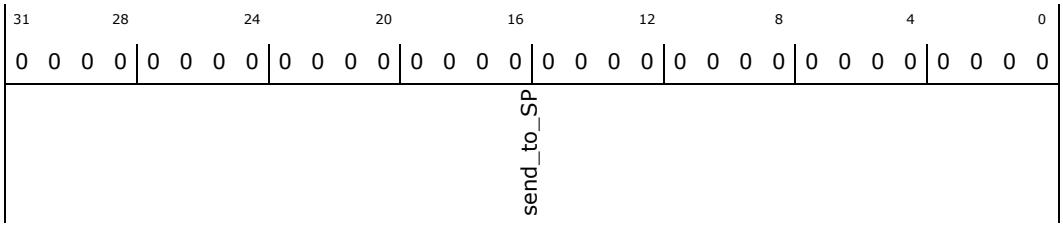
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

fa_sp_isp_send_to_SP: [ISPMMADR] + 380008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h WO	**send_to_SP:** Send data to SP streaming input port

3.7.907 reg_fa_sp_isp_send_to_ISP_type (fa_sp_isp_send_to_ISP)—Offset 38000Ch

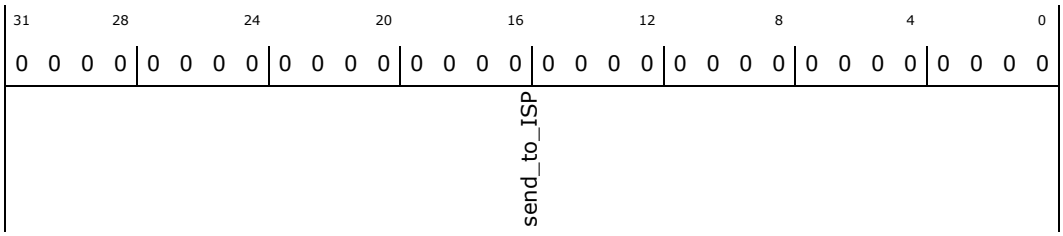
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

fa_sp_isp_send_to_ISP: [ISPMMADR] + 38000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h WO	**send_to_ISP:** Send data to ISP streaming input port

3.7.908 reg_fa_sp_isp_check_receive_from_SP_type (fa_sp_isp_check_receive_from_SP)—Offset 380010h

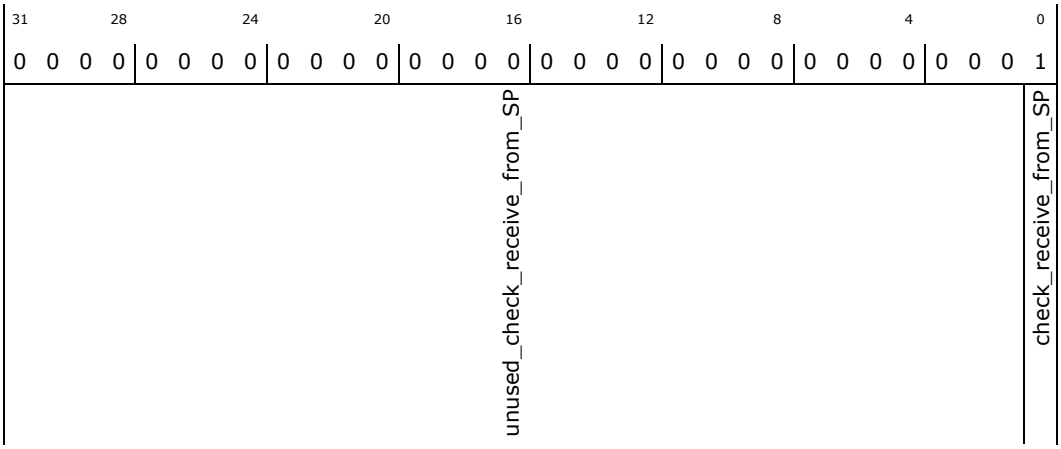
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

fa_sp_isp_check_receive_from_SP: [ISPMMADR] + 380010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_check_receive_from_SP:** Unused
0	1h RO	**check_receive_from_SP:** Check for potential stalling for receiving data on SP streaming output port. Returns 1 if a receive from SP would lead to a stall. Returns 0 if a token is available from the SP.

3.7.909 reg_fa_sp_isp_check_receive_from_ISP_type (fa_sp_isp_check_receive_from_ISP)—Offset 380014h

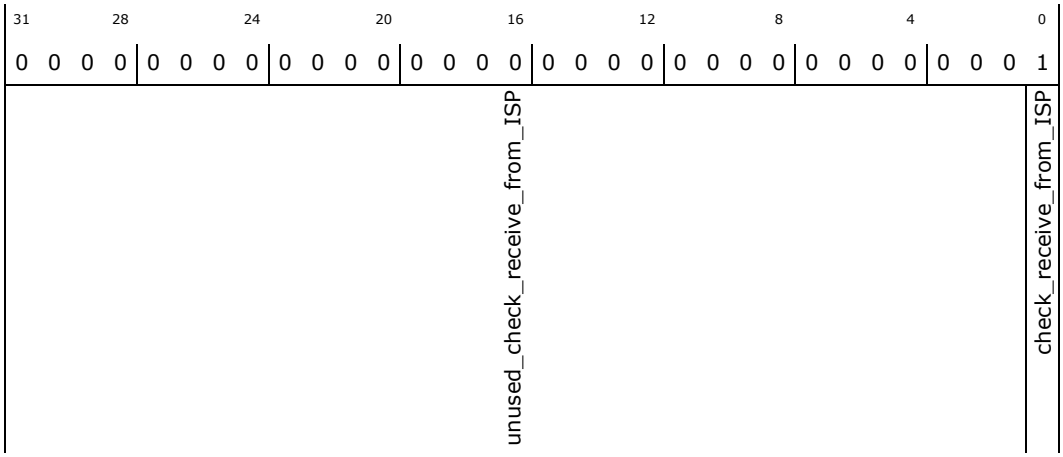
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

fa_sp_isp_check_receive_from_ISP: [ISPMMADR] + 380014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_check_receive_from_ISP:** Unused
0	1h RO	**check_receive_from_ISP:** Check for potential stalling for receiving data on ISP streaming output port. Returns 1 if a receive from ISP would lead to a stall. Returns 0 if a token is available from the ISP.

3.7.910 reg_fa_sp_isp_check_send_to_SP_type (fa_sp_isp_check_send_to_SP)—Offset 380018h

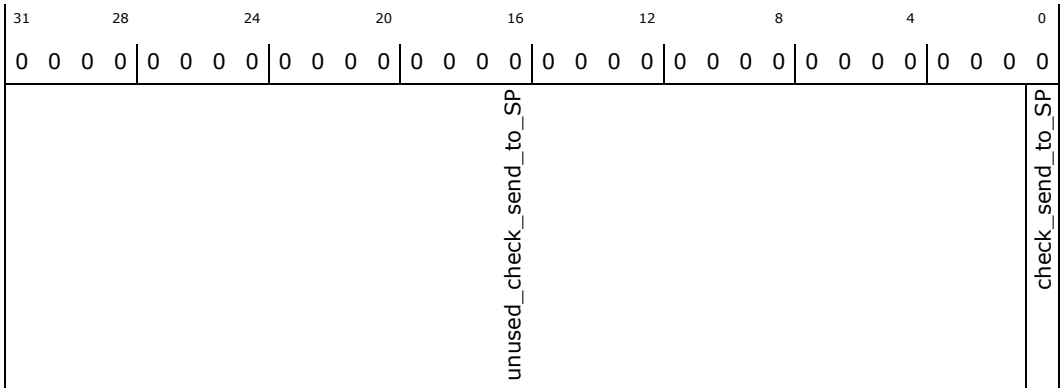
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

fa_sp_isp_check_send_to_SP: [ISPMMADR] + 380018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_check_send_to_SP:** Unused
0	0h RO	**check_send_to_SP:** Check for potential stalling for sending data to SP streaming input port. Returns 1 if a send to SP would lead to a stall. Returns 0 when there is space left in the SP token FIFO

3.7.911 reg_fa_sp_isp_check_send_to_ISP_type (fa_sp_isp_check_send_to_ISP)—Offset 38001Ch

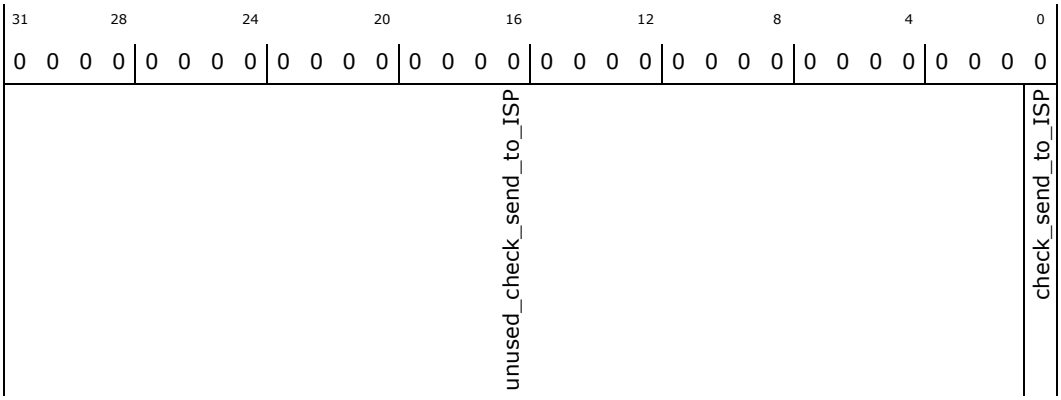
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

fa_sp_isp_check_send_to_ISP: [ISPMMADR] + 38001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_check_send_to_ISP:** Unused
0	0h RO	**check_send_to_ISP:** Check for potential stalling for sending data to ISP streaming input port. Returns 1 if a send to ISP would lead to a stall. Returns 0 when there is space left in the ISP token FIFO

3.8 eMMC PCI Configuration Registers

Table 16. Summary of eMMC PCI Configuration Registers—0/16/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 1468	00000000h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 1469	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 1470	00000000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 1471	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 1471	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 1472	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 1473	00000000h
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 1473	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 1474	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 1474	00000100h
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 1475	48030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 1476	00000008h
A0h	4	"reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h" on page 1476	00000000h
A4h	4	"reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h" on page 1477	00000000h
A8h	4	"reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h" on page 1477	00000000h
ACh	4	"reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh" on page 1478	00000000h
C0h	4	"reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h" on page 1478	00000000h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 1479	00000000h

3.8.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

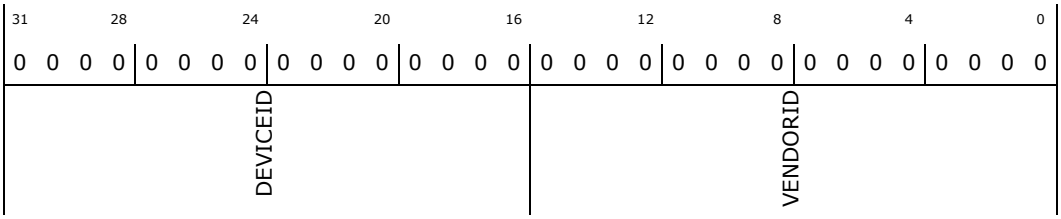
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:16, F:0] + 0h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**DEVICEID:** Reserved.
15:0	0000h RO	**VENDORID:** Reserved.

3.8.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

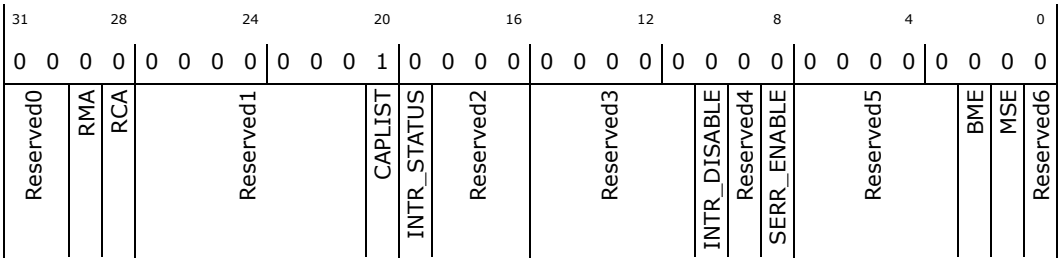
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:16, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** Reserved.
29	0h RW/1C	**RMA:** Reserved.
28	0h RW/1C	**RCA:** Reserved.
27:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**CAPLIST:** Reserved.
19	0h RO	**INTR_STATUS:** Reserved.

Bit Range	Default & Access	Description
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**INTR_DISABLE:** Reserved.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR_ENABLE:** Reserved.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**BME:** Reserved.
1	0h RW	**MSE:** Reserved.
0	0h RO	**Reserved6:** Reserved.

3.8.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

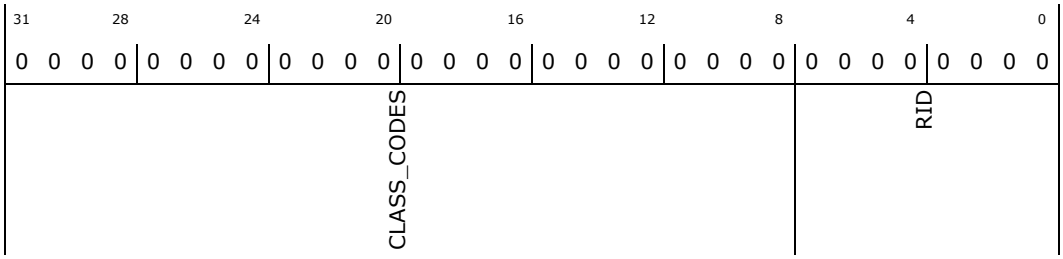
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:16, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**CLASS_CODES:** Reserved.
7:0	00h RO	**RID:** Reserved.

3.8.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

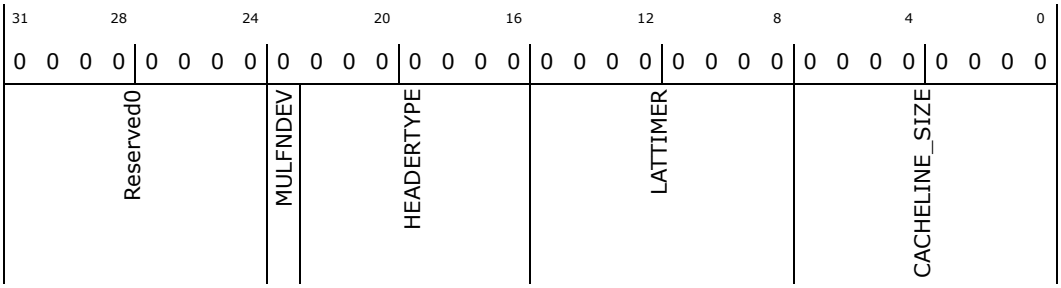
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:16, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	0h RO	**MULFNDEV:** Reserved.
22:16	00h RO	**HEADERTYPE:** Reserved.
15:8	00h RO	**LATTIMER:** Reserved.
7:0	00h RW	**CACHELINE_SIZE:** Reserved.

3.8.5 reg_BAR_type (BAR)—Offset 10h

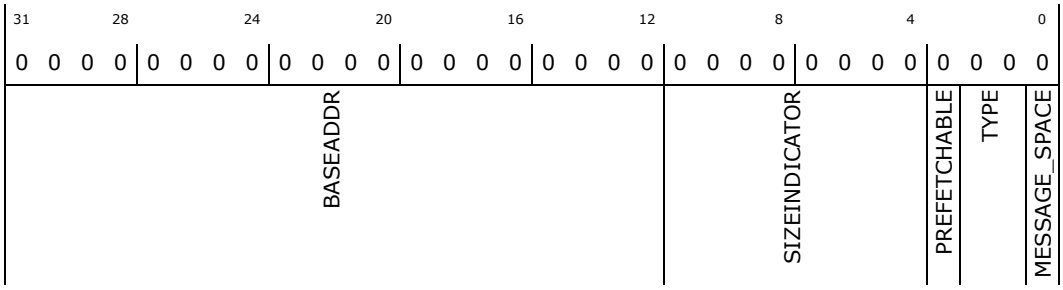
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Reserved.
11:4	00h RO	**SIZEINDICATOR:** Reserved.
3	0h RO	**PREFETCHABLE:** Reserved.
2:1	0h RO	**TYPE:** Reserved.
0	0h RO	**MESSAGE_SPACE:** Reserved.

3.8.6 reg_BAR1_type (BAR1)—Offset 14h

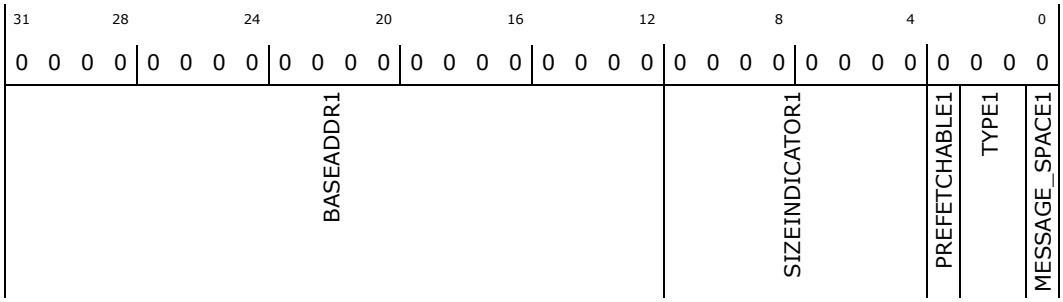
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:16, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** Reserved.
11:4	00h RO	**SIZEINDICATOR1:** Reserved.

Bit Range	Default & Access	Description
3	0h RO	**PREFETCHABLE1:** Reserved.
2:1	0h RO	**TYPE1:** Reserved.
0	0h RO	**MESSAGE_SPACE1:** Reserved.

3.8.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

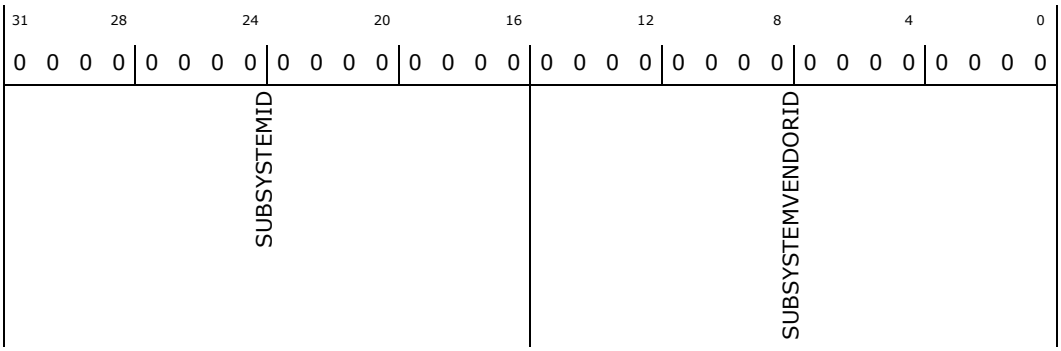
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:16, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Reserved.
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Reserved.

3.8.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

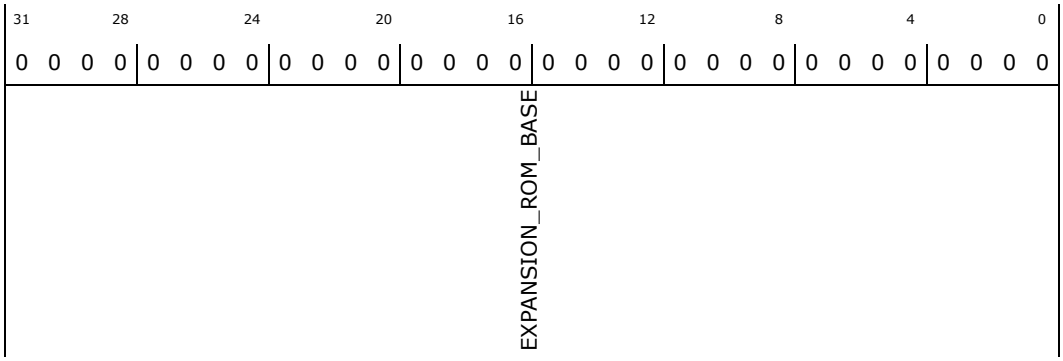
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:16, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

3.8.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

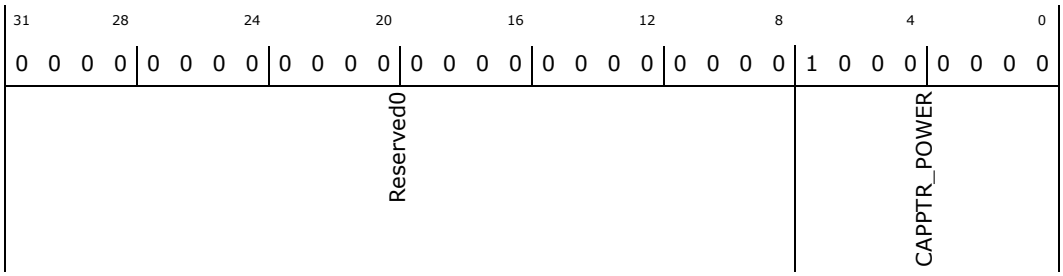
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:16, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	80h RO	**CAPPTR_POWER:** Reserved.

3.8.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

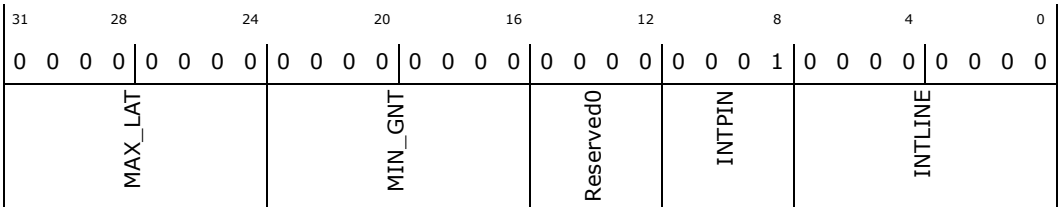
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:16, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Reserved.
23:16	00h RO	**MIN_GNT:** Reserved.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**INTPIN:** Reserved.
7:0	00h RW	**INTLINE:** Reserved.

3.8.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

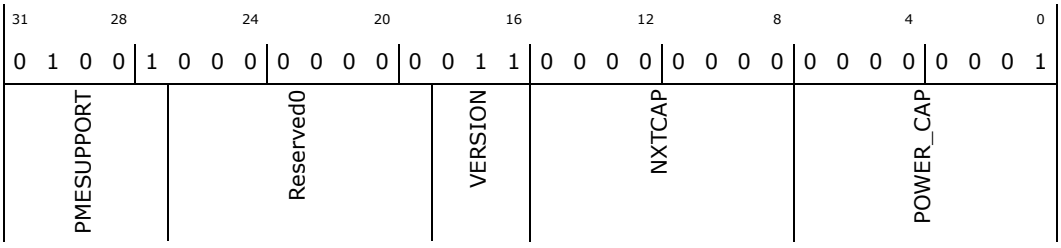
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:16, F:0] + 80h

Default: 48030001h



Bit Range	Default & Access	Description
31:27	09h RO	**PMESUPPORT:** Reserved.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**VERSION:** Reserved.

Bit Range	Default & Access	Description
15:8	00h RO	**NXTCAP:** Reserved.
7:0	01h RO	**POWER_CAP:** Reserved.

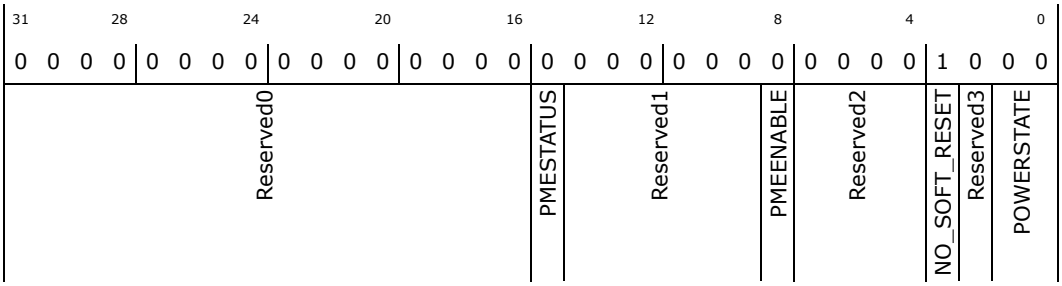
3.8.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:16, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PMESTATUS:** Reserved.
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PMEENABLE:** Reserved.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**NO_SOFT_RESET:** Reserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**POWERSTATE:** Reserved.

3.8.13 reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h

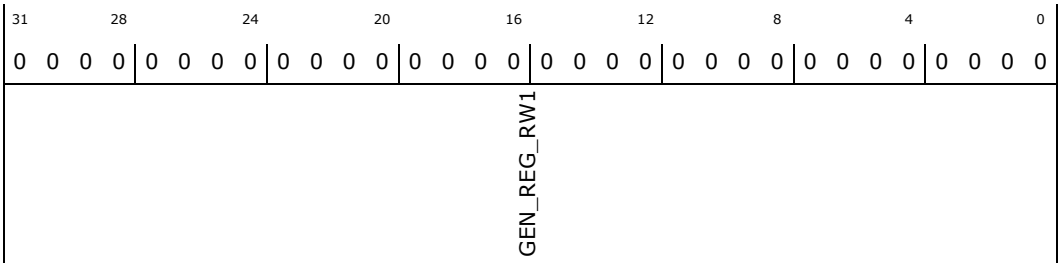
General Purpose Read Write Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW1: [B:0, D:16, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW1:** capabilities over-ride for the sd/sdio/emmc host controller (bits 31:0)

3.8.14 reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h

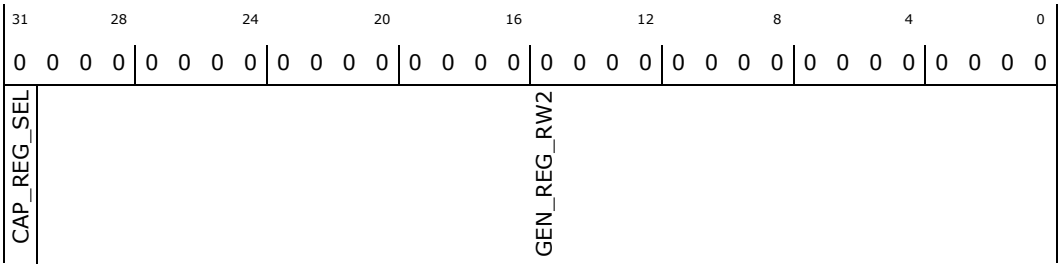
General Purpose Read Write Register2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW2: [B:0, D:16, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**CAP_REG_SEL:** select if the capability will come from the GEN PCI register or from a hard wire
30:0	0h RW	**GEN_REG_RW2:** capabilities over-ride for the sd/sdio/emmc host controller (bits 62:32)

3.8.15 reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h

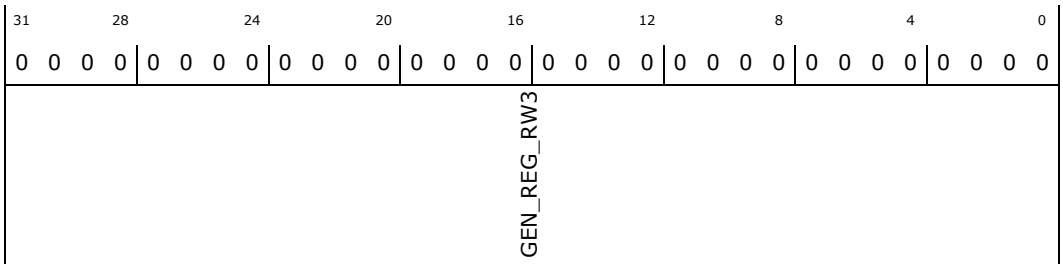
General Purpose Read Write Register3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW3: [B:0, D:16, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW3:** Reserved.

3.8.16 reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh

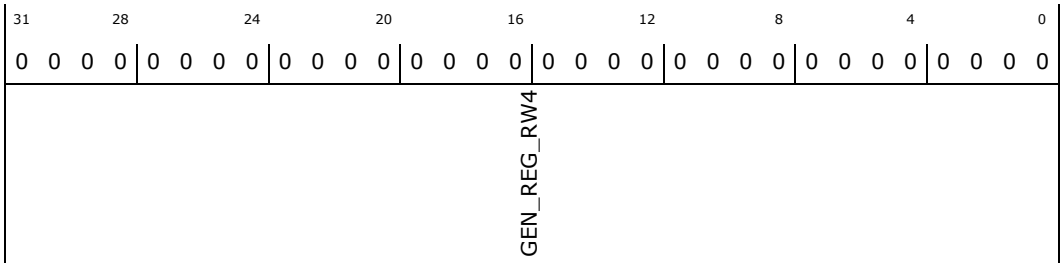
General Purpose Read Write Register4

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW4: [B:0, D:16, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW4:** Reserved.

3.8.17 reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h

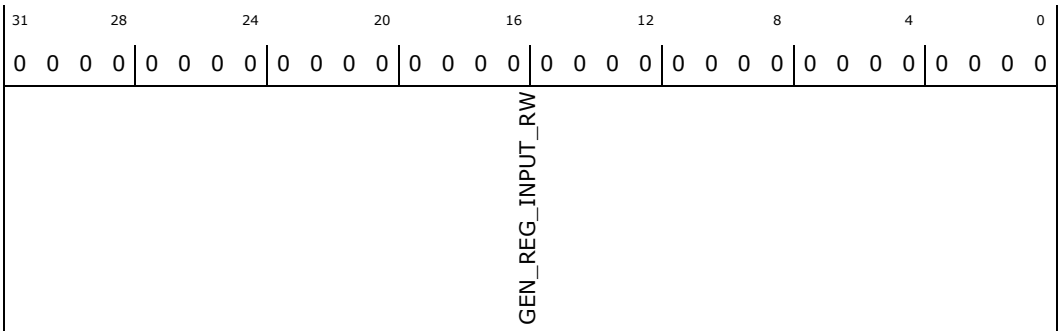
General Purpose Input Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_INPUT_REGRW: [B:0, D:16, F:0] + C0h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**GEN_REG_INPUT_RW:** Reserved.

3.8.18 reg_MANID_type (MANID)—Offset F8h

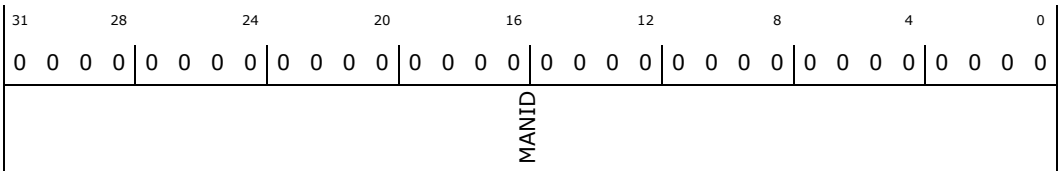
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:16, F:0] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**MANID:** Reserved.

3.9 eMMC Memory Mapped IO Registers

Table 17. Summary of eMMC Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"SDMA System Address Register (SYS_ADR)—Offset 0h" on page 1481	00000000h
4h	2	"Block Size Register (BLK_SIZE)—Offset 4h" on page 1482	0000h
6h	2	"Block Count Register (BLK_COUNT)—Offset 6h" on page 1483	0000h
8h	4	"Argument Register (ARGUMENT)—Offset 8h" on page 1484	00000000h
Ch	2	"Transfer Mode Register (TX_MODE)—Offset Ch" on page 1484	0000h
Eh	2	"Command Register (CMD)—Offset Eh" on page 1485	0000h
10h	4	"Response Register0 (RESPONSE0)—Offset 10h" on page 1486	00000000h
14h	4	"Response Register2 (RESPONSE2)—Offset 14h" on page 1487	00000000h
18h	4	"Response Register4 (RESPONSE4)—Offset 18h" on page 1487	00000000h
1Ch	4	"Response Register6 (RESPONSE6)—Offset 1Ch" on page 1488	00000000h
20h	4	"Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h" on page 1489	00000000h
24h	4	"Present State Register (PRE_STATE)—Offset 24h" on page 1489	1FFF0000h
28h	1	"Host Control Register (HOST_CTL)—Offset 28h" on page 1490	00h
29h	1	"Power Control Register (PWR_CTL)—Offset 29h" on page 1491	00h
2Ah	1	"Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah" on page 1492	00h
2Bh	1	"Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh" on page 1493	00h
2Ch	2	"Clock Control Register (CLK_CTL)—Offset 2Ch" on page 1493	0000h
2Eh	1	"Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh" on page 1494	00h
2Fh	1	"Software Reset Register (SW_RST)—Offset 2Fh" on page 1495	00h
30h	2	"Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h" on page 1495	0000h
32h	2	"Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h" on page 1496	0000h
34h	2	"Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h" on page 1498	0000h
36h	2	"Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h" on page 1499	0000h
38h	2	"Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h" on page 1500	0000h
3Ah	2	"Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah" on page 1501	0000h
3Ch	4	"Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch" on page 1503	00000000h
40h	4	"Capabilities Register (CAPABILITIES)—Offset 40h" on page 1504	00000000h
44h	4	"Capabilities Register 2 (CAPABILITIES_2)—Offset 44h" on page 1505	00000000h

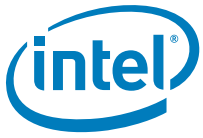


Table 17. Summary of eMMC Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
48h	4	"Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h" on page 1505	00000000h
50h	2	"Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h" on page 1506	0000h
52h	2	"Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h" on page 1507	0000h
54h	1	"ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h" on page 1508	00h
58h	4	"ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h" on page 1509	00000000h
60h	4	"Preset Values registers (PRESET_VALUE_0)—Offset 60h" on page 1509	00020002h
64h	4	"Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h" on page 1510	00020001h
68h	4	"Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h" on page 1510	00000001h
6Ch	4	"Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch" on page 1511	00010000h
70h	4	"BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h" on page 1511	00000000h
74h	1	"DEBUG_SEL (DEBUG_SEL)—Offset 74h" on page 1512	00h
E0h	4	"Shared Bus Control Register (SHARED_BUS)—Offset E0h" on page 1512	00000000h
F0h	1	"SPI_INT_SUP (SPI_INT_SUP)—Offset F0h" on page 1514	00h
FCh	2	"Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh" on page 1515	0000h
FEh	2	"Host Controller Version Register (HOST_CTRL_VER)—Offset FEh" on page 1515	B402h

3.9.1 SDMA System Address Register (SYS_ADR)—Offset 0h

This register contains the physical system memory address used for DMA transfers

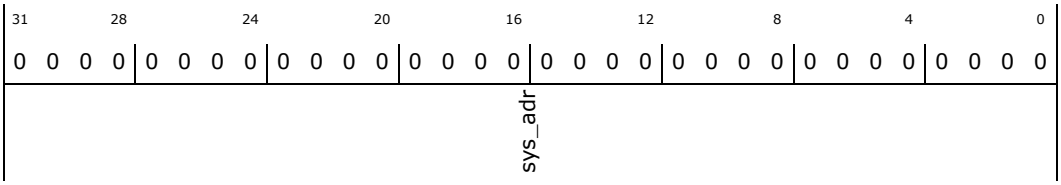
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SYS_ADR: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**SYS_ADR (sys_adr):** SDMA System Address This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register.

3.9.2 Block Size Register (BLK_SIZE)—Offset 4h

This register is used to configure the number of bytes in a data block.

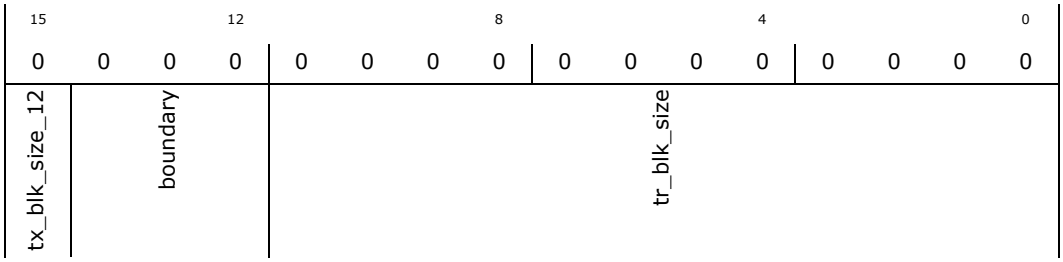
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

BLK_SIZE: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**TX_BLK_SIZE_12 (tx_blk_size_12):** Transfer Block Size 12th bit. This bit is added to support 4Kb Data block transfer.

Bit Range	Default & Access	Description
14:12	000b RW	**BOUNDARY (boundary):** Host SDMA Buffer Boundary The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. ADMA does not use this register. 000b - 4K bytes (Detects A11 carry out) 001b - 8K bytes (Detects A12 carry out) 010b - 16K Bytes (Detects A13 carry out) 011b - 32K Bytes (Detects A14 carry out) 100b - 64K bytes (Detects A15 carry out) 101b - 128K Bytes (Detects A16 carry out) 110b - 256K Bytes (Detects A17 carry out) 111b - 512K Bytes (Detects A18 carry out)
11:0	000h RW	**TR_BLK_SIZE (tr_blk_size):** Transfer Block Size This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes (Refer to Implementation Note in Section 1.7.2). It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. 0800h 2048 Bytes ??? ??? 0200h 512 Bytes 01FFh 511 Bytes ??? ??? 0004h 4 Bytes 0003h 3 Bytes 0002h 2 Bytes 0001h 1 Byte 0000h No data transfer

3.9.3 Block Count Register (BLK_COUNT)—Offset 6h

This register is used to configure the number of data blocks

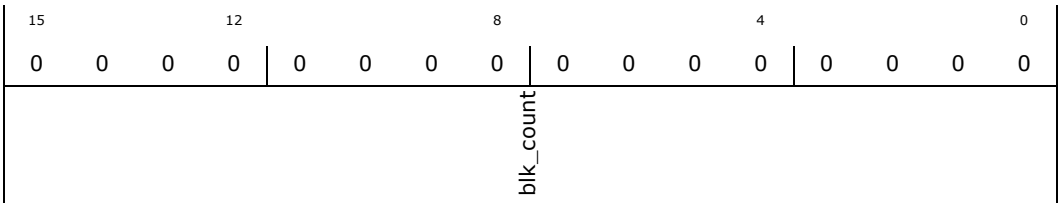
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

BLK_COUNT: [BAR] + 6h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	0000h RW	**BLK_COUNT (blk_count):** Blocks Count For Current Transfer This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers

3.9.4 Argument Register (ARGUMENT)—Offset 8h

This register contains the SD Command Argument.

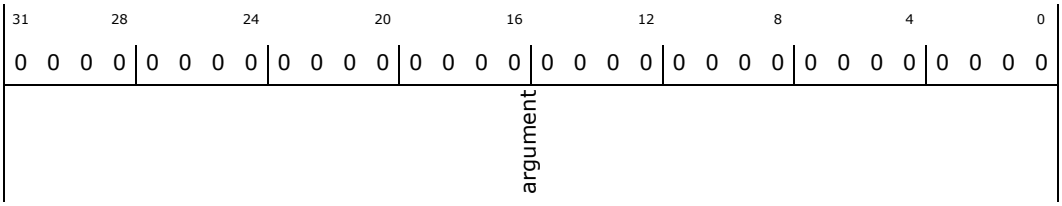
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ARGUMENT: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**ARGUMENT (argument):** Command Argument The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

3.9.5 Transfer Mode Register (TX_MODE)—Offset Ch

Transfer Mode Register

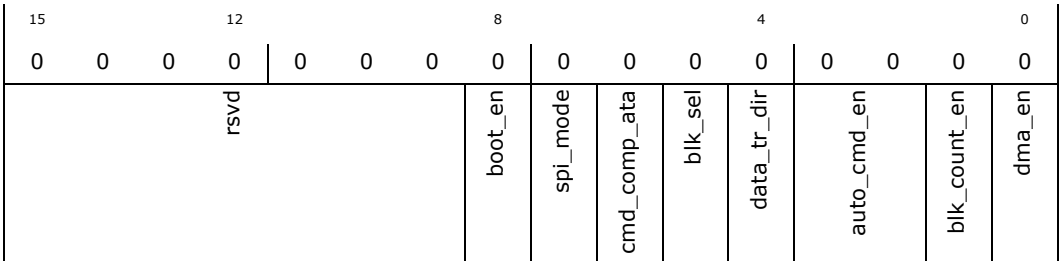
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

TX_MODE: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:9	00h RO	**RSVD (rsvd):** Reserved
8	0b RW	**BOOT_EN (boot_en):** To start boot operation for MMC4.3 1 - To start boot mode 0 - Stop the boot read
7	0b RW	**SPI_MODE (spi_mode):** SPI mode enable bit. 1 - SPI mode 0 - SD mode
6	0b RW	**CMD_COMP_ATA (cmd_comp_ata):** Command Completion Signal Enable for CE-ATA Device. ???1??? - Device will send command completion Signal ???0??? - Device will not send command completion Signal
5	0b RW	**BLK_SEL (blk_sel):** Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the Block Count register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block
4	0b RW	**Data_TR_Dir (data_tr_dir):** Data Transfer Direction Select This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller and it is set to 0 for all other commands. 1 Read (Card to Host) 0 Write (Host to Card)
3:2	0b RW	**AUTO_CMD_EN (auto_cmd_en):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0b RW	**BLK_COUNT_EN (blk_count_en):** Block Count Enable This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8) If ADMA2 data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table. 1 Enable 0 Disable
0	0b RW	**DMA_EN (dma_en):** DMA Enable This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the Capabilities register. One of the DMA modes can be selected by DMA Select in the Host Control register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of Command register (00Fh). 1 DMA Data transfer 0 No data transfer or Non DMA data transfer

3.9.6 Command Register (CMD)—Offset Eh

Command Register

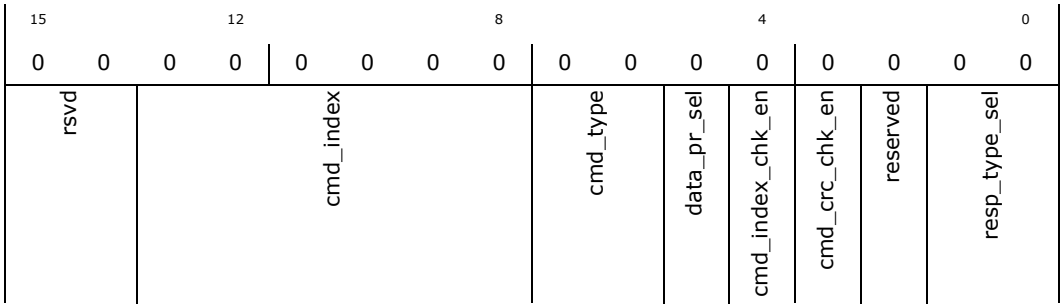
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

CMD: [BAR] + Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:14	0h RO	**RSVD (rsvd):** Reserved
13:8	0h RW	**CMD_INDEX (cmd_index):** Command Index These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.
7:6	00b RW	**CMD_TYPE (cmd_type):** Command Type
5	0b RW	**DATA_PR_SEL (data_pr_sel):** Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) (3) Resume command 1 Data Present 0 No Data Present
4	0b RW	**CMD_INDEX_CHK_EN (cmd_index_chk_en):** Command Index Check Enable If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 1 Enable 0 Disable
3	0b RW	**CMD_CRC_CHK_EN (cmd_crc_chk_en):** Command CRC Check Enable If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response. (Refer to definition in D01-00 and Table 2-10 below.) 1 Enable 0 Disable
2	0b RO	**Reserved (reserved):** Reserved
1:0	0h RW	**RESP_TYPE_SEL (resp_type_sel):** Response Type Select 00 No Response 01 Response Length 136 10 Response Length 48 11 Response Length 48 check Busy after response

3.9.7 Response Register0 (RESPONSE0)—Offset 10h

This register is used to store responses from SD cards

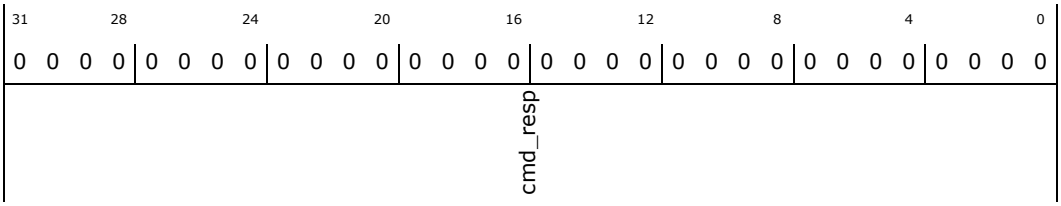
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE0: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP0 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.9.8 Response Register2 (RESPONSE2)—Offset 14h

This register is used to store responses from SD cards

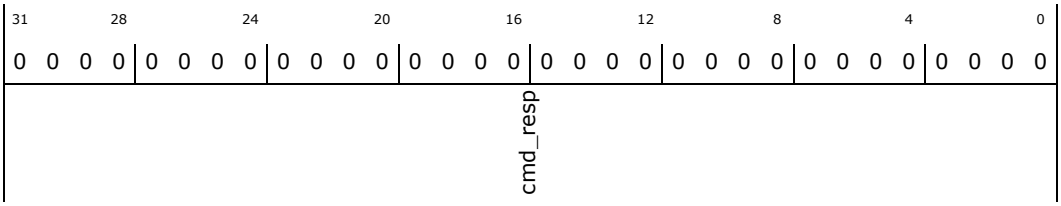
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE2: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP2 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.9.9 Response Register4 (RESPONSE4)—Offset 18h

This register is used to store responses from SD cards

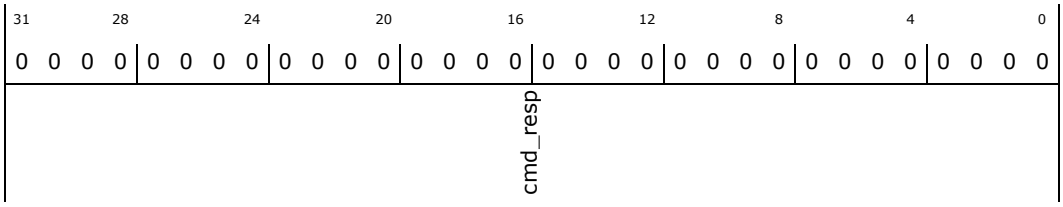
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE4: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP4 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.9.10 Response Register6 (RESPONSE6)—Offset 1Ch

This register is used to store responses from SD cards

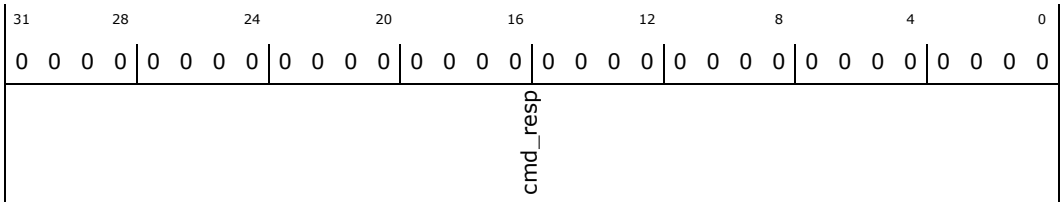
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE6: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP6 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.9.11 Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h

32-bit data port register to access internal buffer

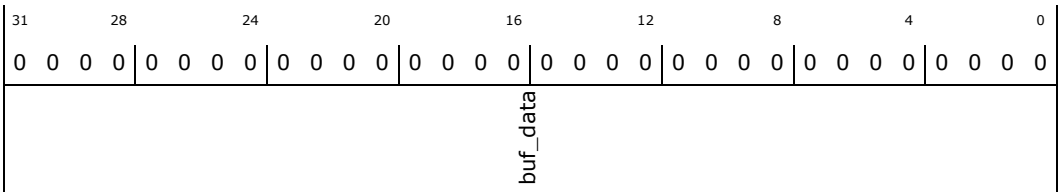
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BUF_DATA_PORT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUF_DATA (buf_data):** Buffer Data The Host Controller buffer can be accessed through this 32-bit Data Port register. Refer to 1.7

3.9.12 Present State Register (PRE_STATE)—Offset 24h

The Host Driver can get status of the Host Controller from this 32-bit read only register

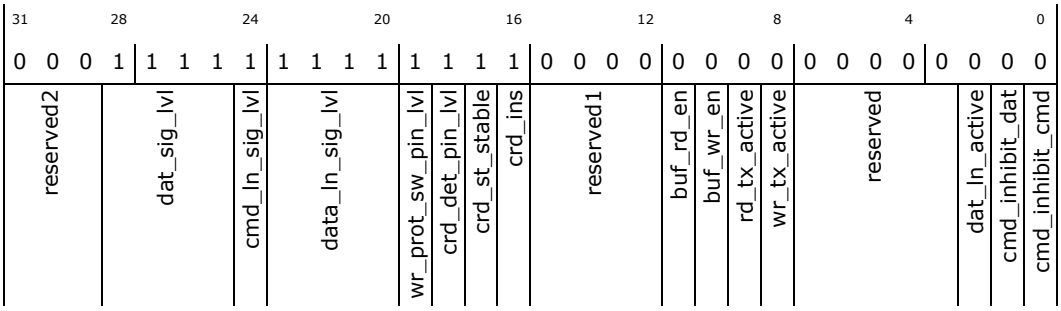
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRE_STATE: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 1FFF0000h



Bit Range	Default & Access	Description
31:29	0h RO	**Reserved2 (reserved2):** Reserved

Bit Range	Default & Access	Description
28:25	1111b RO	**DAT_SIG_LVL (dat_sig_lvl):** This status is used to check DAT line level to recover from errors, and for debugging. D28 - DAT[7] D27 - DAT[6] D26 - DAT[5] D25 - DAT[4]
24	1b RO	**CMD_LN_SIG_LVL (cmd_ln_sig_lvl):** CMD Line Signal Level This status is used to check the CMD line level to recover from errors, and for debugging.
23:20	Fh RO	**DATA_LN_SIG_LVL (data_ln_sig_lvl):** DAT[3:0] Line Signal Level This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D23 DAT[3] D22 DAT[2] D21 DAT[1] D20 DAT[0]
19	1b RO	**WR_PROT_SW_PIN_LVL (wr_prot_sw_pin_lvl):** Write Protect Switch Pin Level
18	1b RO	**CRD_DET_PIN_LVL (crd_det_pin_lvl):** Card Detect Pin Level
17	1b RO	**CRD_ST_STABLE (crd_st_stable):** Card State Stable
16	1b RO	**CRD_INS (crd_ins):** Card Inserted
15:12	0h RO	**Reserved1 (reserved1):** Reserved
11	0b RO	**BUF_RD_EN (buf_rd_en):** Buffer Read Enable
10	0b RO	**BUF_WR_EN (buf_wr_en):** Buffer Write Enable
9	0b RO	**RD_TX_ACTIVE (rd_tx_active):** Read Transfer Active
8	0b RO	**WR_TX_ACTIVE (wr_tx_active):** Write Transfer Active
7:3	00h RO	**Reserved (reserved):** Reserved
2	0b RO	**DAT_LN_ACTIVE (dat_ln_active):** DAT Line Active
1	0b RO	**CMD_INHIBIT_DAT (cmd_inhibit_dat):** Command Inhibit (DAT)
0	0b RO	**CMD_INHIBIT_CMD (cmd_inhibit_cmd):** Command Inhibit (CMD)

3.9.13 Host Control Register (HOST_CTL)—Offset 28h

Host Control Register

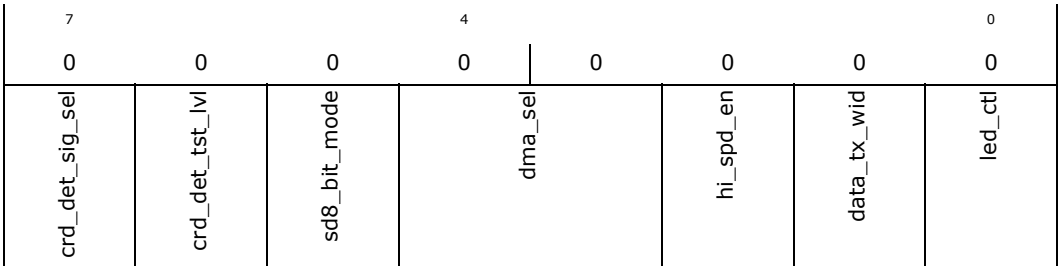
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

HOST_CTL: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RW	**CRD_DET_SIG_SEL (crd_det_sig_sel):** Card Detect Signal Selection
6	0b RW	**CRD_DET_TST_LVL (crd_det_tst_lvl):** Card Detect Test Level
5	0b RW	**SD8_BIT_MODE (sd8_bit_mode):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card.
4:3	00b RW	**DMA_SEL (dma_sel):** DMA Select
2	0b RW	**HI_SPD_EN (hi_spd_en):** High Speed Enable
1	0b RW	**DATA_TX_WID (data_tx_wid):** Data Transfer Width
0	0b RW	**LED_CTL (led_ctl):** LED Control

3.9.14 Power Control Register (PWR_CTL)—Offset 29h

Power Control Register

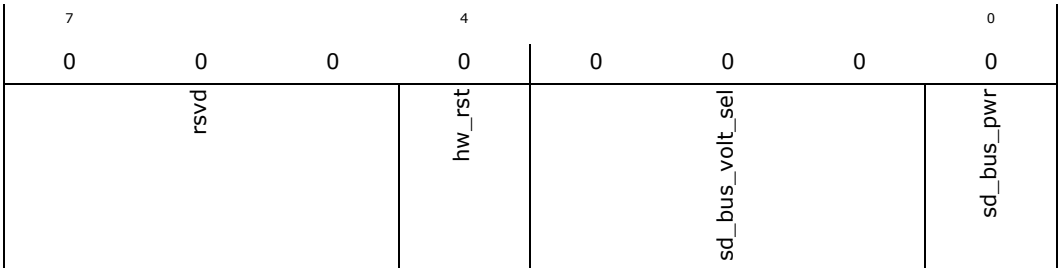
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PWR_CTL: [BAR] + 29h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:5	0h RO	**RSVD (rsvd):** Reserved
4	0b RW	**HW_rst (hw_rst):** HW reset
3:1	0h RW	**SD_BUS_VOLT_SEL (sd_bus_volt_sel):** SD Bus Voltage Select
0	0b RW	**SD_BUS_PWR (sd_bus_pwr):** SD Bus Power

3.9.15 Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah

Block Gap Control Register

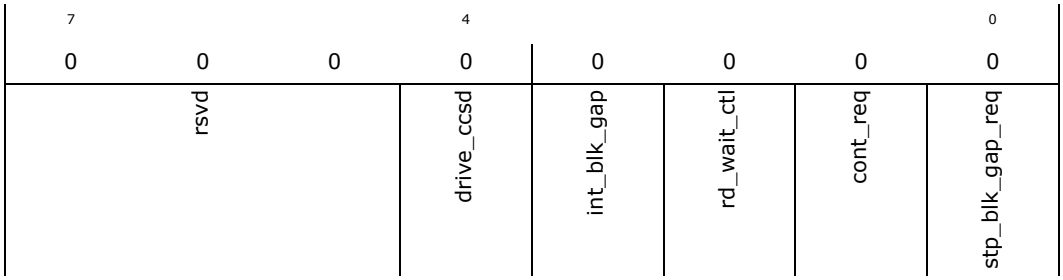
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

_BLK_GAP_CTL: [BAR] + 2Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:5	0h RO	**RSVD (rsvd):** Reserved
4	0b RW	**DRIVE_CCSD (drive_ccsd):** If the driver set this bit (change from ???0?? to ???1??), Host controller will send command completion
3	0b RW	**INT_BLK_GAP (int_blk_gap):** Interrupt At Block Gap
2	0b RW	**RD_WAIT_CTL (rd_wait_ctl):** Read Wait Control
1	0b RW	**CONT_REQ (cont_req):** Continue Request
0	0b RW	**STP_BLK_GAP_REQ (stp_blk_gap_req):** Stop At Block Gap Request

3.9.16 Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh

This register is used for wakeup event control.

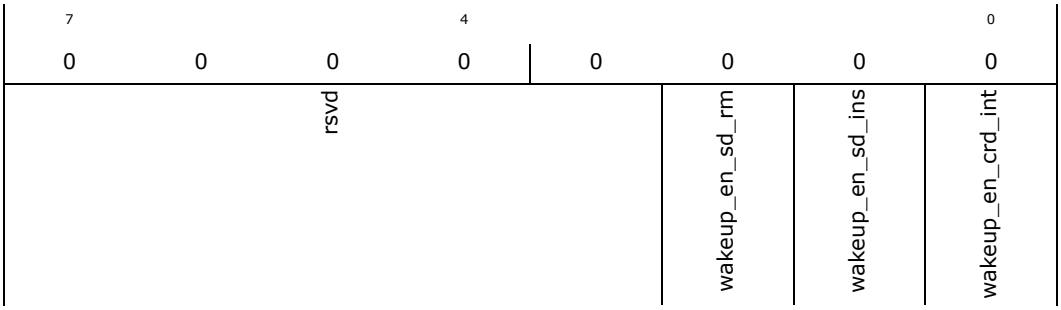
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

WAKEUP_CTL: [BAR] + 2Bh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**WAKEUP_EN_SD_RM (wakeup_en_sd_rm):** Wakeup Event Enable On SD Card Removal
1	0b RW	**WAKEUP_EN_SD_INS (wakeup_en_sd_ins):** Wakeup Event Enable On SD Card Insertion
0	0b RW	**WAKEUP_EN_CRD_INT (wakeup_en_crd_int):** Wakeup Event Enable On Card Interrupt

3.9.17 Clock Control Register (CLK_CTL)—Offset 2Ch

This register is used configure the frequency of the SDIO controller, and enable the clock.

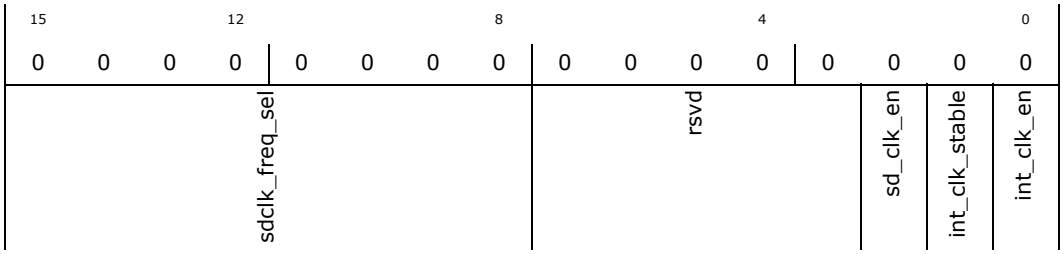
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

CLK_CTL: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RW	**SDCLK_FREQ_SEL (sdclk_freq_sel):** SDCLK Frequency Select
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**SD_CLK_EN (sd_clk_en):** SD Clock Enable
1	0b RO	**INT_CLK_STABLE (int_clk_stable):** Internal Clock Stable
0	0b RW	**INT_CLK_EN (int_clk_en):** Internal Clock Enable

3.9.18 Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh

Timeout Control Register

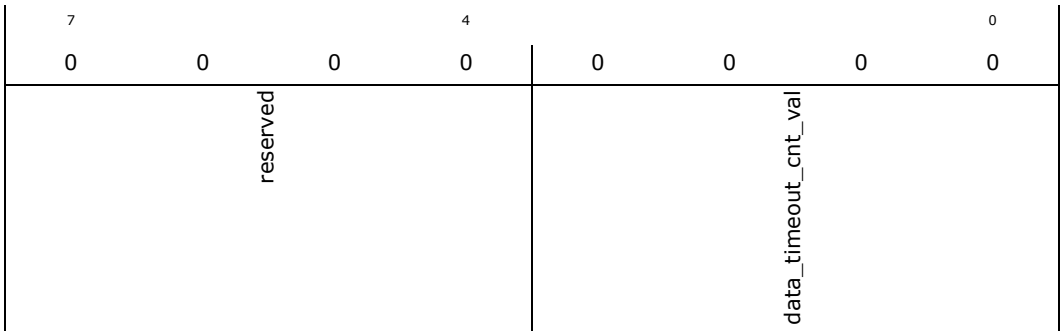
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

TIMEOUT_CTL: [BAR] + 2Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:4	0h RO	**Reserved (reserved):** Reserved

Bit Range	Default & Access	Description
3:0	0h RW	**DATA_TIMEOUT_CNT_VAL (data_timeout_cnt_val):** Data Timeout Counter Value

3.9.19 Software Reset Register (SW_RST)—Offset 2Fh

Software Reset Register

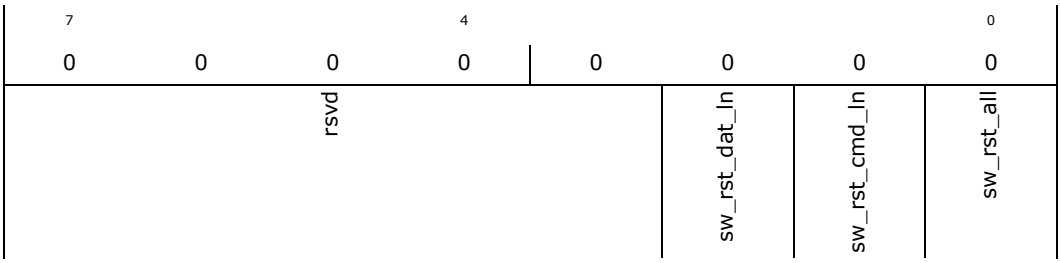
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SW_RST: [BAR] + 2Fh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**SW_RST_DAT_LN (sw_rst_dat_ln):** Software Reset For DAT Line
1	0b RW	**SW_RST_CMD_LN (sw_rst_cmd_ln):** Software Reset For CMD Line
0	0b RW	**SW_RST_ALL (sw_rst_all):** Software Reset For All

3.9.20 Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h

Normal Interrupt Status Register

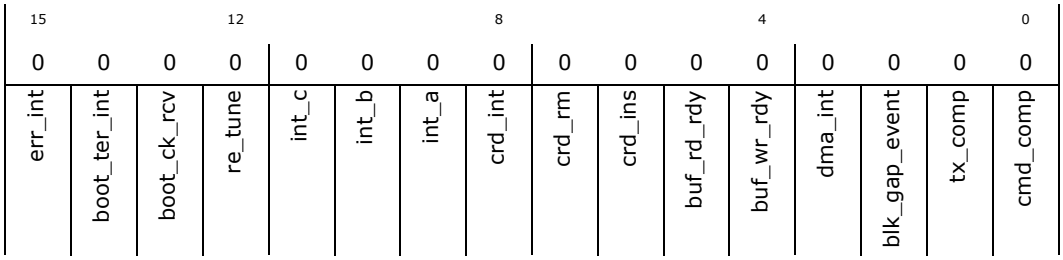
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NML_INT_STATUS: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RO	**ERR_INT (err_int):** Error Interrupt
14	0b RW/1C	**BOOT_TER_INT (boot_ter_int):** boot ter int
13	0b RW/1C	**BOOT_ACK_RCV (boot_ck_rcv):** boot ack rcv
12	0b RO	**RE_TUNE (re_tune):** re tuning event
11	0b RO	**INT_C (int_c):** int c
10	0b RO	**INT_B (int_b):** int b
9	0b RO	**INT_A (int_a):** int a
8	0b RO	**CRD_INT (crd_int):** Card Interrupt
7	0b RW/1C	**CRD_RM (crd_rm):** Card Removal
6	0b RW/1C	**CRD_INS (crd_ins):** Card Insertion
5	0b RW/1C	**BUF_RD_RDY (buf_rd_rdy):** Buffer Read Ready
4	0b RW/1C	**BUF_WR_RDY (buf_wr_rdy):** Buffer Write Ready
3	0b RW/1C	**DMA_INT (dma_int):** DMA Interrupt
2	0b RW/1C	**BLK_GAP_EVENT (blk_gap_event):** Block Gap Event
1	0b RW/1C	**TX_COMP (tx_comp):** Transfer Complete
0	0b RW/1C	**CMD_COMP (cmd_comp):** Command Complete

3.9.21 Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h

Error Interrupt Status Register

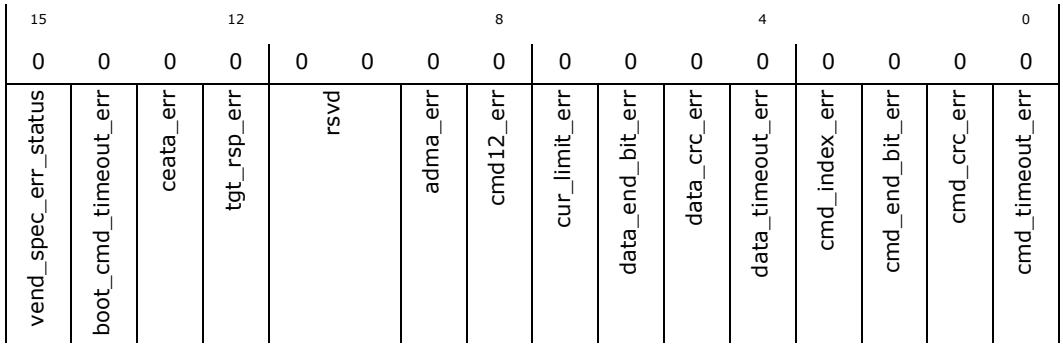
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_STATUS: [BAR] + 32h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**VEND_SPEC_ERR_STATUS (vend_spec_err_status):** Vendor Specific Error Status
14	0b RW	**BOOT_CMD_TIMEOUT_ERR (boot_cmd_timeout_err):** Occur if the boot are access command is issued to the agent which has no permission to access the boot area.
13	0b RW	**CEATA_ERR (ceata_err):** Occurs when ATA command termination has occurred due to an error condition the device has encountered.
12	0b RW	**TGT_RSP_ERR (tgt_rsp_err):** Occurs when detecting ERROR in m_hresp(dma transaction)
11:10	0h RO	**RSVD (rsvd):** Reserved
9	0b RW	**ADMA_ERR (adma_err):** ADMA Error
8	0b RW	**CMD12_ERR (cmd12_err):** Auto CMD12 Error
7	0b RW	**CUR_LIMIT_ERR (cur_limit_err):** Current Limit Error
6	0b RW	**DATA_END_BIT_ERR (data_end_bit_err):** Data End Bit Error
5	0b RW	**DATA_CRC_ERR (data_crc_err):** Data CRC Error
4	0b RW	**DATA_TIMEOUT_ERR (data_timeout_err):** Data Timeout Error
3	0b RW	**CMD_INDEX_ERR (cmd_index_err):** Command Index Error
2	0b RW	**CMD_END_BIT_ERR (cmd_end_bit_err):** Command End Bit Error

Bit Range	Default & Access	Description
1	0b RW	**CMD_CRC_ERR (cmd_crc_err):** Command CRC Error
0	0b RW	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Command Timeout Error

3.9.22 Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h

Normal Interrupt Status Enable

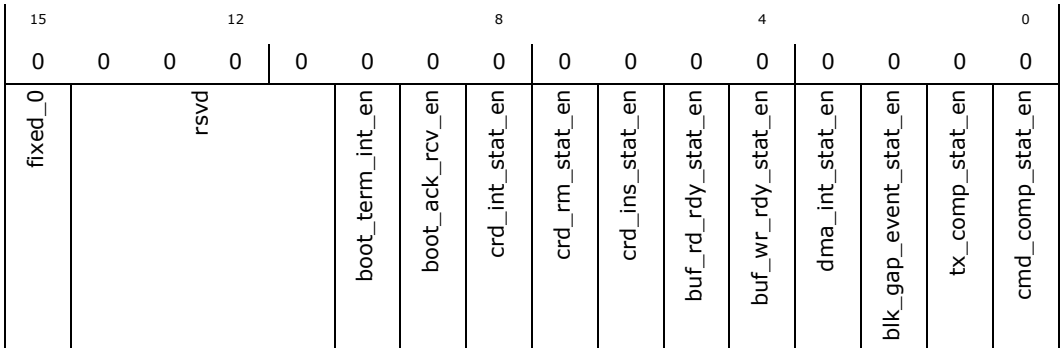
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NRM_INT_STATUS_EN: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RO	**FIXED_0 (fixed_0):** Fixed to 0
14:11	0h RO	**RSVD (rsvd):** Reserved
10	0b RW	**BOOT_TERM_INT_EN (boot_term_int_en):** 0 - Masked
9	0b RW	**BOOT_ACK_RCV_EN (boot_ack_rcv_en):** 0 -Masked
8	0b RW	**CRD_INT_STAT_EN (crd_int_stat_en):** Card Interrupt Status Enable
7	0b RW	**CRD_RM_STAT_EN (crd_rm_stat_en):** Card Removal Status Enable
6	0b RW	**CRD_INS_STAT_EN (crd_ins_stat_en):** Card Insertion Status Enable

Bit Range	Default & Access	Description
5	0b RW	**BUF_RD_RDY_STAT_EN (buf_rd_rdy_stat_en):** Buffer Read Ready Status Enable
4	0b RW	**BUF_WR_RDY_STAT_EN (buf_wr_rdy_stat_en):** Buffer Write Ready Status Enable
3	0b RW	**DMA_INT_STAT_EN (dma_int_stat_en):** DMA Interrupt Status Enable
2	0b RW	**BLK_GAP_EVENT_STAT_EN (blk_gap_event_stat_en):** Block Gap Event Status Enable
1	0b RW	**TX_COMP_STAT_EN (tx_comp_stat_en):** Transfer Complete Status Enable
0	0b RW	**CMD_COMP_STAT_EN (cmd_comp_stat_en):** Command Complete Status Enable

3.9.23 Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h

Error Interrupt Status Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_STAT_EN: [BAR] + 36h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_en	tgt_rsp_err_en	rsvd	tune_err_stat_en	adma_err_stat_en	cmd12_err_stat_en	cur_limit_err_stat_en	data_end_bit_err_stat_en	data_crc_err_stat_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Description
15:14	0b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR_EN (ceata_err_en):** 0 - masked
12	0b RW	**TGT_RSP_ERR_EN (tgt_rsp_err_en):** 0 - masked

Bit Range	Default & Access	Description
11	0b RO	**RSVD (rsvd):** Reserved
10	0b RW	**TUNE_ERR_STATE_EN (tune_err_stat_en):** 0 - masked
9	0b RW	**ADMA_ERR_STAT_EN (adma_err_stat_en):** ADMA Error Status Enable
8	0b RW	**CMD12_ERR_STAT_EN (cmd12_err_stat_en):** Auto CMD12 Error Status Enable
7	0b RW	**CUR_LIMIT_ERR_STAT_EN (cur_limit_err_stat_en):** Current Limit Error Status Enable
6	0b RW	**DATA_END_BIT_ERR_STAT_EN (data_end_bit_err_stat_en):** Data End Bit Error Status Enable
5	0b RW	**DATA_CRC_ERR_STAT_EN (data_crc_err_stat_en):** Data CRC Error Status Enable
4	0b RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Status Enable
3	0b RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Status Enable
2	0b RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Status Enable
1	0b RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Status Enable
0	0b RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Status Enable

3.9.24 Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h

Normal Interrupt Signal Enable Register

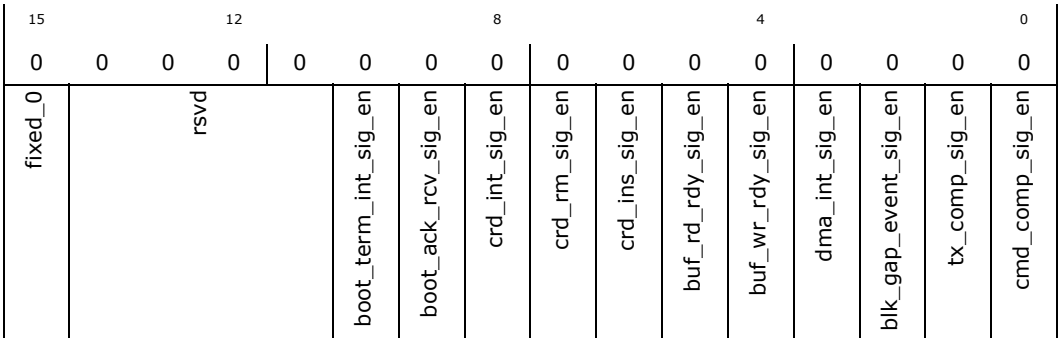
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NRM_INT_SIG_EN: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h

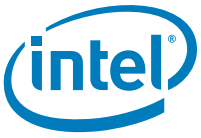


Bit Range	Default & Access	Description
15	0b RO	**FIXED_0 (fixed_0):** Fixed to 0
14:11	0h RO	**RSVD (rsvd):** Reserved
10	0b RW	**BOOT_TERM_INT_SIG_EN (boot_term_int_sig_en):** 0 - masked
9	0b RW	**BOOT_ACK_RCV_SIG_EN (boot_ack_rcv_sig_en):** 0 - masked
8	0b RW	**CRD_INT_SIG_EN (crd_int_sig_en):** Card Interrupt Signal Enable
7	0b RW	**CRD_RM_SIG_EN (crd_rm_sig_en):** Card Removal Signal Enable
6	0b RW	**CRD_INS_SIG_EN (crd_ins_sig_en):** Card Insertion Signal Enable
5	0b RW	**BUF_RD_RDY_SIG_EN (buf_rd_rdy_sig_en):** Buffer Read Ready Signal Enable
4	0b RW	**BUF_WR_RDY_SIG_EN (buf_wr_rdy_sig_en):** Buffer Write Ready Signal Enable
3	0b RW	**DMA_INT_SIG_EN (dma_int_sig_en):** DMA Interrupt Signal Enable
2	0b RW	**BLK_GAP_EVENT_SIG_EN (blk_gap_event_sig_en):** Block Gap Event Signal Enable
1	0b RW	**TX_COMP_SIG_EN (tx_comp_sig_en):** Transfer Complete Signal Enable
0	0b RW	**CMD_COMP_SIG_EN (cmd_comp_sig_en):** Command Complete Signal Enable

3.9.25 Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah

Error Interrupt Signal Enable Register

Access Method



Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_SIG_EN: [BAR] + 3Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_sig_en	tgt_err_rsp_sig_en	rsvd	tune_err_sig	adma_err_sig_en	cmd12_err_sig_en	cur_limit_err_sig_en	data_end_bit_err_sig_en	data_crc_err_sig_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Description
15:14	0b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR_SIG_EN (ceata_err_sig_en):** 0 - masked
12	0b RW	**TGT_ERR_RSP_SIG_EN (tgt_err_rsp_sig_en):** 0 - masked
11	0b RO	**RSVD (rsvd):** Reserved
10	0b RW	**TUNE_ERR_SIG (tune_err_sig):** 0 - masked
9	0b RW	**ADMA_ERR_SIG_EN (adma_err_sig_en):** ADMA Error Signal Enable
8	0b RW	**CMD12_ERR_SIG_EN (cmd12_err_sig_en):** Auto CMD12 Error Signal Enable
7	0b RW	**CUR_LIMIT_ERR_SIG_EN (cur_limit_err_sig_en):** Current Limit Error Signal Enable
6	0b RW	**DATA_END_BIT_ERR_SIG_EN (data_end_bit_err_sig_en):** Data End Bit Error Signal Enable
5	0b RW	**DATA_CRC_ERR_SIG_EN (data_crc_err_sig_en):** Data CRC Error Signal Enable
4	0b RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Signal Enable
3	0b RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Signal Enable
2	0b RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Signal Enable

Bit Range	Default & Access	Description
1	0b RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Signal Enable
0	0b RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Signal Enable

3.9.26 Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch

Auto CMD12 Error Status Register and Host control 2 Register

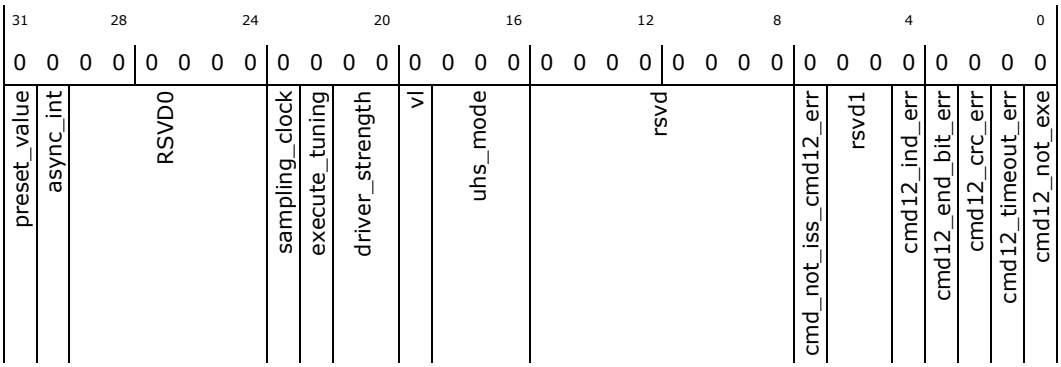
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CMD12_ERR_STAT_HOST_CTRL_2: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**PRESET_VALUE (preset_value):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic This bit enables the functions defined in the Preset Value registers. 1 Automatic Selection by Preset Value are Enabled 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.

Bit Range	Default & Access	Description
30	0b RW	**ASYNC_INT (async_int):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 1 Enabled 0 Disabled
29:24	0b RO	**RSVD0:** Reserved
23	0b RW	**SAMPLING_CLOCK (sampling_clock):** This bit is set by tuning procedure when Execute Tuning is cleared
22	0b RW/AC	**EXECUTE_TUNING (execute_tuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 1 Execute Tuning 0 Not Tuned or Tuning Completed
21:20	0b RW	**DRIVER_STRENGTH (driver_strength):** Host Controller output driver in 1.8V signaling is selected by this bit
19	0b RW	**VL (vl):** This bit controls voltage regulator for I/O cell
18:16	0b RW	**UHS_MODE (uhs_mode):** This field is used to select one of UHS-I modes
15:8	0h RO	**RSVD (rsvd):** Reserved
7	0b RO	**CMD_NOT_ISS_CMD12_ERR (cmd_not_iss_cmd12_err):** Command Not Issued By Auto CMD12 Error
6:5	0h RO	**RSVD1 (rsvd1):** Reserved
4	0b RO	**CMD12_IND_ERR (cmd12_ind_err):** Auto CMD12 Index Error
3	0b RO	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Auto CMD12 End Bit Error
2	0b RO	**CMD12_CRC_ERR (cmd12_crc_err):** Auto CMD12 CRC Error
1	0b RO	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Auto CMD12 Timeout Error
0	0b RO	**CMD12_NOT_EXE (cmd12_not_exe):** Auto CMD12 Not Executed

3.9.27 Capabilities Register (CAPABILITIES)—Offset 40h

Capabilities Register

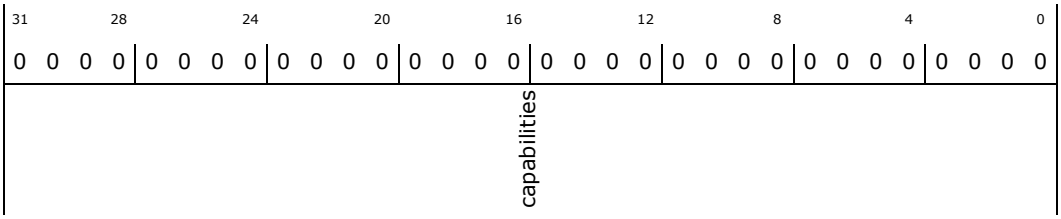
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITIES: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**capabilities:** capabilities

3.9.28 Capabilities Register 2 (CAPABILITIES_2)—Offset 44h

Capabilities Register 2

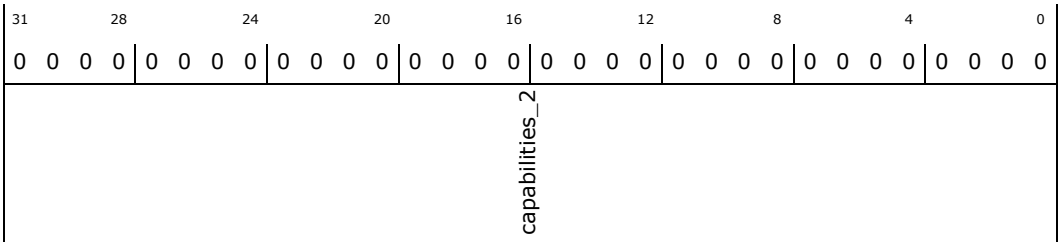
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITIES_2: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**capabilities_2:** capabilities 2

3.9.29 Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h

These registers indicate maximum current capability for each voltage

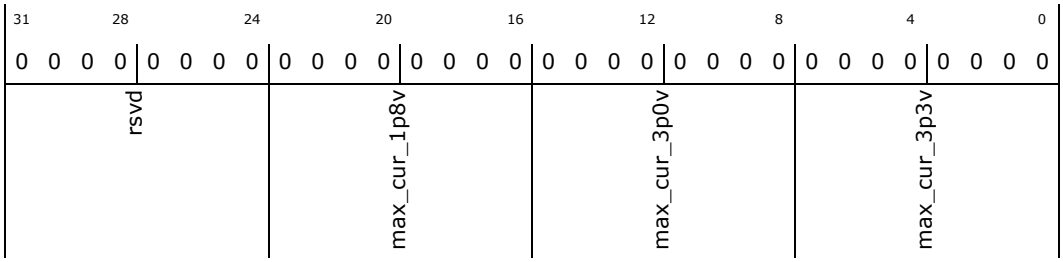
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MAX_CUR_CAP: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**RSVD (rsvd):** Reserved
23:16	00h RO	**MAX_CUR_1p8V (max_cur_1p8v):** Maximum Current for 1.8V
15:8	00h RO	**MAX_CUR_3p0V (max_cur_3p0v):** Maximum Current for 3.0V
7:0	00h RO	**MAX_CUR_3p3V (max_cur_3p3v):** Maximum Current for 3.3V

3.9.30 Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h

Force Event Register for Auto CMD12 Error Status

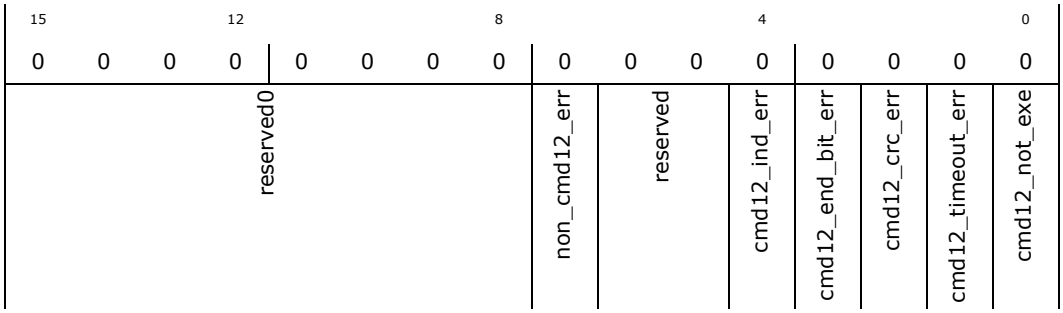
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

FORCE_EVENT_CMD12_ERR_STAT: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**Reserved0 (reserved0):** Reserved
7	0b RW	**NON_CMD12_ERR (non_cmd12_err):** Force Event for Command Not Issued By Auto CMD12 Error :
6:5	00b RO	**Reserved (reserved):** Reserved
4	0b RW	**CMD12_IND_ERR (cmd12_ind_err):** Force Event for Auto CMD12 Index Error
3	0b RW	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Force Event for Auto CMD12 End Bit Error
2	0b RW	**CMD12_CRC_ERR (cmd12_crc_err):** Force Event for Auto CMD12 CRC Error
1	0b RW	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Force Event for Auto CMD12 Timeout Error
0	0b RW	**CMD12_NOT_EXE (cmd12_not_exe):** Force Event for Auto CMD12 Not Executed

3.9.31 Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h

Force Event Register for Error Interrupt Status

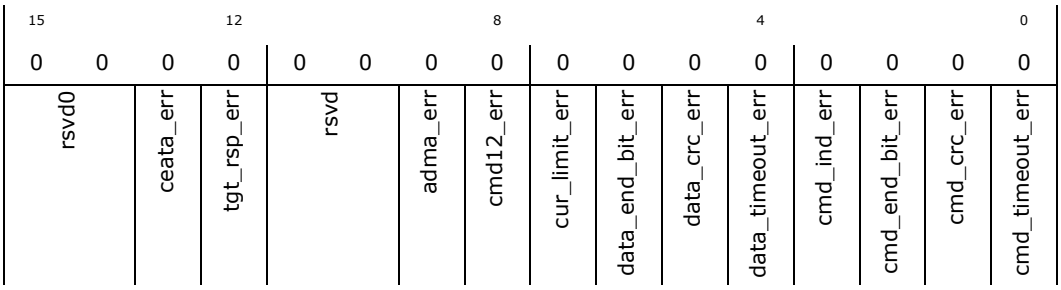
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

FORCE_EVENT_ERR_INT_STAT: [BAR] + 52h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:14	00b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR (ceata_err):** Force Event for CEATA error

Bit Range	Default & Access	Description
12	0b RW	**TGT_RSP_ERR (tgt_rsp_err):** Force Event for Target Response Error
11:10	0h RO	**RSVD (rsvd):** Reserved
9	0b RW	**ADMA_ERR (adma_err):** Force Event for ADMA Error
8	0b RW	**CMD12_ERR (cmd12_err):** Force Event for Auto CMD12 Error
7	0b RW	**CUR_LIMIT_ERR (cur_limit_err):** Force Event for Current Limit Error
6	0b RW	**DATA_END_BIT_ERR (data_end_bit_err):** Force Event for Data End Bit Error
5	0b RW	**DATA_CRC_ERR (data_crc_err):** Event for Data CRC Error
4	0b RW	**DATA_TIMEOUT_ERR (data_timeout_err):** Event for Data Timeout Error
3	0b RW	**CMD_IND_ERR (cmd_ind_err):** Force Event for Command Index Error
2	0b RW	**CMD_END_BIT_ERR (cmd_end_bit_err):** Force Event for Command End Bit Error
1	0b RW	**CMD_CRC_ERR (cmd_crc_err):** Force Event for Command CRC Error
0	0b RW	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Force Event for Command Timeout Error

3.9.32 ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h

ADMA Error Status Register

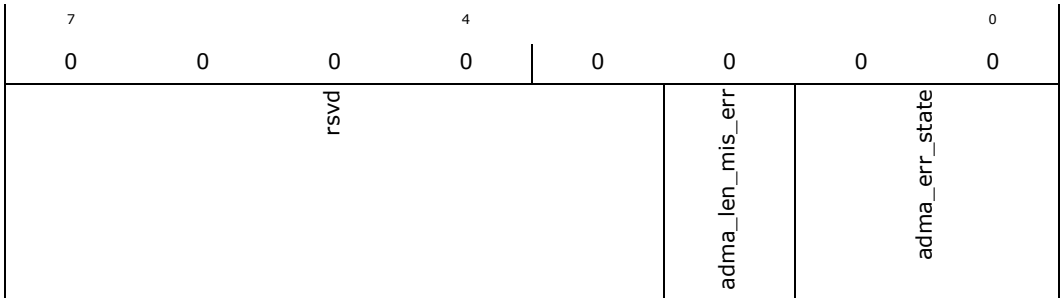
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

ADMA_ERR_STAT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RO	**ADMA_LEN_MIS_ERR (adma_len_mis_err):** ADMA Length Mismatch Error
1:0	00b RO	**ADMA_ERR_STATE (adma_err_state):** ADMA Error State

3.9.33 ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h

This register contains the physical Descriptor address used for ADMA data transfer.

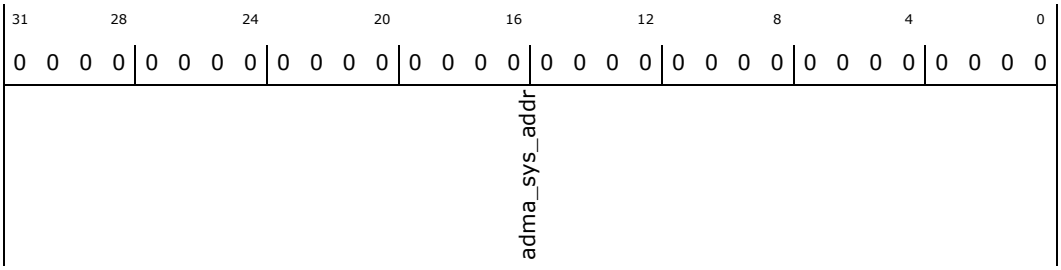
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ADMA_SYS_ADDR: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**ADMA_SYS_ADDR (adma_sys_addr):** ADMA System Address

3.9.34 Preset Values registers (PRESET_VALUE_0)—Offset 60h

Preset Values init and default speed

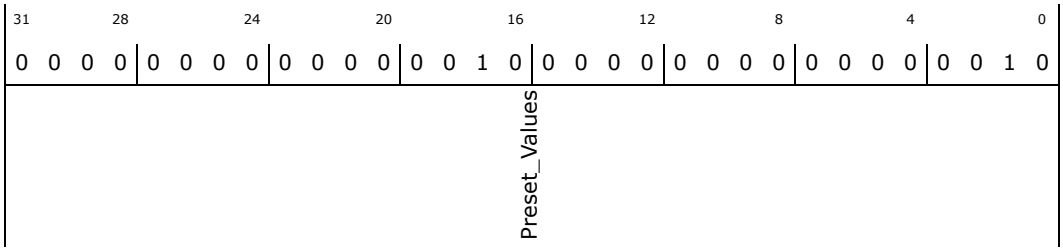
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_0: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00020002h



Bit Range	Default & Access	Description
31:0	00020002h RO	**PresetValues (Preset_Values):** Reserved.

3.9.35 Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h

Preset Values high and sdr12

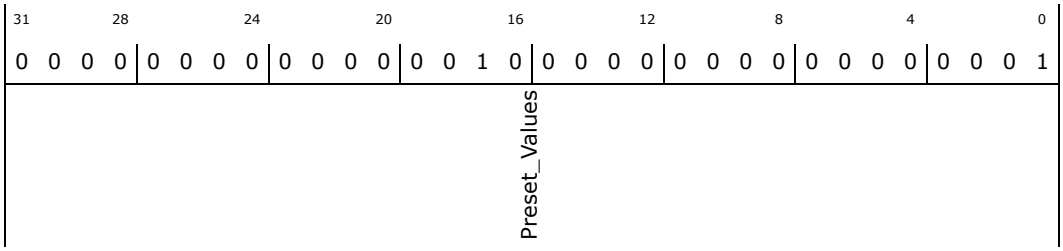
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_1: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00020001h



Bit Range	Default & Access	Description
31:0	00020001h RO	**PresetValues (Preset_Values):** Reserved.

3.9.36 Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h

Preset Values sdr25 and sdr50

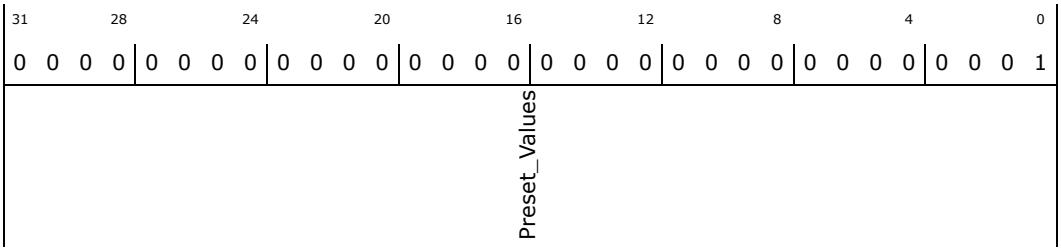
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_2: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:0	00000001h RO	**PresetValues (Preset_Values):** Reserved.

3.9.37 Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch

Preset Values sdr104 and ddr50

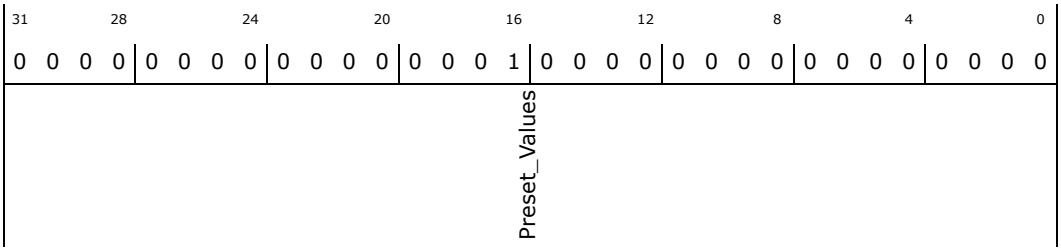
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_3: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31:0	00010000h RO	**PresetValues (Preset_Values):** Reserved.

3.9.38 BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h

BOOT_TIMEOUT_CTRL

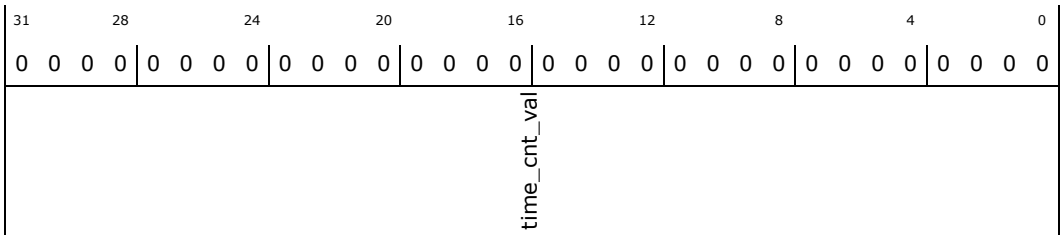
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BOOT_TIMEOUT_CTRL: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**TIME_CNT_VAL (time_cnt_val):** Boot Data Timeout Counter Value

3.9.39 DEBUG_SEL (DEBUG_SEL)—Offset 74h

Debug Selection Register

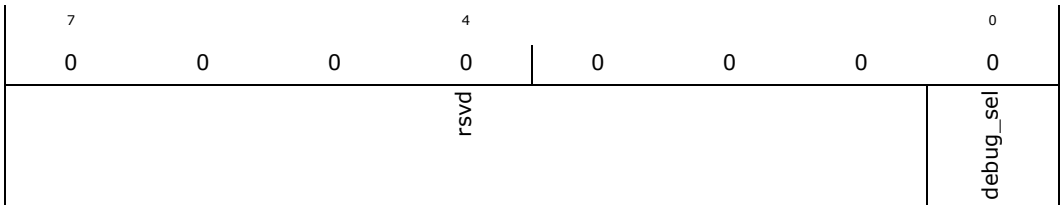
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

DEBUG_SEL: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:1	00h RO	**RSVD (rsvd):** Reserved
0	0b WO	**DEBUG_SEL (debug_sel):** 1 - cmd register, interrupt status, transmitter module, ahb_iface module and clk sdcard signals are probed out..

3.9.40 Shared Bus Control Register (SHARED_BUS)—Offset E0h

Shared Bus Control Register

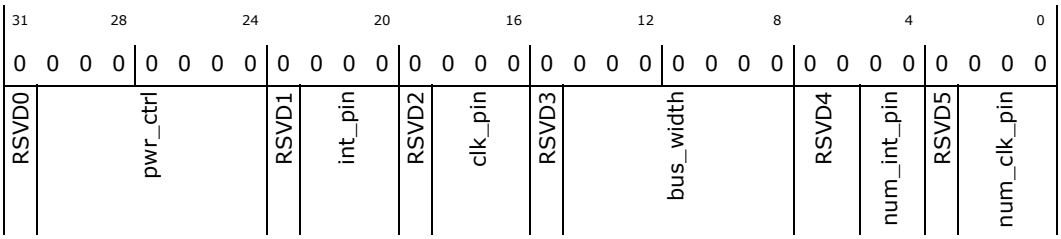
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SHARED_BUS: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**RSVD0:** Reserved
30:24	0h RW	**PWR_CTRL (pwr_ctrl):** Each bit of this field controls back-end power supply for an embedded device. Host interface voltage (VDDH) is not controlled by this field. The number of devices supported is specified by Number of Clock Pins and a maximum of 7 devices can be controlled D24 Back-end Power Control for Device 1 D25 Back-end Power Control for Device 2 D26 Back-end Power Control for Device 3 D27 Back-end Power Control for Device 4 D28 Back-end Power Control for Device 5 D29 Back-end Power Control for Device 6 D30 Back-end Power Control for Device 7 The function of each bit is defined as follows: 0 Back-end Power is Off 1 Back-end Power is Supplied Back-End power control is effective for embedded memory devices in the Sleep State that support the Sleep command (CMD14) to reduce power consumption and embedded SDIO devices when IOEx is set to 0.
23	0b RO	**RSVD1:** Reserved
22:20	0h RW	**INT_PIN (int_pin):** Interrupt pin inputs are enabled by this field. Enable of unsupported interrupt pin is meaningless. 000b Interrupt is detected by Interrupt Cycle xx1b INT_A is Enabled x1xb INT_B is Enabled 1xxb INT_C is Enabled
19	0b RO	**RSVD2:** Reserved
18:16	0h RW	**CLK_PIN (clk_pin):** One of clock pin outputs is selected by this field. Select of unsupported clock pin is meaningless. Refer to Figure 2-38 for the timing of clock outputs. 000b Clock Pins are Disabled 001b CLK[1] is Selected 010b CLK[2] is Selected .... 111b CLK[7] is Selected
15	0b RO	**RSVD3:** Reserved

Bit Range	Default & Access	Description
14:8	0h RO	**BUS_WIDTH (bus_width):** Shared bus supports mixing of 4-bit and 8-bit bus width devices. Each bit of this field specifies the bus width for each embedded device. The number of devices supported is specified by Number of Clock Pins and a maximum of 7 devices are supported.This field is effective when multiple devices are connected to a shared bus (Slot Type is set to 10b in the Capabilities register). In the other case, Extended Data Transfer Width in the Host Control 1 register is used to select 8-bit bus width. As use of 1-bit mode is not intended for shared bus, Data Transfer Width in the Host Control 1 register should be set to 1.D08 - Bus width preset for Device 1 D09 - Bus width preset for Device 2 D10 - Bus width preset for Device 3 D11 - Bus width preset for Device 4 D12 - Bus width preset for Device 5 D13 - Bus width preset for Device 6 D14 - Bus width preset for Device 7 The function of each bit is defined as follows: 0 - 4 bit bus width mode 1 - 8 bit bus width mode
7:6	0b RO	**RSVD4:** Reserved
5:4	0h RO	**NUM_INT_PIN (num_int_pin):** This field indicates support of interrupt input pins for shared bus system.Three asynchronous interrupt pins are defined, INT_A#, INT_B# and INT_C#. Which interrupt pin is used is determined by the system. Each one is driven by open drain and then wired or connection is possible. 00b Interrupt Input Pin is Not Supported 01b INTA is Supported 10b INTA and INTB are Supported 11b INTA, INTB and INTC are Supported
3	0b RO	**RSVD5:** Reserved
2:0	0h RO	**NUM_CLK_PIN (num_clk_pin):** This field indicates support of clock pins to select one of devices for shared bus system. Up to 7 clock pins can be supported.Shared bus is supported by specific system. Then Standard Host Driver does not support control of these clock pins. 000b Shared bus is not supported 001b 1 SDCLK pin is supported 010b 2 SDCLK pins are supported .... 111b 7 SDCLK pins are supported

3.9.41 SPI_INT_SUP (SPI_INT_SUP)—Offset F0h

SPI_INT_SUP

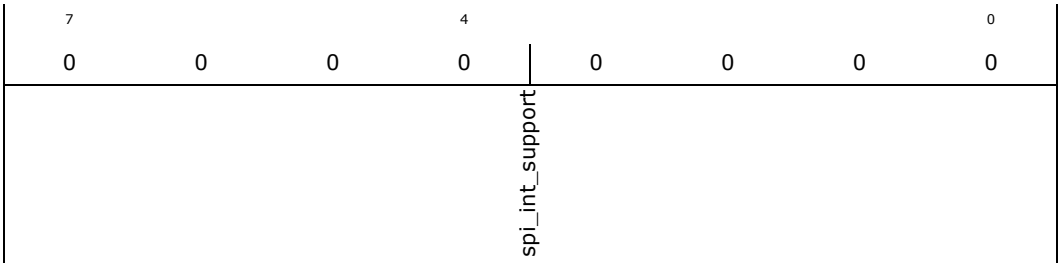
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SPI_INT_SUP: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**SPI_INT_SUPPORT (spi_int_support):** This bit is set to indicate the assertion assertion of interrupts in the SPI mode at any time, irrespective of the status of thecard select (CS) line. If this bit is zero, then SDIO card can only assert the interrupt line in the SPI mode when the CS line is asserted.

3.9.42 Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh

Slot Interrupt Status Register

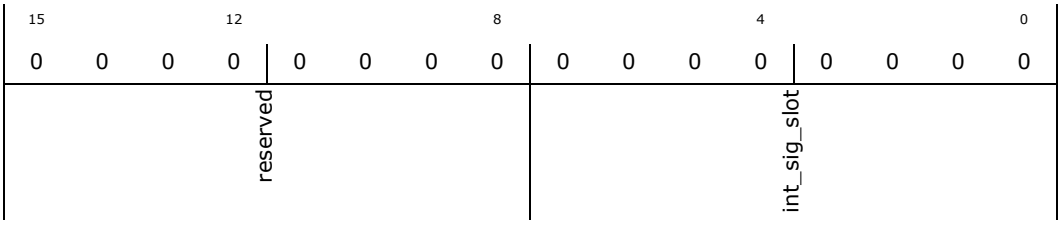
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

SLOT_INT_STAT: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**Reserved (reserved):** Reserved
7:0	00h RO	**INT_SIG_SLOT (int_sig_slot):** Interrupt Signal For Each Slot

3.9.43 Host Controller Version Register (HOST_CTRL_VER)—Offset FEh

Host Controller Version Register

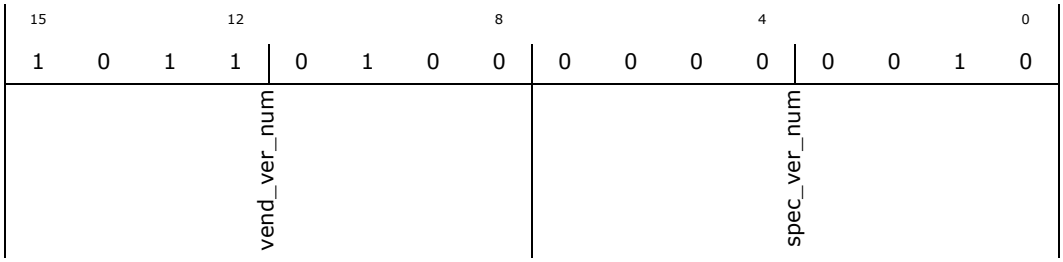
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

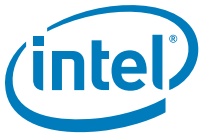
HOST_CTRL_VER: [BAR] + FEh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: B402h



Bit Range	Default & Access	Description
15:8	b4h RO	**VEND_VER_NUM (vend_ver_num):** Vendor Version Number
7:0	02h RO	**SPEC_VER_NUM (spec_ver_num):** Version Number



3.10 SDIO PCI Configuration Registers

Table 18. Summary of SDIO PCI Configuration Registers—0/17/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 1517	00000000h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 1518	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 1519	00000000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 1520	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 1520	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 1521	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 1522	00000000h
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 1522	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 1523	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 1523	00000100h
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 1524	48030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 1525	00000008h
A0h	4	"reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h" on page 1525	00000000h
A4h	4	"reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h" on page 1526	00000000h
A8h	4	"reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h" on page 1526	00000000h
ACh	4	"reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh" on page 1527	00000000h
C0h	4	"reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h" on page 1527	00000000h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 1528	00000000h

3.10.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

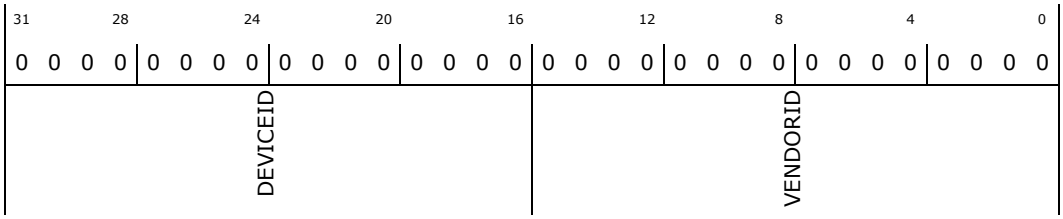
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:17, F:0] + 0h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**DEVICEID:** Reserved.
15:0	0000h RO	**VENDORID:** Reserved.

3.10.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

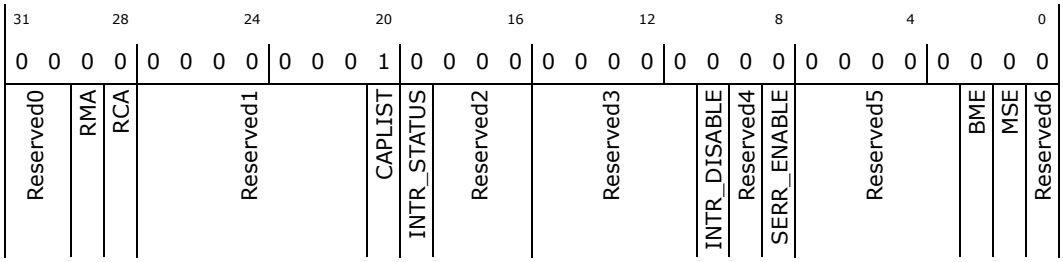
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:17, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** Reserved.
29	0h RW/1C	**RMA:** Reserved.
28	0h RW/1C	**RCA:** Reserved.
27:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**CAPLIST:** Reserved.
19	0h RO	**INTR_STATUS:** Reserved.

Bit Range	Default & Access	Description
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**INTR_DISABLE:** Reserved.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR_ENABLE:** Reserved.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**BME:** Reserved.
1	0h RW	**MSE:** Reserved.
0	0h RO	**Reserved6:** Reserved.

3.10.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

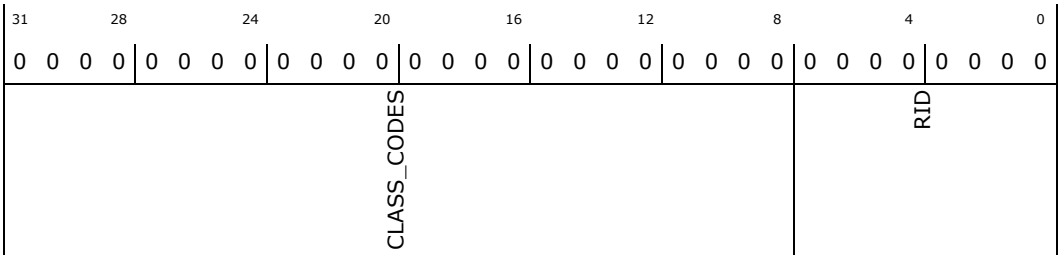
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:17, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**CLASS_CODES:** Reserved.
7:0	00h RO	**RID:** Reserved.

3.10.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

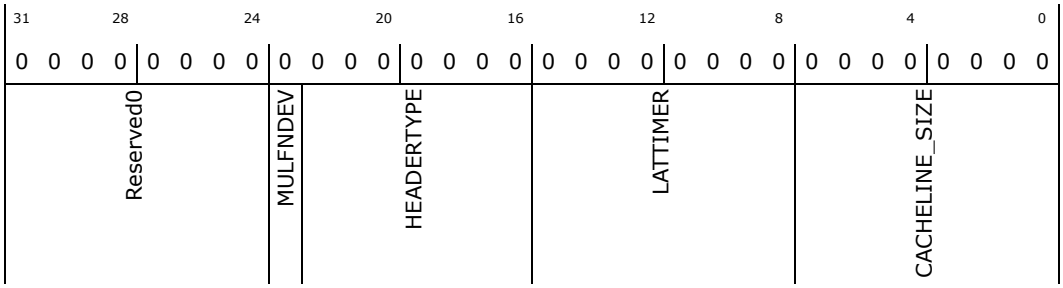
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:17, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	0h RO	**MULFNDEV:** Reserved.
22:16	00h RO	**HEADERTYPE:** Reserved.
15:8	00h RO	**LATTIMER:** Reserved.
7:0	00h RW	**CACHELINE_SIZE:** Reserved.

3.10.5 reg_BAR_type (BAR)—Offset 10h

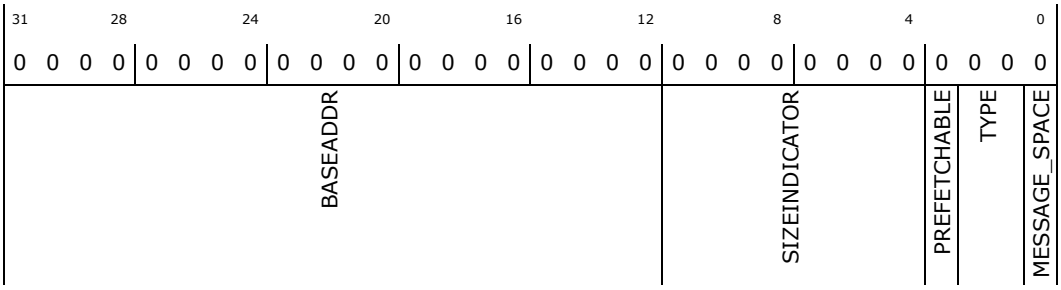
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Reserved.
11:4	00h RO	**SIZEINDICATOR:** Reserved.
3	0h RO	**PREFETCHABLE:** Reserved.
2:1	0h RO	**TYPE:** Reserved.
0	0h RO	**MESSAGE_SPACE:** Reserved.

3.10.6 reg_BAR1_type (BAR1)—Offset 14h

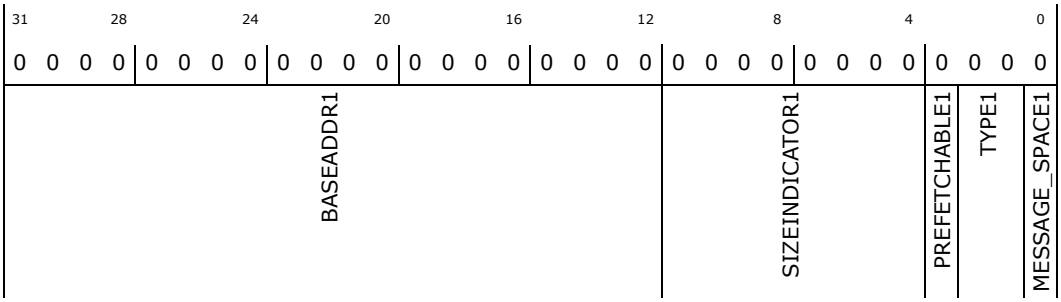
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:17, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** Reserved.
11:4	00h RO	**SIZEINDICATOR1:** Reserved.

Bit Range	Default & Access	Description
3	0h RO	**PREFETCHABLE1:** Reserved.
2:1	0h RO	**TYPE1:** Reserved.
0	0h RO	**MESSAGE_SPACE1:** Reserved.

3.10.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

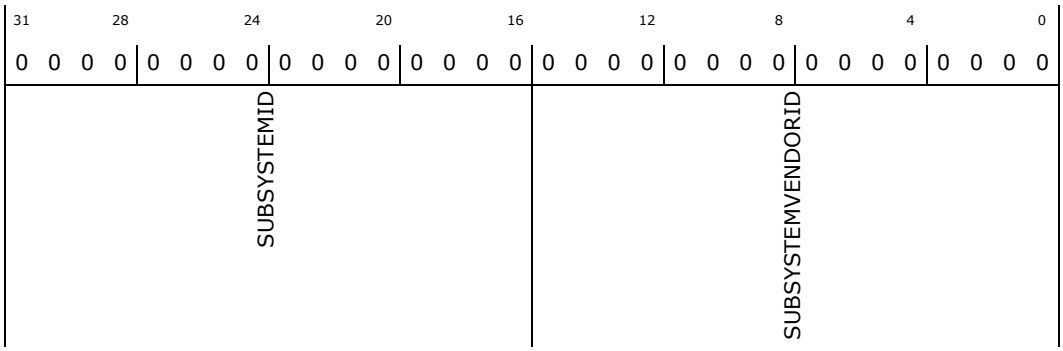
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:17, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Reserved.
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Reserved.

3.10.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

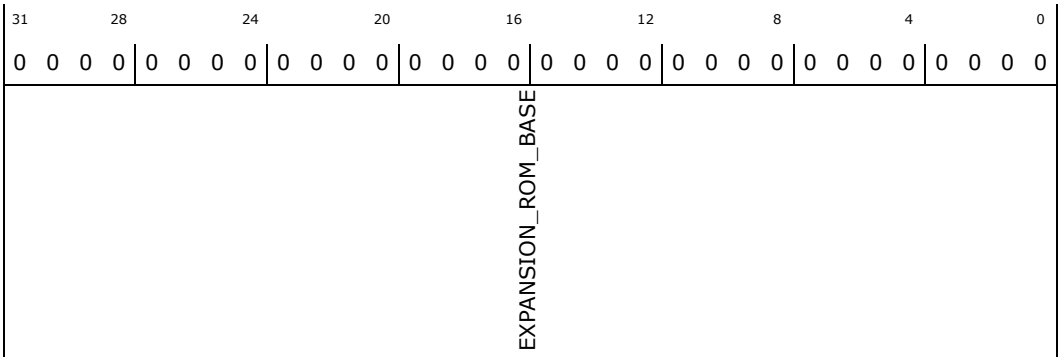
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:17, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

3.10.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

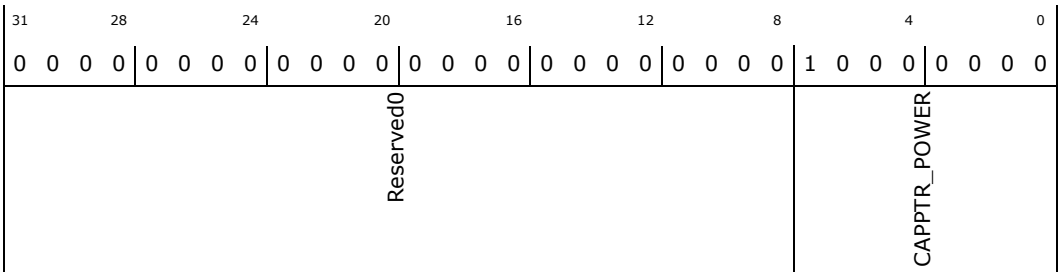
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:17, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	80h RO	**CAPPTR_POWER:** Reserved.

3.10.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

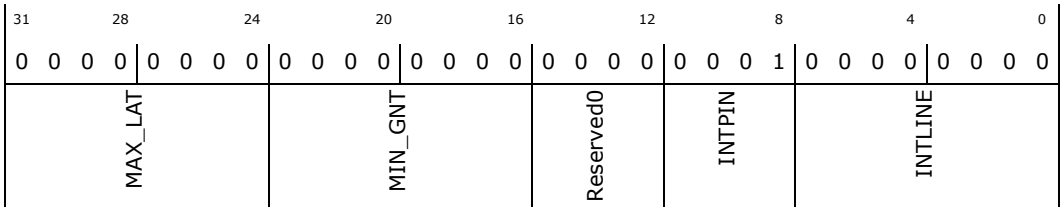
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:17, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Reserved.
23:16	00h RO	**MIN_GNT:** Reserved.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**INTPIN:** Reserved.
7:0	00h RW	**INTLINE:** Reserved.

3.10.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

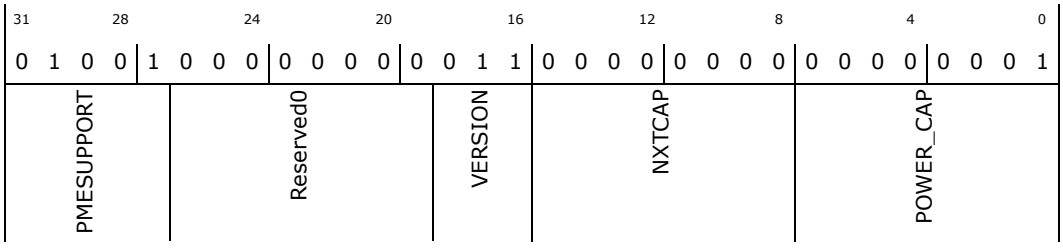
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:17, F:0] + 80h

Default: 48030001h



Bit Range	Default & Access	Description
31:27	09h RO	**PMESUPPORT:** Reserved.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**VERSION:** Reserved.

Bit Range	Default & Access	Description
15:8	00h RO	**NXTCAP:** Reserved.
7:0	01h RO	**POWER_CAP:** Reserved.

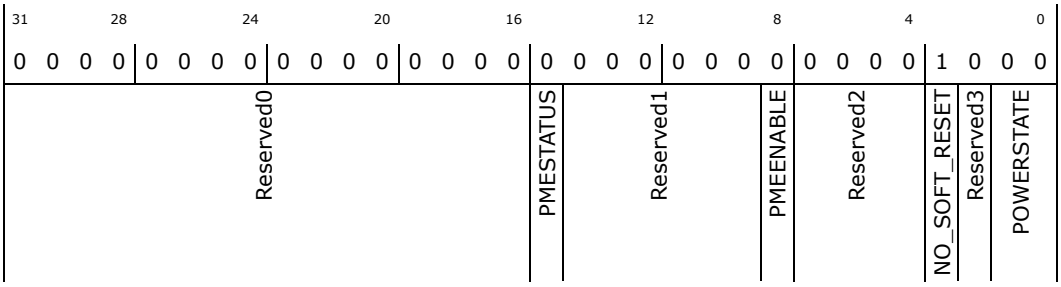
3.10.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:17, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PMESTATUS:** Reserved.
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PMEENABLE:** Reserved.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**NO_SOFT_RESET:** Reserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**POWERSTATE:** Reserved.

3.10.13 reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h

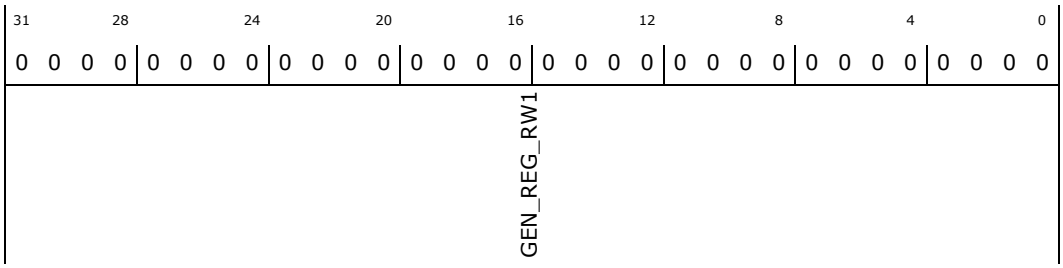
General Purpose Read Write Register1

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

GEN_REGRW1: [B:0, D:17, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW1:** capabilities over-ride for the sd/sdio/emmc host controller (bits 31:0)

3.10.14 reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h

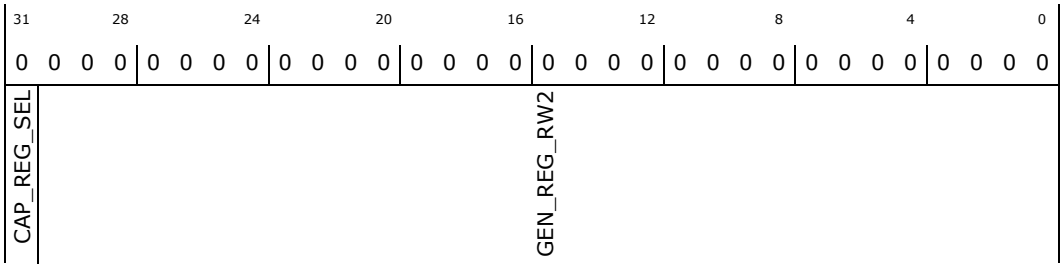
General Purpose Read Write Register2

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

GEN_REGRW2: [B:0, D:17, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**CAP_REG_SEL:** select if the capability will come from the GEN PCI register or from a hard wire
30:0	0h RW	**GEN_REG_RW2:** capabilities over-ride for the sd/sdio/emmc host controller (bits 62:32)

3.10.15 reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h

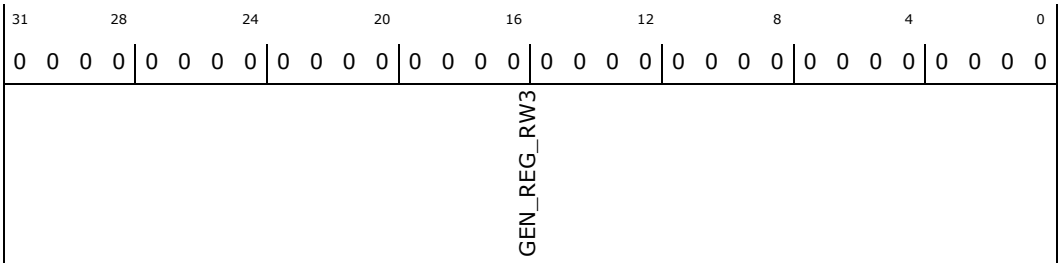
General Purpose Read Write Register3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW3: [B:0, D:17, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW3:** Reserved.

3.10.16 reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh

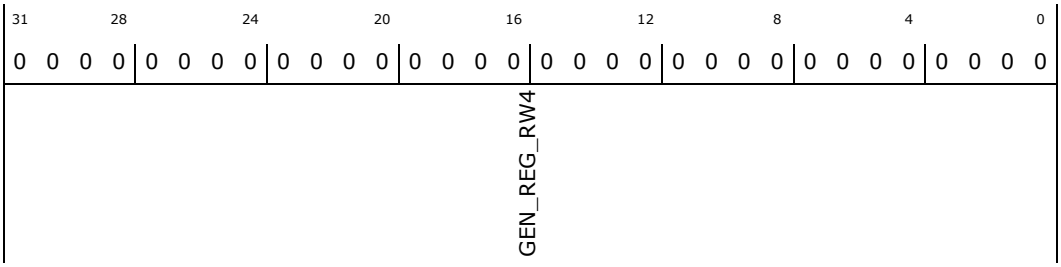
General Purpose Read Write Register4

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW4: [B:0, D:17, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW4:** Reserved.

3.10.17 reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h

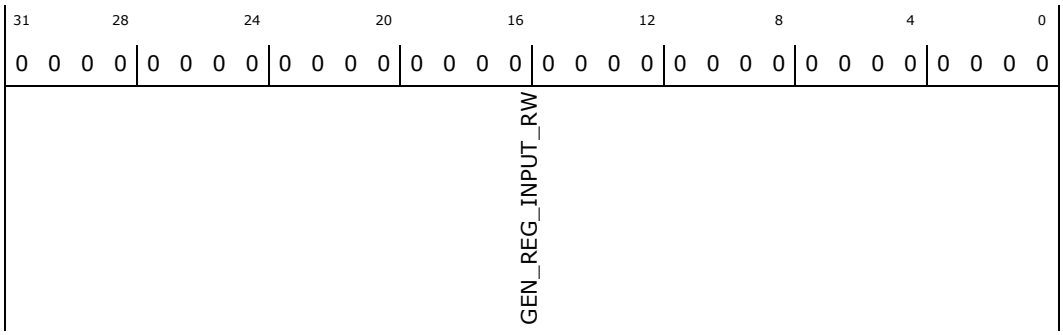
General Purpose Input Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_INPUT_REGRW: [B:0, D:17, F:0] + C0h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**GEN_REG_INPUT_RW:** Reserved.

3.10.18 reg_MANID_type (MANID)—Offset F8h

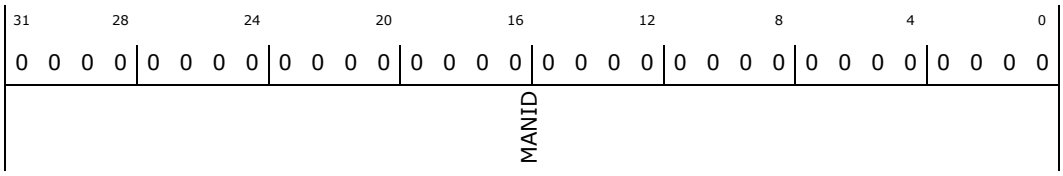
Manufacturers ID

Access Method

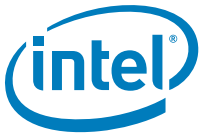
Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:17, F:0] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**MANID:** Reserved.



3.11 SDIO Memory Mapped IO Registers

Table 19. Summary of SDIO Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"SDMA System Address Register (SYS_ADR)—Offset 0h" on page 1530	00000000h
4h	2	"Block Size Register (BLK_SIZE)—Offset 4h" on page 1531	0000h
6h	2	"Block Count Register (BLK_COUNT)—Offset 6h" on page 1532	0000h
8h	4	"Argument Register (ARGUMENT)—Offset 8h" on page 1533	00000000h
Ch	2	"Transfer Mode Register (TX_MODE)—Offset Ch" on page 1533	0000h
Eh	2	"Command Register (CMD)—Offset Eh" on page 1534	0000h
10h	4	"Response Register0 (RESPONSE0)—Offset 10h" on page 1535	00000000h
14h	4	"Response Register2 (RESPONSE2)—Offset 14h" on page 1536	00000000h
18h	4	"Response Register4 (RESPONSE4)—Offset 18h" on page 1536	00000000h
1Ch	4	"Response Register6 (RESPONSE6)—Offset 1Ch" on page 1537	00000000h
20h	4	"Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h" on page 1538	00000000h
24h	4	"Present State Register (PRE_STATE)—Offset 24h" on page 1538	1FFF0000h
28h	1	"Host Control Register (HOST_CTL)—Offset 28h" on page 1539	00h
29h	1	"Power Control Register (PWR_CTL)—Offset 29h" on page 1540	00h
2Ah	1	"Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah" on page 1541	00h
2Bh	1	"Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh" on page 1542	00h
2Ch	2	"Clock Control Register (CLK_CTL)—Offset 2Ch" on page 1542	0000h
2Eh	1	"Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh" on page 1543	00h
2Fh	1	"Software Reset Register (SW_RST)—Offset 2Fh" on page 1544	00h
30h	2	"Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h" on page 1544	0000h
32h	2	"Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h" on page 1545	0000h
34h	2	"Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h" on page 1547	0000h
36h	2	"Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h" on page 1548	0000h
38h	2	"Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h" on page 1549	0000h
3Ah	2	"Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah" on page 1550	0000h
3Ch	4	"Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch" on page 1552	00000000h
40h	4	"Capabilities Register (CAPABILITIES)—Offset 40h" on page 1553	00000000h
44h	4	"Capabilities Register 2 (CAPABILITIES_2)—Offset 44h" on page 1554	00000000h

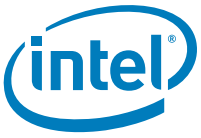


Table 19. Summary of SDIO Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
48h	4	"Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h" on page 1554	00000000h
50h	2	"Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h" on page 1555	0000h
52h	2	"Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h" on page 1556	0000h
54h	1	"ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h" on page 1557	00h
58h	4	"ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h" on page 1558	00000000h
60h	4	"Preset Values registers (PRESET_VALUE_0)—Offset 60h" on page 1558	00020002h
64h	4	"Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h" on page 1559	00020001h
68h	4	"Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h" on page 1559	00000001h
6Ch	4	"Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch" on page 1560	00010000h
70h	4	"BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h" on page 1560	00000000h
74h	1	"DEBUG_SEL (DEBUG_SEL)—Offset 74h" on page 1561	00h
E0h	4	"Shared Bus Control Register (SHARED_BUS)—Offset E0h" on page 1561	00000000h
F0h	1	"SPI_INT_SUP (SPI_INT_SUP)—Offset F0h" on page 1563	00h
FCh	2	"Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh" on page 1564	0000h
FEh	2	"Host Controller Version Register (HOST_CTRL_VER)—Offset FEh" on page 1564	B402h

3.11.1 SDMA System Address Register (SYS_ADR)—Offset 0h

This register contains the physical system memory address used for DMA transfers

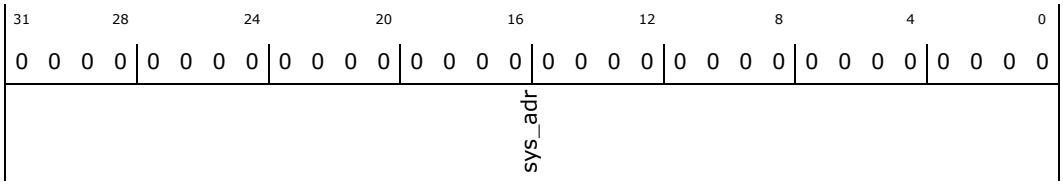
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SYS_ADR: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**SYS_ADR (sys_adr):** SDMA System Address This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register.

3.11.2 Block Size Register (BLK_SIZE)—Offset 4h

This register is used to configure the number of bytes in a data block.

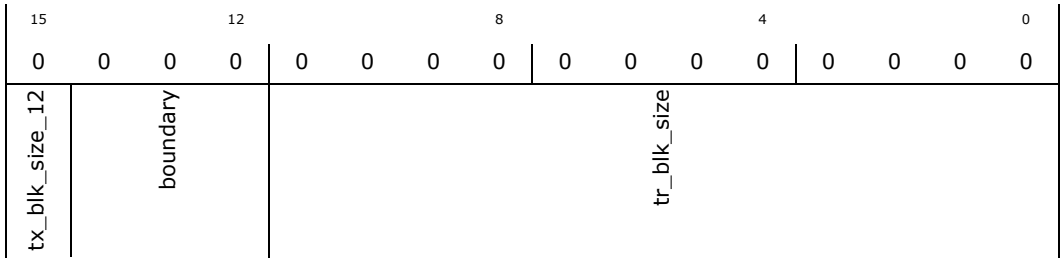
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

BLK_SIZE: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**TX_BLK_SIZE_12 (tx_blk_size_12):** Transfer Block Size 12th bit. This bit is added to support 4Kb Data block transfer.

Bit Range	Default & Access	Description
14:12	000b RW	**BOUNDARY (boundary):** Host SDMA Buffer Boundary The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. ADMA does not use this register. 000b - 4K bytes (Detects A11 carry out) 001b - 8K bytes (Detects A12 carry out) 010b - 16K Bytes (Detects A13 carry out) 011b - 32K Bytes (Detects A14 carry out) 100b - 64K bytes (Detects A15 carry out) 101b - 128K Bytes (Detects A16 carry out) 110b - 256K Bytes (Detects A17 carry out) 111b - 512K Bytes (Detects A18 carry out)
11:0	000h RW	**TR_BLK_SIZE (tr_blk_size):** Transfer Block Size This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes (Refer to Implementation Note in Section 1.7.2). It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. 0800h 2048 Bytes ??? ??? 0200h 512 Bytes 01FFh 511 Bytes ??? ??? 0004h 4 Bytes 0003h 3 Bytes 0002h 2 Bytes 0001h 1 Byte 0000h No data transfer

3.11.3 Block Count Register (BLK_COUNT)—Offset 6h

This register is used to configure the number of data blocks

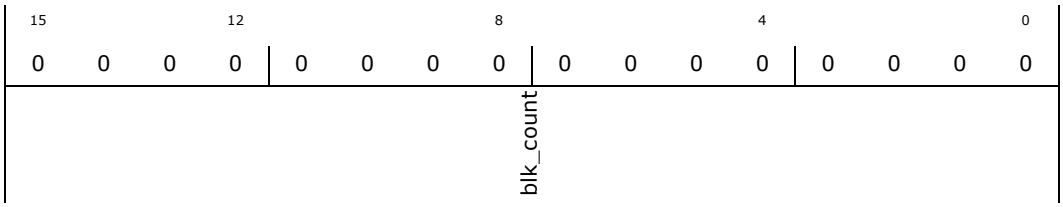
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

BLK_COUNT: [BAR] + 6h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	0000h RW	**BLK_COUNT (blk_count):** Blocks Count For Current Transfer This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers

3.11.4 Argument Register (ARGUMENT)—Offset 8h

This register contains the SD Command Argument.

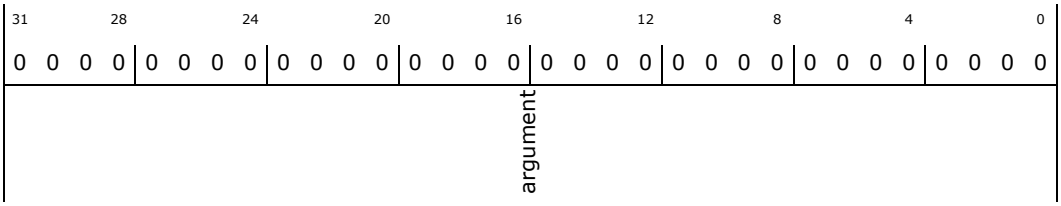
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ARGUMENT: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**ARGUMENT (argument):** Command Argument The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

3.11.5 Transfer Mode Register (TX_MODE)—Offset Ch

Transfer Mode Register

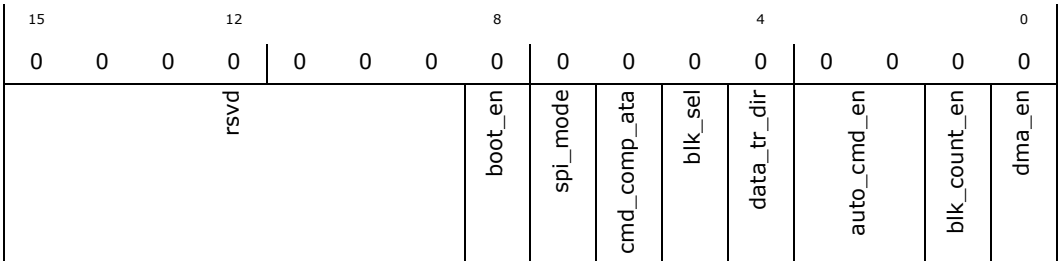
Access Method

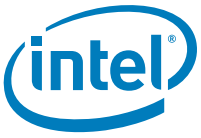
Type: Memory Mapped I/O Register (Size: 16 bits)

TX_MODE: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h





Bit Range	Default & Access	Description
15:9	00h RO	**RSVD (rsvd):** Reserved
8	0b RW	**BOOT_EN (boot_en):** To start boot operation for MMC4.3 1 - To start boot mode 0 - Stop the boot read
7	0b RW	**SPI_MODE (spi_mode):** SPI mode enable bit. 1 - SPI mode 0 - SD mode
6	0b RW	**CMD_COMP_ATA (cmd_comp_ata):** Command Completion Signal Enable for CE-ATA Device. ???1??? - Device will send command completion Signal ???0??? - Device will not send command completion Signal
5	0b RW	**BLK_SEL (blk_sel):** Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the Block Count register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block
4	0b RW	**Data_TR_Dir (data_tr_dir):** Data Transfer Direction Select This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller and it is set to 0 for all other commands. 1 Read (Card to Host) 0 Write (Host to Card)
3:2	0b RW	**AUTO_CMD_EN (auto_cmd_en):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0b RW	**BLK_COUNT_EN (blk_count_en):** Block Count Enable This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8) If ADMA2 data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table. 1 Enable 0 Disable
0	0b RW	**DMA_EN (dma_en):** DMA Enable This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the Capabilities register. One of the DMA modes can be selected by DMA Select in the Host Control register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of Command register (00Fh). 1 DMA Data transfer 0 No data transfer or Non DMA data transfer

3.11.6 Command Register (CMD)—Offset Eh

Command Register

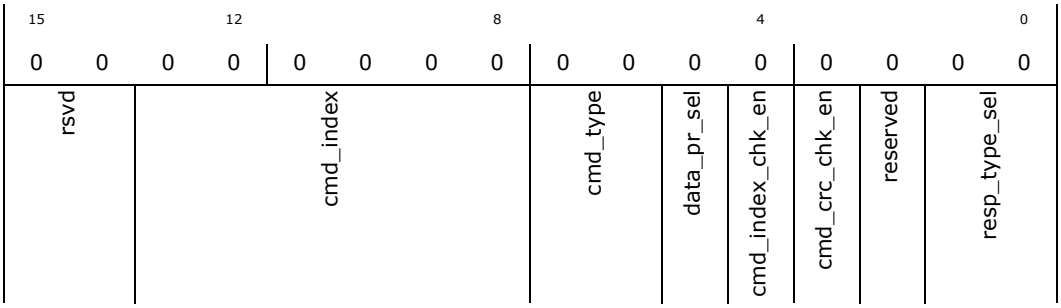
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

CMD: [BAR] + Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:14	0h RO	**RSVD (rsvd):** Reserved
13:8	0h RW	**CMD_INDEX (cmd_index):** Command Index These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.
7:6	00b RW	**CMD_TYPE (cmd_type):** Command Type
5	0b RW	**DATA_PR_SEL (data_pr_sel):** Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) (3) Resume command 1 Data Present 0 No Data Present
4	0b RW	**CMD_INDEX_CHK_EN (cmd_index_chk_en):** Command Index Check Enable If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 1 Enable 0 Disable
3	0b RW	**CMD_CRC_CHK_EN (cmd_crc_chk_en):** Command CRC Check Enable If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response. (Refer to definition in D01-00 and Table 2-10 below.) 1 Enable 0 Disable
2	0b RO	**Reserved (reserved):** Reserved
1:0	0h RW	**RESP_TYPE_SEL (resp_type_sel):** Response Type Select 00 No Response 01 Response Length 136 10 Response Length 48 11 Response Length 48 check Busy after response

3.11.7 Response Register0 (RESPONSE0)—Offset 10h

This register is used to store responses from SD cards

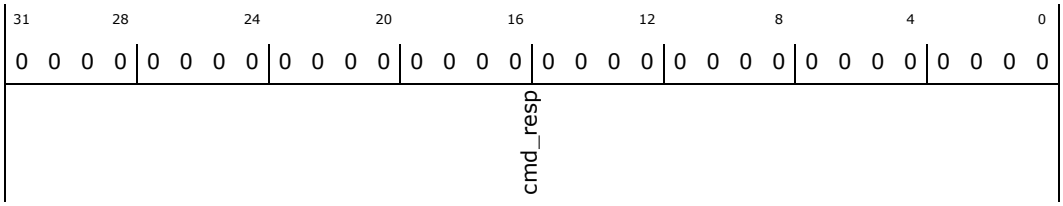
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE0: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP0 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.11.8 Response Register2 (RESPONSE2)—Offset 14h

This register is used to store responses from SD cards

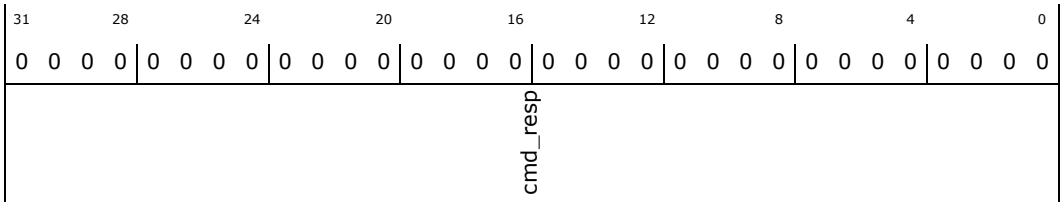
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE2: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP2 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.11.9 Response Register4 (RESPONSE4)—Offset 18h

This register is used to store responses from SD cards

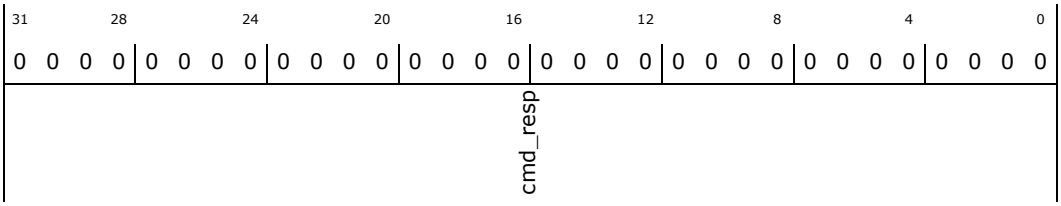
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE4: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP4 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.11.10 Response Register6 (RESPONSE6)—Offset 1Ch

This register is used to store responses from SD cards

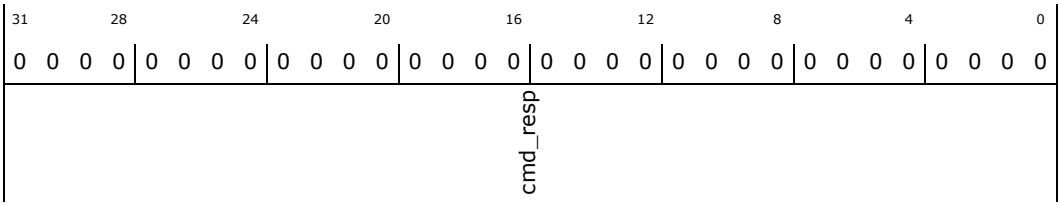
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE6: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP6 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.11.11 Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h

32-bit data port register to access internal buffer

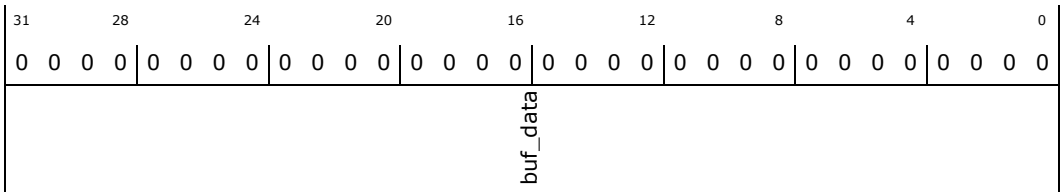
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BUF_DATA_PORT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUF_DATA (buf_data):** Buffer Data The Host Controller buffer can be accessed through this 32-bit Data Port register. Refer to 1.7

3.11.12 Present State Register (PRE_STATE)—Offset 24h

The Host Driver can get status of the Host Controller from this 32-bit read only register

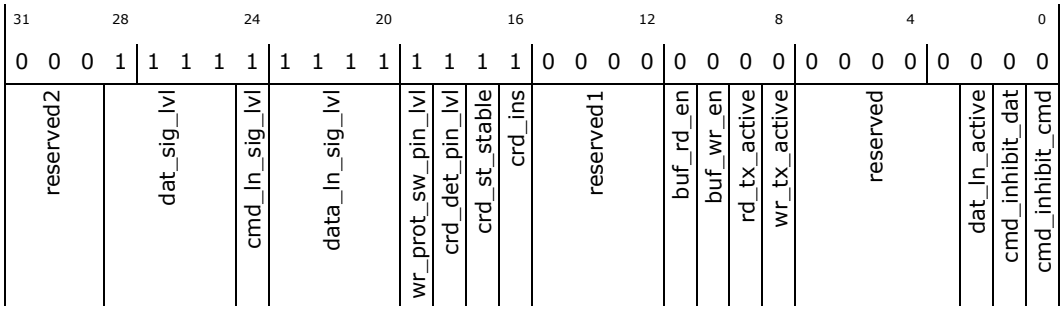
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRE_STATE: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 1FFF0000h



Bit Range	Default & Access	Description
31:29	0h RO	**Reserved2 (reserved2):** Reserved

Bit Range	Default & Access	Description
28:25	1111b RO	**DAT_SIG_LVL (dat_sig_lvl):** This status is used to check DAT line level to recover from errors, and for debugging. D28 - DAT[7] D27 - DAT[6] D26 - DAT[5] D25 - DAT[4]
24	1b RO	**CMD_LN_SIG_LVL (cmd_ln_sig_lvl):** CMD Line Signal Level This status is used to check the CMD line level to recover from errors, and for debugging.
23:20	Fh RO	**DATA_LN_SIG_LVL (data_ln_sig_lvl):** DAT[3:0] Line Signal Level This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D23 DAT[3] D22 DAT[2] D21 DAT[1] D20 DAT[0]
19	1b RO	**WR_PROT_SW_PIN_LVL (wr_prot_sw_pin_lvl):** Write Protect Switch Pin Level
18	1b RO	**CRD_DET_PIN_LVL (crd_det_pin_lvl):** Card Detect Pin Level
17	1b RO	**CRD_ST_STABLE (crd_st_stable):** Card State Stable
16	1b RO	**CRD_INS (crd_ins):** Card Inserted
15:12	0h RO	**Reserved1 (reserved1):** Reserved
11	0b RO	**BUF_RD_EN (buf_rd_en):** Buffer Read Enable
10	0b RO	**BUF_WR_EN (buf_wr_en):** Buffer Write Enable
9	0b RO	**RD_TX_ACTIVE (rd_tx_active):** Read Transfer Active
8	0b RO	**WR_TX_ACTIVE (wr_tx_active):** Write Transfer Active
7:3	00h RO	**Reserved (reserved):** Reserved
2	0b RO	**DAT_LN_ACTIVE (dat_ln_active):** DAT Line Active
1	0b RO	**CMD_INHIBIT_DAT (cmd_inhibit_dat):** Command Inhibit (DAT)
0	0b RO	**CMD_INHIBIT_CMD (cmd_inhibit_cmd):** Command Inhibit (CMD)

3.11.13 Host Control Register (HOST_CTL)—Offset 28h

Host Control Register

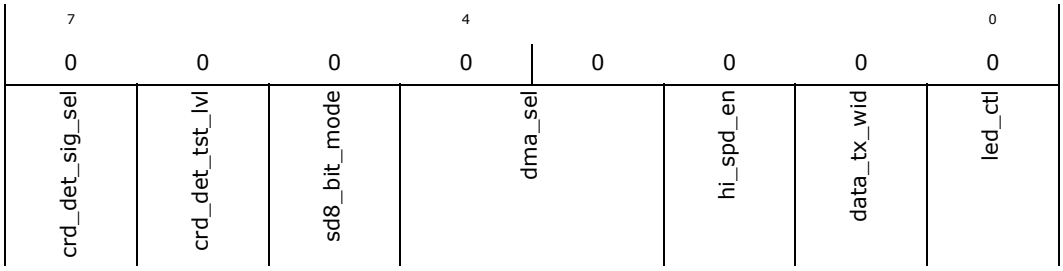
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

HOST_CTL: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RW	**CRD_DET_SIG_SEL (crd_det_sig_sel):** Card Detect Signal Selection
6	0b RW	**CRD_DET_TST_LVL (crd_det_tst_lvl):** Card Detect Test Level
5	0b RW	**SD8_BIT_MODE (sd8_bit_mode):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card.
4:3	00b RW	**DMA_SEL (dma_sel):** DMA Select
2	0b RW	**HI_SPD_EN (hi_spd_en):** High Speed Enable
1	0b RW	**DATA_TX_WID (data_tx_wid):** Data Transfer Width
0	0b RW	**LED_CTL (led_ctl):** LED Control

3.11.14 Power Control Register (PWR_CTL)—Offset 29h

Power Control Register

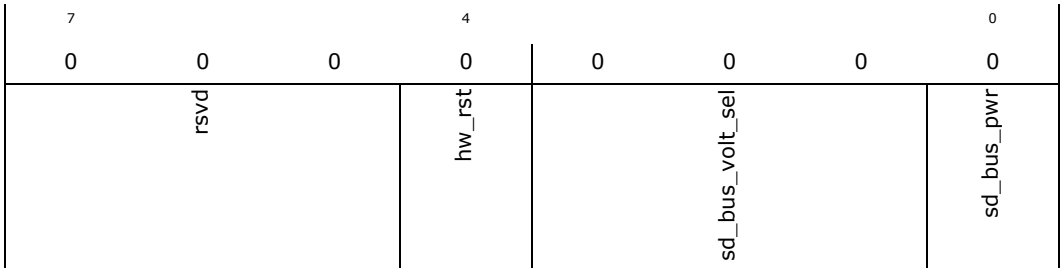
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PWR_CTL: [BAR] + 29h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:5	0h RO	**RSVD (rsvd):** Reserved
4	0b RW	**HW_rst (hw_rst):** HW reset
3:1	0h RW	**SD_BUS_VOLT_SEL (sd_bus_volt_sel):** SD Bus Voltage Select
0	0b RW	**SD_BUS_PWR (sd_bus_pwr):** SD Bus Power

3.11.15 Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah

Block Gap Control Register

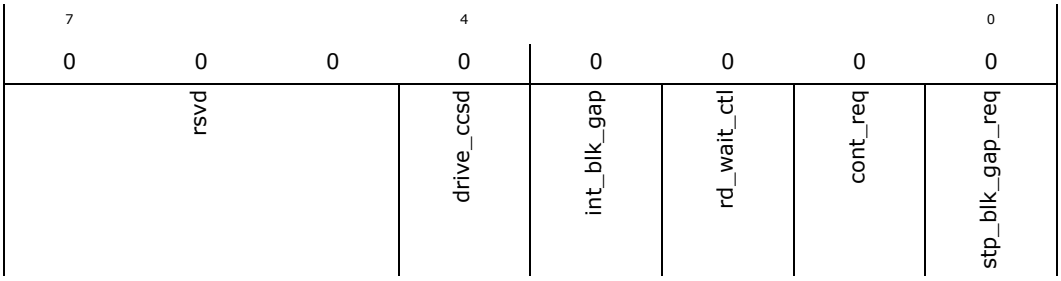
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

_BLK_GAP_CTL: [BAR] + 2Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:5	0h RO	**RSVD (rsvd):** Reserved
4	0b RW	**DRIVE_CCSD (drive_ccsd):** If the driver set this bit (change from ???0?? to ???1??), Host controller will send command completion
3	0b RW	**INT_BLK_GAP (int_blk_gap):** Interrupt At Block Gap
2	0b RW	**RD_WAIT_CTL (rd_wait_ctl):** Read Wait Control
1	0b RW	**CONT_REQ (cont_req):** Continue Request
0	0b RW	**STP_BLK_GAP_REQ (stp_blk_gap_req):** Stop At Block Gap Request

3.11.16 Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh

This register is used for wakeup event control.

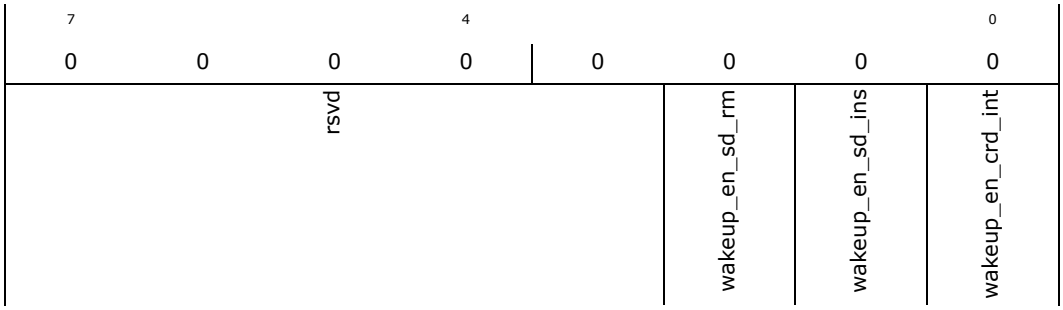
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

WAKEUP_CTL: [BAR] + 2Bh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**WAKEUP_EN_SD_RM (wakeup_en_sd_rm):** Wakeup Event Enable On SD Card Removal
1	0b RW	**WAKEUP_EN_SD_INS (wakeup_en_sd_ins):** Wakeup Event Enable On SD Card Insertion
0	0b RW	**WAKEUP_EN_CRD_INT (wakeup_en_crd_int):** Wakeup Event Enable On Card Interrupt

3.11.17 Clock Control Register (CLK_CTL)—Offset 2Ch

This register is used configure the frequency of the SDIO controller, and enable the clock.

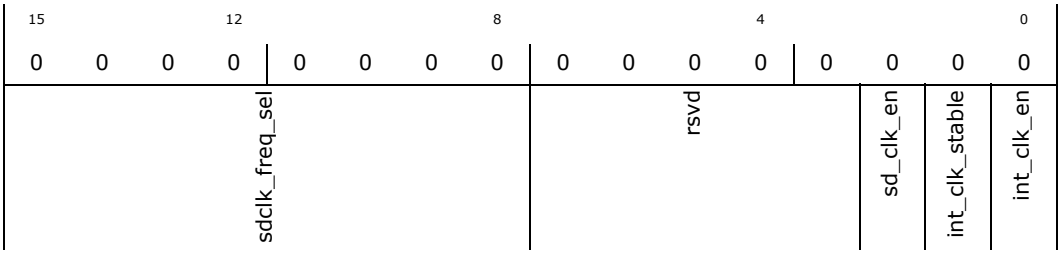
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

CLK_CTL: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RW	**SDCLK_FREQ_SEL (sdclk_freq_sel):** SDCLK Frequency Select
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**SD_CLK_EN (sd_clk_en):** SD Clock Enable
1	0b RO	**INT_CLK_STABLE (int_clk_stable):** Internal Clock Stable
0	0b RW	**INT_CLK_EN (int_clk_en):** Internal Clock Enable

3.11.18 Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh

Timeout Control Register

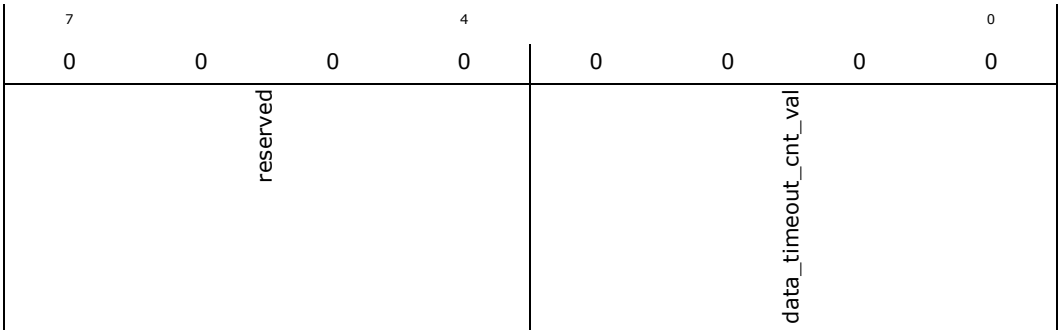
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

TIMEOUT_CTL: [BAR] + 2Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:4	0h RO	**Reserved (reserved):** Reserved

Bit Range	Default & Access	Description
3:0	0h RW	**DATA_TIMEOUT_CNT_VAL (data_timeout_cnt_val):** Data Timeout Counter Value

3.11.19 Software Reset Register (SW_RST)—Offset 2Fh

Software Reset Register

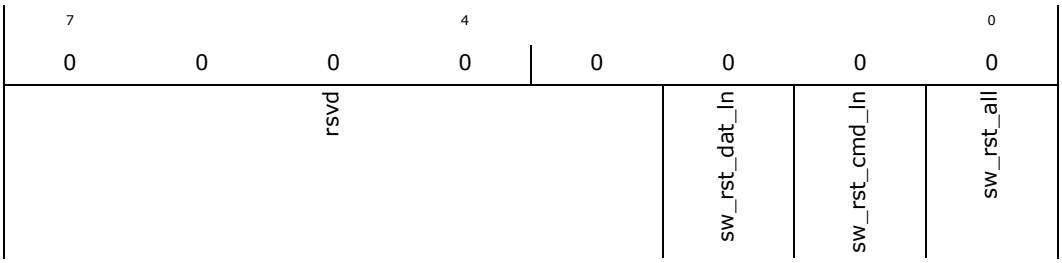
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SW_RST: [BAR] + 2Fh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**SW_RST_DAT_LN (sw_rst_dat_ln):** Software Reset For DAT Line
1	0b RW	**SW_RST_CMD_LN (sw_rst_cmd_ln):** Software Reset For CMD Line
0	0b RW	**SW_RST_ALL (sw_rst_all):** Software Reset For All

3.11.20 Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h

Normal Interrupt Status Register

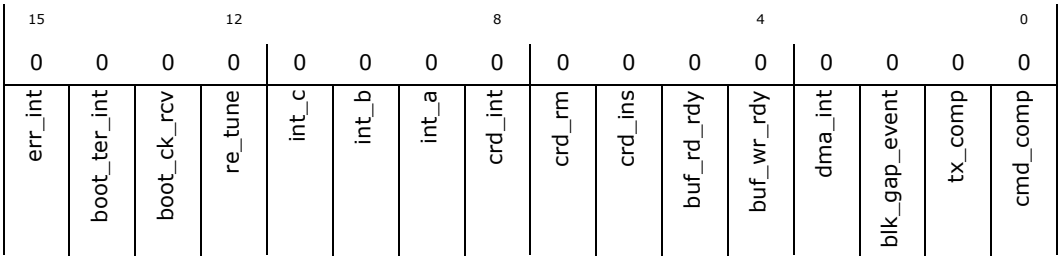
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NML_INT_STATUS: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
err_int	boot_ter_int	boot_ck_rcv	re_tune	int_c	int_b	int_a	crd_int	crd_rm	crd_ins	buf_rd_rdy	buf_wr_rdy	dma_int	blk_gap_event	tx_comp	cmd_comp

Bit Range	Default & Access	Description
15	0b RO	**ERR_INT (err_int):** Error Interrupt
14	0b RW/1C	**BOOT_TER_INT (boot_ter_int):** boot ter int
13	0b RW/1C	**BOOT_ACK_RCV (boot_ck_rcv):** boot ack rcv
12	0b RO	**RE_TUNE (re_tune):** re tuning event
11	0b RO	**INT_C (int_c):** int c
10	0b RO	**INT_B (int_b):** int b
9	0b RO	**INT_A (int_a):** int a
8	0b RO	**CRD_INT (crd_int):** Card Interrupt
7	0b RW/1C	**CRD_RM (crd_rm):** Card Removal
6	0b RW/1C	**CRD_INS (crd_ins):** Card Insertion
5	0b RW/1C	**BUF_RD_RDY (buf_rd_rdy):** Buffer Read Ready
4	0b RW/1C	**BUF_WR_RDY (buf_wr_rdy):** Buffer Write Ready
3	0b RW/1C	**DMA_INT (dma_int):** DMA Interrupt
2	0b RW/1C	**BLK_GAP_EVENT (blk_gap_event):** Block Gap Event
1	0b RW/1C	**TX_COMP (tx_comp):** Transfer Complete
0	0b RW/1C	**CMD_COMP (cmd_comp):** Command Complete

3.11.21 Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h

Error Interrupt Status Register

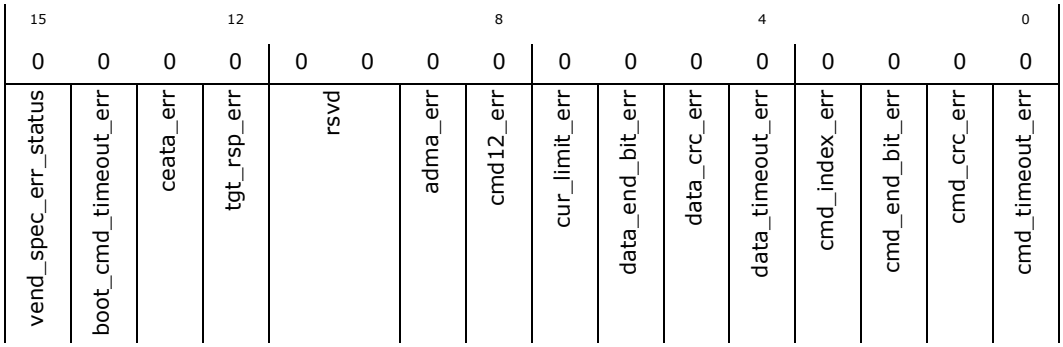
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_STATUS: [BAR] + 32h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**VEND_SPEC_ERR_STATUS (vend_spec_err_status):** Vendor Specific Error Status
14	0b RW	**BOOT_CMD_TIMEOUT_ERR (boot_cmd_timeout_err):** Occur if the boot are access command is issued to the agent which has no permission to access the boot area.
13	0b RW	**CEATA_ERR (ceata_err):** Occurs when ATA command termination has occurred due to an error condition the device has encountered.
12	0b RW	**TGT_RSP_ERR (tgt_rsp_err):** Occurs when detecting ERROR in m_hresp(dma transaction)
11:10	0h RO	**RSVD (rsvd):** Reserved
9	0b RW	**ADMA_ERR (adma_err):** ADMA Error
8	0b RW	**CMD12_ERR (cmd12_err):** Auto CMD12 Error
7	0b RW	**CUR_LIMIT_ERR (cur_limit_err):** Current Limit Error
6	0b RW	**DATA_END_BIT_ERR (data_end_bit_err):** Data End Bit Error
5	0b RW	**DATA_CRC_ERR (data_crc_err):** Data CRC Error
4	0b RW	**DATA_TIMEOUT_ERR (data_timeout_err):** Data Timeout Error
3	0b RW	**CMD_INDEX_ERR (cmd_index_err):** Command Index Error
2	0b RW	**CMD_END_BIT_ERR (cmd_end_bit_err):** Command End Bit Error

Bit Range	Default & Access	Description
1	0b RW	**CMD_CRC_ERR (cmd_crc_err):** Command CRC Error
0	0b RW	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Command Timeout Error

3.11.22 Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h

Normal Interrupt Status Enable

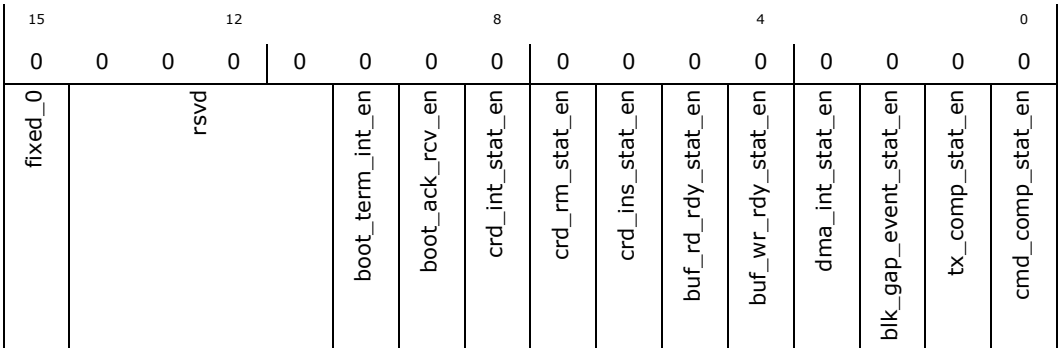
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NRM_INT_STATUS_EN: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RO	**FIXED_0 (fixed_0):** Fixed to 0
14:11	0h RO	**RSVD (rsvd):** Reserved
10	0b RW	**BOOT_TERM_INT_EN (boot_term_int_en):** 0 - Masked
9	0b RW	**BOOT_ACK_RCV_EN (boot_ack_rcv_en):** 0 -Masked
8	0b RW	**CRD_INT_STAT_EN (crd_int_stat_en):** Card Interrupt Status Enable
7	0b RW	**CRD_RM_STAT_EN (crd_rm_stat_en):** Card Removal Status Enable
6	0b RW	**CRD_INS_STAT_EN (crd_ins_stat_en):** Card Insertion Status Enable

Bit Range	Default & Access	Description
5	0b RW	**BUF_RD_RDY_STAT_EN (buf_rd_rdy_stat_en):** Buffer Read Ready Status Enable
4	0b RW	**BUF_WR_RDY_STAT_EN (buf_wr_rdy_stat_en):** Buffer Write Ready Status Enable
3	0b RW	**DMA_INT_STAT_EN (dma_int_stat_en):** DMA Interrupt Status Enable
2	0b RW	**BLK_GAP_EVENT_STAT_EN (blk_gap_event_stat_en):** Block Gap Event Status Enable
1	0b RW	**TX_COMP_STAT_EN (tx_comp_stat_en):** Transfer Complete Status Enable
0	0b RW	**CMD_COMP_STAT_EN (cmd_comp_stat_en):** Command Complete Status Enable

3.11.23 Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h

Error Interrupt Status Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_STAT_EN: [BAR] + 36h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_en	tgt_rsp_err_en	rsvd	tune_err_stat_en	adma_err_stat_en	cmd12_err_stat_en	cur_limit_err_stat_en	data_end_bit_err_stat_en	data_crc_err_stat_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Description
15:14	0b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR_EN (ceata_err_en):** 0 - masked
12	0b RW	**TGT_RSP_ERR_EN (tgt_rsp_err_en):** 0 - masked

Bit Range	Default & Access	Description
11	0b RO	**RSVD (rsvd):** Reserved
10	0b RW	**TUNE_ERR_STATE_EN (tune_err_stat_en):** 0 - masked
9	0b RW	**ADMA_ERR_STAT_EN (adma_err_stat_en):** ADMA Error Status Enable
8	0b RW	**CMD12_ERR_STAT_EN (cmd12_err_stat_en):** Auto CMD12 Error Status Enable
7	0b RW	**CUR_LIMIT_ERR_STAT_EN (cur_limit_err_stat_en):** Current Limit Error Status Enable
6	0b RW	**DATA_END_BIT_ERR_STAT_EN (data_end_bit_err_stat_en):** Data End Bit Error Status Enable
5	0b RW	**DATA_CRC_ERR_STAT_EN (data_crc_err_stat_en):** Data CRC Error Status Enable
4	0b RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Status Enable
3	0b RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Status Enable
2	0b RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Status Enable
1	0b RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Status Enable
0	0b RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Status Enable

3.11.24 Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h

Normal Interrupt Signal Enable Register

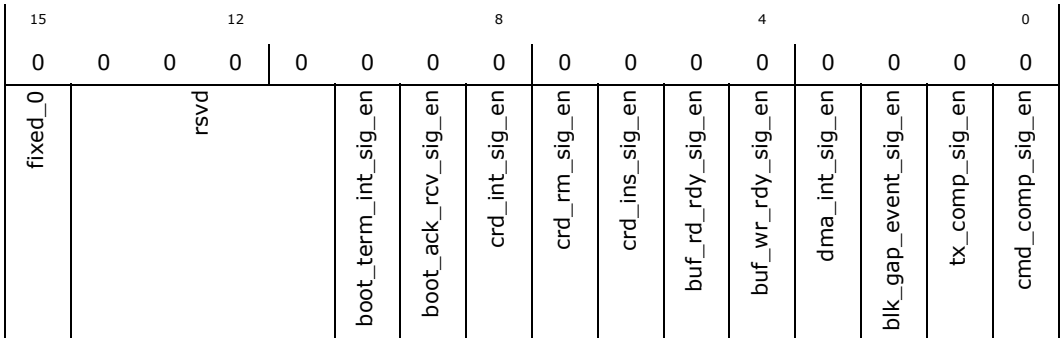
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NRM_INT_SIG_EN: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RO	**FIXED_0 (fixed_0):** Fixed to 0
14:11	0h RO	**RSVD (rsvd):** Reserved
10	0b RW	**BOOT_TERM_INT_SIG_EN (boot_term_int_sig_en):** 0 - masked
9	0b RW	**BOOT_ACK_RCV_SIG_EN (boot_ack_rcv_sig_en):** 0 - masked
8	0b RW	**CRD_INT_SIG_EN (crd_int_sig_en):** Card Interrupt Signal Enable
7	0b RW	**CRD_RM_SIG_EN (crd_rm_sig_en):** Card Removal Signal Enable
6	0b RW	**CRD_INS_SIG_EN (crd_ins_sig_en):** Card Insertion Signal Enable
5	0b RW	**BUF_RD_RDY_SIG_EN (buf_rd_rdy_sig_en):** Buffer Read Ready Signal Enable
4	0b RW	**BUF_WR_RDY_SIG_EN (buf_wr_rdy_sig_en):** Buffer Write Ready Signal Enable
3	0b RW	**DMA_INT_SIG_EN (dma_int_sig_en):** DMA Interrupt Signal Enable
2	0b RW	**BLK_GAP_EVENT_SIG_EN (blk_gap_event_sig_en):** Block Gap Event Signal Enable
1	0b RW	**TX_COMP_SIG_EN (tx_comp_sig_en):** Transfer Complete Signal Enable
0	0b RW	**CMD_COMP_SIG_EN (cmd_comp_sig_en):** Command Complete Signal Enable

3.11.25 Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah

Error Interrupt Signal Enable Register

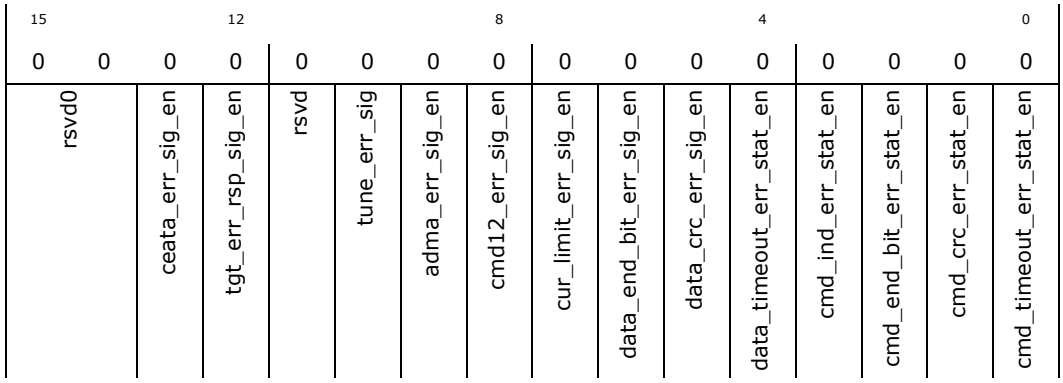
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_SIG_EN: [BAR] + 3Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:14	0b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR_SIG_EN (ceata_err_sig_en):** 0 - masked
12	0b RW	**TGT_ERR_RSP_SIG_EN (tgt_err_rsp_sig_en):** 0 - masked
11	0b RO	**RSVD (rsvd):** Reserved
10	0b RW	**TUNE_ERR_SIG (tune_err_sig):** 0 - masked
9	0b RW	**ADMA_ERR_SIG_EN (adma_err_sig_en):** ADMA Error Signal Enable
8	0b RW	**CMD12_ERR_SIG_EN (cmd12_err_sig_en):** Auto CMD12 Error Signal Enable
7	0b RW	**CUR_LIMIT_ERR_SIG_EN (cur_limit_err_sig_en):** Current Limit Error Signal Enable
6	0b RW	**DATA_END_BIT_ERR_SIG_EN (data_end_bit_err_sig_en):** Data End Bit Error Signal Enable
5	0b RW	**DATA_CRC_ERR_SIG_EN (data_crc_err_sig_en):** Data CRC Error Signal Enable
4	0b RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Signal Enable
3	0b RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Signal Enable
2	0b RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Signal Enable

Bit Range	Default & Access	Description
1	0b RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Signal Enable
0	0b RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Signal Enable

3.11.26 Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch

Auto CMD12 Error Status Register and Host control 2 Register

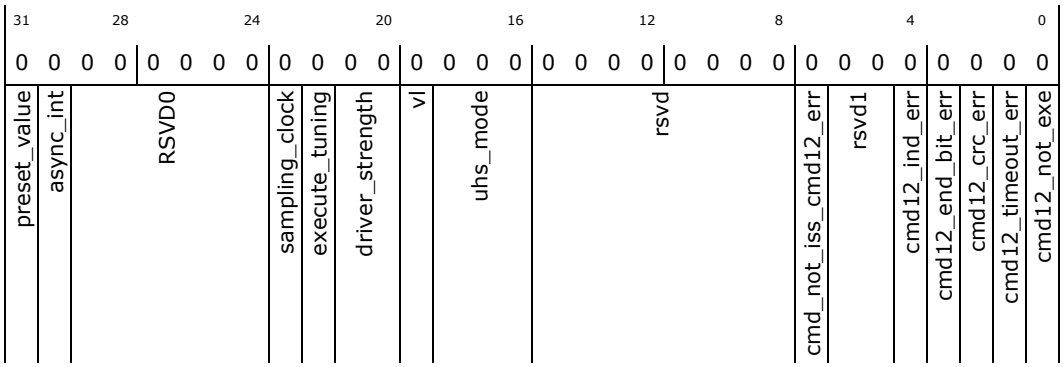
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

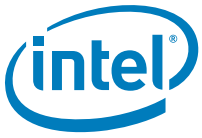
CMD12_ERR_STAT_HOST_CTRL_2: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**PRESET_VALUE (preset_value):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic This bit enables the functions defined in the Preset Value registers. 1 Automatic Selection by Preset Value are Enabled 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.



Bit Range	Default & Access	Description
30	0b RW	**ASYNC_INT (async_int):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 1 Enabled 0 Disabled
29:24	0b RO	**RSVD0:** Reserved
23	0b RW	**SAMPLING_CLOCK (sampling_clock):** This bit is set by tuning procedure when Execute Tuning is cleared
22	0b RW/AC	**EXECUTE_TUNING (execute_tuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 1 Execute Tuning 0 Not Tuned or Tuning Completed
21:20	0b RW	**DRIVER_STRENGTH (driver_strength):** Host Controller output driver in 1.8V signaling is selected by this bit
19	0b RW	**VL (vl):** This bit controls voltage regulator for I/O cell
18:16	0b RW	**UHS_MODE (uhs_mode):** This field is used to select one of UHS-I modes
15:8	0h RO	**RSVD (rsvd):** Reserved
7	0b RO	**CMD_NOT_ISS_CMD12_ERR (cmd_not_iss_cmd12_err):** Command Not Issued By Auto CMD12 Error
6:5	0h RO	**RSVD1 (rsvd1):** Reserved
4	0b RO	**CMD12_IND_ERR (cmd12_ind_err):** Auto CMD12 Index Error
3	0b RO	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Auto CMD12 End Bit Error
2	0b RO	**CMD12_CRC_ERR (cmd12_crc_err):** Auto CMD12 CRC Error
1	0b RO	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Auto CMD12 Timeout Error
0	0b RO	**CMD12_NOT_EXE (cmd12_not_exe):** Auto CMD12 Not Executed

3.11.27 Capabilities Register (CAPABILITIES)—Offset 40h

Capabilities Register

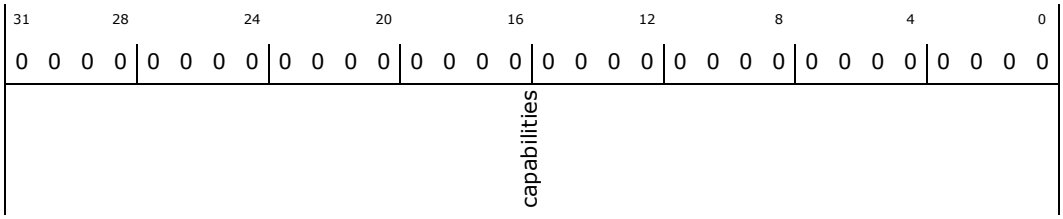
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITIES: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**capabilities:** capabilities

3.11.28 Capabilities Register 2 (CAPABILITIES_2)—Offset 44h

Capabilities Register 2

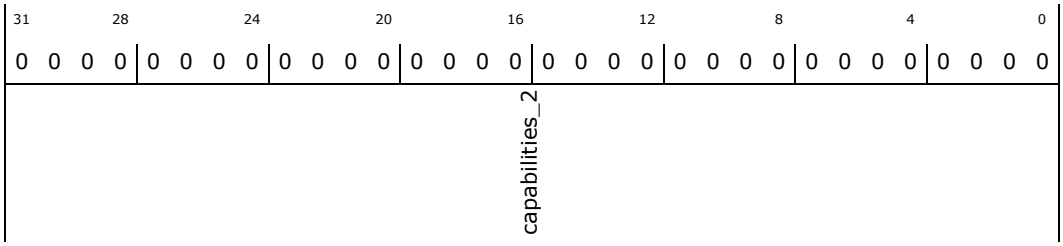
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITIES_2: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**capabilities_2:** capabilities 2

3.11.29 Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h

These registers indicate maximum current capability for each voltage

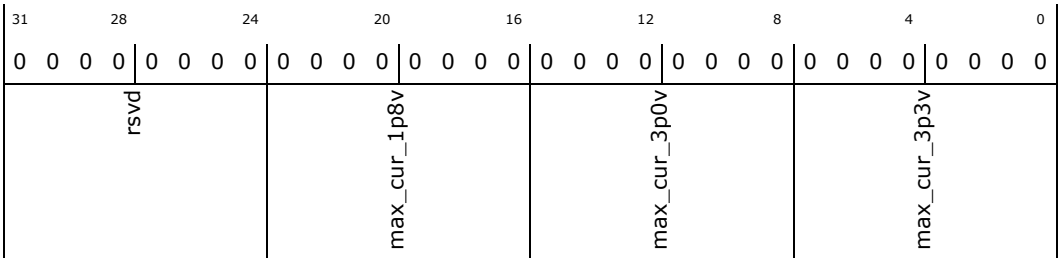
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MAX_CUR_CAP: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**RSVD (rsvd):** Reserved
23:16	00h RO	**MAX_CUR_1p8V (max_cur_1p8v):** Maximum Current for 1.8V
15:8	00h RO	**MAX_CUR_3p0V (max_cur_3p0v):** Maximum Current for 3.0V
7:0	00h RO	**MAX_CUR_3p3V (max_cur_3p3v):** Maximum Current for 3.3V

3.11.30 Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h

Force Event Register for Auto CMD12 Error Status

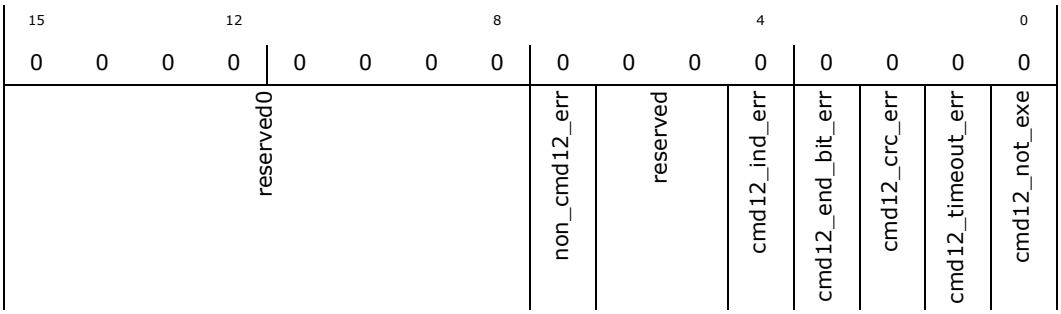
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

FORCE_EVENT_CMD12_ERR_STAT: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**Reserved0 (reserved0):** Reserved
7	0b RW	**NON_CMD12_ERR (non_cmd12_err):** Force Event for Command Not Issued By Auto CMD12 Error :
6:5	00b RO	**Reserved (reserved):** Reserved
4	0b RW	**CMD12_IND_ERR (cmd12_ind_err):** Force Event for Auto CMD12 Index Error
3	0b RW	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Force Event for Auto CMD12 End Bit Error
2	0b RW	**CMD12_CRC_ERR (cmd12_crc_err):** Force Event for Auto CMD12 CRC Error
1	0b RW	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Force Event for Auto CMD12 Timeout Error
0	0b RW	**CMD12_NOT_EXE (cmd12_not_exe):** Force Event for Auto CMD12 Not Executed

3.11.31 Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h

Force Event Register for Error Interrupt Status

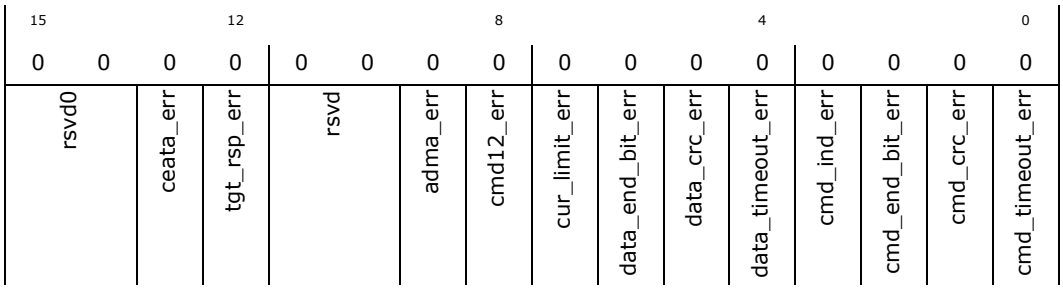
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

FORCE_EVENT_ERR_INT_STAT: [BAR] + 52h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:14	00b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR (ceata_err):** Force Event for CEATA error

Bit Range	Default & Access	Description
12	0b RW	**TGT_RSP_ERR (tgt_rsp_err):** Force Event for Target Response Error
11:10	0h RO	**RSVD (rsvd):** Reserved
9	0b RW	**ADMA_ERR (adma_err):** Force Event for ADMA Error
8	0b RW	**CMD12_ERR (cmd12_err):** Force Event for Auto CMD12 Error
7	0b RW	**CUR_LIMIT_ERR (cur_limit_err):** Force Event for Current Limit Error
6	0b RW	**DATA_END_BIT_ERR (data_end_bit_err):** Force Event for Data End Bit Error
5	0b RW	**DATA_CRC_ERR (data_crc_err):** Event for Data CRC Error
4	0b RW	**DATA_TIMEOUT_ERR (data_timeout_err):** Event for Data Timeout Error
3	0b RW	**CMD_IND_ERR (cmd_ind_err):** Force Event for Command Index Error
2	0b RW	**CMD_END_BIT_ERR (cmd_end_bit_err):** Force Event for Command End Bit Error
1	0b RW	**CMD_CRC_ERR (cmd_crc_err):** Force Event for Command CRC Error
0	0b RW	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Force Event for Command Timeout Error

3.11.32 ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h

ADMA Error Status Register

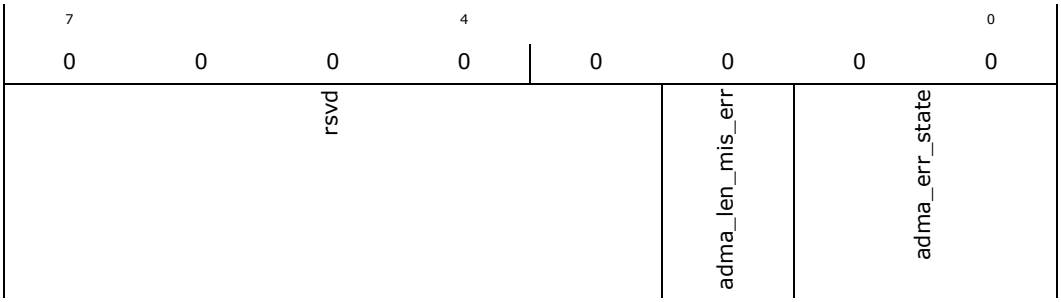
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

ADMA_ERR_STAT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RO	**ADMA_LEN_MIS_ERR (adma_len_mis_err):** ADMA Length Mismatch Error
1:0	00b RO	**ADMA_ERR_STATE (adma_err_state):** ADMA Error State

3.11.33 ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h

This register contains the physical Descriptor address used for ADMA data transfer.

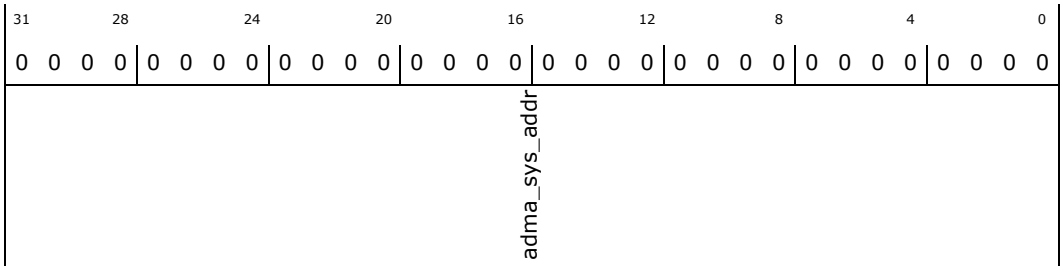
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ADMA_SYS_ADDR: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**ADMA_SYS_ADDR (adma_sys_addr):** ADMA System Address

3.11.34 Preset Values registers (PRESET_VALUE_0)—Offset 60h

Preset Values init and default speed

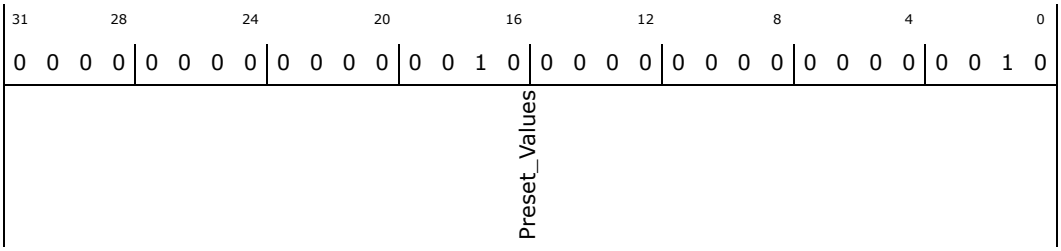
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_0: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00020002h



Bit Range	Default & Access	Description
31:0	00020002h RO	**PresetValues (Preset_Values):** Reserved.

3.11.35 Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h

Preset Values high and sdr12

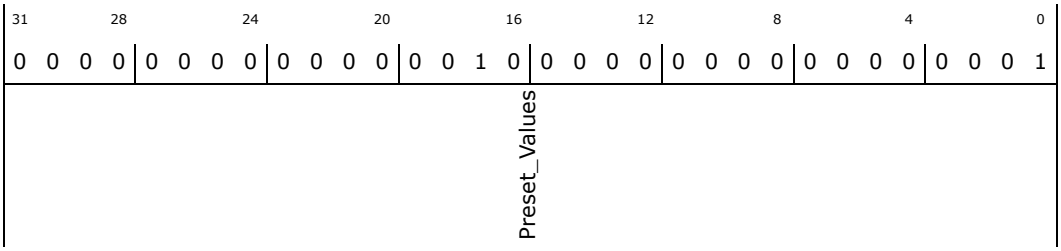
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_1: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00020001h



Bit Range	Default & Access	Description
31:0	00020001h RO	**PresetValues (Preset_Values):** Reserved.

3.11.36 Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h

Preset Values sdr25 and sdr50

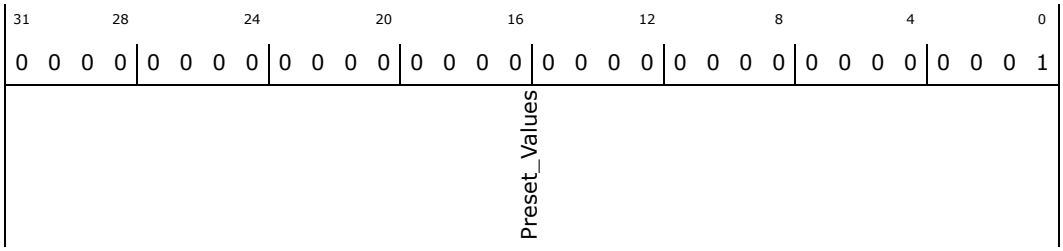
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_2: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:0	00000001h RO	**PresetValues (Preset_Values):** Reserved.

3.11.37 Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch

Preset Values sdr104 and ddr50

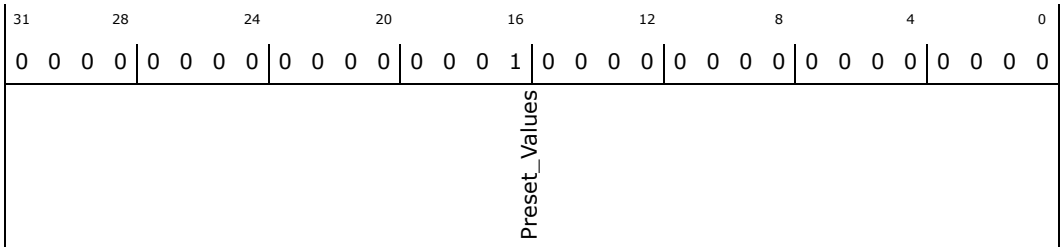
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_3: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31:0	00010000h RO	**PresetValues (Preset_Values):** Reserved.

3.11.38 BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h

BOOT_TIMEOUT_CTRL

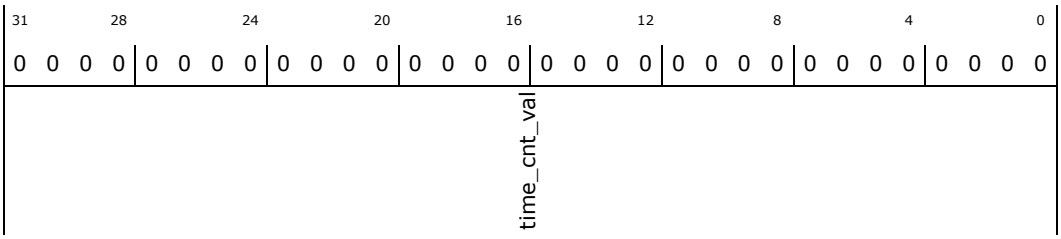
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BOOT_TIMEOUT_CTRL: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**TIME_CNT_VAL (time_cnt_val):** Boot Data Timeout Counter Value

3.11.39 DEBUG_SEL (DEBUG_SEL)—Offset 74h

Debug Selection Register

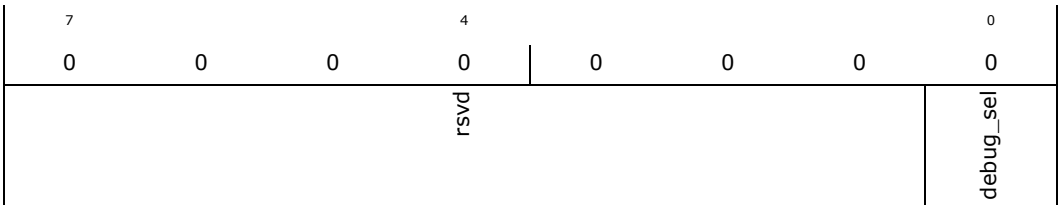
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

DEBUG_SEL: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:1	00h RO	**RSVD (rsvd):** Reserved
0	0b WO	**DEBUG_SEL (debug_sel):** 1 - cmd register, interrupt status, transmitter module, ahb_iface module and clk sdcard signals are probed out..

3.11.40 Shared Bus Control Register (SHARED_BUS)—Offset E0h

Shared Bus Control Register

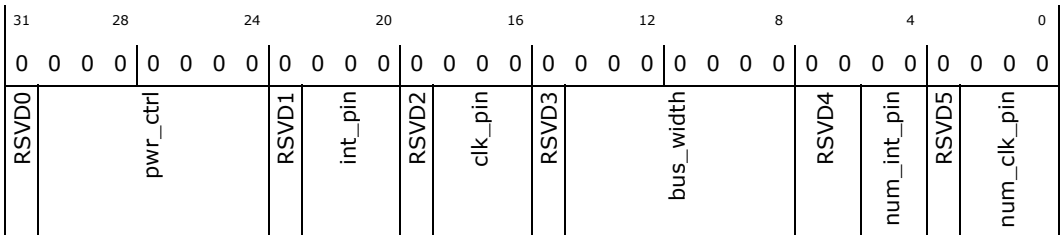
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SHARED_BUS: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**RSVD0:** Reserved
30:24	0h RW	**PWR_CTRL (pwr_ctrl):** Each bit of this field controls back-end power supply for an embedded device. Host interface voltage (VDDH) is not controlled by this field. The number of devices supported is specified by Number of Clock Pins and a maximum of 7 devices can be controlled D24 Back-end Power Control for Device 1 D25 Back-end Power Control for Device 2 D26 Back-end Power Control for Device 3 D27 Back-end Power Control for Device 4 D28 Back-end Power Control for Device 5 D29 Back-end Power Control for Device 6 D30 Back-end Power Control for Device 7 The function of each bit is defined as follows: 0 Back-end Power is Off 1 Back-end Power is Supplied Back-End power control is effective for embedded memory devices in the Sleep State that support the Sleep command (CMD14) to reduce power consumption and embedded SDIO devices when IOEx is set to 0.
23	0b RO	**RSVD1:** Reserved
22:20	0h RW	**INT_PIN (int_pin):** Interrupt pin inputs are enabled by this field. Enable of unsupported interrupt pin is meaningless. 000b Interrupt is detected by Interrupt Cycle xx1b INT_A is Enabled x1xb INT_B is Enabled 1xxb INT_C is Enabled
19	0b RO	**RSVD2:** Reserved
18:16	0h RW	**CLK_PIN (clk_pin):** One of clock pin outputs is selected by this field. Select of unsupported clock pin is meaningless. Refer to Figure 2-38 for the timing of clock outputs. 000b Clock Pins are Disabled 001b CLK[1] is Selected 010b CLK[2] is Selected .... 111b CLK[7] is Selected
15	0b RO	**RSVD3:** Reserved

Bit Range	Default & Access	Description
14:8	0h RO	**BUS_WIDTH (bus_width):** Shared bus supports mixing of 4-bit and 8-bit bus width devices. Each bit of this field specifies the bus width for each embedded device. The number of devices supported is specified by Number of Clock Pins and a maximum of 7 devices are supported.This field is effective when multiple devices are connected to a shared bus (Slot Type is set to 10b in the Capabilities register). In the other case, Extended Data Transfer Width in the Host Control 1 register is used to select 8-bit bus width. As use of 1-bit mode is not intended for shared bus, Data Transfer Width in the Host Control 1 register should be set to 1.D08 - Bus width preset for Device 1 D09 - Bus width preset for Device 2 D10 - Bus width preset for Device 3 D11 - Bus width preset for Device 4 D12 - Bus width preset for Device 5 D13 - Bus width preset for Device 6 D14 - Bus width preset for Device 7 The function of each bit is defined as follows: 0 - 4 bit buswidth mode 1 - 8 bit buswidth mode
7:6	0b RO	**RSVD4:** Reserved
5:4	0h RO	**NUM_INT_PIN (num_int_pin):** This field indicates support of interrupt input pins for shared bus system.Three asynchronous interrupt pins are defined, INT_A#, INT_B# and INT_C#. Which interrupt pin is used is determined by the system. Each one is driven by open drain and then wired or connection is possible. 00b Interrupt Input Pin is Not Supported 01b INTA is Supported 10b INTA and INTB are Supported 11b INTA, INTB and INTC are Supported
3	0b RO	**RSVD5:** Reserved
2:0	0h RO	**NUM_CLK_PIN (num_clk_pin):** This field indicates support of clock pins to select one of devices for shared bus system. Up to 7 clock pins can be supported.Shared bus is supported by specific system. Then Standard Host Driver does not support control of these clock pins. 000b Shared bus is not supported 001b 1 SDCLK pin is supported 010b 2 SDCLK pins are supported .... 111b 7 SDCLK pins are supported

3.11.41 SPI_INT_SUP (SPI_INT_SUP)—Offset F0h

SPI_INT_SUP

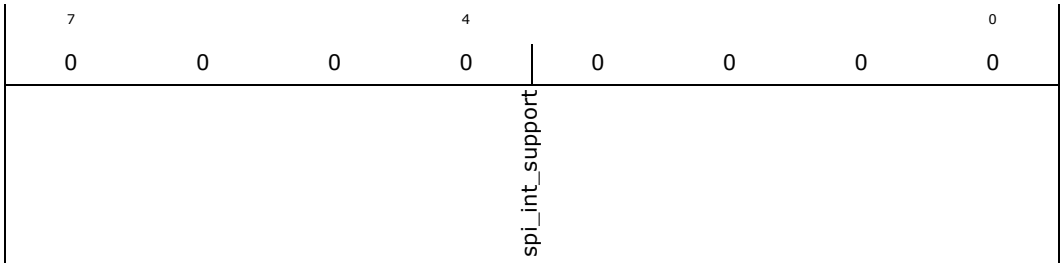
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SPI_INT_SUP: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**SPI_INT_SUPPORT (spi_int_support):** This bit is set to indicate the assertion assertion of interrupts in the SPI mode at any time, irrespective of the status of thecard select (CS) line. If this bit is zero, then SDIO card can only assert the interrupt line in the SPI mode when the CS line is asserted.

3.11.42 Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh

Slot Interrupt Status Register

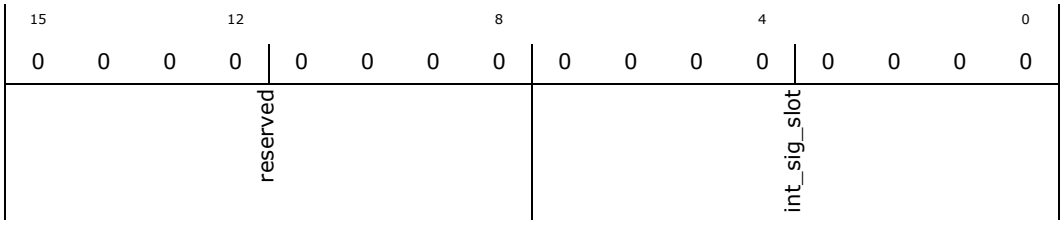
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

SLOT_INT_STAT: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**Reserved (reserved):** Reserved
7:0	00h RO	**INT_SIG_SLOT (int_sig_slot):** Interrupt Signal For Each Slot

3.11.43 Host Controller Version Register (HOST_CTRL_VER)—Offset FEh

Host Controller Version Register

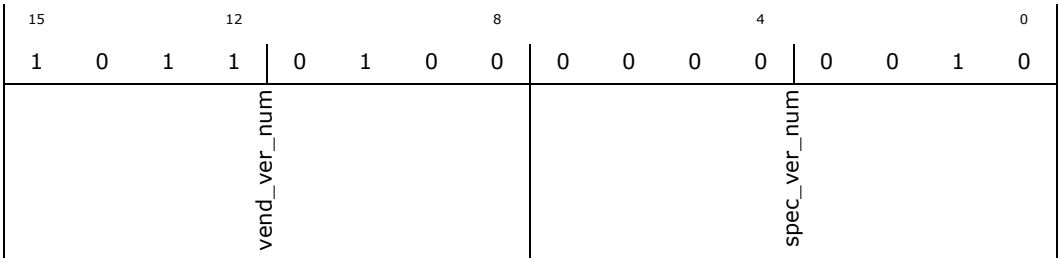
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

HOST_CTRL_VER: [BAR] + FEh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: B402h



Bit Range	Default & Access	Description
15:8	b4h RO	**VEND_VER_NUM (vend_ver_num):** Vendor Version Number
7:0	02h RO	**SPEC_VER_NUM (spec_ver_num):** Version Number

3.12 SD PCI Configuration Registers

Table 20. Summary of SD PCI Configuration Registers—0/18/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 1566	00000000h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 1567	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 1568	00000000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 1569	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 1569	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 1570	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 1571	00000000h
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 1571	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 1572	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 1572	00000100h
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 1573	48030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 1574	00000008h
A0h	4	"reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h" on page 1574	00000000h
A4h	4	"reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h" on page 1575	00000000h
A8h	4	"reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h" on page 1575	00000000h
ACh	4	"reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh" on page 1576	00000000h
C0h	4	"reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h" on page 1576	00000000h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 1577	00000000h

3.12.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

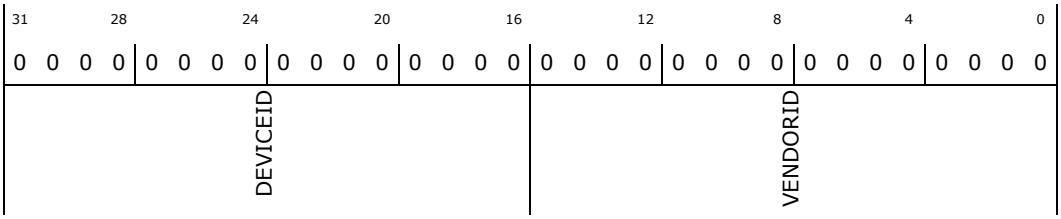
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:18, F:0] + 0h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**DEVICEID:** Reserved.
15:0	0000h RO	**VENDORID:** Reserved.

3.12.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

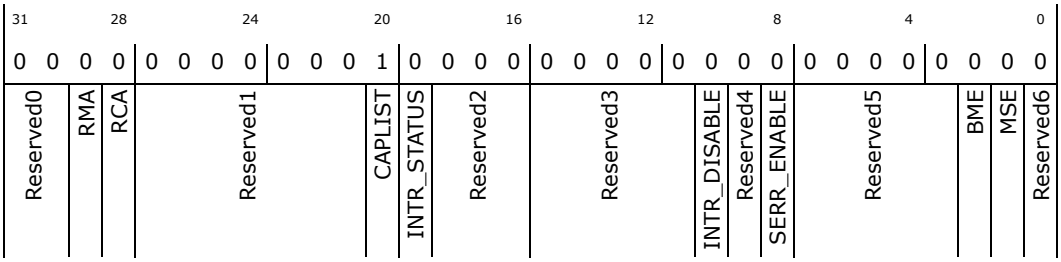
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:18, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** Reserved.
29	0h RW/1C	**RMA:** Reserved.
28	0h RW/1C	**RCA:** Reserved.
27:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**CAPLIST:** Reserved.
19	0h RO	**INTR_STATUS:** Reserved.

Bit Range	Default & Access	Description
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**INTR_DISABLE:** Reserved.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR_ENABLE:** Reserved.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**BME:** Reserved.
1	0h RW	**MSE:** Reserved.
0	0h RO	**Reserved6:** Reserved.

3.12.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

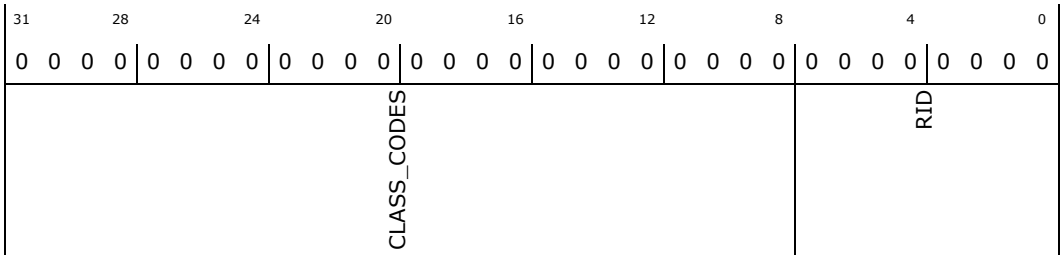
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:18, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**CLASS_CODES:** Reserved.
7:0	00h RO	**RID:** Reserved.

3.12.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

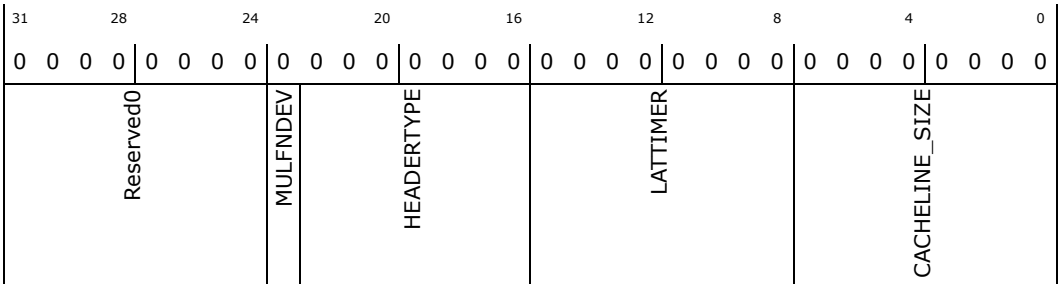
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:18, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	0h RO	**MULFNDEV:** Reserved.
22:16	00h RO	**HEADERTYPE:** Reserved.
15:8	00h RO	**LATTIMER:** Reserved.
7:0	00h RW	**CACHELINE_SIZE:** Reserved.

3.12.5 reg_BAR_type (BAR)—Offset 10h

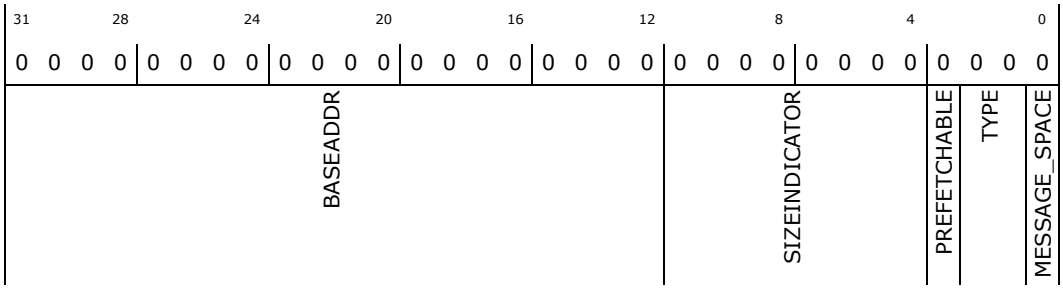
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Reserved.
11:4	00h RO	**SIZEINDICATOR:** Reserved.
3	0h RO	**PREFETCHABLE:** Reserved.
2:1	0h RO	**TYPE:** Reserved.
0	0h RO	**MESSAGE_SPACE:** Reserved.

3.12.6 reg_BAR1_type (BAR1)—Offset 14h

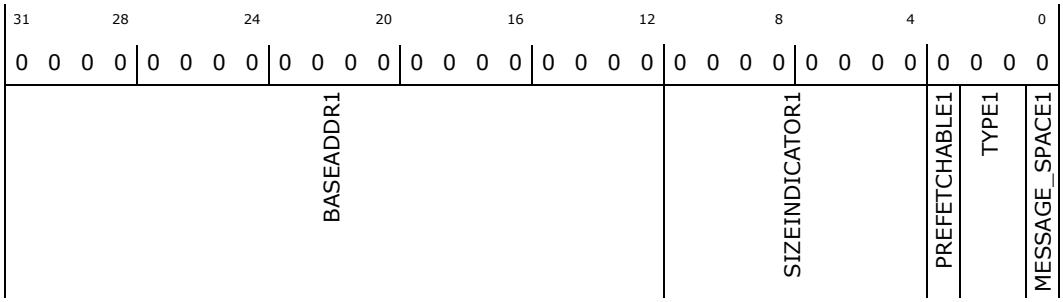
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:18, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** Reserved.
11:4	00h RO	**SIZEINDICATOR1:** Reserved.

Bit Range	Default & Access	Description
3	0h RO	**PREFETCHABLE1:** Reserved.
2:1	0h RO	**TYPE1:** Reserved.
0	0h RO	**MESSAGE_SPACE1:** Reserved.

3.12.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

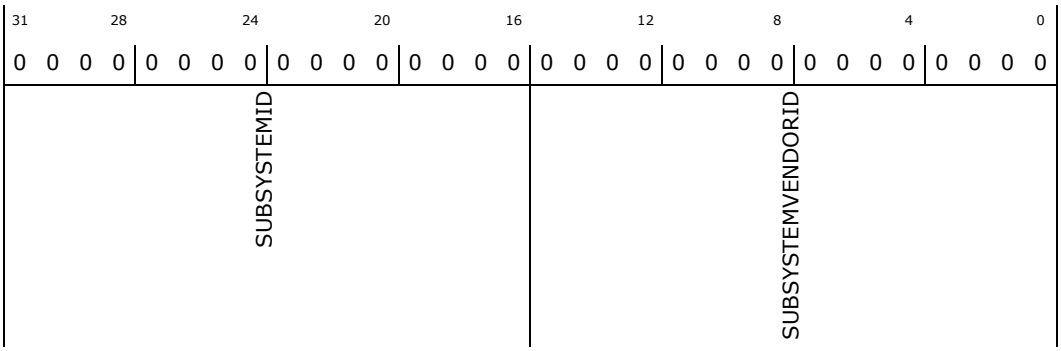
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:18, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Reserved.
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Reserved.

3.12.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

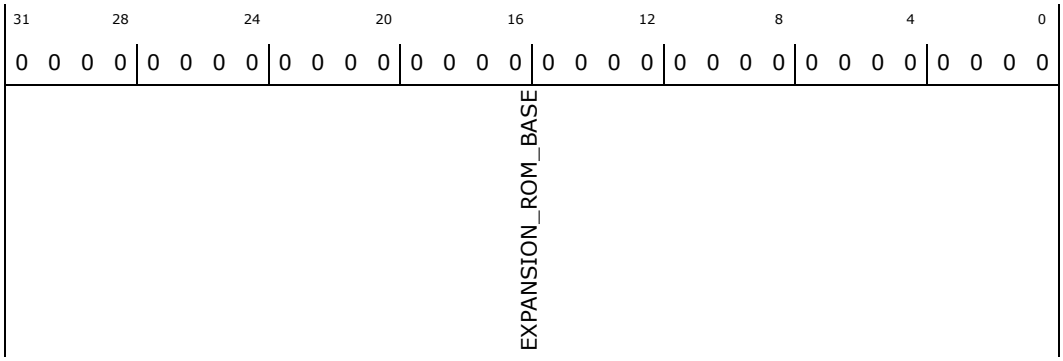
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:18, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

3.12.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

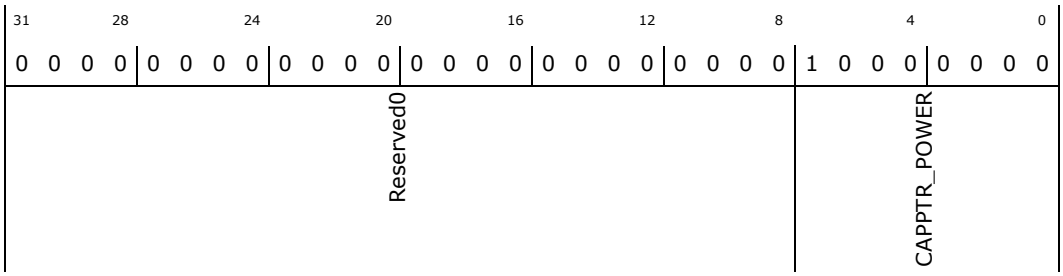
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:18, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	80h RO	**CAPPTR_POWER:** Reserved.

3.12.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

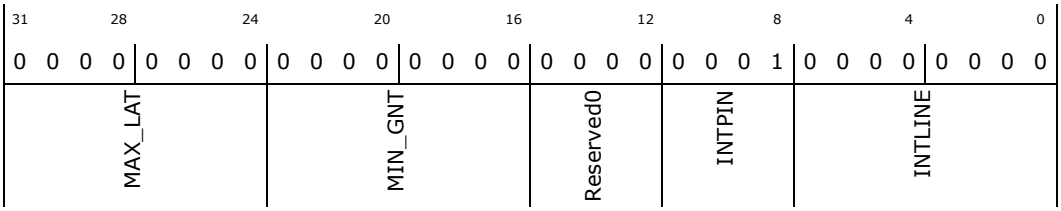
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:18, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Reserved.
23:16	00h RO	**MIN_GNT:** Reserved.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**INTPIN:** Reserved.
7:0	00h RW	**INTLINE:** Reserved.

3.12.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

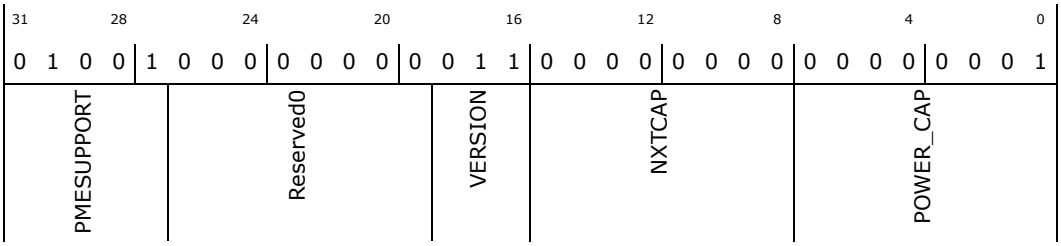
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:18, F:0] + 80h

Default: 48030001h



Bit Range	Default & Access	Description
31:27	09h RO	**PMESUPPORT:** Reserved.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**VERSION:** Reserved.

Bit Range	Default & Access	Description
15:8	00h RO	**NXTCAP:** Reserved.
7:0	01h RO	**POWER_CAP:** Reserved.

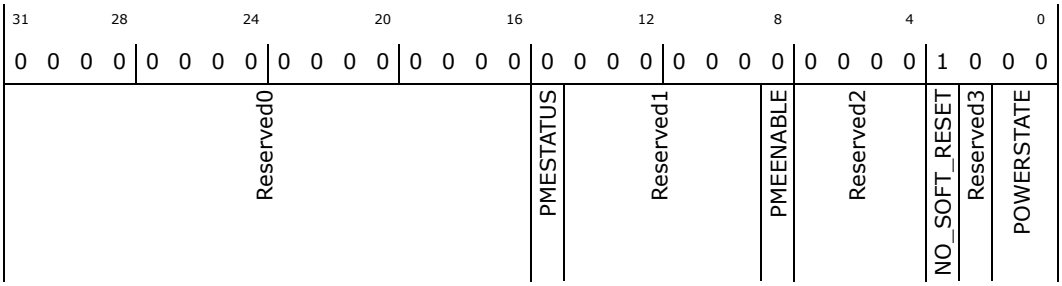
3.12.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:18, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PMESTATUS:** Reserved.
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PMEENABLE:** Reserved.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**NO_SOFT_RESET:** Reserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**POWERSTATE:** Reserved.

3.12.13 reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h

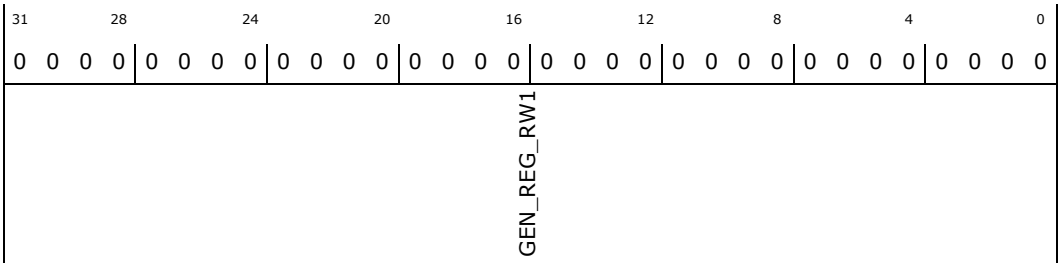
General Purpose Read Write Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW1: [B:0, D:18, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW1:** capabilities over-ride for the sd/sdio/emmc host controller (bits 31:0)

3.12.14 reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h

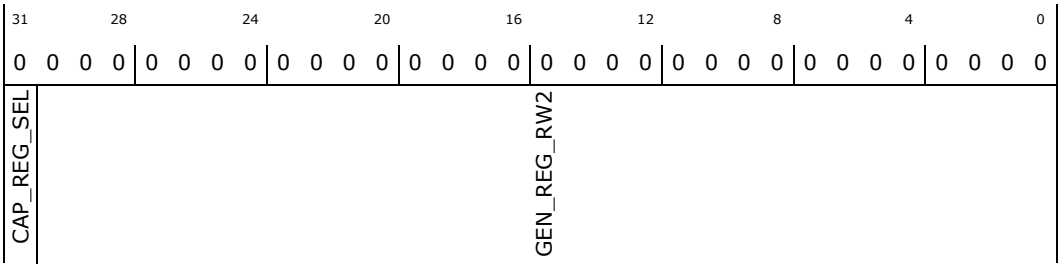
General Purpose Read Write Register2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW2: [B:0, D:18, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**CAP_REG_SEL:** select if the capabilty will come from the GEN PCI register or from a hard wire
30:0	0h RW	**GEN_REG_RW2:** capabilities over-ride for the sd/sdio/emmc host controller (bits 62:32)

3.12.15 reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h

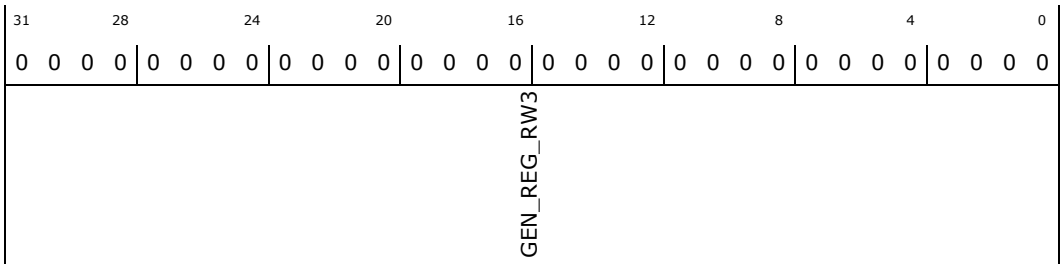
General Purpose Read Write Register3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW3: [B:0, D:18, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW3:** Reserved.

3.12.16 reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh

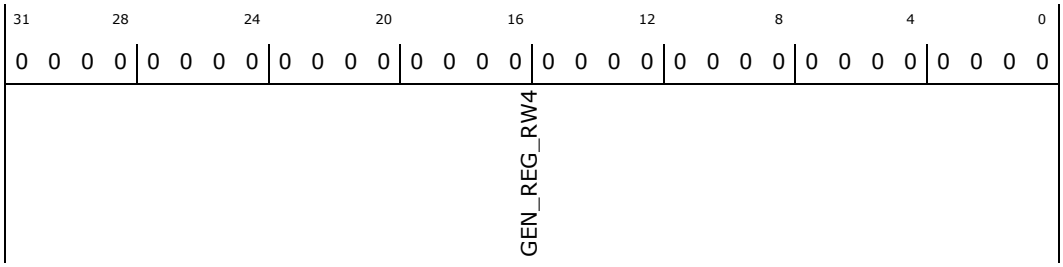
General Purpose Read Write Register4

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW4: [B:0, D:18, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW4:** Reserved.

3.12.17 reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h

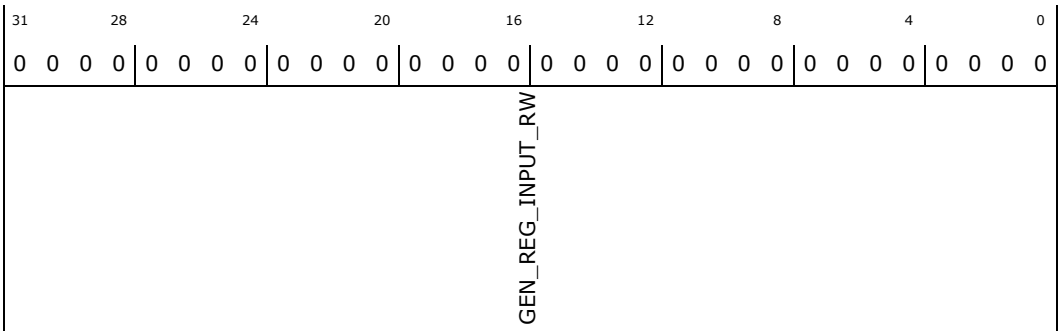
General Purpose Input Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_INPUT_REGRW: [B:0, D:18, F:0] + C0h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**GEN_REG_INPUT_RW:** Reserved.

3.12.18 reg_MANID_type (MANID)—Offset F8h

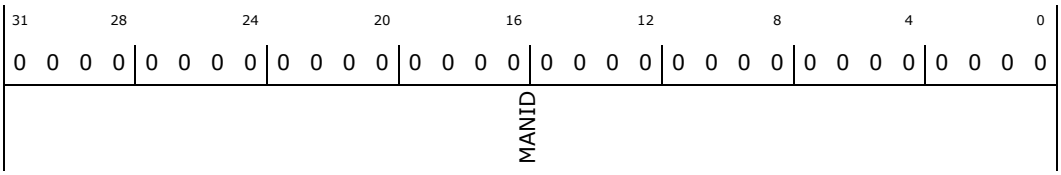
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:18, F:0] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**MANID:** Reserved.

3.13 SD Memory Mapped IO Registers

Table 21. Summary of SD Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"SDMA System Address Register (SYS_ADR)—Offset 0h" on page 1579	00000000h
4h	2	"Block Size Register (BLK_SIZE)—Offset 4h" on page 1580	0000h
6h	2	"Block Count Register (BLK_COUNT)—Offset 6h" on page 1581	0000h
8h	4	"Argument Register (ARGUMENT)—Offset 8h" on page 1582	00000000h
Ch	2	"Transfer Mode Register (TX_MODE)—Offset Ch" on page 1582	0000h
Eh	2	"Command Register (CMD)—Offset Eh" on page 1583	0000h
10h	4	"Response Register0 (RESPONSE0)—Offset 10h" on page 1584	00000000h
14h	4	"Response Register2 (RESPONSE2)—Offset 14h" on page 1585	00000000h
18h	4	"Response Register4 (RESPONSE4)—Offset 18h" on page 1585	00000000h
1Ch	4	"Response Register6 (RESPONSE6)—Offset 1Ch" on page 1586	00000000h
20h	4	"Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h" on page 1587	00000000h
24h	4	"Present State Register (PRE_STATE)—Offset 24h" on page 1587	1FFF0000h
28h	1	"Host Control Register (HOST_CTL)—Offset 28h" on page 1588	00h
29h	1	"Power Control Register (PWR_CTL)—Offset 29h" on page 1589	00h
2Ah	1	"Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah" on page 1590	00h
2Bh	1	"Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh" on page 1591	00h
2Ch	2	"Clock Control Register (CLK_CTL)—Offset 2Ch" on page 1591	0000h
2Eh	1	"Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh" on page 1592	00h
2Fh	1	"Software Reset Register (SW_RST)—Offset 2Fh" on page 1593	00h
30h	2	"Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h" on page 1593	0000h
32h	2	"Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h" on page 1594	0000h
34h	2	"Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h" on page 1596	0000h
36h	2	"Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h" on page 1597	0000h
38h	2	"Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h" on page 1598	0000h
3Ah	2	"Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah" on page 1599	0000h
3Ch	4	"Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch" on page 1601	00000000h
40h	4	"Capabilities Register (CAPABILITIES)—Offset 40h" on page 1602	00000000h
44h	4	"Capabilities Register 2 (CAPABILITIES_2)—Offset 44h" on page 1603	00000000h

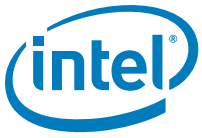


Table 21. Summary of SD Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
48h	4	"Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h" on page 1603	00000000h
50h	2	"Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h" on page 1604	0000h
52h	2	"Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h" on page 1605	0000h
54h	1	"ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h" on page 1606	00h
58h	4	"ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h" on page 1607	00000000h
60h	4	"Preset Values registers (PRESET_VALUE_0)—Offset 60h" on page 1607	00020002h
64h	4	"Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h" on page 1608	00020001h
68h	4	"Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h" on page 1608	00000001h
6Ch	4	"Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch" on page 1609	00010000h
70h	4	"BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h" on page 1609	00000000h
74h	1	"DEBUG_SEL (DEBUG_SEL)—Offset 74h" on page 1610	00h
E0h	4	"Shared Bus Control Register (SHARED_BUS)—Offset E0h" on page 1610	00000000h
F0h	1	"SPI_INT_SUP (SPI_INT_SUP)—Offset F0h" on page 1612	00h
FCh	2	"Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh" on page 1613	0000h
FEh	2	"Host Controller Version Register (HOST_CTRL_VER)—Offset FEh" on page 1613	B402h

3.13.1 SDMA System Address Register (SYS_ADR)—Offset 0h

This register contains the physical system memory address used for DMA transfers

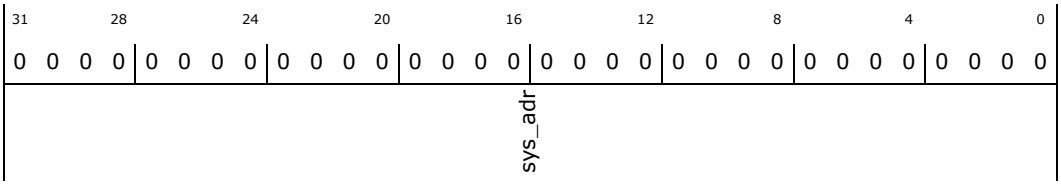
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SYS_ADR: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**SYS_ADR (sys_adr):** SDMA System Address This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register.

3.13.2 Block Size Register (BLK_SIZE)—Offset 4h

This register is used to configure the number of bytes in a data block.

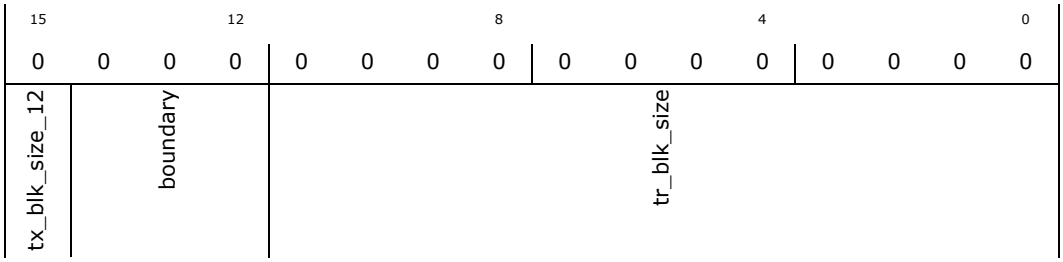
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

BLK_SIZE: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**TX_BLK_SIZE_12 (tx_blk_size_12):** Transfer Block Size 12th bit. This bit is added to support 4Kb Data block transfer.

Bit Range	Default & Access	Description
14:12	000b RW	**BOUNDARY (boundary):** Host SDMA Buffer Boundary The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. ADMA does not use this register. 000b - 4K bytes (Detects A11 carry out) 001b - 8K bytes (Detects A12 carry out) 010b - 16K Bytes (Detects A13 carry out) 011b - 32K Bytes (Detects A14 carry out) 100b - 64K bytes (Detects A15 carry out) 101b - 128K Bytes (Detects A16 carry out) 110b - 256K Bytes (Detects A17 carry out) 111b - 512K Bytes (Detects A18 carry out)
11:0	000h RW	**TR_BLK_SIZE (tr_blk_size):** Transfer Block Size This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes (Refer to Implementation Note in Section 1.7.2). It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. 0800h 2048 Bytes ??? ??? 0200h 512 Bytes 01FFh 511 Bytes ??? ??? 0004h 4 Bytes 0003h 3 Bytes 0002h 2 Bytes 0001h 1 Byte 0000h No data transfer

3.13.3 Block Count Register (BLK_COUNT)—Offset 6h

This register is used to configure the number of data blocks

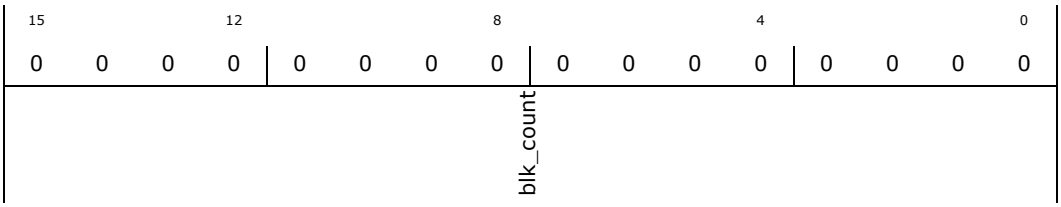
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

BLK_COUNT: [BAR] + 6h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	0000h RW	**BLK_COUNT (blk_count):** Blocks Count For Current Transfer This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers

3.13.4 Argument Register (ARGUMENT)—Offset 8h

This register contains the SD Command Argument.

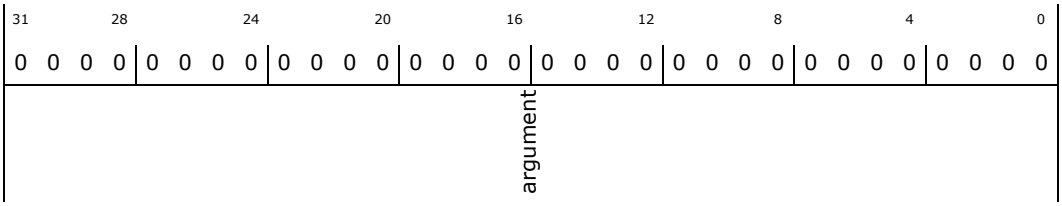
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ARGUMENT: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**ARGUMENT (argument):** Command Argument The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

3.13.5 Transfer Mode Register (TX_MODE)—Offset Ch

Transfer Mode Register

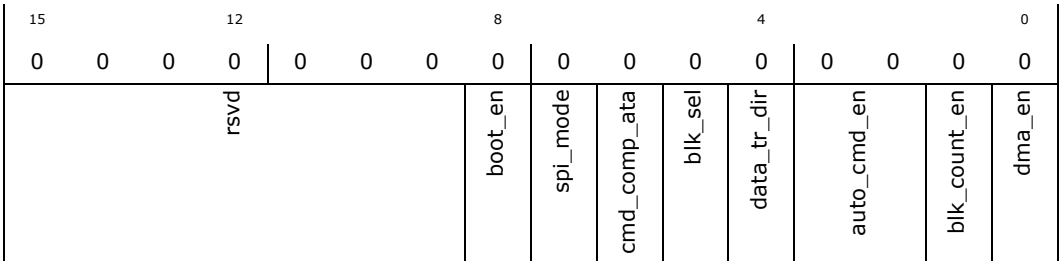
Access Method

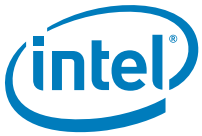
Type: Memory Mapped I/O Register (Size: 16 bits)

TX_MODE: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h





Bit Range	Default & Access	Description
15:9	00h RO	**RSVD (rsvd):** Reserved
8	0b RW	**BOOT_EN (boot_en):** To start boot operation for MMC4.3 1 - To start boot mode 0 - Stop the boot read
7	0b RW	**SPI_MODE (spi_mode):** SPI mode enable bit. 1 - SPI mode 0 - SD mode
6	0b RW	**CMD_COMP_ATA (cmd_comp_ata):** Command Completion Signal Enable for CE-ATA Device. ???1??? - Device will send command completion Signal ???0??? - Device will not send command completion Signal
5	0b RW	**BLK_SEL (blk_sel):** Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the Block Count register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block
4	0b RW	**Data_TR_Dir (data_tr_dir):** Data Transfer Direction Select This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller and it is set to 0 for all other commands. 1 Read (Card to Host) 0 Write (Host to Card)
3:2	0b RW	**AUTO_CMD_EN (auto_cmd_en):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0b RW	**BLK_COUNT_EN (blk_count_en):** Block Count Enable This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8) If ADMA2 data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table. 1 Enable 0 Disable
0	0b RW	**DMA_EN (dma_en):** DMA Enable This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the Capabilities register. One of the DMA modes can be selected by DMA Select in the Host Control register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of Command register (00Fh). 1 DMA Data transfer 0 No data transfer or Non DMA data transfer

3.13.6 Command Register (CMD)—Offset Eh

Command Register

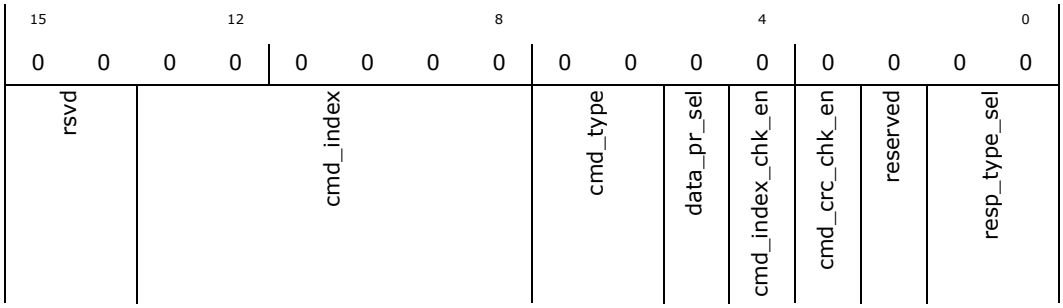
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

CMD: [BAR] + Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:14	0h RO	**RSVD (rsvd):** Reserved
13:8	0h RW	**CMD_INDEX (cmd_index):** Command Index These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.
7:6	00b RW	**CMD_TYPE (cmd_type):** Command Type
5	0b RW	**DATA_PR_SEL (data_pr_sel):** Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) (3) Resume command 1 Data Present 0 No Data Present
4	0b RW	**CMD_INDEX_CHK_EN (cmd_index_chk_en):** Command Index Check Enable If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 1 Enable 0 Disable
3	0b RW	**CMD_CRC_CHK_EN (cmd_crc_chk_en):** Command CRC Check Enable If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response. (Refer to definition in D01-00 and Table 2-10 below.) 1 Enable 0 Disable
2	0b RO	**Reserved (reserved):** Reserved
1:0	0h RW	**RESP_TYPE_SEL (resp_type_sel):** Response Type Select 00 No Response 01 Response Length 136 10 Response Length 48 11 Response Length 48 check Busy after response

3.13.7 Response Register0 (RESPONSE0)—Offset 10h

This register is used to store responses from SD cards

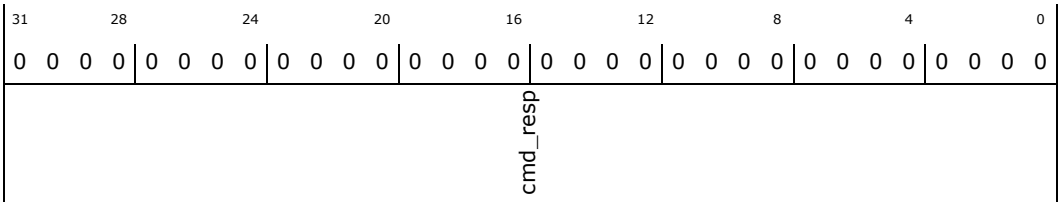
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE0: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP0 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.13.8 Response Register2 (RESPONSE2)—Offset 14h

This register is used to store responses from SD cards

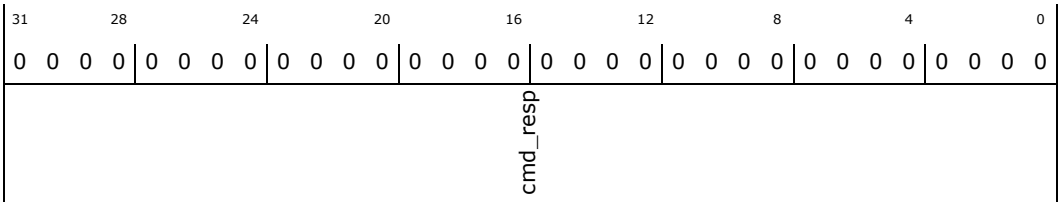
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE2: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP2 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.13.9 Response Register4 (RESPONSE4)—Offset 18h

This register is used to store responses from SD cards

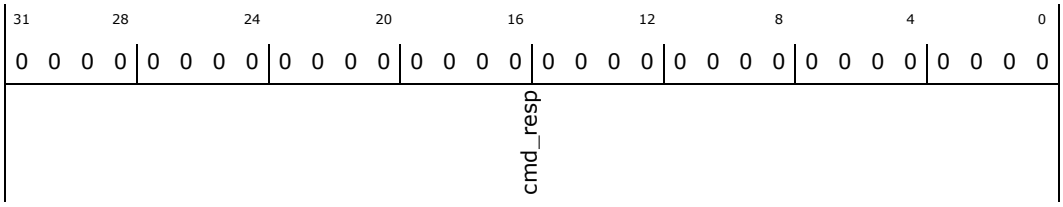
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE4: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP4 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.13.10 Response Register6 (RESPONSE6)—Offset 1Ch

This register is used to store responses from SD cards

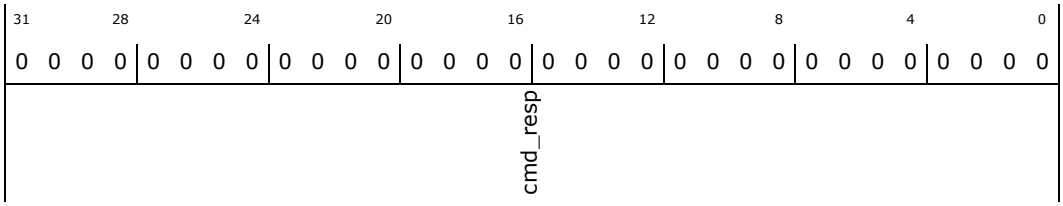
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE6: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP6 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.13.11 Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h

32-bit data port register to access internal buffer

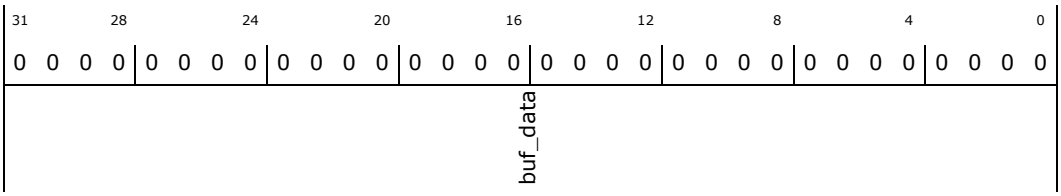
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BUF_DATA_PORT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUF_DATA (buf_data):** Buffer Data The Host Controller buffer can be accessed through this 32-bit Data Port register. Refer to 1.7

3.13.12 Present State Register (PRE_STATE)—Offset 24h

The Host Driver can get status of the Host Controller from this 32-bit read only register

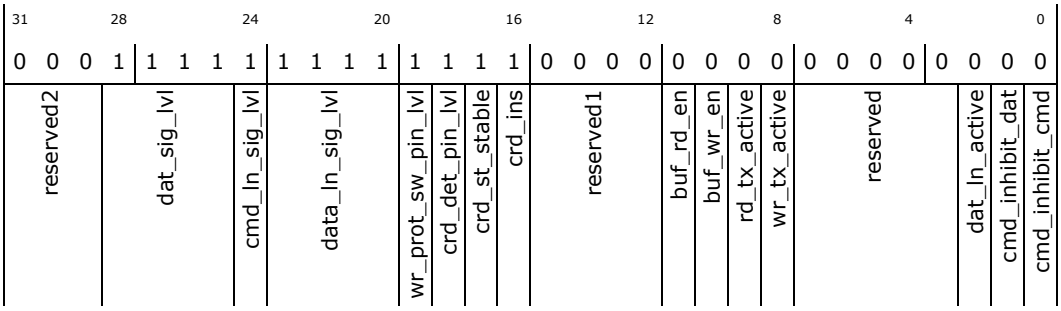
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRE_STATE: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 1FFF0000h



Bit Range	Default & Access	Description
31:29	0h RO	**Reserved2 (reserved2):** Reserved

Bit Range	Default & Access	Description
28:25	1111b RO	**DAT_SIG_LVL (dat_sig_lvl):** This status is used to check DAT line level to recover from errors, and for debugging. D28 - DAT[7] D27 - DAT[6] D26 - DAT[5] D25 - DAT[4]
24	1b RO	**CMD_LN_SIG_LVL (cmd_ln_sig_lvl):** CMD Line Signal Level This status is used to check the CMD line level to recover from errors, and for debugging.
23:20	Fh RO	**DATA_LN_SIG_LVL (data_ln_sig_lvl):** DAT[3:0] Line Signal Level This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D23 DAT[3] D22 DAT[2] D21 DAT[1] D20 DAT[0]
19	1b RO	**WR_PROT_SW_PIN_LVL (wr_prot_sw_pin_lvl):** Write Protect Switch Pin Level
18	1b RO	**CRD_DET_PIN_LVL (crd_det_pin_lvl):** Card Detect Pin Level
17	1b RO	**CRD_ST_STABLE (crd_st_stable):** Card State Stable
16	1b RO	**CRD_INS (crd_ins):** Card Inserted
15:12	0h RO	**Reserved1 (reserved1):** Reserved
11	0b RO	**BUF_RD_EN (buf_rd_en):** Buffer Read Enable
10	0b RO	**BUF_WR_EN (buf_wr_en):** Buffer Write Enable
9	0b RO	**RD_TX_ACTIVE (rd_tx_active):** Read Transfer Active
8	0b RO	**WR_TX_ACTIVE (wr_tx_active):** Write Transfer Active
7:3	00h RO	**Reserved (reserved):** Reserved
2	0b RO	**DAT_LN_ACTIVE (dat_ln_active):** DAT Line Active
1	0b RO	**CMD_INHIBIT_DAT (cmd_inhibit_dat):** Command Inhibit (DAT)
0	0b RO	**CMD_INHIBIT_CMD (cmd_inhibit_cmd):** Command Inhibit (CMD)

3.13.13 Host Control Register (HOST_CTL)—Offset 28h

Host Control Register

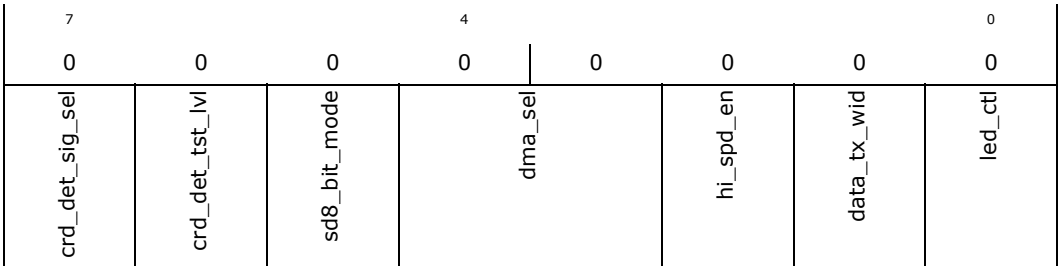
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

HOST_CTL: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RW	**CRD_DET_SIG_SEL (crd_det_sig_sel):** Card Detect Signal Selection
6	0b RW	**CRD_DET_TST_LVL (crd_det_tst_lvl):** Card Detect Test Level
5	0b RW	**SD8_BIT_MODE (sd8_bit_mode):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card.
4:3	00b RW	**DMA_SEL (dma_sel):** DMA Select
2	0b RW	**HI_SPD_EN (hi_spd_en):** High Speed Enable
1	0b RW	**DATA_TX_WID (data_tx_wid):** Data Transfer Width
0	0b RW	**LED_CTL (led_ctl):** LED Control

3.13.14 Power Control Register (PWR_CTL)—Offset 29h

Power Control Register

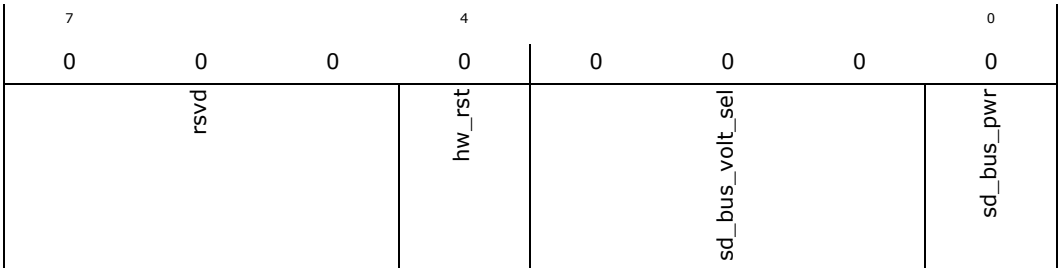
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PWR_CTL: [BAR] + 29h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:5	0h RO	**RSVD (rsvd):** Reserved
4	0b RW	**HW_rst (hw_rst):** HW reset
3:1	0h RW	**SD_BUS_VOLT_SEL (sd_bus_volt_sel):** SD Bus Voltage Select
0	0b RW	**SD_BUS_PWR (sd_bus_pwr):** SD Bus Power

3.13.15 Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah

Block Gap Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

_BLK_GAP_CTL: [BAR] + 2Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd			drive_ccsd	int_blk_gap	rd_wait_ctl	cont_req	stp_blk_gap_req

Bit Range	Default & Access	Description
7:5	0h RO	**RSVD (rsvd):** Reserved
4	0b RW	**DRIVE_CCSD (drive_ccsd):** If the driver set this bit (change from ???0?? to ???1??), Host controller will send command completion
3	0b RW	**INT_BLK_GAP (int_blk_gap):** Interrupt At Block Gap
2	0b RW	**RD_WAIT_CTL (rd_wait_ctl):** Read Wait Control
1	0b RW	**CONT_REQ (cont_req):** Continue Request
0	0b RW	**STP_BLK_GAP_REQ (stp_blk_gap_req):** Stop At Block Gap Request

3.13.16 Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh

This register is used for wakeup event control.

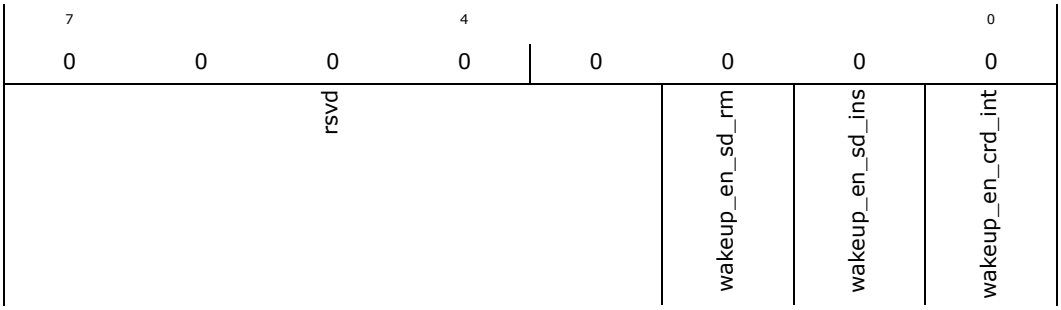
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

WAKEUP_CTL: [BAR] + 2Bh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**WAKEUP_EN_SD_RM (wakeup_en_sd_rm):** Wakeup Event Enable On SD Card Removal
1	0b RW	**WAKEUP_EN_SD_INS (wakeup_en_sd_ins):** Wakeup Event Enable On SD Card Insertion
0	0b RW	**WAKEUP_EN_CRD_INT (wakeup_en_crd_int):** Wakeup Event Enable On Card Interrupt

3.13.17 Clock Control Register (CLK_CTL)—Offset 2Ch

This register is used configure the frequency of the SDIO controller, and enable the clock.

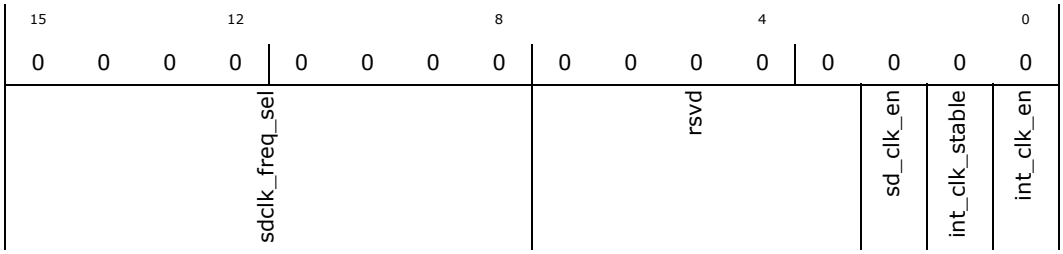
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

CLK_CTL: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RW	**SDCLK_FREQ_SEL (sdclk_freq_sel):** SDCLK Frequency Select
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**SD_CLK_EN (sd_clk_en):** SD Clock Enable
1	0b RO	**INT_CLK_STABLE (int_clk_stable):** Internal Clock Stable
0	0b RW	**INT_CLK_EN (int_clk_en):** Internal Clock Enable

3.13.18 Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh

Timeout Control Register

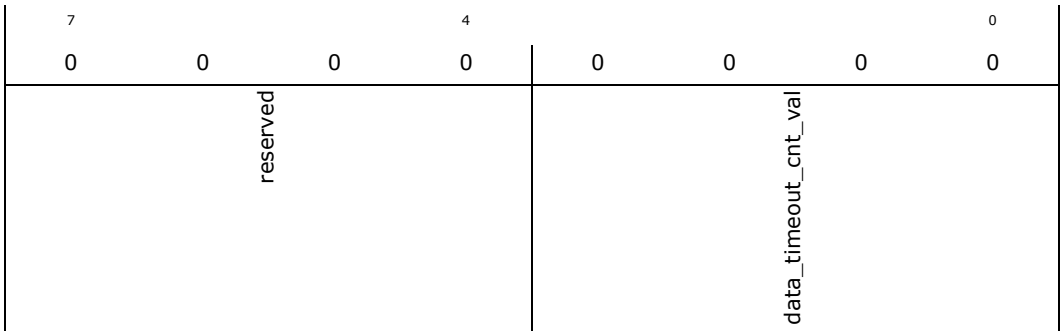
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

TIMEOUT_CTL: [BAR] + 2Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:4	0h RO	**Reserved (reserved):** Reserved

Bit Range	Default & Access	Description
3:0	0h RW	**DATA_TIMEOUT_CNT_VAL (data_timeout_cnt_val):** Data Timeout Counter Value

3.13.19 Software Reset Register (SW_RST)—Offset 2Fh

Software Reset Register

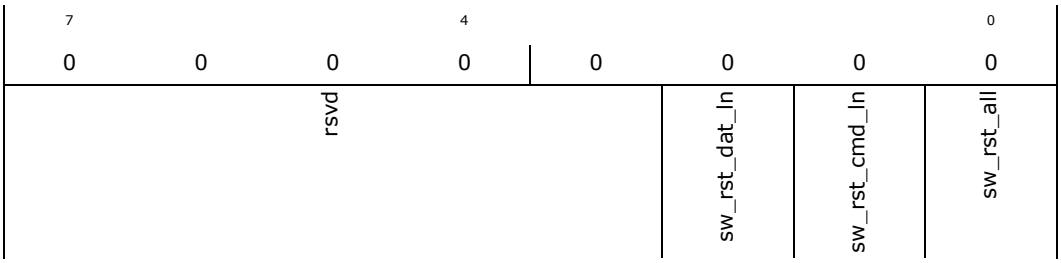
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SW_RST: [BAR] + 2Fh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**SW_RST_DAT_LN (sw_rst_dat_ln):** Software Reset For DAT Line
1	0b RW	**SW_RST_CMD_LN (sw_rst_cmd_ln):** Software Reset For CMD Line
0	0b RW	**SW_RST_ALL (sw_rst_all):** Software Reset For All

3.13.20 Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h

Normal Interrupt Status Register

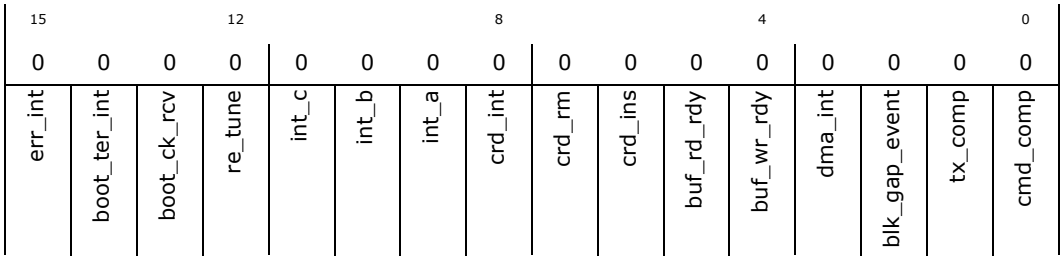
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NML_INT_STATUS: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RO	**ERR_INT (err_int):** Error Interrupt
14	0b RW/1C	**BOOT_TER_INT (boot_ter_int):** boot ter int
13	0b RW/1C	**BOOT_ACK_RCV (boot_ck_rcv):** boot ack rcv
12	0b RO	**RE_TUNE (re_tune):** re tuning event
11	0b RO	**INT_C (int_c):** int c
10	0b RO	**INT_B (int_b):** int b
9	0b RO	**INT_A (int_a):** int a
8	0b RO	**CRD_INT (crd_int):** Card Interrupt
7	0b RW/1C	**CRD_RM (crd_rm):** Card Removal
6	0b RW/1C	**CRD_INS (crd_ins):** Card Insertion
5	0b RW/1C	**BUF_RD_RDY (buf_rd_rdy):** Buffer Read Ready
4	0b RW/1C	**BUF_WR_RDY (buf_wr_rdy):** Buffer Write Ready
3	0b RW/1C	**DMA_INT (dma_int):** DMA Interrupt
2	0b RW/1C	**BLK_GAP_EVENT (blk_gap_event):** Block Gap Event
1	0b RW/1C	**TX_COMP (tx_comp):** Transfer Complete
0	0b RW/1C	**CMD_COMP (cmd_comp):** Command Complete

3.13.21 Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h

Error Interrupt Status Register

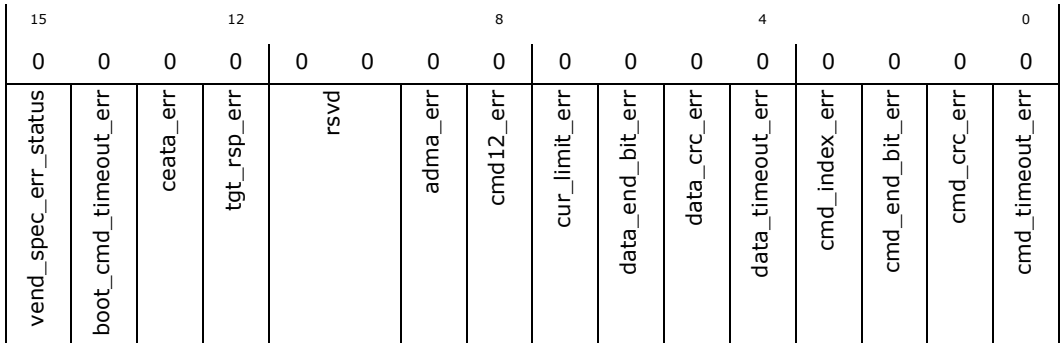
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_STATUS: [BAR] + 32h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**VEND_SPEC_ERR_STATUS (vend_spec_err_status):** Vendor Specific Error Status
14	0b RW	**BOOT_CMD_TIMEOUT_ERR (boot_cmd_timeout_err):** Occur if the boot are access command is issued to the agent which has no permission to access the boot area.
13	0b RW	**CEATA_ERR (ceata_err):** Occurs when ATA command termination has occurred due to an error condition the device has encountered.
12	0b RW	**TGT_RSP_ERR (tgt_rsp_err):** Occurs when detecting ERROR in m_hresp(dma transaction)
11:10	0h RO	**RSVD (rsvd):** Reserved
9	0b RW	**ADMA_ERR (adma_err):** ADMA Error
8	0b RW	**CMD12_ERR (cmd12_err):** Auto CMD12 Error
7	0b RW	**CUR_LIMIT_ERR (cur_limit_err):** Current Limit Error
6	0b RW	**DATA_END_BIT_ERR (data_end_bit_err):** Data End Bit Error
5	0b RW	**DATA_CRC_ERR (data_crc_err):** Data CRC Error
4	0b RW	**DATA_TIMEOUT_ERR (data_timeout_err):** Data Timeout Error
3	0b RW	**CMD_INDEX_ERR (cmd_index_err):** Command Index Error
2	0b RW	**CMD_END_BIT_ERR (cmd_end_bit_err):** Command End Bit Error

Bit Range	Default & Access	Description
1	0b RW	**CMD_CRC_ERR (cmd_crc_err):** Command CRC Error
0	0b RW	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Command Timeout Error

3.13.22 Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h

Normal Interrupt Status Enable

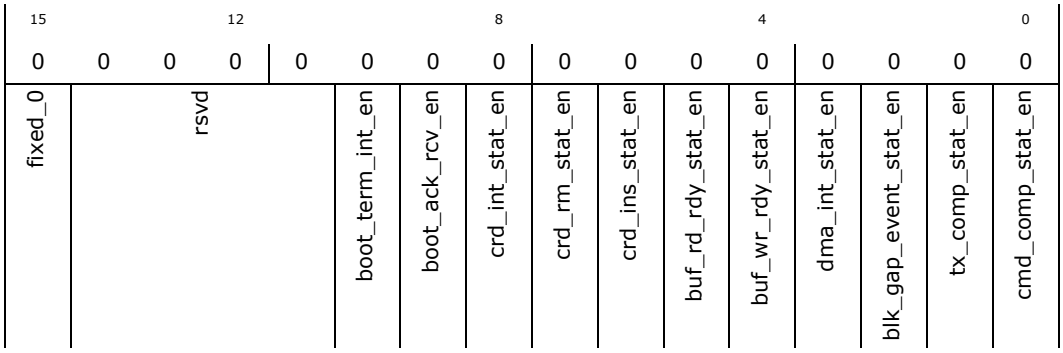
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NRM_INT_STATUS_EN: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RO	**FIXED_0 (fixed_0):** Fixed to 0
14:11	0h RO	**RSVD (rsvd):** Reserved
10	0b RW	**BOOT_TERM_INT_EN (boot_term_int_en):** 0 - Masked
9	0b RW	**BOOT_ACK_RCV_EN (boot_ack_rcv_en):** 0 -Masked
8	0b RW	**CRD_INT_STAT_EN (crd_int_stat_en):** Card Interrupt Status Enable
7	0b RW	**CRD_RM_STAT_EN (crd_rm_stat_en):** Card Removal Status Enable
6	0b RW	**CRD_INS_STAT_EN (crd_ins_stat_en):** Card Insertion Status Enable

Bit Range	Default & Access	Description
5	0b RW	**BUF_RD_RDY_STAT_EN (buf_rd_rdy_stat_en):** Buffer Read Ready Status Enable
4	0b RW	**BUF_WR_RDY_STAT_EN (buf_wr_rdy_stat_en):** Buffer Write Ready Status Enable
3	0b RW	**DMA_INT_STAT_EN (dma_int_stat_en):** DMA Interrupt Status Enable
2	0b RW	**BLK_GAP_EVENT_STAT_EN (blk_gap_event_stat_en):** Block Gap Event Status Enable
1	0b RW	**TX_COMP_STAT_EN (tx_comp_stat_en):** Transfer Complete Status Enable
0	0b RW	**CMD_COMP_STAT_EN (cmd_comp_stat_en):** Command Complete Status Enable

3.13.23 Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h

Error Interrupt Status Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_STAT_EN: [BAR] + 36h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_en	tgt_rsp_err_en	rsvd	tune_err_stat_en	adma_err_stat_en	cmd12_err_stat_en	cur_limit_err_stat_en	data_end_bit_err_stat_en	data_crc_err_stat_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Description
15:14	0b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR_EN (ceata_err_en):** 0 - masked
12	0b RW	**TGT_RSP_ERR_EN (tgt_rsp_err_en):** 0 - masked

Bit Range	Default & Access	Description
11	0b RO	**RSVD (rsvd):** Reserved
10	0b RW	**TUNE_ERR_STATE_EN (tune_err_stat_en):** 0 - masked
9	0b RW	**ADMA_ERR_STAT_EN (adma_err_stat_en):** ADMA Error Status Enable
8	0b RW	**CMD12_ERR_STAT_EN (cmd12_err_stat_en):** Auto CMD12 Error Status Enable
7	0b RW	**CUR_LIMIT_ERR_STAT_EN (cur_limit_err_stat_en):** Current Limit Error Status Enable
6	0b RW	**DATA_END_BIT_ERR_STAT_EN (data_end_bit_err_stat_en):** Data End Bit Error Status Enable
5	0b RW	**DATA_CRC_ERR_STAT_EN (data_crc_err_stat_en):** Data CRC Error Status Enable
4	0b RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Status Enable
3	0b RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Status Enable
2	0b RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Status Enable
1	0b RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Status Enable
0	0b RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Status Enable

3.13.24 Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h

Normal Interrupt Signal Enable Register

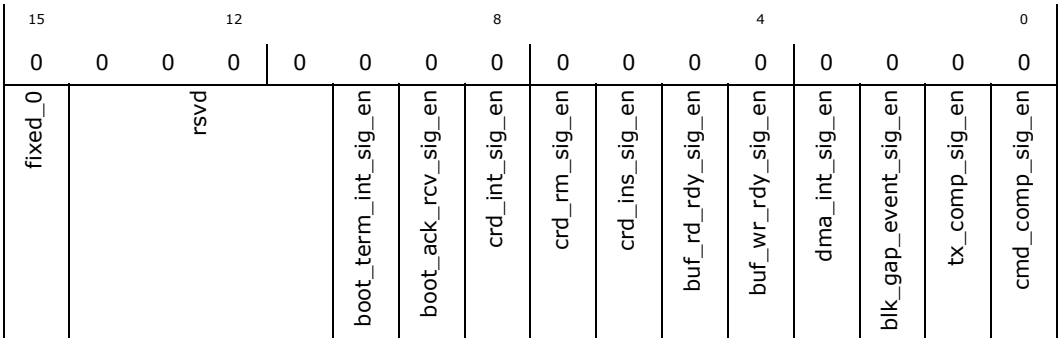
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NRM_INT_SIG_EN: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

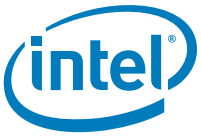


Bit Range	Default & Access	Description
15	0b RO	**FIXED_0 (fixed_0):** Fixed to 0
14:11	0h RO	**RSVD (rsvd):** Reserved
10	0b RW	**BOOT_TERM_INT_SIG_EN (boot_term_int_sig_en):** 0 - masked
9	0b RW	**BOOT_ACK_RCV_SIG_EN (boot_ack_rcv_sig_en):** 0 - masked
8	0b RW	**CRD_INT_SIG_EN (crd_int_sig_en):** Card Interrupt Signal Enable
7	0b RW	**CRD_RM_SIG_EN (crd_rm_sig_en):** Card Removal Signal Enable
6	0b RW	**CRD_INS_SIG_EN (crd_ins_sig_en):** Card Insertion Signal Enable
5	0b RW	**BUF_RD_RDY_SIG_EN (buf_rd_rdy_sig_en):** Buffer Read Ready Signal Enable
4	0b RW	**BUF_WR_RDY_SIG_EN (buf_wr_rdy_sig_en):** Buffer Write Ready Signal Enable
3	0b RW	**DMA_INT_SIG_EN (dma_int_sig_en):** DMA Interrupt Signal Enable
2	0b RW	**BLK_GAP_EVENT_SIG_EN (blk_gap_event_sig_en):** Block Gap Event Signal Enable
1	0b RW	**TX_COMP_SIG_EN (tx_comp_sig_en):** Transfer Complete Signal Enable
0	0b RW	**CMD_COMP_SIG_EN (cmd_comp_sig_en):** Command Complete Signal Enable

3.13.25 Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah

Error Interrupt Signal Enable Register

Access Method



Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_SIG_EN: [BAR] + 3Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_sig_en	tgt_err_rsp_sig_en	rsvd	tune_err_sig	adma_err_sig_en	cmd12_err_sig_en	cur_limit_err_sig_en	data_end_bit_err_sig_en	data_crc_err_sig_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Description
15:14	0b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR_SIG_EN (ceata_err_sig_en):** 0 - masked
12	0b RW	**TGT_ERR_RSP_SIG_EN (tgt_err_rsp_sig_en):** 0 - masked
11	0b RO	**RSVD (rsvd):** Reserved
10	0b RW	**TUNE_ERR_SIG (tune_err_sig):** 0 - masked
9	0b RW	**ADMA_ERR_SIG_EN (adma_err_sig_en):** ADMA Error Signal Enable
8	0b RW	**CMD12_ERR_SIG_EN (cmd12_err_sig_en):** Auto CMD12 Error Signal Enable
7	0b RW	**CUR_LIMIT_ERR_SIG_EN (cur_limit_err_sig_en):** Current Limit Error Signal Enable
6	0b RW	**DATA_END_BIT_ERR_SIG_EN (data_end_bit_err_sig_en):** Data End Bit Error Signal Enable
5	0b RW	**DATA_CRC_ERR_SIG_EN (data_crc_err_sig_en):** Data CRC Error Signal Enable
4	0b RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Signal Enable
3	0b RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Signal Enable
2	0b RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Signal Enable

Bit Range	Default & Access	Description
1	0b RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Signal Enable
0	0b RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Signal Enable

3.13.26 Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch

Auto CMD12 Error Status Register and Host control 2 Register

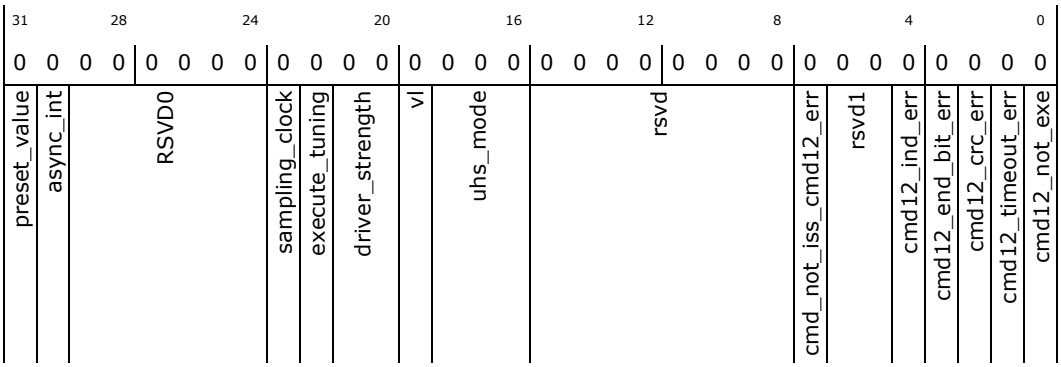
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CMD12_ERR_STAT_HOST_CTRL_2: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**PRESET_VALUE (preset_value):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic This bit enables the functions defined in the Preset Value registers. 1 Automatic Selection by Preset Value are Enabled 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.

Bit Range	Default & Access	Description
30	0b RW	**ASYNC_INT (async_int):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 1 Enabled 0 Disabled
29:24	0b RO	**RSVD0:** Reserved
23	0b RW	**SAMPLING_CLOCK (sampling_clock):** This bit is set by tuning procedure when Execute Tuning is cleared
22	0b RW/AC	**EXECUTE_TUNING (execute_tuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 1 Execute Tuning 0 Not Tuned or Tuning Completed
21:20	0b RW	**DRIVER_STRENGTH (driver_strength):** Host Controller output driver in 1.8V signaling is selected by this bit
19	0b RW	**VL (vl):** This bit controls voltage regulator for I/O cell
18:16	0b RW	**UHS_MODE (uhs_mode):** This field is used to select one of UHS-I modes
15:8	0h RO	**RSVD (rsvd):** Reserved
7	0b RO	**CMD_NOT_ISS_CMD12_ERR (cmd_not_iss_cmd12_err):** Command Not Issued By Auto CMD12 Error
6:5	0h RO	**RSVD1 (rsvd1):** Reserved
4	0b RO	**CMD12_IND_ERR (cmd12_ind_err):** Auto CMD12 Index Error
3	0b RO	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Auto CMD12 End Bit Error
2	0b RO	**CMD12_CRC_ERR (cmd12_crc_err):** Auto CMD12 CRC Error
1	0b RO	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Auto CMD12 Timeout Error
0	0b RO	**CMD12_NOT_EXE (cmd12_not_exe):** Auto CMD12 Not Executed

3.13.27 Capabilities Register (CAPABILITIES)—Offset 40h

Capabilities Register

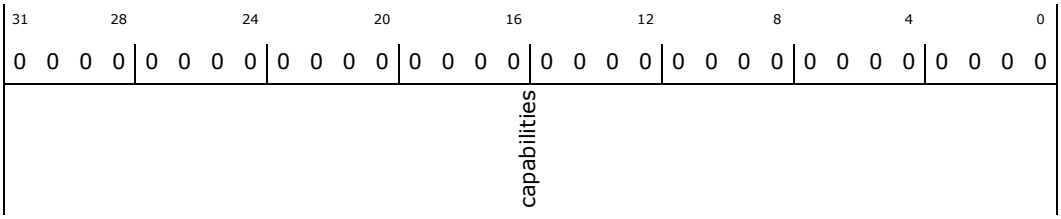
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITIES: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**capabilities:** capabilities

3.13.28 Capabilities Register 2 (CAPABILITIES_2)—Offset 44h

Capabilities Register 2

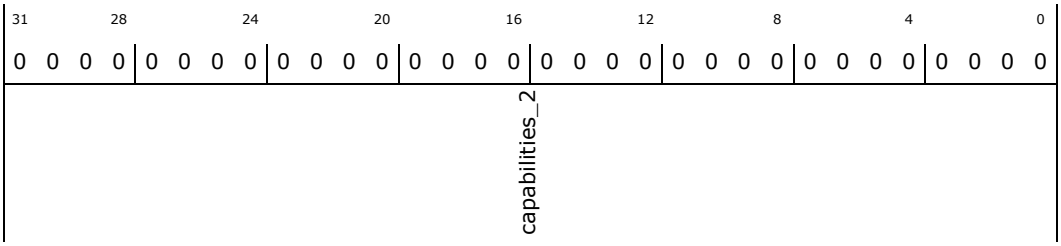
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITIES_2: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**capabilities_2:** capabilities 2

3.13.29 Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h

These registers indicate maximum current capability for each voltage

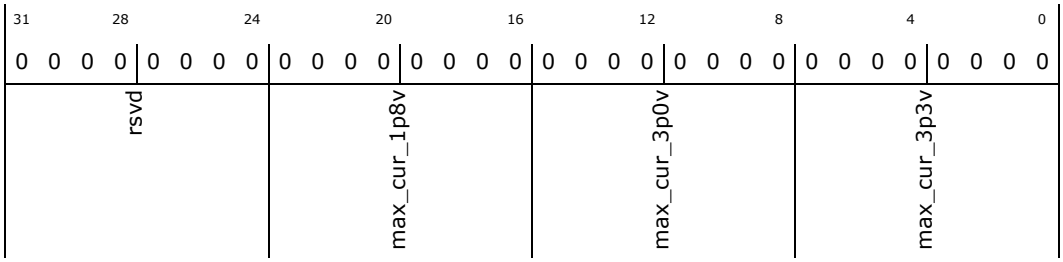
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MAX_CUR_CAP: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**RSVD (rsvd):** Reserved
23:16	00h RO	**MAX_CUR_1p8V (max_cur_1p8v):** Maximum Current for 1.8V
15:8	00h RO	**MAX_CUR_3p0V (max_cur_3p0v):** Maximum Current for 3.0V
7:0	00h RO	**MAX_CUR_3p3V (max_cur_3p3v):** Maximum Current for 3.3V

3.13.30 Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h

Force Event Register for Auto CMD12 Error Status

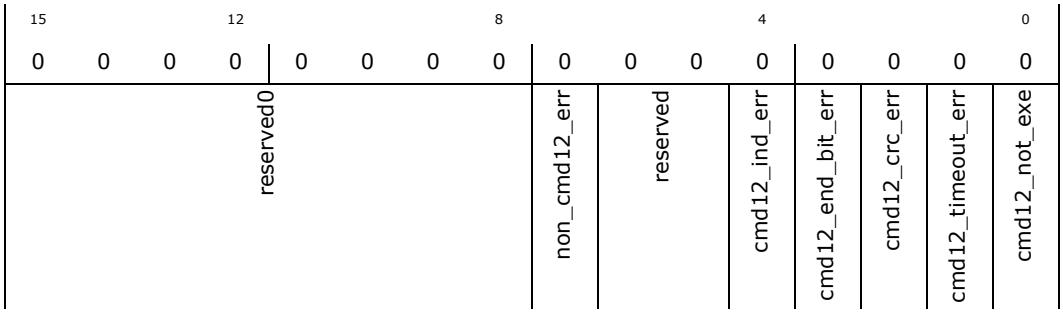
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

FORCE_EVENT_CMD12_ERR_STAT: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**Reserved0 (reserved0):** Reserved
7	0b RW	**NON_CMD12_ERR (non_cmd12_err):** Force Event for Command Not Issued By Auto CMD12 Error :
6:5	00b RO	**Reserved (reserved):** Reserved
4	0b RW	**CMD12_IND_ERR (cmd12_ind_err):** Force Event for Auto CMD12 Index Error
3	0b RW	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Force Event for Auto CMD12 End Bit Error
2	0b RW	**CMD12_CRC_ERR (cmd12_crc_err):** Force Event for Auto CMD12 CRC Error
1	0b RW	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Force Event for Auto CMD12 Timeout Error
0	0b RW	**CMD12_NOT_EXE (cmd12_not_exe):** Force Event for Auto CMD12 Not Executed

3.13.31 Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h

Force Event Register for Error Interrupt Status

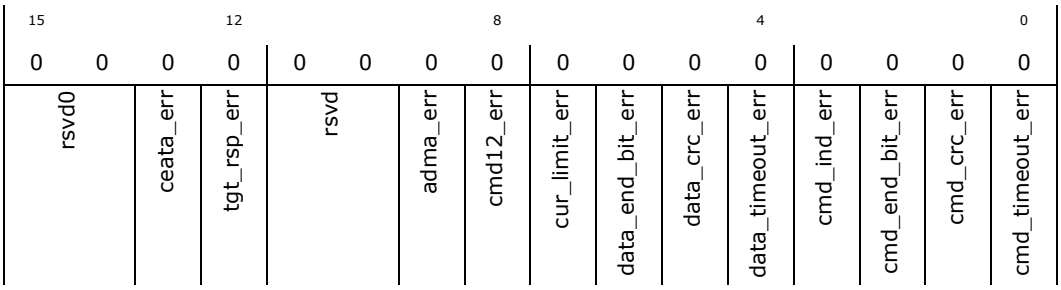
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

FORCE_EVENT_ERR_INT_STAT: [BAR] + 52h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:14	00b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR (ceata_err):** Force Event for CEATA error

Bit Range	Default & Access	Description
12	0b RW	**TGT_RSP_ERR (tgt_rsp_err):** Force Event for Target Response Error
11:10	0h RO	**RSVD (rsvd):** Reserved
9	0b RW	**ADMA_ERR (adma_err):** Force Event for ADMA Error
8	0b RW	**CMD12_ERR (cmd12_err):** Force Event for Auto CMD12 Error
7	0b RW	**CUR_LIMIT_ERR (cur_limit_err):** Force Event for Current Limit Error
6	0b RW	**DATA_END_BIT_ERR (data_end_bit_err):** Force Event for Data End Bit Error
5	0b RW	**DATA_CRC_ERR (data_crc_err):** Event for Data CRC Error
4	0b RW	**DATA_TIMEOUT_ERR (data_timeout_err):** Event for Data Timeout Error
3	0b RW	**CMD_IND_ERR (cmd_ind_err):** Force Event for Command Index Error
2	0b RW	**CMD_END_BIT_ERR (cmd_end_bit_err):** Force Event for Command End Bit Error
1	0b RW	**CMD_CRC_ERR (cmd_crc_err):** Force Event for Command CRC Error
0	0b RW	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Force Event for Command Timeout Error

3.13.32 ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h

ADMA Error Status Register

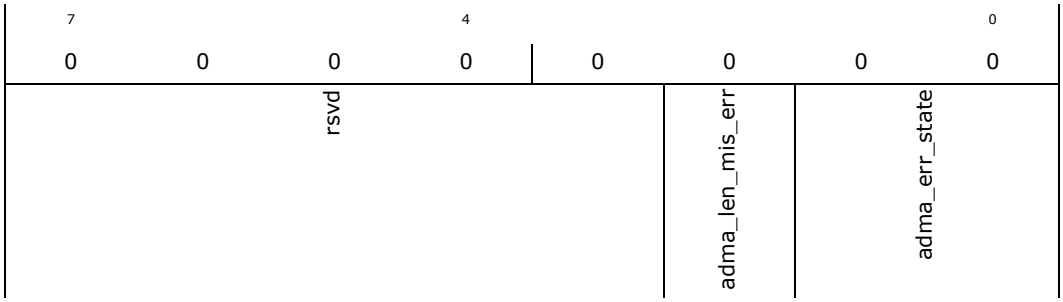
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

ADMA_ERR_STAT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RO	**ADMA_LEN_MIS_ERR (adma_len_mis_err):** ADMA Length Mismatch Error
1:0	00b RO	**ADMA_ERR_STATE (adma_err_state):** ADMA Error State

3.13.33 ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h

This register contains the physical Descriptor address used for ADMA data transfer.

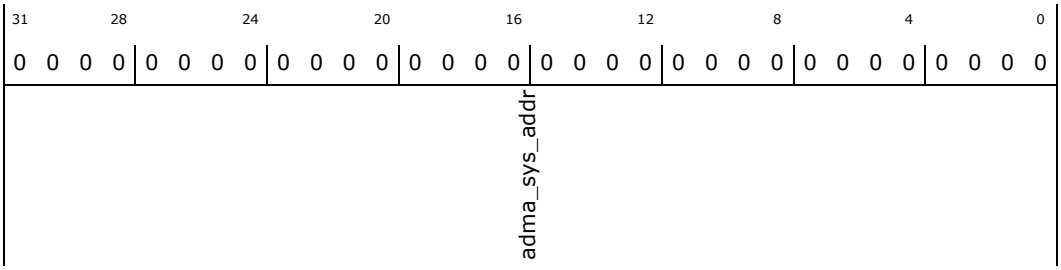
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ADMA_SYS_ADDR: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**ADMA_SYS_ADDR (adma_sys_addr):** ADMA System Address

3.13.34 Preset Values registers (PRESET_VALUE_0)—Offset 60h

Preset Values init and default speed

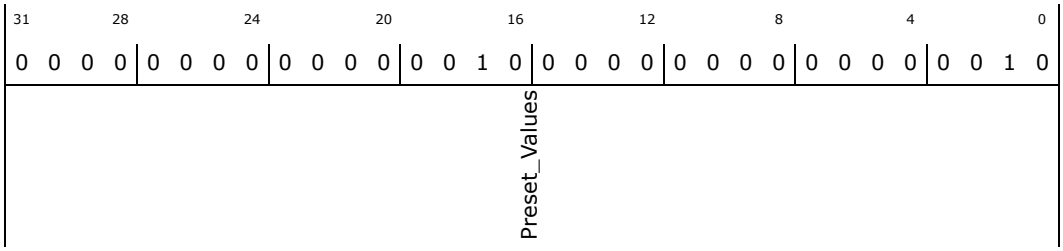
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_0: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00020002h



Bit Range	Default & Access	Description
31:0	00020002h RO	**PresetValues (Preset_Values):** Reserved.

3.13.35 Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h

Preset Values high and sdr12

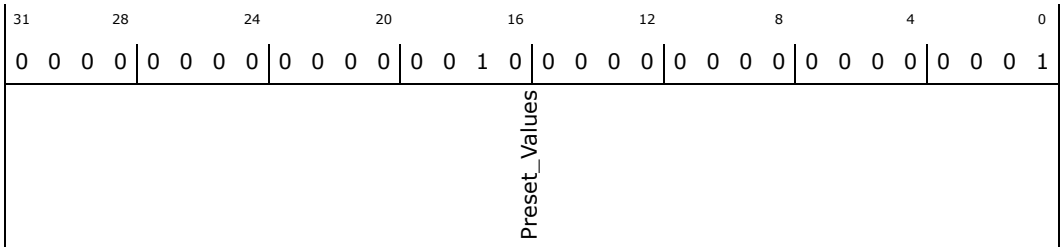
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_1: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00020001h



Bit Range	Default & Access	Description
31:0	00020001h RO	**PresetValues (Preset_Values):** Reserved.

3.13.36 Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h

Preset Values sdr25 and sdr50

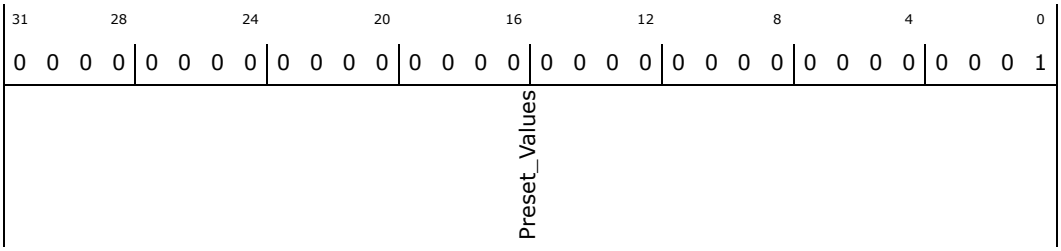
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_2: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:0	00000001h RO	**PresetValues (Preset_Values):** Reserved.

3.13.37 Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch

Preset Values sdr104 and ddr50

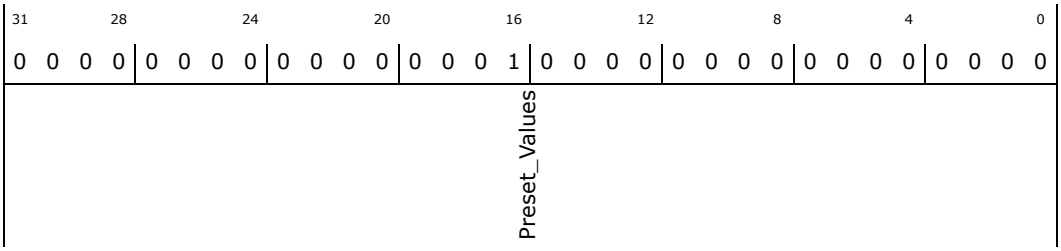
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_3: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31:0	00010000h RO	**PresetValues (Preset_Values):** Reserved.

3.13.38 BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h

BOOT_TIMEOUT_CTRL

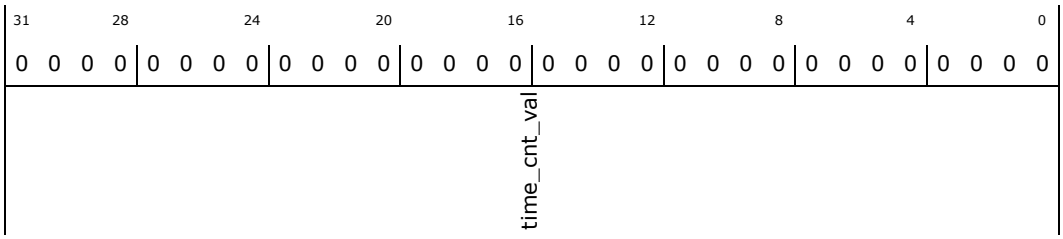
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BOOT_TIMEOUT_CTRL: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**TIME_CNT_VAL (time_cnt_val):** Boot Data Timeout Counter Value

3.13.39 DEBUG_SEL (DEBUG_SEL)—Offset 74h

Debug Selection Register

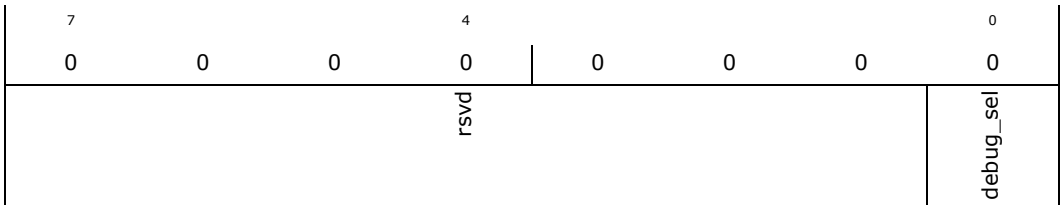
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

DEBUG_SEL: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:1	00h RO	**RSVD (rsvd):** Reserved
0	0b WO	**DEBUG_SEL (debug_sel):** 1 - cmd register, interrupt status, transmitter module, ahb_iface module and clk sdcard signals are probed out..

3.13.40 Shared Bus Control Register (SHARED_BUS)—Offset E0h

Shared Bus Control Register

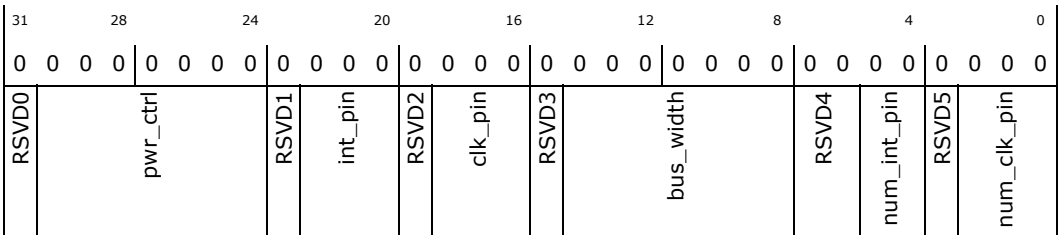
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SHARED_BUS: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**RSVD0:** Reserved
30:24	0h RW	**PWR_CTRL (pwr_ctrl):** Each bit of this field controls back-end power supply for an embedded device. Host interface voltage (VDDH) is not controlled by this field. The number of devices supported is specified by Number of Clock Pins and a maximum of 7 devices can be controlled D24 Back-end Power Control for Device 1 D25 Back-end Power Control for Device 2 D26 Back-end Power Control for Device 3 D27 Back-end Power Control for Device 4 D28 Back-end Power Control for Device 5 D29 Back-end Power Control for Device 6 D30 Back-end Power Control for Device 7 The function of each bit is defined as follows: 0 Back-end Power is Off 1 Back-end Power is Supplied Back-End power control is effective for embedded memory devices in the Sleep State that support the Sleep command (CMD14) to reduce power consumption and embedded SDIO devices when IOEx is set to 0.
23	0b RO	**RSVD1:** Reserved
22:20	0h RW	**INT_PIN (int_pin):** Interrupt pin inputs are enabled by this field. Enable of unsupported interrupt pin is meaningless. 000b Interrupt is detected by Interrupt Cycle xx1b INT_A is Enabled x1xb INT_B is Enabled 1xxb INT_C is Enabled
19	0b RO	**RSVD2:** Reserved
18:16	0h RW	**CLK_PIN (clk_pin):** One of clock pin outputs is selected by this field. Select of unsupported clock pin is meaningless. Refer to Figure 2-38 for the timing of clock outputs. 000b Clock Pins are Disabled 001b CLK[1] is Selected 010b CLK[2] is Selected .... 111b CLK[7] is Selected
15	0b RO	**RSVD3:** Reserved

Bit Range	Default & Access	Description
14:8	0h RO	**BUS_WIDTH (bus_width):** Shared bus supports mixing of 4-bit and 8-bit bus width devices. Each bit of this field specifies the bus width for each embedded device. The number of devices supported is specified by Number of Clock Pins and a maximum of 7 devices are supported.This field is effective when multiple devices are connected to a shared bus (Slot Type is set to 10b in the Capabilities register). In the other case, Extended Data Transfer Width in the Host Control 1 register is used to select 8-bit bus width. As use of 1-bit mode is not intended for shared bus, Data Transfer Width in the Host Control 1 register should be set to 1.D08 - Bus width preset for Device 1 D09 - Bus width preset for Device 2 D10 - Bus width preset for Device 3 D11 - Bus width preset for Device 4 D12 - Bus width preset for Device 5 D13 - Bus width preset for Device 6 D14 - Bus width preset for Device 7 The function of each bit is defined as follows: 0 - 4 bit bus width mode 1 - 8 bit bus width mode
7:6	0b RO	**RSVD4:** Reserved
5:4	0h RO	**NUM_INT_PIN (num_int_pin):** This field indicates support of interrupt input pins for shared bus system.Three asynchronous interrupt pins are defined, INT_A#, INT_B# and INT_C#. Which interrupt pin is used is determined by the system. Each one is driven by open drain and then wired or connection is possible. 00b Interrupt Input Pin is Not Supported 01b INTA is Supported 10b INTA and INTB are Supported 11b INTA, INTB and INTC are Supported
3	0b RO	**RSVD5:** Reserved
2:0	0h RO	**NUM_CLK_PIN (num_clk_pin):** This field indicates support of clock pins to select one of devices for shared bus system. Up to 7 clock pins can be supported.Shared bus is supported by specific system. Then Standard Host Driver does not support control of these clock pins. 000b Shared bus is not supported 001b 1 SDCLK pin is supported 010b 2 SDCLK pins are supported .... 111b 7 SDCLK pins are supported

3.13.41 SPI_INT_SUP (SPI_INT_SUP)—Offset F0h

SPI_INT_SUP

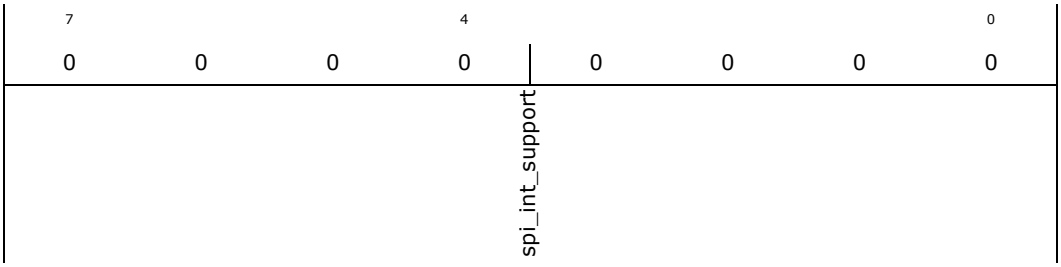
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SPI_INT_SUP: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**SPI_INT_SUPPORT (spi_int_support):** This bit is set to indicate the assertion assertion of interrupts in the SPI mode at any time, irrespective of the status of thecard select (CS) line. If this bit is zero, then SDIO card can only assert the interrupt line in the SPI mode when the CS line is asserted.

3.13.42 Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh

Slot Interrupt Status Register

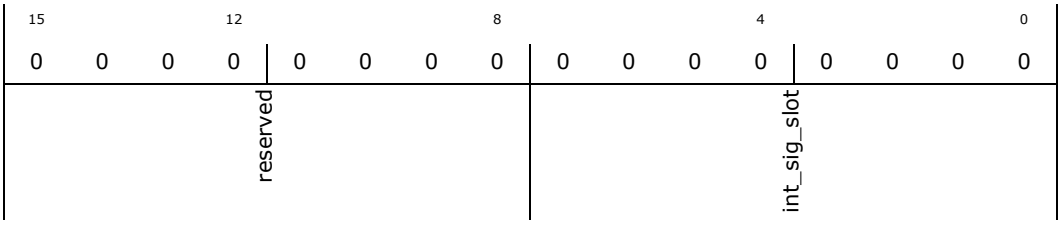
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

SLOT_INT_STAT: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**Reserved (reserved):** Reserved
7:0	00h RO	**INT_SIG_SLOT (int_sig_slot):** Interrupt Signal For Each Slot

3.13.43 Host Controller Version Register (HOST_CTRL_VER)—Offset FEh

Host Controller Version Register

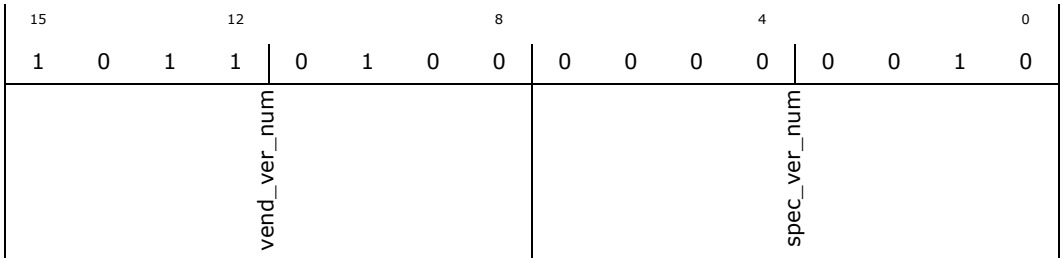
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

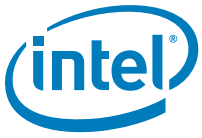
HOST_CTRL_VER: [BAR] + FEh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: B402h



Bit Range	Default & Access	Description
15:8	b4h RO	**VEND_VER_NUM (vend_ver_num):** Vendor Version Number
7:0	02h RO	**SPEC_VER_NUM (spec_ver_num):** Version Number



3.14 eMMC 4.5 PCI Configuration Registers

Table 22. Summary of eMMC 4.5 PCI Configuration Registers—0/23/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 1615	00000000h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 1616	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 1617	00000000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 1618	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 1618	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 1619	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 1620	00000000h
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 1620	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 1621	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 1621	00000100h
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 1622	48030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 1623	00000008h
A0h	4	"reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h" on page 1623	00000000h
A4h	4	"reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h" on page 1624	00000000h
A8h	4	"reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h" on page 1624	00000000h
ACh	4	"reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh" on page 1625	00000000h
C0h	4	"reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h" on page 1625	00000000h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 1626	00000000h

3.14.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

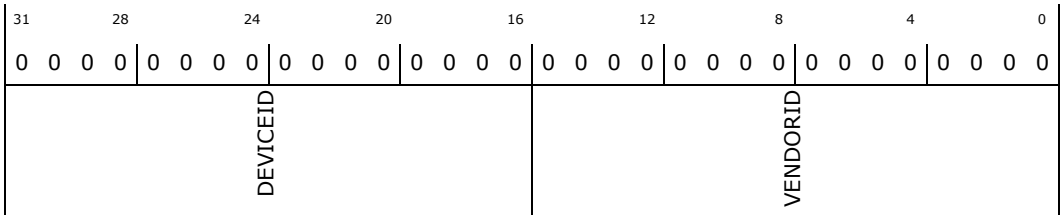
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:23, F:0] + 0h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**DEVICEID:** Reserved.
15:0	0000h RO	**VENDORID:** Reserved.

3.14.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

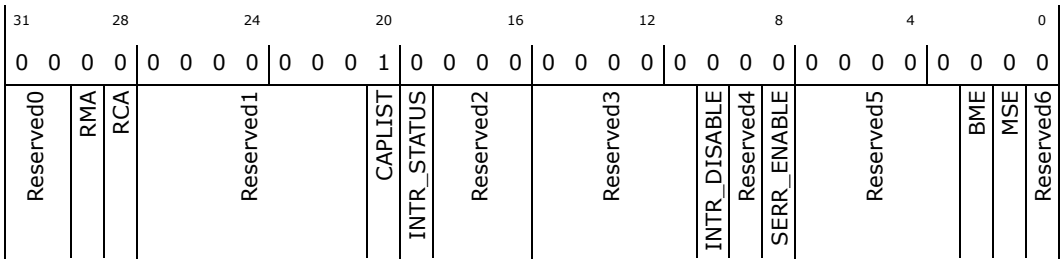
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:23, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** Reserved.
29	0h RW/1C	**RMA:** Reserved.
28	0h RW/1C	**RCA:** Reserved.
27:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**CAPLIST:** Reserved.
19	0h RO	**INTR_STATUS:** Reserved.

Bit Range	Default & Access	Description
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**INTR_DISABLE:** Reserved.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR_ENABLE:** Reserved.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**BME:** Reserved.
1	0h RW	**MSE:** Reserved.
0	0h RO	**Reserved6:** Reserved.

3.14.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

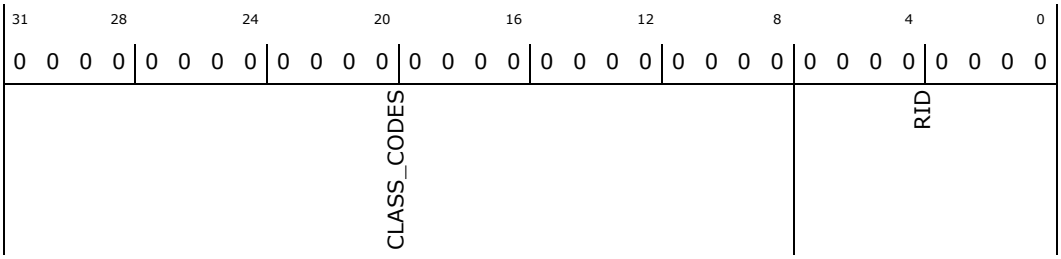
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:23, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**CLASS_CODES:** Reserved.
7:0	00h RO	**RID:** Reserved.

3.14.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

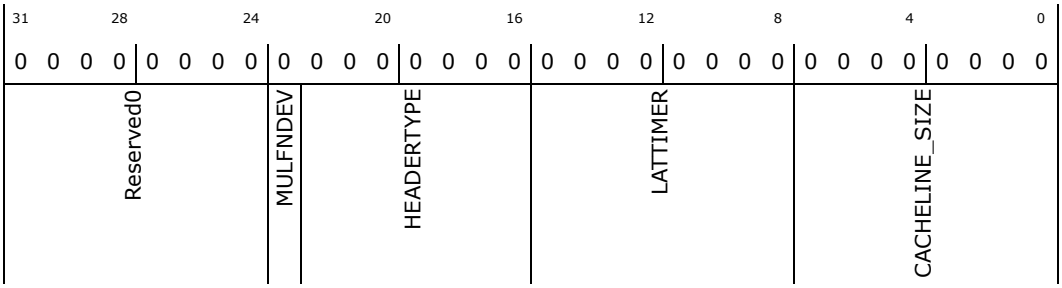
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:23, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	0h RO	**MULFNDEV:** Reserved.
22:16	00h RO	**HEADERTYPE:** Reserved.
15:8	00h RO	**LATTIMER:** Reserved.
7:0	00h RW	**CACHELINE_SIZE:** Reserved.

3.14.5 reg_BAR_type (BAR)—Offset 10h

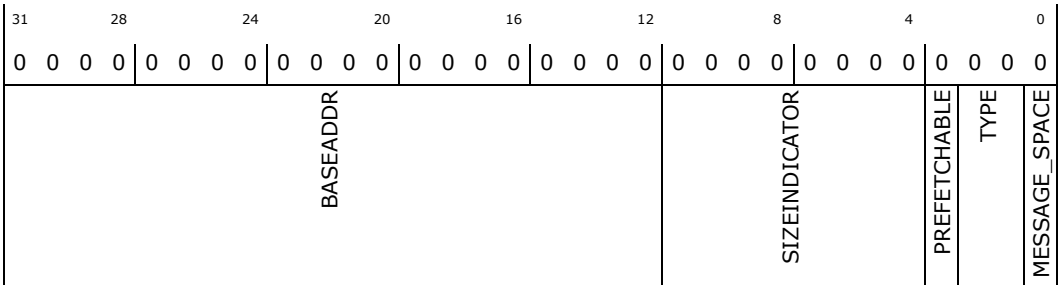
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Reserved.
11:4	00h RO	**SIZEINDICATOR:** Reserved.
3	0h RO	**PREFETCHABLE:** Reserved.
2:1	0h RO	**TYPE:** Reserved.
0	0h RO	**MESSAGE_SPACE:** Reserved.

3.14.6 reg_BAR1_type (BAR1)—Offset 14h

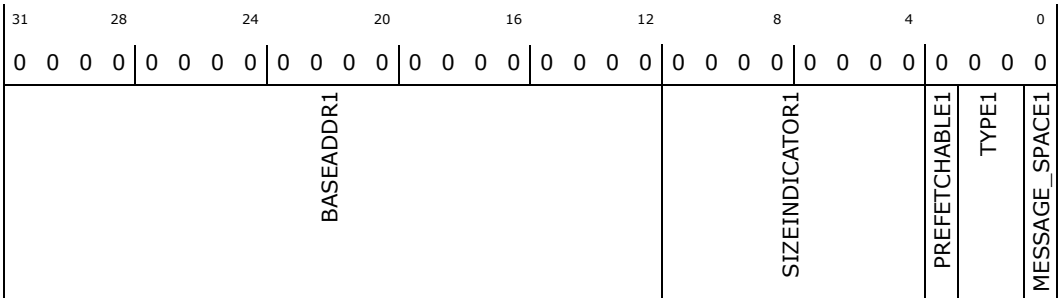
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:23, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** Reserved.
11:4	00h RO	**SIZEINDICATOR1:** Reserved.

Bit Range	Default & Access	Description
3	0h RO	**PREFETCHABLE1:** Reserved.
2:1	0h RO	**TYPE1:** Reserved.
0	0h RO	**MESSAGE_SPACE1:** Reserved.

3.14.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

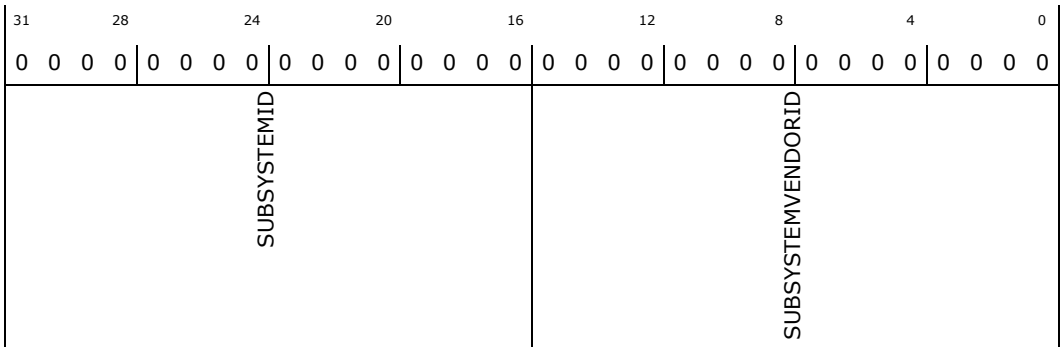
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:23, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Reserved.
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Reserved.

3.14.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

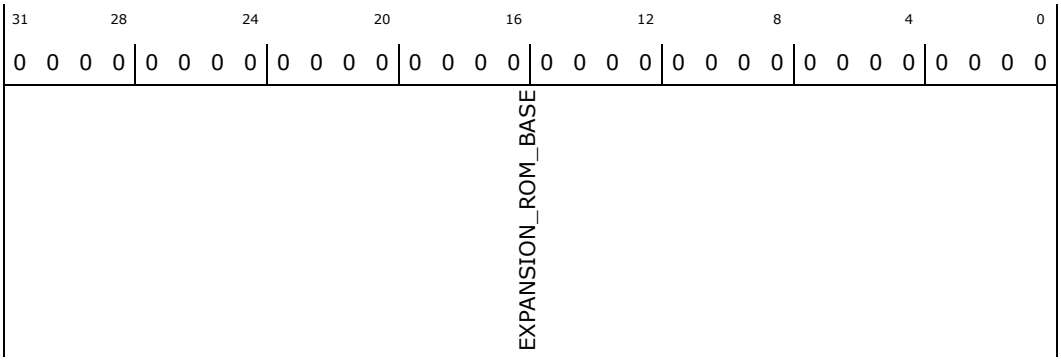
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:23, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

3.14.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

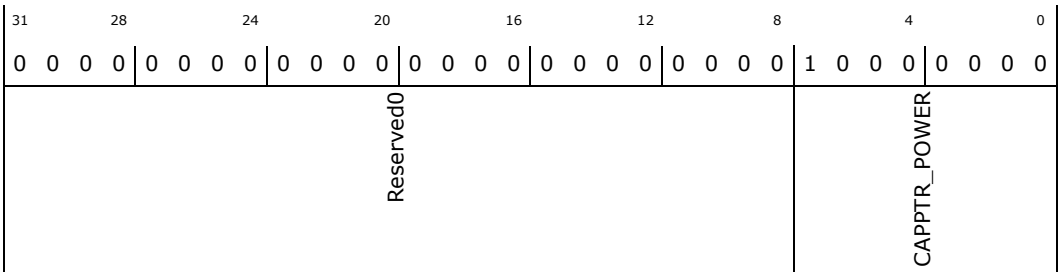
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:23, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	80h RO	**CAPPTR_POWER:** Reserved.

3.14.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

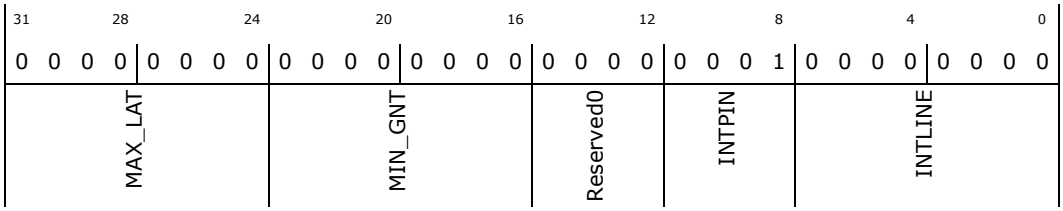
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:23, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Reserved.
23:16	00h RO	**MIN_GNT:** Reserved.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**INTPIN:** Reserved.
7:0	00h RW	**INTLINE:** Reserved.

3.14.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

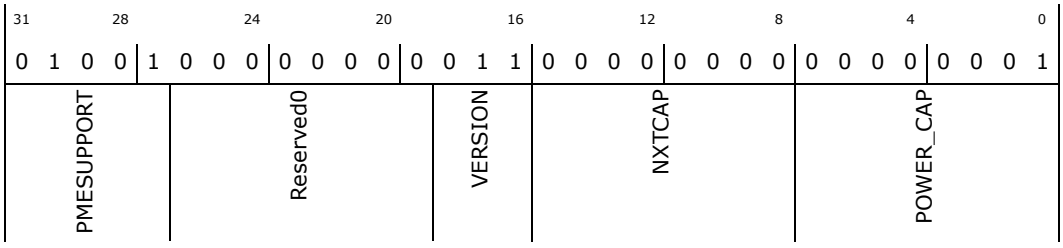
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:23, F:0] + 80h

Default: 48030001h



Bit Range	Default & Access	Description
31:27	09h RO	**PMESUPPORT:** Reserved.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**VERSION:** Reserved.

Bit Range	Default & Access	Description
15:8	00h RO	**NXTCAP:** Reserved.
7:0	01h RO	**POWER_CAP:** Reserved.

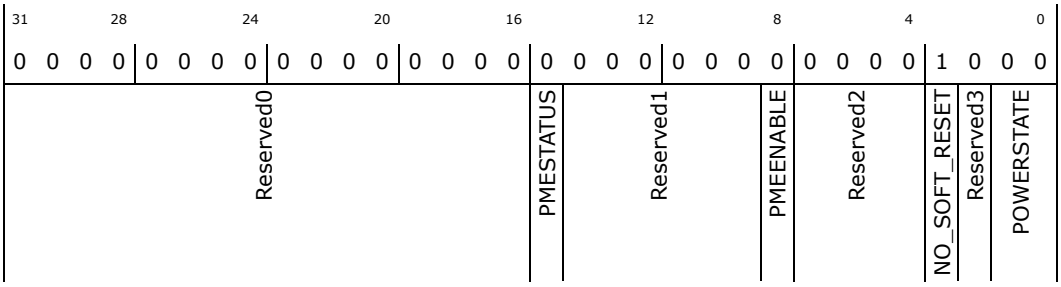
3.14.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:23, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PMESTATUS:** Reserved.
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PMEENABLE:** Reserved.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**NO_SOFT_RESET:** Reserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**POWERSTATE:** Reserved.

3.14.13 reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h

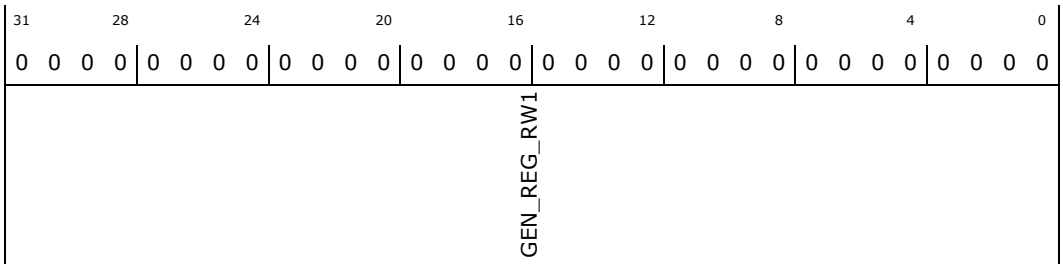
General Purpose Read Write Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW1: [B:0, D:23, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW1:** capabilities over-ride for the sd/sdio/emmc host controller (bits 31:0)

3.14.14 reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h

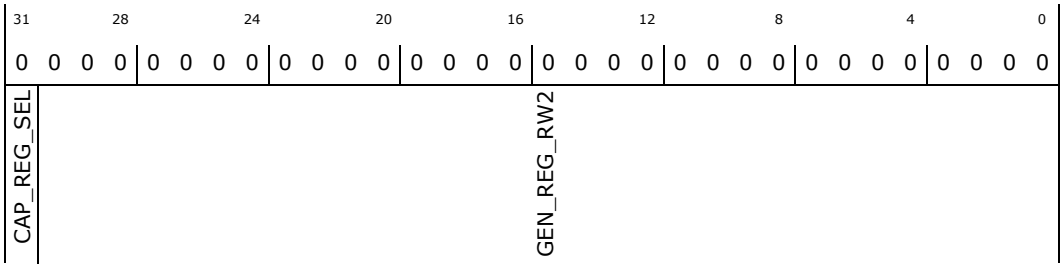
General Purpose Read Write Register2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW2: [B:0, D:23, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**CAP_REG_SEL:** select if the capability will come from the GEN PCI register or from a hard wire
30:0	0h RW	**GEN_REG_RW2:** capabilities over-ride for the sd/sdio/emmc host controller (bits 62:32)

3.14.15 reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h

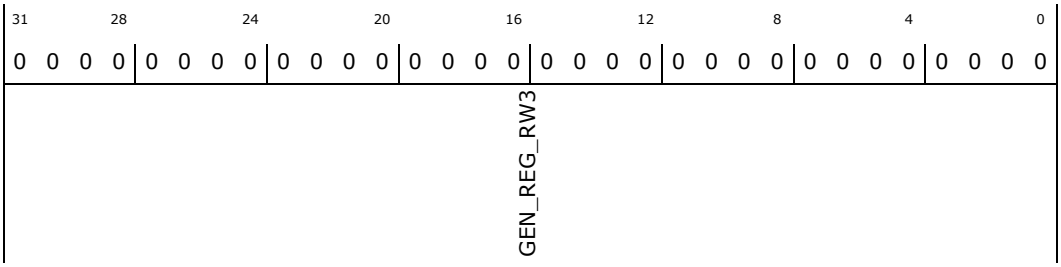
General Purpose Read Write Register3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW3: [B:0, D:23, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW3:** Reserved.

3.14.16 reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh

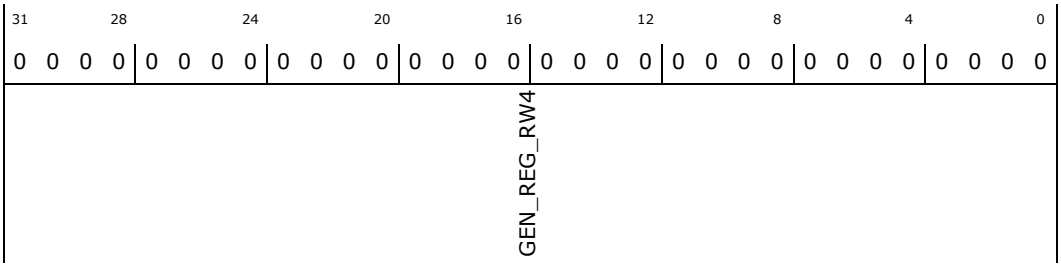
General Purpose Read Write Register4

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW4: [B:0, D:23, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW4:** Reserved.

3.14.17 reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h

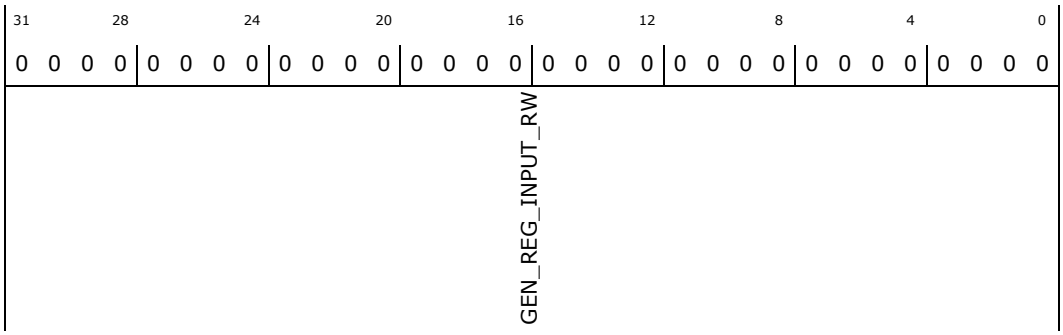
General Purpose Input Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_INPUT_REGRW: [B:0, D:23, F:0] + C0h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**GEN_REG_INPUT_RW:** Reserved.

3.14.18 reg_MANID_type (MANID)—Offset F8h

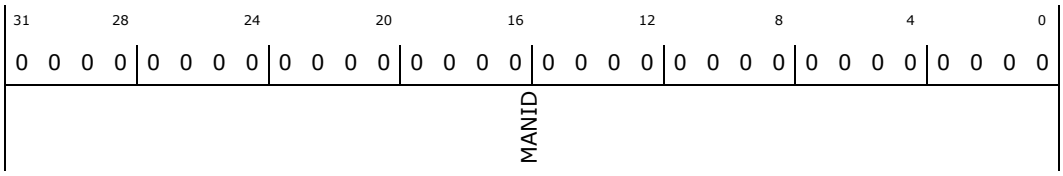
Manufacturers ID

Access Method

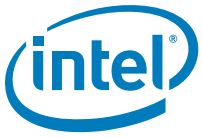
Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:23, F:0] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**MANID:** Reserved.



3.15 eMMC 4.5 Memory Mapped IO Registers

Table 23. Summary of eMMC 4.5 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"SDMA System Address Register (SYS_ADR)—Offset 0h" on page 1628	00000000h
4h	2	"Block Size Register (BLK_SIZE)—Offset 4h" on page 1629	0000h
6h	2	"Block Count Register (BLK_COUNT)—Offset 6h" on page 1630	0000h
8h	4	"Argument Register (ARGUMENT)—Offset 8h" on page 1631	00000000h
Ch	2	"Transfer Mode Register (TX_MODE)—Offset Ch" on page 1631	0000h
Eh	2	"Command Register (CMD)—Offset Eh" on page 1632	0000h
10h	4	"Response Register0 (RESPONSE0)—Offset 10h" on page 1633	00000000h
14h	4	"Response Register2 (RESPONSE2)—Offset 14h" on page 1634	00000000h
18h	4	"Response Register4 (RESPONSE4)—Offset 18h" on page 1634	00000000h
1Ch	4	"Response Register6 (RESPONSE6)—Offset 1Ch" on page 1635	00000000h
20h	4	"Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h" on page 1636	00000000h
24h	4	"Present State Register (PRE_STATE)—Offset 24h" on page 1636	1FFF0000h
28h	1	"Host Control Register (HOST_CTL)—Offset 28h" on page 1637	00h
29h	1	"Power Control Register (PWR_CTL)—Offset 29h" on page 1638	00h
2Ah	1	"Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah" on page 1639	00h
2Bh	1	"Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh" on page 1640	00h
2Ch	2	"Clock Control Register (CLK_CTL)—Offset 2Ch" on page 1640	0000h
2Eh	1	"Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh" on page 1641	00h
2Fh	1	"Software Reset Register (SW_RST)—Offset 2Fh" on page 1642	00h
30h	2	"Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h" on page 1642	0000h
32h	2	"Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h" on page 1643	0000h
34h	2	"Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h" on page 1645	0000h
36h	2	"Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h" on page 1646	0000h
38h	2	"Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h" on page 1647	0000h
3Ah	2	"Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah" on page 1648	0000h
3Ch	4	"Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch" on page 1650	00000000h
40h	4	"Capabilities Register (CAPABILITIES)—Offset 40h" on page 1651	00000000h
44h	4	"Capabilities Register 2 (CAPABILITIES_2)—Offset 44h" on page 1652	00000000h

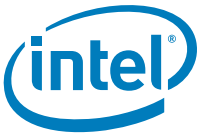


Table 23. Summary of eMMC 4.5 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
48h	4	"Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h" on page 1652	00000000h
50h	2	"Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h" on page 1653	0000h
52h	2	"Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h" on page 1654	0000h
54h	1	"ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h" on page 1655	00h
58h	4	"ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h" on page 1656	00000000h
60h	4	"Preset Values registers (PRESET_VALUE_0)—Offset 60h" on page 1656	00020002h
64h	4	"Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h" on page 1657	00020001h
68h	4	"Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h" on page 1657	00000001h
6Ch	4	"Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch" on page 1658	00010000h
70h	4	"BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h" on page 1658	00000000h
74h	1	"DEBUG_SEL (DEBUG_SEL)—Offset 74h" on page 1659	00h
E0h	4	"Shared Bus Control Register (SHARED_BUS)—Offset E0h" on page 1659	00000000h
F0h	1	"SPI_INT_SUP (SPI_INT_SUP)—Offset F0h" on page 1661	00h
FCh	2	"Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh" on page 1662	0000h
FEh	2	"Host Controller Version Register (HOST_CTRL_VER)—Offset FEh" on page 1662	B402h

3.15.1 SDMA System Address Register (SYS_ADR)—Offset 0h

This register contains the physical system memory address used for DMA transfers

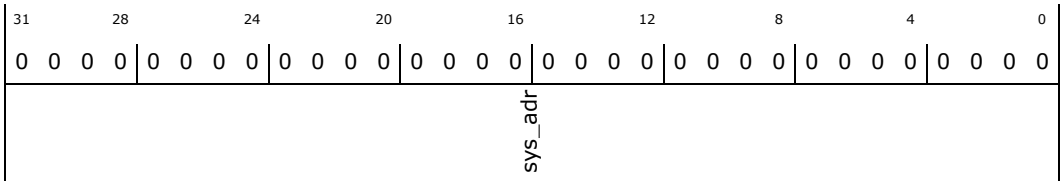
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SYS_ADR: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**SYS_ADR (sys_adr):** SDMA System Address This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register.

3.15.2 Block Size Register (BLK_SIZE)—Offset 4h

This register is used to configure the number of bytes in a data block.

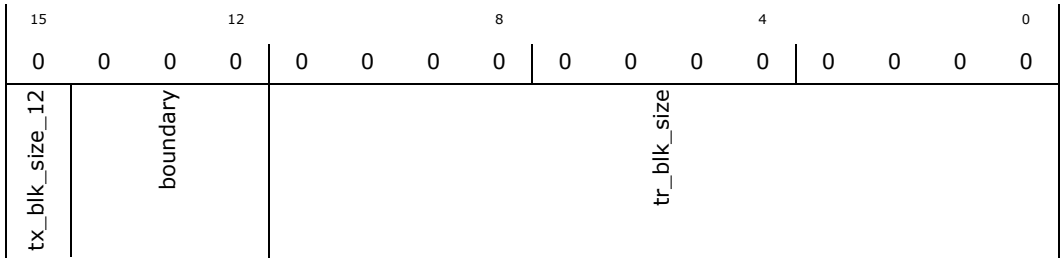
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

BLK_SIZE: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**TX_BLK_SIZE_12 (tx_blk_size_12):** Transfer Block Size 12th bit. This bit is added to support 4Kb Data block transfer.

Bit Range	Default & Access	Description
14:12	000b RW	**BOUNDARY (boundary):** Host SDMA Buffer Boundary The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. ADMA does not use this register. 000b - 4K bytes (Detects A11 carry out) 001b - 8K bytes (Detects A12 carry out) 010b - 16K Bytes (Detects A13 carry out) 011b - 32K Bytes (Detects A14 carry out) 100b - 64K bytes (Detects A15 carry out) 101b - 128K Bytes (Detects A16 carry out) 110b - 256K Bytes (Detects A17 carry out) 111b - 512K Bytes (Detects A18 carry out)
11:0	000h RW	**TR_BLK_SIZE (tr_blk_size):** Transfer Block Size This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes (Refer to Implementation Note in Section 1.7.2). It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. 0800h 2048 Bytes ??? ??? 0200h 512 Bytes 01FFh 511 Bytes ??? ??? 0004h 4 Bytes 0003h 3 Bytes 0002h 2 Bytes 0001h 1 Byte 0000h No data transfer

3.15.3 Block Count Register (BLK_COUNT)—Offset 6h

This register is used to configure the number of data blocks

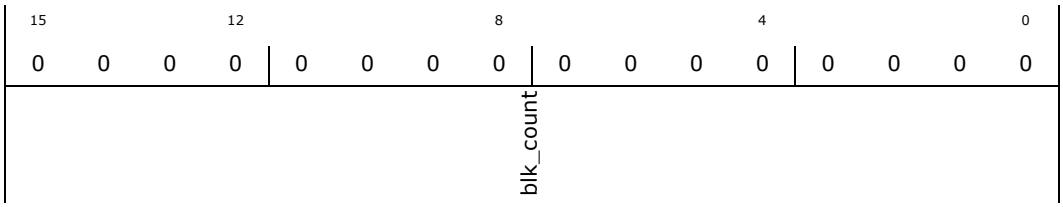
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

BLK_COUNT: [BAR] + 6h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	0000h RW	**BLK_COUNT (blk_count):** Blocks Count For Current Transfer This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers

3.15.4 Argument Register (ARGUMENT)—Offset 8h

This register contains the SD Command Argument.

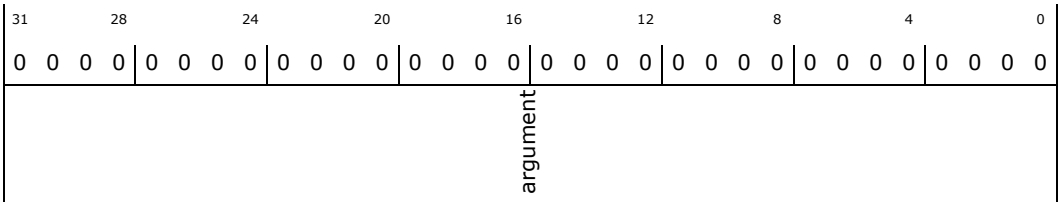
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ARGUMENT: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**ARGUMENT (argument):** Command Argument The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

3.15.5 Transfer Mode Register (TX_MODE)—Offset Ch

Transfer Mode Register

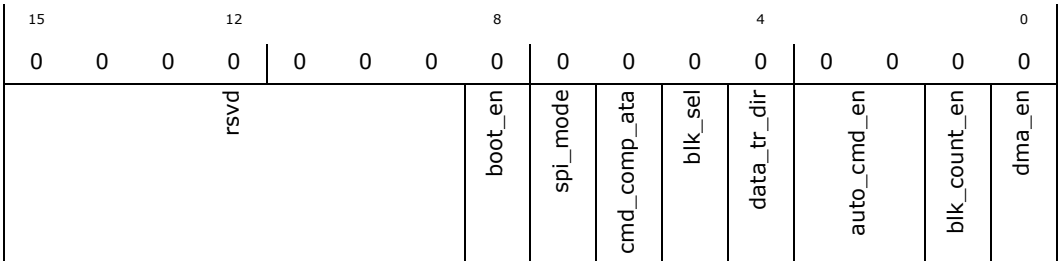
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

TX_MODE: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:9	00h RO	**RSVD (rsvd):** Reserved
8	0b RW	**BOOT_EN (boot_en):** To start boot operation for MMC4.3 1 - To start boot mode 0 - Stop the boot read
7	0b RW	**SPI_MODE (spi_mode):** SPI mode enable bit. 1 - SPI mode 0 - SD mode
6	0b RW	**CMD_COMP_ATA (cmd_comp_ata):** Command Completion Signal Enable for CE-ATA Device. ???1??? - Device will send command completion Signal ???0??? - Device will not send command completion Signal
5	0b RW	**BLK_SEL (blk_sel):** Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the Block Count register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block
4	0b RW	**Data_TR_Dir (data_tr_dir):** Data Transfer Direction Select This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller and it is set to 0 for all other commands. 1 Read (Card to Host) 0 Write (Host to Card)
3:2	0b RW	**AUTO_CMD_EN (auto_cmd_en):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0b RW	**BLK_COUNT_EN (blk_count_en):** Block Count Enable This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8) If ADMA2 data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table. 1 Enable 0 Disable
0	0b RW	**DMA_EN (dma_en):** DMA Enable This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the Capabilities register. One of the DMA modes can be selected by DMA Select in the Host Control register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of Command register (00Fh). 1 DMA Data transfer 0 No data transfer or Non DMA data transfer

3.15.6 Command Register (CMD)—Offset Eh

Command Register

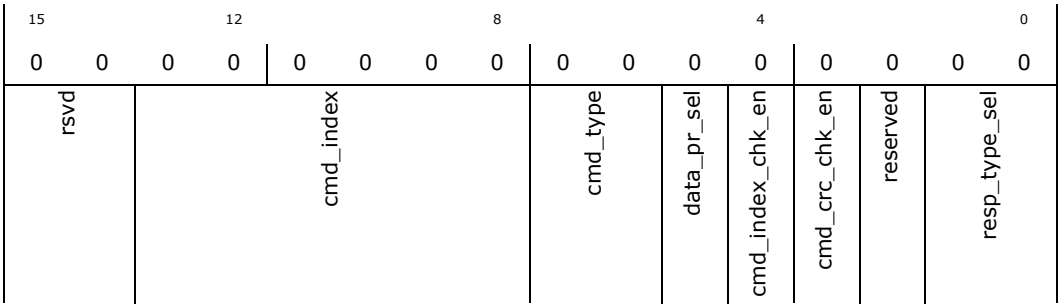
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

CMD: [BAR] + Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:14	0h RO	**RSVD (rsvd):** Reserved
13:8	0h RW	**CMD_INDEX (cmd_index):** Command Index These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.
7:6	00b RW	**CMD_TYPE (cmd_type):** Command Type
5	0b RW	**DATA_PR_SEL (data_pr_sel):** Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) (3) Resume command 1 Data Present 0 No Data Present
4	0b RW	**CMD_INDEX_CHK_EN (cmd_index_chk_en):** Command Index Check Enable If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 1 Enable 0 Disable
3	0b RW	**CMD_CRC_CHK_EN (cmd_crc_chk_en):** Command CRC Check Enable If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response. (Refer to definition in D01-00 and Table 2-10 below.) 1 Enable 0 Disable
2	0b RO	**Reserved (reserved):** Reserved
1:0	0h RW	**RESP_TYPE_SEL (resp_type_sel):** Response Type Select 00 No Response 01 Response Length 136 10 Response Length 48 11 Response Length 48 check Busy after response

3.15.7 Response Register0 (RESPONSE0)—Offset 10h

This register is used to store responses from SD cards

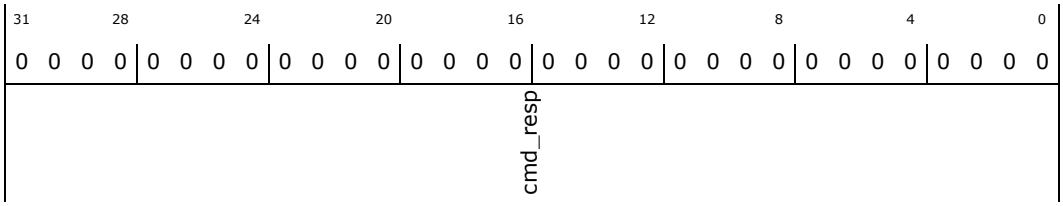
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE0: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP0 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.15.8 Response Register2 (RESPONSE2)—Offset 14h

This register is used to store responses from SD cards

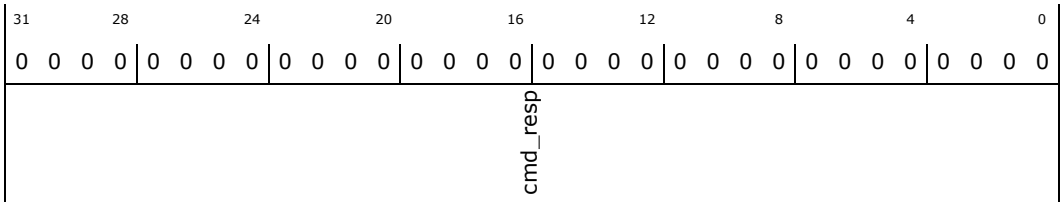
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE2: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP2 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.15.9 Response Register4 (RESPONSE4)—Offset 18h

This register is used to store responses from SD cards

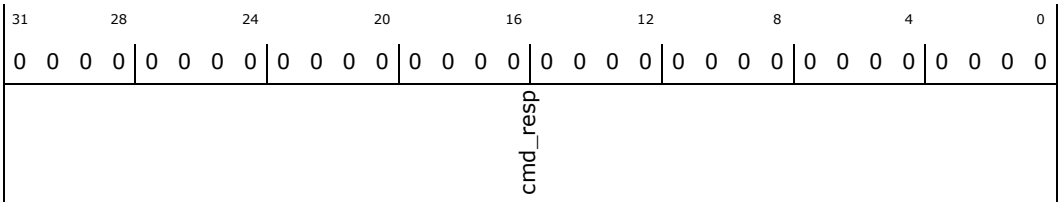
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE4: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP4 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.15.10 Response Register6 (RESPONSE6)—Offset 1Ch

This register is used to store responses from SD cards

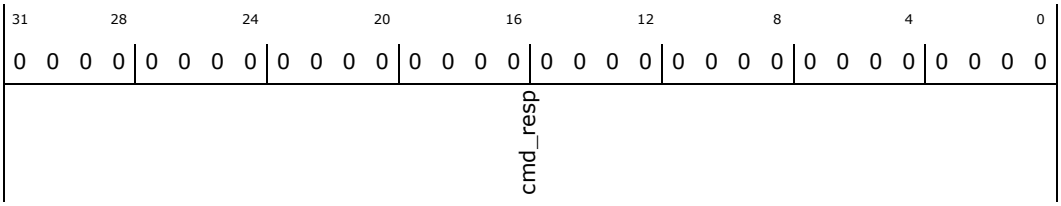
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESPONSE6: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**CMD_RESP6 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

3.15.11 Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h

32-bit data port register to access internal buffer

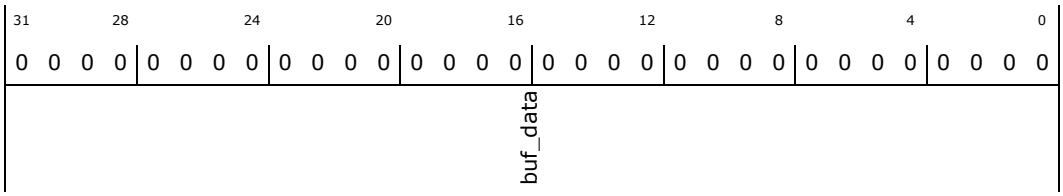
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BUF_DATA_PORT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUF_DATA (buf_data):** Buffer Data The Host Controller buffer can be accessed through this 32-bit Data Port register. Refer to 1.7

3.15.12 Present State Register (PRE_STATE)—Offset 24h

The Host Driver can get status of the Host Controller from this 32-bit read only register

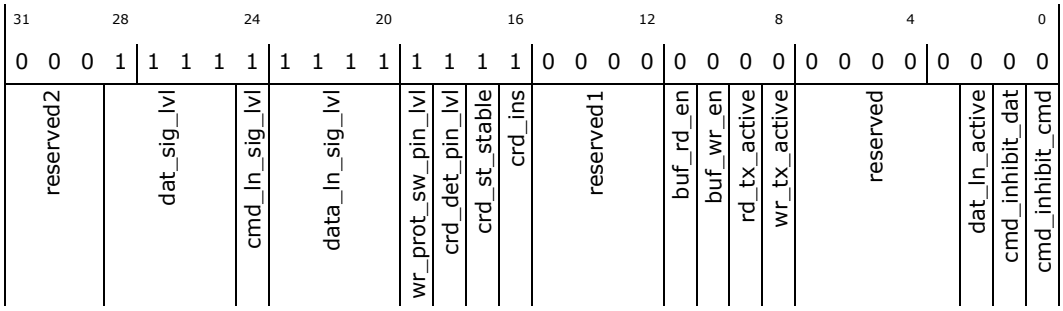
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRE_STATE: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 1FFF0000h



Bit Range	Default & Access	Description
31:29	0h RO	**Reserved2 (reserved2):** Reserved

Bit Range	Default & Access	Description
28:25	1111b RO	**DAT_SIG_LVL (dat_sig_lvl):** This status is used to check DAT line level to recover from errors, and for debugging. D28 - DAT[7] D27 - DAT[6] D26 - DAT[5] D25 - DAT[4]
24	1b RO	**CMD_LN_SIG_LVL (cmd_ln_sig_lvl):** CMD Line Signal Level This status is used to check the CMD line level to recover from errors, and for debugging.
23:20	Fh RO	**DATA_LN_SIG_LVL (data_ln_sig_lvl):** DAT[3:0] Line Signal Level This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D23 DAT[3] D22 DAT[2] D21 DAT[1] D20 DAT[0]
19	1b RO	**WR_PROT_SW_PIN_LVL (wr_prot_sw_pin_lvl):** Write Protect Switch Pin Level
18	1b RO	**CRD_DET_PIN_LVL (crd_det_pin_lvl):** Card Detect Pin Level
17	1b RO	**CRD_ST_STABLE (crd_st_stable):** Card State Stable
16	1b RO	**CRD_INS (crd_ins):** Card Inserted
15:12	0h RO	**Reserved1 (reserved1):** Reserved
11	0b RO	**BUF_RD_EN (buf_rd_en):** Buffer Read Enable
10	0b RO	**BUF_WR_EN (buf_wr_en):** Buffer Write Enable
9	0b RO	**RD_TX_ACTIVE (rd_tx_active):** Read Transfer Active
8	0b RO	**WR_TX_ACTIVE (wr_tx_active):** Write Transfer Active
7:3	00h RO	**Reserved (reserved):** Reserved
2	0b RO	**DAT_LN_ACTIVE (dat_ln_active):** DAT Line Active
1	0b RO	**CMD_INHIBIT_DAT (cmd_inhibit_dat):** Command Inhibit (DAT)
0	0b RO	**CMD_INHIBIT_CMD (cmd_inhibit_cmd):** Command Inhibit (CMD)

3.15.13 Host Control Register (HOST_CTL)—Offset 28h

Host Control Register

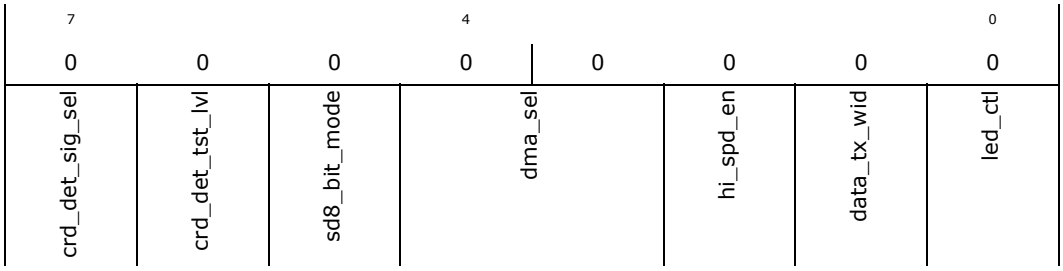
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

HOST_CTL: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7	0b RW	**CRD_DET_SIG_SEL (crd_det_sig_sel):** Card Detect Signal Selection
6	0b RW	**CRD_DET_TST_LVL (crd_det_tst_lvl):** Card Detect Test Level
5	0b RW	**SD8_BIT_MODE (sd8_bit_mode):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card.
4:3	00b RW	**DMA_SEL (dma_sel):** DMA Select
2	0b RW	**HI_SPD_EN (hi_spd_en):** High Speed Enable
1	0b RW	**DATA_TX_WID (data_tx_wid):** Data Transfer Width
0	0b RW	**LED_CTL (led_ctl):** LED Control

3.15.14 Power Control Register (PWR_CTL)—Offset 29h

Power Control Register

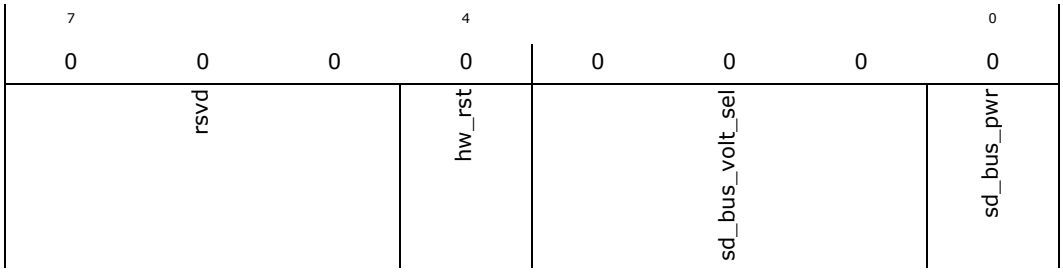
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PWR_CTL: [BAR] + 29h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:5	0h RO	**RSVD (rsvd):** Reserved
4	0b RW	**HW_rst (hw_rst):** HW reset
3:1	0h RW	**SD_BUS_VOLT_SEL (sd_bus_volt_sel):** SD Bus Voltage Select
0	0b RW	**SD_BUS_PWR (sd_bus_pwr):** SD Bus Power

3.15.15 Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah

Block Gap Control Register

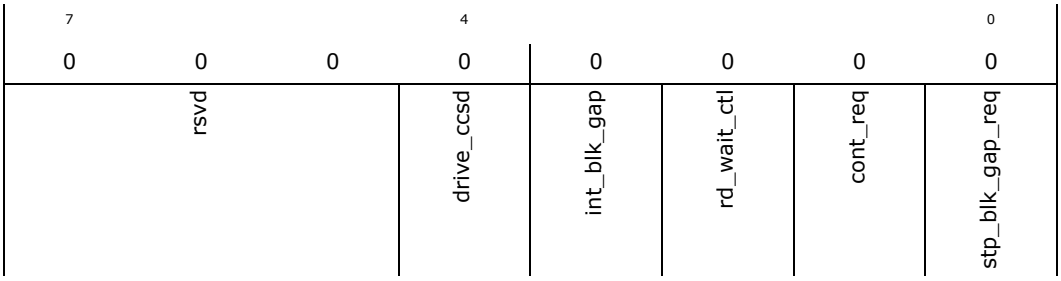
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

_BLK_GAP_CTL: [BAR] + 2Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:5	0h RO	**RSVD (rsvd):** Reserved
4	0b RW	**DRIVE_CCSD (drive_ccsd):** If the driver set this bit (change from ???0?? to ???1??), Host controller will send command completion
3	0b RW	**INT_BLK_GAP (int_blk_gap):** Interrupt At Block Gap
2	0b RW	**RD_WAIT_CTL (rd_wait_ctl):** Read Wait Control
1	0b RW	**CONT_REQ (cont_req):** Continue Request
0	0b RW	**STP_BLK_GAP_REQ (stp_blk_gap_req):** Stop At Block Gap Request

3.15.16 Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh

This register is used for wakeup event control.

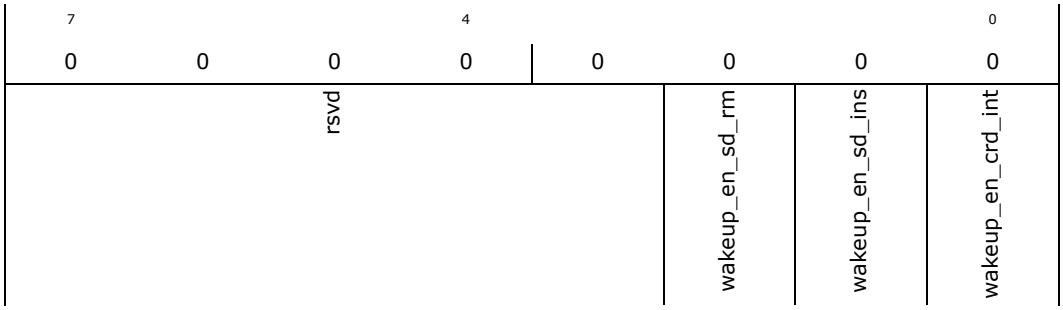
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

WAKEUP_CTL: [BAR] + 2Bh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**WAKEUP_EN_SD_RM (wakeup_en_sd_rm):** Wakeup Event Enable On SD Card Removal
1	0b RW	**WAKEUP_EN_SD_INS (wakeup_en_sd_ins):** Wakeup Event Enable On SD Card Insertion
0	0b RW	**WAKEUP_EN_CRD_INT (wakeup_en_crd_int):** Wakeup Event Enable On Card Interrupt

3.15.17 Clock Control Register (CLK_CTL)—Offset 2Ch

This register is used configure the frequency of the SDIO controller, and enable the clock.

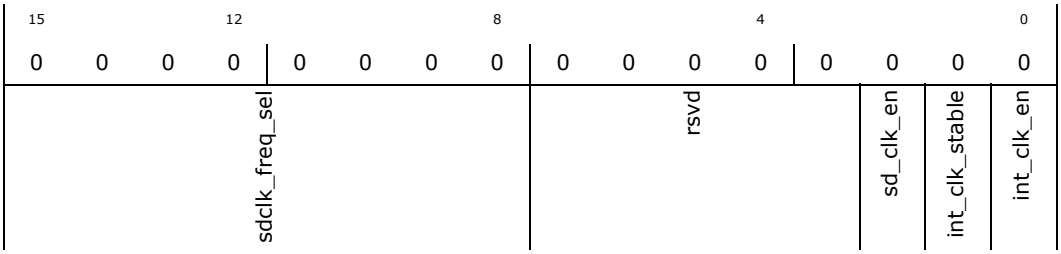
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

CLK_CTL: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RW	**SDCLK_FREQ_SEL (sdclk_freq_sel):** SDCLK Frequency Select
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**SD_CLK_EN (sd_clk_en):** SD Clock Enable
1	0b RO	**INT_CLK_STABLE (int_clk_stable):** Internal Clock Stable
0	0b RW	**INT_CLK_EN (int_clk_en):** Internal Clock Enable

3.15.18 Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh

Timeout Control Register

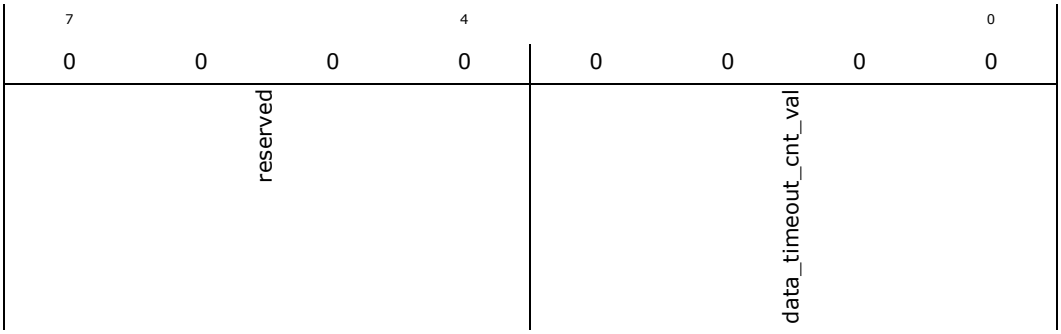
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

TIMEOUT_CTL: [BAR] + 2Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:4	0h RO	**Reserved (reserved):** Reserved

Bit Range	Default & Access	Description
3:0	0h RW	**DATA_TIMEOUT_CNT_VAL (data_timeout_cnt_val):** Data Timeout Counter Value

3.15.19 Software Reset Register (SW_RST)—Offset 2Fh

Software Reset Register

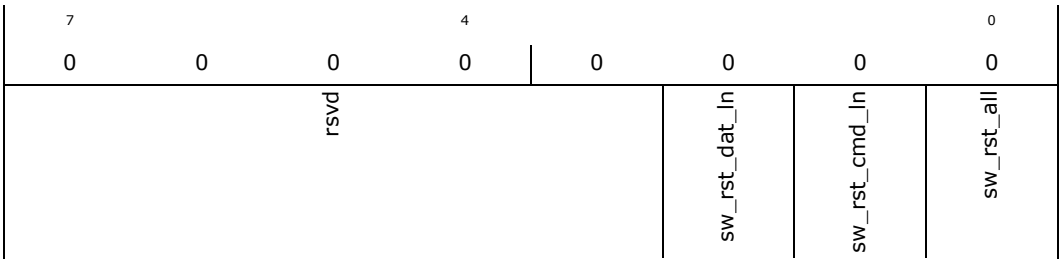
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SW_RST: [BAR] + 2Fh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RW	**SW_RST_DAT_LN (sw_rst_dat_ln):** Software Reset For DAT Line
1	0b RW	**SW_RST_CMD_LN (sw_rst_cmd_ln):** Software Reset For CMD Line
0	0b RW	**SW_RST_ALL (sw_rst_all):** Software Reset For All

3.15.20 Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h

Normal Interrupt Status Register

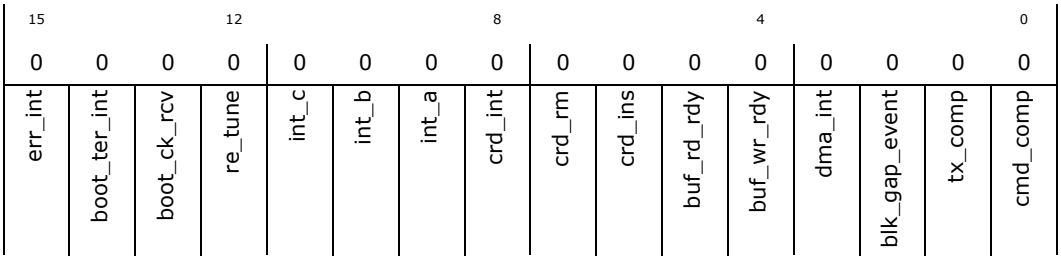
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NML_INT_STATUS: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
err_int	boot_ter_int	boot_ck_rcv	re_tune	int_c	int_b	int_a	crd_int	crd_rm	crd_ins	buf_rd_rdy	buf_wr_rdy	dma_int	blk_gap_event	tx_comp	cmd_comp

Bit Range	Default & Access	Description
15	0b RO	**ERR_INT (err_int):** Error Interrupt
14	0b RW/1C	**BOOT_TER_INT (boot_ter_int):** boot ter int
13	0b RW/1C	**BOOT_ACK_RCV (boot_ck_rcv):** boot ack rcv
12	0b RO	**RE_TUNE (re_tune):** re tuning event
11	0b RO	**INT_C (int_c):** int c
10	0b RO	**INT_B (int_b):** int b
9	0b RO	**INT_A (int_a):** int a
8	0b RO	**CRD_INT (crd_int):** Card Interrupt
7	0b RW/1C	**CRD_RM (crd_rm):** Card Removal
6	0b RW/1C	**CRD_INS (crd_ins):** Card Insertion
5	0b RW/1C	**BUF_RD_RDY (buf_rd_rdy):** Buffer Read Ready
4	0b RW/1C	**BUF_WR_RDY (buf_wr_rdy):** Buffer Write Ready
3	0b RW/1C	**DMA_INT (dma_int):** DMA Interrupt
2	0b RW/1C	**BLK_GAP_EVENT (blk_gap_event):** Block Gap Event
1	0b RW/1C	**TX_COMP (tx_comp):** Transfer Complete
0	0b RW/1C	**CMD_COMP (cmd_comp):** Command Complete

3.15.21 Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h

Error Interrupt Status Register

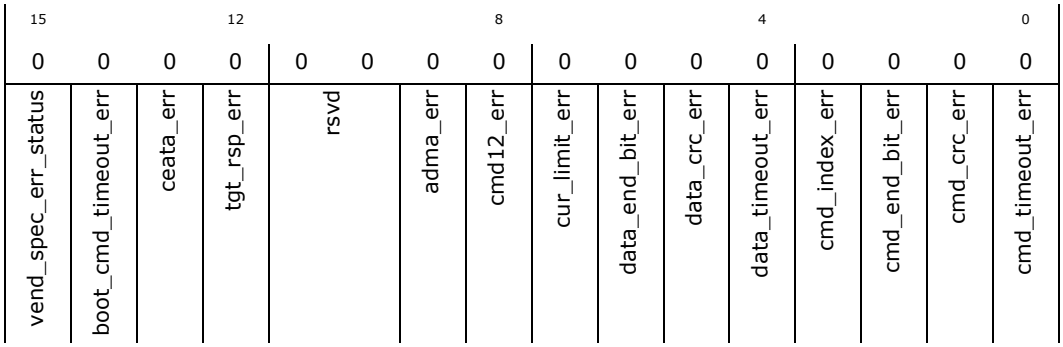
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_STATUS: [BAR] + 32h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**VEND_SPEC_ERR_STATUS (vend_spec_err_status):** Vendor Specific Error Status
14	0b RW	**BOOT_CMD_TIMEOUT_ERR (boot_cmd_timeout_err):** Occur if the boot are access command is issued to the agent which has no permission to access the boot area.
13	0b RW	**CEATA_ERR (ceata_err):** Occurs when ATA command termination has occurred due to an error condition the device has encountered.
12	0b RW	**TGT_RSP_ERR (tgt_rsp_err):** Occurs when detecting ERROR in m_hresp(dma transaction)
11:10	0h RO	**RSVD (rsvd):** Reserved
9	0b RW	**ADMA_ERR (adma_err):** ADMA Error
8	0b RW	**CMD12_ERR (cmd12_err):** Auto CMD12 Error
7	0b RW	**CUR_LIMIT_ERR (cur_limit_err):** Current Limit Error
6	0b RW	**DATA_END_BIT_ERR (data_end_bit_err):** Data End Bit Error
5	0b RW	**DATA_CRC_ERR (data_crc_err):** Data CRC Error
4	0b RW	**DATA_TIMEOUT_ERR (data_timeout_err):** Data Timeout Error
3	0b RW	**CMD_INDEX_ERR (cmd_index_err):** Command Index Error
2	0b RW	**CMD_END_BIT_ERR (cmd_end_bit_err):** Command End Bit Error

Bit Range	Default & Access	Description
1	0b RW	**CMD_CRC_ERR (cmd_crc_err):** Command CRC Error
0	0b RW	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Command Timeout Error

3.15.22 Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h

Normal Interrupt Status Enable

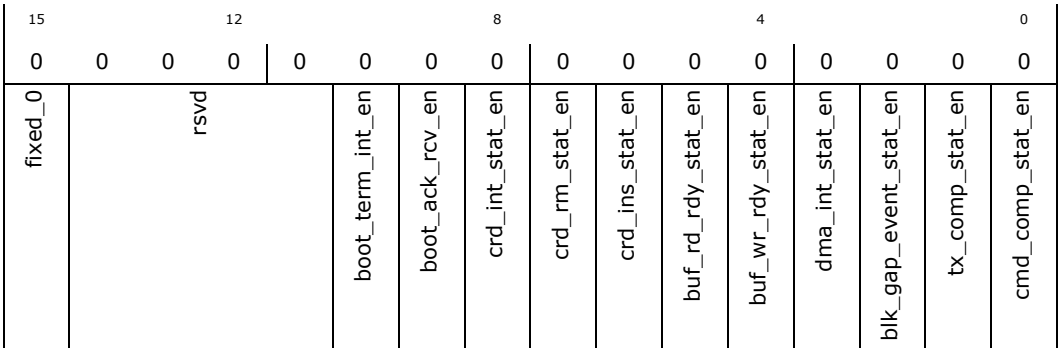
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NRM_INT_STATUS_EN: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RO	**FIXED_0 (fixed_0):** Fixed to 0
14:11	0h RO	**RSVD (rsvd):** Reserved
10	0b RW	**BOOT_TERM_INT_EN (boot_term_int_en):** 0 - Masked
9	0b RW	**BOOT_ACK_RCV_EN (boot_ack_rcv_en):** 0 -Masked
8	0b RW	**CRD_INT_STAT_EN (crd_int_stat_en):** Card Interrupt Status Enable
7	0b RW	**CRD_RM_STAT_EN (crd_rm_stat_en):** Card Removal Status Enable
6	0b RW	**CRD_INS_STAT_EN (crd_ins_stat_en):** Card Insertion Status Enable

Bit Range	Default & Access	Description
5	0b RW	**BUF_RD_RDY_STAT_EN (buf_rd_rdy_stat_en):** Buffer Read Ready Status Enable
4	0b RW	**BUF_WR_RDY_STAT_EN (buf_wr_rdy_stat_en):** Buffer Write Ready Status Enable
3	0b RW	**DMA_INT_STAT_EN (dma_int_stat_en):** DMA Interrupt Status Enable
2	0b RW	**BLK_GAP_EVENT_STAT_EN (blk_gap_event_stat_en):** Block Gap Event Status Enable
1	0b RW	**TX_COMP_STAT_EN (tx_comp_stat_en):** Transfer Complete Status Enable
0	0b RW	**CMD_COMP_STAT_EN (cmd_comp_stat_en):** Command Complete Status Enable

3.15.23 Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h

Error Interrupt Status Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_STAT_EN: [BAR] + 36h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_en	tgt_rsp_err_en	rsvd	tune_err_stat_en	adma_err_stat_en	cmd12_err_stat_en	cur_limit_err_stat_en	data_end_bit_err_stat_en	data_crc_err_stat_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Description
15:14	0b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR_EN (ceata_err_en):** 0 - masked
12	0b RW	**TGT_RSP_ERR_EN (tgt_rsp_err_en):** 0 - masked

Bit Range	Default & Access	Description
11	0b RO	**RSVD (rsvd):** Reserved
10	0b RW	**TUNE_ERR_STATE_EN (tune_err_stat_en):** 0 - masked
9	0b RW	**ADMA_ERR_STAT_EN (adma_err_stat_en):** ADMA Error Status Enable
8	0b RW	**CMD12_ERR_STAT_EN (cmd12_err_stat_en):** Auto CMD12 Error Status Enable
7	0b RW	**CUR_LIMIT_ERR_STAT_EN (cur_limit_err_stat_en):** Current Limit Error Status Enable
6	0b RW	**DATA_END_BIT_ERR_STAT_EN (data_end_bit_err_stat_en):** Data End Bit Error Status Enable
5	0b RW	**DATA_CRC_ERR_STAT_EN (data_crc_err_stat_en):** Data CRC Error Status Enable
4	0b RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Status Enable
3	0b RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Status Enable
2	0b RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Status Enable
1	0b RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Status Enable
0	0b RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Status Enable

3.15.24 Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h

Normal Interrupt Signal Enable Register

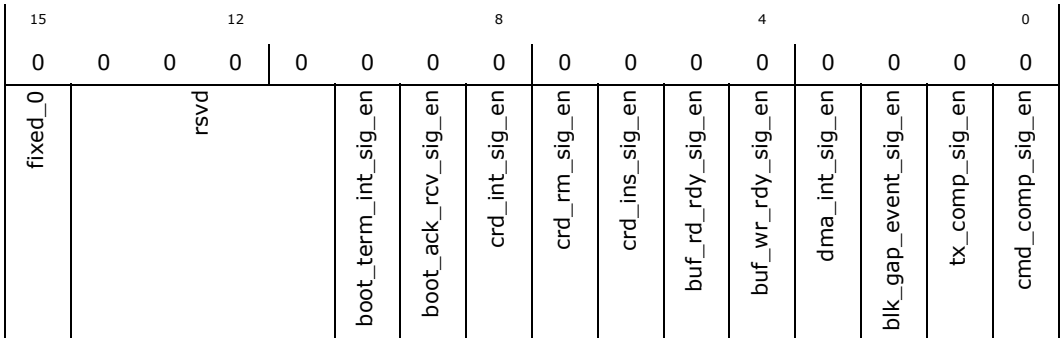
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

NRM_INT_SIG_EN: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RO	**FIXED_0 (fixed_0):** Fixed to 0
14:11	0h RO	**RSVD (rsvd):** Reserved
10	0b RW	**BOOT_TERM_INT_SIG_EN (boot_term_int_sig_en):** 0 - masked
9	0b RW	**BOOT_ACK_RCV_SIG_EN (boot_ack_rcv_sig_en):** 0 - masked
8	0b RW	**CRD_INT_SIG_EN (crd_int_sig_en):** Card Interrupt Signal Enable
7	0b RW	**CRD_RM_SIG_EN (crd_rm_sig_en):** Card Removal Signal Enable
6	0b RW	**CRD_INS_SIG_EN (crd_ins_sig_en):** Card Insertion Signal Enable
5	0b RW	**BUF_RD_RDY_SIG_EN (buf_rd_rdy_sig_en):** Buffer Read Ready Signal Enable
4	0b RW	**BUF_WR_RDY_SIG_EN (buf_wr_rdy_sig_en):** Buffer Write Ready Signal Enable
3	0b RW	**DMA_INT_SIG_EN (dma_int_sig_en):** DMA Interrupt Signal Enable
2	0b RW	**BLK_GAP_EVENT_SIG_EN (blk_gap_event_sig_en):** Block Gap Event Signal Enable
1	0b RW	**TX_COMP_SIG_EN (tx_comp_sig_en):** Transfer Complete Signal Enable
0	0b RW	**CMD_COMP_SIG_EN (cmd_comp_sig_en):** Command Complete Signal Enable

3.15.25 Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah

Error Interrupt Signal Enable Register

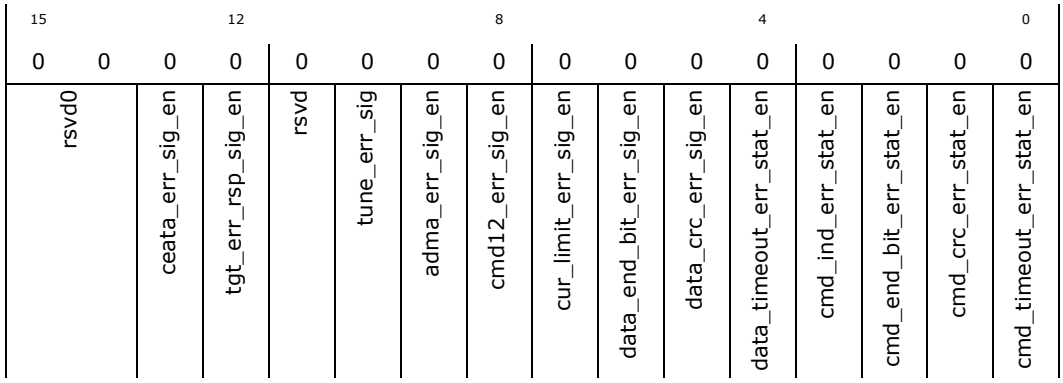
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ERR_INT_SIG_EN: [BAR] + 3Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:14	0b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR_SIG_EN (ceata_err_sig_en):** 0 - masked
12	0b RW	**TGT_ERR_RSP_SIG_EN (tgt_err_rsp_sig_en):** 0 - masked
11	0b RO	**RSVD (rsvd):** Reserved
10	0b RW	**TUNE_ERR_SIG (tune_err_sig):** 0 - masked
9	0b RW	**ADMA_ERR_SIG_EN (adma_err_sig_en):** ADMA Error Signal Enable
8	0b RW	**CMD12_ERR_SIG_EN (cmd12_err_sig_en):** Auto CMD12 Error Signal Enable
7	0b RW	**CUR_LIMIT_ERR_SIG_EN (cur_limit_err_sig_en):** Current Limit Error Signal Enable
6	0b RW	**DATA_END_BIT_ERR_SIG_EN (data_end_bit_err_sig_en):** Data End Bit Error Signal Enable
5	0b RW	**DATA_CRC_ERR_SIG_EN (data_crc_err_sig_en):** Data CRC Error Signal Enable
4	0b RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Signal Enable
3	0b RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Signal Enable
2	0b RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Signal Enable

Bit Range	Default & Access	Description
1	0b RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Signal Enable
0	0b RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Signal Enable

3.15.26 Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch

Auto CMD12 Error Status Register and Host control 2 Register

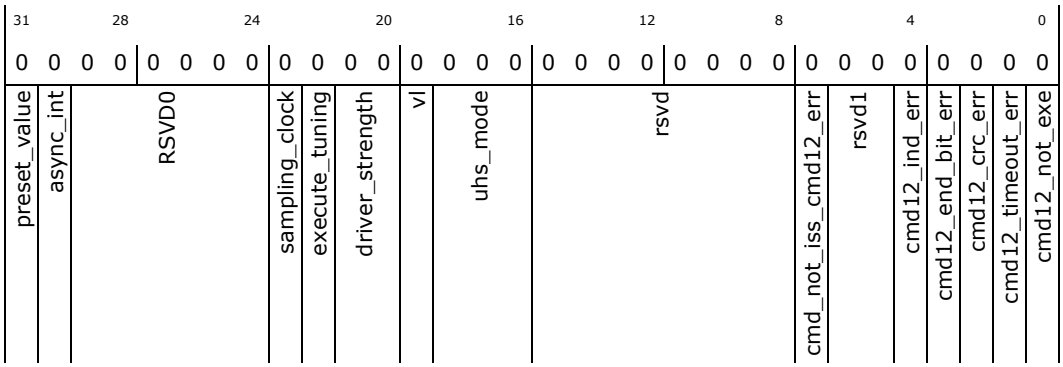
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

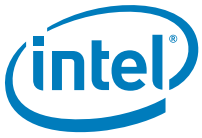
CMD12_ERR_STAT_HOST_CTRL_2: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**PRESET_VALUE (preset_value):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic This bit enables the functions defined in the Preset Value registers. 1 Automatic Selection by Preset Value are Enabled 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.



Bit Range	Default & Access	Description
30	0b RW	**ASYNC_INT (async_int):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 1 Enabled 0 Disabled
29:24	0b RO	**RSVD0:** Reserved
23	0b RW	**SAMPLING_CLOCK (sampling_clock):** This bit is set by tuning procedure when Execute Tuning is cleared
22	0b RW/AC	**EXECUTE_TUNING (execute_tuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 1 Execute Tuning 0 Not Tuned or Tuning Completed
21:20	0b RW	**DRIVER_STRENGTH (driver_strength):** Host Controller output driver in 1.8V signaling is selected by this bit
19	0b RW	**VL (vl):** This bit controls voltage regulator for I/O cell
18:16	0b RW	**UHS_MODE (uhs_mode):** This field is used to select one of UHS-I modes
15:8	0h RO	**RSVD (rsvd):** Reserved
7	0b RO	**CMD_NOT_ISS_CMD12_ERR (cmd_not_iss_cmd12_err):** Command Not Issued By Auto CMD12 Error
6:5	0h RO	**RSVD1 (rsvd1):** Reserved
4	0b RO	**CMD12_IND_ERR (cmd12_ind_err):** Auto CMD12 Index Error
3	0b RO	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Auto CMD12 End Bit Error
2	0b RO	**CMD12_CRC_ERR (cmd12_crc_err):** Auto CMD12 CRC Error
1	0b RO	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Auto CMD12 Timeout Error
0	0b RO	**CMD12_NOT_EXE (cmd12_not_exe):** Auto CMD12 Not Executed

3.15.27 Capabilities Register (CAPABILITIES)—Offset 40h

Capabilities Register

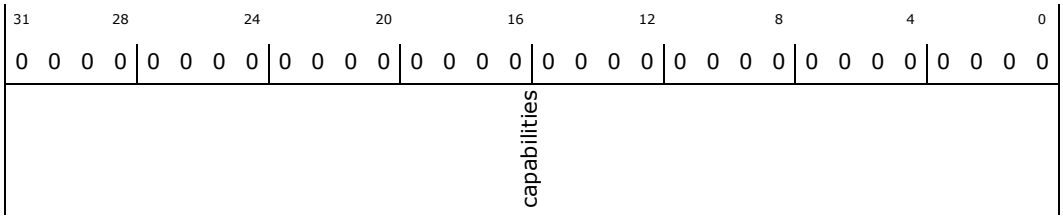
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITIES: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**capabilities:** capabilities

3.15.28 Capabilities Register 2 (CAPABILITIES_2)—Offset 44h

Capabilities Register 2

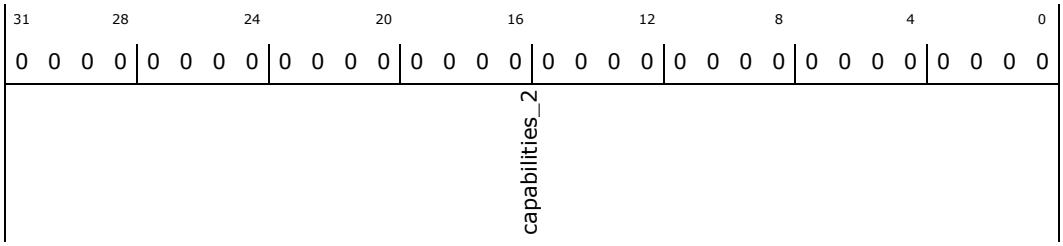
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITIES_2: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**capabilities_2:** capabilities 2

3.15.29 Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h

These registers indicate maximum current capability for each voltage

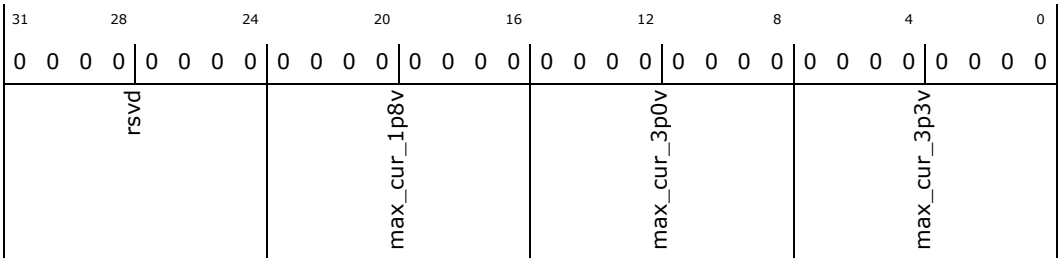
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MAX_CUR_CAP: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**RSVD (rsvd):** Reserved
23:16	00h RO	**MAX_CUR_1p8V (max_cur_1p8v):** Maximum Current for 1.8V
15:8	00h RO	**MAX_CUR_3p0V (max_cur_3p0v):** Maximum Current for 3.0V
7:0	00h RO	**MAX_CUR_3p3V (max_cur_3p3v):** Maximum Current for 3.3V

3.15.30 Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h

Force Event Register for Auto CMD12 Error Status

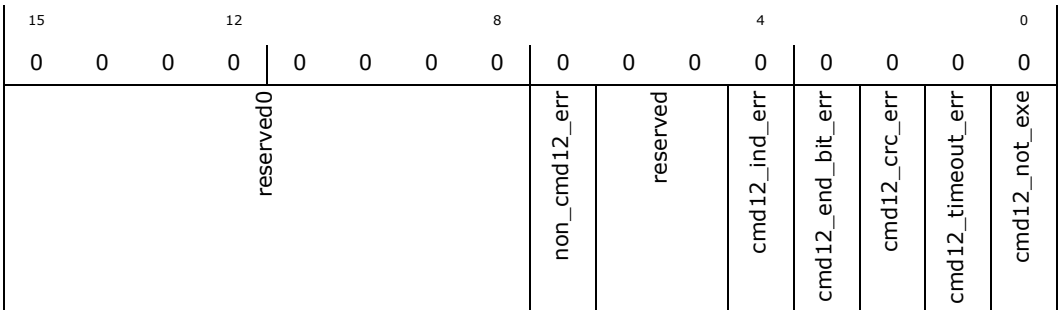
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

FORCE_EVENT_CMD12_ERR_STAT: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**Reserved0 (reserved0):** Reserved
7	0b RW	**NON_CMD12_ERR (non_cmd12_err):** Force Event for Command Not Issued By Auto CMD12 Error :
6:5	00b RO	**Reserved (reserved):** Reserved
4	0b RW	**CMD12_IND_ERR (cmd12_ind_err):** Force Event for Auto CMD12 Index Error
3	0b RW	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Force Event for Auto CMD12 End Bit Error
2	0b RW	**CMD12_CRC_ERR (cmd12_crc_err):** Force Event for Auto CMD12 CRC Error
1	0b RW	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Force Event for Auto CMD12 Timeout Error
0	0b RW	**CMD12_NOT_EXE (cmd12_not_exe):** Force Event for Auto CMD12 Not Executed

3.15.31 Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h

Force Event Register for Error Interrupt Status

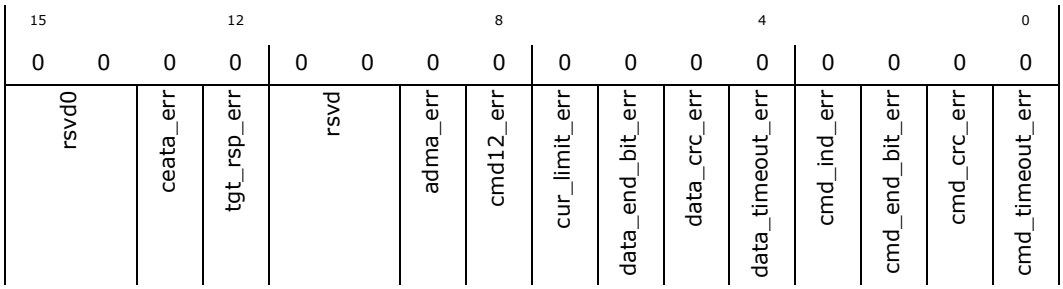
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

FORCE_EVENT_ERR_INT_STAT: [BAR] + 52h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:14	00b RO	**RSVD0 (rsvd0):** Reserved
13	0b RW	**CEATA_ERR (ceata_err):** Force Event for CEATA error

Bit Range	Default & Access	Description
12	0b RW	**TGT_RSP_ERR (tgt_rsp_err):** Force Event for Target Response Error
11:10	0h RO	**RSVD (rsvd):** Reserved
9	0b RW	**ADMA_ERR (adma_err):** Force Event for ADMA Error
8	0b RW	**CMD12_ERR (cmd12_err):** Force Event for Auto CMD12 Error
7	0b RW	**CUR_LIMIT_ERR (cur_limit_err):** Force Event for Current Limit Error
6	0b RW	**DATA_END_BIT_ERR (data_end_bit_err):** Force Event for Data End Bit Error
5	0b RW	**DATA_CRC_ERR (data_crc_err):** Event for Data CRC Error
4	0b RW	**DATA_TIMEOUT_ERR (data_timeout_err):** Event for Data Timeout Error
3	0b RW	**CMD_IND_ERR (cmd_ind_err):** Force Event for Command Index Error
2	0b RW	**CMD_END_BIT_ERR (cmd_end_bit_err):** Force Event for Command End Bit Error
1	0b RW	**CMD_CRC_ERR (cmd_crc_err):** Force Event for Command CRC Error
0	0b RW	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Force Event for Command Timeout Error

3.15.32 ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h

ADMA Error Status Register

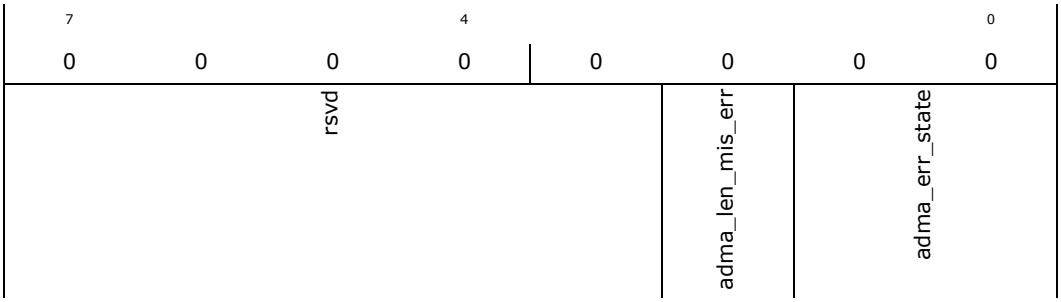
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

ADMA_ERR_STAT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	0h RO	**RSVD (rsvd):** Reserved
2	0b RO	**ADMA_LEN_MIS_ERR (adma_len_mis_err):** ADMA Length Mismatch Error
1:0	00b RO	**ADMA_ERR_STATE (adma_err_state):** ADMA Error State

3.15.33 ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h

This register contains the physical Descriptor address used for ADMA data transfer.

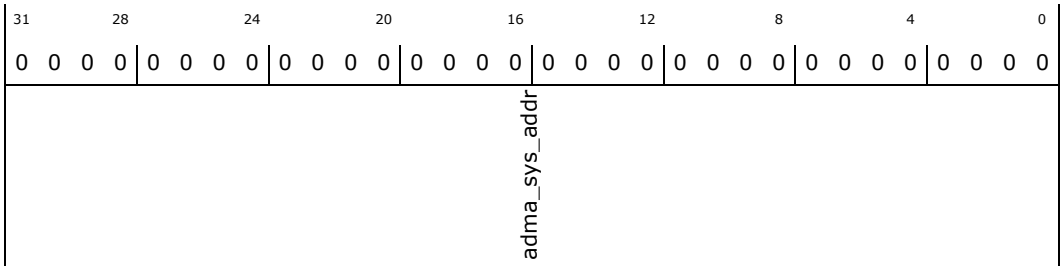
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ADMA_SYS_ADDR: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**ADMA_SYS_ADDR (adma_sys_addr):** ADMA System Address

3.15.34 Preset Values registers (PRESET_VALUE_0)—Offset 60h

Preset Values init and default speed

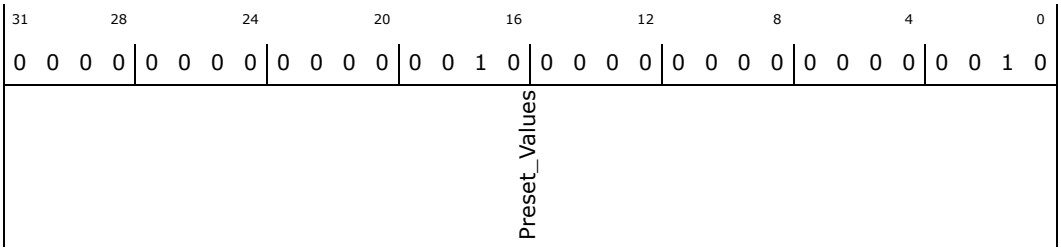
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_0: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00020002h



Bit Range	Default & Access	Description
31:0	00020002h RO	**PresetValues (Preset_Values):** Reserved.

3.15.35 Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h

Preset Values high and sdr12

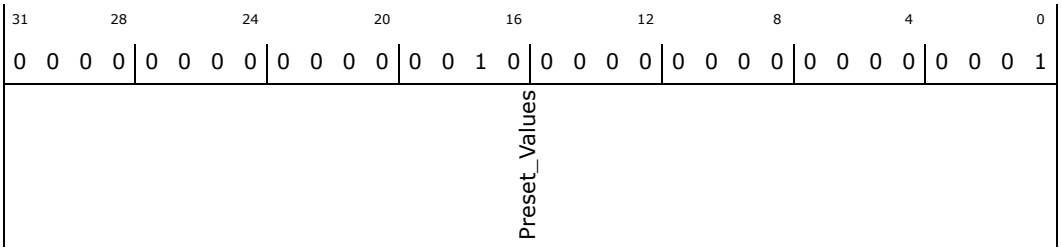
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_1: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00020001h



Bit Range	Default & Access	Description
31:0	00020001h RO	**PresetValues (Preset_Values):** Reserved.

3.15.36 Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h

Preset Values sdr25 and sdr50

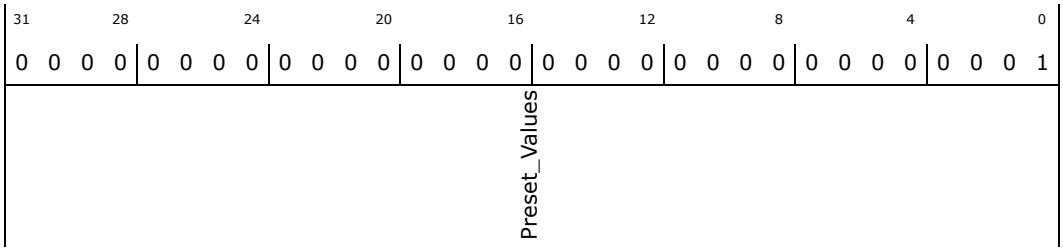
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_2: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:0	00000001h RO	**PresetValues (Preset_Values):** Reserved.

3.15.37 Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch

Preset Values sdr104 and ddr50

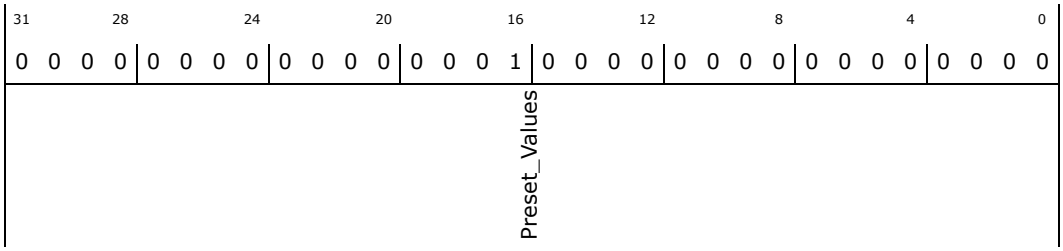
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRESET_VALUE_3: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31:0	00010000h RO	**PresetValues (Preset_Values):** Reserved.

3.15.38 BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h

BOOT_TIMEOUT_CTRL

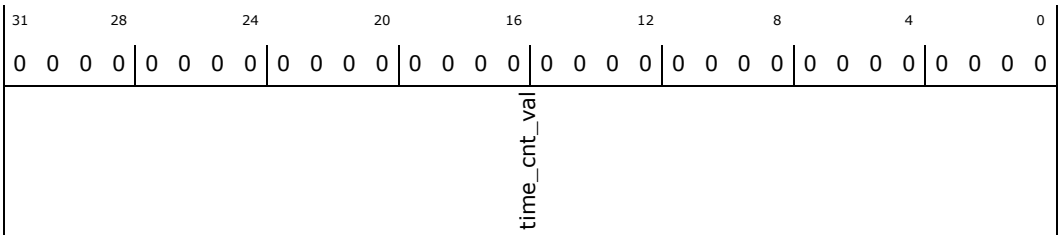
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BOOT_TIMEOUT_CTRL: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**TIME_CNT_VAL (time_cnt_val):** Boot Data Timeout Counter Value

3.15.39 DEBUG_SEL (DEBUG_SEL)—Offset 74h

Debug Selection Register

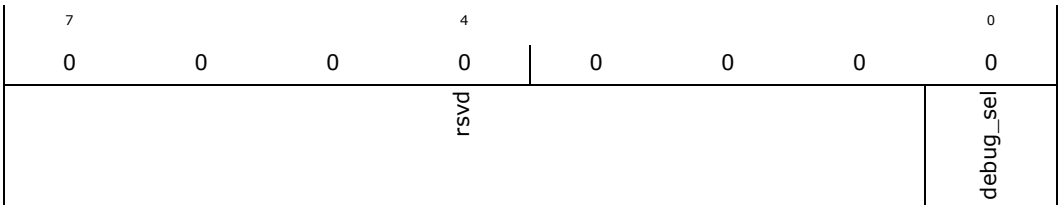
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

DEBUG_SEL: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:1	00h RO	**RSVD (rsvd):** Reserved
0	0b WO	**DEBUG_SEL (debug_sel):** 1 - cmd register, interrupt status, transmitter module, ahb_iface module and clk sdcard signals are probed out..

3.15.40 Shared Bus Control Register (SHARED_BUS)—Offset E0h

Shared Bus Control Register

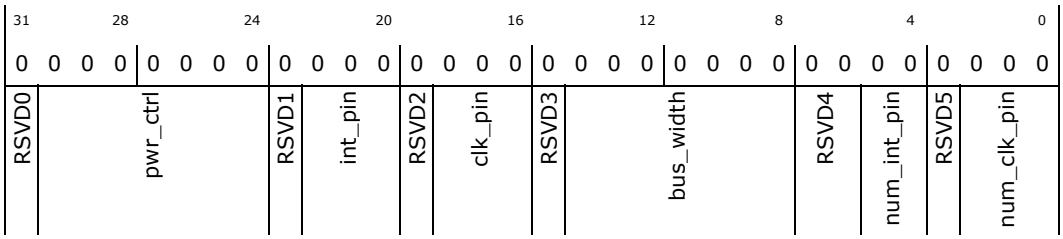
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SHARED_BUS: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**RSVD0:** Reserved
30:24	0h RW	**PWR_CTRL (pwr_ctrl):** Each bit of this field controls back-end power supply for an embedded device. Host interface voltage (VDDH) is not controlled by this field. The number of devices supported is specified by Number of Clock Pins and a maximum of 7 devices can be controlled D24 Back-end Power Control for Device 1 D25 Back-end Power Control for Device 2 D26 Back-end Power Control for Device 3 D27 Back-end Power Control for Device 4 D28 Back-end Power Control for Device 5 D29 Back-end Power Control for Device 6 D30 Back-end Power Control for Device 7 The function of each bit is defined as follows: 0 Back-end Power is Off 1 Back-end Power is Supplied Back-End power control is effective for embedded memory devices in the Sleep State that support the Sleep command (CMD14) to reduce power consumption and embedded SDIO devices when IOEx is set to 0.
23	0b RO	**RSVD1:** Reserved
22:20	0h RW	**INT_PIN (int_pin):** Interrupt pin inputs are enabled by this field. Enable of unsupported interrupt pin is meaningless. 000b Interrupt is detected by Interrupt Cycle xx1b INT_A is Enabled x1xb INT_B is Enabled 1xxb INT_C is Enabled
19	0b RO	**RSVD2:** Reserved
18:16	0h RW	**CLK_PIN (clk_pin):** One of clock pin outputs is selected by this field. Select of unsupported clock pin is meaningless. Refer to Figure 2-38 for the timing of clock outputs. 000b Clock Pins are Disabled 001b CLK[1] is Selected 010b CLK[2] is Selected .... 111b CLK[7] is Selected
15	0b RO	**RSVD3:** Reserved

Bit Range	Default & Access	Description
14:8	0h RO	**BUS_WIDTH (bus_width):** Shared bus supports mixing of 4-bit and 8-bit bus width devices. Each bit of this field specifies the bus width for each embedded device. The number of devices supported is specified by Number of Clock Pins and a maximum of 7 devices are supported.This field is effective when multiple devices are connected to a shared bus (Slot Type is set to 10b in the Capabilities register). In the other case, Extended Data Transfer Width in the Host Control 1 register is used to select 8-bit bus width. As use of 1-bit mode is not intended for shared bus, Data Transfer Width in the Host Control 1 register should be set to 1.D08 - Bus width preset for Device 1 D09 - Bus width preset for Device 2 D10 - Bus width preset for Device 3 D11 - Bus width preset for Device 4 D12 - Bus width preset for Device 5 D13 - Bus width preset for Device 6 D14 - Bus width preset for Device 7 The function of each bit is defined as follows: 0 - 4 bit bus width mode 1 - 8 bit bus width mode
7:6	0b RO	**RSVD4:** Reserved
5:4	0h RO	**NUM_INT_PIN (num_int_pin):** This field indicates support of interrupt input pins for shared bus system.Three asynchronous interrupt pins are defined, INT_A#, INT_B# and INT_C#. Which interrupt pin is used is determined by the system. Each one is driven by open drain and then wired or connection is possible. 00b Interrupt Input Pin is Not Supported 01b INTA is Supported 10b INTA and INTB are Supported 11b INTA, INTB and INTC are Supported
3	0b RO	**RSVD5:** Reserved
2:0	0h RO	**NUM_CLK_PIN (num_clk_pin):** This field indicates support of clock pins to select one of devices for shared bus system. Up to 7 clock pins can be supported.Shared bus is supported by specific system. Then Standard Host Driver does not support control of these clock pins. 000b Shared bus is not supported 001b 1 SDCLK pin is supported 010b 2 SDCLK pins are supported .... 111b 7 SDCLK pins are supported

3.15.41 SPI_INT_SUP (SPI_INT_SUP)—Offset F0h

SPI_INT_SUP

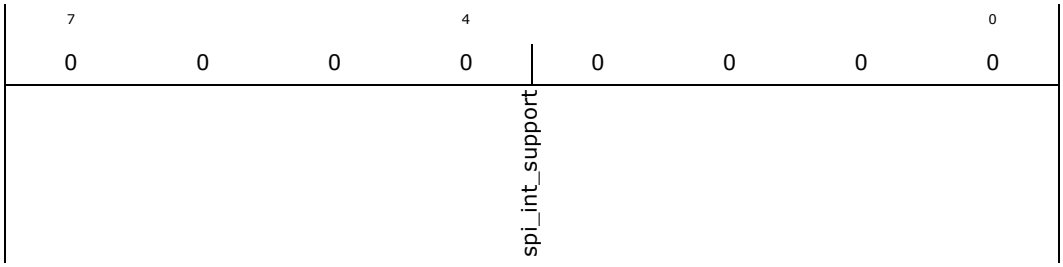
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SPI_INT_SUP: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**SPI_INT_SUPPORT (spi_int_support):** This bit is set to indicate the assertion assertion of interrupts in the SPI mode at any time, irrespective of the status of thecard select (CS) line. If this bit is zero, then SDIO card can only assert the interrupt line in the SPI mode when the CS line is asserted.

3.15.42 Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh

Slot Interrupt Status Register

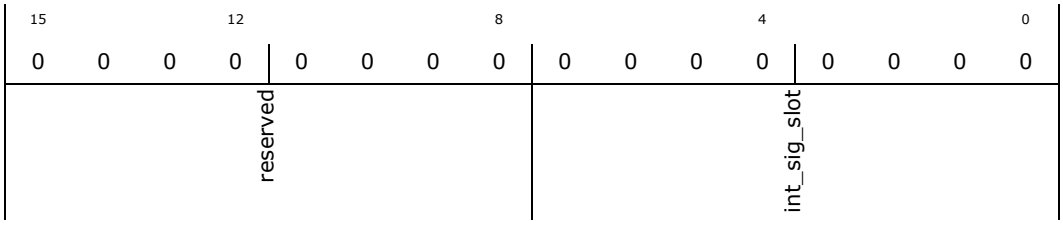
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

SLOT_INT_STAT: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**Reserved (reserved):** Reserved
7:0	00h RO	**INT_SIG_SLOT (int_sig_slot):** Interrupt Signal For Each Slot

3.15.43 Host Controller Version Register (HOST_CTRL_VER)—Offset FEh

Host Controller Version Register

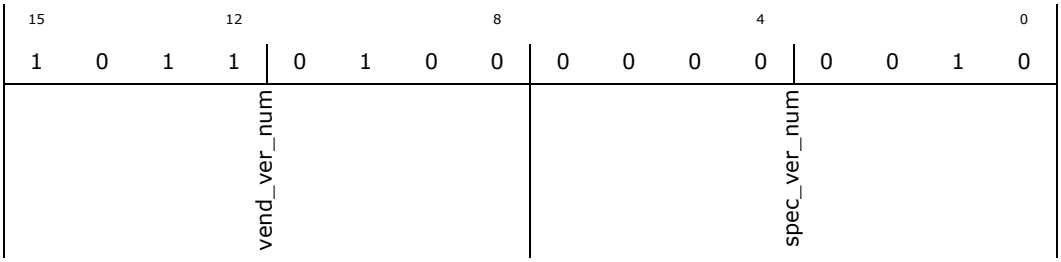
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

HOST_CTRL_VER: [BAR] + FEh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: B402h



Bit Range	Default & Access	Description
15:8	b4h RO	**VEND_VER_NUM (vend_ver_num):** Vendor Version Number
7:0	02h RO	**SPEC_VER_NUM (spec_ver_num):** Version Number

3.16 USB EHCI PCI Configuration Registers

Table 24. Summary of USB EHCI PCI Configuration Registers—0/29/0

Offset	Size	Register ID—Description	Default Value
0h	1	"Vendor ID and Device ID (VID_DID)—Offset 0h" on page 1664	00008086h
4h	1	"Command and Device Status (CMD_STS)—Offset 4h" on page 1665	02900000h
8h	4	"Revision ID and Programming Interface and Sub/Base Class Code (RID_PI_CC)—Offset 8h" on page 1667	0C032000h
Ch	4	"Reserved and Master Latency Timer and Header Type (RSVD_MLT_HT)—Offset Ch" on page 1668	00000000h
10h	4	"Memory Base Address (MBAR)—Offset 10h" on page 1668	00000000h
2Ch	4	"USB2 Subsystem Vendor ID and USB2 Subsystem ID (SSVID_SSID)—Offset 2Ch" on page 1669	00000000h
34h	4	"Capabilities Pointer and Reserved (CAP_PTR_RSVD)—Offset 34h" on page 1670	00000050h
3Ch	4	"Interrupt Line and Interrupt Pin and Reserved (ILINE_IPIN_RSVD)—Offset 3Ch" on page 1670	00000000h
50h	4	"PCI Power Management Capability ID and Next Item Pointer #1 and PM Capabilities (PM_CID_NEXT_CAP)—Offset 50h" on page 1671	C9C35801h
54h	4	"Power Management Control/Status (PM_CS)—Offset 54h" on page 1672	00000008h
58h	4	"Debug Port Capability ID and Next Item Pointer #2 and Debug Port Base Offset (DP_CID_NEXT_BASE)—Offset 58h" on page 1673	20A0980Ah
60h	4	"Serial Bus Release Number and Frame Length Adjustment and Port Wake Capability (SBRN_FLA_PWC)—Offset 60h" on page 1674	07FF2020h
64h	4	"Port Disable Override and RMH Device Removable (PDO_RMHDR)—Offset 64h" on page 1675	00000000h
68h	4	"USB2 Legacy Support Extended Capability (ULSEC)—Offset 68h" on page 1676	00000001h
6Ch	4	"USB2 Legacy Support Control/Status (ULSCS)—Offset 6Ch" on page 1677	00000000h
70h	4	"Intel-Specific USB2 SMI (ISU2SMI)—Offset 70h" on page 1679	00000000h
74h	4	"OverCurrent Mapping (OCMAP)—Offset 74h" on page 1681	C0300C03h
7Ch	4	"EHC Suspend Well Configuration and RMH Wake Control (EHCSUSCFGRMHWC)—Offset 7Ch" on page 1682	0000408Ch
F8h	4	"Manufacturer's ID (MANID)—Offset F8h" on page 1684	00000F86h

3.16.1 Vendor ID and Device ID (VID_DID)—Offset 0h

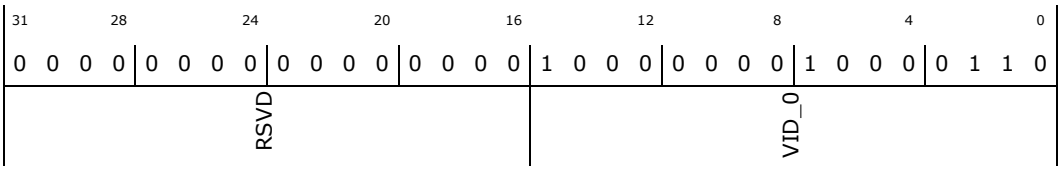
Access Method

Type: PCI Configuration Register (Size: 32 bits)

VID_DID: [B:0, D:29, F:0] + 0h

Power Well: Core

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15:0	8086h RO	**Vendor ID (VID_0):** 16-bit field which indicates company vendor as Intel.

3.16.2 Command and Device Status (CMD_STS)—Offset 4h

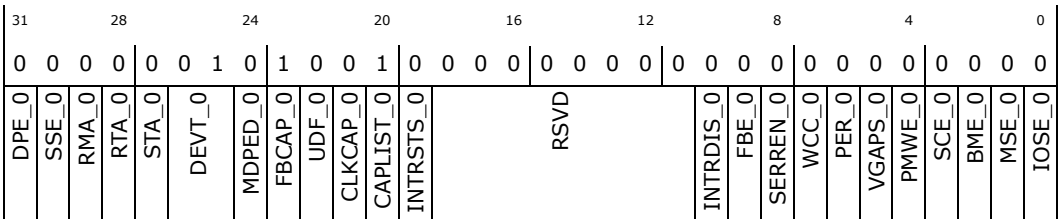
Access Method

Type: PCI Configuration Register (Size: 32 bits)

CMD_STS: [B:0, D:29, F:0] + 4h

Power Well: Core

Default: 02900000h



Bit Range	Default & Access	Description
31	0b RWC	**Detected Parity Error (DPE_0):** This bit is set whenever a parity error is seen on the internal interface to the USB2 host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a '1' to this bit location.
30	0b RWC	**Signaled System Error (SSE_0):** This bit is set whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. The following conditions can cause the generation of SERR#: a parity error is seen on address, command, or data (if the data was targeting the EHC) on the internal interface to the USB2 host controller due to a parity error on the system interface and bit 6 of the Command register is set to 1. An EHC-initiated memory read results in a completion packet with a status other than successful on the system interface (if SERR on Aborts Enable is also set) Software clears this bit by writing a '1' to this bit location.

Bit Range	Default & Access	Description
29	0b RWC	**Received Master-Abort Status (RMA_0):** This bit is set when USB2, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit and the SERR on Aborts Enable (bit 3, offset 84h). Software clears this bit by writing a '1' to this bit location.
28	0b RWC	**Received Target Abort Status (RTA_0):** This bit is set when USB2, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit and the SERR on Aborts Enable (bit 3, offset 84h). Software clears this bit by writing a '1' to this bit location.
27	0b RO	**Signaled Target-Abort Status (STA_0):** This bit is used to indicate when the USB2 function responds to a cycle with a target abort. There is no reason for this to happen, so this bit will be hard-wired to '0'. Read-Only
26:25	01b RO	**DEVSEL# Timing Status (DEVT_0):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only.
24	0b RWC	**Master Data Parity Error Detected (MDPED_0):** This bit is set whenever a data parity error is detected on a USB2 read completion packet on the internal interface to the USB2 host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a '1' to this bit location.
23	1b RO	**Fast Back-to-Back Capable (FBCAP_0):** Reserved as '1'.
22	0b RO	**User Definable Features (UDF_0):** Reserved as '0'
21	0b RO	**66 MHz Capable (CLKCAP_0):** Reserved as '0'
20	1b RO	**Capabilities List (CAPLIST_0):** Hardwired to '1' indicating that offset 34h contains a valid capabilities pointer.
19	0b RO	**Interrupt Status (INTRSTS_0):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
18:11	00000000b RO	**Reserved (RSVD):** Reserved.
10	0b RW	**Interrupt Disable (INTRDIS_0):** When cleared to '0', the function is capable of generating interrupts. When '1', the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable. This bit defaults to '0'. This bit is added as part of the PCI 2.3 Specification.
9	0b RO	**Fast Back to Back Enable (FBE_0):** Reserved as '0'.
8	0b RW	**SERR# Enable (SERREN_0):** on a memory read completion (if SERR on Aborts Enable is also set) Detection of an address or command parity error and the Parity Error Response bit is setDetection of a data parity error (when the data is going to the EHC) and the Parity Error Response bit is set
7	0b RO	**Wait Cycle Control (WCC_0):** Reserved as '0'.

Bit Range	Default & Access	Description
6	0b RW	**Parity Error Response (PER_0):** When set to 1, the USB2 Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the EHCI specification. If it detects bad parity on the address or command phases when this bit is set to 1, the host controller does not take the cycle, halts the host controller (if currently not halted) and sets the host system error bit in the USBSTS register. Note that this applies to both requests and completions from the system interface. See section 9.19.2.4 for information regarding parity errors detected by the Prefetch DMA Engine. This bit must be set in order for the parity errors to generate SERR#.
5	0b RO	**VGA Palette Snoop (VGAPS_0):** Reserved as '0'
4	0b RO	**Postable Memory Write Enable (PMWE_0):** Reserved as '0'
3	0b RO	**Special Cycle Enable (SCE_0):** Reserved as '0'
2	0b RW	**Bus Master Enable (BME_0):** When set, bus mastering from EHCI is allowed, and will generate memory reads and writes for USB transfers. Notes on the EHC implementation: - Writes to change this bit occur immediately. Specifically, a write followed by a read will return the updated value. - When the BME bit is changed from 1 to 0, the EHC will cease accessing main memory within 2 microframes (250 usec). During this time, any number of reads and/or writes to memory may occur. - Clearing the BME bit shuts down the EHC DMA engines in the same manner that clearing the Run/Stop does. However, the schedule status bits and the HCHalted bit do not change based on the BME value.
1	0b RW	**Memory Space Enable (MSE_0):** This bit controls access to the USB2 Memory Space registers. If this bit is set, accesses to the USB2 registers are enabled. The Base Address register for USB2 should be programmed before this bit is set.
0	0b RO	**I/O Space Enable (IOSE_0):** Reserved as '0'.

3.16.3 Revision ID and Programming Interface and Sub/Base Class Code (RID_PI_CC)—Offset 8h

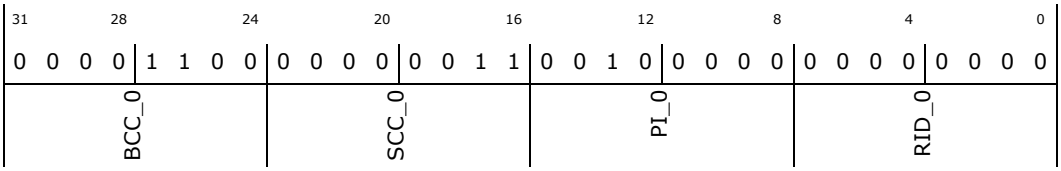
Access Method

Type: PCI Configuration Register (Size: 32 bits)

RID_PI_CC: [B:0, D:29, F:0] + 8h

Power Well: Core

Default: 0C032000h



Bit Range	Default & Access	Description
31:24	0Ch RO	**Base Class Code (BCC_0):** A value of 0Ch indicates that this is a Serial Bus controller.
23:16	03h RO	**Sub Class Code (SCC_0):** A value of 03h indicates that this is a Universal Serial Bus Host Controller.
15:8	20h RO	**Programming Interface (PI_0):** A value of 20h indicates that this USB2 Host Controller conforms to the EHCI specification.
7:0	00h RO	**Revision ID (RID_0):** The value reported in this register indicates stepping of the host controller hardware.

3.16.4 Reserved and Master Latency Timer and Header Type (RSVD_MLT_HT)—Offset Ch

Reserved, for padding Master Latency Timer Header Type Reserved

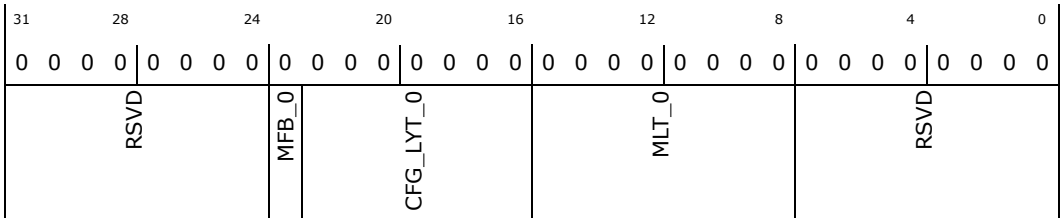
Access Method

Type: PCI Configuration Register (Size: 32 bits)

RSVD_MLT_HT: [B:0, D:29, F:0] + Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Multi Function Bit (MFB_0):** When set to 1 this indicates that this is a multifunction device. Default to 0 since EHCI is at function 0, no other function beyond.
22:16	0000000b RO	**Configuration Layout (CFG_LYT_0):** Hardwired to 0 to indicate a standard PCI configuration layout.
15:8	00h RO	**Master Latency Timer (MLT_0):** Because the USB2 controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0
7:0	00h RO	**Reserved (RSVD):** Reserved.

3.16.5 Memory Base Address (MBAR)—Offset 10h

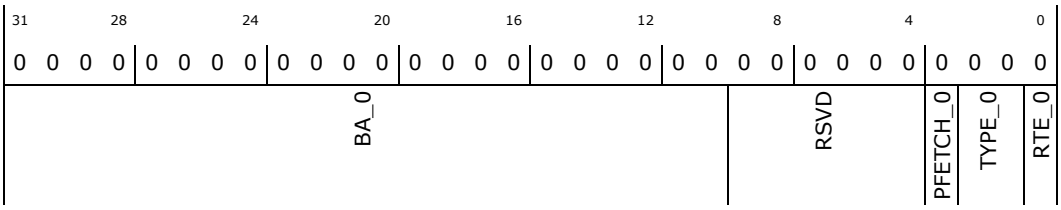
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MBAR: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:10	000000h RW	**Base Address (BA_0):** Bits (31:10) correspond to memory address signals (31:10), respectively. This gives 1 KB of relocatable memory space aligned to 1 KB boundaries.
9:4	000000b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Prefetchable (PFETCH_0):** Read Only. This bit is hardwired to 0 indicating that this range should not be prefetched.
2:1	00b RO	**Type (TYPE_0):** indicating that this range can be mapped anywhere within 32-bit address space.
0	0b RO	**Resource Type Indicator (RTE_0):** Read Only. This bit is hardwired to 0 indicating that the base address field in this register maps to memory space

3.16.6 USB2 Subsystem Vendor ID and USB2 Subsystem ID (SSVID_SSID)—Offset 2Ch

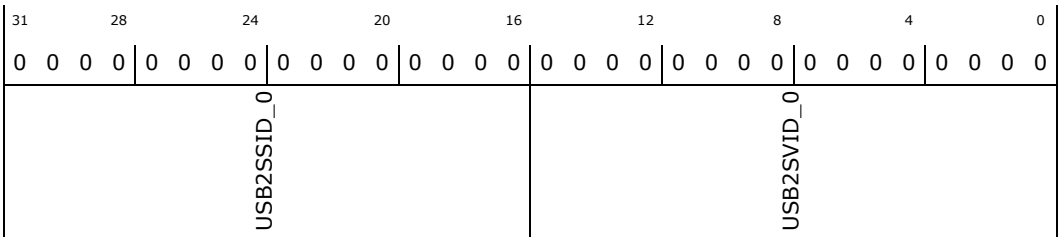
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SSVID_SSID: [B:0, D:29, F:0] + 2Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/L	**USB2 Subsystem ID (USB2SSID_0):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). Writes to this register are enabled when the WRT_RDONLY bit (offset 80h, bit 0) is set to 1. Writes should be done as a single 16-bit cycle. Reset: none
15:0	0000h RW/L	**USB2 Subsystem Vendor ID (USB2SVID_0):** This register, in combination with the USB2 Subsystem ID register, enables the operating system to distinguish each subsystem from the others. Writes to this register are enabled when the WRT_RDONLY bit (offset 80h, bit 0) is set to 1. Reset: none

3.16.7 Capabilities Pointer and Reserved (CAP_PTR_RSVD)—Offset 34h

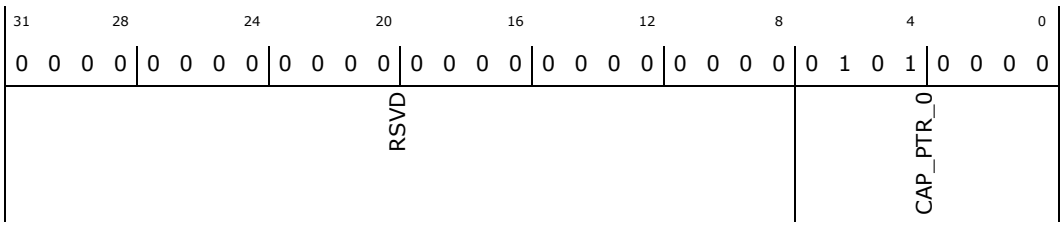
Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAP_PTR_RSVD: [B:0, D:29, F:0] + 34h

Power Well: Core

Default: 00000050h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved (RSVD):** Reserved.
7:0	50h RO	**Capabilities Pointer (CAP_PTR_0):** This register points to the starting offset of the USB2 capabilities ranges.

3.16.8 Interrupt Line and Interrupt Pin and Reserved (ILINE_IPIN_RSVD)—Offset 3Ch

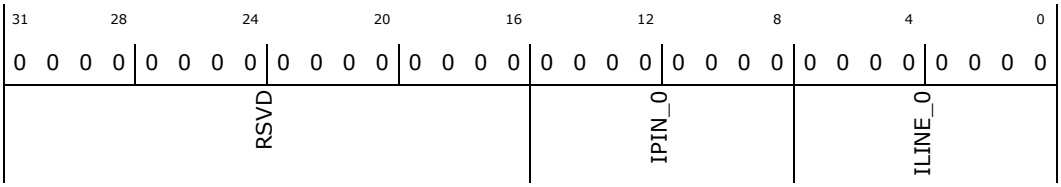
Access Method

Type: PCI Configuration Register (Size: 32 bits)

ILINE_IPIN_RSVD: [B:0, D:29, F:0] + 3Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15:8	00h RO	**Interrupt Pin (IPIN_0):** Bits 3:0 reflect the value programmed in the interrupt pin registers in chipset configuration space. Bits 7:4 are hardwired to 0000b. NOTE: As a single function device, only INTA# may be used while the other three interrupt lines have no meaning. (refer to PCI 3.0 spec section 2.2.6 Interrupt Pins)
7:0	00h RW	**Interrupt line (ILINE_0):** This data is not used by the SOC. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to. Reset: core well and D3-to-D0.

3.16.9 PCI Power Management Capability ID and Next Item Pointer #1 and PM Capabilities (PM_CID_NEXT_CAP)—Offset 50h

PCI Power Management Capabilities ID Next Item Pointer #1 Power Management Capabilities

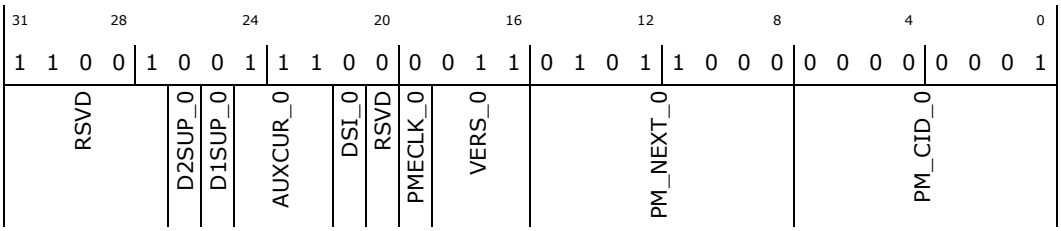
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PM_CID_NEXT_CAP: [B:0, D:29, F:0] + 50h

Power Well: Core

Default: C9C35801h



Bit Range	Default & Access	Description
31:27	11001b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**D2_Support (D2SUP_0):** The D2 state is not supported. Reset: core well, but not D3-to-D0.

Bit Range	Default & Access	Description
25	0b RO	**D1_Support (D1SUP_0):** The D1 state is not supported. Reset: core well, but not D3-to-D0.
24:22	111b RW/L	**Aux_Current (AUXCUR_0):** The USB2 SIP EHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known.
21	0b RO	**DSI (DSI_0):** The Intel EHC reports 0, indicating that no device-specific initialization is required. Reset: core well, but not D3-to-D0.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**PME Clock (PMECLK_0):** The Intel EHC reports 0, indicating that no PCI clock is required to generate PME#. Reset: core well, but not D3-to-D0.
18:16	011b RW/L	**Version (VERS_0):** Version: The Intel EHC reports 011, indicating that it complies with Revision 1.21 of the PCI Power Management Specification. Note: As contingency plan, the bit can be reverted by BIOS to 010b to support PCI PM Revision 1.1, by manipulating the offset80h Access Control register's WRT_RDONLY bit.
15:8	58h RW/L	**Next Item Pointer #1 (PM_NEXT_0):** This register defaults to 58h, which indicates that the next capability registers begin at configuration offset 58h. This register is writable when the WRT_RDONLY bit is set. This allows BIOS to effectively hide the Debug Port capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of 58h implies Debug Port and FLR capabilities visible 98h implies Debug Port invisible, next capability is FLR 00h implies that both Debug port and FLR capability are hidden Note that this value is never expected to be programmed. Reset: core well, but not D3-to-D0
7:0	01h RO	**PCI Power Management Capability ID (PM_CID_0):** A value of 01h indicates that this is a PCI Power Management capabilities field.

3.16.10 Power Management Control/Status (PM_CS)—Offset 54h

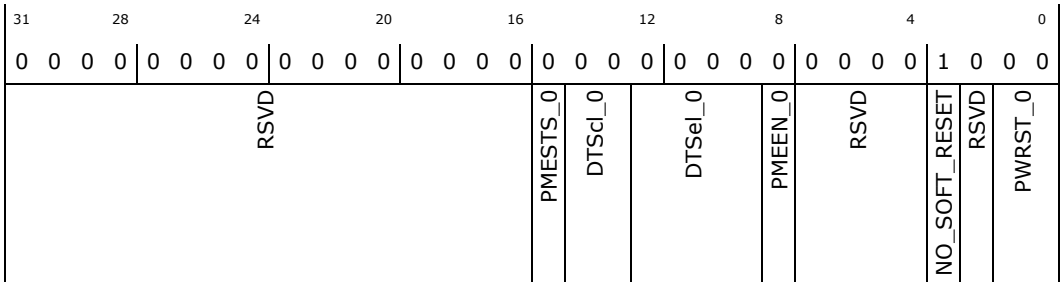
Access Method

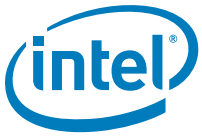
Type: PCI Configuration Register (Size: 32 bits)

PM_CS: [B:0, D:29, F:0] + 54h

Power Well: Core

Default: 00000008h





Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15	0b RWC	**PME_Status (PMESTS_0):** This bit is set when the EHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	00b RO	**Data_Scale (DTScl_0):** because it does not support the associated Data register.
12:9	0h RO	**Data_Select (DTSel_0):** because it does not support the associated Data register.
8	0b RW	**PME_En (PMEEN_0):** A '1' enables the EHC to generate an internal PME signal when PME_Status is '1'. This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:4	0000b RO	**Reserved (RSVD):** Reserved.
3	1b RO	**No Soft Reset (NO_SOFT_RESET):** A '0' indicates device does perform an internal reset upon D3hot to D0 transition via software control of the PowerState bits. Configuration Context is lost. Full re-initialization sequence is needed to return the device to D0 Initialized.(Default to '1') Note: As contingency plan, the bit can be reverted by BIOS to 0, by manipulating the offset80h Access Control registers WRT_RDONLY bit.
2	0b RO	**Reserved (RSVD):** Reserved.
1:0	00b RW	**PowerState (PWRST_0):** This 2-bit field is used both to determine the current power state of EHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3hot state, the accesses to the EHC memory range must not be accepted; but the configuration space must still be accessible. When not in the D0 state, the generation of the interrupt output is blocked. Specifically, the PIRQ[H] is not asserted when not in the D0 state. When software changes this value from the D3hot state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

3.16.11 Debug Port Capability ID and Next Item Pointer #2 and Debug Port Base Offset (DP_CID_NEXT_BASE)—Offset 58h

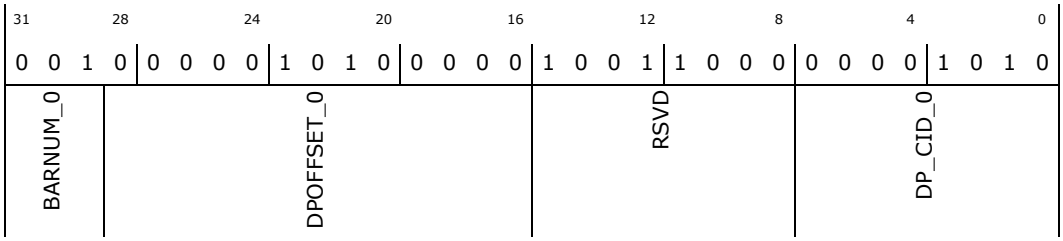
Access Method

Type: PCI Configuration Register (Size: 32 bits)

DP_CID_NEXT_BASE: [B:0, D:29, F:0] + 58h

Power Well: Core

Default: 20A0980Ah



Bit Range	Default & Access	Description
31:29	001b RO	**BAR Number (BARNUM_0):** Read-Only. This field is hardwired to 001b to indicate the memory BAR at offset 10h in the EHCI configuration space. Reset: Not applicable.
28:16	00A0h RO	**Debug Port Offset (DPOFFSET_0):** This field is hardwired to 0A0h to indicate that the debug port registers begin at offset A0h in the EHCI memory range. Reset: Not applicable.
15:8	98h RO	**Reserved (RSVD):** Reserved.
7:0	0Ah RO	**Debug Port Capability ID (DP_CID_0):** This register is hardwired to 0Ah which indicates that this is the start of a Debug Port Capability structure. Reset: Not applicable.

3.16.12 Serial Bus Release Number and Frame Length Adjustment and Port Wake Capability (SBRN_FLA_PWC)—Offset 60h

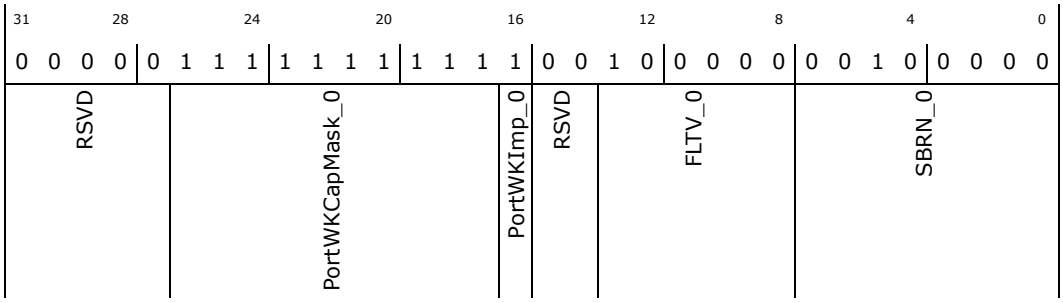
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SBRN_FLA_PWC: [B:0, D:29, F:0] + 60h

Power Well: Resume

Default: 07FF2020h



Bit Range	Default & Access	Description
31:27	00000b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
26:17	3FFh RW	**Port Wake Up Capability Mask (PortWKCapMask_0):** Bit positions 1 through 8 correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 1, position 2 port 2, etc. Are only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
16	1b RW	**Port Wake Implemented (PortWKImp_0):** A '1' in bit 0 indicates that this register is implemented to software. Are only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
15:14	00b RO	**Reserved (RSVD):** Reserved.
13:8	100000b RW	**Frame Length Timing Value (FLTV_0):** Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Are only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
7:0	20h RO	**Serial Bus Release Number (SBRN_0):** value of 20h indicates that this controller follows USB release 2.0

3.16.13 Port Disable Override and RMH Device Removable (PDO_RMHDR)—Offset 64h

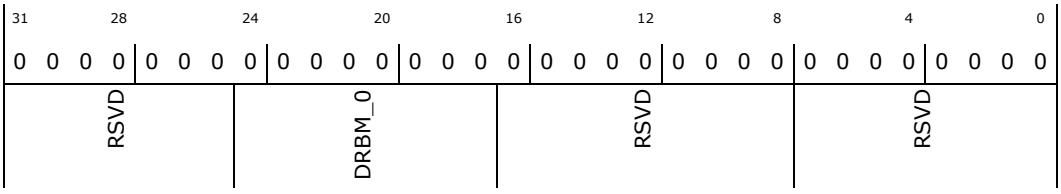
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PDO_RMHDR: [B:0, D:29, F:0] + 64h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0000000b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
24:17	00h RW	**Device Removable Bit Map (DRBM_0):** A 1 in a given bit position in this field indicates that the corresponding downstream port of the RMH is connected to a non-removable device. A 0 indicates that the port is exposed to the user. Bits 8:1 are mapped to Ports 8:1. This bits control the value returned by the RMH in the Deviceremovable field of the Hub Descriptor. A 1 in a given bit position in this register will result in the corresponding bit in the DeviceRemovable field of the hub descriptor being set to 1 as well (indicating that the port is connected to a non-removable device). System BIOS is expected to set these values upon Boot and resume from Sx states.
16:8	000000000b RO	**Reserved (RSVD):** Reserved.
7:0	00h RO	**Reserved (RSVD):** Reserved.

3.16.14 USB2 Legacy Support Extended Capability (ULSEC)—Offset 68h

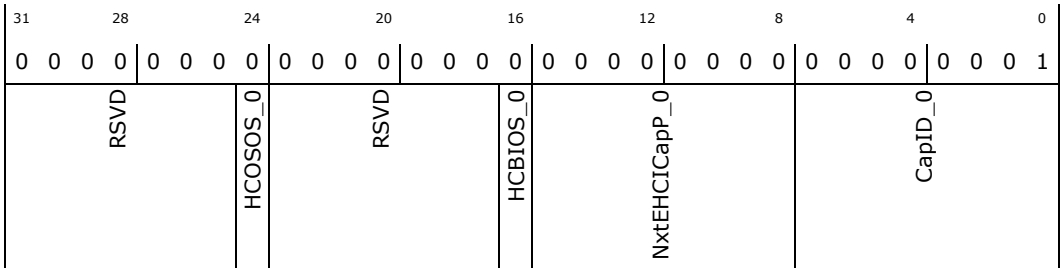
Access Method

Type: PCI Configuration Register (Size: 32 bits)

ULSEC: [B:0, D:29, F:0] + 68h

Power Well: Resume

Default: 00000001h



Bit Range	Default & Access	Description
31:25	0000000b RO	**Reserved (RSVD):** Reserved.
24	0b RW	**HC OS Owned Semaphore (HCOSOS_0):** System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as clear. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
23:17	0000000b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
16	0b RW	**HC BIOS Owned Semaphore (HCBIOS_0):** The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will clear this bit in response to a request for ownership of the EHCI controller by system software. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
15:8	00h RO	**Next EHCI Capability Pointer (NxtEHCICapP_0):** A value of 00h indicates that there are no EHCI Extended Capability structures in this device. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
7:0	01h RO	**Capability ID (CapID_0):** A value of 01h indicates that this EHCI Extended Capability is the Legacy Support Capability. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.

3.16.15 USB2 Legacy Support Control/Status (ULSCS)—Offset 6Ch

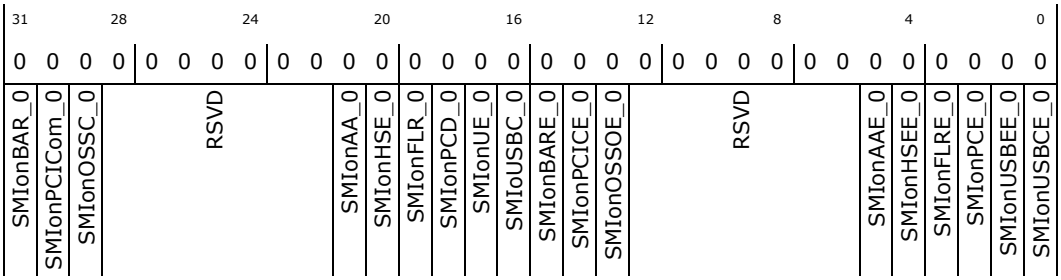
Access Method

Type: PCI Configuration Register (Size: 32 bits)

ULSCS: [B:0, D:29, F:0] + 6Ch

Power Well: Resume

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RWC	**SMI on BAR (SMIonBAR_0):** This bit is set to '1' whenever the Base Address Register (BAR) is written. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
30	0b RWC	**SMI on PCI Command (SMIonPCICom_0):** This bit is set to '1' whenever the PCI Command Register is written. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.

Bit Range	Default & Access	Description
29	0b RWC	**SMI on OS Ownership Change (SMIonOSSC_0):** This bit is set to '1' whenever the HC OS Owned Semaphore bit in the USB2 Legacy Support Extended Capability register transitions from 1 to a 0 or 0 to a 1. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
28:22	00h RO	**Reserved (RSVD):** Reserved.
21	0b RO	**SMI on Async Advance (SMIonAA_0):** Shadow bit of the Interrupt on Async Advance bit in the USB2STS register. To clear this bit system software must write a one to the Interrupt on Async Advance bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
20	0b RO	**SMI on Host System Error (SMIonHSE_0):** Shadow bit of Host System Error bit in the USB2STS. To clear this bit system software must write a one to the Host System Error bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
19	0b RO	**SMI on Frame List Rollover (SMIonFLR_0):** Shadow bit of Frame List Rollover bit in the USB2STS register. To clear this bit system software must write a one to the Frame List Rollover bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
18	0b RO	**SMI on Port Change Detect (SMIonPCD_0):** Shadow bit of Port Change Detect bit in the USB2STS register. To clear this bit system software must write a one to the Port Change Detect bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
17	0b RO	**SMI on USB Error (SMIonUE_0):** Shadow bit of USB Error Interrupt (USBERRINT) bit in the USB2STS register. To clear this bit system software must write a one to the USB Error Interrupt bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
16	0b RO	**SMI on USB Complete (SMIoUSBC_0):** Shadow bit of USB Interrupt (USBINT) bit in the USB2STS register. To clear this bit system software must write a one to the USB Interrupt bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
15	0b RW	**SMI on BAR Enable (SMIonBARE_0):** When this bit is '1' and SMIonBAR_0 is '1', then the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
14	0b RW	**SMI on PCI Command Enable (SMIonPCICE_0):** When this bit is '1' and SMI on PCI Command is '1', then the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
13	0b RW	**SMI on OS Ownership Enable (SMIonOSSOE_0):** When this bit is a one AND the OS Ownership Change bit is one, the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.

Bit Range	Default & Access	Description
12:6	00h RO	**Reserved (RSVD):** Reserved.
5	0b RW	**SMI on Async Advance Enable (SMIonAAE_0):** When this bit is a one, and the SMI on Async Advance bit is a one, the host controller will issue an SMI immediately. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
4	0b RW	**SMI on Host System Error Enable (SMIonHSEE_0):** When this bit is a one, and the SMI on Host System Error is a one, the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
3	0b RW	**SMI on Frame List Rollover Enable (SMIonFLRE_0):** When this bit is a one, and the SMI on Frame List Rollover bit is a one, the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
2	0b RW	**SMI on Port Change Enable (SMIonPCE_0):** When this bit is a one, and the SMI on Port Change Detect bit is a one, the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
1	0b RW	**SMI on USB Error Enable (SMIonUSBEE_0):** When this bit is a one, and the SMI on USB Error bit is a one, the host controller will issue an SMI immediately. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.
0	0b RW	**SMI on USB Complete Enable (SMIonUSBCE_0):** When this bit is a one, and the SMI on USB Complete bit is a one, the host controller will issue an SMI immediately. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition.

3.16.16 Intel-Specific USB2 SMI (ISU2SMI)—Offset 70h

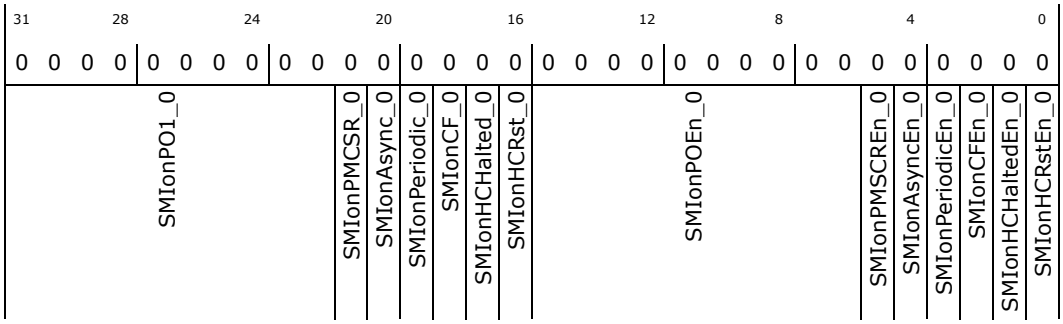
Access Method

Type: PCI Configuration Register (Size: 32 bits)

ISU2SMI: [B:0, D:29, F:0] + 70h

Power Well: Resume

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RWC	**SMI on PortOwner (SMIonPO1_0):** Bits 29:22 correspond to the Port Owner bits for ports 1 (22) through 8 (29). These bits are set to '1' whenever the associated Port Owner bits transition from 0-)1 or 1-)0. Software clears these bits by writing a one. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
21	0b RWC	**SMI on PMCSR (SMIonPMCSR_0):** This bit is set to '1' whenever software modifies the Power State bits in the Power Management Control/Status register. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
20	0b RWC	**SMI on Async (SMIonAsync_0):** This bit is set to '1' whenever the Async Schedule Enable bit transitions from 1-)0 or 0-)1. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
19	0b RWC	**SMI on Periodic (SMIonPeriodic_0):** This bit is set to '1' whenever the Periodic Schedule Enable bit transitions from 1-)0 or 0-)1. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
18	0b RWC	**SMI on CF (SMIonCF_0):** This bit is set to '1' whenever the Configure Flag transitions from 1-)0 or 0-)1. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
17	0b RWC	**SMI on HCHalted (SMIonHCHalted_0):** This bit is set to '1' whenever HCHalted transitions to '1' as a result of the Run/Stop bit being cleared. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
16	0b RWC	**SMI on HCReset (SMIonHCRst_0):** This bit is set to '1' whenever HCRESET transitions to '1'. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition

Bit Range	Default & Access	Description
15:6	000h RW	**SMI on PortOwner Enable (SMIonPOEn_0):** When any of these bits are '1' and the corresponding SMI on PortOwner bits are '1', then the host controller will issue an SMI. Unused ports should have their corresponding bits cleared. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
5	0b RW	**SMI on PMSCR Enable (SMIonPMSCREn_0):** When this bit is '1' and SMI on PMSCR is '1', then the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
4	0b RW	**SMI on Async Enable (SMIonAsyncEn_0):** When this bit is '1 and SMI on Async is '1' , then the host controller will issue an SMI. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
3	0b RW	**SMI on Periodic Enable (SMIonPeriodicEn_0):** When this bit is '1 and SMI on Periodic is '1', then the host controller will issue an SMI. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
2	0b RW	**SMI on CF Enable (SMIonCFEn_0):** When this bit is '1' and SMI on CF is '1', then the host controller will issue an SMI. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
1	0b RW	**SMI on HCHalted Enable (SMIonHCHaltedEn_0):** When this bit is a '1' and SMI on HCHalted is '1', then the host controller will issue an SMI. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition
0	0b RW	**SMI on HCReset Enable (SMIonHCRstEn_0):** When this bit is a '1' and SMI on HCHalted is '1', then the host controller will issue an SMI. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition

3.16.17 OverCurrent Mapping (OCMAP)—Offset 74h

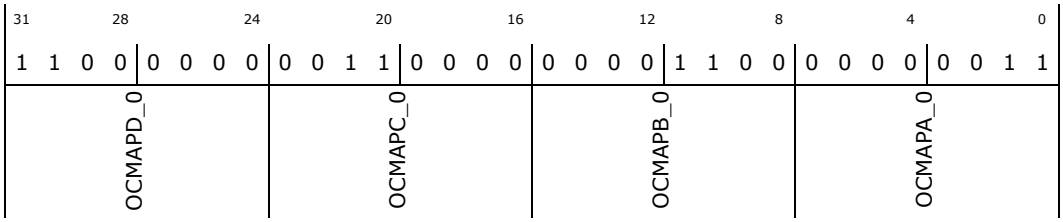
Access Method

Type: PCI Configuration Register (Size: 32 bits)

OCMAP: [B:0, D:29, F:0] + 74h

Power Well: Resume

Default: C0300C03h



Bit Range	Default & Access	Description
31:24	C0h RW	**OC Mapping D (OCMAPD_0):** Each bit position maps OC4, for EHCI1 to a set of ports as follows: The OC4 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin.
23:16	30h RW	**OC Mapping C (OCMAPC_0):** OC Mapping C. Each bit position maps OC3, for EHCI1 to a set of ports as follows: The OC3 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin.
15:8	0Ch RW	**OC Mapping B (OCMAPB_0):** OC Mapping B. Each bit position maps OC2, for EHCI1 to a set of ports as follows: The OC2 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin.
7:0	03h RW	**OC Mapping A (OCMAPA_0):** OC Mapping A: Each bit position maps OC1, for EHCI1 to a set of ports as follows: The OC1 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin.

3.16.18 EHC Suspend Well Configuration and RMH Wake Control (EHCSUSCFGRMHWC)—Offset 7Ch

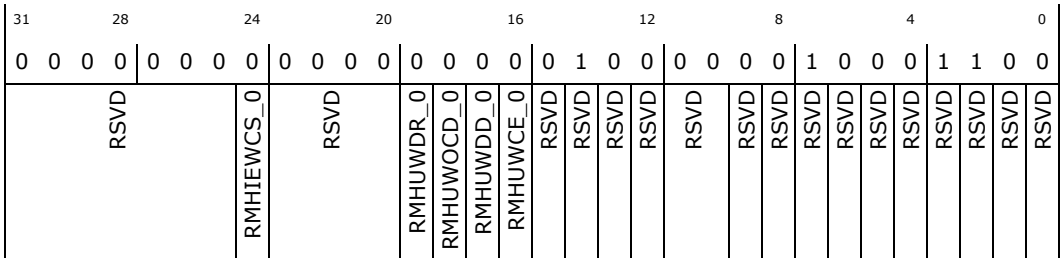
Access Method

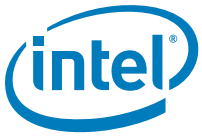
Type: PCI Configuration Register (Size: 32 bits)

EHCSUSCFGRMHWC: [B:0, D:29, F:0] + 7Ch

Power Well: Resume

Default: 0000408Ch





Bit Range	Default & Access	Description
31:25	0000000b RO	**Reserved (RSVD):** Reserved.
24	0b RW	**RMH Inherit EHCI Wake Control Settings (RMHIEWCS_0):** When this bit is set, the RMH behaves as if bits 2:0 of this register reflect the appropriate bits of EHCI PORTSC0 bits 22:20.
23:20	0000b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**RMH Upstream Wake on Device Resume (RMHUWDR_0):** This bit governs the hub behavior when globally suspended. When this bit is 0 it enables the port to be sensitive to device initiated resume events as system wake-up events. i.e, the hub will initiate a resume on its upstream port and cause a wake when a device resume occurs on an enabled DS port When this bit is set to 1 and a device resume event is seen on a downstream port, the hub does not initiate a wake upstream and does not cause a wake.
18	0b RW	**RMH Upstream Wake on OC Disable (RMHUWOCD_0):** This bit governs the hub behavior when globally suspended. When this bit is 0 it enables the port to be sensitive to overcurrent conditions as system wake-up events. i.e,, the hub will initiate a resume on its upstream port and cause a wake when an OC condition occurs on an enabled DS port When this bit is set to 1 and an over current event is seen, the hub does not initiate a wake upstream and does not cause a wake.
17	0b RW	**RMH Upstream Wake on Disconnect Disable (RMHUWDD_0):** This bit governs the hub behavior when globally suspended. When this bit is set to 0, the globally suspended hub treats disconnect events on downstream port as resume events to be propagated upstream. In this case, it is allowed to initiate a wake on its upstream por and cause a system wake in response to a disconnect event on a downstream port When this bit is set to 1, and the hub is globally suspended, the hub does not initiate a resume on its upstream port or cause a resume when a disconnect event occurs on a downstream port.
16	0b RW	**RMH Upstream Wake on Connect Enable (RMHUWCE_0):** This bit governs the hub behavior when globally suspended. When this bit is set to 0, and the hub is globally suspended, the hub treats connect events on a downstream port as resume events to be propagated upstream. As well as waking up the system. When this bit is set to 1,and the hub is globally suspended, the hub does not wake the system nor does it initiate a resume on its upstream port when a connect event occurs on a downstream port.
15	0b RO	**Reserved (RSVD):** Reserved.
14	1b RO	**Reserved (RSVD):** Reserved.
13	0b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11:10	00b RO	**Reserved (RSVD):** Reserved.
9	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
8	0b RO	**Reserved (RSVD):** Reserved.
7	1b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	1b RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

3.16.19 Manufacturer's ID (MANID)—Offset F8h

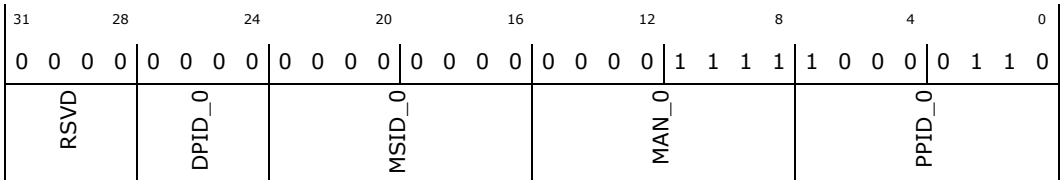
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:29, F:0] + F8h

Power Well: Core

Default: 00000F86h



Bit Range	Default & Access	Description
31:28	0h RO	**Reserved (RSVD):** Reserved.
27:24	0h RO	**Dot portion of Process ID (DPID_0):** Dot portion of Process ID: Indicates the dot Note: Process is reflected in bits [7:0] This is SIP customer implementation specific and SIP customer need to tie off the field accordingly.

Bit Range	Default & Access	Description
23:16	00h RO	**Manufacturing Stepping Identifier (MSID_0):** Stepping ID: This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. This is SIP customer implementation specific and SIP customer need to tie off the field accordingly. Implementation Note: A single Stepping ID can be implemented that is readable from all functions in the chip because all of them are incremented in lock-step.
15:8	0Fh RO	**Manufacturer (MAN_0):** 0Fh = Intel
7:0	86h RO	**Process portion of process ID (PPID_0):** Process portion of process ID: Indicates the process. Note: Dot is reflected in bits [27:24] This is SIP customer implementation specific and SIP customer need to tie off the field accordingly. Implementation Note: It is recommended that the Manufacturing ID is implemented in one place and readable from all functions. This minimizes the changes required for a process shrink.

3.17 USB EHCI Memory Mapped IO Registers

Table 25. Summary of USB EHCI Memory Mapped I/O Registers—MBAR

Offset	Size	Register ID—Description	Default Value
0h	1	"Capability Registers Length and HC Interface Version Number (CAP_HCIV)—Offset 0h" on page 1686	01000020h
4h	1	"Host Controller Structural Parameters (HCSPARAMS)—Offset 4h" on page 1687	00200008h
8h	4	"Host Controller Capability Parameters (HCCPARAMS)—Offset 8h" on page 1689	00036881h
20h	4	"USB2 Command Register (USB2CMD)—Offset 20h" on page 1690	00080000h
24h	4	"USB2 Status (USB2STS)—Offset 24h" on page 1692	00001000h
28h	4	"USB2 Interrupt Enable (USB2INTR)—Offset 28h" on page 1694	00000000h
2Ch	4	"Frame Index (FRINDEX)—Offset 2Ch" on page 1695	00000000h
30h	4	"Control Data Structure Segment Register (CTRLDSSEGMENT)—Offset 30h" on page 1696	00000000h
34h	4	"Periodic Frame List Base Address (PERIODICLISTBASE)—Offset 34h" on page 1696	00000000h
38h	4	"Current Asynchronous List Address (ASYNCLISTADDR)—Offset 38h" on page 1697	00000000h
60h	4	"Configure Flag Register (CONFIGFLAG)—Offset 60h" on page 1698	00000000h
64h	4	"Port Status and Control (PORTSC1)—Offset 64h" on page 1698	00003000h
68h	4	"Port Status and Control (PORTSC2)—Offset 68h" on page 1702	00003000h
6Ch	4	"Port Status and Control (PORTSC3)—Offset 6Ch" on page 1706	00003000h
70h	4	"Port Status and Control (PORTSC4)—Offset 70h" on page 1710	00003000h
74h	4	"Port Status and Control (PORTSC5)—Offset 74h" on page 1714	00003000h
78h	4	"Port Status and Control (PORTSC6)—Offset 78h" on page 1718	00003000h
7Ch	4	"Port Status and Control (PORTSC7)—Offset 7Ch" on page 1722	00003000h
80h	4	"Port Status and Control (PORTSC8)—Offset 80h" on page 1726	00003000h
A0h	1	"Debug Port Control/Status Register (DP_CTRLSTS)—Offset A0h" on page 1730	00000000h
A4h	1	"USB PIDs Register (DP_USB_PIDs)—Offset A4h" on page 1731	00000000h
A8h	8	"Debug Port Data Buffer Bytes 7:0 (DP_DATA_BUF_B)—Offset A8h" on page 1732	0000000000000000h
B0h	4	"Debug Port Config Register (DP_CFG)—Offset B0h" on page 1733	00007F01h

3.17.1 Capability Registers Length and HC Interface Version Number (CAP_HCIV)—Offset 0h

Access Method

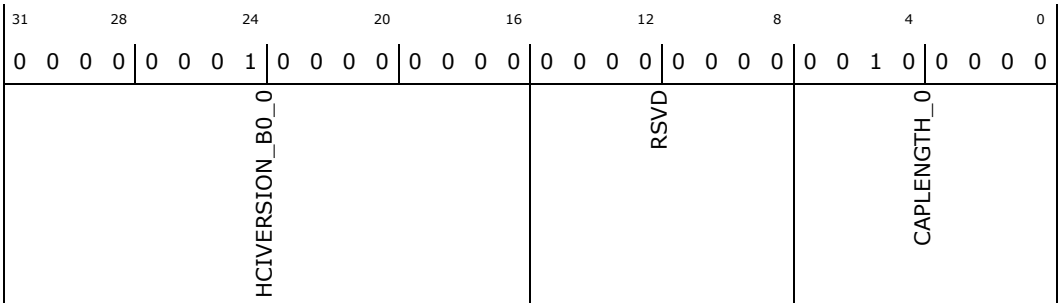
Type: Memory Mapped I/O Register (Size: 32 bits)

CAP_HCIV: [MBAR] + 0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 01000020h



Bit Range	Default & Access	Description
31:16	0100h RO	**Host Controller Interface Version Number (HCIVERSION_B0_0):** This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms.
15:8	00h RO	**Reserved (RSVD):** Reserved.
7:0	20h RO	**Capability Registers Length (CAPLENGTH_0):** This register is used as an offset to add to the Memory Base Register to find the beginning of the Operational Register Space. This is fixed at 20h, indicating that the Operation Registers begin at offset 20h.

3.17.2 Host Controller Structural Parameters (HCSPARAMS)—Offset 4h

Access Method

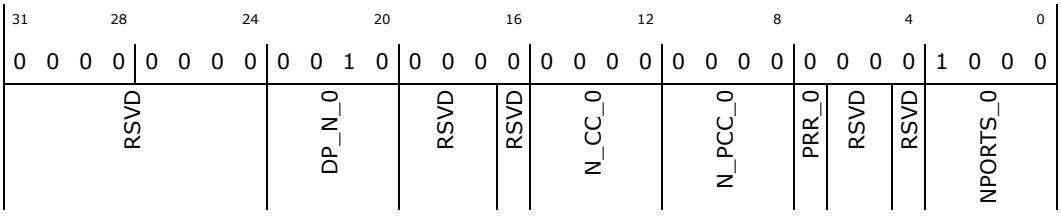
Type: Memory Mapped I/O Register (Size: 32 bits)

HCSPARAMS: [MBAR] + 4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00200008h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved (RSVD):** Reserved.
23:20	2h RO	**Debug Port Number (DP_N_0):** Hardwired to 2h, indicating that the Debug Port is on the 2nd port on the EHC. This register is only reset by the resume power well going low. It is not reset by a D3-to-D0 state transition or HCRESET (Host Controller Reset)
19:17	000b RO	**Reserved (RSVD):** Reserved.
16	0b RO	**Reserved (RSVD):** Reserved.
15:12	0h RO	**Number of Companion Controllers (N_CC_0):** This field indicates the number of companion controllers associated with this USB 2.0 host controller. A zero in this field indicates there are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports. A value larger than one in this field indicates there are companion USB 1.1 host controller(s). Port-ownership hand-offs are supported. High, Full- and Low-speed devices are supported on the host controller root ports. There are no companion controllers. This field is set to '0' as Read-Only bit.
11:8	0h RO	**Number of Ports per Companion Controller (N_PCC_0):** This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software. Read-Only. This register is only reset by the resume power well going low. It is not reset by a D3-to-D0 state transition or HCRESET (Host Controller Reset)
7	0b RO	**Port Routing Rules (PRR_0):** This field indicates the method used by this implementation for how all ports are mapped to companion controllers. This is hardwired to 0, indicating that the first N_PCC (=2) ports are routed to the lowest numbered function companion host controller, the next N_PCC ports are routed to the next lowest function companion controller, and so on
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3:0	8h RW	**N_PORTS (NPORTS_0):** This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 1H to FH. The default value for the EHCI controller indicates 8 ports. BIOS may overwrite the default value to properly describe the board or chip SKU . (please refer to RMH Configuration Details in section 1.23.2). A zero in this field is undefined. Integrated RMH - If USBr is disabled, this should be updated by BIOS to 2 such that the EHC reports 2ports to be default, port 0 assigned to the RMH and port 1 assigned to the debug device. If USB-R is enabled, the number reported should be updated to 3 by BIOS (port 2 will be assigned to USB-R in this case) Legacy Mode - The default value for the EHCI controller indicates 8 ports. If USB-R support is enabled, BIOS should account for the additional ports in calculating the value to write to this field.

3.17.3 Host Controller Capability Parameters (HCCPARAMS)—Offset 8h

Access Method

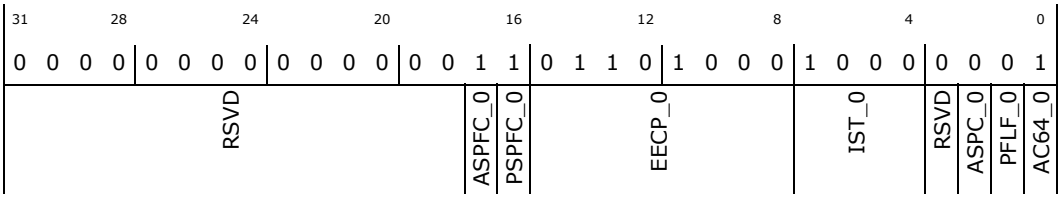
Type: Memory Mapped I/O Register (Size: 32 bits)

HCCPARAMS: [MBAR] + 8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Resume

Default: 00036881h



Bit Range	Default & Access	Description
31:18	00000000000000b RO	**Reserved (RSVD):** Reserved.
17	1b RW	**Asynchronous Schedule Prefetch Capability (ASPFC_0):** This bit indicates that the hardware support the Asynch schedule prefetch enable bit in the USB command register.
16	1b RW	**Periodic Schedule Prefetch Capability (PSPFC_0):** This bit indicates that the EHC hardware supports the Periodic Schedule prefetch bit in the USB2 Command Register.
15:8	68h RO	**EHCI Extended Capabilities Pointer (EECP_0):** This field is hardwired to 68h, indicating that the EHCI capabilities list exists and begins at offset 68h in the PCI configuration space.
7:4	8h RO	**Isochronous Scheduling Threshold (IST_0):** This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit [7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame. Refer to the EHCI specification for details on how software uses this information for scheduling isochronous transfers. The Intel USB2 hardwires this field to 8h.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Asynchronous Schedule Park Capability (ASPC_0):** This bit is hardwired to 0 indicating that the Host Controller does not support this optional feature.

Bit Range	Default & Access	Description
1	0b RO	**Programmable Frame List Flag (PFLF_0):** If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and must be set to zero. If set to a one, then system software can specify and use a smaller frame list and configure the host controller via the USBCMD register Frame List Size field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous. The Intel EHC does not support different frame list lengths. This bit is read-only '0'.
0	1b RO	**64-bit Addressing Capability (AC64_0):** This field documents the addressing range capability of this implementation. The value of this field determines whether software should use the 32-bit or 64-bit data structures. Values for this field have the following interpretation:0b data structures using 32-bit address memory pointers; 1b data structures using 64-bit address memory pointers The USB2 SIP supports 64-bit addressing only. This bit is read-only '1'.

3.17.4 USB2 Command Register (USB2CMD)—Offset 20h

Access Method

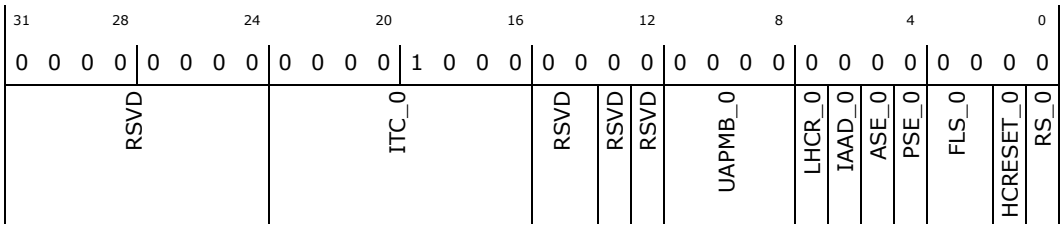
Type: Memory Mapped I/O Register (Size: 32 bits)

USB2CMD: [MBAR] + 20h

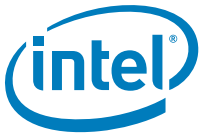
MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00080000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved (RSVD):** Reserved.
23:16	08h RW	**Interrupt Threshold Control (ITC_0):** This field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. Value Maximum Interrupt Interval 00h Reserved 01h 1 micro-frame 02h 2 micro-frames 04h 4 micro-frames 08h 8 micro-frames (default, equates to 1 ms) 10h 16 micro-frames (2 ms) 20h 32 micro-frames (4 ms) 40h 64 micro-frames (8 ms) Refer to Section 4 in the EHCI specification for interrupts affected by this field.



Bit Range	Default & Access	Description
15:14	00b RO	**Reserved (RSVD):** Reserved.
13	0b RO	**Reserved (RSVD):** Reserved.
12	0h RO	**Reserved (RSVD):** Reserved.
11:8	0h RO	**Unimplemented Asynchronous Park Mode Bits (UAPMB_0):** This field is hardwired to 000b because the host controller does not support this optional feature.
7	0b RO	**Light Host Controller Reset (LHCR_0):** Read Only 0b. The Intel EHC does not implement this optional reset and hardwires this bit to 0.
6	0b RW	**Interrupt on Async Advance Doorbell (IAAD_0):** This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state , it sets the Interrupt on Async Advance status bit in the USBSTS register. If the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold. See the EHCI specification for operational details. The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one. Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.
5	0b RW	**Asynchronous Schedule Enable (ASE_0):** This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean: 0b Do not process the Asynchronous Schedule 1b Use the ASYNCLISTADDR register to access the Asynchronous Schedule.
4	0b RW	**Periodic Schedule Enable (PSE_0):** This bit controls whether the host controller skips processing the Periodic Schedule. Values mean: 0b Do not process the Periodic Schedule 1b Use the PERIODICLISTBASE register to access the Periodic Schedule.
3:2	00b RO	**Frame List Size (FLS_0):** This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. . This field specifies the size of the frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean:00b 1024 elements (4096 bytes) Default value; 01b 512 elements (2048 bytes); 10b 256 elements (1024 bytes) - for resource-constrained environments

Bit Range	Default & Access	Description
1	0b RW	**Host Controller Reset (HCRESET_0):** This control bit used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. Note: PCI Configuration registers and Host Controller Capability Registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership will be disowned by the host controller(s), with the side effects described in the EHCI spec. Software must re initialize the host controller in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HCHalted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior. This reset must be used to leave EHCI port test modes.
0	0b RW	**Run/Stop (RS_0):** 1=Run. 0=Stop. When set to a 1, the Host Controller proceeds with execution of the schedule. The Host Controller continues execution as long as this bit is set to a 1. When this bit is set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 microframes after software clears the Run bit. The HC Halted bit in the status register indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software should not write a 1 to this field unless the host controller is in the Halted state (i.e. HCHalted in the USBSTS register is a one). The following table explains how the different combinations of Run and Halted must be interpreted: Run/Stop Halted Interpretation 0 0 Valid- in the process of halting 0 1 Valid- halted 1 0 Valid- running 1 1 Invalid- the HCHalted bit clears immediately Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being cleared (and also affect the Host Error bit).

3.17.5 USB2 Status (USB2STS)—Offset 24h

Access Method

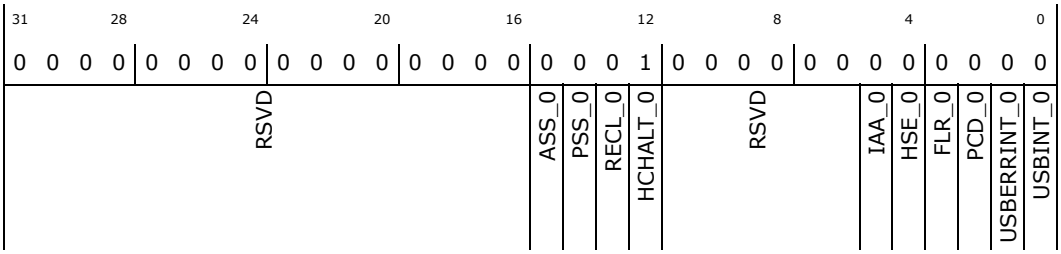
Type: Memory Mapped I/O Register (Size: 32 bits)

USB2STS: [MBAR] + 24h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00001000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15	0b RO	**Asynchronous Schedule Status (ASS_0):** This bit reports the current real status of the Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	0b RO	**Periodic Schedule Status (PSS_0):** This bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0). The Prefetch-Based Pause feature prevents this bit from transitioning to 0 if it currently has a request pending, in addition to the regular Periodic DMA engine.
13	0b RO	**Reclamation (RECL_0):** This is a read-only status bit, which is used to detect an empty asynchronous schedule. The operational model and valid transitions for this bit are described in Section 4 of the EHCI Specification.
12	1b RO	**HCHalted (HCHALT_0):** This bit is a zero whenever the Run/Stop bit is a one. The Host Controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller hardware (e.g. internal error). The Prefetch-Based Pause feature prevents this bit from transitioning to 0 if it is currently has a request pending, in addition to the regular DMA engines.
11:6	000000b RO	**Reserved (RSVD):** Reserved.
5	0b RWC	**Interrupt on Async Advance (IAA_0):** System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.

Bit Range	Default & Access	Description
4	0b RWC	**Host System Error (HSE_0):** The Host Controller sets this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being set. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system (if enabled in the Interrupt Enable Register).
3	0b RWC	**Frame List Rollover (FLR_0):** The Host Controller sets this bit to a one when the Frame List Index (see Section 9.3.2.4) rolls over from its maximum value to zero. Since the USB2 SIP only supports the 1024-entry Frame List Size, the Frame List Index rolls over every time FRNUM[13] toggles.
2	0b RWC	**Port Change Detect (PCD_0):** The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Change being set to a one after system software has relinquished ownership of a connected port by writing a zero to a port's Port Owner bit. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, over-current change, enable/disable change and connect status change). Regardless of the implementation, whenever this bit is readable (i.e., in the D0 state), it must provide a valid view of the Port Status registers.
1	0b RWC	**USB Error Interrupt (USBERRINT_0):** The Host Controller sets this bit to 1 when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and Bit 0 are set. See the EHCI specification for a list of the USB errors that will result in this interrupt being asserted.
0	0b RWC	**USB Interrupt (USBINT_0):** The Host Controller sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).

3.17.6 USB2 Interrupt Enable (USB2INTR)—Offset 28h

Access Method

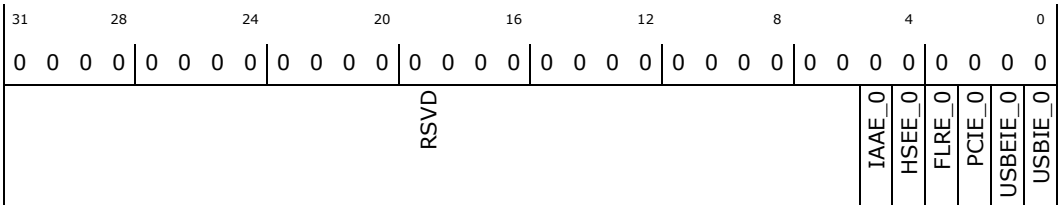
Type: Memory Mapped I/O Register (Size: 32 bits)

USB2INTR: [MBAR] + 28h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0000000h RO	**Reserved (RSVD):** Reserved.
5	0b RW	**Interrupt on Async Advance Enable (IAAE_0):** When this bit is a one, and the Interrupt on Async Advance bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	0b RW	**Host System Error Enable (HSEE_0):** When this bit is a one, and the Host System Error Status bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	0b RW	**Frame List Rollover Enable (FLRE_0):** When this bit is a one, and the Frame List Rollover bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	0b RW	**Port Change Interrupt Enable (PCIE_0):** When this bit is a one, and the Port Change Detect bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.
1	0b RW	**USB Error Interrupt Enable (USBEIE_0):** When this bit is a one, and the USBERRINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBERRINT bit.
0	0b RW	**USB Interrupt Enable (USBIE_0):** When this bit is a one, and the USBINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBINT bit.

3.17.7 Frame Index (FRINDEX)—Offset 2Ch

Access Method

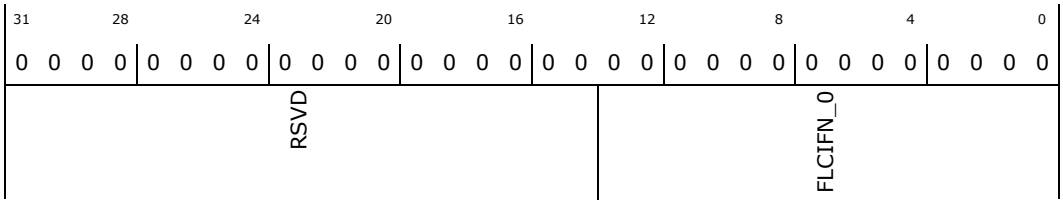
Type: Memory Mapped I/O Register (Size: 32 bits)

FRINDEX: [MBAR] + 2Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:14	00000000000000000b RO	**Reserved (RSVD):** Reserved.
13:0	00000000000000b RW	**Frame List Current Index/Frame Number (FLCIFN_0):** The value in this register increments at the end of each time frame (e.g. micro-frame). Bits (12:3) are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index

3.17.8 Control Data Structure Segment Register (CTRLDSSEGMENT)—Offset 30h

Access Method

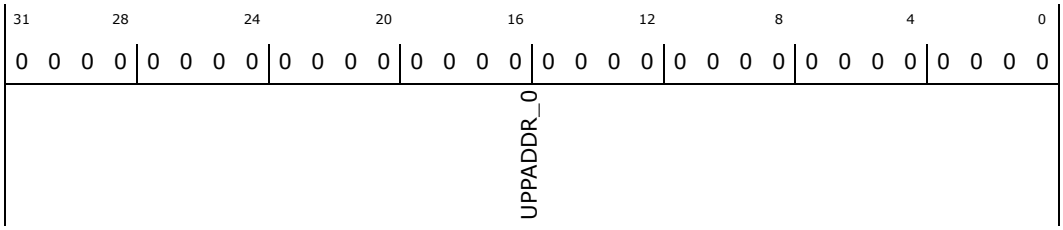
Type: Memory Mapped I/O Register (Size: 32 bits)

CTRLDSSEGMENT: [MBAR] + 30h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Upper Address[63 (UPPADDR_0):** 32]: This 32-bit field corresponds to address bits 63:32 when forming a control data structure address.

3.17.9 Periodic Frame List Base Address (PERIODICLISTBASE)—Offset 34h

Access Method

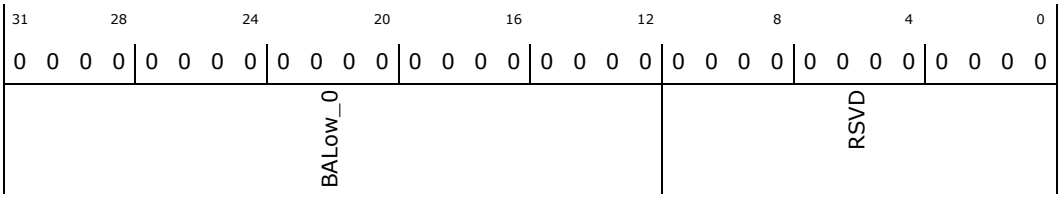
Type: Memory Mapped I/O Register (Size: 32 bits)

PERIODICLISTBASE: [MBAR] + 34h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BALow_0):** These bits correspond to memory address signals (31:12), respectively.
11:0	000000000000b RO	**Reserved (RSVD):** Reserved.

3.17.10 Current Asynchronous List Address (ASYNCLISTADDR)—Offset 38h

Access Method

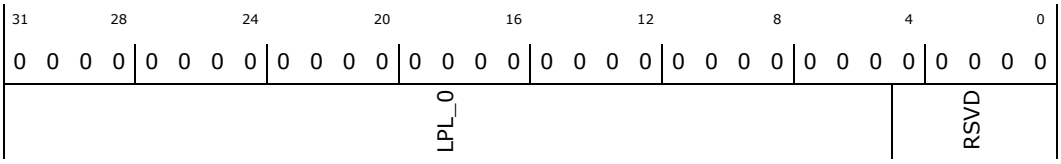
Type: Memory Mapped I/O Register (Size: 32 bits)

ASYNCLISTADDR: [MBAR] + 38h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0000000h RW	**Link Pointer Low (LPL_0):** These bits correspond to memory address signals (31:5), respectively. This field may only reference a Queue Head (QH).
4:0	0000b RO	**Reserved (RSVD):** Reserved.

3.17.11 Configure Flag Register (CONFIGFLAG)—Offset 60h

Access Method

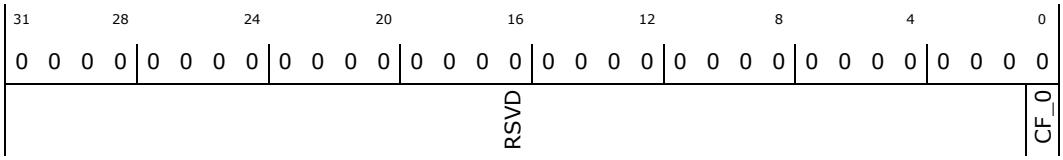
Type: Memory Mapped I/O Register (Size: 32 bits)

CONFIGFLAG: [MBAR] + 60h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Resume

Default: 00000000h



Bit Range	Default & Access	Description
31:1	00000000h RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Configure Flag (CF_0):** Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below. See section 4 of the EHCI spec for operation details. 0b Port routing control logic default-routes each port to the classic host controllers. 1b Port routing control logic default-routes all ports to this host controller. This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset.

3.17.12 Port Status and Control (PORTSC1)—Offset 64h

Access Method

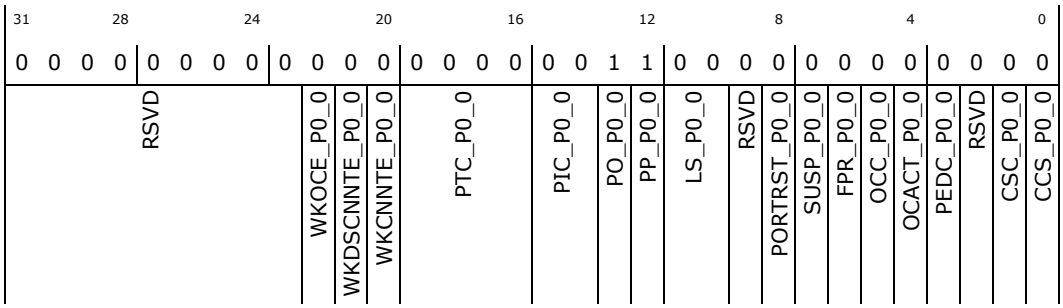
Type: Memory Mapped I/O Register (Size: 32 bits)

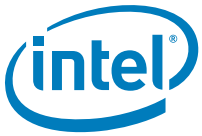
PORTSC1: [MBAR] + 64h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

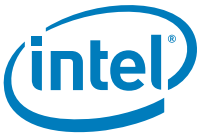
Power Well: Resume

Default: 00003000h





Bit Range	Default & Access	Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set.
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0).
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1).
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one.
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior.
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power.



Bit Range	Default & Access	Description
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared.
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined.

Bit Range	Default & Access	Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero.
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner.
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'.
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it.
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set.

3.17.13 Port Status and Control (PORTSC2)—Offset 68h

Access Method

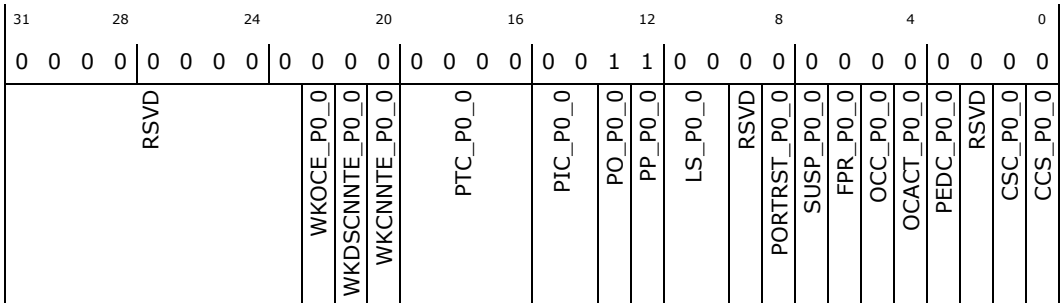
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC2: [MBAR] + 68h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Resume

Default: 00003000h



Bit Range	Default & Access	Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set.
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0).
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1).

Bit Range	Default & Access	Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one.
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior.
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power.
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset
9	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared.
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined.

Bit Range	Default & Access	Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero.
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner.
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'.
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it.
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set.

3.17.14 Port Status and Control (PORTSC3)—Offset 6Ch

Access Method

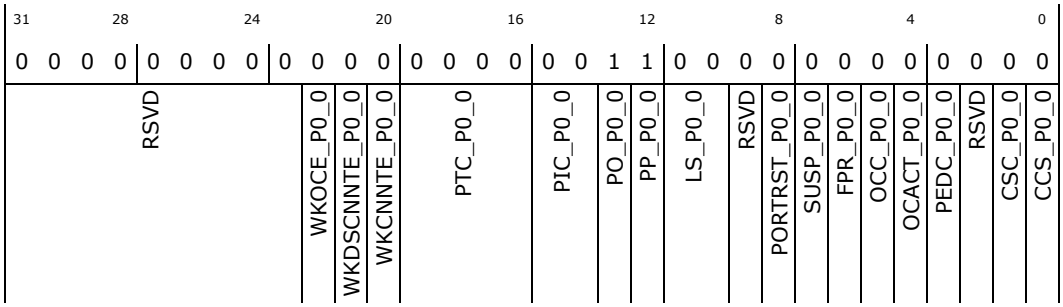
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC3: [MBAR] + 6Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Resume

Default: 00003000h



Bit Range	Default & Access	Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set.
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0).
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1).

Bit Range	Default & Access	Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one.
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior.
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power.
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset
9	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared.
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined.

Bit Range	Default & Access	Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero.
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner.
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'.
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it.
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set.

3.17.15 Port Status and Control (PORTSC4)—Offset 70h

Access Method

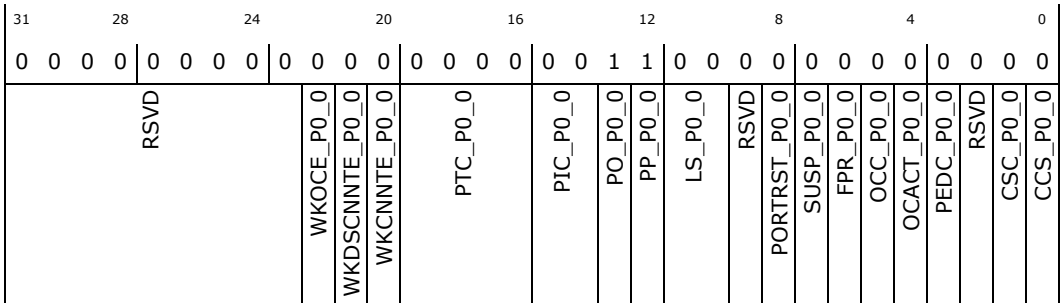
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC4: [MBAR] + 70h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

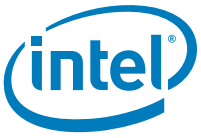
Power Well: Resume

Default: 00003000h



Bit Range	Default & Access	Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set.
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0).
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1).

Bit Range	Default & Access	Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one.
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior.
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power.
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset
9	0b RO	**Reserved (RSVD):** Reserved.



Bit Range	Default & Access	Description
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared.
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined.

Bit Range	Default & Access	Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero.
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner.
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'.
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it.
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set.

3.17.16 Port Status and Control (PORTSC5)—Offset 74h

Access Method

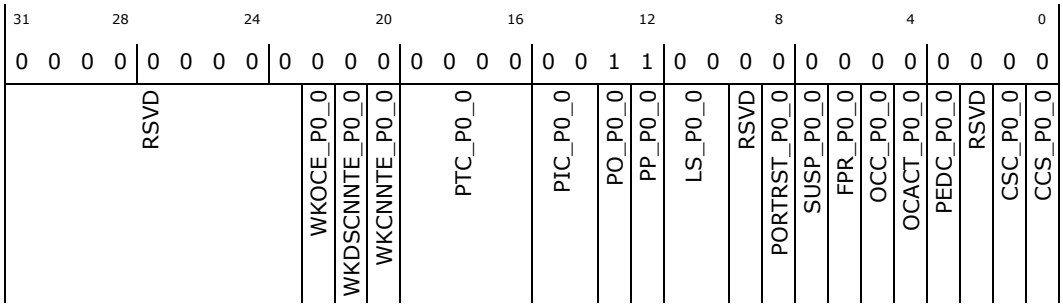
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC5: [MBAR] + 74h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

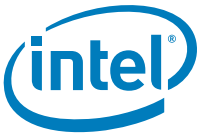
Power Well: Resume

Default: 00003000h



Bit Range	Default & Access	Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set.
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0).
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1).

Bit Range	Default & Access	Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one.
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior.
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power.
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset
9	0b RO	**Reserved (RSVD):** Reserved.



Bit Range	Default & Access	Description
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared.
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined.

Bit Range	Default & Access	Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero.
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner.
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'.
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it.
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set.

3.17.17 Port Status and Control (PORTSC6)—Offset 78h

Access Method

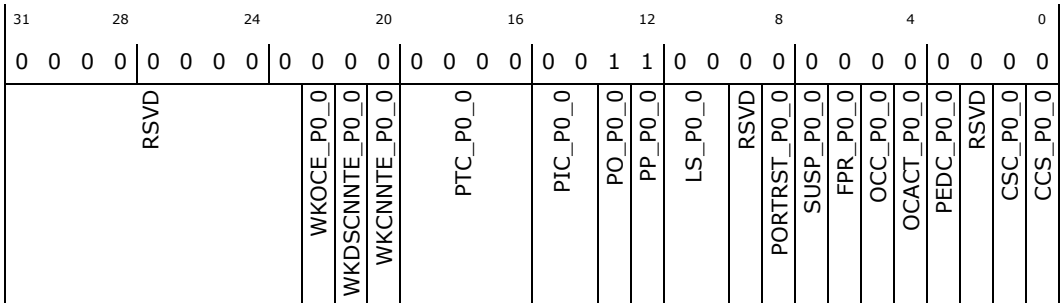
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC6: [MBAR] + 78h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

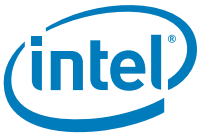
Power Well: Resume

Default: 00003000h



Bit Range	Default & Access	Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set.
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0).
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1).

Bit Range	Default & Access	Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one.
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior.
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power.
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset
9	0b RO	**Reserved (RSVD):** Reserved.



Bit Range	Default & Access	Description
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared.
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined.

Bit Range	Default & Access	Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero.
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner.
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'.
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it.
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set.

3.17.18 Port Status and Control (PORTSC7)—Offset 7Ch

Access Method

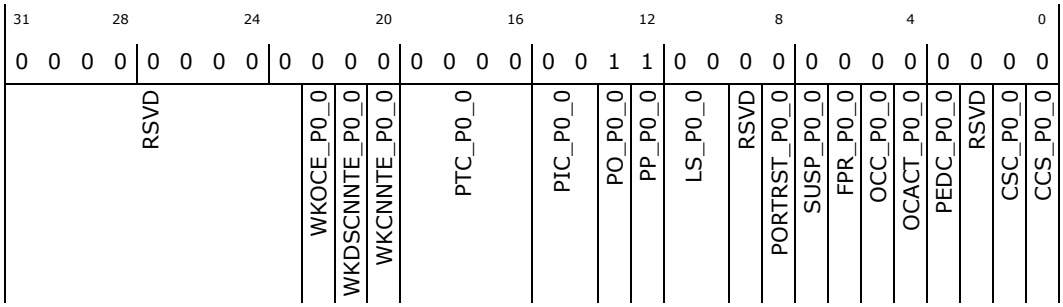
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC7: [MBAR] + 7Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

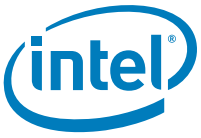
Power Well: Resume

Default: 00003000h



Bit Range	Default & Access	Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set.
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0).
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1).

Bit Range	Default & Access	Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one.
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior.
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power.
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset
9	0b RO	**Reserved (RSVD):** Reserved.



Bit Range	Default & Access	Description
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared.
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined.

Bit Range	Default & Access	Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero.
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner.
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'.
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it.
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set.

3.17.19 Port Status and Control (PORTSC8)—Offset 80h

Access Method

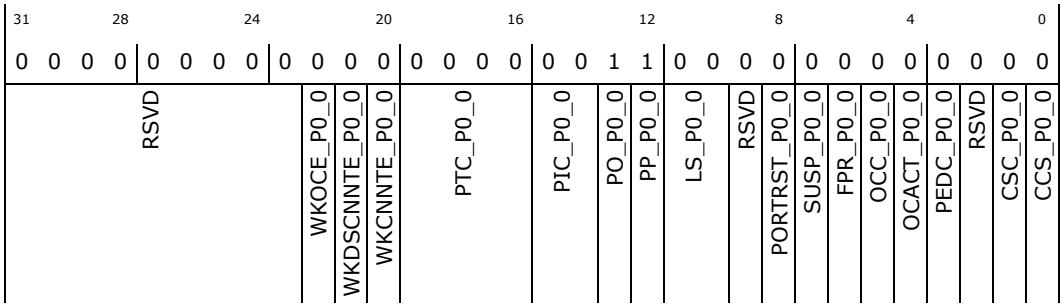
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC8: [MBAR] + 80h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Resume

Default: 00003000h



Bit Range	Default & Access	Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set.
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0).
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1).

Bit Range	Default & Access	Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one.
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior.
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power.
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset
9	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared.
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined.

Bit Range	Default & Access	Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero.
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner.
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'.
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it.
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set.

3.17.20 Debug Port Control/Status Register (DP_CTRLSTS)—Offset A0h

Access Method

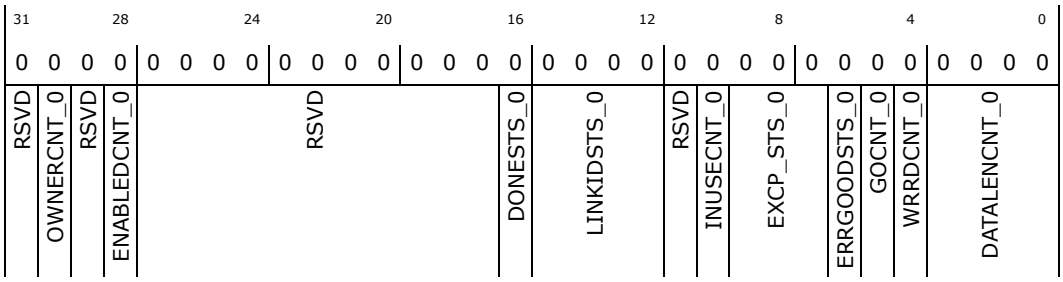
Type: Memory Mapped I/O Register (Size: 32 bits)

DP_CTRLSTS: [MBAR] + A0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RW	**OWNER_CNT (OWNERCNT_0):** When software writes a 1 to this bit, the ownership of the debug port is forced to the EHCI controller (i.e. immediately taken away from the companion Classic USB Host Controller) If the port was already owned by the EHCI controller, then setting this bit has no effect. This bit overrides all of the ownership-related bits in the standard EHCI registers. Note that the value in this bit does not affect the value reported in the PORTSC Port Owner bit.
29	0b RO	**Reserved (RSVD):** Reserved.
28	0b RW	**ENABLED_CNT (ENABLEDCNT_0):** This bit = 1 if the debug port is enabled for operation. Software can clear this by writing a zero to it. The hardware clears the bit for the same conditions where hardware clears the Port Enable/Disable bit (in the PORTSC register). (Note this bit is not cleared when software clears the Port Enabled/Disabled bit in the PORTSC.) Software can directly set this bit if the port is already enabled in the associated Port Status and Control register (this is enforced by the hardware). Reset default = 0.
27:17	00000000000b RO	**Reserved (RSVD):** Reserved.
16	0b RWC	**DONE_STS (DONESTS_0):** Read/Write-Clear. This bit is set by hardware to indicate that the request is complete. Writing a 1 to this bit will clear it if it is set. Writing a 0 to this bit has no effect. Reset default = 0
15:12	0000b RO	**LINK_ID_STS (LINKIDSTS_0):** Read-Only. This field identifies the link interface. It is hardwired to 0h to indicate that it is a USB Debug Port.

Bit Range	Default & Access	Description
11	0b RO	**Reserved (RSVD):** Reserved.
10	0b RO	**IN_USE_CNT (INUSECNT_0):** Set by software to indicate that the port is in use. Cleared by software to indicate that the port is free and may be used by other software. This bit is cleared after reset. (This bit has no affect on hardware.)
9:7	000b RO	**EXCEPTION_STS (EXCP_STS_0):** Read-Only. This field indicates the exception when the ERROR_GOOD#_STS bit is set. This field should be ignored if the ERROR_GOOD#_STS bit is 0. 000 No Error. Note: this should not be seen, since this field should only be checked if there is an error. 001 Transaction error: indicates the USB2 transaction had an error (CRC, bad PID, time out, etc.) 010 HW error. Request was attempted (or in progress) when port was suspended or reset. All Others are reserved Reset default = 000b
6	0b RO	**ERROR_GOOD_STS (ERRGOODSTS_0):** Read-Only. The hardware clears this bit to 0 upon the proper completion of a read or write. The hardware sets this bit to indicate that an error has occurred. Details on the nature of the error are provided in the Exception field. Reset default = 0.
5	0b RW	**GO_CNT (GOCNT_0):** Software sets this bit to cause the hardware to perform a read or write request. Writing a 0 to this bit has no effect. Writing a 1 to this bit when it is already set may result in undefined behavior. When set, the hardware clears this bit when the hardware sets the DONE_STS bit. Reset default = 0.
4	0b RW	**WRITE_READ_CNT (WRRDCNT_0):** Software sets this bit to indicate that the current request is a write. Software clears this bit to indicate that the current request is a read. Reset default = 0.
3:0	0000b RW	**DATA_LEN_CNT (DATALENCNT_0):** This field is used to indicate the size of the data to be transferred. Reset default = 0h. For write operations, this field is set by software to indicate to the hardware how many bytes of data in Data Buffer are to be transferred to the console. A value of 0h indicates that a zero-length packet should be sent. A value of 1-8 indicates 1-8 bytes are to be transferred. Values 9-Fh are illegal and how hardware behaves if used is undefined. For read operations, this field is set by hardware to indicate to software how many bytes in Data Buffer are valid in response to a read operation. A value of 0h indicates that a zero length packet was returned and the state of Data Buffer is not defined. A value of 1-8 indicates 1-8 bytes were received. Hardware is not allowed to return values 9-Fh. The transferring of data always starts with byte 0 in the data area and moves toward byte 7 until the transfer size is reached.

3.17.21 USB PIDs Register (DP_USB_PIDs)—Offset A4h

Access Method

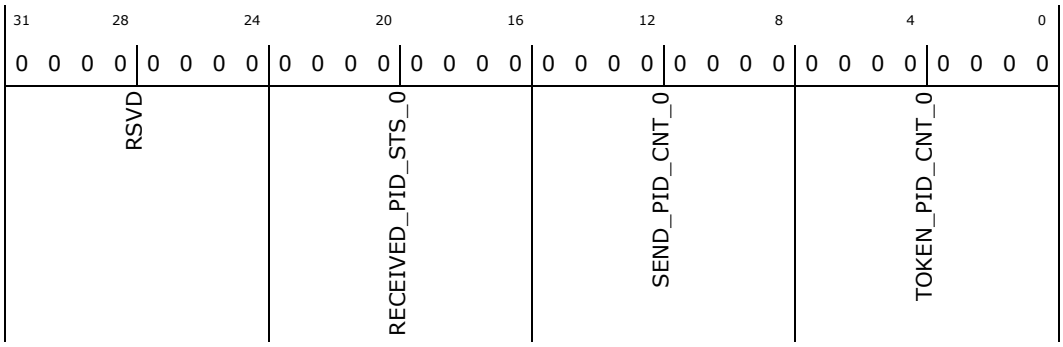
Type: Memory Mapped I/O Register (Size: 32 bits)

DP_USB_PIDs: [MBAR] + A4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved (RSVD):** Reserved.
23:16	00h RO	**RECEIVED_PID_STS (RECEIVED_PID_STS_0):** The hardware updates this field with the received PID for transactions in either direction. When the controller is writing data, this field is updated with the handshake PID that is received from the device. When the host controller is reading data, this field is updated with the data packet PID (if the device sent data), or the handshake PID (if the device NAKs the request). This field is valid when the hardware clears the GO_DONE#_CNT bit. Reset Default = 0.
15:8	00h RW	**SEND_PID_CNT (SEND_PID_CNT_0):** The hardware sends this PID to begin the data packet when sending data to USB (ie. WRITE_READ#_CNT is asserted). Software will typically set this field to either DATA0 or DATA1 PID values. Reset Default = 0
7:0	00h RW	**TOKEN_PID_CNT (TOKEN_PID_CNT_0):** The hardware sends this PID as the Token PID for each USB transaction. Software will typically set this field to either IN, OUT or SETUP PID values. Reset Default = 0.

3.17.22 Debug Port Data Buffer Bytes 7:0 (DP_DATA_BUF_B)—Offset A8h

Access Method

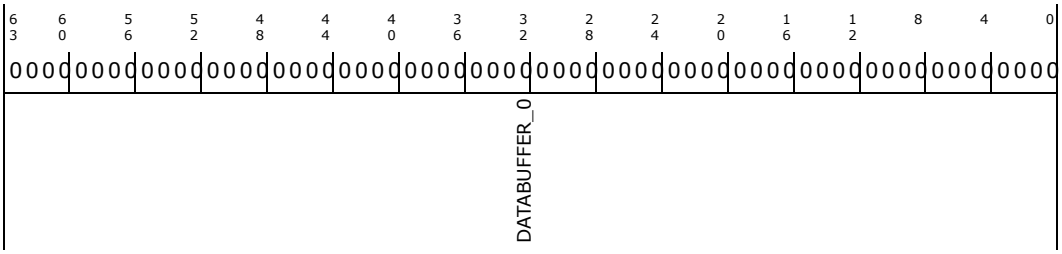
Type: Memory Mapped I/O Register (Size: 64 bits)

DP_DATA_BUF_B: [MBAR] + A8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Power Well: Core

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:0	0000000000000000h RW	**DATABUFFER (DATABUFFER_0):** These are the 8 bytes of the data buffer. Bits 7:0 correspond to least significant byte (byte 0). Bits 63:56 correspond to the most significant byte (byte 7). The bytes in the Data Buffer must be written with data before software initiates a write request. For a read request, the Data Buffer contains valid data when DONE_STS is set by the hardware, ERROR_GOOD#_STS is cleared by the hardware, and the DATA_LENGTH_CNT field indicates the number of bytes that are valid. Reset Default = 0.

3.17.23 Debug Port Config Register (DP_CFG)—Offset B0h

Access Method

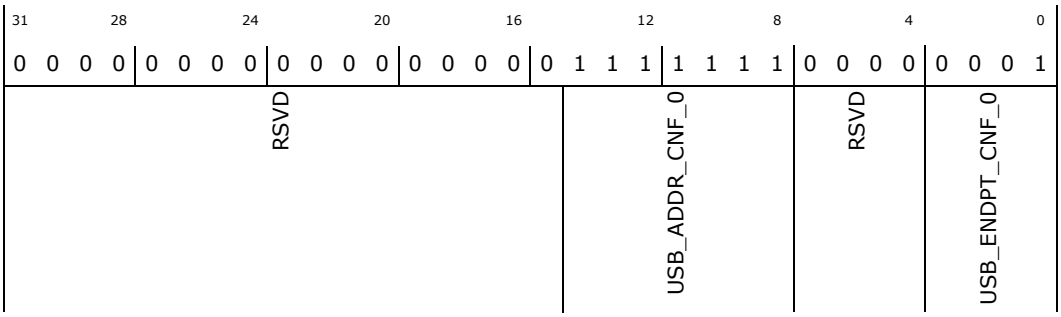
Type: Memory Mapped I/O Register (Size: 32 bits)

DP_CFG: [MBAR] + B0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

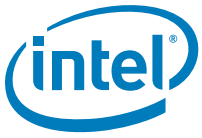
Power Well: Core

Default: 00007F01h



Bit Range	Default & Access	Description
31:15	000000000000000b RO	**Reserved (RSVD):** Reserved.
14:8	7fh RW	**USB_ADDRESS_CNF (USB_ADDR_CNF_0):** 7-bit field that identifies the USB device address used by the controller for all Token PID generation. This is a R/W field that is set to 7Fh after reset

Bit Range	Default & Access	Description
7:4	0000b RO	**Reserved (RSVD):** Reserved.
3:0	01h RW	**USB_ENDPOINT_CNF (USB_ENDPT_CNF_0):** This 4-bit field identifies the endpoint used by the controller for all Token PID generation. This is a R/W field that is set to 01h after reset.



3.18 Low Power Audio I2S0 Address Map

Table 26. Summary of Low Power Audio I2S0 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 1735	00000000h
4h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 1737	43000000h
8h	4	"SSP Status Register (SSSR)—Offset 8h" on page 1739	0000F004h
Ch	4	"SSP Interrupt Test Register (SSITR)—Offset Ch" on page 1740	00000000h
10h	4	"SSP Data Register (SSDR)—Offset 10h" on page 1741	00000000h
28h	4	"SSP Time-Out Register (SSTO)—Offset 28h" on page 1742	00000000h
2Ch	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 1743	00000000h
30h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 1744	00000000h
34h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 1744	00000000h
38h	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 1745	00000000h
3Ch	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 1746	00000000h
40h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 1746	000000C0h
44h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 1748	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 1748	00000000h
68h	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 1749	FFFF0000h
6Ch	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 1750	00000000h
70h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 1750	0002C604h
74h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 1752	00000000h
78h	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 1753	00000000h
7Ch	4	"ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch" on page 1754	00000000h
80h	4	"Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h" on page 1754	00000000h
84h	4	"ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h" on page 1755	00000000h
88h	4	"ASRC Frame Count (ASRC_FRMCNT)—Offset 88h" on page 1756	00000000h

3.18.1 SSP Control 0 Register (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

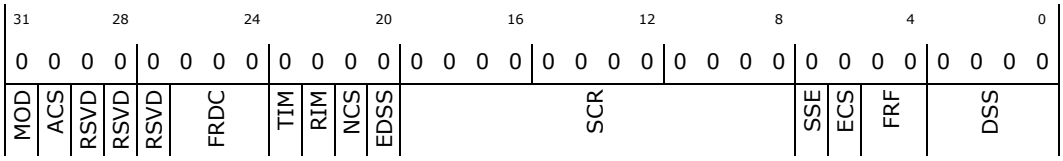
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR0: [BAR + 0A0000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0b RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0b RO	**Reserved (RSVD):** Reserved.
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26:24	000b RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0b RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0b RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0b RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0b RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	000h RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0b RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0b RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	00b RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)

Bit Range	Default & Access	Description
3:0	0000b RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

3.18.2 SSP Control 1 Register (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

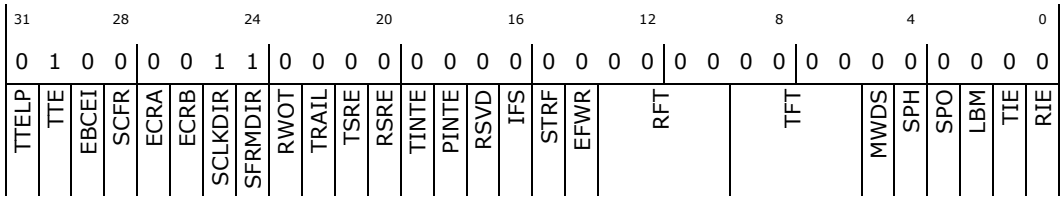
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

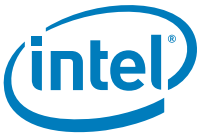
SSCR1: [BAR + 0A0000h] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 43000000h



Bit Range	Default & Access	Description
31	0b RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	1b RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0b RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled
28	0b RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active during transfers
27	0b RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0b RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	1b RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP receives SSPSCLK
24	1b RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0b RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode



Bit Range	Default & Access	Description
22	0b RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0b RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0b RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0b RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0b RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0b RW	**RSVD:** Reserved
16	0b RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0b RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0b RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/ read special function is enabled
13:10	0000b RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0000b RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0b RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0b RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one cycle at the start of a frame and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0b RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0b RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0b RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled

Bit Range	Default & Access	Description
0	0b RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

3.18.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

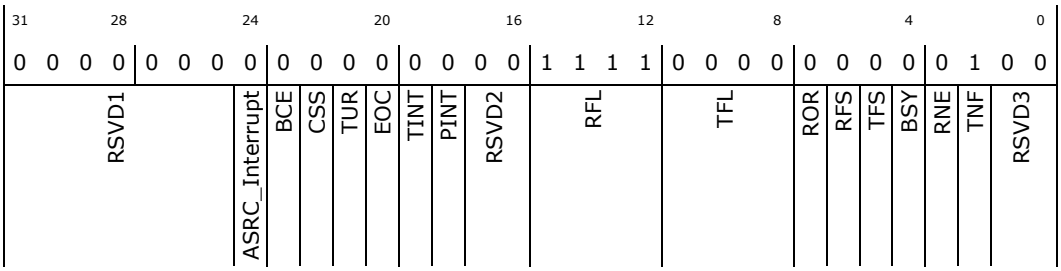
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

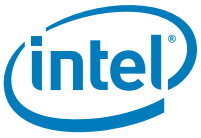
SSSR: [BAR + 0A0000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000F004h



Bit Range	Default & Access	Description
31:25	00h RO	**RSVD1:** Reserved
24	0b RW/1C	**ASRC Interrupt (ASRC_Interrupt):** The interrupt bit is set to 1 when the frame count matches the frame threshold. This is Write 1 to clear register bit.
23	0b RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0b RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0b RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0b RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition



Bit Range	Default & Access	Description
19	0b RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0b RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	00b RO	**RSVD2:** Reserved
15:12	1111b RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0000b RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0b RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0b RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0b RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0b RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0b RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1b RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	00b RO	**RSVD3:** Reserved

3.18.4 SSP Interrupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status

register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

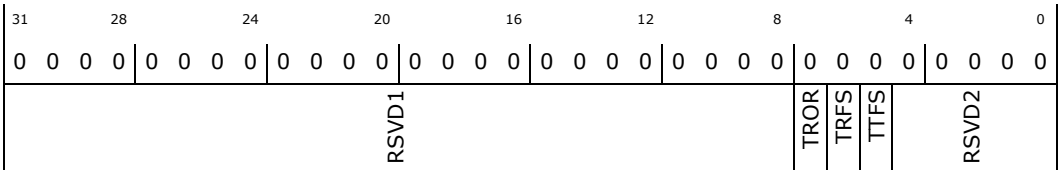
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSITR: [BAR + 0A0000h] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD1:** Reserved
7	0b RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0b RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0b RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	00000b RO	**RSVD2:** Reserved

3.18.5 SSP Data Register (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the

Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

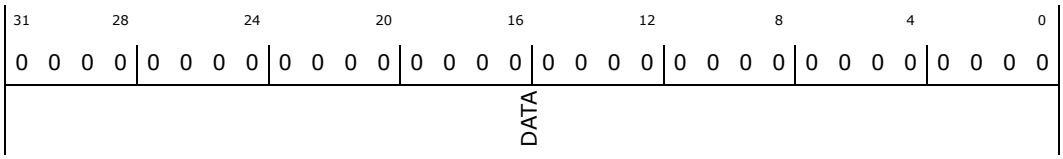
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSDR: [BAR + 0A0000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

3.18.6 SSP Time-Out Register (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes and reads are undetermined.

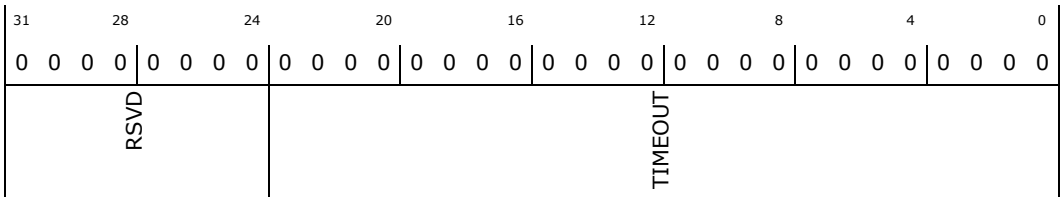
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTO: [BAR + 0A0000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
23:0	000000h RW	**Timeout Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

3.18.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

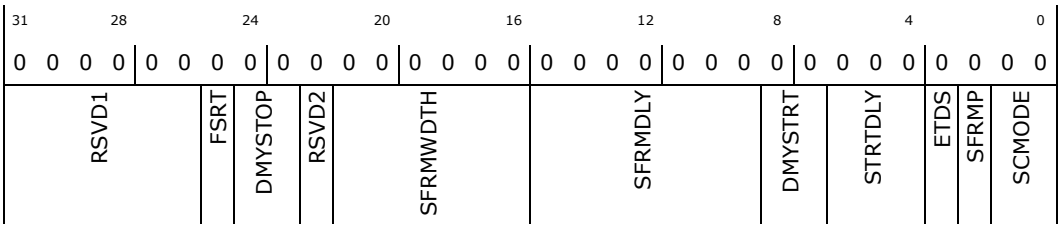
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSPSP: [BAR + 0A0000h] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	000000b RO	**RSVD1:** Reserved
25	0b RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	00b RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0b RW	**RSVD2:** Reserved
21:16	000000b RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0000000b RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	00b RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data

Bit Range	Default & Access	Description
6:4	000b RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0b RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)
2	0b RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	00b RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

3.18.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

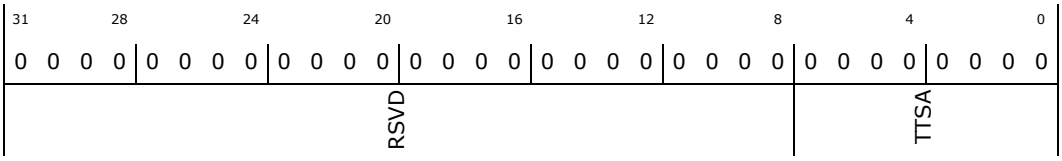
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTSA: [BAR + 0A0000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

3.18.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

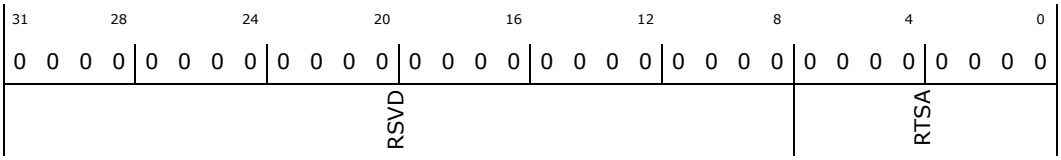
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSRSA: [BAR + 0A0000h] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

3.18.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

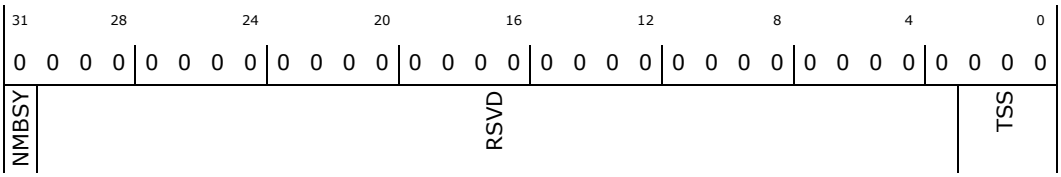
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTSS: [BAR + 0A0000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0000000h RO	**RSVD:** Reserved
2:0	000b RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

3.18.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

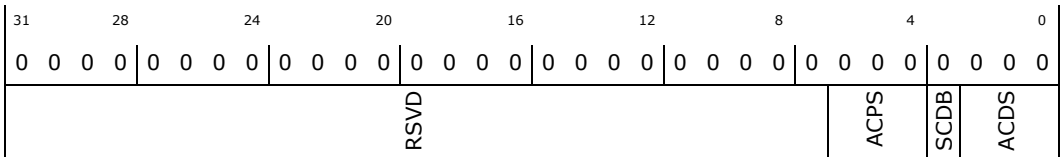
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSACD: [BAR + 0A0000h] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0000000h RO	**RSVD:** Reserved
6:4	000b RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0b RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	000b RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

3.18.12 SSP Control 2 Register (SSCR2)—Offset 40h

The command status register 2 is extension of command status register and contains various feature enable and disables.

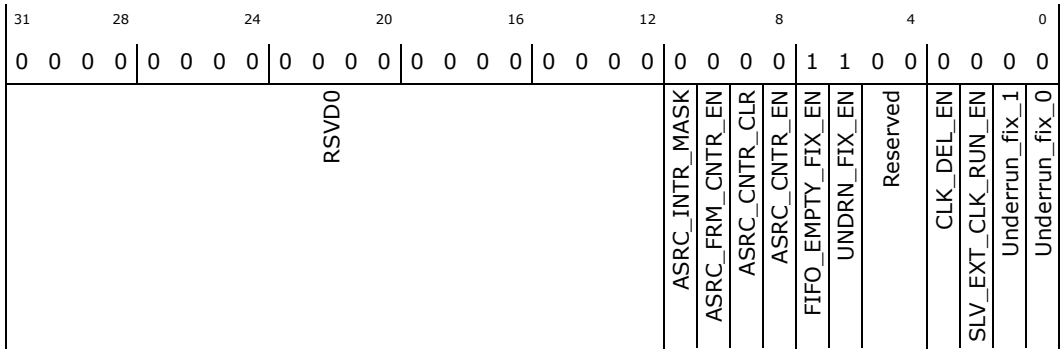
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR2: [BAR + 0A0000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 000000C0h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold. Software should override this bit, since it have no reset value
10	0b RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.
9	0b RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0b RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	1b RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	1b RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5:4	00b RW	**Reserved:** This is a RW bit with no effect on IP behavior
3	0b RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0b RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable

Bit Range	Default & Access	Description
1	0b RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0b RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

3.18.13 SSP Frame Select Register (SSFS)—Offset 44h

The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targeted device.

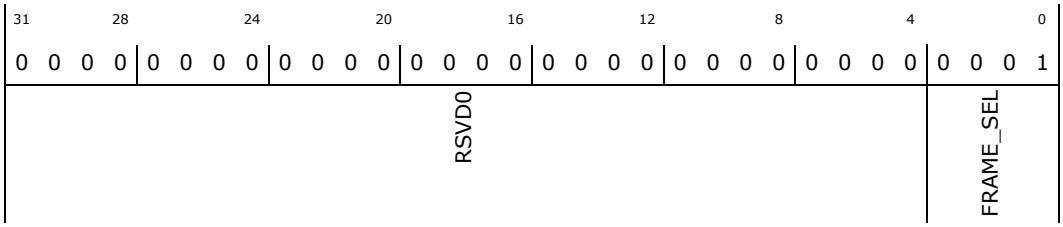
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSFS: [BAR + 0A0000h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:4	0b RO	**RSVD0:** Reserved
3:0	0001b RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

3.18.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support up to 8 slots in network mode there are 8 slot frame counters.

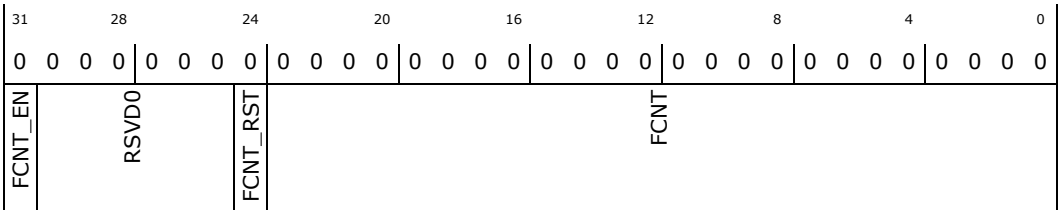
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FRAME_CNT[0-7]: [BAR + 0A0000h] + 48h + [0-7]*4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0b RO	**RSVD0:** Reserved
24	0b WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	000000h RO	**Slot Frame Count (FCNT):** SSP frame count.

3.18.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

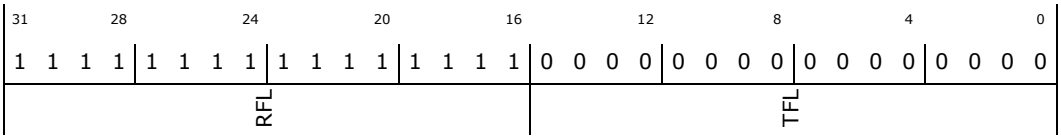
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOL: [BAR + 0A0000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: FFFF0000h



Bit Range	Default & Access	Description
31:16	FFFFh RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.

Bit Range	Default & Access	Description
15:0	0000h RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

3.18.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actual FIFO depth in hardware and not the actual size of the bit field.

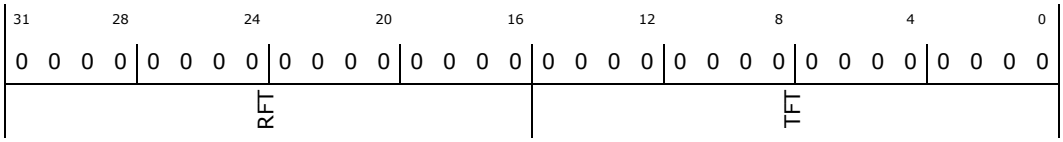
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOTT: [BAR + 0A0000h] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0000h RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

3.18.17 SSP Control 3 Register (SSCR3)—Offset 70h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

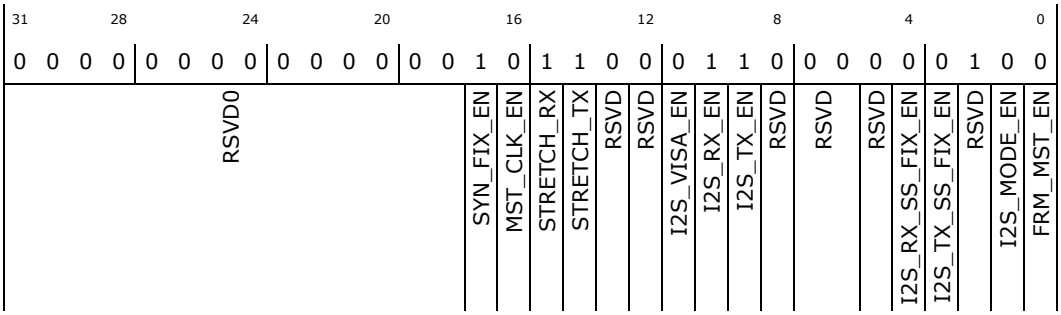
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR3: [BAR + 0A0000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0002C604h



Bit Range	Default & Access	Description
31:18	0b RO	**RSVD0:** Reserved
17	1b RW	**Sync Fix Enable (SYN_FIX_EN):** This is a chicken bit for enabling the synchronizer fix for clr_underrun_ssp signal. SW should preserve this bit at its default value.
16	0b RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	1b RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	1b RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
13	0b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	0b RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals

Bit Range	Default & Access	Description
10	1b RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	1b RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0b RO	**Reserved (RSVD):** Reserved.
7:6	00b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0b RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0b RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

3.18.18 SSP Control 4 Register (SSCR4)—Offset 74h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

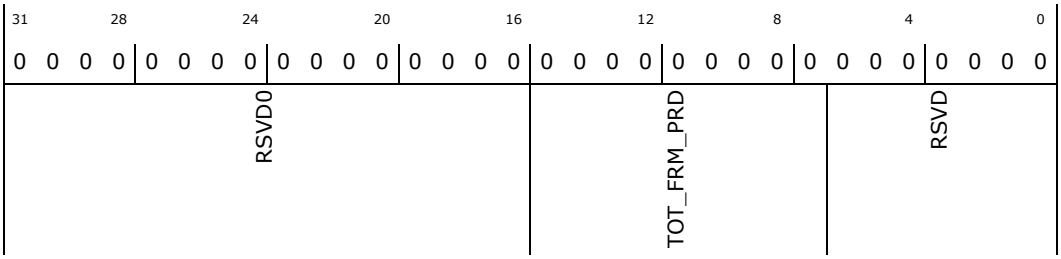
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR4: [BAR + 0A0000h] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:7	000h RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	00h RO	**Reserved (RSVD):** Reserved.

3.18.19 SSP Control 5 Register (SSCR5)—Offset 78h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

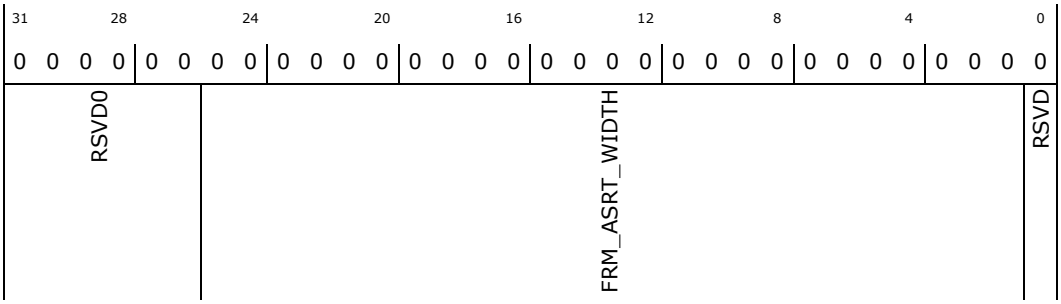
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR5: [BAR + 0A0000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0b RO	**RSVD0:** Reserved
25:1	0000000h RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.
0	0b RO	**Reserved (RSVD):** Reserved.

3.18.20 ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch

This is a 32 bit free running counter that can be enabled, paused or cleared using bits in the SSCR2_XR register. The value reflected here will be noted down in the timer snapshot register when the frame count matches the frame threshold

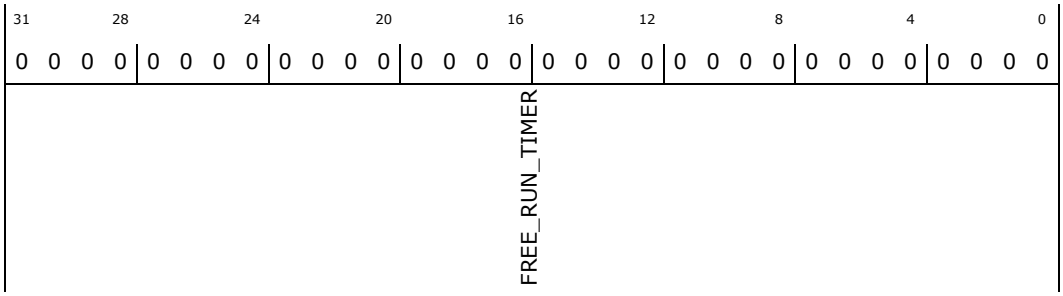
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_FRT: [BAR + 0A0000h] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO/V	**ASRC free running timer (FREE_RUN_TIMER):** This field reflects the value of the free running timer.

3.18.21 Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h

The frame threshold value at which the timer snapshot will be taken is written here.

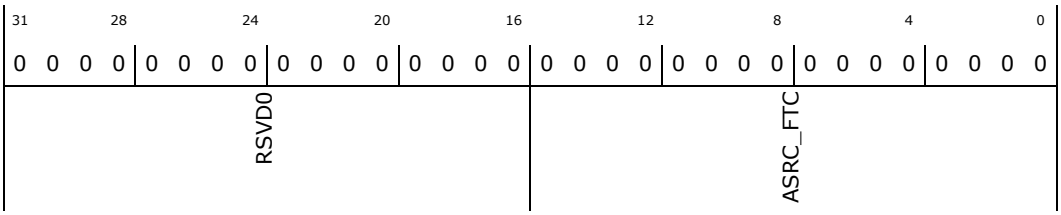
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_FTC: [BAR + 0A0000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RW	**ASRC Frame Threshold (ASRC_FTC):** The 16 bit frame threshold value needs to be written here. Every time the frame count matches the frame threshold a snapshot of the free running timer will be taken and stored in the snapshot register. An interrupt will be generated as well. If the frame threshold is changed on the fly during operation then the following behavior is expected. Previous value = A, New value value = B If B) A : The frame counter keeps counting up to the new value. Nothing happens when the frame counter reaches the old value of A. If B (A : The frame counter resets to zero on the next frame. No interrupt or snapshot is generated in this case.

3.18.22 ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h

Frame Snapshot Register

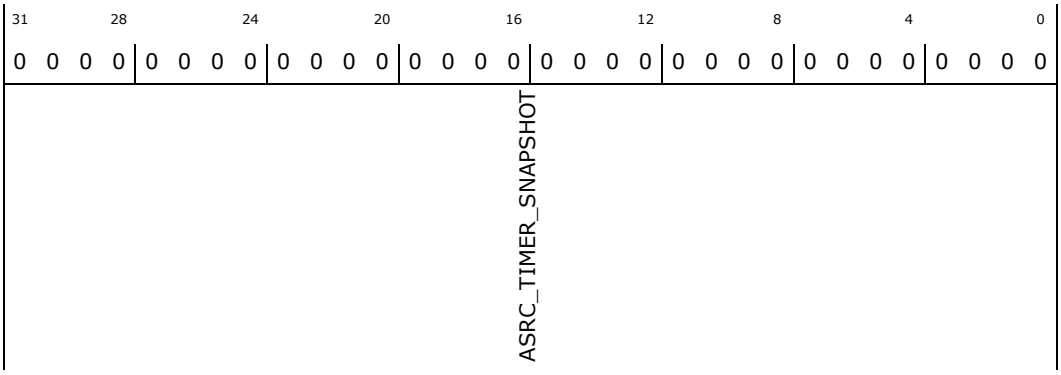
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_SNPSHT: [BAR + 0A0000h] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**ASRC Frame Snapshot (ASRC_TIMER_SNAPSHOT):** This field holds the 32 bit snapshot value. The value is noted on the clock cycle when the frame threshold matches the frame count.

3.18.23 ASRC Frame Count (ASRC_FRMCNT)—Offset 88h

Frame Count Register

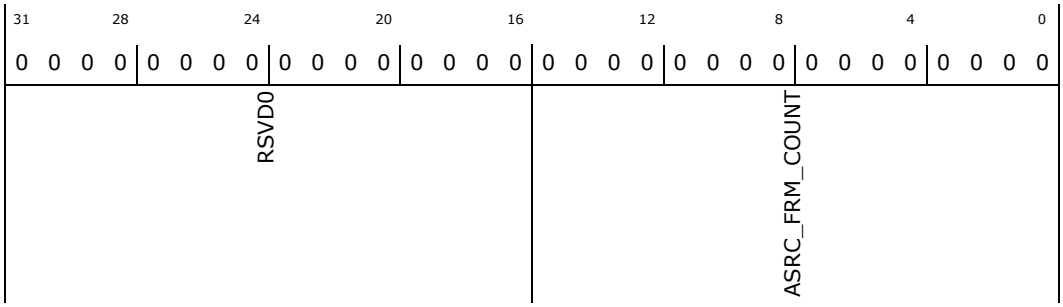
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

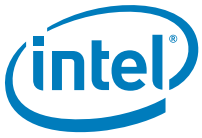
ASRC_FRMCNT: [BAR + 0A0000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RO	**ASRC Frame Count (ASRC_FRM_COUNT):** This is the current frame count. This is a debug register and the value is noted in this register only when the LSB of the frame counter flips. If the counter is cleared when it was at an even value, the cleared value is not reflected here.



3.19 Low Power Audio I²S0 Address Map

Table 27. Summary of Low Power Audio I²S0 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 1757	00000000h
4h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 1759	43000000h
8h	4	"SSP Status Register (SSSR)—Offset 8h" on page 1761	0000F004h
Ch	4	"SSP Interrupt Test Register (SSITR)—Offset Ch" on page 1762	00000000h
10h	4	"SSP Data Register (SSDR)—Offset 10h" on page 1763	00000000h
28h	4	"SSP Time-Out Register (SSTO)—Offset 28h" on page 1764	00000000h
2Ch	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 1765	00000000h
30h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 1766	00000000h
34h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 1766	00000000h
38h	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 1767	00000000h
3Ch	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 1768	00000000h
40h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 1768	000000C0h
44h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 1770	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 1770	00000000h
68h	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 1771	FFFF0000h
6Ch	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 1772	00000000h
70h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 1772	0002C604h
74h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 1774	00000000h
78h	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 1775	00000000h
7Ch	4	"ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch" on page 1776	00000000h
80h	4	"Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h" on page 1776	00000000h
84h	4	"ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h" on page 1777	00000000h
88h	4	"ASRC Frame Count (ASRC_FRMCNT)—Offset 88h" on page 1778	00000000h

3.19.1 SSP Control 0 Register (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

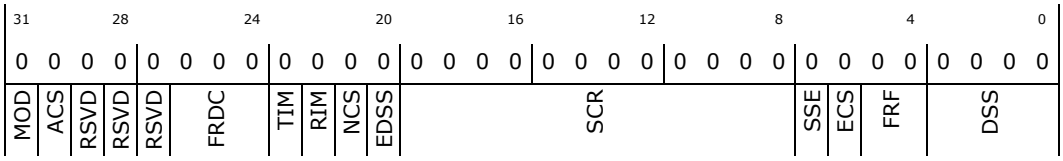
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR0: [BAR + 0A1000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0b RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0b RO	**Reserved (RSVD):** Reserved.
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26:24	000b RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0b RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0b RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0b RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0b RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	000h RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0b RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0b RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	00b RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)

Bit Range	Default & Access	Description
3:0	0000b RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

3.19.2 SSP Control 1 Register (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

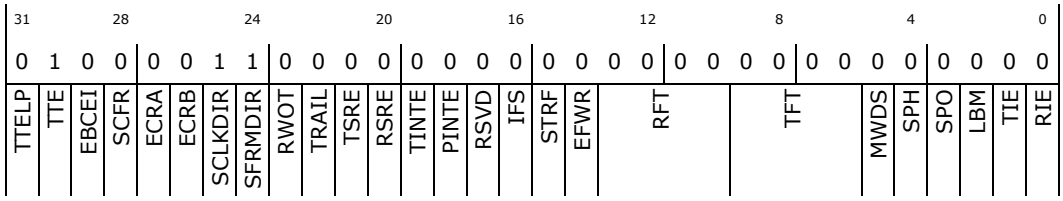
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

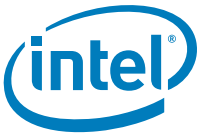
SSCR1: [BAR + 0A1000h] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 43000000h



Bit Range	Default & Access	Description
31	0b RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	1b RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0b RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled
28	0b RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active during transfers
27	0b RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0b RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	1b RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP receives SSPSCLK
24	1b RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0b RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode



Bit Range	Default & Access	Description
22	0b RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0b RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0b RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0b RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0b RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0b RW	**RSVD:** Reserved
16	0b RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0b RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0b RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/ read special function is enabled
13:10	0000b RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0000b RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0b RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0b RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one cycle at the start of a frame and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0b RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0b RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0b RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled

Bit Range	Default & Access	Description
0	0b RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

3.19.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

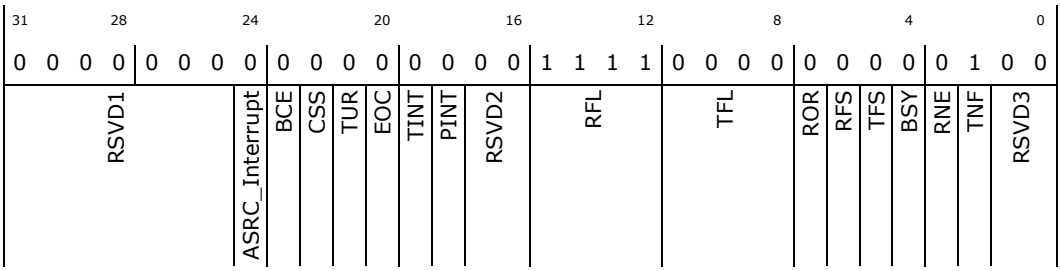
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSSR: [BAR + 0A1000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000F004h



Bit Range	Default & Access	Description
31:25	00h RO	**RSVD1:** Reserved
24	0b RW/1C	**ASRC Interrupt (ASRC_Interrupt):** The interrupt bit is set to 1 when the frame count matches the frame threshold. This is Write 1 to clear register bit.
23	0b RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0b RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0b RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0b RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition

Bit Range	Default & Access	Description
19	0b RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0b RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	00b RO	**RSVD2:** Reserved
15:12	1111b RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0000b RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0b RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0b RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0b RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0b RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0b RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1b RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	00b RO	**RSVD3:** Reserved

3.19.4 SSP Interrupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status

register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

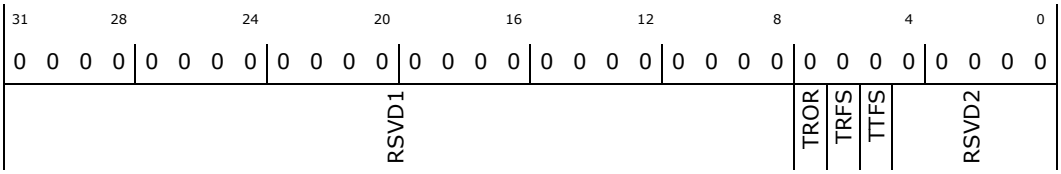
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSITR: [BAR + 0A1000h] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD1:** Reserved
7	0b RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0b RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0b RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	00000b RO	**RSVD2:** Reserved

3.19.5 SSP Data Register (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the

Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

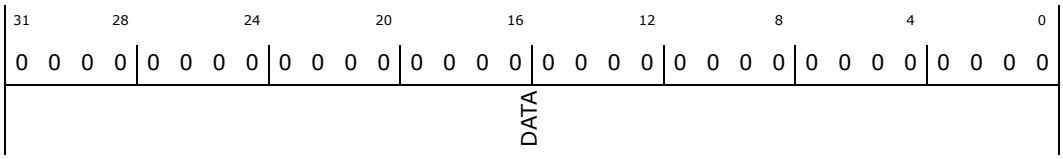
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSDR: [BAR + 0A1000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

3.19.6 SSP Time-Out Register (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes and reads are undetermined.

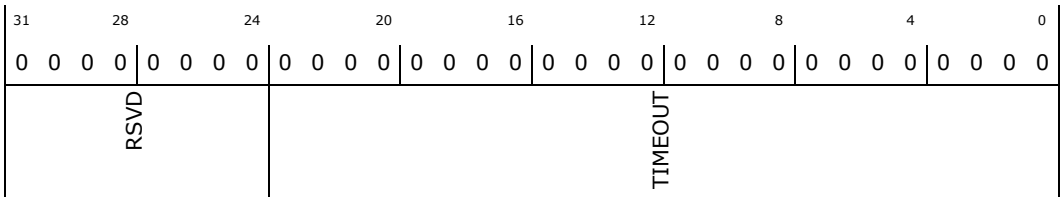
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTO: [BAR + 0A1000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
23:0	000000h RW	**Time out Value (TIMEOUT):** Is the value that defines the time out interval, given by TIMEOUT/Peripheral Clock Frequency

3.19.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

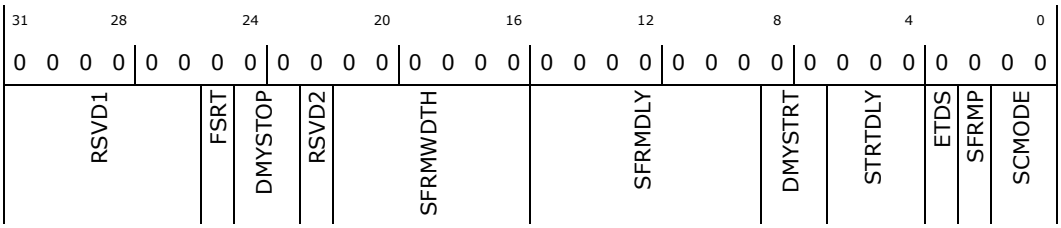
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSPSP: [BAR + 0A1000h] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	000000b RO	**RSVD1:** Reserved
25	0b RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	00b RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0b RW	**RSVD2:** Reserved
21:16	000000b RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0000000b RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	00b RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data

Bit Range	Default & Access	Description
6:4	000b RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0b RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)
2	0b RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	00b RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

3.19.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

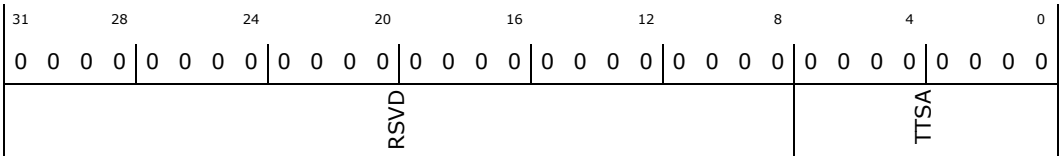
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTSA: [BAR + 0A1000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

3.19.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

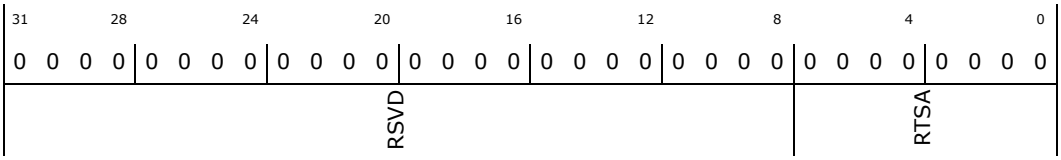
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSRSA: [BAR + 0A1000h] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

3.19.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

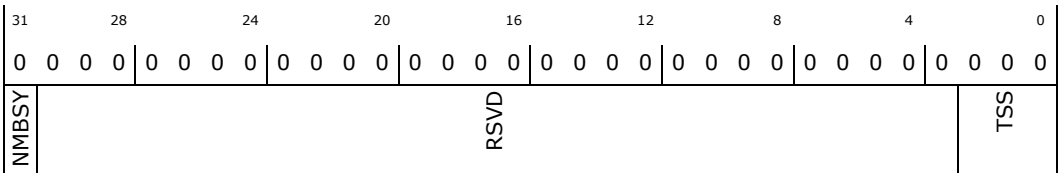
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTSS: [BAR + 0A1000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0000000h RO	**RSVD:** Reserved
2:0	000b RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

3.19.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

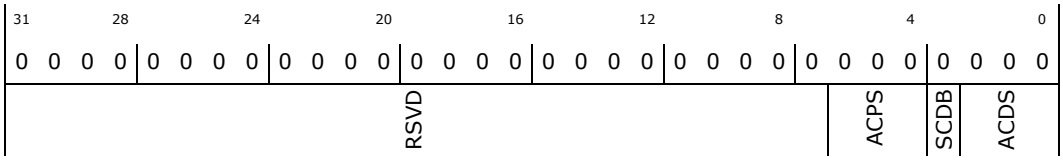
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSACD: [BAR + 0A1000h] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0000000h RO	**RSVD:** Reserved
6:4	000b RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0b RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	000b RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

3.19.12 SSP Control 2 Register (SSCR2)—Offset 40h

The command status register 2 is extension of command status register and contains various feature enable and disables.

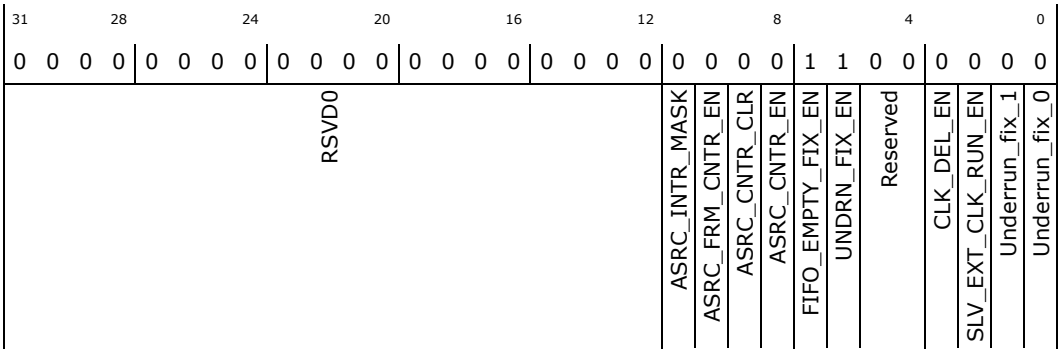
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR2: [BAR + 0A1000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 000000C0h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold. Software should override this bit, since it have no reset value
10	0b RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.
9	0b RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0b RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	1b RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	1b RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5:4	00b RW	**Reserved:** This is a RW bit with no effect on IP behavior
3	0b RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0b RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable

Bit Range	Default & Access	Description
1	0b RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0b RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

3.19.13 SSP Frame Select Register (SSFS)—Offset 44h

The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targeted device.

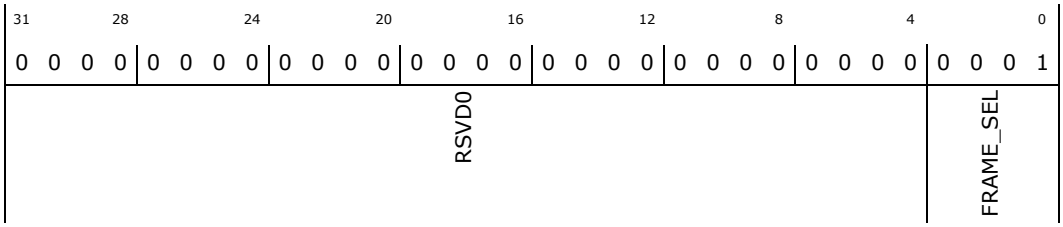
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSFS: [BAR + 0A1000h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:4	0b RO	**RSVD0:** Reserved
3:0	0001b RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

3.19.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support up to 8 slots in network mode there are 8 slot frame counters.

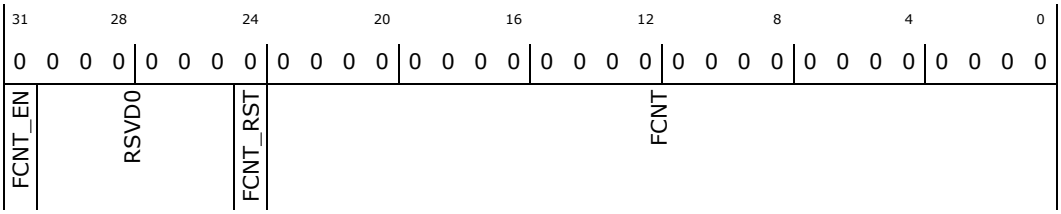
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FRAME_CNT[0-7]: [BAR + 0A1000h] + 48h + [0-7]*4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0b RO	**RSVD0:** Reserved
24	0b WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	000000h RO	**Slot Frame Count (FCNT):** SSP frame count.

3.19.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

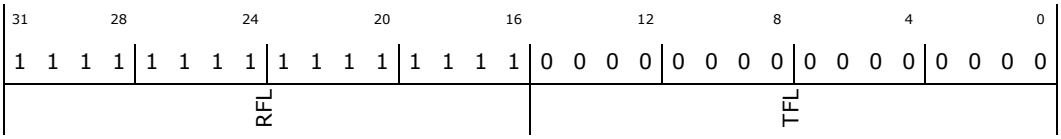
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOL: [BAR + 0A1000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: FFFF0000h



Bit Range	Default & Access	Description
31:16	FFFFh RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.

Bit Range	Default & Access	Description
15:0	0000h RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

3.19.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actual FIFO depth in hardware and not the actual size of the bit field.

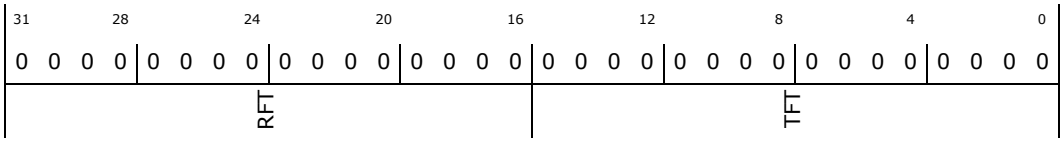
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOTT: [BAR + 0A1000h] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0000h RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

3.19.17 SSP Control 3 Register (SSCR3)—Offset 70h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

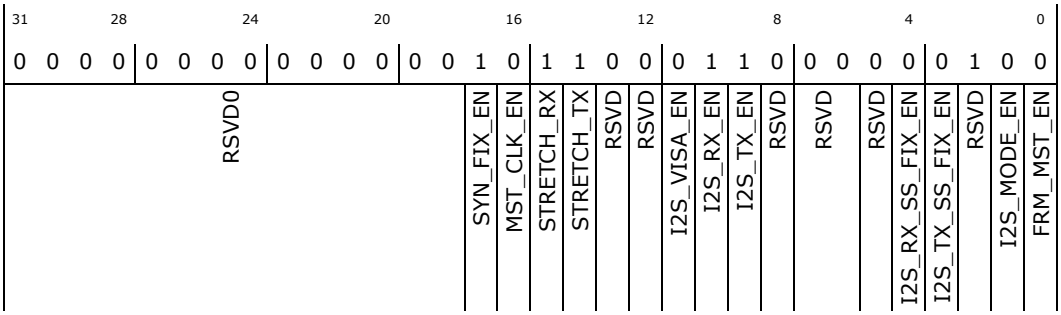
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR3: [BAR + 0A1000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0002C604h



Bit Range	Default & Access	Description
31:18	0b RO	**RSVD0:** Reserved
17	1b RW	**Sync Fix Enable (SYN_FIX_EN):** This is a chicken bit for enabling the synchronizer fix for clr_underrun_ssp signal. SW should preserve this bit at its default value.
16	0b RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	1b RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	1b RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
13	0b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	0b RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals

Bit Range	Default & Access	Description
10	1b RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	1b RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0b RO	**Reserved (RSVD):** Reserved.
7:6	00b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0b RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0b RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

3.19.18 SSP Control 4 Register (SSCR4)—Offset 74h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

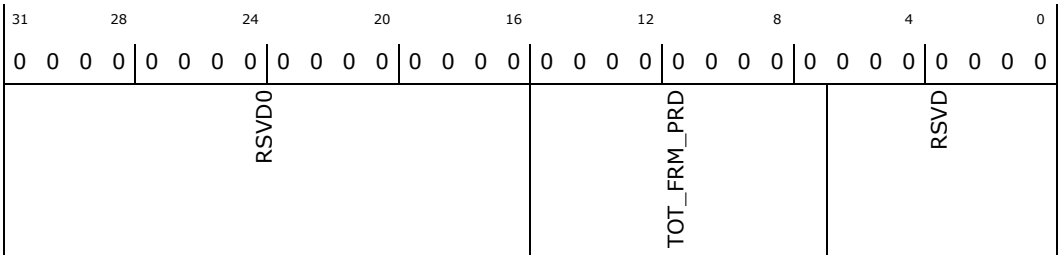
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR4: [BAR + 0A1000h] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:7	000h RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	00h RO	**Reserved (RSVD):** Reserved.

3.19.19 SSP Control 5 Register (SSCR5)—Offset 78h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

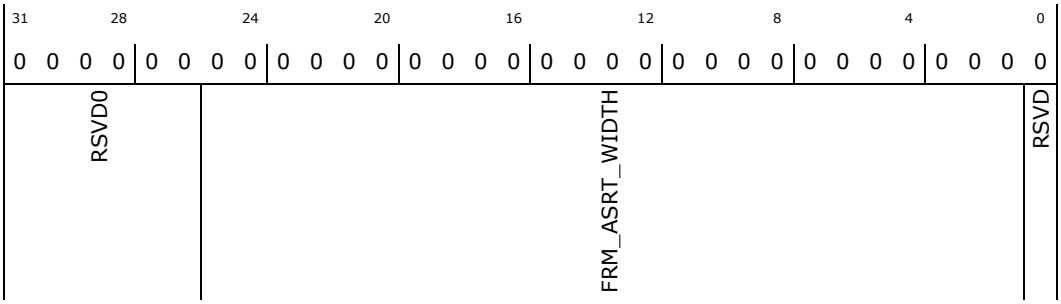
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR5: [BAR + 0A1000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0b RO	**RSVD0:** Reserved
25:1	0000000h RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.
0	0b RO	**Reserved (RSVD):** Reserved.

3.19.20 ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch

This is a 32 bit free running counter that can be enabled, paused or cleared using bits in the SSCR2_XR register. The value reflected here will be noted down in the timer snapshot register when the frame count matches the frame threshold

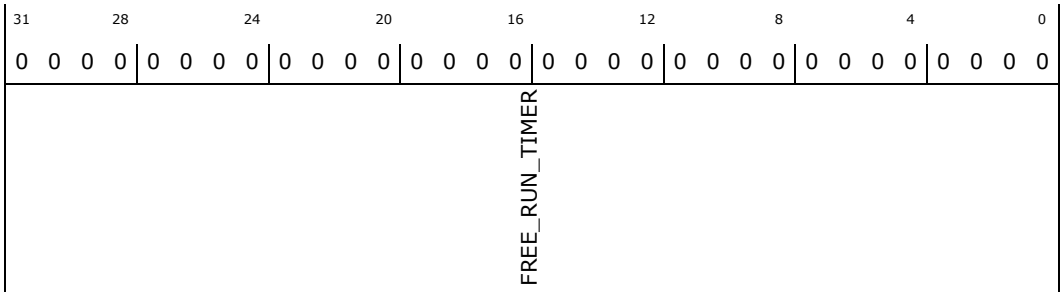
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_FRT: [BAR + 0A1000h] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO/V	**ASRC free running timer (FREE_RUN_TIMER):** This field reflects the value of the free running timer.

3.19.21 Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h

The frame threshold value at which the timer snapshot will be taken is written here.

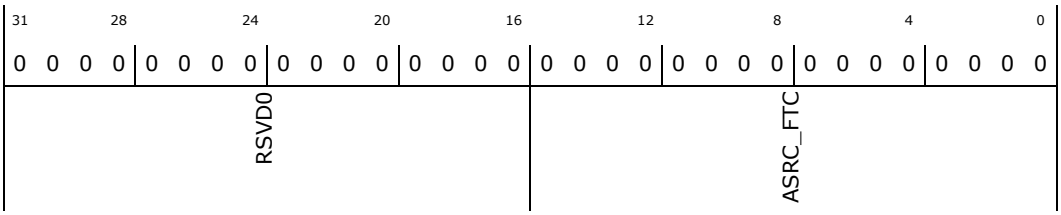
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_FTC: [BAR + 0A1000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RW	**ASRC Frame Threshold (ASRC_FTC):** The 16 bit frame threshold value needs to be written here. Every time the frame count matches the frame threshold a snapshot of the free running timer will be taken and stored in the snapshot register. An interrupt will be generated as well. If the frame threshold is changed on the fly during operation then the following behavior is expected. Previous value = A, New value value = B If B) A : The frame counter keeps counting up to the new value. Nothing happens when the frame counter reaches the old value of A. If B (A : The frame counter resets to zero on the next frame. No interrupt or snapshot is generated in this case.

3.19.22 ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h

Frame Snapshot Register

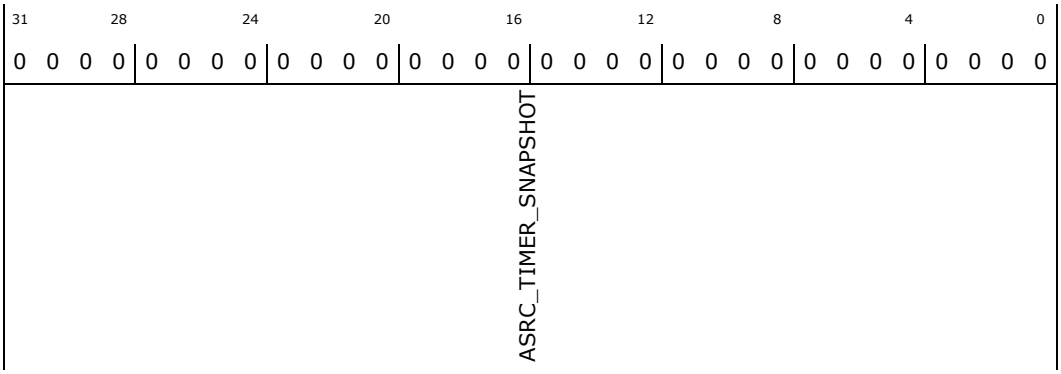
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_SNPSHT: [BAR + 0A1000h] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**ASRC Frame Snapshot (ASRC_TIMER_SNAPSHOT):** This field holds the 32 bit snapshot value. The value is noted on the clock cycle when the frame threshold matches the frame count.

3.19.23 ASRC Frame Count (ASRC_FRMCNT)—Offset 88h

Frame Count Register

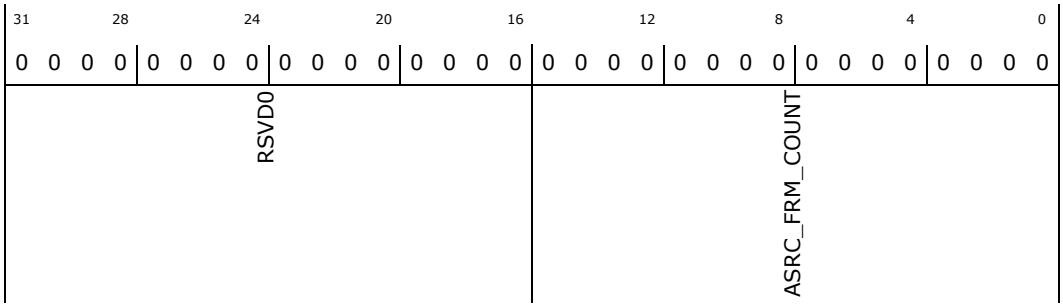
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

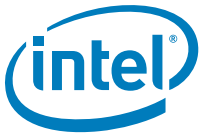
ASRC_FRMCNT: [BAR + 0A1000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RO	**ASRC Frame Count (ASRC_FRM_COUNT):** This is the current frame count. This is a debug register and the value is noted in this register only when the LSB of the frame counter flips. If the counter is cleared when it was at an even value, the cleared value is not reflected here.



3.20 Low Power Audio I2S0 Address Map

Table 28. Summary of Low Power Audio I2S0 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 1779	00000000h
4h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 1781	43000000h
8h	4	"SSP Status Register (SSSR)—Offset 8h" on page 1783	0000F004h
Ch	4	"SSP Interrupt Test Register (SSITR)—Offset Ch" on page 1784	00000000h
10h	4	"SSP Data Register (SSDR)—Offset 10h" on page 1785	00000000h
28h	4	"SSP Time-Out Register (SSTO)—Offset 28h" on page 1786	00000000h
2Ch	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 1787	00000000h
30h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 1788	00000000h
34h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 1788	00000000h
38h	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 1789	00000000h
3Ch	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 1790	00000000h
40h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 1790	000000C0h
44h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 1792	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 1792	00000000h
68h	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 1793	FFFF0000h
6Ch	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 1794	00000000h
70h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 1794	0002C604h
74h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 1796	00000000h
78h	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 1797	00000000h
7Ch	4	"ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch" on page 1798	00000000h
80h	4	"Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h" on page 1798	00000000h
84h	4	"ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h" on page 1799	00000000h
88h	4	"ASRC Frame Count (ASRC_FRMCNT)—Offset 88h" on page 1800	00000000h

3.20.1 SSP Control 0 Register (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

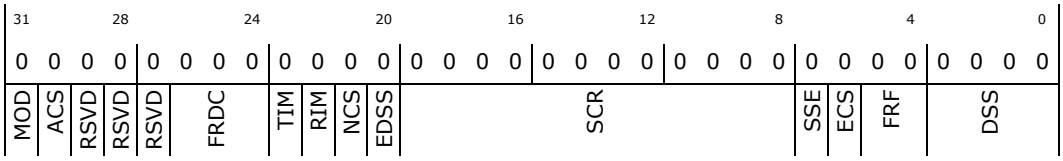
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR0: [BAR + 0A2000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0b RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0b RO	**Reserved (RSVD):** Reserved.
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26:24	000b RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0b RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0b RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0b RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0b RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	000h RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0b RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0b RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	00b RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)

Bit Range	Default & Access	Description
3:0	0000b RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

3.20.2 SSP Control 1 Register (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

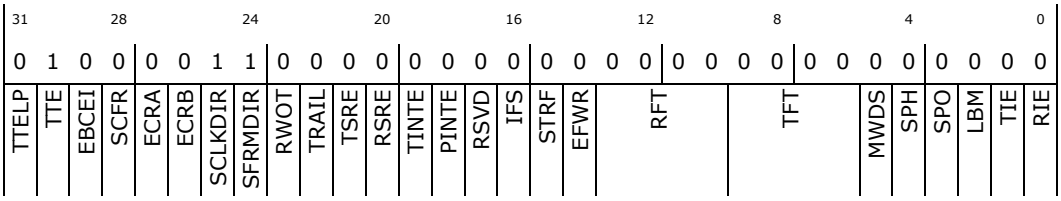
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR1: [BAR + 0A2000h] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 43000000h



Bit Range	Default & Access	Description
31	0b RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	1b RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0b RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled
28	0b RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active during transfers
27	0b RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0b RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	1b RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP receives SSPSCLK
24	1b RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0b RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode

Bit Range	Default & Access	Description
22	0b RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0b RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0b RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0b RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0b RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0b RW	**RSVD:** Reserved
16	0b RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0b RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0b RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/ read special function is enabled
13:10	0000b RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0000b RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0b RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0b RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one cycle at the start of a frame and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0b RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0b RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0b RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled

Bit Range	Default & Access	Description
0	0b RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

3.20.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

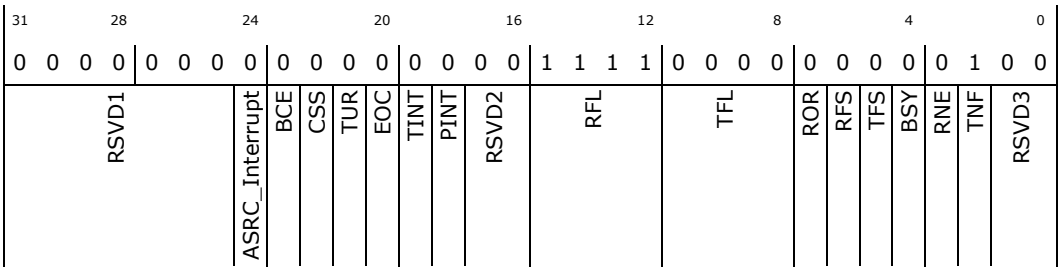
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

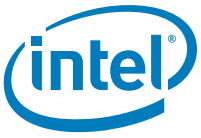
SSSR: [BAR + 0A2000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000F004h



Bit Range	Default & Access	Description
31:25	00h RO	**RSVD1:** Reserved
24	0b RW/1C	**ASRC Interrupt (ASRC_Interrupt):** The interrupt bit is set to 1 when the frame count matches the frame threshold. This is Write 1 to clear register bit.
23	0b RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0b RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0b RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0b RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition



Bit Range	Default & Access	Description
19	0b RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0b RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	00b RO	**RSVD2:** Reserved
15:12	1111b RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0000b RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0b RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0b RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0b RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0b RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0b RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1b RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	00b RO	**RSVD3:** Reserved

3.20.4 SSP Interrupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status

register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

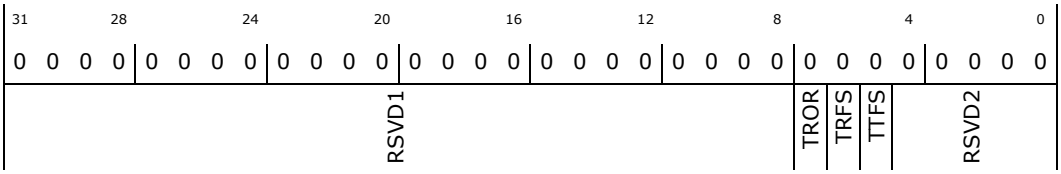
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSITR: [BAR + 0A2000h] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD1:** Reserved
7	0b RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0b RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0b RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	00000b RO	**RSVD2:** Reserved

3.20.5 SSP Data Register (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the

Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

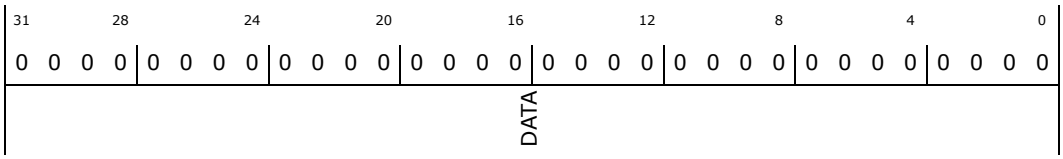
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSDR: [BAR + 0A2000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

3.20.6 SSP Time-Out Register (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes and reads are undetermined.

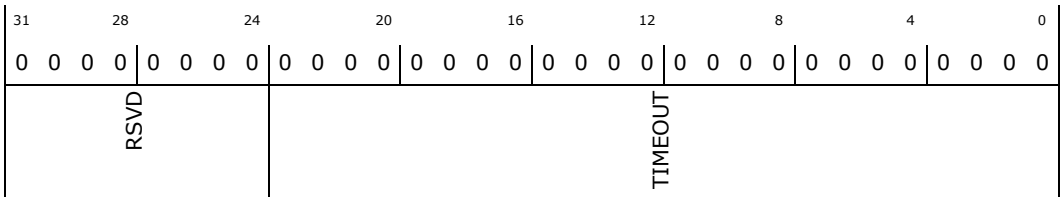
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTO: [BAR + 0A2000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
23:0	000000h RW	**Time out Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

3.20.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

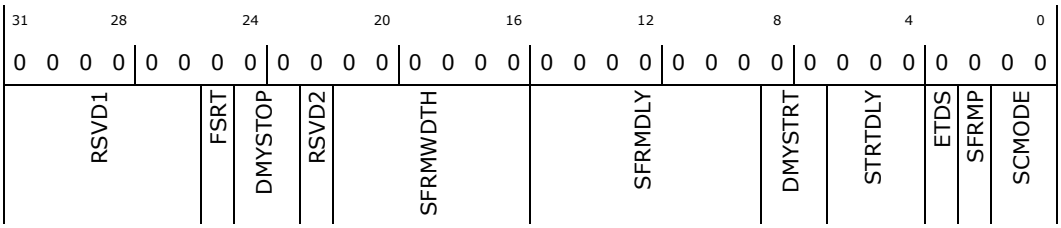
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSPSP: [BAR + 0A2000h] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	000000b RO	**RSVD1:** Reserved
25	0b RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	00b RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0b RW	**RSVD2:** Reserved
21:16	000000b RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0000000b RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	00b RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data

Bit Range	Default & Access	Description
6:4	000b RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0b RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)
2	0b RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	00b RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

3.20.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

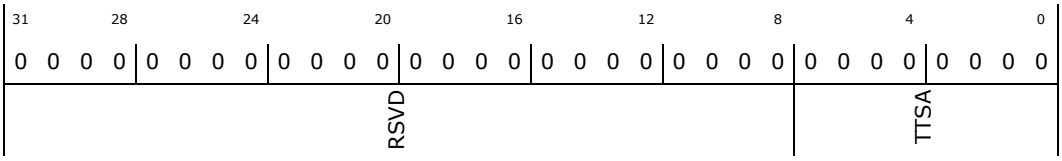
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTSA: [BAR + 0A2000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

3.20.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

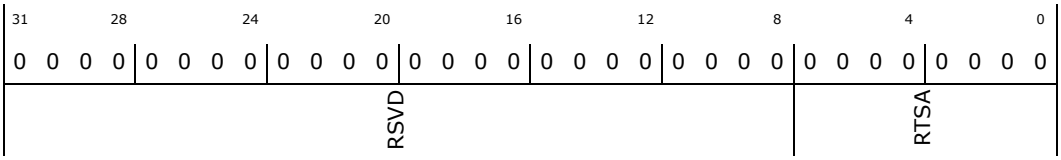
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSRSA: [BAR + 0A2000h] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

3.20.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

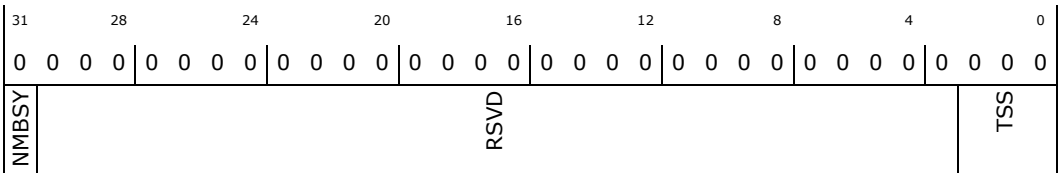
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTSS: [BAR + 0A2000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0000000h RO	**RSVD:** Reserved
2:0	000b RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

3.20.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

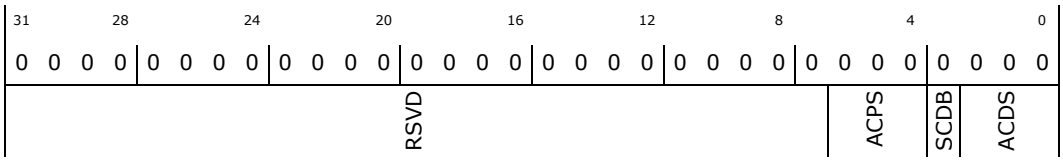
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSACD: [BAR + 0A2000h] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0000000h RO	**RSVD:** Reserved
6:4	000b RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0b RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	000b RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

3.20.12 SSP Control 2 Register (SSCR2)—Offset 40h

The command status register 2 is extension of command status register and contains various feature enable and disables.

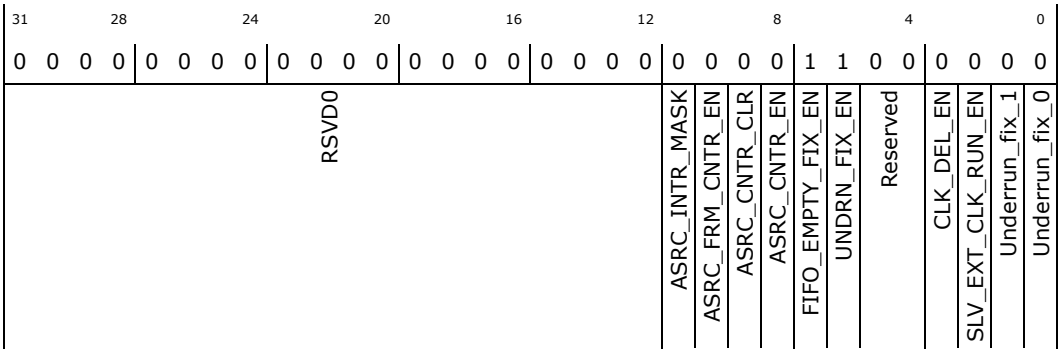
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR2: [BAR + 0A2000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 000000C0h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold. Software should override this bit, since it have no reset value
10	0b RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.
9	0b RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0b RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	1b RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	1b RW	**Under run fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5:4	00b RW	**Reserved:** This is a RW bit with no effect on IP behavior
3	0b RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0b RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable

Bit Range	Default & Access	Description
1	0b RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0b RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

3.20.13 SSP Frame Select Register (SSFS)—Offset 44h

The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targeted device.

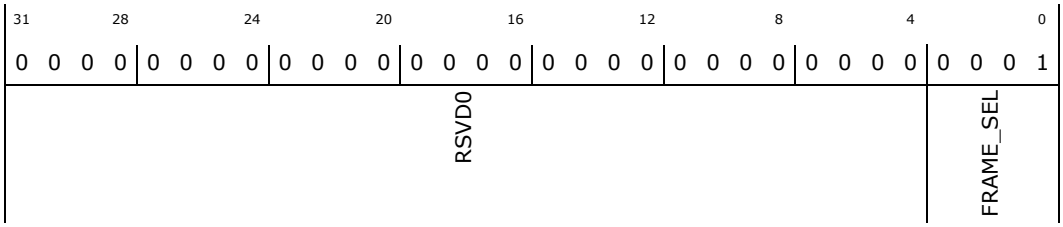
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSFS: [BAR + 0A2000h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:4	0b RO	**RSVD0:** Reserved
3:0	0001b RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

3.20.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support up to 8 slots in network mode there are 8 slot frame counters.

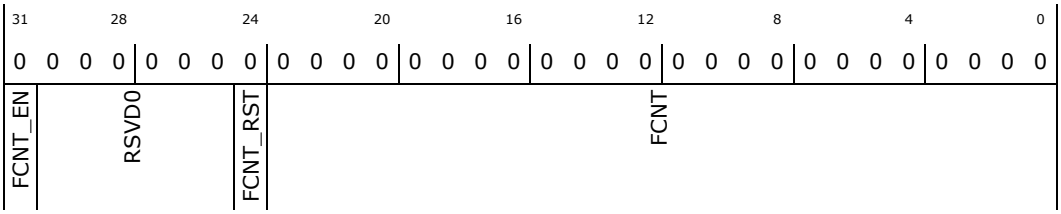
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FRAME_CNT[0-7]: [BAR + 0A2000h] + 48h + [0-7]*4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0b RO	**RSVD0:** Reserved
24	0b WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	000000h RO	**Slot Frame Count (FCNT):** SSP frame count.

3.20.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

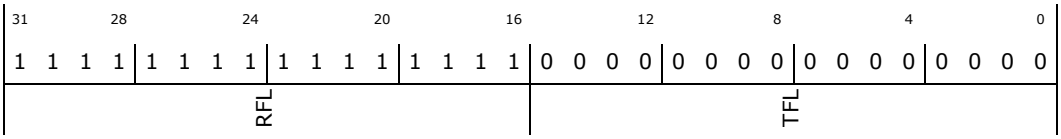
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOL: [BAR + 0A2000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: FFFF0000h



Bit Range	Default & Access	Description
31:16	FFFFh RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.

Bit Range	Default & Access	Description
15:0	0000h RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

3.20.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actual FIFO depth in hardware and not the actual size of the bit field.

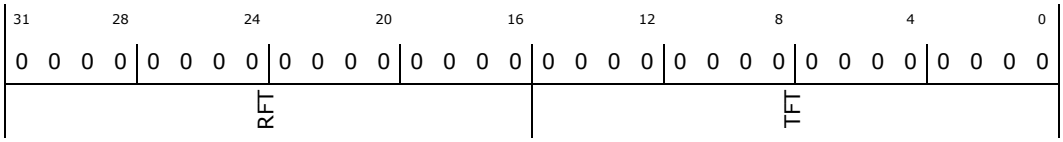
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOTT: [BAR + 0A2000h] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0000h RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

3.20.17 SSP Control 3 Register (SSCR3)—Offset 70h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

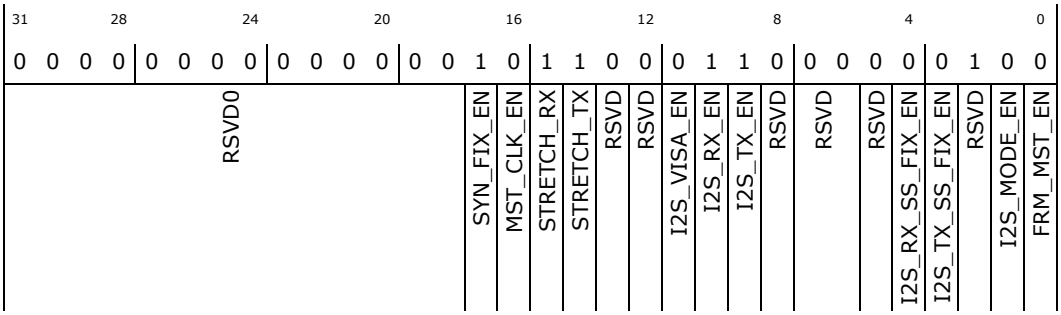
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR3: [BAR + 0A2000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0002C604h



Bit Range	Default & Access	Description
31:18	0b RO	**RSVD0:** Reserved
17	1b RW	**Sync Fix Enable (SYN_FIX_EN):** This is a chicken bit for enabling the synchronizer fix for clr_underrun_ssp signal. SW should preserve this bit at its default value.
16	0b RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	1b RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	1b RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
13	0b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	0b RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals

Bit Range	Default & Access	Description
10	1b RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	1b RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0b RO	**Reserved (RSVD):** Reserved.
7:6	00b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0b RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0b RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

3.20.18 SSP Control 4 Register (SSCR4)—Offset 74h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

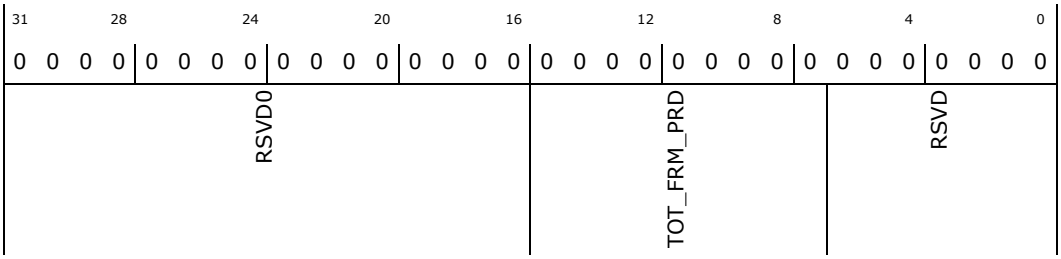
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR4: [BAR + 0A2000h] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:7	000h RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	00h RO	**Reserved (RSVD):** Reserved.

3.20.19 SSP Control 5 Register (SSCR5)—Offset 78h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

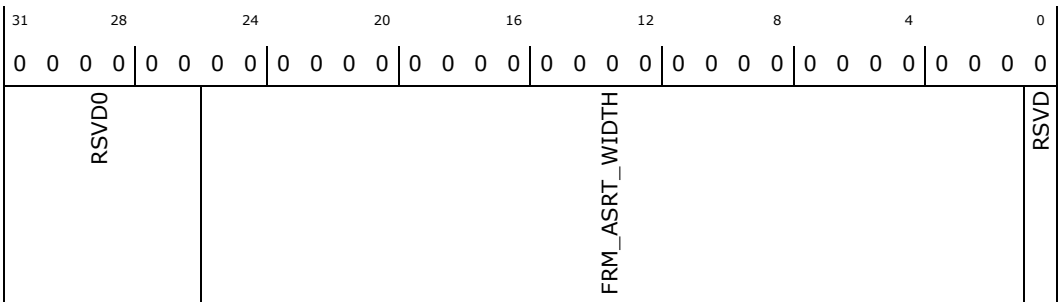
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR5: [BAR + 0A2000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0b RO	**RSVD0:** Reserved
25:1	0000000h RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.
0	0b RO	**Reserved (RSVD):** Reserved.

3.20.20 ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch

This is a 32 bit free running counter that can be enabled, paused or cleared using bits in the SSCR2_XR register. The value reflected here will be noted down in the timer snapshot register when the frame count matches the frame threshold

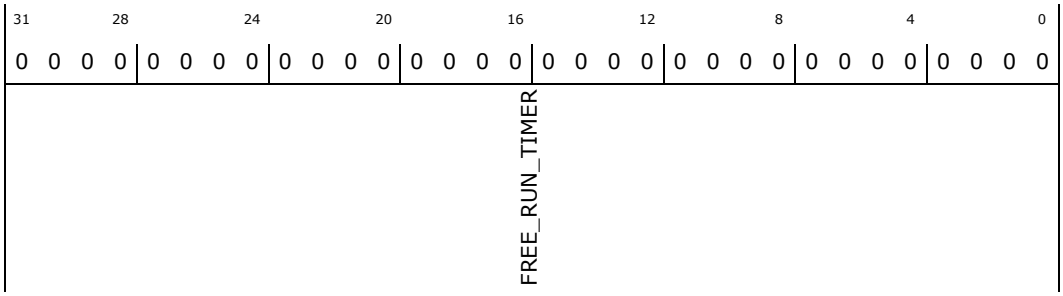
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_FRT: [BAR + 0A2000h] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO/V	**ASRC free running timer (FREE_RUN_TIMER):** This field reflects the value of the free running timer.

3.20.21 Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h

The frame threshold value at which the timer snapshot will be taken is written here.

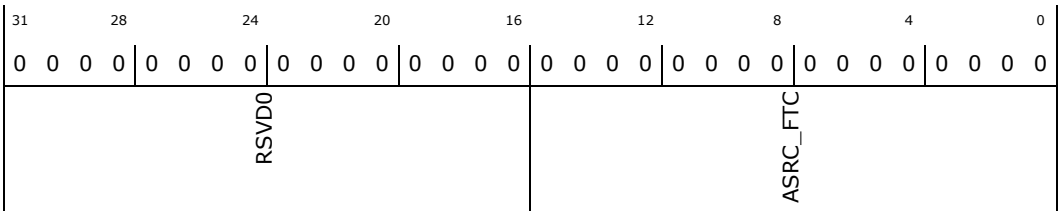
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_FTC: [BAR + 0A2000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RW	**ASRC Frame Threshold (ASRC_FTC):** The 16 bit frame threshold value needs to be written here. Every time the frame count matches the frame threshold a snapshot of the free running timer will be taken and stored in the snapshot register. An interrupt will be generated as well. If the frame threshold is changed on the fly during operation then the following behavior is expected. Previous value = A, New value value = B If B) A : The frame counter keeps counting up to the new value. Nothing happens when the frame counter reaches the old value of A. If B (A : The frame counter resets to zero on the next frame. No interrupt or snapshot is generated in this case.

3.20.22 ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h

Frame Snapshot Register

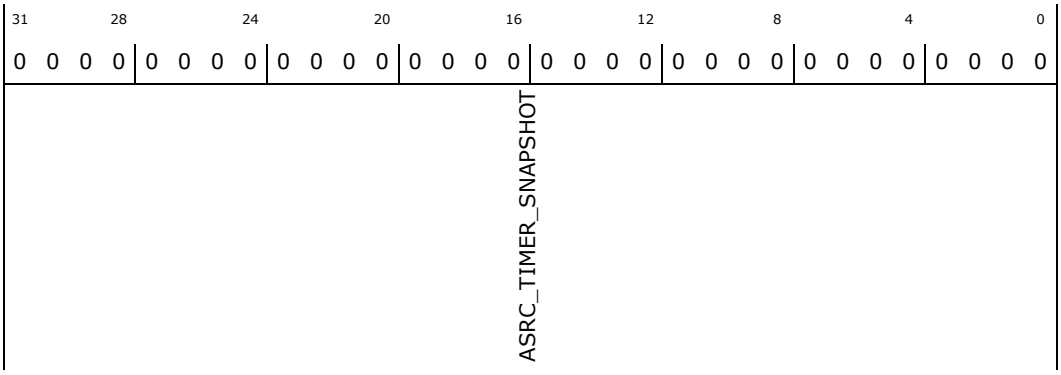
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_SNPSHT: [BAR + 0A2000h] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**ASRC Frame Snapshot (ASRC_TIMER_SNAPSHOT):** This field holds the 32 bit snapshot value. The value is noted on the clock cycle when the frame threshold matches the frame count.

3.20.23 ASRC Frame Count (ASRC_FRMCNT)—Offset 88h

Frame Count Register

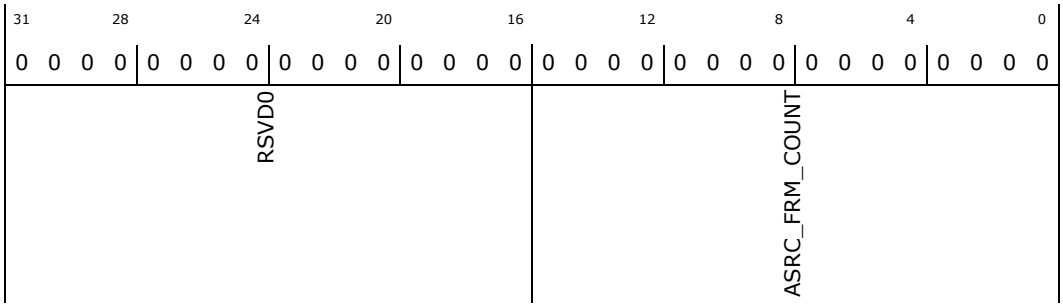
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

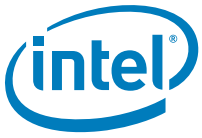
ASRC_FRMCNT: [BAR + 0A2000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RO	**ASRC Frame Count (ASRC_FRM_COUNT):** This is the current frame count. This is a debug register and the value is noted in this register only when the LSB of the frame counter flips. If the counter is cleared when it was at an even value, the cleared value is not reflected here.



3.21 Low Power Audio DMA0 Memory Mapped IO Registers

Table 29. Summary of Low Power Audio DMA0 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_SAR_type (SAR0)—Offset 0h" on page 1805	00000000h
8h	4	"reg_DAR_type (DAR0)—Offset 8h" on page 1806	00000000h
10h	4	"reg_LLP_type (LLP0)—Offset 10h" on page 1807	00000000h
18h	4	"reg_CTL_LO_type (CTL_LO0)—Offset 18h" on page 1808	00000000h
1Ch	4	"reg_CTL_HI_type (CTL_HI0)—Offset 1Ch" on page 1809	00000000h
20h	4	"reg_SSTAT_type (SSTAT0)—Offset 20h" on page 1811	00000000h
28h	4	"reg_DSTAT_type (DSTAT0)—Offset 28h" on page 1811	00000000h
30h	4	"reg_SSTATAR_type (SSTATAR0)—Offset 30h" on page 1812	00000000h
38h	4	"reg_DSTATAR_type (DSTATAR0)—Offset 38h" on page 1812	00000000h
40h	4	"reg_CFG_LO_type (CFG_LO0)—Offset 40h" on page 1813	00000203h
44h	4	"reg_CFG_HI_type (CFG_HI0)—Offset 44h" on page 1815	00000000h
48h	4	"reg_SGR_type (SGR0)—Offset 48h" on page 1816	00000000h
50h	4	"reg_DSR_type (DSR0)—Offset 50h" on page 1817	00000000h
58h	4	"reg_SAR_type (SAR1)—Offset 58h" on page 1818	00000000h
60h	4	"reg_DAR_type (DAR1)—Offset 60h" on page 1818	00000000h
68h	4	"reg_LLP_type (LLP1)—Offset 68h" on page 1819	00000000h
70h	4	"reg_CTL_LO_type (CTL_LO1)—Offset 70h" on page 1820	00000000h
74h	4	"reg_CTL_HI_type (CTL_HI1)—Offset 74h" on page 1822	00000000h
78h	4	"reg_SSTAT_type (SSTAT1)—Offset 78h" on page 1823	00000000h
80h	4	"reg_DSTAT_type (DSTAT1)—Offset 80h" on page 1824	00000000h
88h	4	"reg_SSTATAR_type (SSTATAR1)—Offset 88h" on page 1824	00000000h
90h	4	"reg_DSTATAR_type (DSTATAR1)—Offset 90h" on page 1825	00000000h
98h	4	"reg_CFG_LO_type (CFG_LO1)—Offset 98h" on page 1825	00000203h
9Ch	4	"reg_CFG_HI_type (CFG_HI1)—Offset 9Ch" on page 1827	00000000h
A0h	4	"reg_SGR_type (SGR1)—Offset A0h" on page 1829	00000000h
A8h	4	"reg_DSR_type (DSR1)—Offset A8h" on page 1829	00000000h
B0h	4	"reg_SAR_type (SAR2)—Offset B0h" on page 1830	00000000h
B8h	4	"reg_DAR_type (DAR2)—Offset B8h" on page 1831	00000000h
C0h	4	"reg_LLP_type (LLP2)—Offset C0h" on page 1832	00000000h
C8h	4	"reg_CTL_LO_type (CTL_LO2)—Offset C8h" on page 1833	00000000h
CCh	4	"reg_CTL_HI_type (CTL_HI2)—Offset CCh" on page 1834	00000000h
D0h	4	"reg_SSTAT_type (SSTAT2)—Offset D0h" on page 1836	00000000h

Table 29. Summary of Low Power Audio DMA0 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
D8h	4	"reg_DSTAT_type (DSTAT2)—Offset D8h" on page 1836	00000000h
E0h	4	"reg_SSTATAR_type (SSTATAR2)—Offset E0h" on page 1837	00000000h
E8h	4	"reg_DSTATAR_type (DSTATAR2)—Offset E8h" on page 1837	00000000h
F0h	4	"reg_CFG_LO_type (CFG_LO2)—Offset F0h" on page 1838	00000203h
F4h	4	"reg_CFG_HI_type (CFG_HI2)—Offset F4h" on page 1840	00000000h
F8h	4	"reg_SGR_type (SGR2)—Offset F8h" on page 1841	00000000h
100h	4	"reg_DSR_type (DSR2)—Offset 100h" on page 1842	00000000h
108h	4	"reg_SAR_type (SAR3)—Offset 108h" on page 1843	00000000h
110h	4	"reg_DAR_type (DAR3)—Offset 110h" on page 1843	00000000h
118h	4	"reg_LLP_type (LLP3)—Offset 118h" on page 1844	00000000h
120h	4	"reg_CTL_LO_type (CTL_LO3)—Offset 120h" on page 1845	00000000h
124h	4	"reg_CTL_HI_type (CTL_HI3)—Offset 124h" on page 1847	00000000h
128h	4	"reg_SSTAT_type (SSTAT3)—Offset 128h" on page 1848	00000000h
130h	4	"reg_DSTAT_type (DSTAT3)—Offset 130h" on page 1849	00000000h
138h	4	"reg_SSTATAR_type (SSTATAR3)—Offset 138h" on page 1849	00000000h
140h	4	"reg_DSTATAR_type (DSTATAR3)—Offset 140h" on page 1850	00000000h
148h	4	"reg_CFG_LO_type (CFG_LO3)—Offset 148h" on page 1850	00000203h
14Ch	4	"reg_CFG_HI_type (CFG_HI3)—Offset 14Ch" on page 1852	00000000h
150h	4	"reg_SGR_type (SGR3)—Offset 150h" on page 1854	00000000h
158h	4	"reg_DSR_type (DSR3)—Offset 158h" on page 1854	00000000h
160h	4	"reg_SAR_type (SAR4)—Offset 160h" on page 1855	00000000h
168h	4	"reg_DAR_type (DAR4)—Offset 168h" on page 1856	00000000h
170h	4	"reg_LLP_type (LLP4)—Offset 170h" on page 1857	00000000h
178h	4	"reg_CTL_LO_type (CTL_LO4)—Offset 178h" on page 1858	00000000h
17Ch	4	"reg_CTL_HI_type (CTL_HI4)—Offset 17Ch" on page 1859	00000000h
180h	4	"reg_SSTAT_type (SSTAT4)—Offset 180h" on page 1861	00000000h
188h	4	"reg_DSTAT_type (DSTAT4)—Offset 188h" on page 1861	00000000h
190h	4	"reg_SSTATAR_type (SSTATAR4)—Offset 190h" on page 1862	00000000h
198h	4	"reg_DSTATAR_type (DSTATAR4)—Offset 198h" on page 1862	00000000h
1A0h	4	"reg_CFG_LO_type (CFG_LO4)—Offset 1A0h" on page 1863	00000203h
1A4h	4	"reg_CFG_HI_type (CFG_HI4)—Offset 1A4h" on page 1865	00000000h
1A8h	4	"reg_SGR_type (SGR4)—Offset 1A8h" on page 1866	00000000h
1B0h	4	"reg_DSR_type (DSR4)—Offset 1B0h" on page 1867	00000000h
1B8h	4	"reg_SAR_type (SAR5)—Offset 1B8h" on page 1868	00000000h
1C0h	4	"reg_DAR_type (DAR5)—Offset 1C0h" on page 1868	00000000h

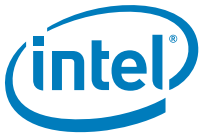


Table 29. Summary of Low Power Audio DMA0 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
1C8h	4	"reg_LLP_type (LLP5)—Offset 1C8h" on page 1869	00000000h
1D0h	4	"reg_CTL_LO_type (CTL_LO5)—Offset 1D0h" on page 1870	00000000h
1D4h	4	"reg_CTL_HI_type (CTL_HI5)—Offset 1D4h" on page 1872	00000000h
1D8h	4	"reg_SSTAT_type (SSTAT5)—Offset 1D8h" on page 1873	00000000h
1E0h	4	"reg_DSTAT_type (DSTAT5)—Offset 1E0h" on page 1874	00000000h
1E8h	4	"reg_SSTATAR_type (SSTATAR5)—Offset 1E8h" on page 1874	00000000h
1F0h	4	"reg_DSTATAR_type (DSTATAR5)—Offset 1F0h" on page 1875	00000000h
1F8h	4	"reg_CFG_LO_type (CFG_LO5)—Offset 1F8h" on page 1875	00000203h
1FCh	4	"reg_CFG_HI_type (CFG_HI5)—Offset 1FCh" on page 1877	00000000h
200h	4	"reg_SGR_type (SGR5)—Offset 200h" on page 1879	00000000h
208h	4	"reg_DSR_type (DSR5)—Offset 208h" on page 1879	00000000h
210h	4	"reg_SAR_type (SAR6)—Offset 210h" on page 1880	00000000h
218h	4	"reg_DAR_type (DAR6)—Offset 218h" on page 1881	00000000h
220h	4	"reg_LLP_type (LLP6)—Offset 220h" on page 1882	00000000h
228h	4	"reg_CTL_LO_type (CTL_LO6)—Offset 228h" on page 1883	00000000h
22Ch	4	"reg_CTL_HI_type (CTL_HI6)—Offset 22Ch" on page 1884	00000000h
230h	4	"reg_SSTAT_type (SSTAT6)—Offset 230h" on page 1886	00000000h
238h	4	"reg_DSTAT_type (DSTAT6)—Offset 238h" on page 1886	00000000h
240h	4	"reg_SSTATAR_type (SSTATAR6)—Offset 240h" on page 1887	00000000h
248h	4	"reg_DSTATAR_type (DSTATAR6)—Offset 248h" on page 1887	00000000h
250h	4	"reg_CFG_LO_type (CFG_LO6)—Offset 250h" on page 1888	00000203h
254h	4	"reg_CFG_HI_type (CFG_HI6)—Offset 254h" on page 1890	00000000h
258h	4	"reg_SGR_type (SGR6)—Offset 258h" on page 1891	00000000h
260h	4	"reg_DSR_type (DSR6)—Offset 260h" on page 1892	00000000h
268h	4	"reg_SAR_type (SAR7)—Offset 268h" on page 1893	00000000h
270h	4	"reg_DAR_type (DAR7)—Offset 270h" on page 1893	00000000h
278h	4	"reg_LLP_type (LLP7)—Offset 278h" on page 1894	00000000h
280h	4	"reg_CTL_LO_type (CTL_LO7)—Offset 280h" on page 1895	00000000h
284h	4	"reg_CTL_HI_type (CTL_HI7)—Offset 284h" on page 1897	00000000h
288h	4	"reg_SSTAT_type (SSTAT7)—Offset 288h" on page 1898	00000000h
290h	4	"reg_DSTAT_type (DSTAT7)—Offset 290h" on page 1899	00000000h
298h	4	"reg_SSTATAR_type (SSTATAR7)—Offset 298h" on page 1899	00000000h
2A0h	4	"reg_DSTATAR_type (DSTATAR7)—Offset 2A0h" on page 1900	00000000h
2A8h	4	"reg_CFG_LO_type (CFG_LO7)—Offset 2A8h" on page 1900	00000203h
2ACh	4	"reg_CFG_HI_type (CFG_HI7)—Offset 2ACh" on page 1902	00000000h

Table 29. Summary of Low Power Audio DMA0 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
2B0h	4	"reg_SGR_type (SGR7)—Offset 2B0h" on page 1904	00000000h
2B8h	4	"reg_DSR_type (DSR7)—Offset 2B8h" on page 1904	00000000h
2C0h	4	"reg_Raw_type (RawTfr)—Offset 2C0h" on page 1905	00000000h
2C8h	4	"reg_Raw_type (RawBlock)—Offset 2C8h" on page 1906	00000000h
2D0h	4	"reg_Raw_type (RawSrcTran)—Offset 2D0h" on page 1906	00000000h
2D8h	4	"reg_Raw_type (RawDstTran)—Offset 2D8h" on page 1907	00000000h
2E0h	4	"reg_Raw_type (RawErr)—Offset 2E0h" on page 1908	00000000h
2E8h	4	"reg_Status_type (StatusTfr)—Offset 2E8h" on page 1908	00000000h
2F0h	4	"reg_Status_type (StatusBlock)—Offset 2F0h" on page 1909	00000000h
2F8h	4	"reg_Status_type (StatusSrcTran)—Offset 2F8h" on page 1910	00000000h
300h	4	"reg_Status_type (StatusDstTran)—Offset 300h" on page 1910	00000000h
308h	4	"reg_Status_type (StatusErr)—Offset 308h" on page 1911	00000000h
310h	4	"reg_Mask_type (MaskTfr)—Offset 310h" on page 1911	00000000h
318h	4	"reg_Mask_type (MaskBlock)—Offset 318h" on page 1912	00000000h
320h	4	"reg_Mask_type (MaskSrcTran)—Offset 320h" on page 1913	00000000h
328h	4	"reg_Mask_type (MaskDstTran)—Offset 328h" on page 1914	00000000h
330h	4	"reg_Mask_type (MaskErr)—Offset 330h" on page 1915	00000000h
338h	4	"reg_Clear_type (ClearTfr)—Offset 338h" on page 1916	00000000h
340h	4	"reg_Clear_type (ClearBlock)—Offset 340h" on page 1917	00000000h
348h	4	"reg_Clear_type (ClearSrcTran)—Offset 348h" on page 1917	00000000h
350h	4	"reg_Clear_type (ClearDstTran)—Offset 350h" on page 1918	00000000h
358h	4	"reg_Clear_type (ClearErr)—Offset 358h" on page 1918	00000000h
360h	4	"reg_StatusInt_type (StatusInt)—Offset 360h" on page 1919	00000000h
398h	4	"reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h" on page 1920	00000000h
3A0h	4	"reg_ChEnReg_type (ChEnReg)—Offset 3A0h" on page 1920	00000000h
3B8h	4	"reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h" on page 1921	00000000h
3BCh	4	"reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh" on page 1922	00000000h
3C0h	4	"reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h" on page 1922	00000000h
3C4h	4	"reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h" on page 1923	00000000h
400h	4	"reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h" on page 1924	00000000h
404h	4	"reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h" on page 1924	00000000h

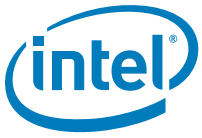


Table 29. Summary of Low Power Audio DMA0 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
408h	4	"reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h" on page 1925	00000000h
40Ch	4	"reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch" on page 1926	00000000h
410h	4	"reg_SAI_Error_type (SAI_ERR)—Offset 410h" on page 1926	00000000h
418h	4	"reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h" on page 1927	00000000h

3.21.1 reg_SAR_type (SAR0)—Offset 0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

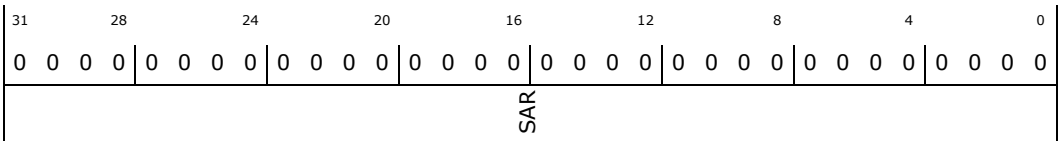
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR0: [BAR + 98000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.2 reg_DAR_type (DAR0)—Offset 8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

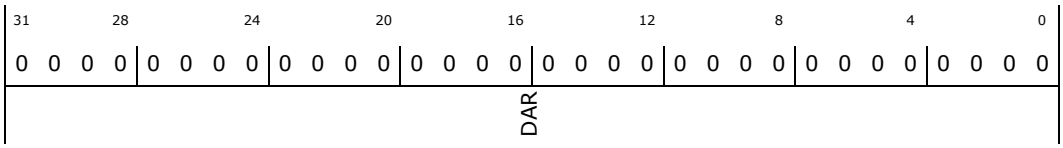
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR0: [BAR + 98000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.3 reg_LLP_type (LLP0)—Offset 10h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

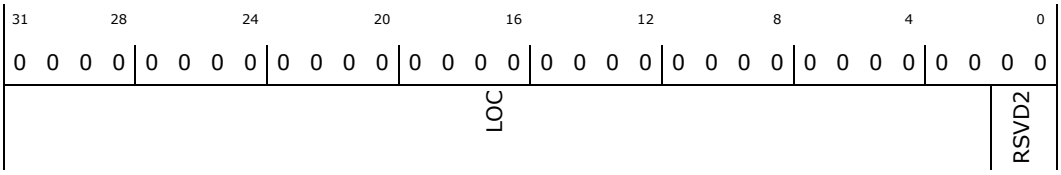
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP0: [BAR + 98000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.21.4 reg_CTL_LO_type (CTL_LO0)—Offset 18h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

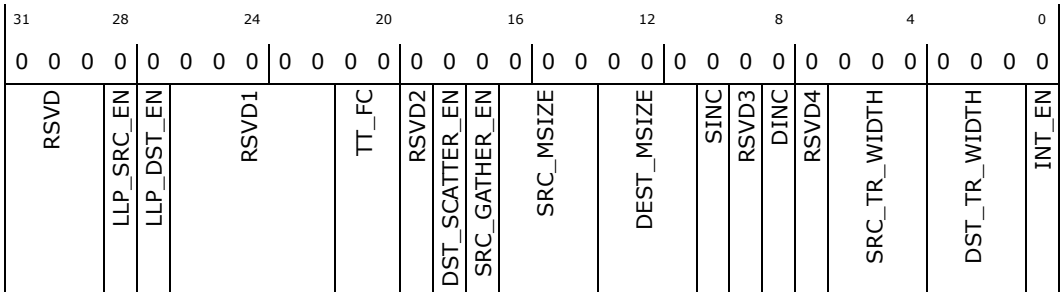
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

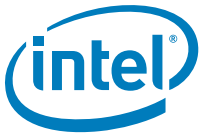
CTL_LO0: [BAR + 98000h] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved



Bit Range	Default & Access	Description
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.21.5 reg_CTL_HI_type (CTL_HI0)—Offset 1Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

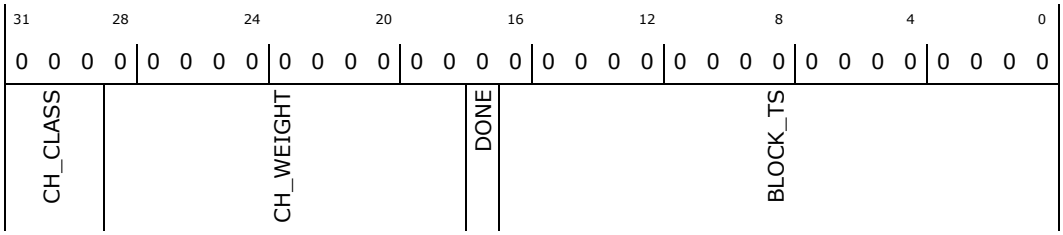
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI0: [BAR + 98000h] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.21.6 reg_SSTAT_type (SSTAT0)—Offset 20h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

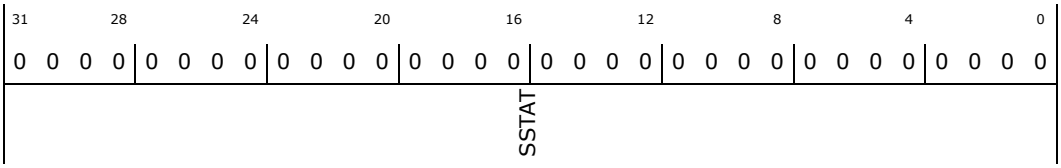
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT0: [BAR + 98000h] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.21.7 reg_DSTAT_type (DSTAT0)—Offset 28h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

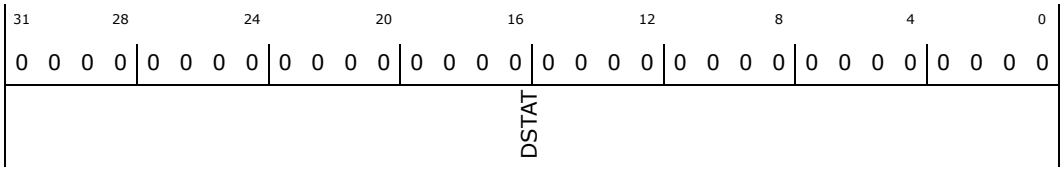
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT0: [BAR + 98000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.21.8 reg_SSTATAR_type (SSTATAR0)—Offset 30h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

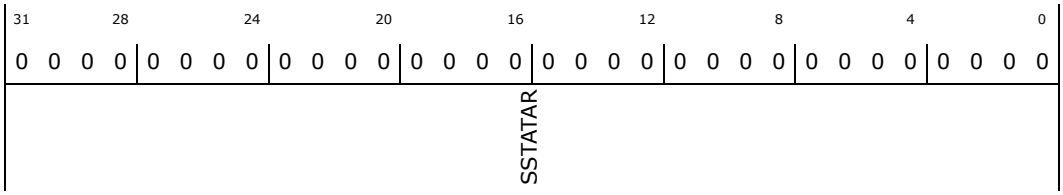
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR0: [BAR + 98000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.21.9 reg_DSTATAR_type (DSTATAR0)—Offset 38h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

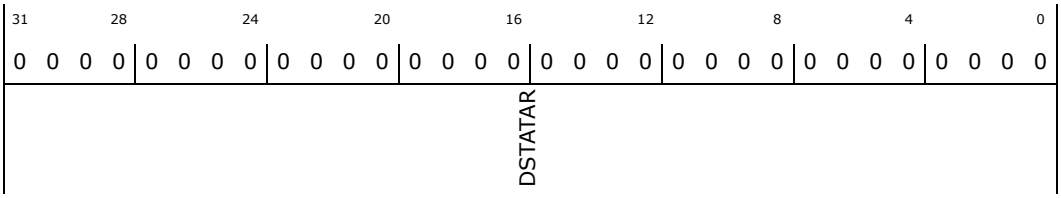
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR0: [BAR + 98000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.21.10 reg_CFG_LO_type (CFG_LO0)—Offset 40h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

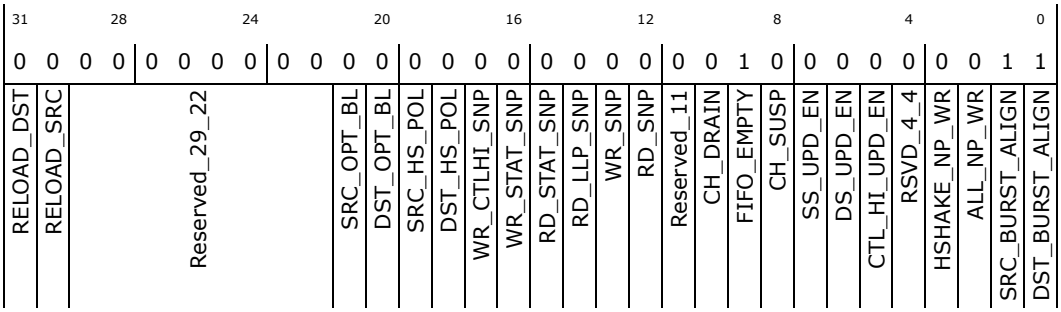
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

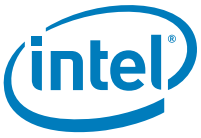
CFG_LO0: [BAR + 98000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.



Bit Range	Default & Access	Description
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.21.11 reg_CFG_HI_type (CFG_HI0)—Offset 44h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

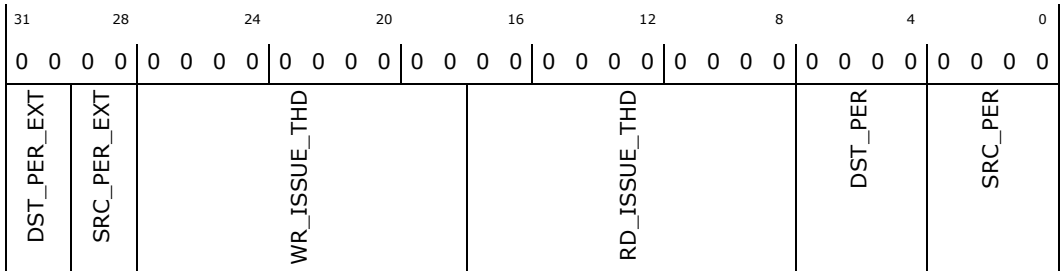
Access Method

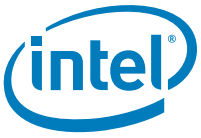
Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI0: [BAR + 98000h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.21.12 reg_SGR_type (SGR0)—Offset 48h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

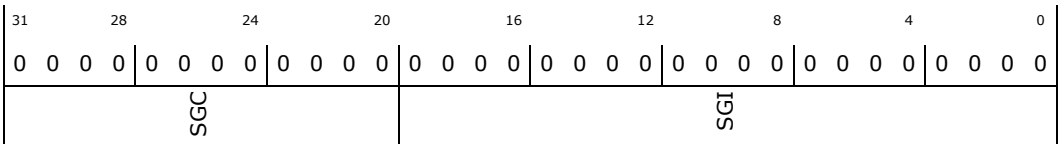
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR0: [BAR + 98000h] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.21.13 reg_DSR_type (DSR0)—Offset 50h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

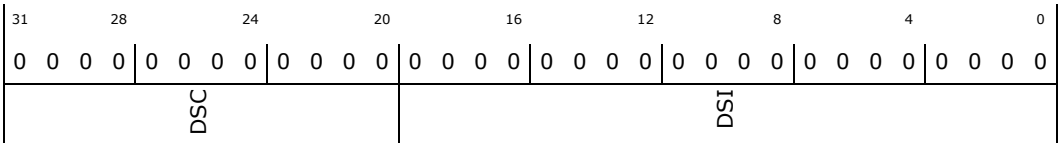
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR0: [BAR + 98000h] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.21.14 reg_SAR_type (SAR1)—Offset 58h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

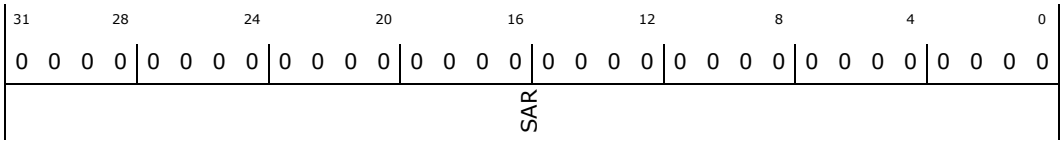
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR1: [BAR + 98000h] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.15 reg_DAR_type (DAR1)—Offset 60h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

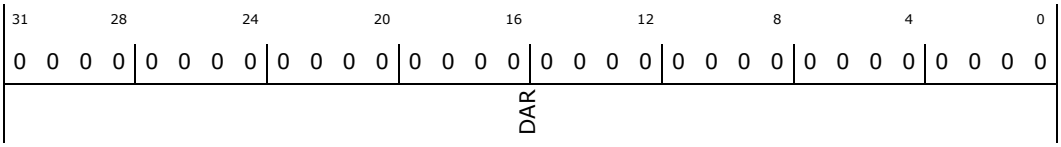
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR1: [BAR + 98000h] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.16 reg_LLP_type (LLP1)—Offset 68h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

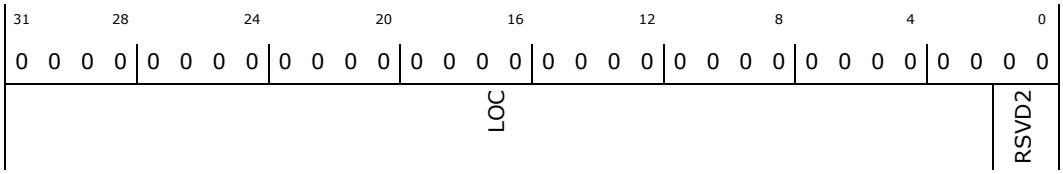
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP1: [BAR + 98000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.21.17 reg_CTL_LO_type (CTL_LO1)—Offset 70h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

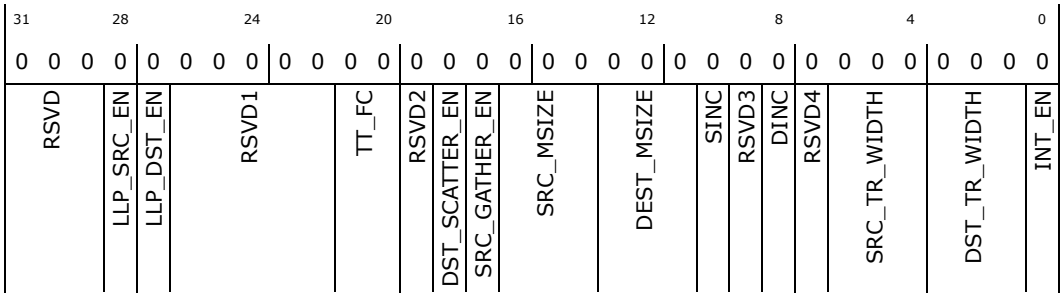
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO1: [BAR + 98000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.

Bit Range	Default & Access	Description
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.21.18 reg_CTL_HI_type (CTL_HI1)—Offset 74h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

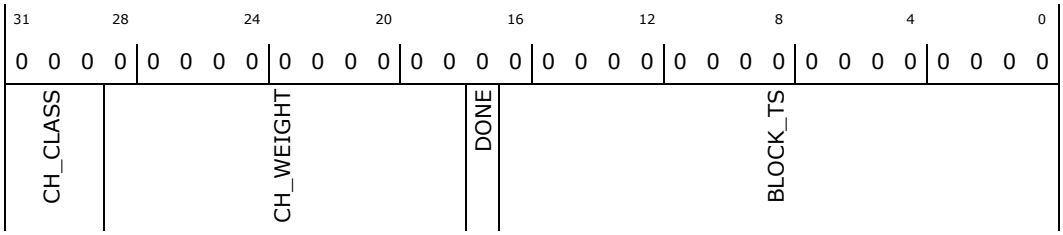
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI1: [BAR + 98000h] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.

Bit Range	Default & Access	Description
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.21.19 reg_SSTAT_type (SSTAT1)—Offset 78h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

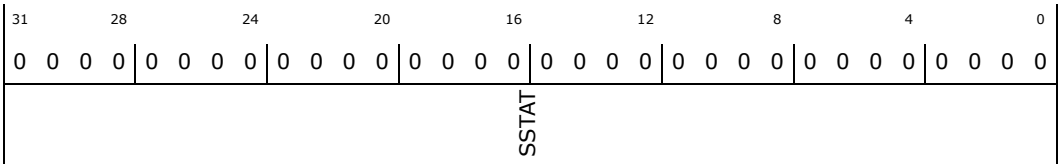
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT1: [BAR + 98000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.21.20 reg_DSTAT_type (DSTAT1)—Offset 80h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

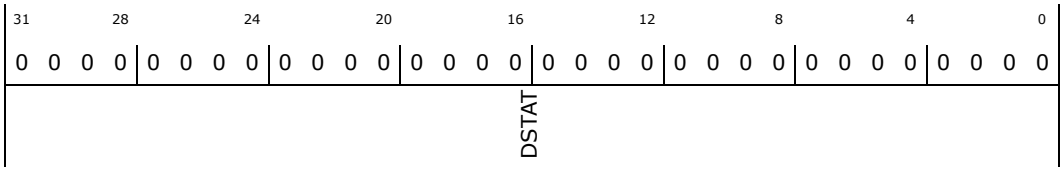
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT1: [BAR + 98000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.21.21 reg_SSTATAR_type (SSTATAR1)—Offset 88h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

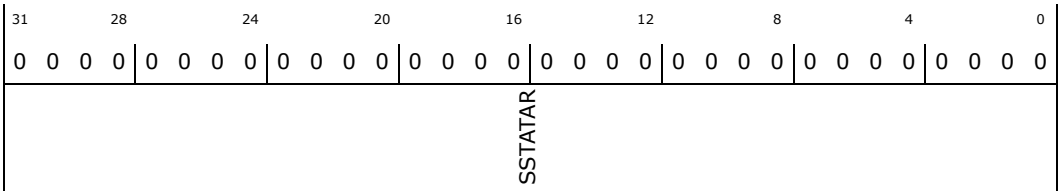
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR1: [BAR + 98000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.21.22 reg_DSTATAR_type (DSTATAR1)—Offset 90h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

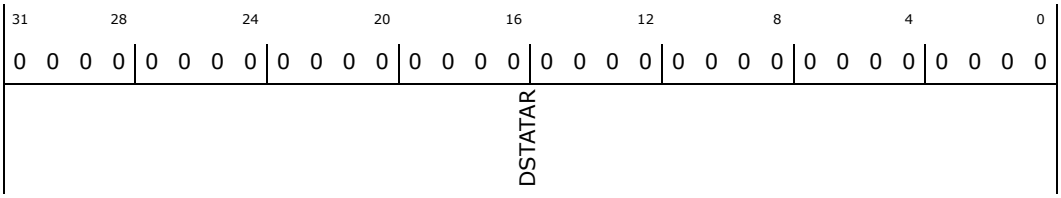
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR1: [BAR + 98000h] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.21.23 reg_CFG_LO_type (CFG_LO1)—Offset 98h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

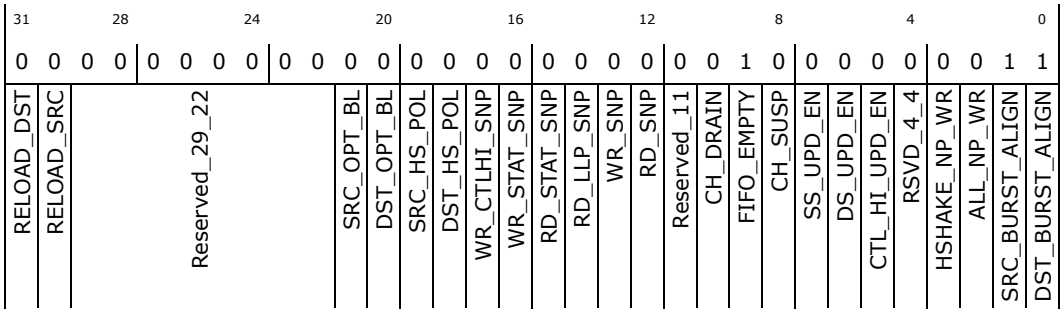
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

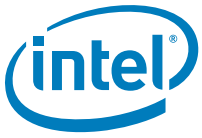
CFG_LO1: [BAR + 98000h] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port



Bit Range	Default & Access	Description
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.21.24 reg_CFG_HI_type (CFG_HI1)—Offset 9Ch

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

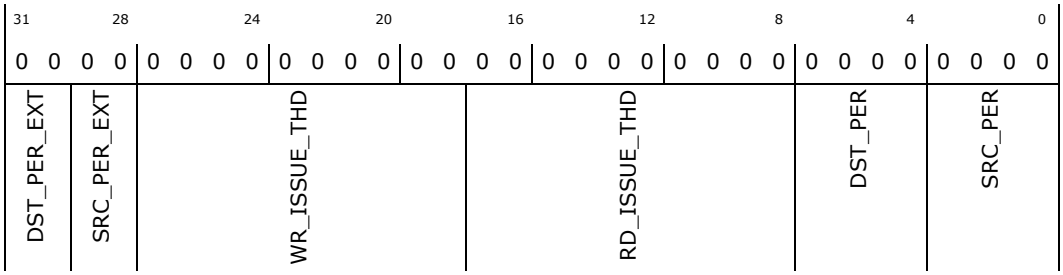
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI1: [BAR + 98000h] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.21.25 reg_SGR_type (SGR1)—Offset A0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

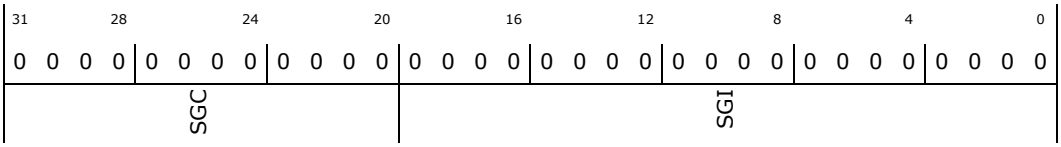
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR1: [BAR + 98000h] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.21.26 reg_DSR_type (DSR1)—Offset A8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

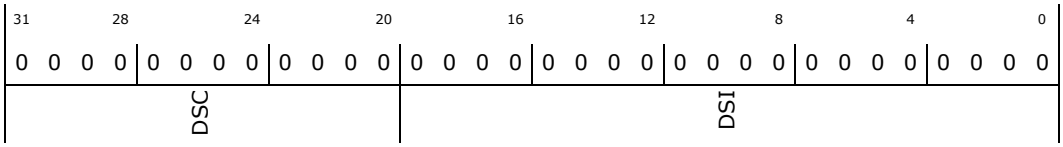
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR1: [BAR + 98000h] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.21.27 reg_SAR_type (SAR2)—Offset B0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

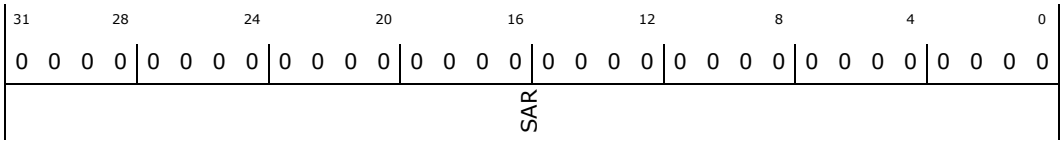
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR2: [BAR + 98000h] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.28 reg_DAR_type (DAR2)—Offset B8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

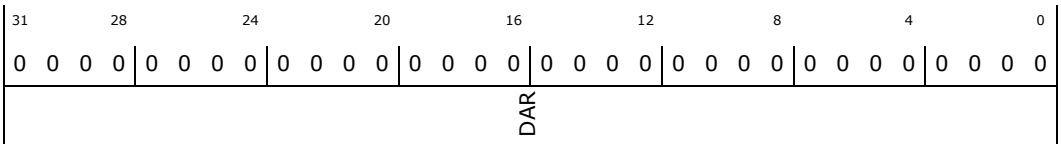
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR2: [BAR + 98000h] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.29 reg_LLP_type (LLP2)—Offset C0h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

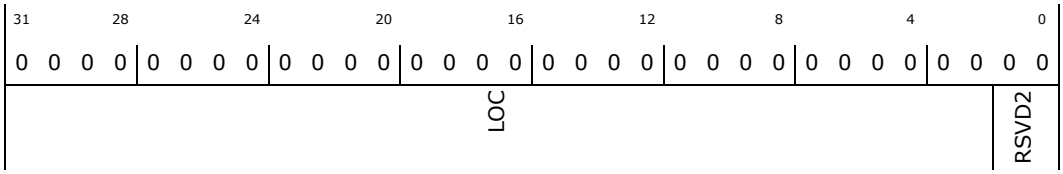
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP2: [BAR + 98000h] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.21.30 reg_CTL_LO_type (CTL_LO2)—Offset C8h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

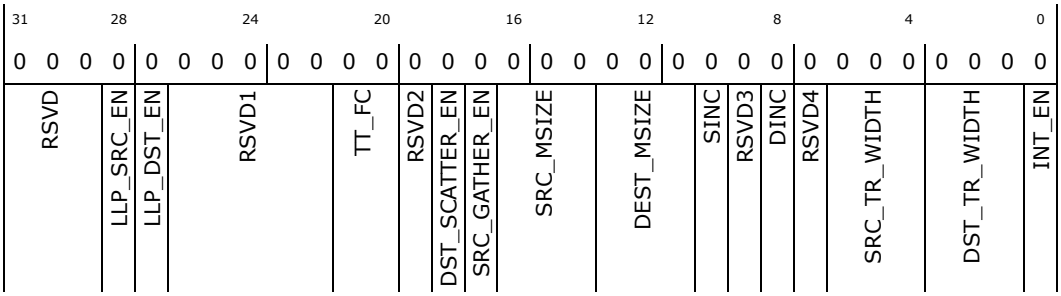
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO2: [BAR + 98000h] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved

Bit Range	Default & Access	Description
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.21.31 reg_CTL_HI_type (CTL_HI2)—Offset CCh

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

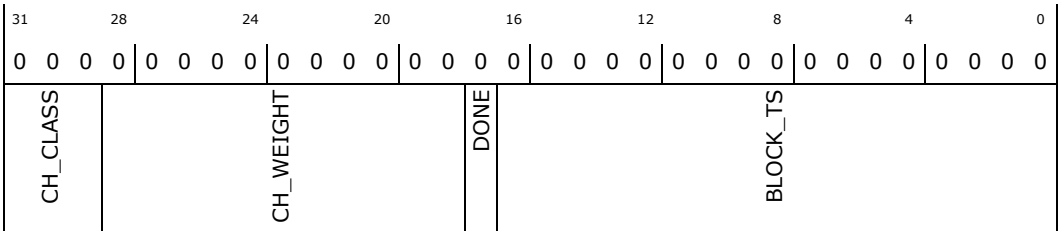
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI2: [BAR + 98000h] + CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.21.32 reg_SSTAT_type (SSTAT2)—Offset D0h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

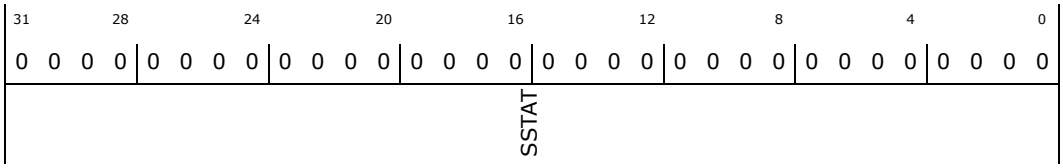
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT2: [BAR + 98000h] + D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.21.33 reg_DSTAT_type (DSTAT2)—Offset D8h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

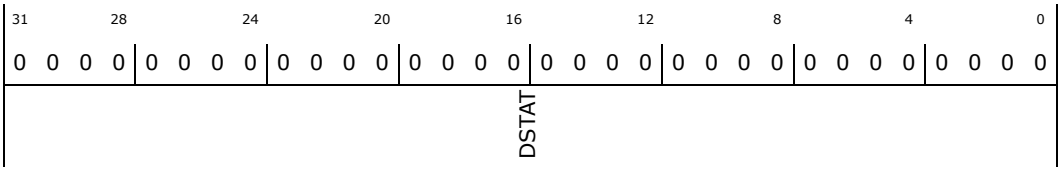
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT2: [BAR + 98000h] + D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.21.34 reg_SSTATAR_type (SSTATAR2)—Offset E0h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

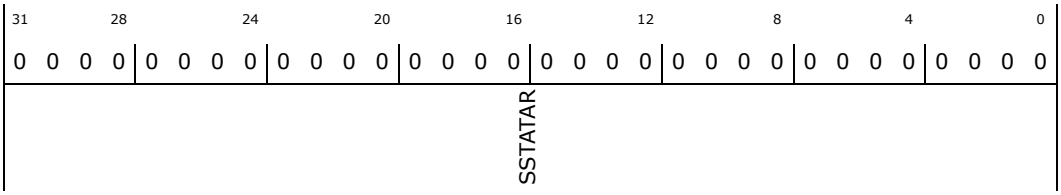
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR2: [BAR + 98000h] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.21.35 reg_DSTATAR_type (DSTATAR2)—Offset E8h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

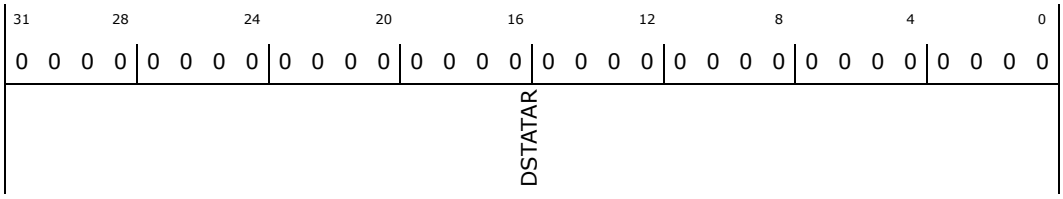
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR2: [BAR + 98000h] + E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.21.36 reg_CFG_LO_type (CFG_LO2)—Offset F0h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

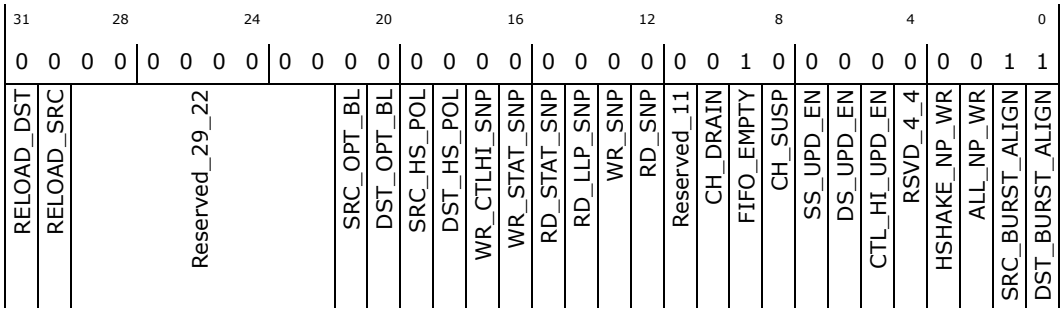
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO2: [BAR + 98000h] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.

Bit Range	Default & Access	Description
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.21.37 reg_CFG_HI_type (CFG_HI2)—Offset F4h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

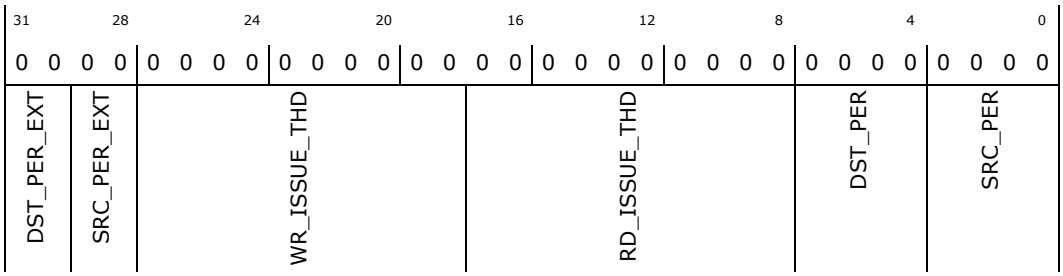
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI2: [BAR + 98000h] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.21.38 reg_SGR_type (SGR2)—Offset F8h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

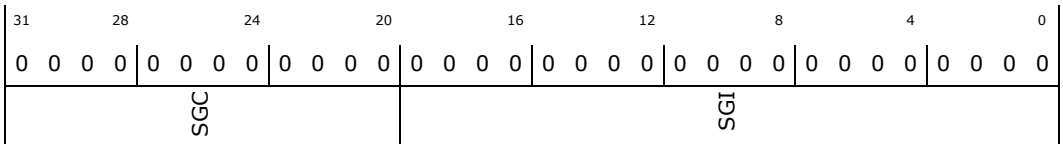
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR2: [BAR + 98000h] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.21.39 reg_DSR_type (DSR2)—Offset 100h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

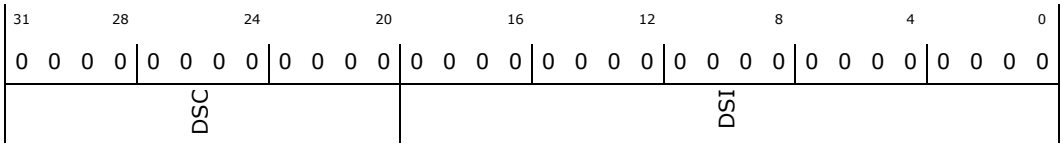
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR2: [BAR + 98000h] + 100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.21.40 reg_SAR_type (SAR3)—Offset 108h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

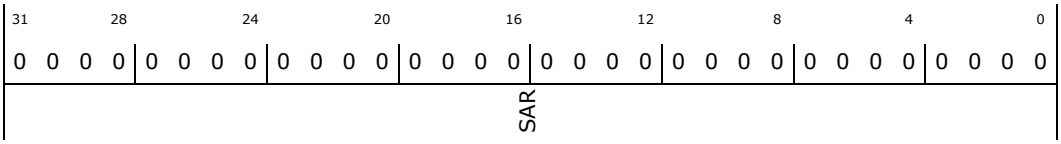
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR3: [BAR + 98000h] + 108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.41 reg_DAR_type (DAR3)—Offset 110h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

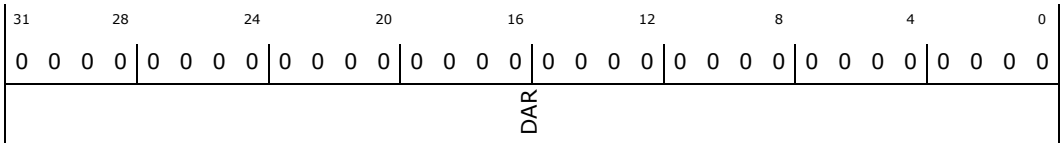
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR3: [BAR + 98000h] + 110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.42 reg_LLP_type (LLP3)—Offset 118h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

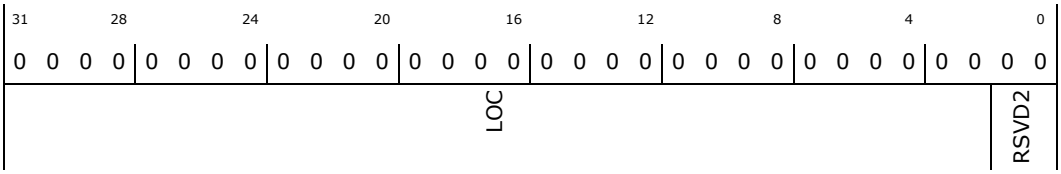
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP3: [BAR + 98000h] + 118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.21.43 reg_CTL_LO_type (CTL_LO3)—Offset 120h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

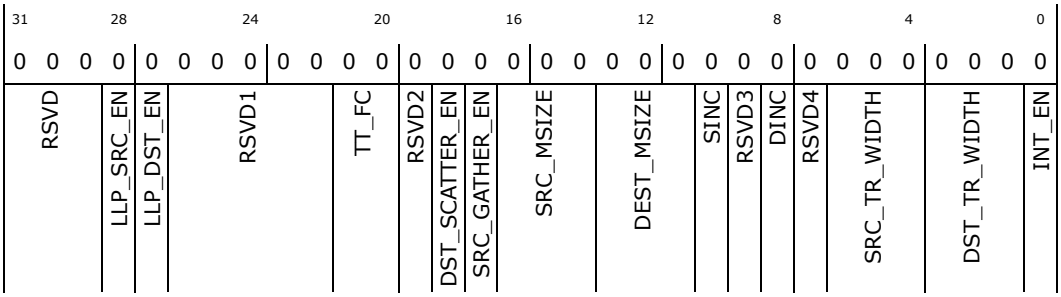
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

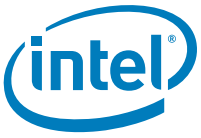
CTL_LO3: [BAR + 98000h] + 120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved



Bit Range	Default & Access	Description
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.

Bit Range	Default & Access	Description
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.21.44 reg_CTL_HI_type (CTL_HI3)—Offset 124h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

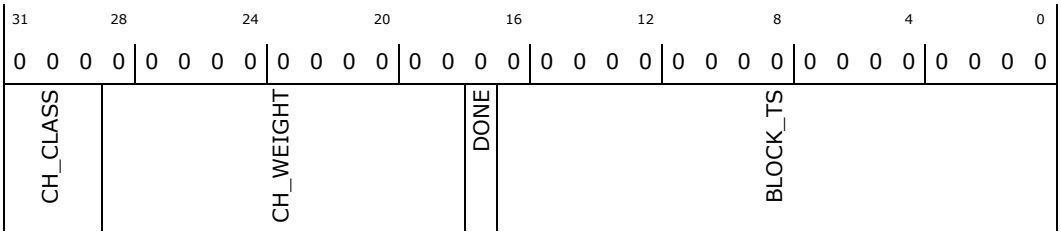
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI3: [BAR + 98000h] + 124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.

Bit Range	Default & Access	Description
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.21.45 reg_SSTAT_type (SSTAT3)—Offset 128h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

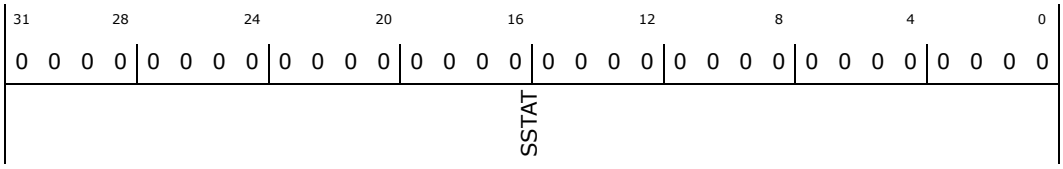
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT3: [BAR + 98000h] + 128h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.21.46 reg_DSTAT_type (DSTAT3)—Offset 130h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

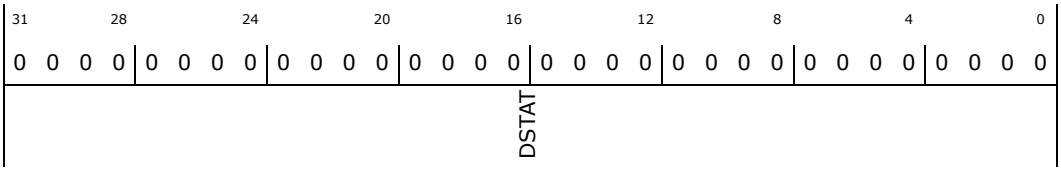
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT3: [BAR + 98000h] + 130h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.21.47 reg_SSTATAR_type (SSTATAR3)—Offset 138h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

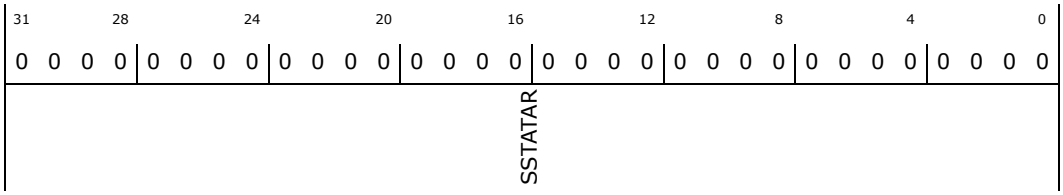
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR3: [BAR + 98000h] + 138h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.21.48 reg_DSTATAR_type (DSTATAR3)—Offset 140h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

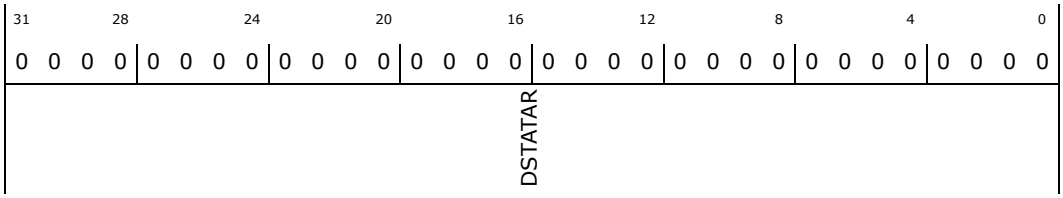
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR3: [BAR + 98000h] + 140h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.21.49 reg_CFG_LO_type (CFG_LO3)—Offset 148h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

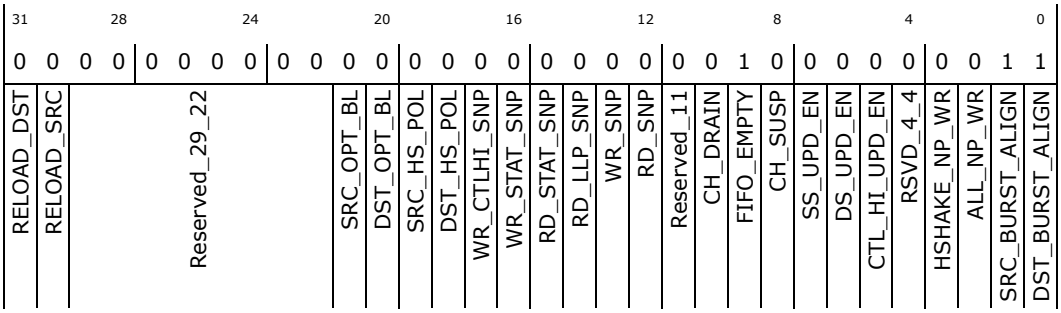
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO3: [BAR + 98000h] + 148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port

Bit Range	Default & Access	Description
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.21.50 reg_CFG_HI_type (CFG_HI3)—Offset 14Ch

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

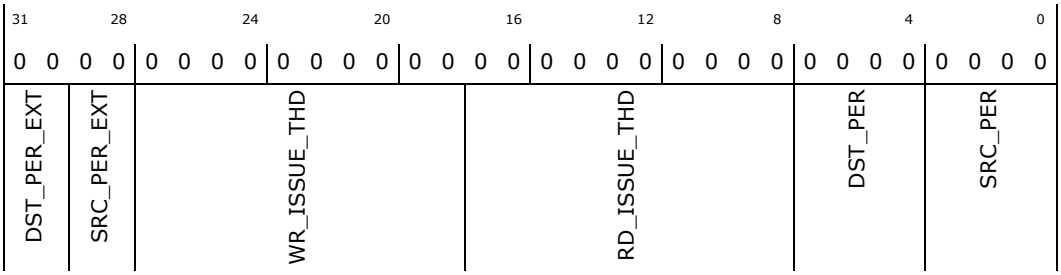
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI3: [BAR + 98000h] + 14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.21.51 reg_SGR_type (SGR3)—Offset 150h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

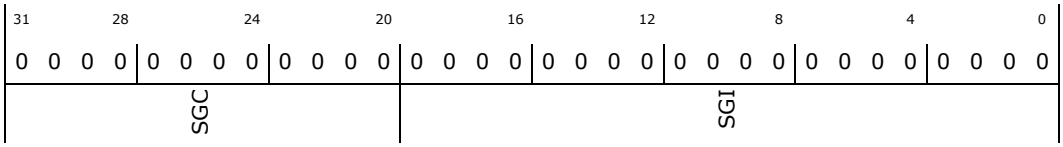
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR3: [BAR + 98000h] + 150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.21.52 reg_DSR_type (DSR3)—Offset 158h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

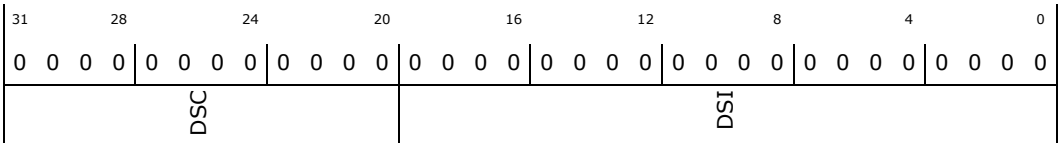
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR3: [BAR + 98000h] + 158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.21.53 reg_SAR_type (SAR4)—Offset 160h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

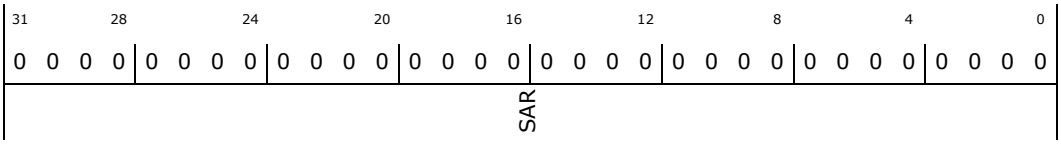
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR4: [BAR + 98000h] + 160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.54 reg_DAR_type (DAR4)—Offset 168h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

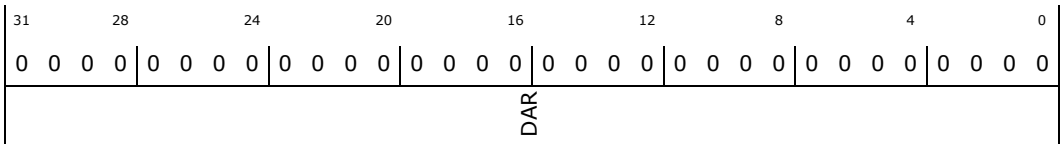
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR4: [BAR + 98000h] + 168h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.55 reg_LLP_type (LLP4)—Offset 170h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

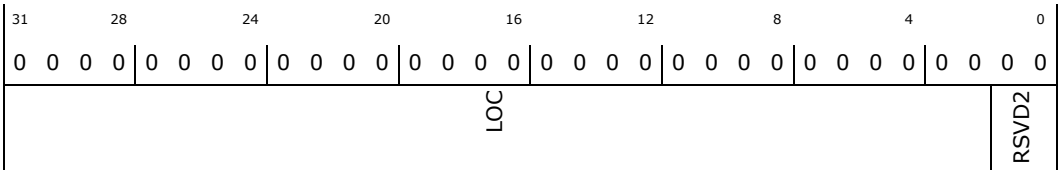
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP4: [BAR + 98000h] + 170h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.21.56 reg_CTL_LO_type (CTL_LO4)—Offset 178h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

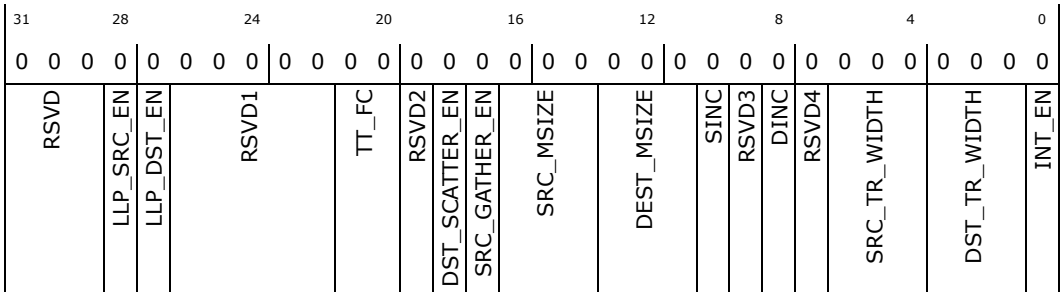
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

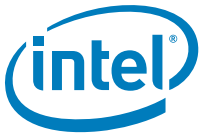
CTL_LO4: [BAR + 98000h] + 178h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved



Bit Range	Default & Access	Description
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.21.57 reg_CTL_HI_type (CTL_HI4)—Offset 17Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

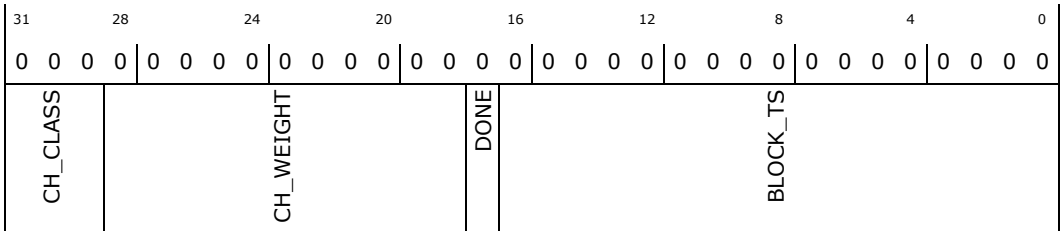
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI4: [BAR + 98000h] + 17Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.21.58 reg_SSTAT_type (SSTAT4)—Offset 180h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

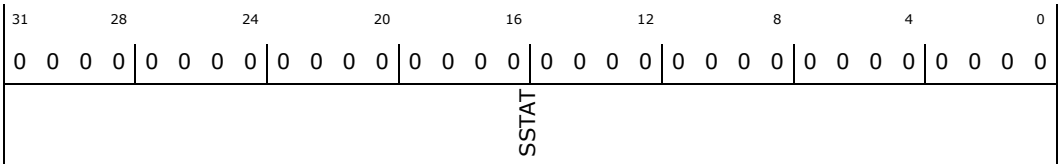
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT4: [BAR + 98000h] + 180h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.21.59 reg_DSTAT_type (DSTAT4)—Offset 188h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

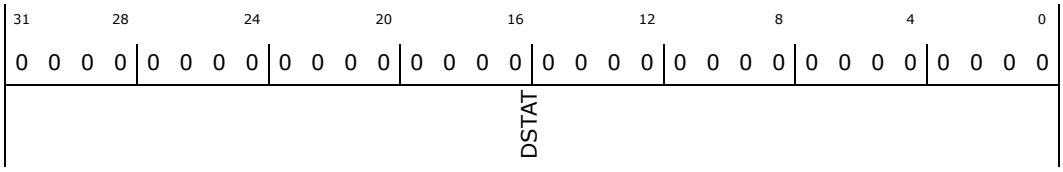
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT4: [BAR + 98000h] + 188h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.21.60 reg_SSTATAR_type (SSTATAR4)—Offset 190h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

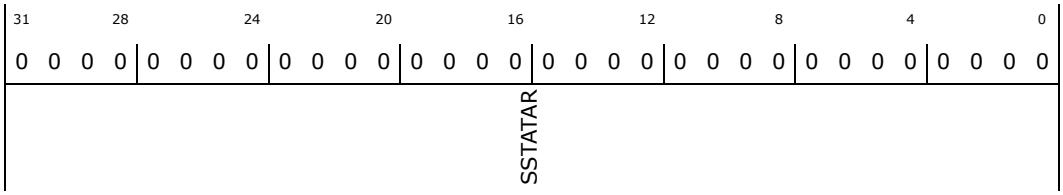
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR4: [BAR + 98000h] + 190h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.21.61 reg_DSTATAR_type (DSTATAR4)—Offset 198h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

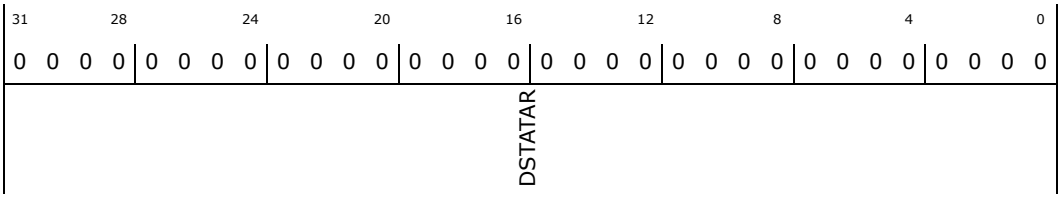
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR4: [BAR + 98000h] + 198h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.21.62 reg_CFG_LO_type (CFG_LO4)—Offset 1A0h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

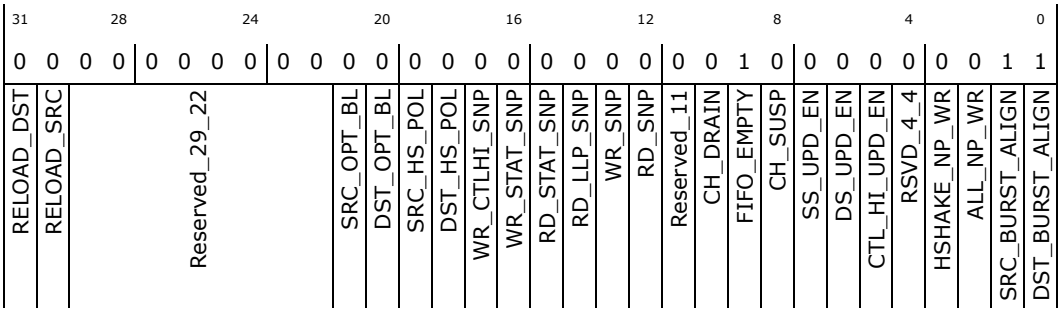
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO4: [BAR + 98000h] + 1A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.

Bit Range	Default & Access	Description
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.21.63 reg_CFG_HI_type (CFG_HI4)—Offset 1A4h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

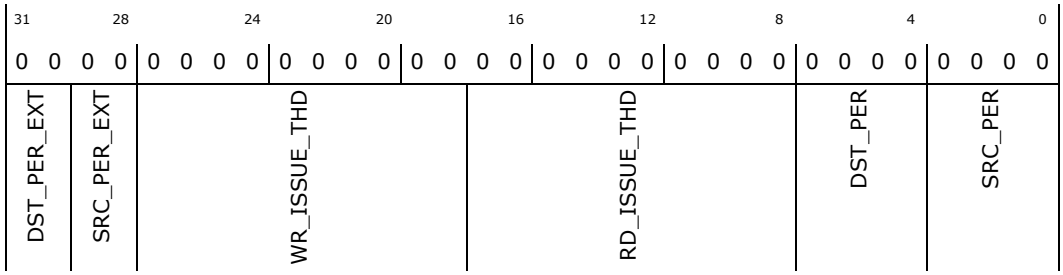
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI4: [BAR + 98000h] + 1A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.21.64 reg_SGR_type (SGR4)—Offset 1A8h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

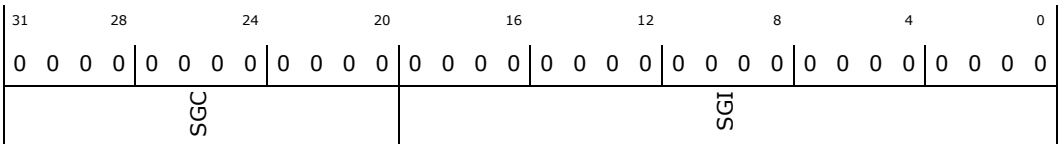
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR4: [BAR + 98000h] + 1A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.21.65 reg_DSR_type (DSR4)—Offset 1B0h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

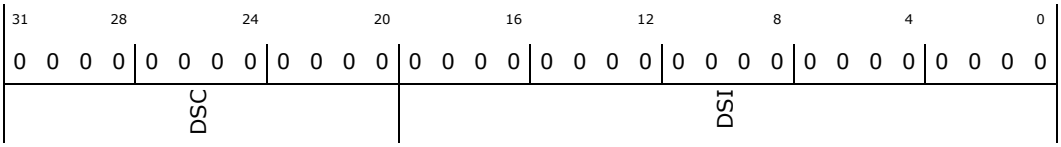
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR4: [BAR + 98000h] + 1B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.21.66 reg_SAR_type (SAR5)—Offset 1B8h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

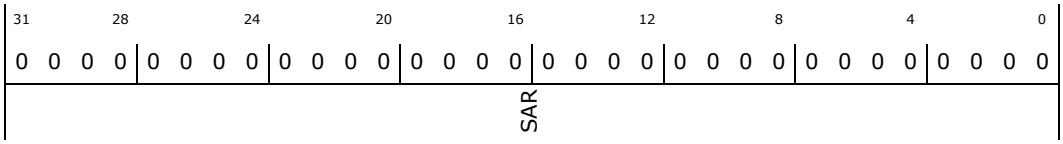
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR5: [BAR + 98000h] + 1B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.67 reg_DAR_type (DAR5)—Offset 1C0h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

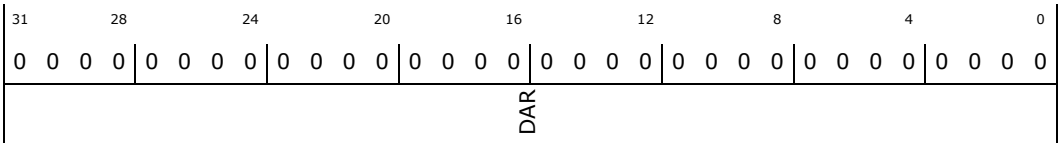
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR5: [BAR + 98000h] + 1C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.68 reg_LLP_type (LLP5)—Offset 1C8h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

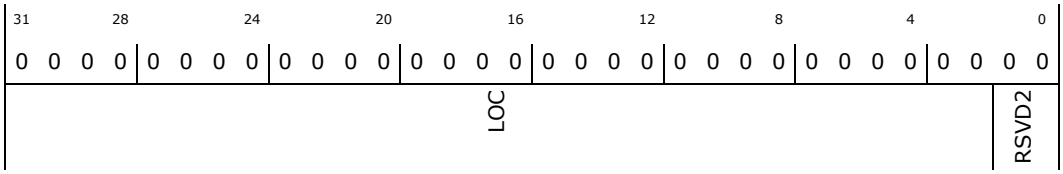
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP5: [BAR + 98000h] + 1C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.21.69 reg_CTL_LO_type (CTL_LO5)—Offset 1D0h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

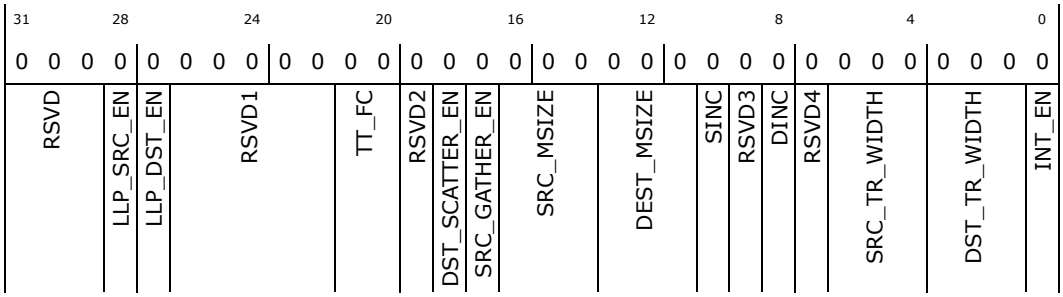
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

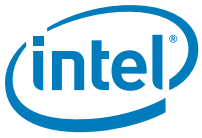
CTL_LO5: [BAR + 98000h] + 1D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved



Bit Range	Default & Access	Description
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.

Bit Range	Default & Access	Description
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.21.70 reg_CTL_HI_type (CTL_HI5)—Offset 1D4h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

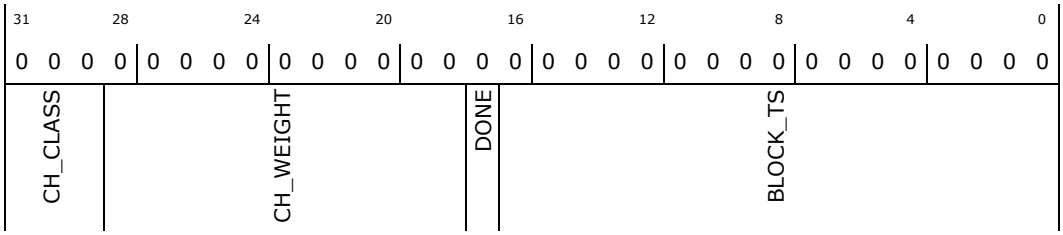
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI5: [BAR + 98000h] + 1D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.

Bit Range	Default & Access	Description
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.21.71 reg_SSTAT_type (SSTAT5)—Offset 1D8h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

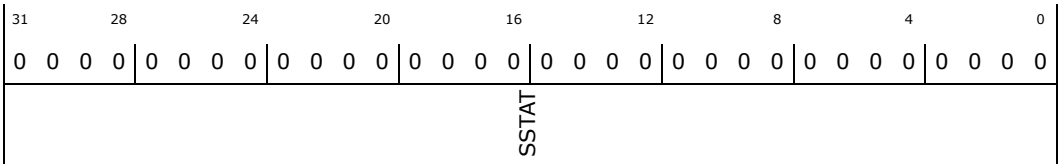
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT5: [BAR + 98000h] + 1D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.21.72 reg_DSTAT_type (DSTAT5)—Offset 1E0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

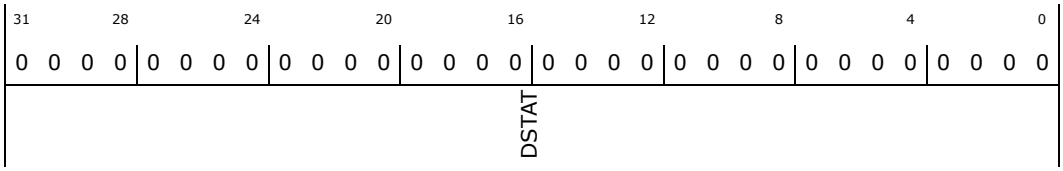
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT5: [BAR + 98000h] + 1E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.21.73 reg_SSTATAR_type (SSTATAR5)—Offset 1E8h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

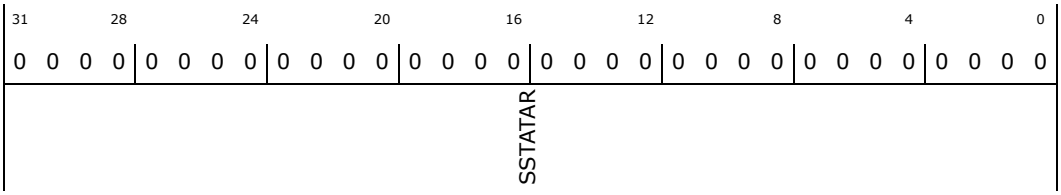
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR5: [BAR + 98000h] + 1E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.21.74 reg_DSTATAR_type (DSTATAR5)—Offset 1F0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

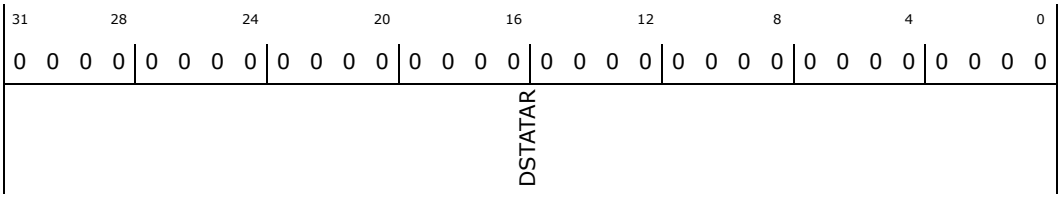
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR5: [BAR + 98000h] + 1F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.21.75 reg_CFG_LO_type (CFG_LO5)—Offset 1F8h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

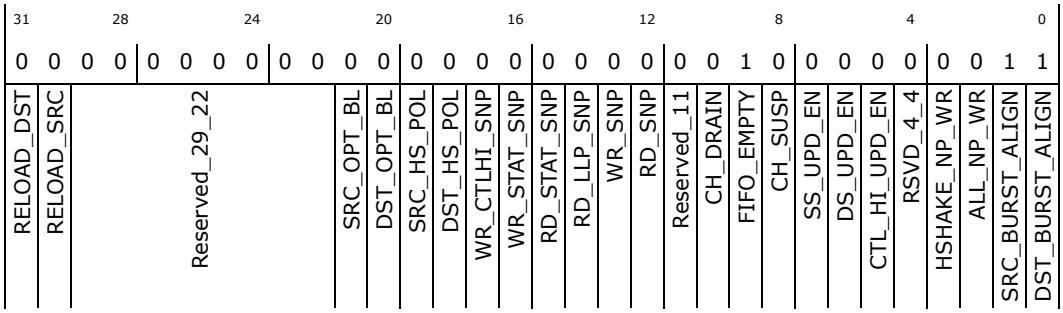
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

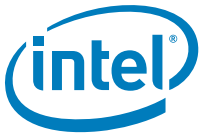
CFG_LO5: [BAR + 98000h] + 1F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port



Bit Range	Default & Access	Description
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.21.76 reg_CFG_HI_type (CFG_HI5)—Offset 1FCh

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

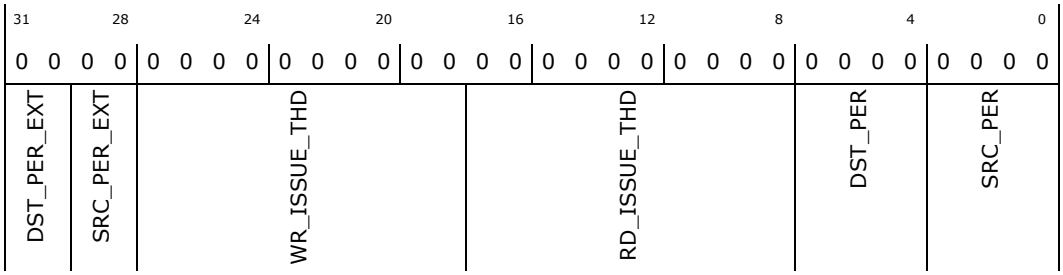
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI5: [BAR + 98000h] + 1FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.21.77 reg_SGR_type (SGR5)—Offset 200h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

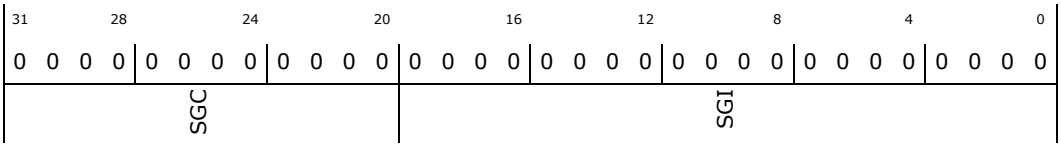
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR5: [BAR + 98000h] + 200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.21.78 reg_DSR_type (DSR5)—Offset 208h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

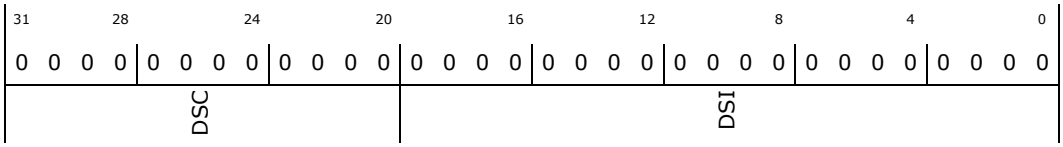
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR5: [BAR + 98000h] + 208h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.21.79 reg_SAR_type (SAR6)—Offset 210h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

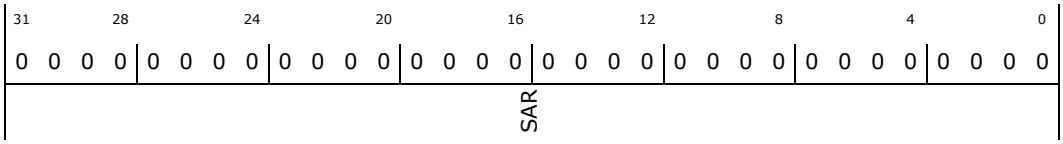
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR6: [BAR + 98000h] + 210h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.80 reg_DAR_type (DAR6)—Offset 218h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

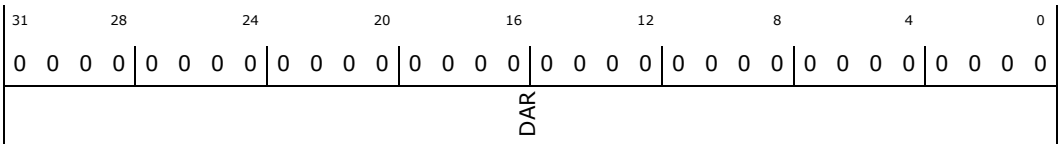
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR6: [BAR + 98000h] + 218h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.81 reg_LLP_type (LLP6)—Offset 220h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

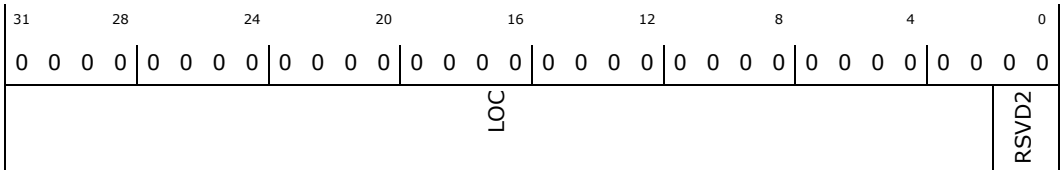
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP6: [BAR + 98000h] + 220h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.21.82 reg_CTL_LO_type (CTL_LO6)—Offset 228h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

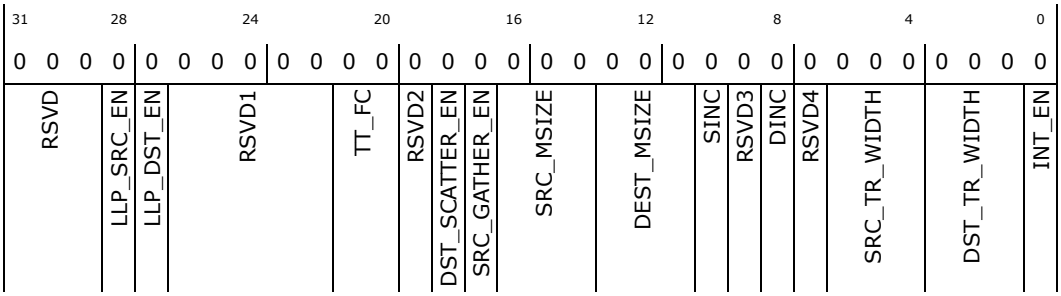
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO6: [BAR + 98000h] + 228h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved

Bit Range	Default & Access	Description
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.21.83 reg_CTL_HI_type (CTL_HI6)—Offset 22Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

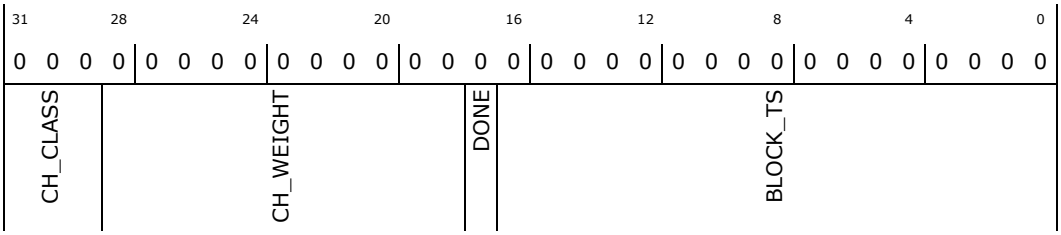
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI6: [BAR + 98000h] + 22Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.21.84 reg_SSTAT_type (SSTAT6)—Offset 230h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

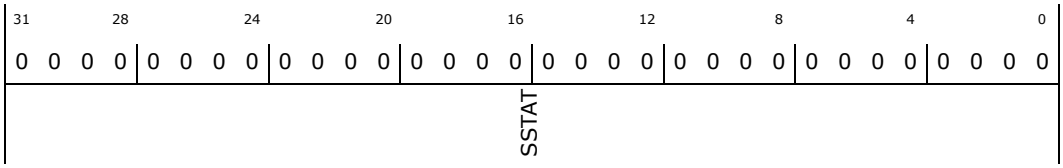
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT6: [BAR + 98000h] + 230h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.21.85 reg_DSTAT_type (DSTAT6)—Offset 238h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

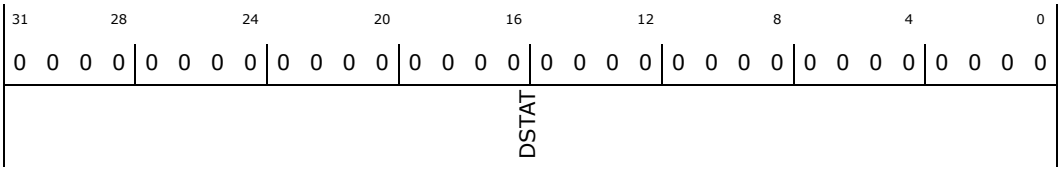
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT6: [BAR + 98000h] + 238h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.21.86 reg_SSTATAR_type (SSTATAR6)—Offset 240h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

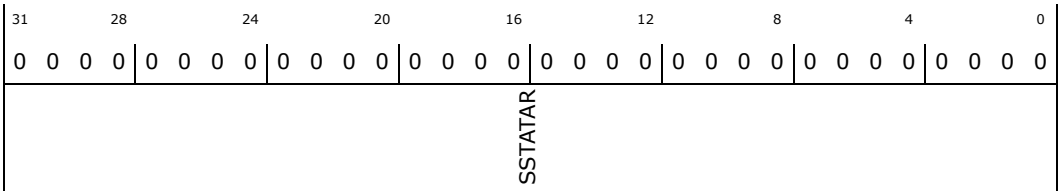
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR6: [BAR + 98000h] + 240h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.21.87 reg_DSTATAR_type (DSTATAR6)—Offset 248h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

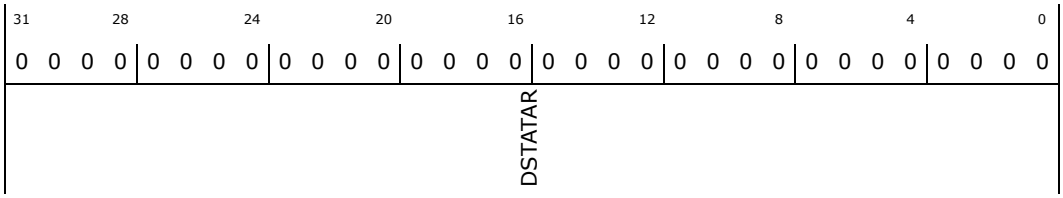
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR6: [BAR + 98000h] + 248h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.21.88 reg_CFG_LO_type (CFG_LO6)—Offset 250h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

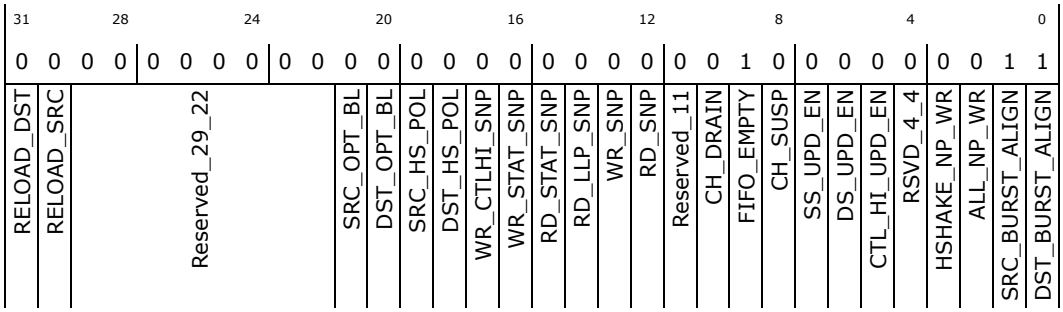
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO6: [BAR + 98000h] + 250h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.

Bit Range	Default & Access	Description
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.21.89 reg_CFG_HI_type (CFG_HI6)—Offset 254h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

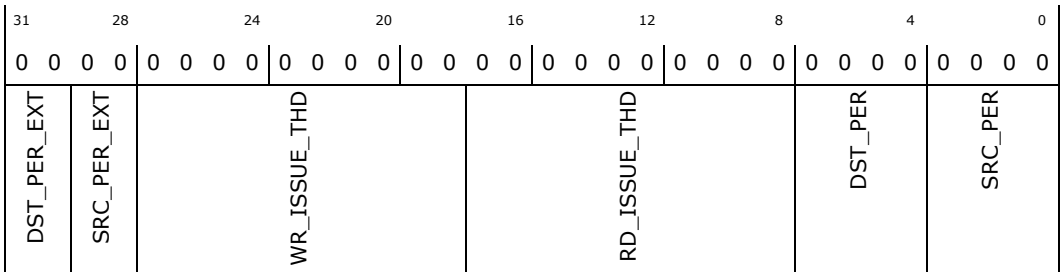
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI6: [BAR + 98000h] + 254h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.21.90 reg_SGR_type (SGR6)—Offset 258h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

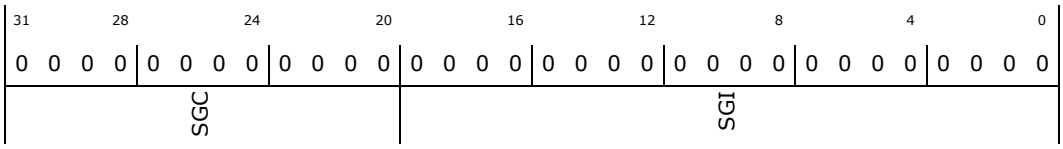
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR6: [BAR + 98000h] + 258h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.21.91 reg_DSR_type (DSR6)—Offset 260h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

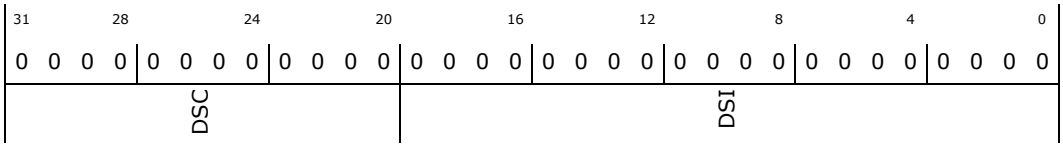
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR6: [BAR + 98000h] + 260h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.21.92 reg_SAR_type (SAR7)—Offset 268h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

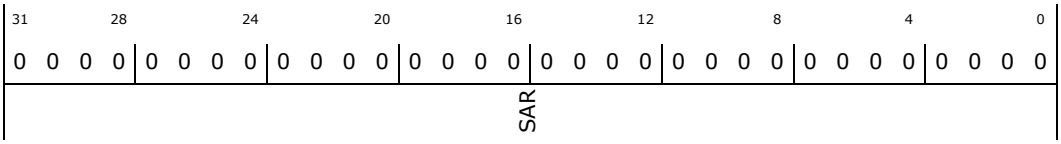
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR7: [BAR + 98000h] + 268h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.93 reg_DAR_type (DAR7)—Offset 270h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

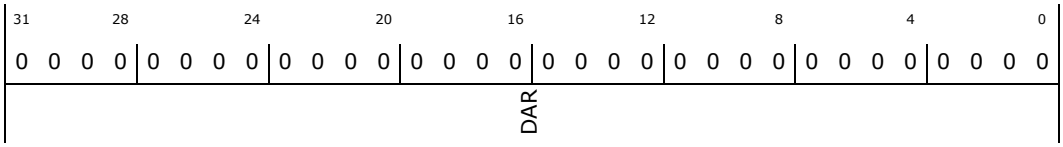
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR7: [BAR + 98000h] + 270h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.21.94 reg_LLP_type (LLP7)—Offset 278h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

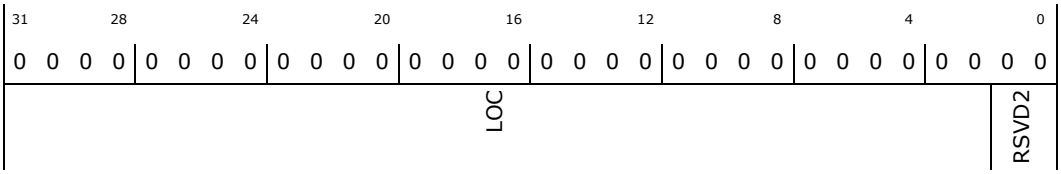
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP7: [BAR + 98000h] + 278h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.21.95 reg_CTL_LO_type (CTL_LO7)—Offset 280h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

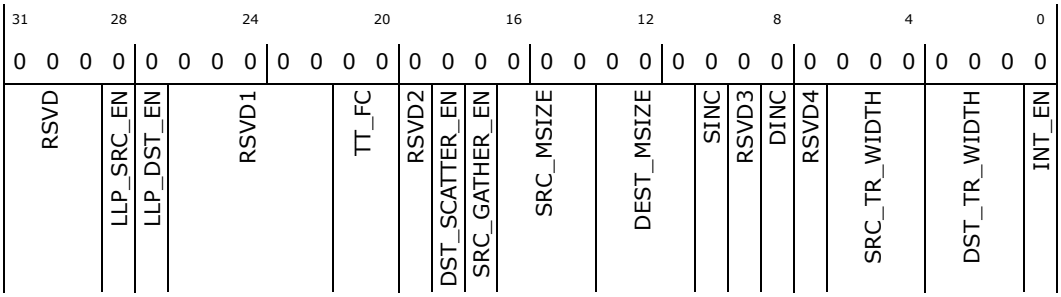
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO7: [BAR + 98000h] + 280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.

Bit Range	Default & Access	Description
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.21.96 reg_CTL_HI_type (CTL_HI7)—Offset 284h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

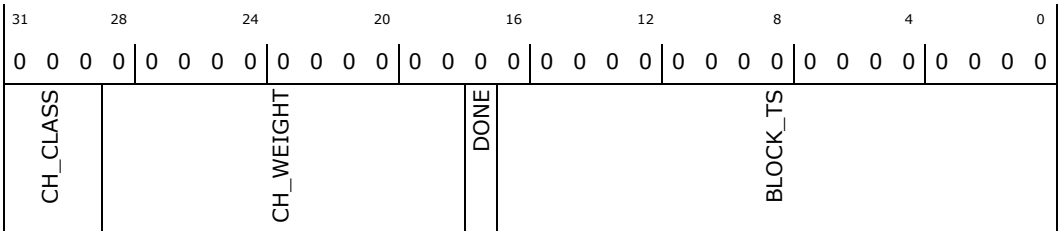
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI7: [BAR + 98000h] + 284h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.

Bit Range	Default & Access	Description
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.21.97 reg_SSTAT_type (SSTAT7)—Offset 288h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

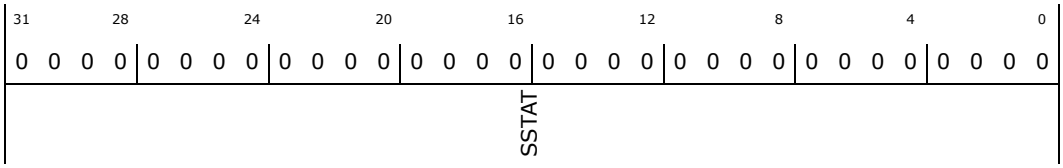
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT7: [BAR + 98000h] + 288h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.21.98 reg_DSTAT_type (DSTAT7)—Offset 290h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

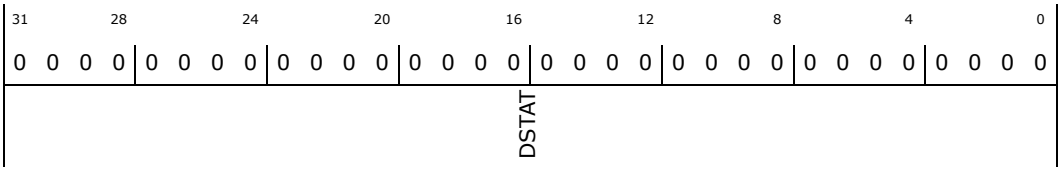
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT7: [BAR + 98000h] + 290h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.21.99 reg_SSTATAR_type (SSTATAR7)—Offset 298h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

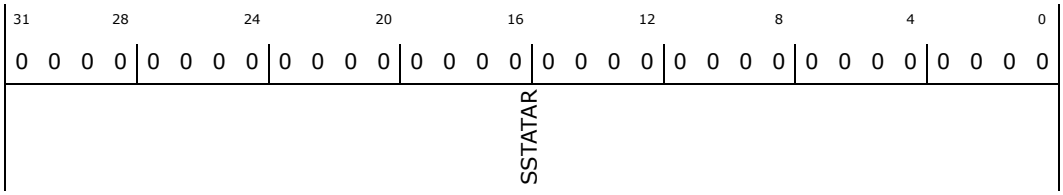
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR7: [BAR + 98000h] + 298h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.21.100 reg_DSTATAR_type (DSTATAR7)—Offset 2A0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

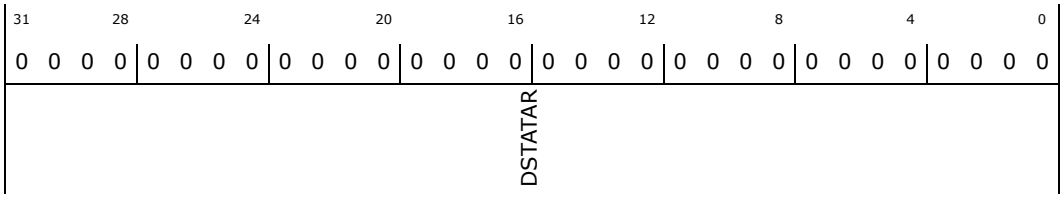
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR7: [BAR + 98000h] + 2A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.21.101 reg_CFG_LO_type (CFG_LO7)—Offset 2A8h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

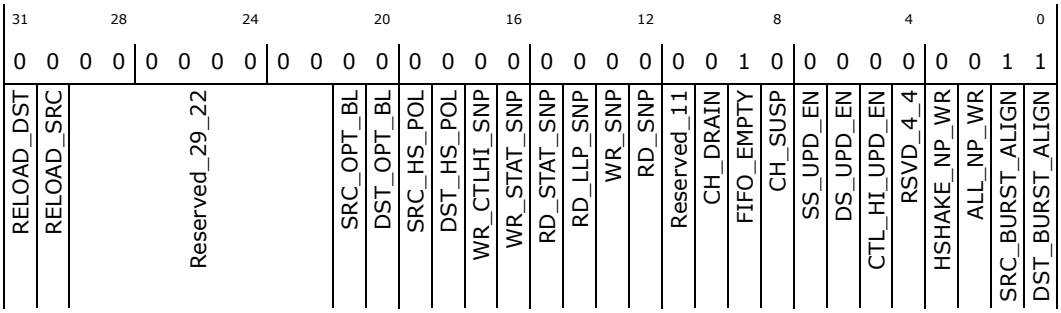
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO7: [BAR + 98000h] + 2A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port

Bit Range	Default & Access	Description
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.21.102 reg_CFG_HI_type (CFG_HI7)—Offset 2ACh

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

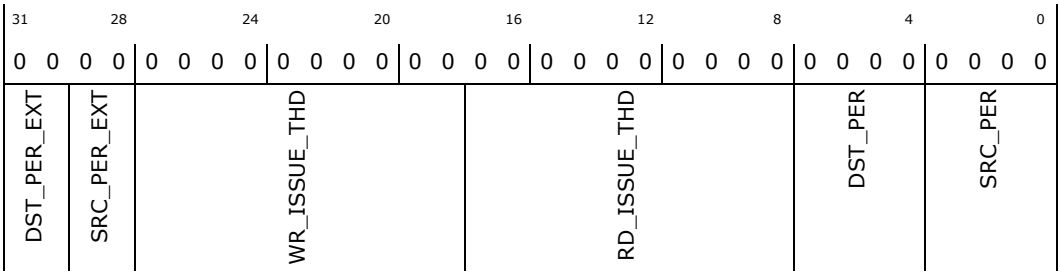
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI7: [BAR + 98000h] + 2ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.21.103 reg_SGR_type (SGR7)—Offset 2B0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

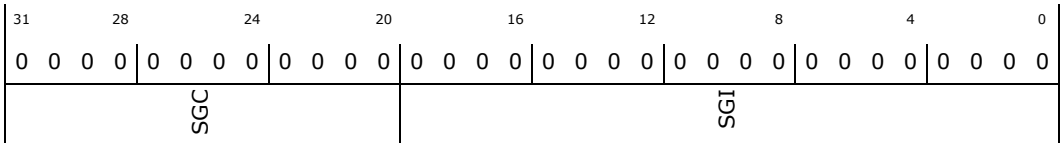
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR7: [BAR + 98000h] + 2B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.21.104 reg_DSR_type (DSR7)—Offset 2B8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

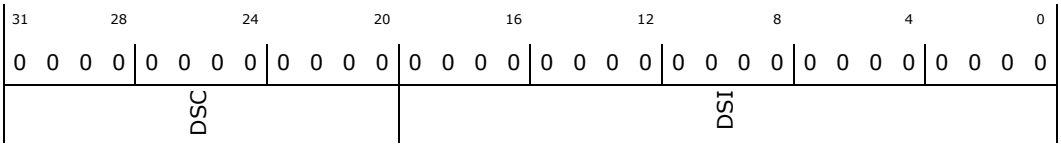
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR7: [BAR + 98000h] + 2B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.21.105 reg_Raw_type (RawTfr)—Offset 2C0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

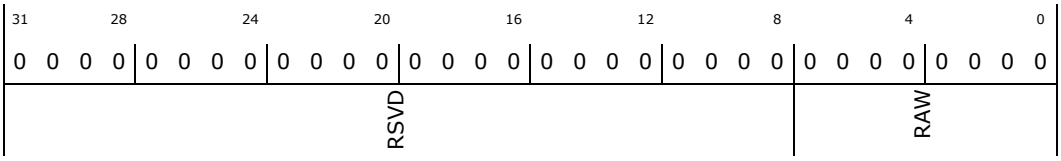
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawTfr: [BAR + 98000h] + 2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

3.21.106 reg_Raw_type (RawBlock)—Offset 2C8h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

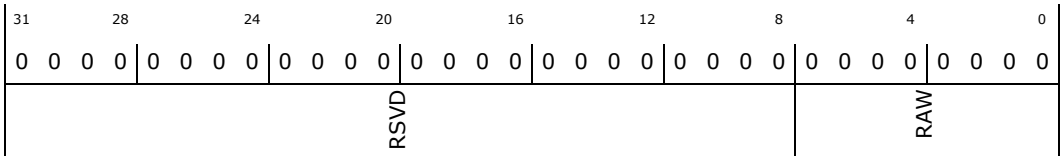
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawBlock: [BAR + 98000h] + 2C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

3.21.107 reg_Raw_type (RawSrcTran)—Offset 2D0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

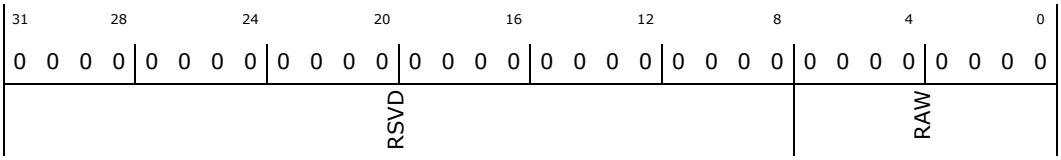
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawSrcTran: [BAR + 98000h] + 2D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

3.21.108 reg_Raw_type (RawDstTran)—Offset 2D8h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

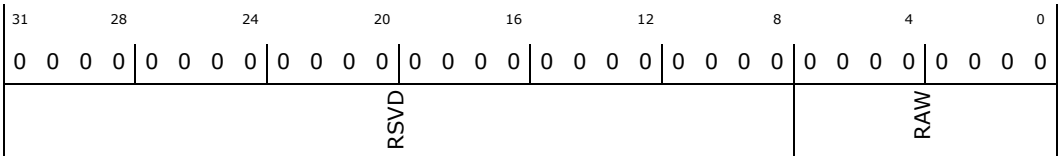
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawDstTran: [BAR + 98000h] + 2D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
7:0	0h RO	**RAW:** Raw interrupt status

3.21.109 reg_Raw_type (RawErr)—Offset 2E0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

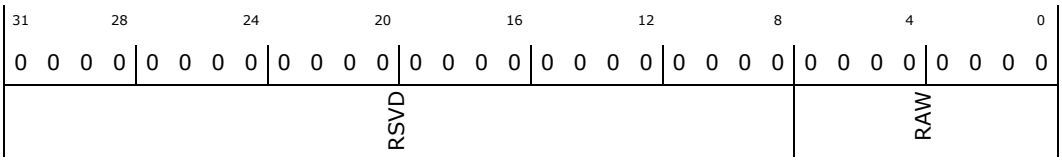
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawErr: [BAR + 98000h] + 2E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

3.21.110 reg_Status_type (StatusTfr)—Offset 2E8h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

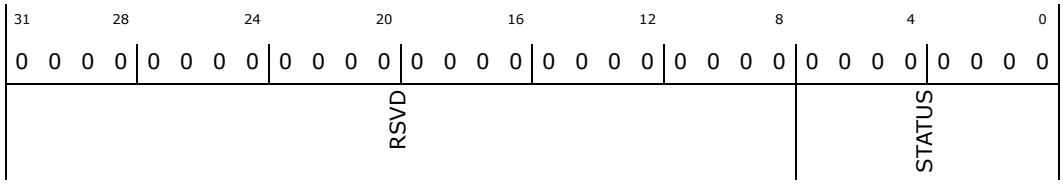
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusTfr: [BAR + 98000h] + 2E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

3.21.111 reg_Status_type (StatusBlock)—Offset 2F0h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

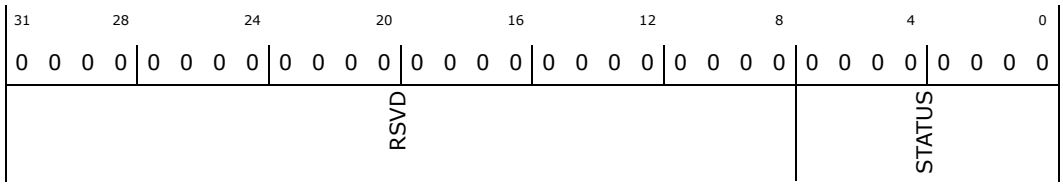
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusBlock: [BAR + 98000h] + 2F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

3.21.112 reg_Status_type (StatusSrcTran)—Offset 2F8h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

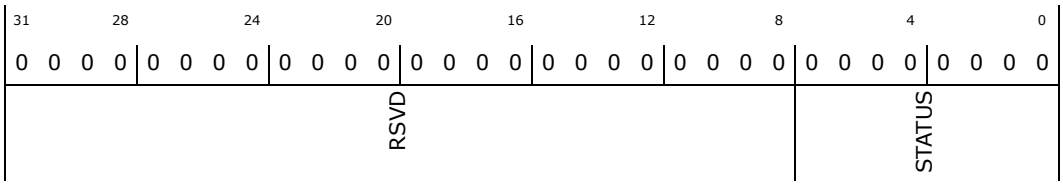
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusSrcTran: [BAR + 98000h] + 2F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

3.21.113 reg_Status_type (StatusDstTran)—Offset 300h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

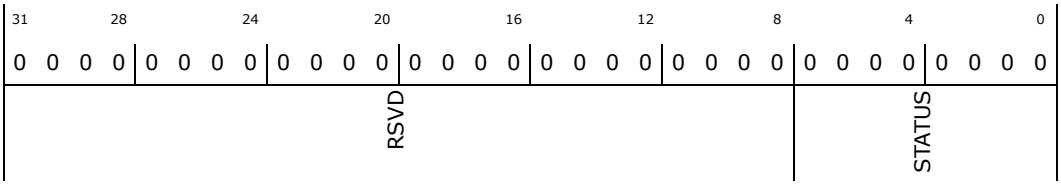
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusDstTran: [BAR + 98000h] + 300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

3.21.114 reg_Status_type (StatusErr)—Offset 308h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

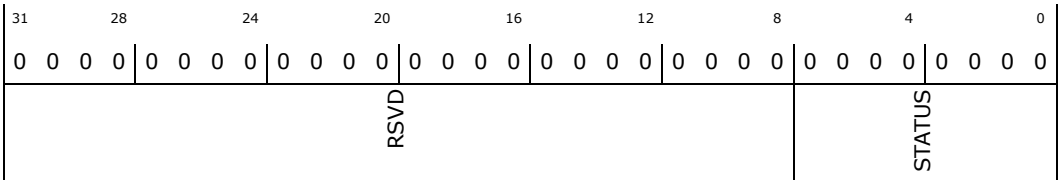
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusErr: [BAR + 98000h] + 308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

3.21.115 reg_Mask_type (MaskTfr)—Offset 310h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA

channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

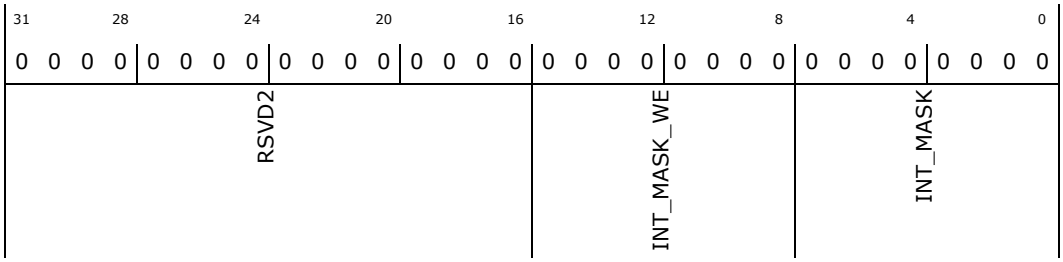
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskTfr: [BAR + 98000h] + 310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

3.21.116 reg_Mask_type (MaskBlock)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be

masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

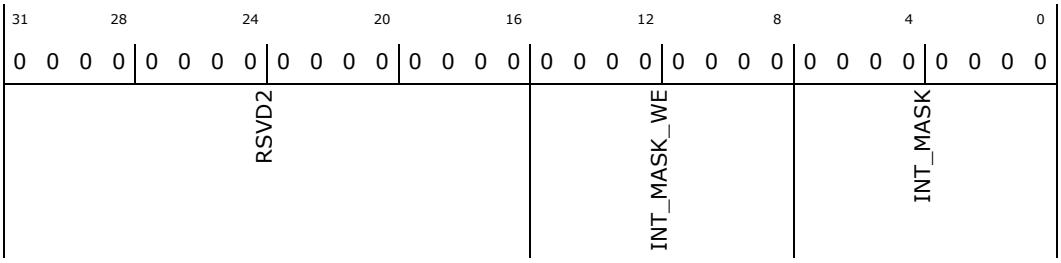
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskBlock: [BAR + 98000h] + 318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

3.21.117 reg_Mask_type (MaskSrcTran)—Offset 320h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation.

For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

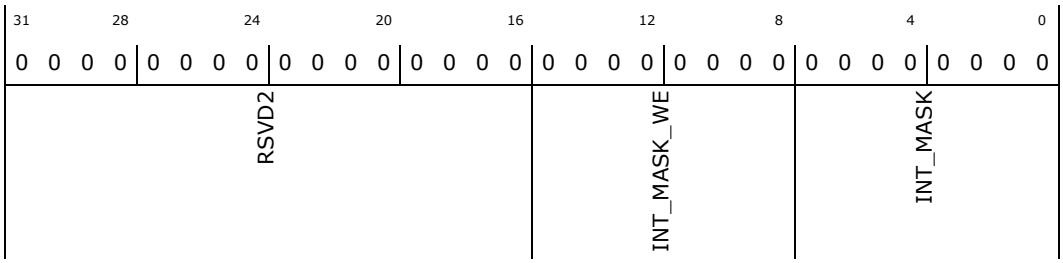
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskSrcTran: [BAR + 98000h] + 320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

3.21.118 reg_Mask_type (MaskDstTran)—Offset 328h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

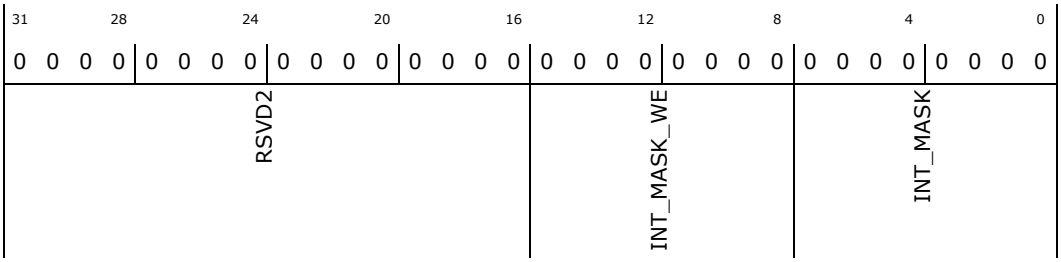
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskDstTran: [BAR + 98000h] + 328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

3.21.119 reg_Mask_type (MaskErr)—Offset 330h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

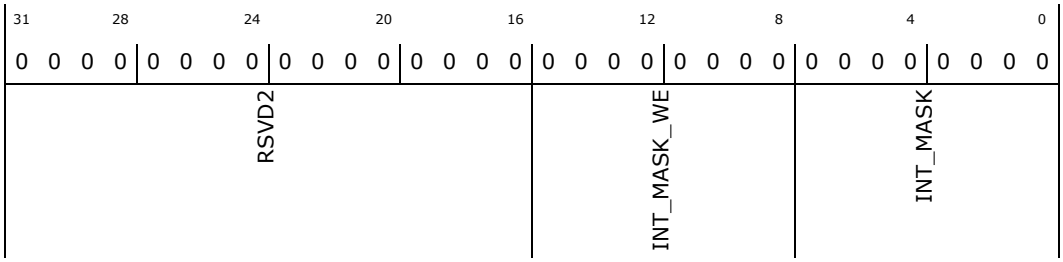
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskErr: [BAR + 98000h] + 330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

3.21.120 reg_Clear_type (ClearTfr)—Offset 338h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

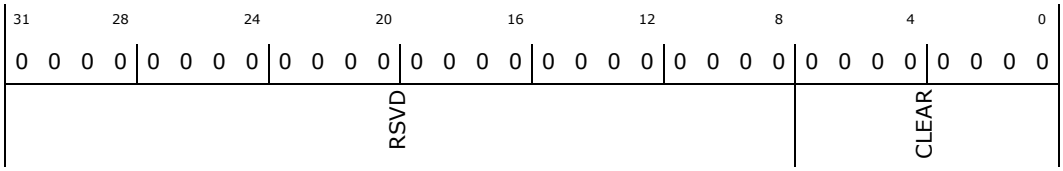
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearTfr: [BAR + 98000h] + 338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

3.21.121 reg_Clear_type (ClearBlock)—Offset 340h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

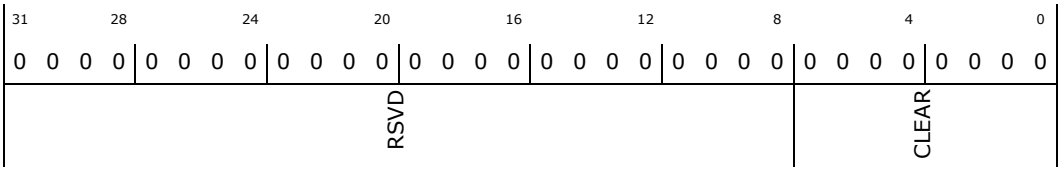
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearBlock: [BAR + 98000h] + 340h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

3.21.122 reg_Clear_type (ClearSrcTran)—Offset 348h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

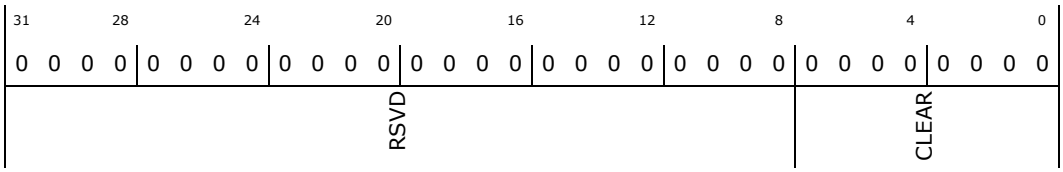
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearSrcTran: [BAR + 98000h] + 348h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

3.21.123 reg_Clear_type (ClearDstTran)—Offset 350h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

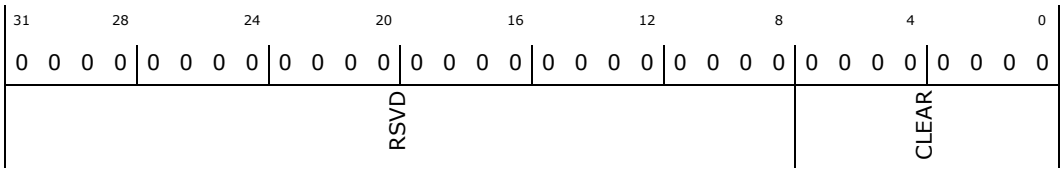
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearDstTran: [BAR + 98000h] + 350h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

3.21.124 reg_Clear_type (ClearErr)—Offset 358h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

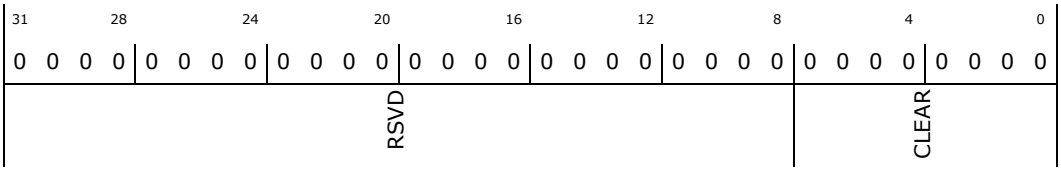
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearErr: [BAR + 98000h] + 358h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

3.21.125 reg_StatusInt_type (StatusInt)—Offset 360h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

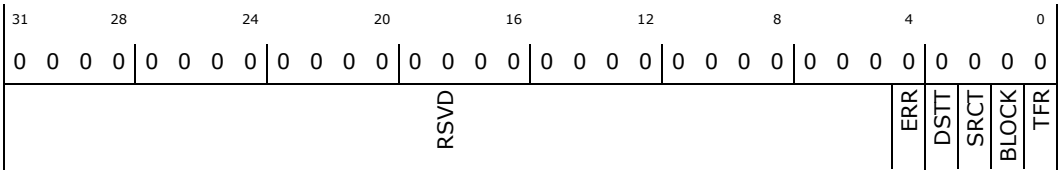
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusInt: [BAR + 98000h] + 360h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RO	**RSVD:** Reserved
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register

Bit Range	Default & Access	Description
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

3.21.126 reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

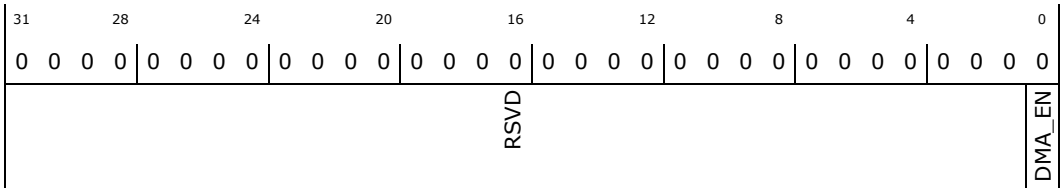
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaCfgReg: [BAR + 98000h] + 398h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RO	**RSVD:** Reserved
0	0h RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

3.21.127 reg_ChEnReg_type (ChEnReg)—Offset 3A0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged. Note that a read-modified write is not required.

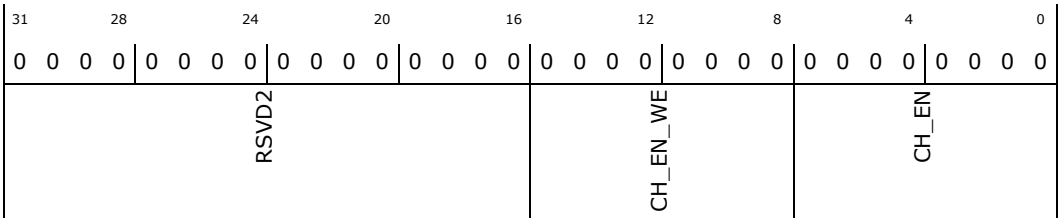
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ChEnReg: [BAR + 98000h] + 3A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**CH_EN_WE:** Channel enable write enable.
7:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

3.21.128 reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h

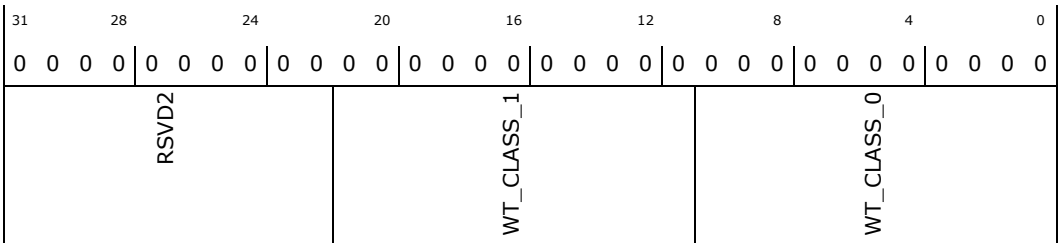
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority0_LO: [BAR + 98000h] + 3B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RO	**RSVD2:** Reserved
21:11	0h RW	**WT_CLASS_1:** Class Weight 1: Value of K assigns a weight of (K+1) to Class 1. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_0:** Class Weight 0: Value of K assigns a weight of (K+1) to Class 0. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

3.21.129 reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh

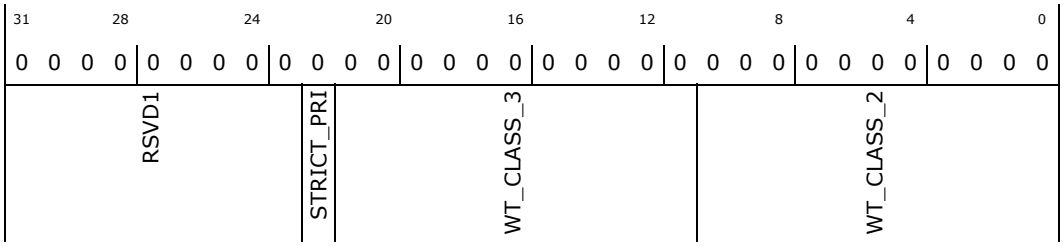
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority0_HI: [BAR + 98000h] + 3BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RO	**RSVD1:** Reserved
22	0h RW	**STRICT_PRI:** If set, Higher class values will always have higher priorities than lower class values. If not set, round-robin arbitration will be used between different classes using WT_CLASS_n values.
21:11	0h RW	**WT_CLASS_3:** Class Weight 3: Value of K assigns a weight of (K+1) to Class 3. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_2:** Class Weight 2: Value of K assigns a weight of (K+1) to Class 2. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

3.21.130 reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h

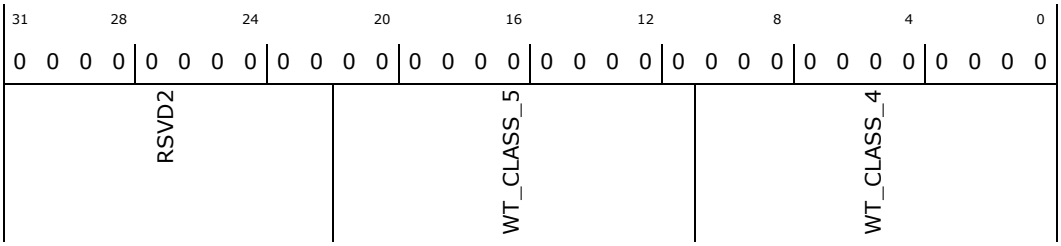
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority1_LO: [BAR + 98000h] + 3C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RO	**RSVD2:** Reserved
21:11	0h RW	**WT_CLASS_5:** Class Weight 5: Value of K assigns a weight of (K+1) to Class 5. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_4:** Class Weight 4: Value of K assigns a weight of (K+1) to Class 4. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

3.21.131 reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h

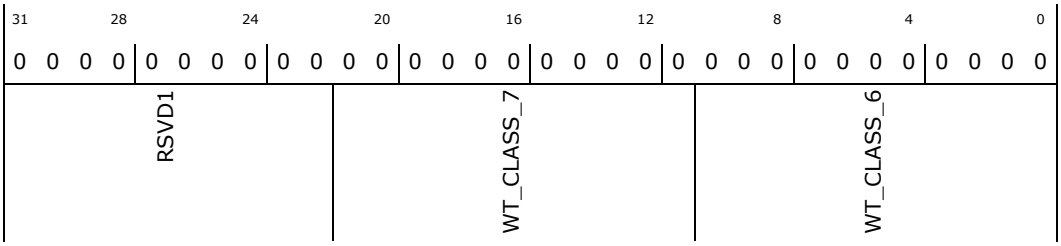
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority1_HI: [BAR + 98000h] + 3C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RO	**RSVD1:** Reserved

Bit Range	Default & Access	Description
21:11	0h RW	**WT_CLASS_7:** Class Weight 7: Value of K assigns a weight of (K+1) to Class 7. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_6:** Class Weight 6: Value of K assigns a weight of (K+1) to Class 6. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

3.21.132 reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h

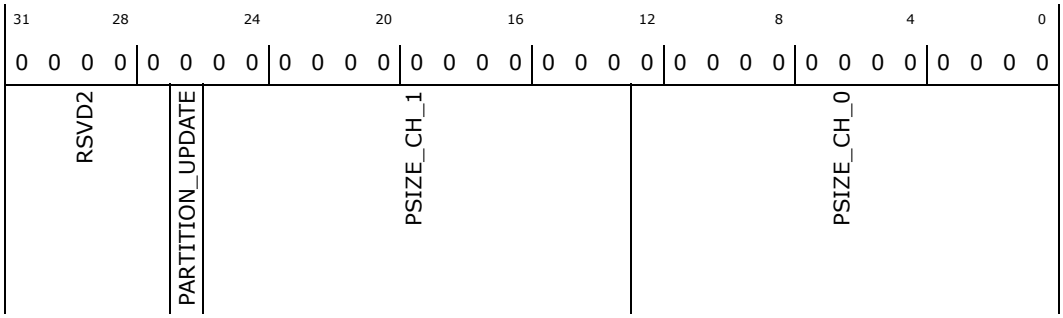
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FifoPartition0_LO: [BAR + 98000h] + 400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:27	0h RO	**RSVD2:** Reserved
26	0h RW	**PARTITION_UPDATE:** SW needs to write to this bit for the partitioning assignments to take effect.
25:13	0h RW	**PSIZE_CH_1:** Partition Byte Size assigned to Channel 1. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_0:** Partition Byte Size assigned to Channel 0. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

3.21.133 reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h

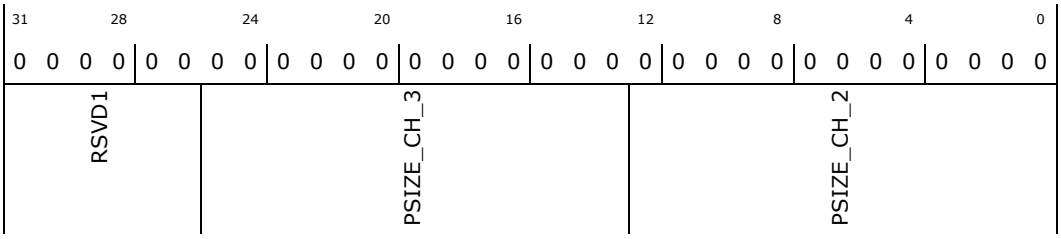
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FifoPartition0_HI: [BAR + 98000h] + 404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0h RO	**RSVD1:** Reserved
25:13	0h RW	**PSIZE_CH_3:** Partition Byte Size assigned to Channel 3. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_2:** Partition Byte Size assigned to Channel 2. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

3.21.134 reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h

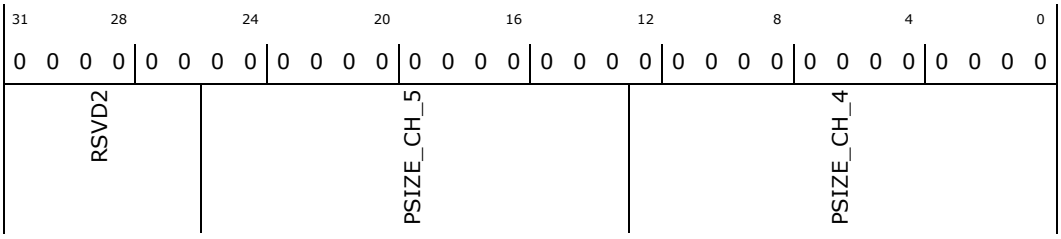
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FifoPartition1_LO: [BAR + 98000h] + 408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0h RO	**RSVD2:** Reserved

Bit Range	Default & Access	Description
25:13	0h RW	**PSIZE_CH_5:** Partition Byte Size assigned to Channel 5. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_4:** Partition Byte Size assigned to Channel 4. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

3.21.135 reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch

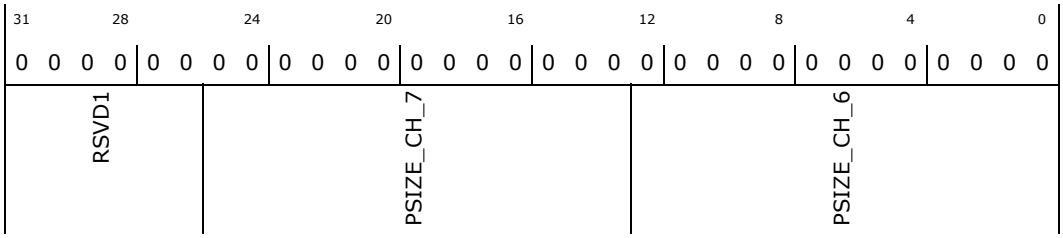
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FifoPartition1_HI: [BAR + 98000h] + 40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0h RO	**RSVD1:** Reserved
25:13	0h RW	**PSIZE_CH_7:** Partition Byte Size assigned to Channel 7. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_6:** Partition Byte Size assigned to Channel 6. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

3.21.136 reg_SAI_Error_type (SAI_ERR)—Offset 410h

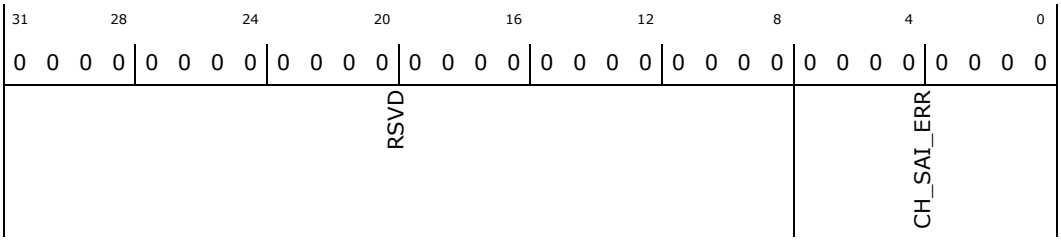
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAI_ERR: [BAR + 98000h] + 410h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**CH_SAI_ERR:** 1: SAI Error occurred on Ch [n] 0: No SAI Error occurred on Ch [n] SAI_ERROR[n] is set by HW on SAI violation for channel [n]. All bits get cleared by SW when reading this register

3.21.137 reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h

GLOBAL_CFG: GLOBAL DMA Configuration Register

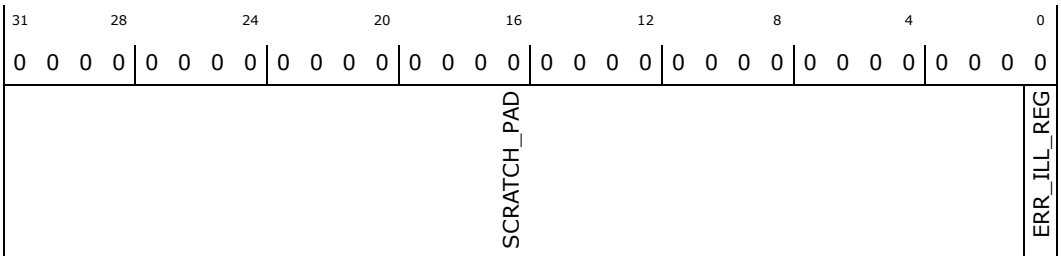
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GLOBAL_CFG: [BAR + 98000h] + 418h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future configuration and de-feature bits.
0	0b RW	**ERR_ILL_REG:** 0x1 : Issue ERR response on reading illegal (non-existing) registers 0x0 : Issue DVA response on reading illegal (non-existing) registers

3.22 Low Power Audio DMA1 Memory Mapped IO Registers

Table 30. Summary of Low Power Audio DMA1 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_SAR_type (SAR0)—Offset 0h" on page 1932	00000000h
8h	4	"reg_DAR_type (DAR0)—Offset 8h" on page 1933	00000000h
10h	4	"reg_LLP_type (LLP0)—Offset 10h" on page 1934	00000000h
18h	4	"reg_CTL_LO_type (CTL_LO0)—Offset 18h" on page 1935	00000000h
1Ch	4	"reg_CTL_HI_type (CTL_HI0)—Offset 1Ch" on page 1936	00000000h
20h	4	"reg_SSTAT_type (SSTAT0)—Offset 20h" on page 1938	00000000h
28h	4	"reg_DSTAT_type (DSTAT0)—Offset 28h" on page 1938	00000000h
30h	4	"reg_SSTATAR_type (SSTATAR0)—Offset 30h" on page 1939	00000000h
38h	4	"reg_DSTATAR_type (DSTATAR0)—Offset 38h" on page 1939	00000000h
40h	4	"reg_CFG_LO_type (CFG_LO0)—Offset 40h" on page 1940	00000203h
44h	4	"reg_CFG_HI_type (CFG_HI0)—Offset 44h" on page 1942	00000000h
48h	4	"reg_SGR_type (SGR0)—Offset 48h" on page 1943	00000000h
50h	4	"reg_DSR_type (DSR0)—Offset 50h" on page 1944	00000000h
58h	4	"reg_SAR_type (SAR1)—Offset 58h" on page 1945	00000000h
60h	4	"reg_DAR_type (DAR1)—Offset 60h" on page 1945	00000000h
68h	4	"reg_LLP_type (LLP1)—Offset 68h" on page 1946	00000000h
70h	4	"reg_CTL_LO_type (CTL_LO1)—Offset 70h" on page 1947	00000000h
74h	4	"reg_CTL_HI_type (CTL_HI1)—Offset 74h" on page 1949	00000000h
78h	4	"reg_SSTAT_type (SSTAT1)—Offset 78h" on page 1950	00000000h
80h	4	"reg_DSTAT_type (DSTAT1)—Offset 80h" on page 1951	00000000h
88h	4	"reg_SSTATAR_type (SSTATAR1)—Offset 88h" on page 1951	00000000h
90h	4	"reg_DSTATAR_type (DSTATAR1)—Offset 90h" on page 1952	00000000h
98h	4	"reg_CFG_LO_type (CFG_LO1)—Offset 98h" on page 1952	00000203h
9Ch	4	"reg_CFG_HI_type (CFG_HI1)—Offset 9Ch" on page 1954	00000000h
A0h	4	"reg_SGR_type (SGR1)—Offset A0h" on page 1956	00000000h
A8h	4	"reg_DSR_type (DSR1)—Offset A8h" on page 1956	00000000h
B0h	4	"reg_SAR_type (SAR2)—Offset B0h" on page 1957	00000000h
B8h	4	"reg_DAR_type (DAR2)—Offset B8h" on page 1958	00000000h
C0h	4	"reg_LLP_type (LLP2)—Offset C0h" on page 1959	00000000h
C8h	4	"reg_CTL_LO_type (CTL_LO2)—Offset C8h" on page 1960	00000000h
CCh	4	"reg_CTL_HI_type (CTL_HI2)—Offset CCh" on page 1961	00000000h
D0h	4	"reg_SSTAT_type (SSTAT2)—Offset D0h" on page 1963	00000000h

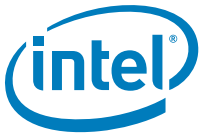


Table 30. Summary of Low Power Audio DMA1 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
D8h	4	"reg_DSTAT_type (DSTAT2)—Offset D8h" on page 1963	00000000h
E0h	4	"reg_SSTATAR_type (SSTATAR2)—Offset E0h" on page 1964	00000000h
E8h	4	"reg_DSTATAR_type (DSTATAR2)—Offset E8h" on page 1964	00000000h
F0h	4	"reg_CFG_LO_type (CFG_LO2)—Offset F0h" on page 1965	00000203h
F4h	4	"reg_CFG_HI_type (CFG_HI2)—Offset F4h" on page 1967	00000000h
F8h	4	"reg_SGR_type (SGR2)—Offset F8h" on page 1968	00000000h
100h	4	"reg_DSR_type (DSR2)—Offset 100h" on page 1969	00000000h
108h	4	"reg_SAR_type (SAR3)—Offset 108h" on page 1970	00000000h
110h	4	"reg_DAR_type (DAR3)—Offset 110h" on page 1970	00000000h
118h	4	"reg_LLP_type (LLP3)—Offset 118h" on page 1971	00000000h
120h	4	"reg_CTL_LO_type (CTL_LO3)—Offset 120h" on page 1972	00000000h
124h	4	"reg_CTL_HI_type (CTL_HI3)—Offset 124h" on page 1974	00000000h
128h	4	"reg_SSTAT_type (SSTAT3)—Offset 128h" on page 1975	00000000h
130h	4	"reg_DSTAT_type (DSTAT3)—Offset 130h" on page 1976	00000000h
138h	4	"reg_SSTATAR_type (SSTATAR3)—Offset 138h" on page 1976	00000000h
140h	4	"reg_DSTATAR_type (DSTATAR3)—Offset 140h" on page 1977	00000000h
148h	4	"reg_CFG_LO_type (CFG_LO3)—Offset 148h" on page 1977	00000203h
14Ch	4	"reg_CFG_HI_type (CFG_HI3)—Offset 14Ch" on page 1979	00000000h
150h	4	"reg_SGR_type (SGR3)—Offset 150h" on page 1981	00000000h
158h	4	"reg_DSR_type (DSR3)—Offset 158h" on page 1981	00000000h
160h	4	"reg_SAR_type (SAR4)—Offset 160h" on page 1982	00000000h
168h	4	"reg_DAR_type (DAR4)—Offset 168h" on page 1983	00000000h
170h	4	"reg_LLP_type (LLP4)—Offset 170h" on page 1984	00000000h
178h	4	"reg_CTL_LO_type (CTL_LO4)—Offset 178h" on page 1985	00000000h
17Ch	4	"reg_CTL_HI_type (CTL_HI4)—Offset 17Ch" on page 1986	00000000h
180h	4	"reg_SSTAT_type (SSTAT4)—Offset 180h" on page 1988	00000000h
188h	4	"reg_DSTAT_type (DSTAT4)—Offset 188h" on page 1988	00000000h
190h	4	"reg_SSTATAR_type (SSTATAR4)—Offset 190h" on page 1989	00000000h
198h	4	"reg_DSTATAR_type (DSTATAR4)—Offset 198h" on page 1989	00000000h
1A0h	4	"reg_CFG_LO_type (CFG_LO4)—Offset 1A0h" on page 1990	00000203h
1A4h	4	"reg_CFG_HI_type (CFG_HI4)—Offset 1A4h" on page 1992	00000000h
1A8h	4	"reg_SGR_type (SGR4)—Offset 1A8h" on page 1993	00000000h
1B0h	4	"reg_DSR_type (DSR4)—Offset 1B0h" on page 1994	00000000h
1B8h	4	"reg_SAR_type (SAR5)—Offset 1B8h" on page 1995	00000000h
1C0h	4	"reg_DAR_type (DAR5)—Offset 1C0h" on page 1995	00000000h

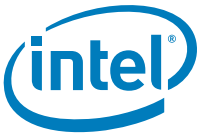


Table 30. Summary of Low Power Audio DMA1 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
1C8h	4	"reg_LLP_type (LLP5)—Offset 1C8h" on page 1996	00000000h
1D0h	4	"reg_CTL_LO_type (CTL_LO5)—Offset 1D0h" on page 1997	00000000h
1D4h	4	"reg_CTL_HI_type (CTL_HI5)—Offset 1D4h" on page 1999	00000000h
1D8h	4	"reg_SSTAT_type (SSTAT5)—Offset 1D8h" on page 2000	00000000h
1E0h	4	"reg_DSTAT_type (DSTAT5)—Offset 1E0h" on page 2001	00000000h
1E8h	4	"reg_SSTATAR_type (SSTATAR5)—Offset 1E8h" on page 2001	00000000h
1F0h	4	"reg_DSTATAR_type (DSTATAR5)—Offset 1F0h" on page 2002	00000000h
1F8h	4	"reg_CFG_LO_type (CFG_LO5)—Offset 1F8h" on page 2002	00000203h
1FCh	4	"reg_CFG_HI_type (CFG_HI5)—Offset 1FCh" on page 2004	00000000h
200h	4	"reg_SGR_type (SGR5)—Offset 200h" on page 2006	00000000h
208h	4	"reg_DSR_type (DSR5)—Offset 208h" on page 2006	00000000h
210h	4	"reg_SAR_type (SAR6)—Offset 210h" on page 2007	00000000h
218h	4	"reg_DAR_type (DAR6)—Offset 218h" on page 2008	00000000h
220h	4	"reg_LLP_type (LLP6)—Offset 220h" on page 2009	00000000h
228h	4	"reg_CTL_LO_type (CTL_LO6)—Offset 228h" on page 2010	00000000h
22Ch	4	"reg_CTL_HI_type (CTL_HI6)—Offset 22Ch" on page 2011	00000000h
230h	4	"reg_SSTAT_type (SSTAT6)—Offset 230h" on page 2013	00000000h
238h	4	"reg_DSTAT_type (DSTAT6)—Offset 238h" on page 2013	00000000h
240h	4	"reg_SSTATAR_type (SSTATAR6)—Offset 240h" on page 2014	00000000h
248h	4	"reg_DSTATAR_type (DSTATAR6)—Offset 248h" on page 2014	00000000h
250h	4	"reg_CFG_LO_type (CFG_LO6)—Offset 250h" on page 2015	00000203h
254h	4	"reg_CFG_HI_type (CFG_HI6)—Offset 254h" on page 2017	00000000h
258h	4	"reg_SGR_type (SGR6)—Offset 258h" on page 2018	00000000h
260h	4	"reg_DSR_type (DSR6)—Offset 260h" on page 2019	00000000h
268h	4	"reg_SAR_type (SAR7)—Offset 268h" on page 2020	00000000h
270h	4	"reg_DAR_type (DAR7)—Offset 270h" on page 2020	00000000h
278h	4	"reg_LLP_type (LLP7)—Offset 278h" on page 2021	00000000h
280h	4	"reg_CTL_LO_type (CTL_LO7)—Offset 280h" on page 2022	00000000h
284h	4	"reg_CTL_HI_type (CTL_HI7)—Offset 284h" on page 2024	00000000h
288h	4	"reg_SSTAT_type (SSTAT7)—Offset 288h" on page 2025	00000000h
290h	4	"reg_DSTAT_type (DSTAT7)—Offset 290h" on page 2026	00000000h
298h	4	"reg_SSTATAR_type (SSTATAR7)—Offset 298h" on page 2026	00000000h
2A0h	4	"reg_DSTATAR_type (DSTATAR7)—Offset 2A0h" on page 2027	00000000h
2A8h	4	"reg_CFG_LO_type (CFG_LO7)—Offset 2A8h" on page 2027	00000203h
2ACh	4	"reg_CFG_HI_type (CFG_HI7)—Offset 2ACh" on page 2029	00000000h

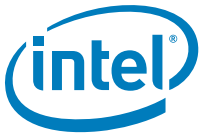


Table 30. Summary of Low Power Audio DMA1 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
2B0h	4	"reg_SGR_type (SGR7)—Offset 2B0h" on page 2031	00000000h
2B8h	4	"reg_DSR_type (DSR7)—Offset 2B8h" on page 2031	00000000h
2C0h	4	"reg_Raw_type (RawTfr)—Offset 2C0h" on page 2032	00000000h
2C8h	4	"reg_Raw_type (RawBlock)—Offset 2C8h" on page 2033	00000000h
2D0h	4	"reg_Raw_type (RawSrcTran)—Offset 2D0h" on page 2033	00000000h
2D8h	4	"reg_Raw_type (RawDstTran)—Offset 2D8h" on page 2034	00000000h
2E0h	4	"reg_Raw_type (RawErr)—Offset 2E0h" on page 2035	00000000h
2E8h	4	"reg_Status_type (StatusTfr)—Offset 2E8h" on page 2035	00000000h
2F0h	4	"reg_Status_type (StatusBlock)—Offset 2F0h" on page 2036	00000000h
2F8h	4	"reg_Status_type (StatusSrcTran)—Offset 2F8h" on page 2037	00000000h
300h	4	"reg_Status_type (StatusDstTran)—Offset 300h" on page 2037	00000000h
308h	4	"reg_Status_type (StatusErr)—Offset 308h" on page 2038	00000000h
310h	4	"reg_Mask_type (MaskTfr)—Offset 310h" on page 2038	00000000h
318h	4	"reg_Mask_type (MaskBlock)—Offset 318h" on page 2039	00000000h
320h	4	"reg_Mask_type (MaskSrcTran)—Offset 320h" on page 2040	00000000h
328h	4	"reg_Mask_type (MaskDstTran)—Offset 328h" on page 2041	00000000h
330h	4	"reg_Mask_type (MaskErr)—Offset 330h" on page 2042	00000000h
338h	4	"reg_Clear_type (ClearTfr)—Offset 338h" on page 2043	00000000h
340h	4	"reg_Clear_type (ClearBlock)—Offset 340h" on page 2044	00000000h
348h	4	"reg_Clear_type (ClearSrcTran)—Offset 348h" on page 2044	00000000h
350h	4	"reg_Clear_type (ClearDstTran)—Offset 350h" on page 2045	00000000h
358h	4	"reg_Clear_type (ClearErr)—Offset 358h" on page 2045	00000000h
360h	4	"reg_StatusInt_type (StatusInt)—Offset 360h" on page 2046	00000000h
398h	4	"reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h" on page 2047	00000000h
3A0h	4	"reg_ChEnReg_type (ChEnReg)—Offset 3A0h" on page 2047	00000000h
3B8h	4	"reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h" on page 2048	00000000h
3BCh	4	"reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh" on page 2049	00000000h
3C0h	4	"reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h" on page 2049	00000000h
3C4h	4	"reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h" on page 2050	00000000h
400h	4	"reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h" on page 2051	00000000h
404h	4	"reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h" on page 2051	00000000h

Table 30. Summary of Low Power Audio DMA1 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
408h	4	"reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h" on page 2052	00000000h
40Ch	4	"reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch" on page 2053	00000000h
410h	4	"reg_SAI_Error_type (SAI_ERR)—Offset 410h" on page 2053	00000000h
418h	4	"reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h" on page 2054	00000000h

3.22.1 reg_SAR_type (SAR0)—Offset 0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

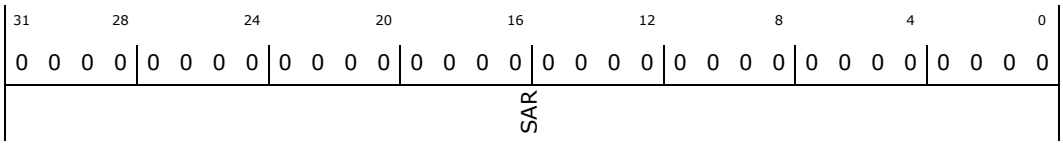
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR0: [BAR + 9C000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.2 reg_DAR_type (DAR0)—Offset 8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

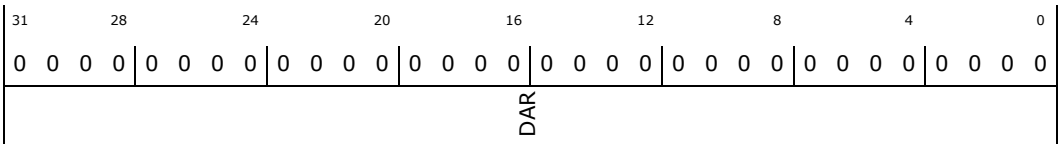
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR0: [BAR + 9C000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.3 reg_LLP_type (LLP0)—Offset 10h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

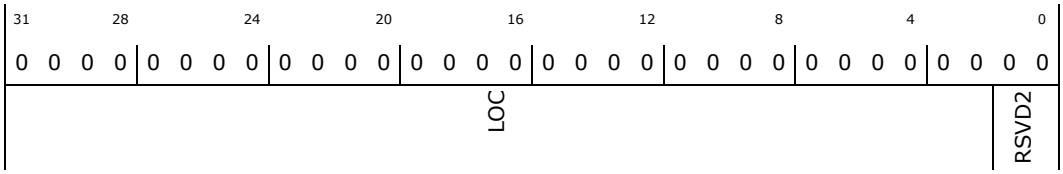
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP0: [BAR + 9C000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.22.4 reg_CTL_LO_type (CTL_LO0)—Offset 18h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

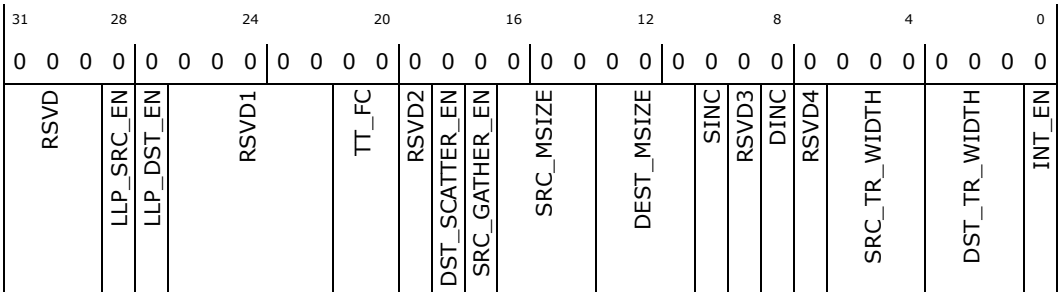
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO0: [BAR + 9C000h] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved

Bit Range	Default & Access	Description
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.22.5 reg_CTL_HI_type (CTL_HI0)—Offset 1Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

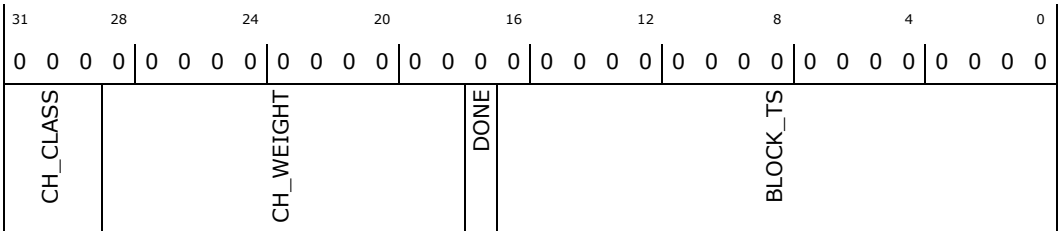
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI0: [BAR + 9C000h] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.22.6 reg_SSTAT_type (SSTAT0)—Offset 20h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

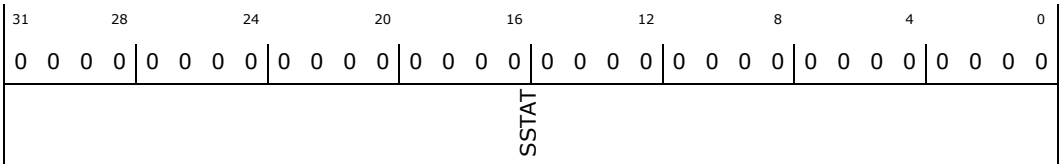
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT0: [BAR + 9C000h] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.22.7 reg_DSTAT_type (DSTAT0)—Offset 28h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

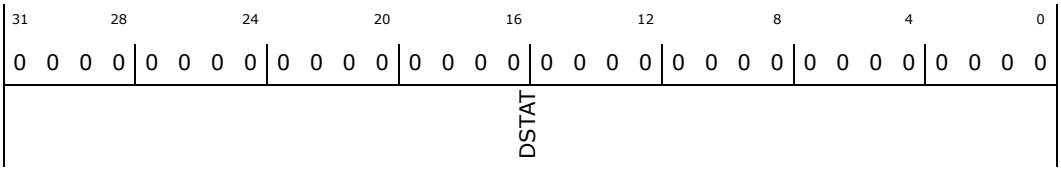
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT0: [BAR + 9C000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.22.8 reg_SSTATAR_type (SSTATAR0)—Offset 30h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

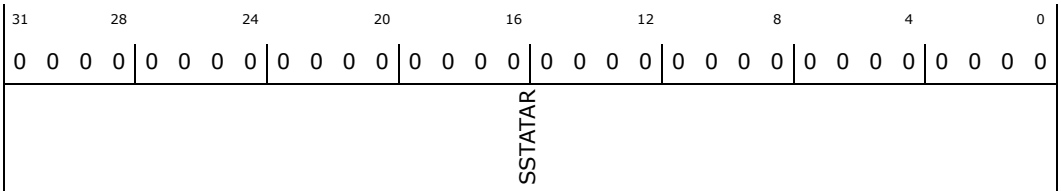
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR0: [BAR + 9C000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.22.9 reg_DSTATAR_type (DSTATAR0)—Offset 38h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

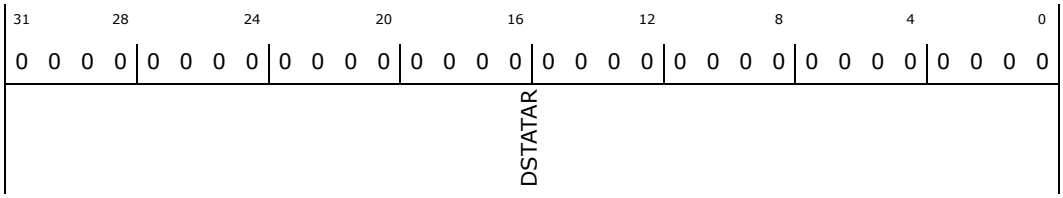
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR0: [BAR + 9C000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.22.10 reg_CFG_LO_type (CFG_LO0)—Offset 40h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

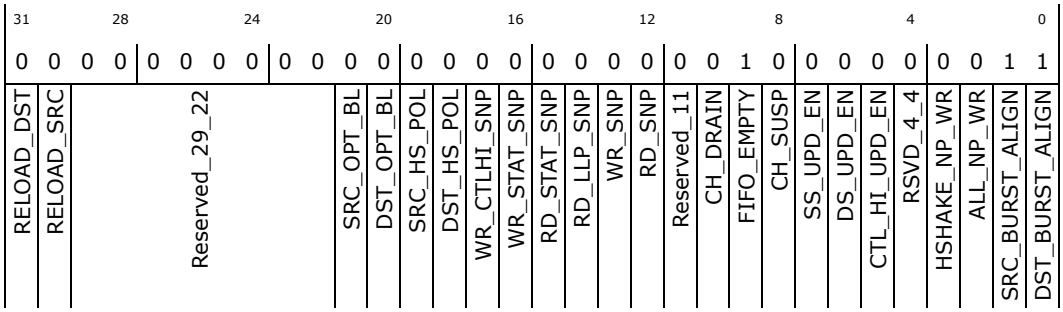
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO0: [BAR + 9C000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.

Bit Range	Default & Access	Description
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.22.11 reg_CFG_HI_type (CFG_HI0)—Offset 44h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

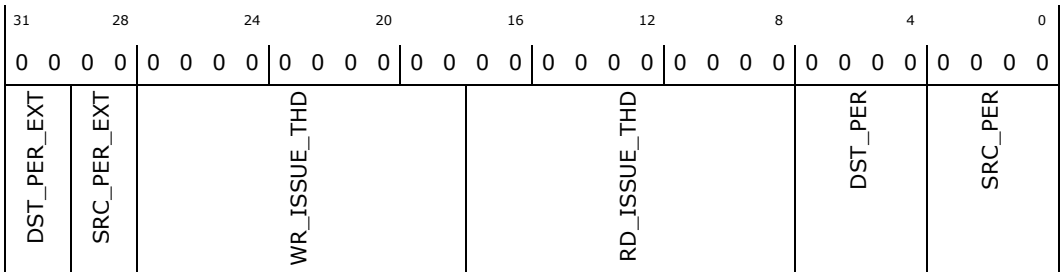
Access Method

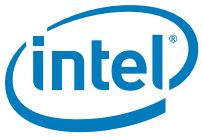
Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI0: [BAR + 9C000h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.22.12 reg_SGR_type (SGR0)—Offset 48h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

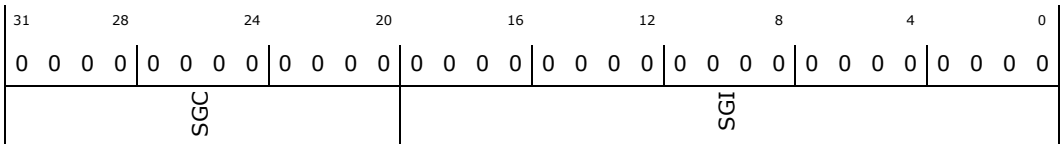
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR0: [BAR + 9C000h] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.22.13 reg_DSR_type (DSR0)—Offset 50h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

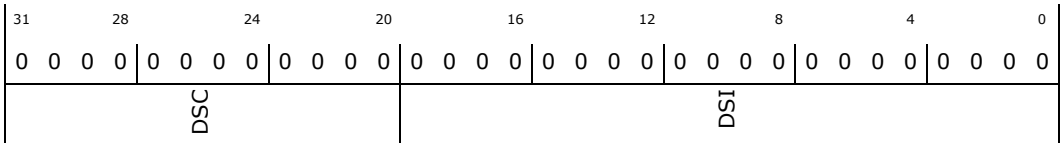
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR0: [BAR + 9C000h] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.22.14 reg_SAR_type (SAR1)—Offset 58h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

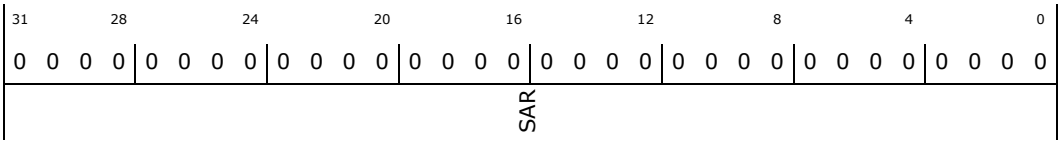
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR1: [BAR + 9C000h] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.15 reg_DAR_type (DAR1)—Offset 60h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

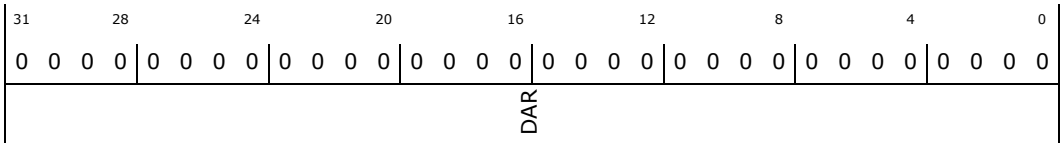
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR1: [BAR + 9C000h] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.16 reg_LLP_type (LLP1)—Offset 68h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

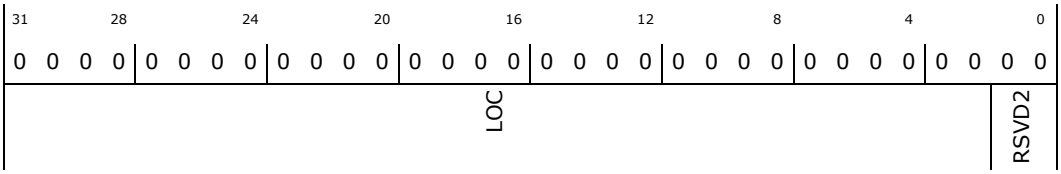
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP1: [BAR + 9C000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.22.17 reg_CTL_LO_type (CTL_LO1)—Offset 70h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

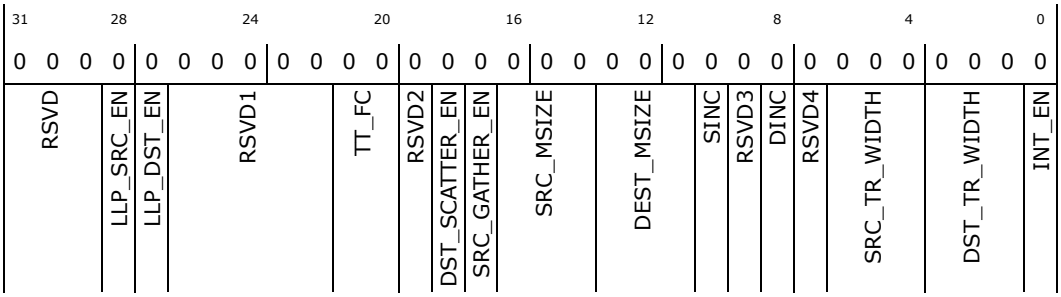
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

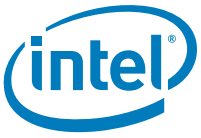
CTL_LO1: [BAR + 9C000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved



Bit Range	Default & Access	Description
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.

Bit Range	Default & Access	Description
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.22.18 reg_CTL_HI_type (CTL_HI1)—Offset 74h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

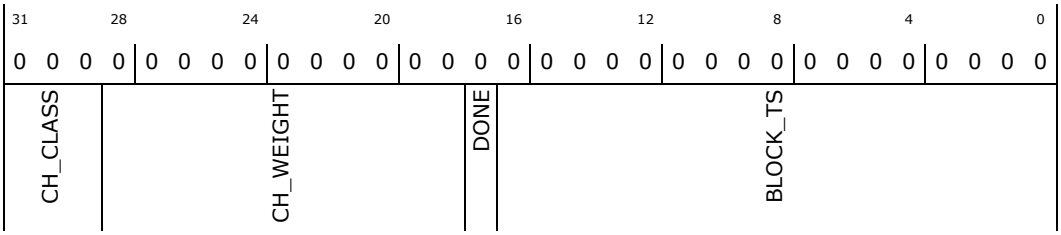
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI1: [BAR + 9C000h] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.

Bit Range	Default & Access	Description
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.22.19 reg_SSTAT_type (SSTAT1)—Offset 78h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

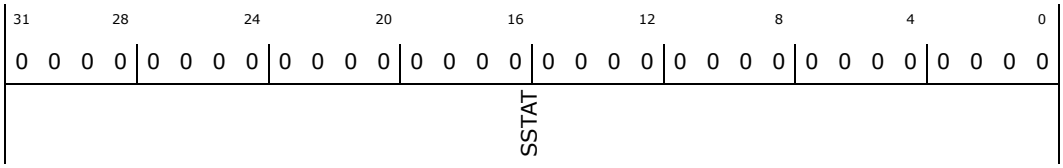
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT1: [BAR + 9C000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.22.20 reg_DSTAT_type (DSTAT1)—Offset 80h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

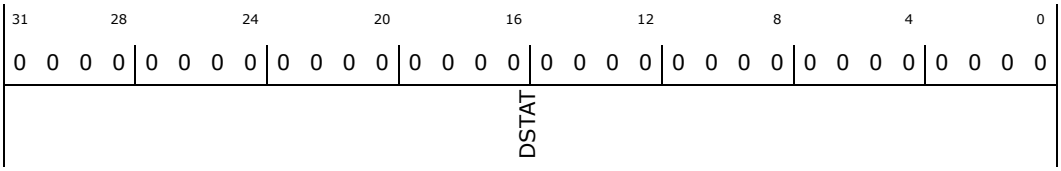
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT1: [BAR + 9C000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.22.21 reg_SSTATAR_type (SSTATAR1)—Offset 88h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

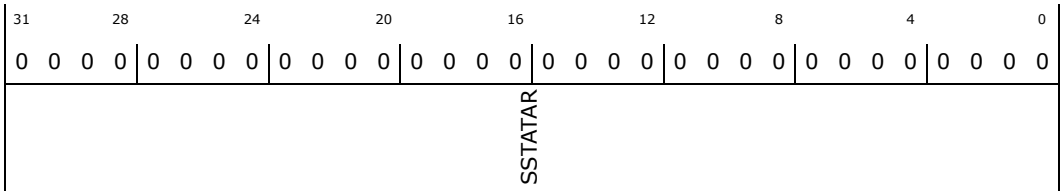
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR1: [BAR + 9C000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.22.22 reg_DSTATAR_type (DSTATAR1)—Offset 90h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

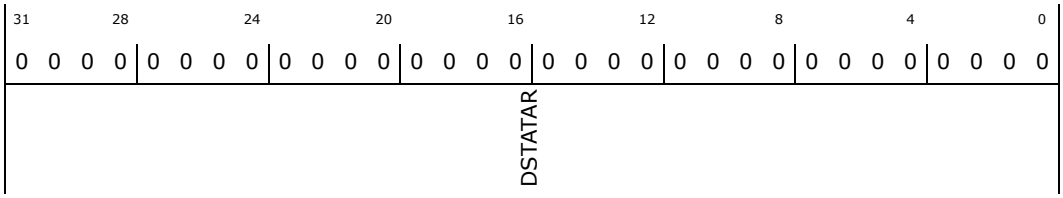
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR1: [BAR + 9C000h] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.22.23 reg_CFG_LO_type (CFG_LO1)—Offset 98h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

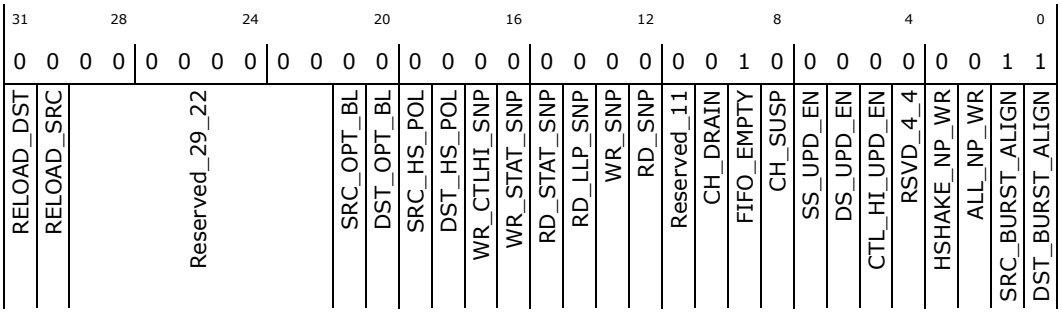
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO1: [BAR + 9C000h] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port

Bit Range	Default & Access	Description
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.22.24 reg_CFG_HI_type (CFG_HI1)—Offset 9Ch

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

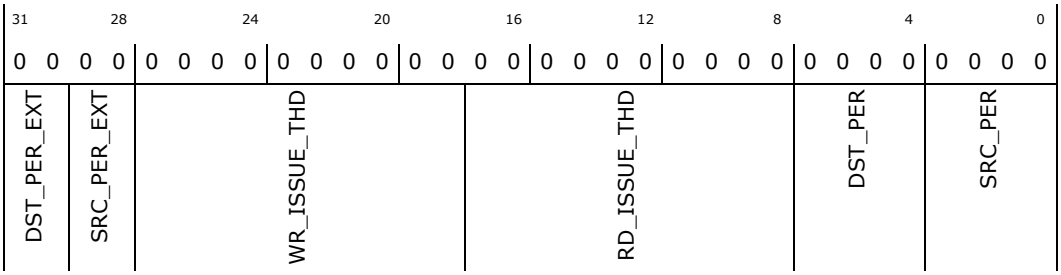
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI1: [BAR + 9C000h] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.22.25 reg_SGR_type (SGR1)—Offset A0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

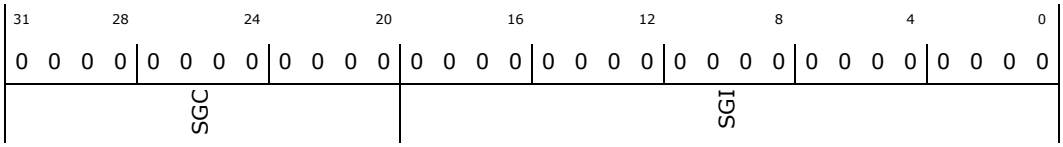
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR1: [BAR + 9C000h] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.22.26 reg_DSR_type (DSR1)—Offset A8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

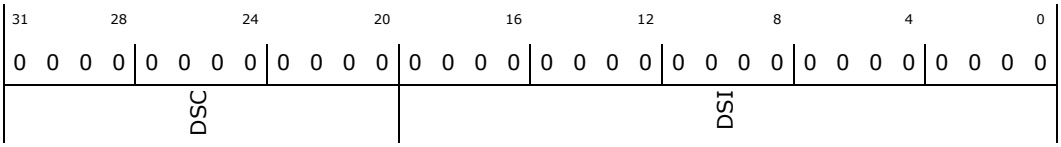
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR1: [BAR + 9C000h] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.22.27 reg_SAR_type (SAR2)—Offset B0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

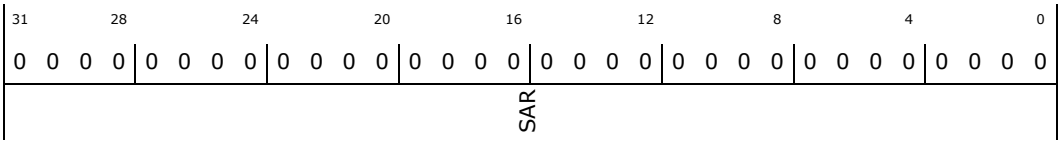
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR2: [BAR + 9C000h] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.28 reg_DAR_type (DAR2)—Offset B8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

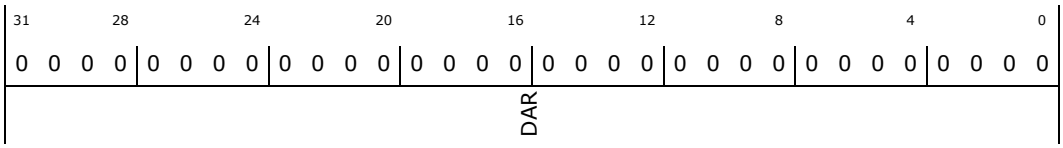
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR2: [BAR + 9C000h] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.29 reg_LLP_type (LLP2)—Offset C0h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

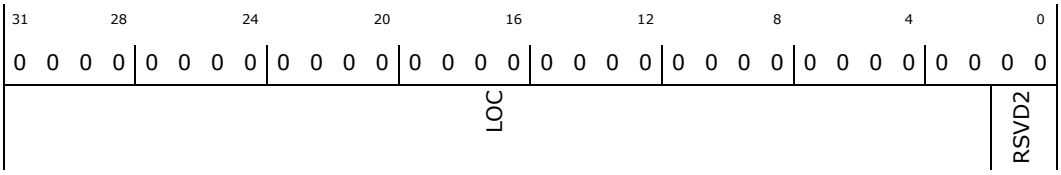
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP2: [BAR + 9C000h] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.22.30 reg_CTL_LO_type (CTL_LO2)—Offset C8h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

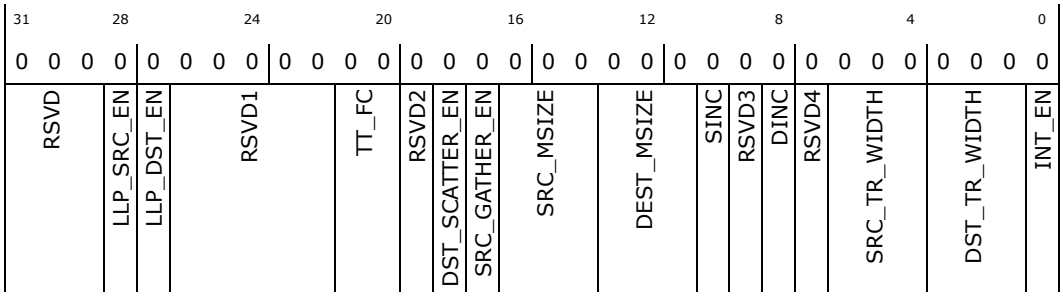
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

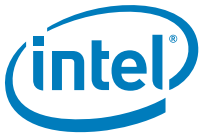
CTL_LO2: [BAR + 9C000h] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved



Bit Range	Default & Access	Description
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.22.31 reg_CTL_HI_type (CTL_HI2)—Offset CCh

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

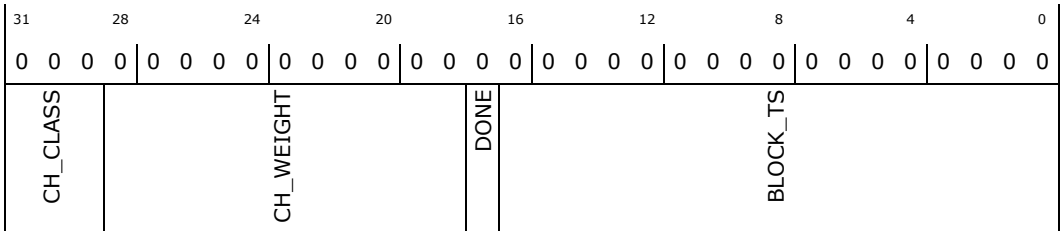
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI2: [BAR + 9C000h] + CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.22.32 reg_SSTAT_type (SSTAT2)—Offset D0h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

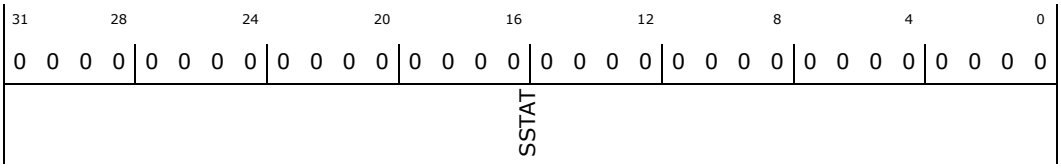
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT2: [BAR + 9C000h] + D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.22.33 reg_DSTAT_type (DSTAT2)—Offset D8h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

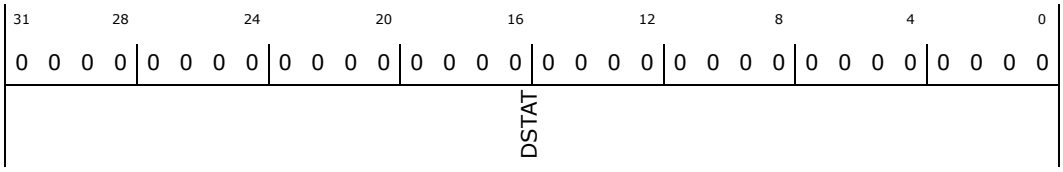
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT2: [BAR + 9C000h] + D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.22.34 reg_SSTATAR_type (SSTATAR2)—Offset E0h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

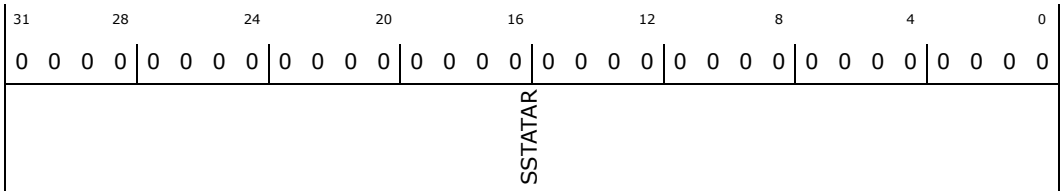
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR2: [BAR + 9C000h] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.22.35 reg_DSTATAR_type (DSTATAR2)—Offset E8h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

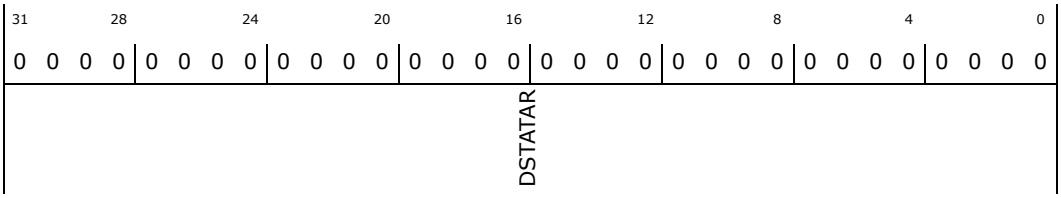
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR2: [BAR + 9C000h] + E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.22.36 reg_CFG_LO_type (CFG_LO2)—Offset F0h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

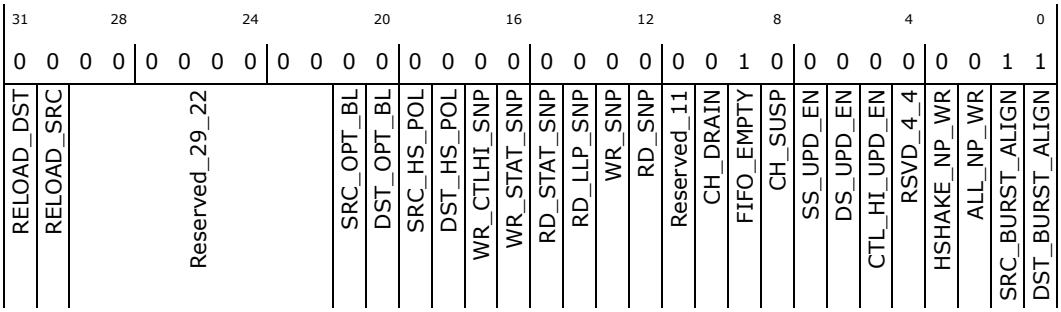
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

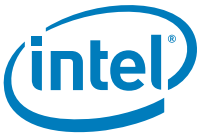
CFG_LO2: [BAR + 9C000h] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.



Bit Range	Default & Access	Description
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.22.37 reg_CFG_HI_type (CFG_HI2)—Offset F4h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

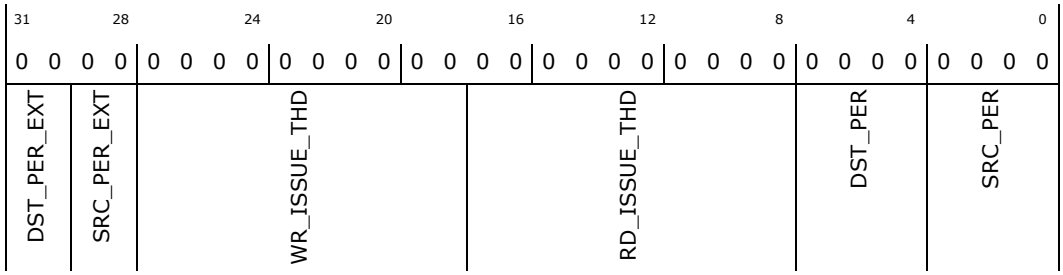
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI2: [BAR + 9C000h] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.22.38 reg_SGR_type (SGR2)—Offset F8h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

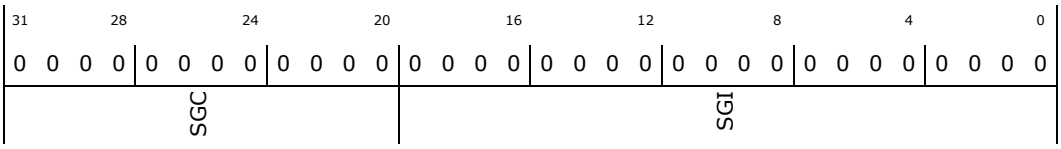
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR2: [BAR + 9C000h] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.22.39 reg_DSR_type (DSR2)—Offset 100h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

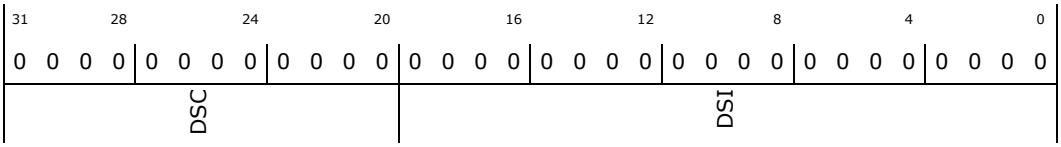
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR2: [BAR + 9C000h] + 100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.22.40 reg_SAR_type (SAR3)—Offset 108h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

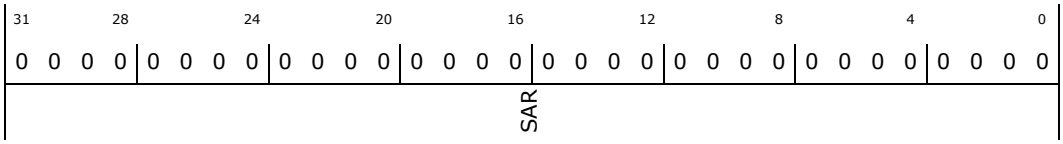
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR3: [BAR + 9C000h] + 108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.41 reg_DAR_type (DAR3)—Offset 110h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

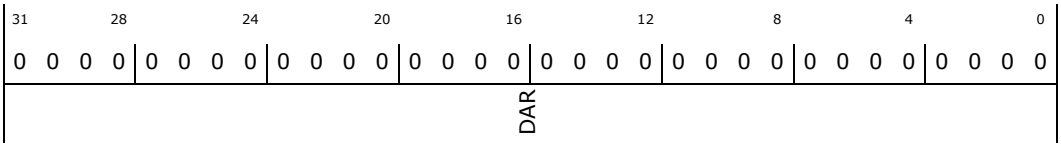
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR3: [BAR + 9C000h] + 110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.42 reg_LLP_type (LLP3)—Offset 118h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

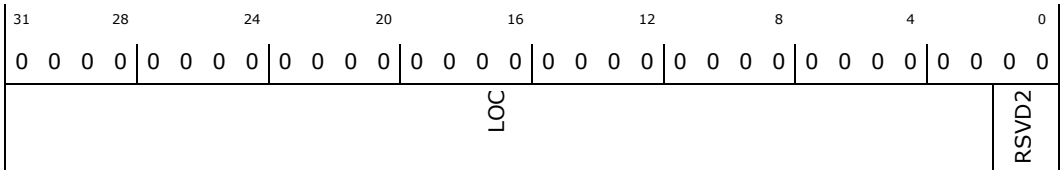
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP3: [BAR + 9C000h] + 118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.22.43 reg_CTL_LO_type (CTL_LO3)—Offset 120h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

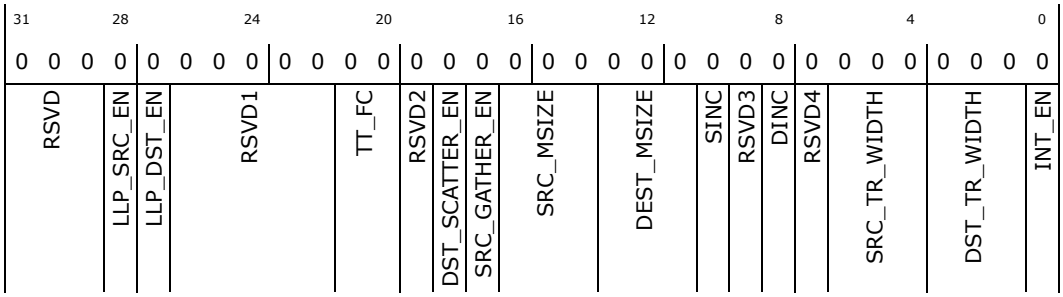
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO3: [BAR + 9C000h] + 120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.

Bit Range	Default & Access	Description
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.22.44 reg_CTL_HI_type (CTL_HI3)—Offset 124h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

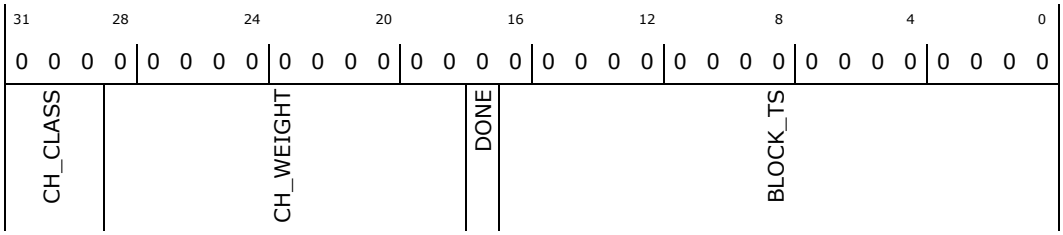
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI3: [BAR + 9C000h] + 124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.

Bit Range	Default & Access	Description
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.22.45 reg_SSTAT_type (SSTAT3)—Offset 128h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

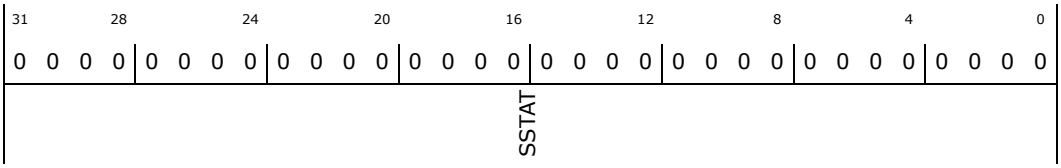
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT3: [BAR + 9C000h] + 128h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.22.46 reg_DSTAT_type (DSTAT3)—Offset 130h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

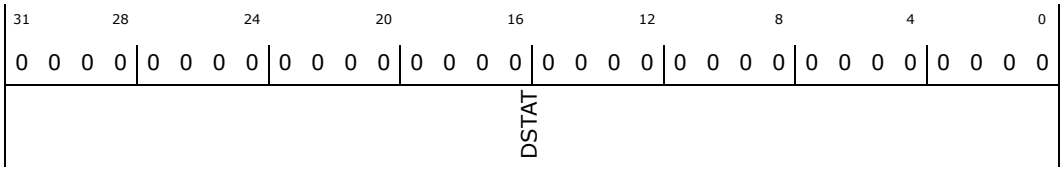
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT3: [BAR + 9C000h] + 130h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.22.47 reg_SSTATAR_type (SSTATAR3)—Offset 138h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

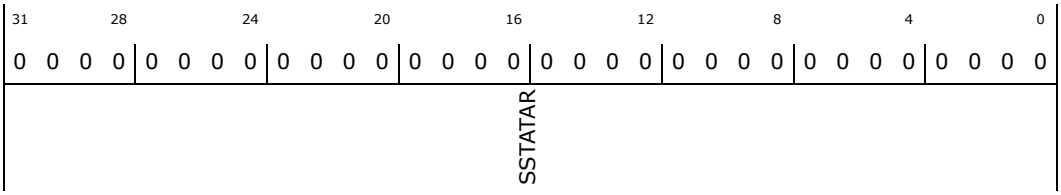
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR3: [BAR + 9C000h] + 138h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.22.48 reg_DSTATAR_type (DSTATAR3)—Offset 140h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

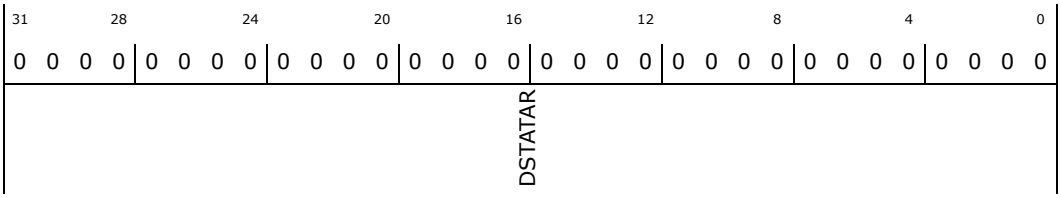
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR3: [BAR + 9C000h] + 140h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.22.49 reg_CFG_LO_type (CFG_LO3)—Offset 148h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

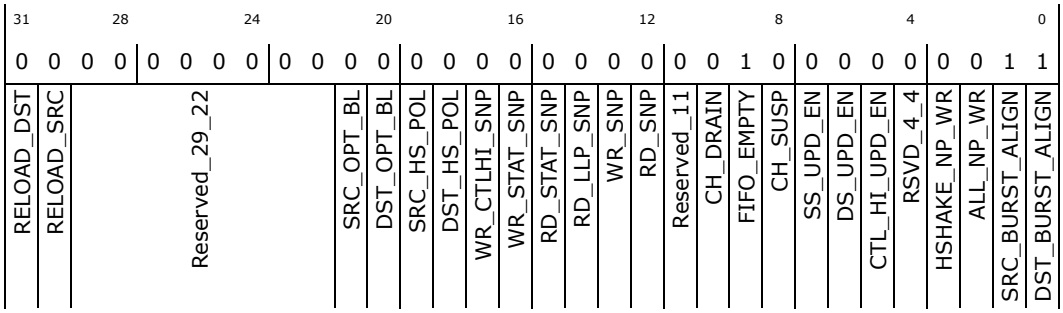
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

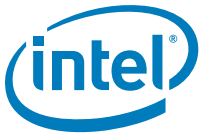
CFG_LO3: [BAR + 9C000h] + 148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port



Bit Range	Default & Access	Description
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.22.50 reg_CFG_HI_type (CFG_HI3)—Offset 14Ch

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

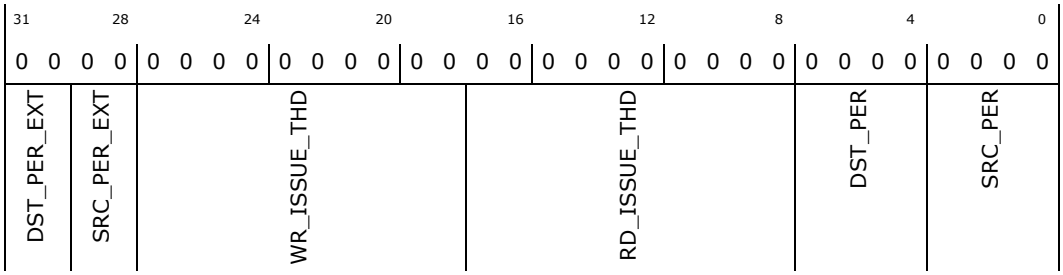
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI3: [BAR + 9C000h] + 14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.22.51 reg_SGR_type (SGR3)—Offset 150h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

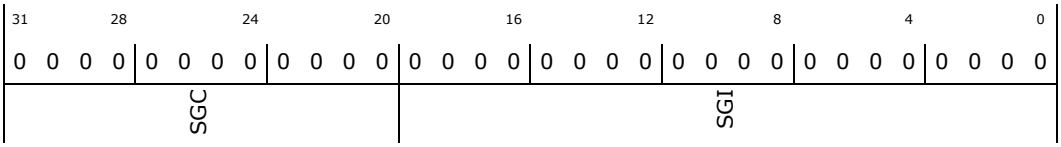
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR3: [BAR + 9C000h] + 150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.22.52 reg_DSR_type (DSR3)—Offset 158h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

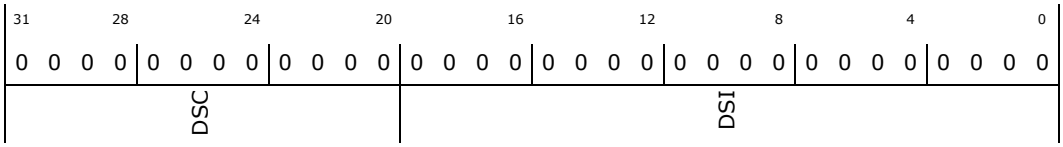
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR3: [BAR + 9C000h] + 158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.22.53 reg_SAR_type (SAR4)—Offset 160h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

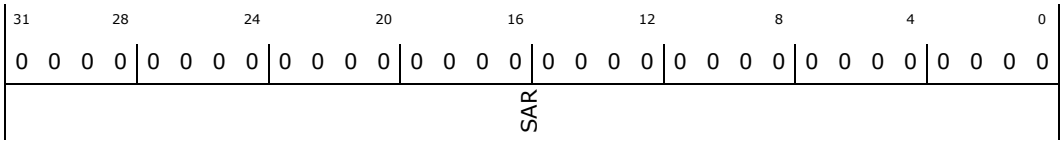
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR4: [BAR + 9C000h] + 160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.54 reg_DAR_type (DAR4)—Offset 168h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

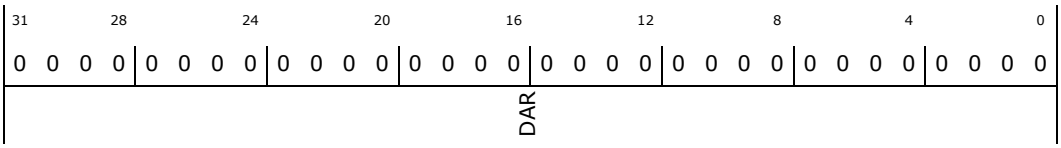
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR4: [BAR + 9C000h] + 168h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.55 reg_LLP_type (LLP4)—Offset 170h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

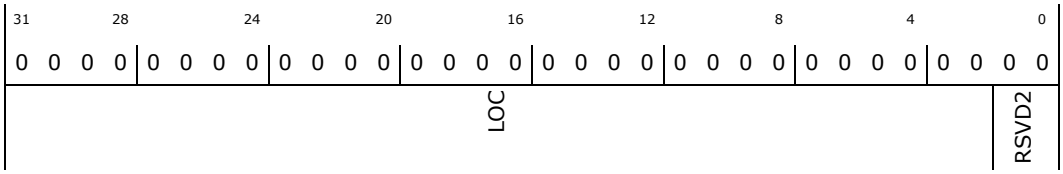
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP4: [BAR + 9C000h] + 170h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.22.56 reg_CTL_LO_type (CTL_LO4)—Offset 178h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

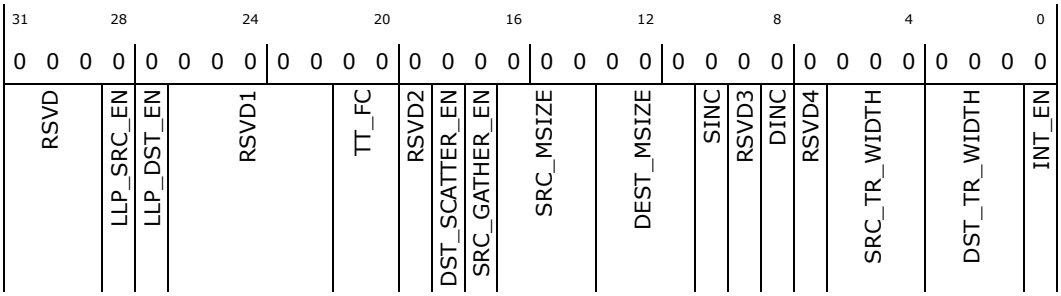
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO4: [BAR + 9C000h] + 178h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved

Bit Range	Default & Access	Description
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.22.57 reg_CTL_HI_type (CTL_HI4)—Offset 17Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

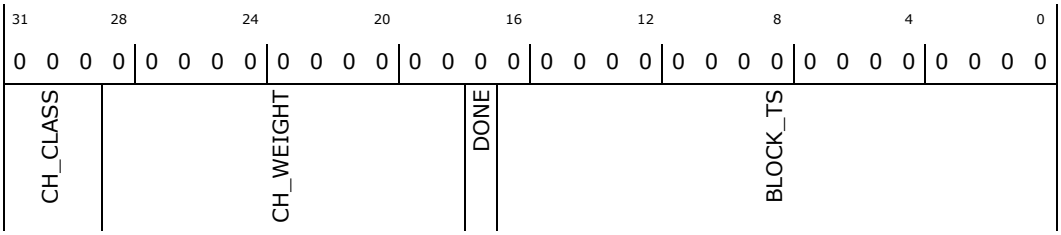
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI4: [BAR + 9C000h] + 17Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.22.58 reg_SSTAT_type (SSTAT4)—Offset 180h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

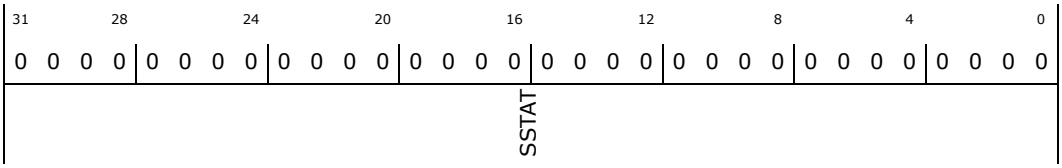
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT4: [BAR + 9C000h] + 180h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.22.59 reg_DSTAT_type (DSTAT4)—Offset 188h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

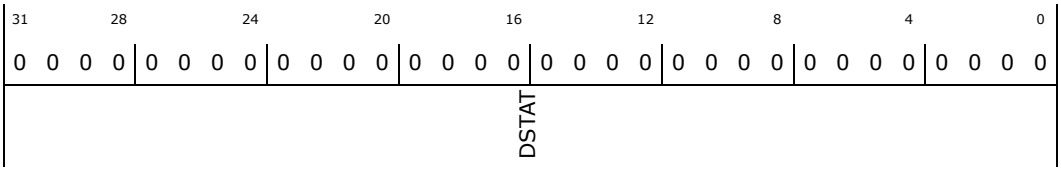
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT4: [BAR + 9C000h] + 188h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.22.60 reg_SSTATAR_type (SSTATAR4)—Offset 190h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

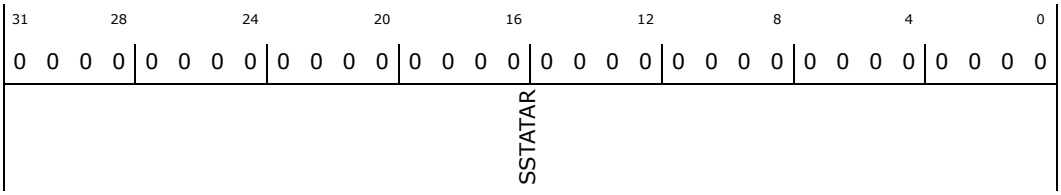
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR4: [BAR + 9C000h] + 190h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.22.61 reg_DSTATAR_type (DSTATAR4)—Offset 198h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

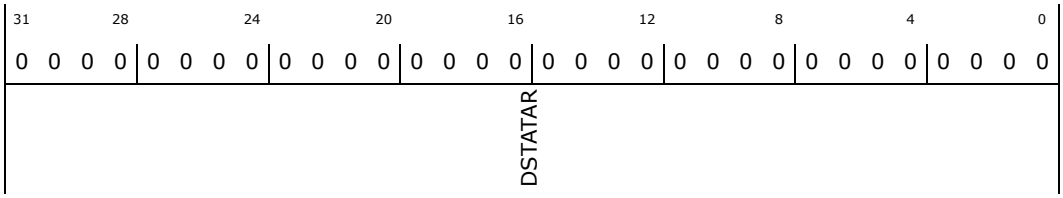
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR4: [BAR + 9C000h] + 198h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.22.62 reg_CFG_LO_type (CFG_LO4)—Offset 1A0h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

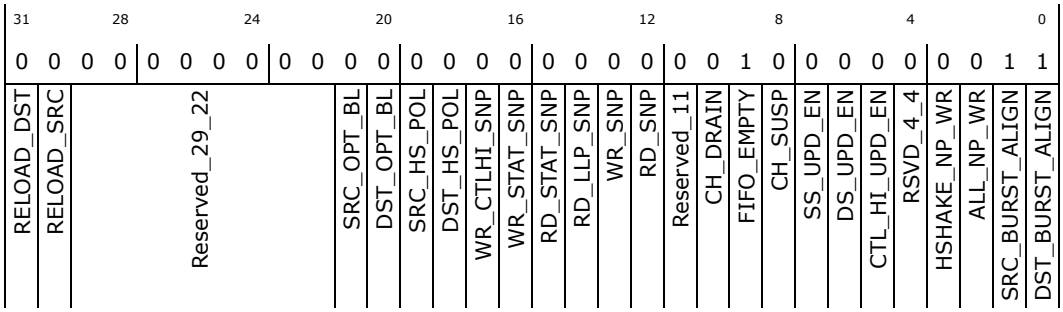
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO4: [BAR + 9C000h] + 1A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.

Bit Range	Default & Access	Description
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.22.63 reg_CFG_HI_type (CFG_HI4)—Offset 1A4h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

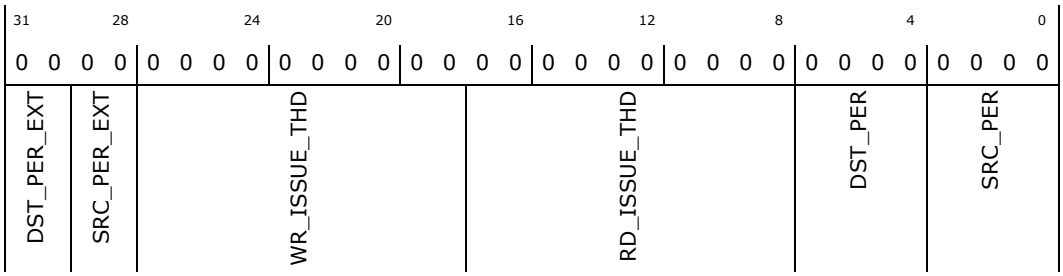
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI4: [BAR + 9C000h] + 1A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.22.64 reg_SGR_type (SGR4)—Offset 1A8h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

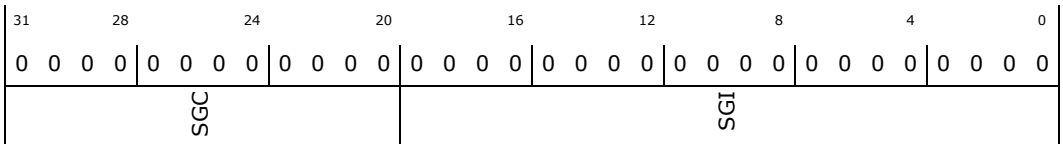
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR4: [BAR + 9C000h] + 1A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.22.65 reg_DSR_type (DSR4)—Offset 1B0h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

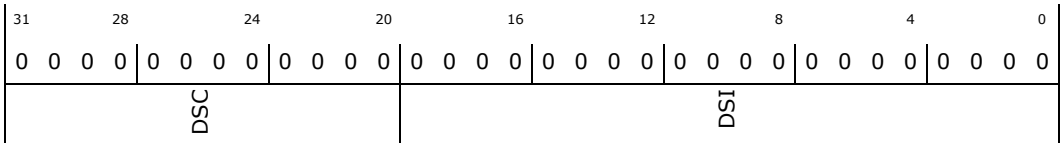
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR4: [BAR + 9C000h] + 1B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.22.66 reg_SAR_type (SAR5)—Offset 1B8h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

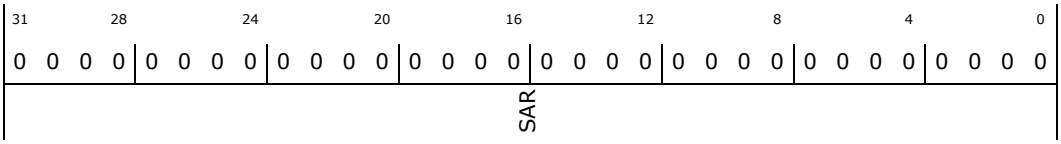
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR5: [BAR + 9C000h] + 1B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.67 reg_DAR_type (DAR5)—Offset 1C0h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

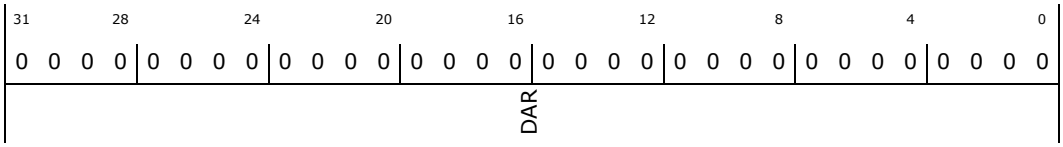
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR5: [BAR + 9C000h] + 1C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.68 reg_LLP_type (LLP5)—Offset 1C8h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

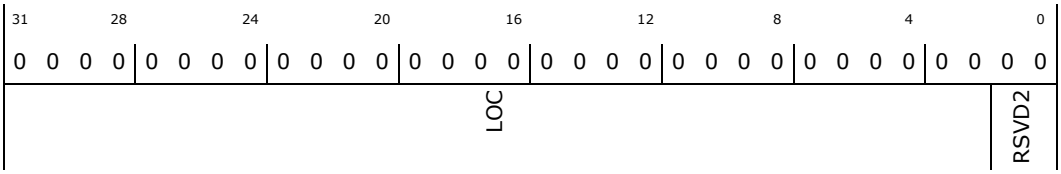
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP5: [BAR + 9C000h] + 1C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.22.69 reg_CTL_LO_type (CTL_LO5)—Offset 1D0h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

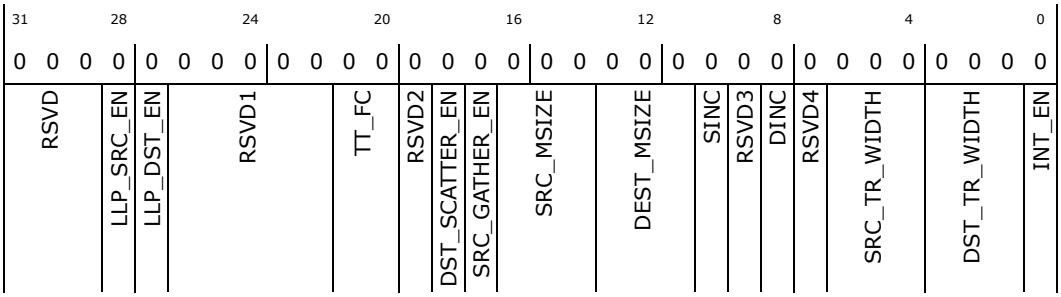
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

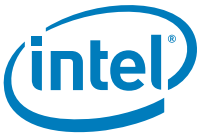
CTL_LO5: [BAR + 9C000h] + 1D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved



Bit Range	Default & Access	Description
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.

Bit Range	Default & Access	Description
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.22.70 reg_CTL_HI_type (CTL_HI5)—Offset 1D4h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

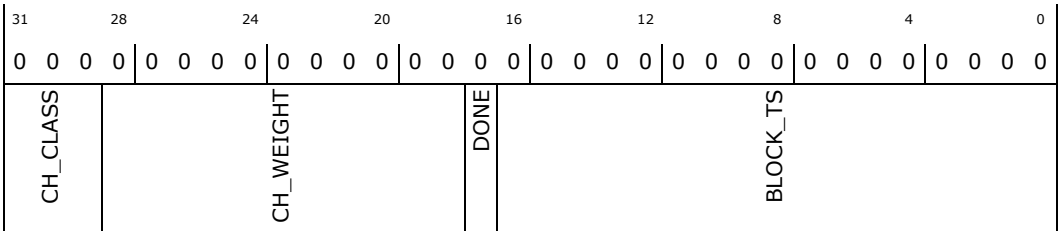
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI5: [BAR + 9C000h] + 1D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.

Bit Range	Default & Access	Description
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.22.71 reg_SSTAT_type (SSTAT5)—Offset 1D8h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

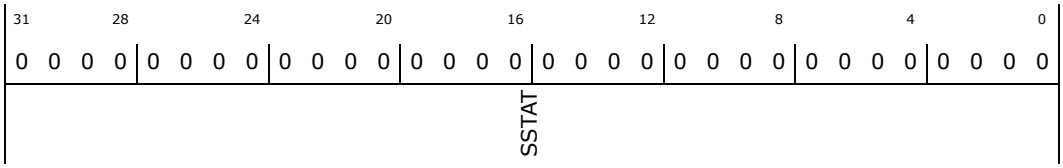
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT5: [BAR + 9C000h] + 1D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.22.72 reg_DSTAT_type (DSTAT5)—Offset 1E0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

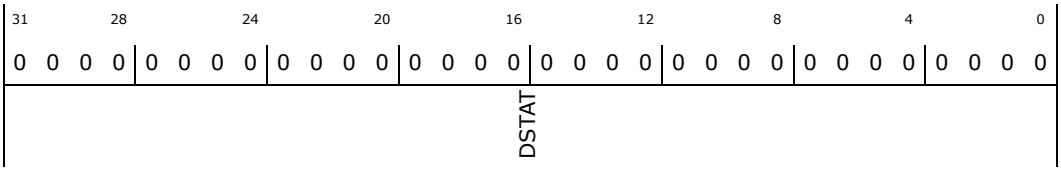
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT5: [BAR + 9C000h] + 1E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.22.73 reg_SSTATAR_type (SSTATAR5)—Offset 1E8h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

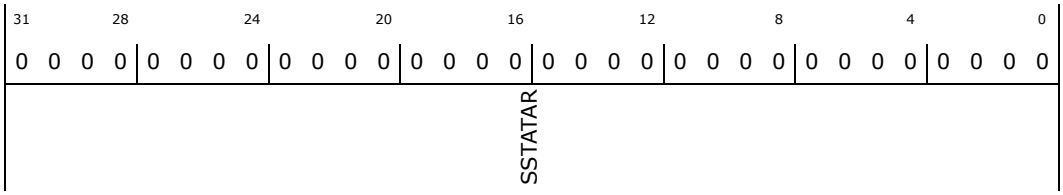
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR5: [BAR + 9C000h] + 1E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.22.74 reg_DSTATAR_type (DSTATAR5)—Offset 1F0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

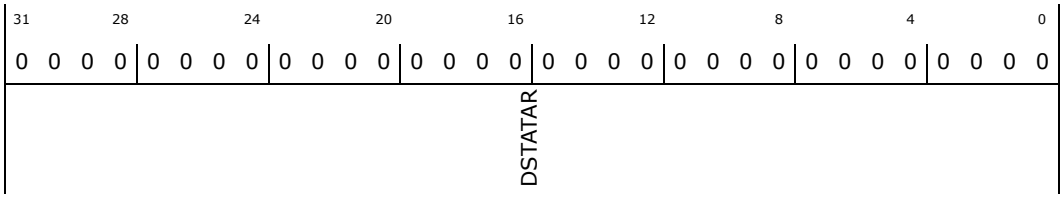
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR5: [BAR + 9C000h] + 1F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.22.75 reg_CFG_LO_type (CFG_LO5)—Offset 1F8h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

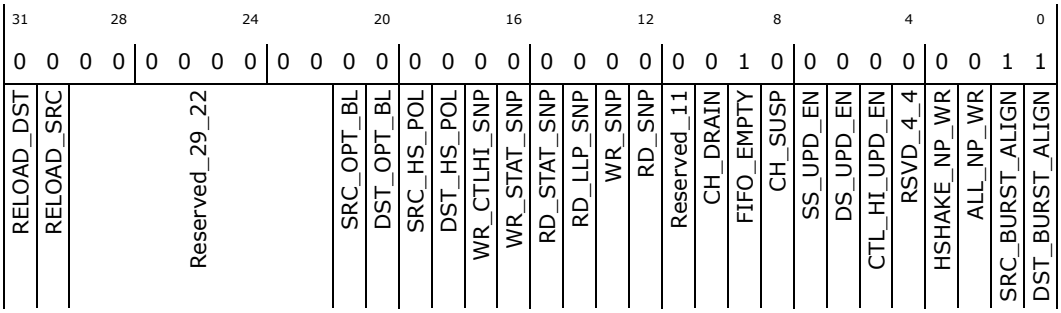
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO5: [BAR + 9C000h] + 1F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port

Bit Range	Default & Access	Description
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.22.76 reg_CFG_HI_type (CFG_HI5)—Offset 1FCh

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

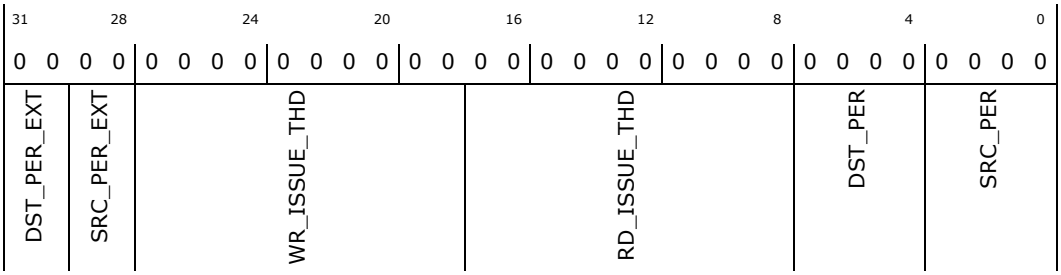
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

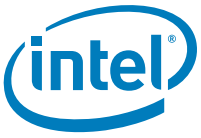
CFG_HI5: [BAR + 9C000h] + 1FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS



3.22.77 reg_SGR_type (SGR5)—Offset 200h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

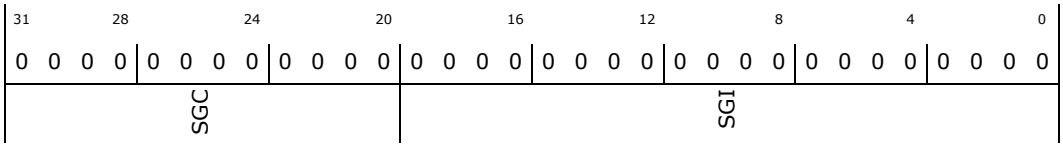
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR5: [BAR + 9C000h] + 200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.22.78 reg_DSR_type (DSR5)—Offset 208h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

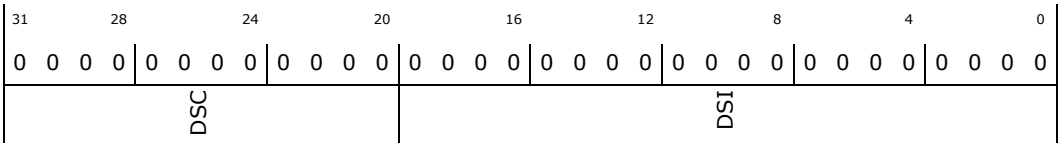
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR5: [BAR + 9C000h] + 208h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.22.79 reg_SAR_type (SAR6)—Offset 210h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

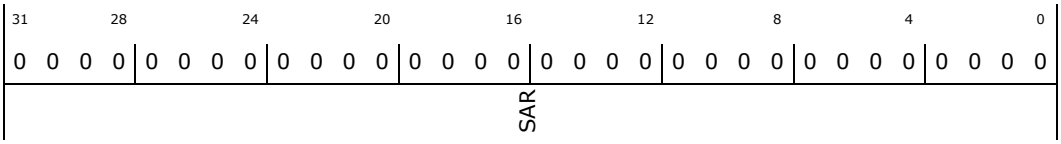
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR6: [BAR + 9C000h] + 210h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.80 reg_DAR_type (DAR6)—Offset 218h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

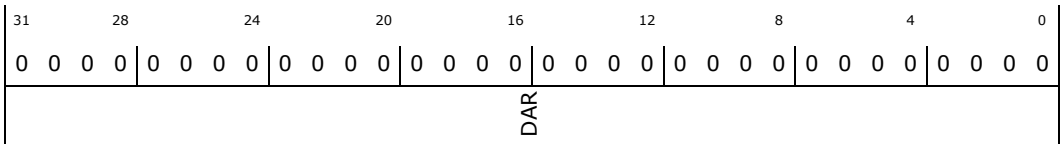
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR6: [BAR + 9C000h] + 218h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.81 reg_LLP_type (LLP6)—Offset 220h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

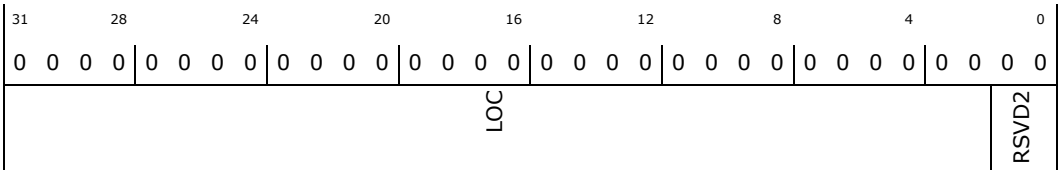
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP6: [BAR + 9C000h] + 220h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.22.82 reg_CTL_LO_type (CTL_LO6)—Offset 228h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

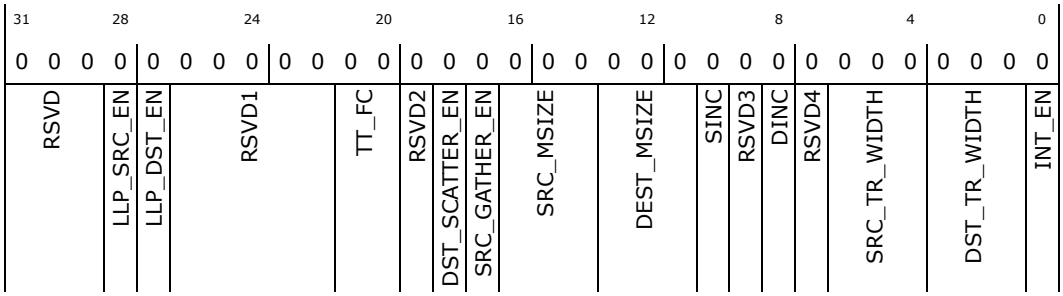
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

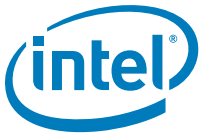
CTL_LO6: [BAR + 9C000h] + 228h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved



Bit Range	Default & Access	Description
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.22.83 reg_CTL_HI_type (CTL_HI6)—Offset 22Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

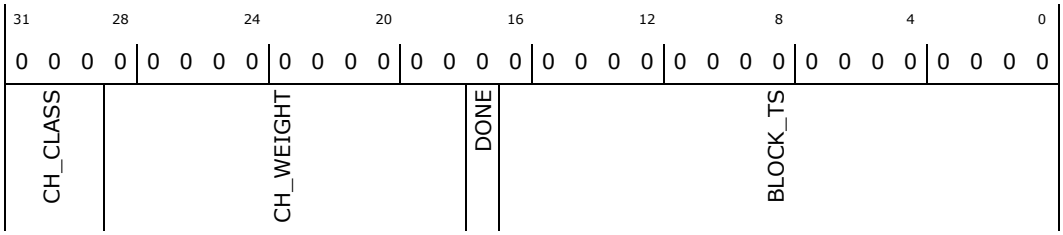
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI6: [BAR + 9C000h] + 22Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.22.84 reg_SSTAT_type (SSTAT6)—Offset 230h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

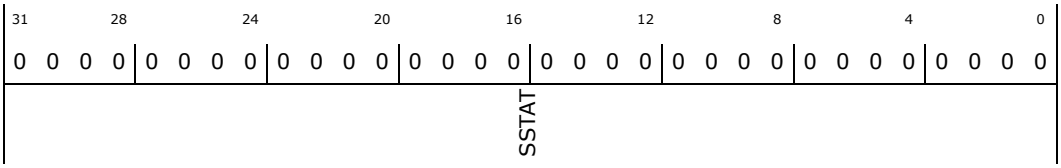
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT6: [BAR + 9C000h] + 230h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.22.85 reg_DSTAT_type (DSTAT6)—Offset 238h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

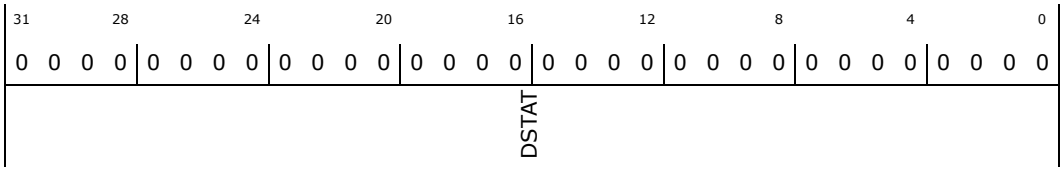
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT6: [BAR + 9C000h] + 238h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.22.86 reg_SSTATAR_type (SSTATAR6)—Offset 240h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

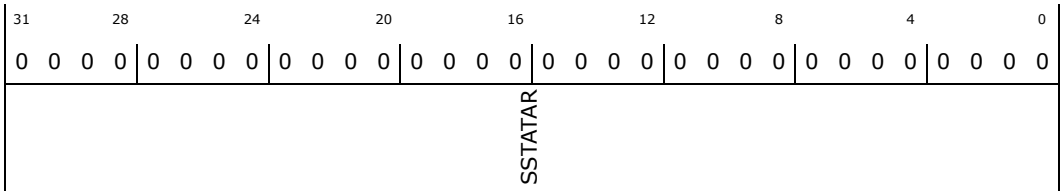
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR6: [BAR + 9C000h] + 240h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.22.87 reg_DSTATAR_type (DSTATAR6)—Offset 248h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

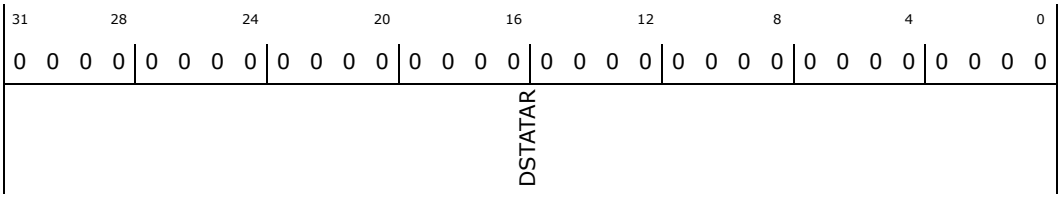
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR6: [BAR + 9C000h] + 248h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.22.88 reg_CFG_LO_type (CFG_LO6)—Offset 250h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

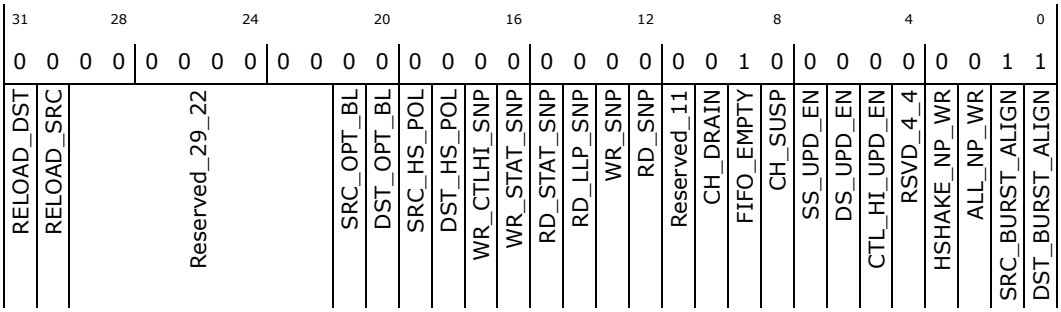
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

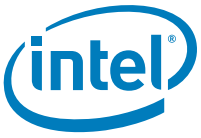
CFG_LO6: [BAR + 9C000h] + 250h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.



Bit Range	Default & Access	Description
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Description
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.22.89 reg_CFG_HI_type (CFG_HI6)—Offset 254h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

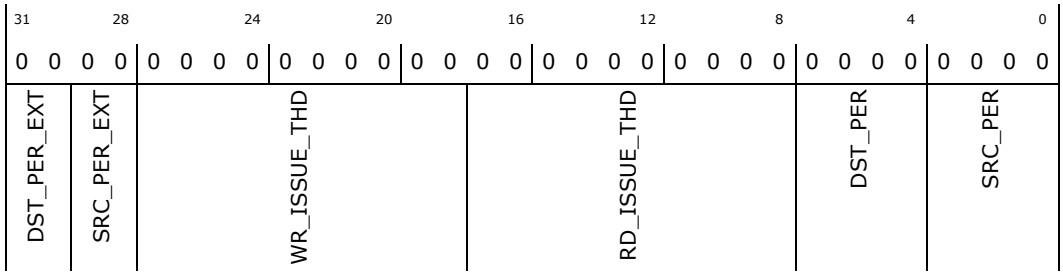
Access Method

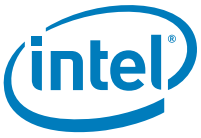
Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI6: [BAR + 9C000h] + 254h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.22.90 reg_SGR_type (SGR6)—Offset 258h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

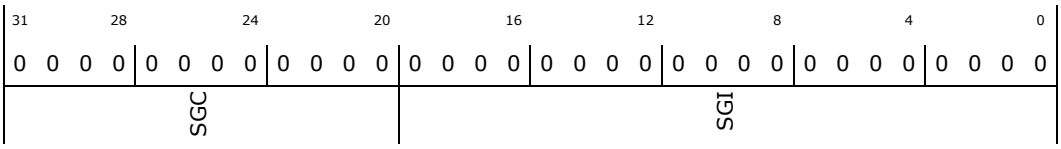
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR6: [BAR + 9C000h] + 258h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.22.91 reg_DSR_type (DSR6)—Offset 260h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

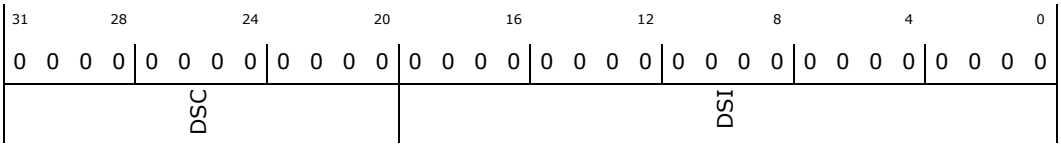
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR6: [BAR + 9C000h] + 260h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.22.92 reg_SAR_type (SAR7)—Offset 268h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

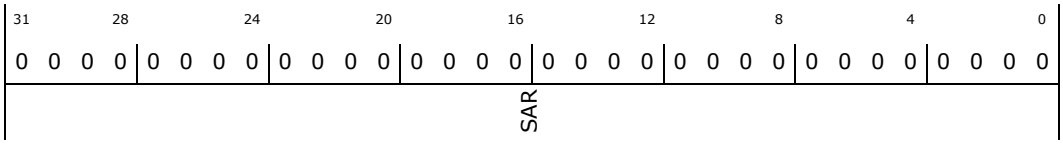
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR7: [BAR + 9C000h] + 268h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.93 reg_DAR_type (DAR7)—Offset 270h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

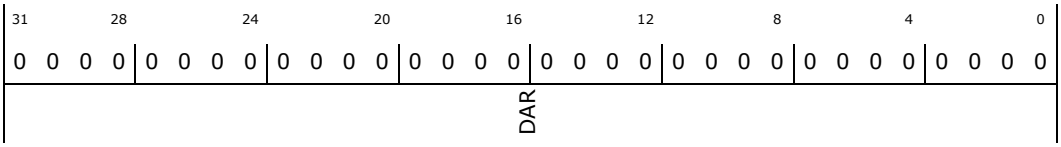
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR7: [BAR + 9C000h] + 270h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

3.22.94 reg_LLP_type (LLP7)—Offset 278h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

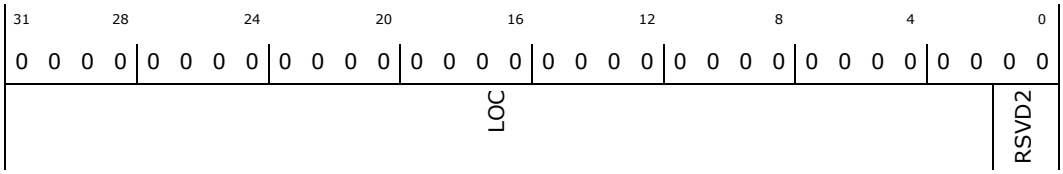
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP7: [BAR + 9C000h] + 278h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

3.22.95 reg_CTL_LO_type (CTL_LO7)—Offset 280h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

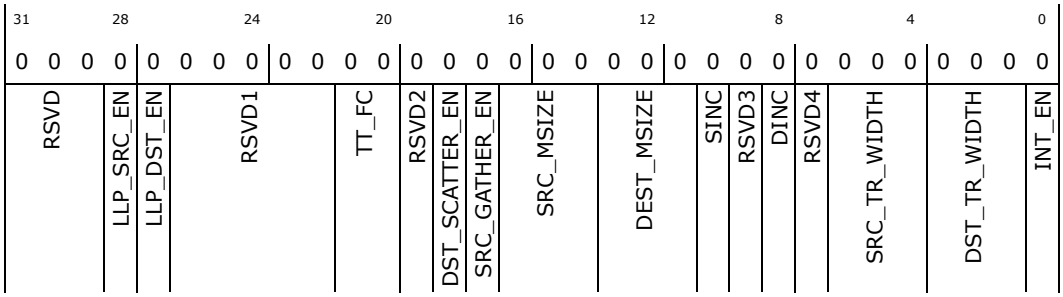
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO7: [BAR + 9C000h] + 280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.

Bit Range	Default & Access	Description
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

3.22.96 reg_CTL_HI_type (CTL_HI7)—Offset 284h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

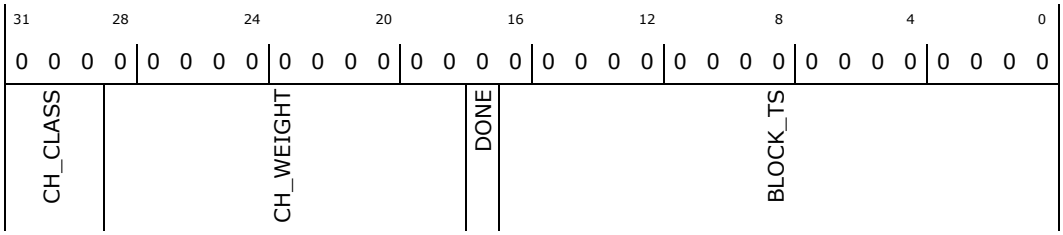
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI7: [BAR + 9C000h] + 284h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.

Bit Range	Default & Access	Description
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

3.22.97 reg_SSTAT_type (SSTAT7)—Offset 288h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

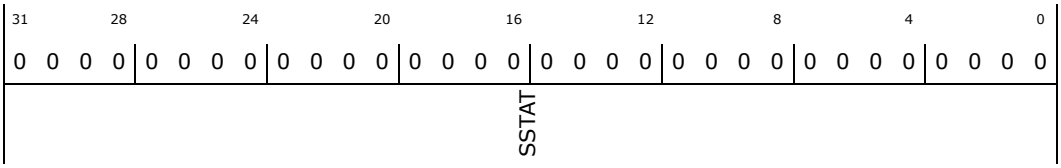
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT7: [BAR + 9C000h] + 288h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

3.22.98 reg_DSTAT_type (DSTAT7)—Offset 290h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

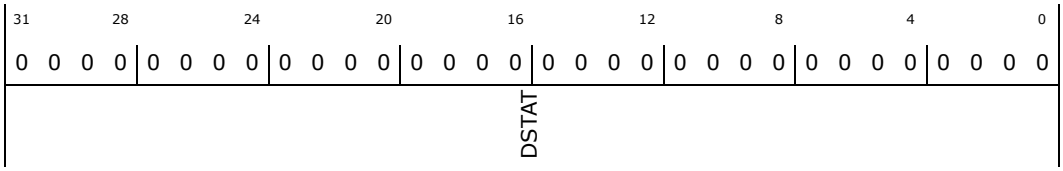
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT7: [BAR + 9C000h] + 290h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

3.22.99 reg_SSTATAR_type (SSTATAR7)—Offset 298h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

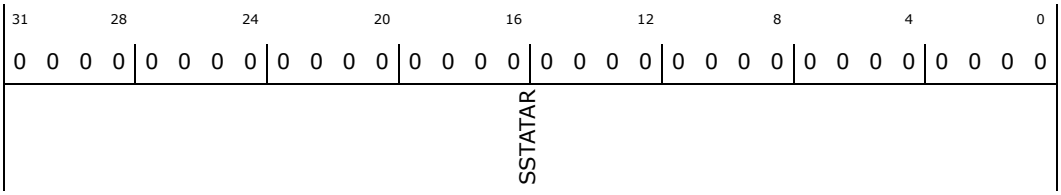
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR7: [BAR + 9C000h] + 298h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

3.22.100 reg_DSTATAR_type (DSTATAR7)—Offset 2A0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

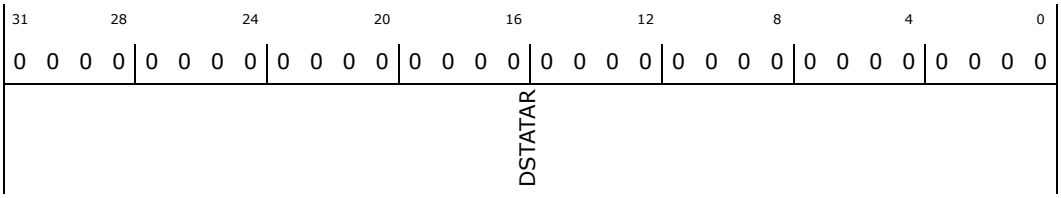
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR7: [BAR + 9C000h] + 2A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

3.22.101 reg_CFG_LO_type (CFG_LO7)—Offset 2A8h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

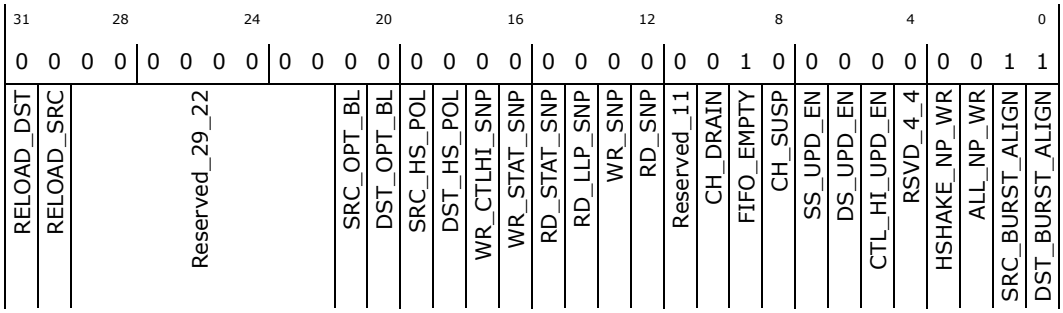
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO7: [BAR + 9C000h] + 2A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h



Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port

Bit Range	Default & Access	Description
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

3.22.102 reg_CFG_HI_type (CFG_HI7)—Offset 2ACh

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

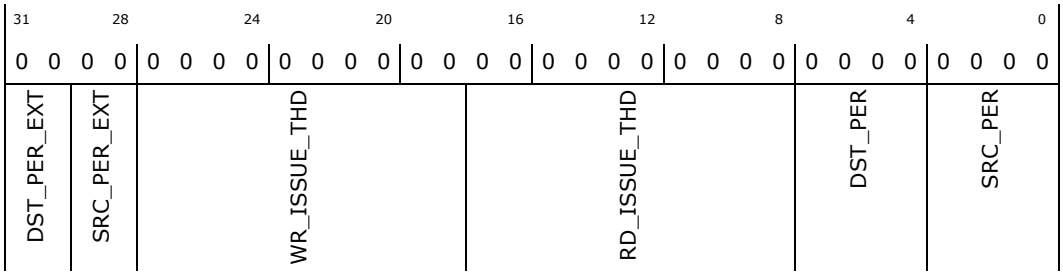
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI7: [BAR + 9C000h] + 2ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

3.22.103 reg_SGR_type (SGR7)—Offset 2B0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

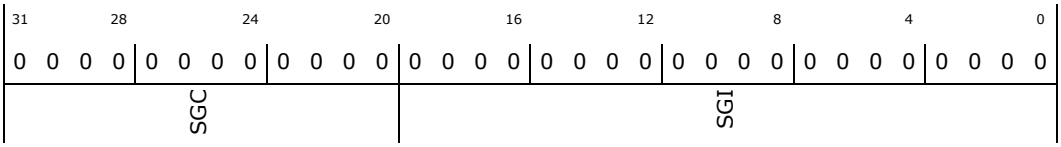
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR7: [BAR + 9C000h] + 2B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

3.22.104 reg_DSR_type (DSR7)—Offset 2B8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

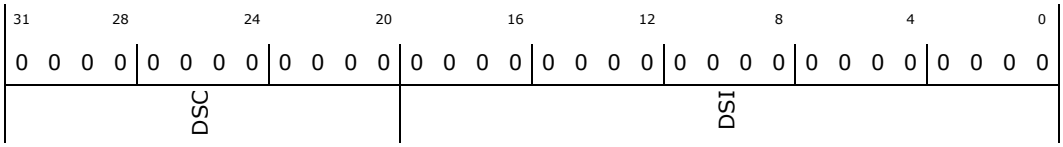
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR7: [BAR + 9C000h] + 2B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

3.22.105 reg_Raw_type (RawTfr)—Offset 2C0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

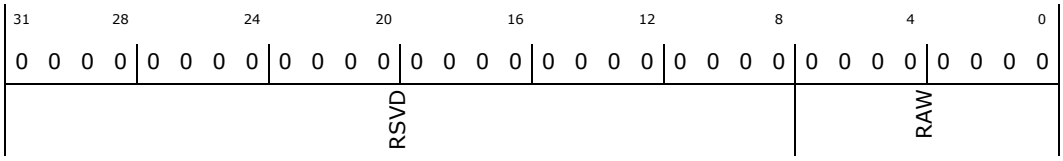
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawTfr: [BAR + 9C000h] + 2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

3.22.106 reg_Raw_type (RawBlock)—Offset 2C8h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

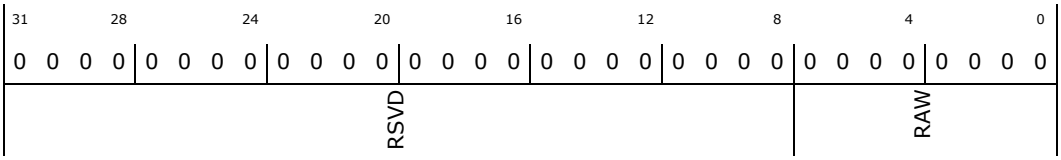
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawBlock: [BAR + 9C000h] + 2C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

3.22.107 reg_Raw_type (RawSrcTran)—Offset 2D0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

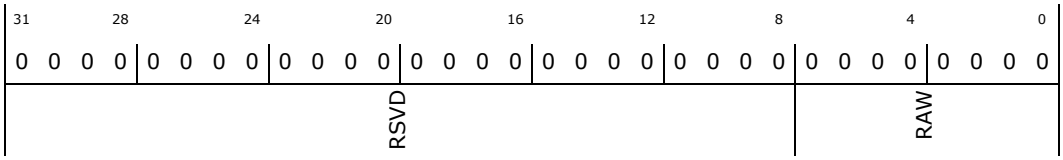
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawSrcTran: [BAR + 9C000h] + 2D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

3.22.108 reg_Raw_type (RawDstTran)—Offset 2D8h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

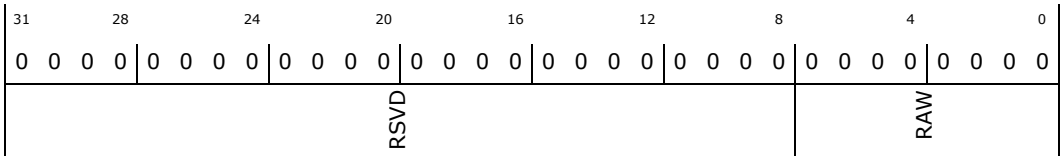
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawDstTran: [BAR + 9C000h] + 2D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
7:0	0h RO	**RAW:** Raw interrupt status

3.22.109 reg_Raw_type (RawErr)—Offset 2E0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

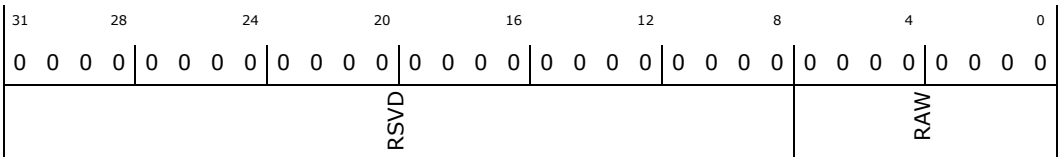
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawErr: [BAR + 9C000h] + 2E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

3.22.110 reg_Status_type (StatusTfr)—Offset 2E8h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

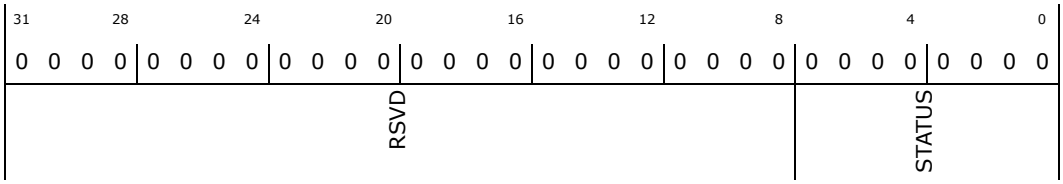
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusTfr: [BAR + 9C000h] + 2E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

3.22.111 reg_Status_type (StatusBlock)—Offset 2F0h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

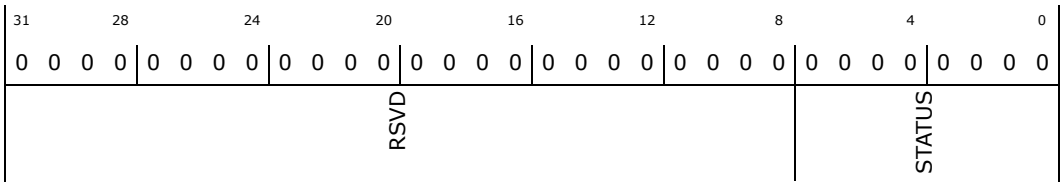
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusBlock: [BAR + 9C000h] + 2F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

3.22.112 reg_Status_type (StatusSrcTran)—Offset 2F8h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

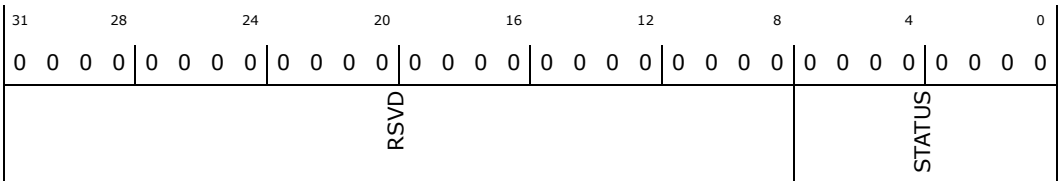
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusSrcTran: [BAR + 9C000h] + 2F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

3.22.113 reg_Status_type (StatusDstTran)—Offset 300h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

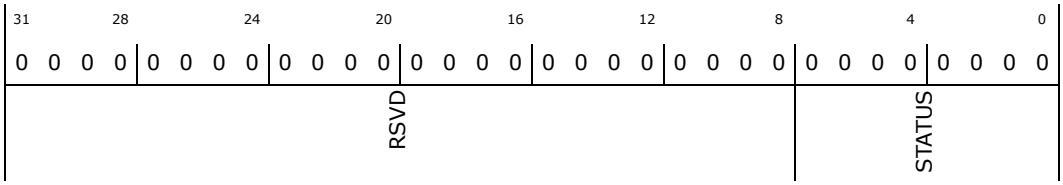
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusDstTran: [BAR + 9C000h] + 300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

3.22.114 reg_Status_type (StatusErr)—Offset 308h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

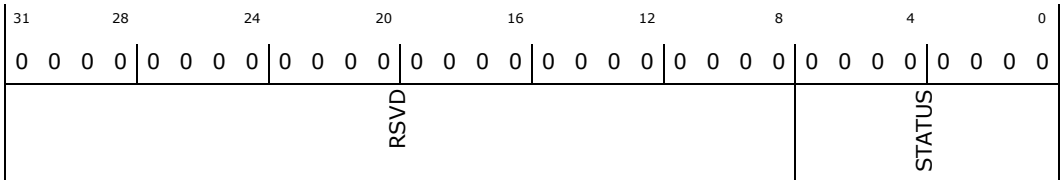
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusErr: [BAR + 9C000h] + 308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

3.22.115 reg_Mask_type (MaskTfr)—Offset 310h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA

channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

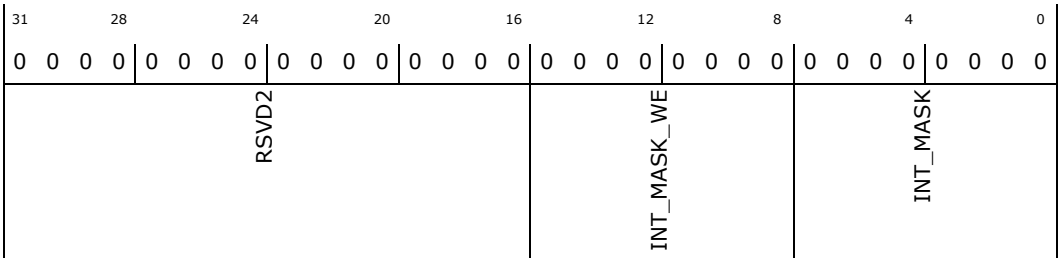
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskTfr: [BAR + 9C000h] + 310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

3.22.116 reg_Mask_type (MaskBlock)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be

masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

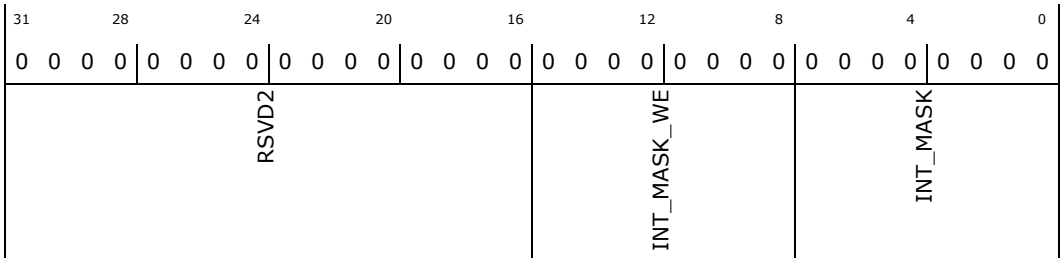
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskBlock: [BAR + 9C000h] + 318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

3.22.117 reg_Mask_type (MaskSrcTran)—Offset 320h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation.

For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

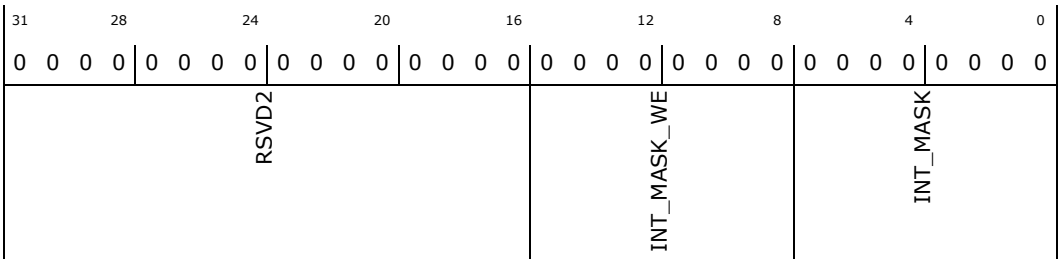
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskSrcTran: [BAR + 9C000h] + 320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

3.22.118 reg_Mask_type (MaskDstTran)—Offset 328h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

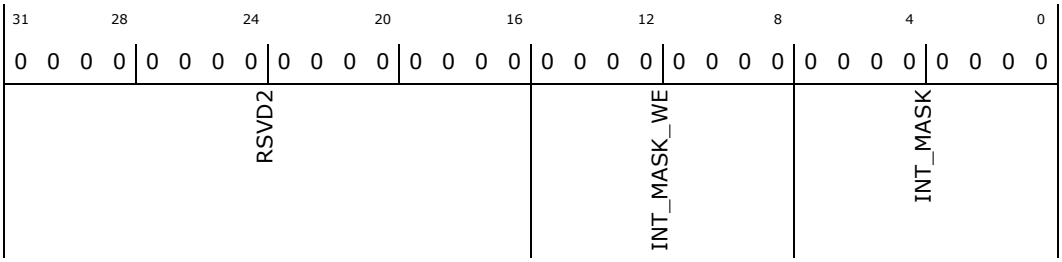
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskDstTran: [BAR + 9C000h] + 328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

3.22.119 reg_Mask_type (MaskErr)—Offset 330h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

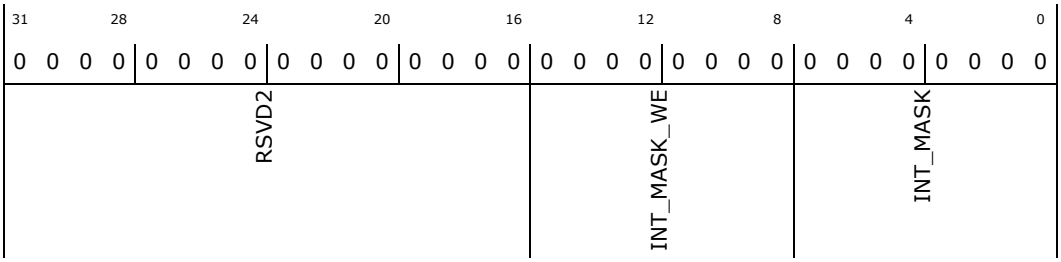
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskErr: [BAR + 9C000h] + 330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

3.22.120 reg_Clear_type (ClearTfr)—Offset 338h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

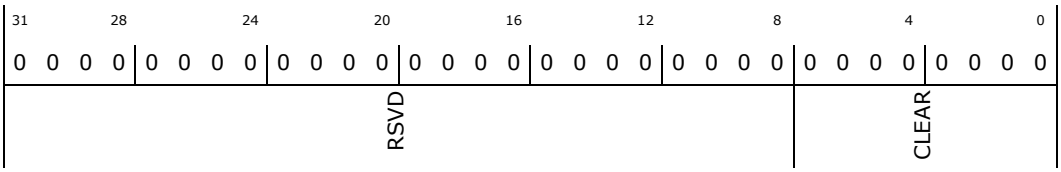
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearTfr: [BAR + 9C000h] + 338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

3.22.121 reg_Clear_type (ClearBlock)—Offset 340h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

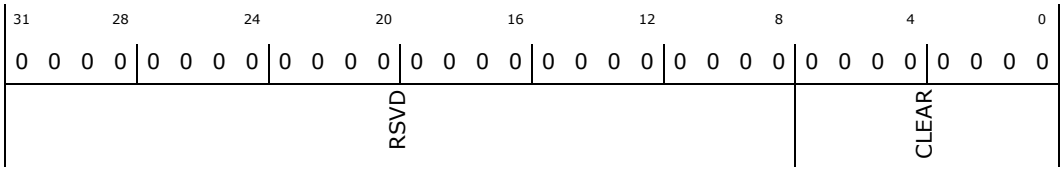
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearBlock: [BAR + 9C000h] + 340h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

3.22.122 reg_Clear_type (ClearSrcTran)—Offset 348h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

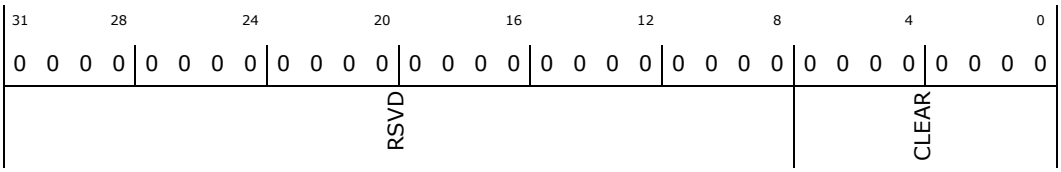
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearSrcTran: [BAR + 9C000h] + 348h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

3.22.123 reg_Clear_type (ClearDstTran)—Offset 350h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

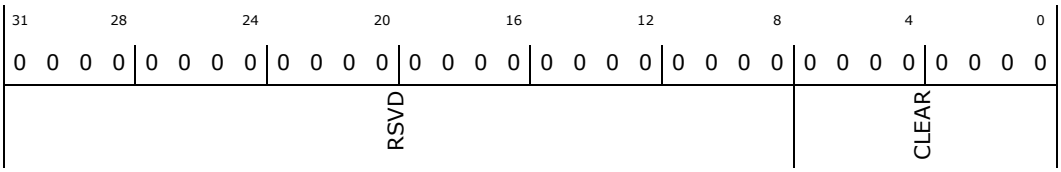
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearDstTran: [BAR + 9C000h] + 350h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

3.22.124 reg_Clear_type (ClearErr)—Offset 358h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

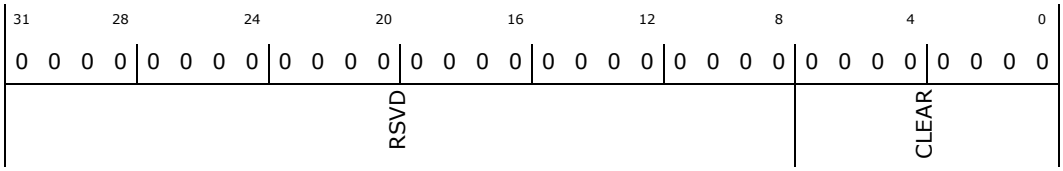
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearErr: [BAR + 9C000h] + 358h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

3.22.125 reg_StatusInt_type (StatusInt)—Offset 360h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

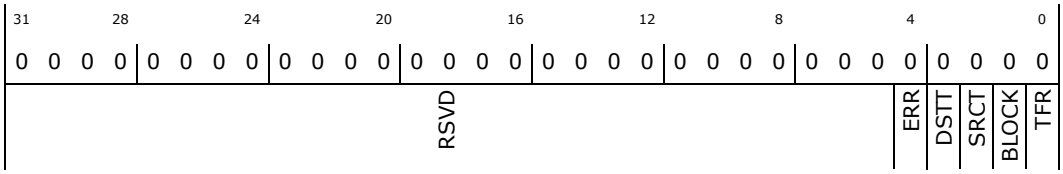
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusInt: [BAR + 9C000h] + 360h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RO	**RSVD:** Reserved
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register

Bit Range	Default & Access	Description
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

3.22.126 reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

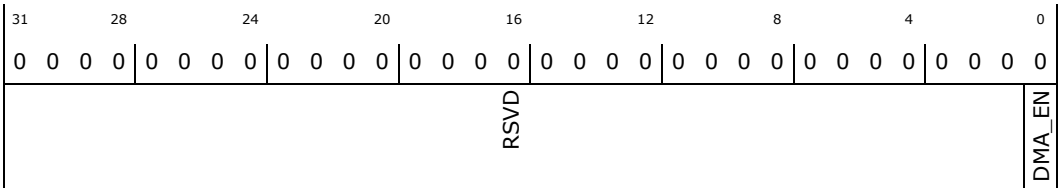
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaCfgReg: [BAR + 9C000h] + 398h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RO	**RSVD:** Reserved
0	0h RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

3.22.127 reg_ChEnReg_type (ChEnReg)—Offset 3A0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged. Note that a read-modified write is not required.

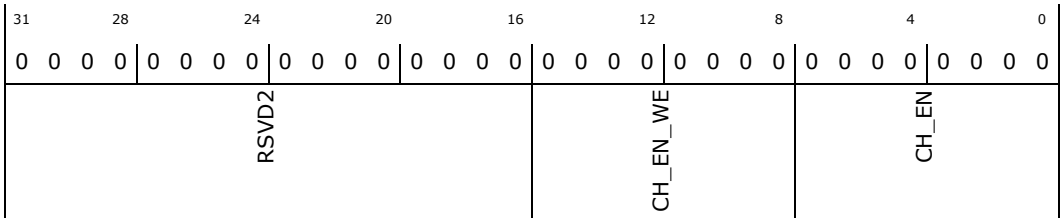
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ChEnReg: [BAR + 9C000h] + 3A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**CH_EN_WE:** Channel enable write enable.
7:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

3.22.128 reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h

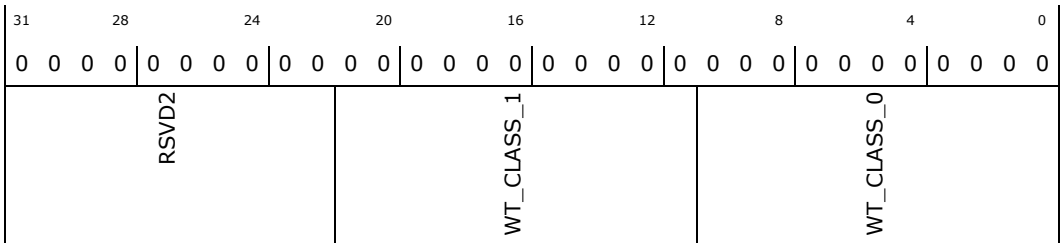
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority0_LO: [BAR + 9C000h] + 3B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RO	**RSVD2:** Reserved
21:11	0h RW	**WT_CLASS_1:** Class Weight 1: Value of K assigns a weight of (K+1) to Class 1. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_0:** Class Weight 0: Value of K assigns a weight of (K+1) to Class 0. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

3.22.129 reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh

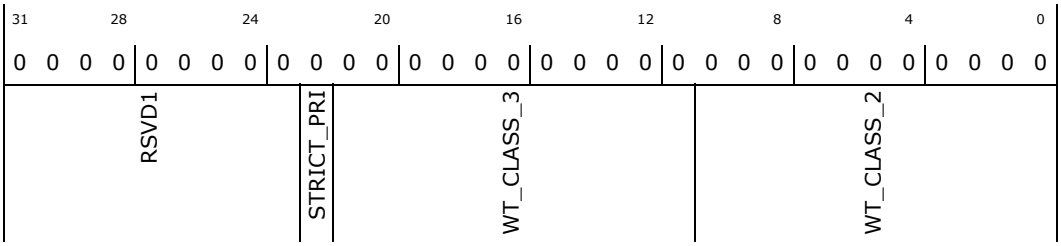
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority0_HI: [BAR + 9C000h] + 3BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RO	**RSVD1:** Reserved
22	0h RW	**STRICT_PRI:** If set, Higher class values will always have higher priorities than lower class values. If not set, round-robin arbitration will be used between different classes using WT_CLASS_n values.
21:11	0h RW	**WT_CLASS_3:** Class Weight 3: Value of K assigns a weight of (K+1) to Class 3. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_2:** Class Weight 2: Value of K assigns a weight of (K+1) to Class 2. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

3.22.130 reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h

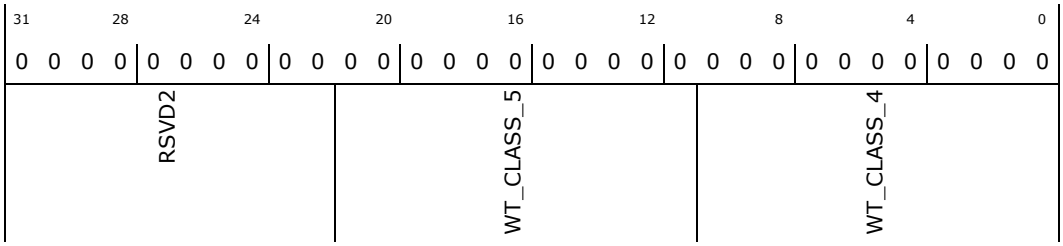
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority1_LO: [BAR + 9C000h] + 3C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RO	**RSVD2:** Reserved
21:11	0h RW	**WT_CLASS_5:** Class Weight 5: Value of K assigns a weight of (K+1) to Class 5. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_4:** Class Weight 4: Value of K assigns a weight of (K+1) to Class 4. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

3.22.131 reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h

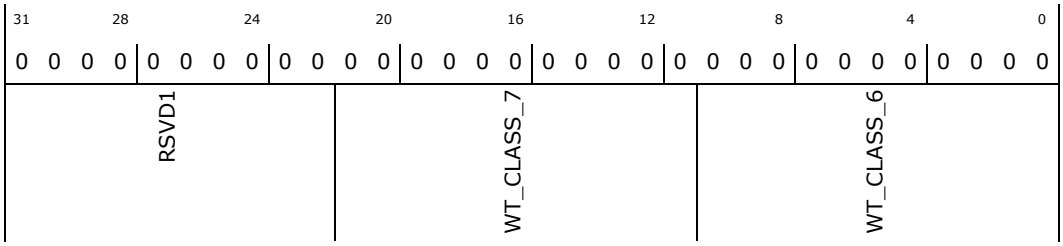
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority1_HI: [BAR + 9C000h] + 3C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RO	**RSVD1:** Reserved

Bit Range	Default & Access	Description
21:11	0h RW	**WT_CLASS_7:** Class Weight 7: Value of K assigns a weight of (K+1) to Class 7. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_6:** Class Weight 6: Value of K assigns a weight of (K+1) to Class 6. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

3.22.132 reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h

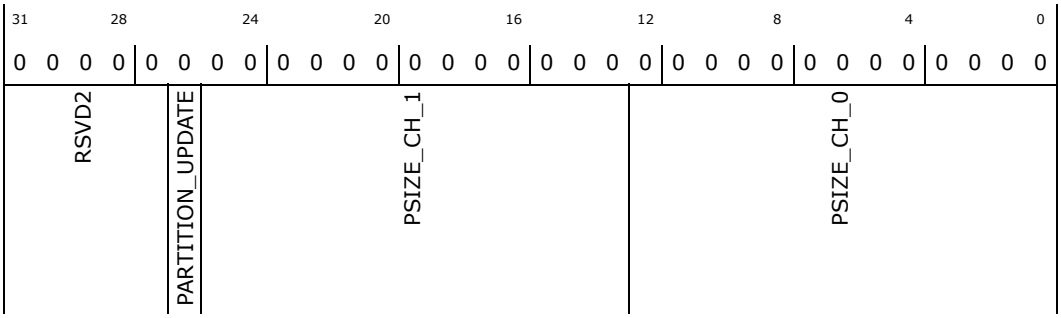
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FifoPartition0_LO: [BAR + 9C000h] + 400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:27	0h RO	**RSVD2:** Reserved
26	0h RW	**PARTITION_UPDATE:** SW needs to write to this bit for the partitioning assignments to take effect.
25:13	0h RW	**PSIZE_CH_1:** Partition Byte Size assigned to Channel 1. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_0:** Partition Byte Size assigned to Channel 0. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

3.22.133 reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h

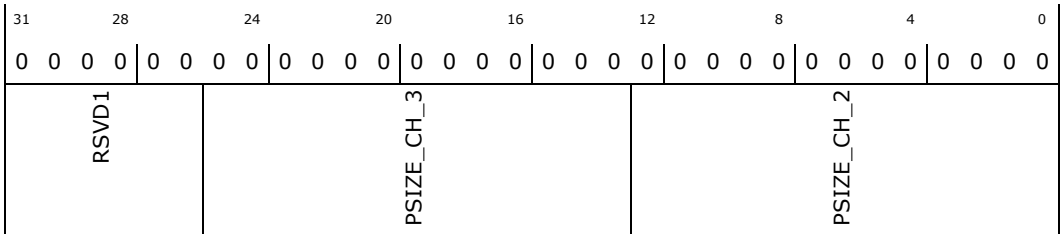
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FifoPartition0_HI: [BAR + 9C000h] + 404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0h RO	**RSVD1:** Reserved
25:13	0h RW	**PSIZE_CH_3:** Partition Byte Size assigned to Channel 3. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_2:** Partition Byte Size assigned to Channel 2. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

3.22.134 reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h

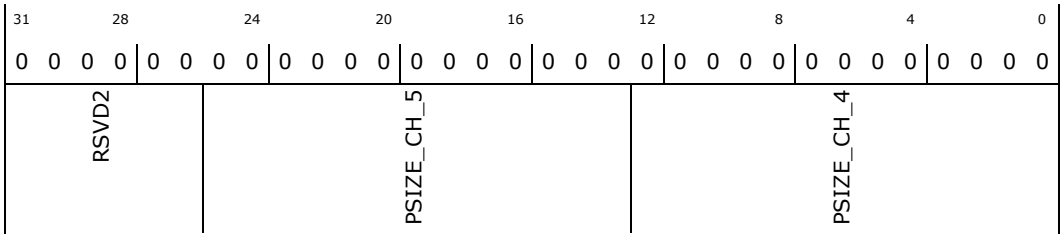
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FifoPartition1_LO: [BAR + 9C000h] + 408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0h RO	**RSVD2:** Reserved

Bit Range	Default & Access	Description
25:13	0h RW	**PSIZE_CH_5:** Partition Byte Size assigned to Channel 5. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_4:** Partition Byte Size assigned to Channel 4. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

3.22.135 reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch

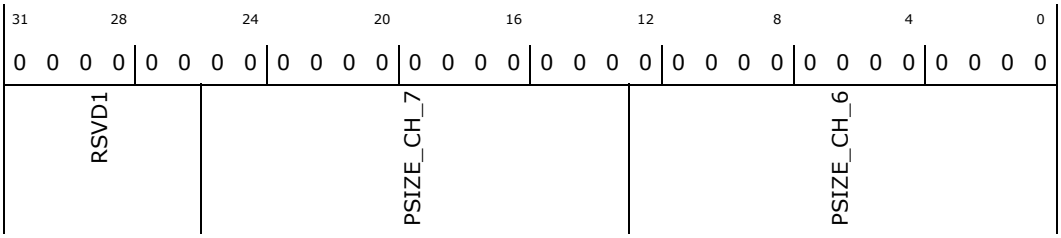
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FifoPartition1_HI: [BAR + 9C000h] + 40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0h RO	**RSVD1:** Reserved
25:13	0h RW	**PSIZE_CH_7:** Partition Byte Size assigned to Channel 7. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_6:** Partition Byte Size assigned to Channel 6. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

3.22.136 reg_SAI_Error_type (SAI_ERR)—Offset 410h

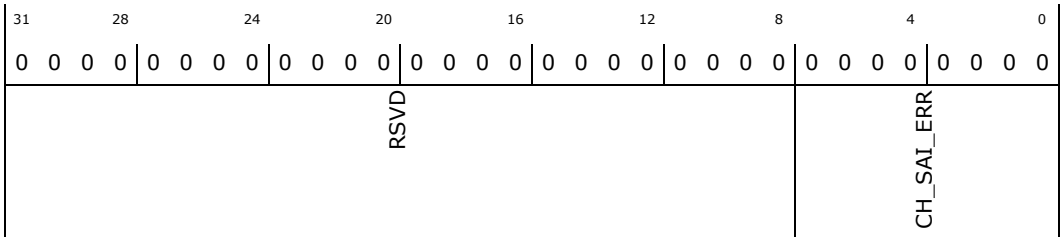
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAI_ERR: [BAR + 9C000h] + 410h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**CH_SAI_ERR:** 1: SAI Error occurred on Ch [n] 0: No SAI Error occurred on Ch [n] SAI_ERROR[n] is set by HW on SAI violation for channel [n]. All bits get cleared by SW when reading this register

3.22.137 reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h

GLOBAL_CFG: GLOBAL DMA Configuration Register

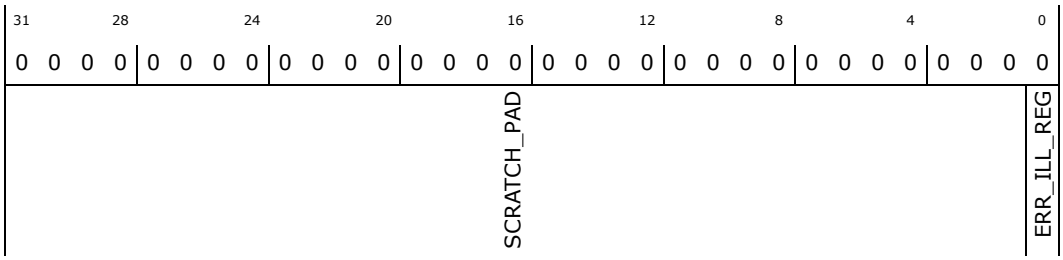
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

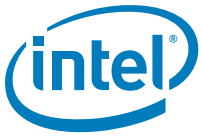
GLOBAL_CFG: [BAR + 9C000h] + 418h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future configuration and de-feature bits.
0	0b RW	**ERR_ILL_REG:** 0x1 : Issue ERR response on reading illegal (non-existing) registers 0x0 : Issue DVA response on reading illegal (non-existing) registers



3.23 Memory Mapped Shim Registers

Table 31. Summary of LPE Shim Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	8	"reg_CSR_type (CSR)—Offset 0h" on page 2056	0000000001E40001h
8h	8	"reg_XT_PISR_type (PISR)—Offset 8h" on page 2058	0000000000000000h
10h	8	"reg_XT_PIMR_type (PIMR)—Offset 10h" on page 2059	0000000000000000h
18h	8	"reg_IA_PISR_type (ISRX)—Offset 18h" on page 2060	0000000000000000h
20h	8	"reg_ISRD_type (ISRD)—Offset 20h" on page 2061	0000000000000000h
28h	8	"reg_IA_PIMR_type (IMRX)—Offset 28h" on page 2062	0000000000000000h
30h	8	"reg_IMRD_type (IMRD)—Offset 30h" on page 2063	0000000000000000h
38h	8	"reg_IPCX_type (IPCX)—Offset 38h" on page 2064	0000000000000000h
40h	8	"reg_IPCD_type (IPCD)—Offset 40h" on page 2064	0000000000000000h
48h	8	"reg_ISRSC_type (ISRSC)—Offset 48h" on page 2065	0000000000000000h
50h	8	"reg_ISRLPESC_type (ISRLPESC)—Offset 50h" on page 2066	0000000000000000h
58h	8	"reg_IMRSC_type (IMRSC)—Offset 58h" on page 2067	0000000000000000h
60h	8	"reg_IMRLPESC_type (IMRLPESC)—Offset 60h" on page 2068	0000000000000000h
68h	8	"reg_IPCSC_type (IPCSC)—Offset 68h" on page 2068	0000000000000000h
70h	8	"reg_IPCLPESC_type (IPCLPESC)—Offset 70h" on page 2069	0000000000000000h
78h	8	"reg_CLKCTL_type (CLKCTL)—Offset 78h" on page 2070	0000000000070013h
80h	8	"reg_FR_LAT_REQ_type (FR_LAT_REQ)—Offset 80h" on page 2071	0000000000000000h
88h	8	"reg_CHICKEN_BITS_type (CHICKEN_BITS)—Offset 88h" on page 2071	0000000000000000h
90h	8	"reg_ISRPSH_type (ISRPSH)—Offset 90h" on page 2072	0000000000000000h
98h	8	"reg_ISRLPEPSH_type (ISRLPEPSH)—Offset 98h" on page 2073	0000000000000000h

Table 31. Summary of LPE Shim Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
A0h	8	"reg_IMRPSH_type (IMRPSH)—Offset A0h" on page 2074	0000000000000000h
A8h	8	"reg_IMRLPEPSH_type (IMRLPEPSH)—Offset A8h" on page 2074	0000000000000000h
B0h	8	"reg_IPCPSH_type (IPCPSH)—Offset B0h" on page 2075	0000000000000000h
B8h	8	"reg_IPCLPEPSH_type (IPCLPEPSH)—Offset B8h" on page 2076	0000000000000000h
C0h	8	"reg_EXT_TIMER_CNTL_type (EXT_TIMER_CNTL)—Offset C0h" on page 2077	0000000000000000h
C8h	8	"reg_EXT_TIMER_STAT_type (EXT_TIMER_STAT)—Offset C8h" on page 2078	0000000000000000h
D0h	8	"reg_S0ix_TIMER_CNTL_type (S0ix_TIMER_CNTL)—Offset D0h" on page 2078	0000000000000000h
D8h	8	"reg_S0ix_TIMER_STAT_type (S0ix_TIMER_STAT)—Offset D8h" on page 2079	0000000000000000h
E0h	8	"reg_RAW_PISR_type (XT_RAW_PISR)—Offset E0h" on page 2080	0000000000000000h
E8h	8	"reg_SSP0_DIV_CTRL_type (SSP0_DIV_CTRL)—Offset E8h" on page 2080	8000000100000001h
F0h	8	"reg_SSP1_DIV_CTRL_type (SSP1_DIV_CTRL)—Offset F0h" on page 2081	8000000100000001h
F8h	8	"reg_SSP2_DIV_CTRL_type (SSP2_DIV_CTRL)—Offset F8h" on page 2082	8000000100000001h

3.23.1 reg_CSR_type (CSR)—Offset 0h

This register controls clock and reset of the block, various configurations of the block and reflects general status of the block.

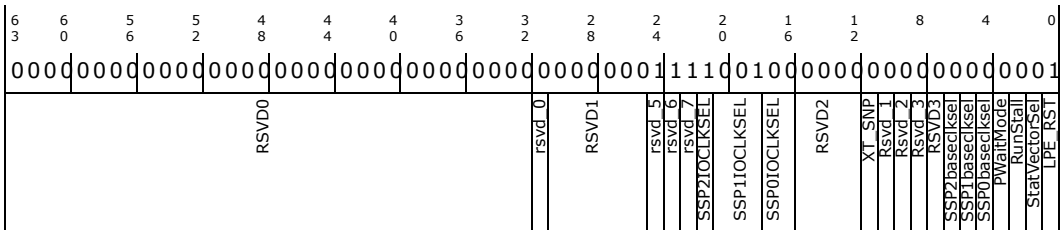
Access Method

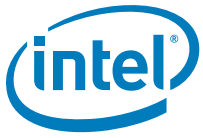
Type: Memory Mapped I/O Register (Size: 64 bits)

CSR: [BAR + 140000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000001E40001h





Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31	0b RW	**rsvd_0:** Reserved
30:25	0b RO	**RSVD1:** Reserved
24	1b RW	**rsvd_5:** Reserved
23	1b RW	**rsvd_6:** Reserved
22	1b RW	**rsvd_7:** Reserved
21:20	10b RW	**SSP2IOCLKSEL:** SSP 2 IO clock select 0: select SSP 0 IO clock for SSP 2 IO clock input 1: select SSP 1 IO clock for SSP 2 IO clock input 2: select SSP 2 IO clock for SSP 2 IO clock input
19:18	01b RW	**SSP1IOCLKSEL:** SSP 1 IO clock select 0: select SSP 0 IO clock for SSP 1 IO clock input 1: select SSP 1 IO clock for SSP 1 IO clock input 2: select SSP 2 IO clock for SSP 1 IO clock input
17:16	00b RW	**SSP0IOCLKSEL:** SSP 0 IO clock select 0: select SSP 0 IO clock for SSP 0 IO clock input 1: select SSP 1 IO clock for SSP 0 IO clock input 2: select SSP 2 IO clock for SSP 0 IO clock input
15:12	0b RO	**RSVD2:** Reserved
11	0b RW	**XT_SNP:** This bit controls whether the Tensilica initiated traffic is Snooped or Non-snooped. 0 =) Non-Snooped 1 =) Snooped
10	0b RW	**Rsvd_1:** Reserved
9	0b RW	**Rsvd_2:** Reserved
8	0b RW	**Rsvd_3:** Reserved
7	0b RO	**RSVD3:** Reserved
6	0b RW	**SSP2baseclksel:** 1 =) Select 25 MHz clock for the SSP2 base clock; 0 =) Select 19.2 MHz clock for the SSP base clock
5	0b RW	**SSP1baseclksel:** 1 =) Select 25 MHz clock for the SSP1 base clock; 0 =) Select 19.2 MHz clock for the SSP base clock
4	0b RW	**SSP0baseclksel:** 1 =) Select 25 MHz clock for the SSP0 base clock; 0 =) Select 19.2 MHz clock for the SSP base clock
3	0b RO	**PWaitMode:** Status bit when set to '1 indicates that LPE core is stalled.
2	0b RW	**RunStall:** When set to '1, LPE core is stalled.
1	0b RW	**StatVectorSel:** When set to '1, LPE core boots from the Alternate reset vector. This is set to ff2c_0000 - first address of Audio IRAM. Default reset vector is set to 0x100000. This needs to be set to 1'b1 for TNG.

Bit Range	Default & Access	Description
0	1b RW	**LPE_RST:** LPE Reset. LPE held in reset state until this bit is set to 1. Minimum number of cycles is defined LPE manual. The bit should be cleared to bring the LPE out of reset.

3.23.2 reg_XT_PISR_type (PISR)—Offset 8h

PISR

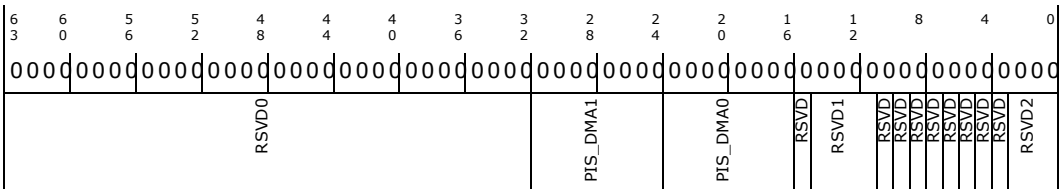
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

PISR: [BAR + 140000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:24	00000000b RW/1C	**PIS_DMA1:** DMA 1 interrupts
23:16	00000000b RW/1C	**PIS_DMA0:** DMA 0 interrupts
15	0b RO	**Reserved (RSVD):** Reserved.
14:11	0b RO	**RSVD1:** Reserved
10	0b RO	**Reserved (RSVD):** Reserved.
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	0b RO	**RSVD2:** Reserved

3.23.3 reg_XT_PIMR_type (PIMR)—Offset 10h

PIMR

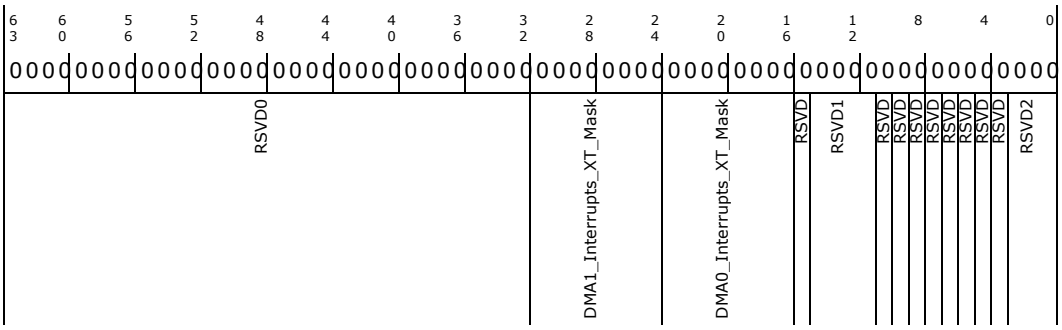
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

PIMR: [BAR + 140000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:24	00000000b RW	**DMA1_Interrupts_XT_Mask:** DMA 1 interrupts
23:16	00000000b RW	**DMA0_Interrupts_XT_Mask:** DMA 0 interrupts
15	0b RO	**Reserved (RSVD):** Reserved.
14:11	0b RO	**RSVD1:** Reserved
10	0b RO	**Reserved (RSVD):** Reserved.
9	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
8	0b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	0b RO	**RSVD2:** Reserved

3.23.4 reg_IA_PISR_type (ISRX)—Offset 18h

PISR

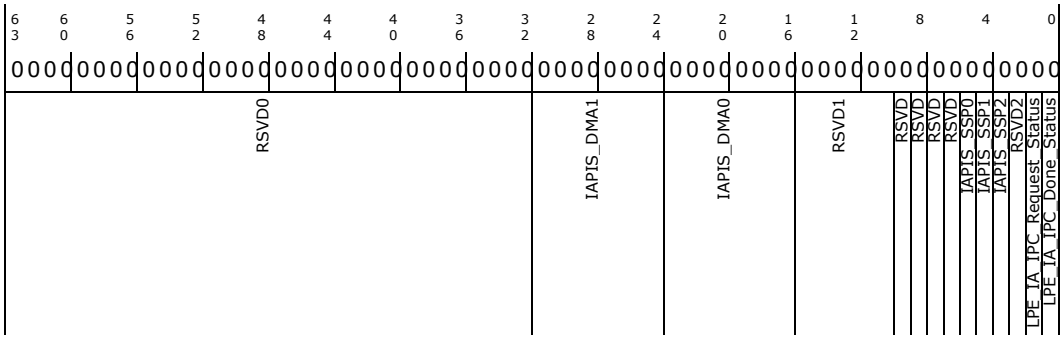
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

ISRX: [BAR + 140000h] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:24	00000000b RW/1C	**IAPIS_DMA1:** DMA 1 interrupts
23:16	00000000b RW/1C	**IAPIS_DMA0:** DMA 0 interrupts

Bit Range	Default & Access	Description
15:10	0b RO	**RSVD1:** Reserved
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RW/1C	**IAPIS_SSP0:** SSP0 Interrupt Request for SC 1: interrupt when SSP0 interrupt is asserted. 0: Deasserted
4	0b RW/1C	**IAPIS_SSP1:** SSP1 Interrupt Request for SC 1: interrupt when SSP1 interrupt is asserted. 0: Deasserted
3	0b RW/1C	**IAPIS_SSP2:** SSP2 Interrupt Request for SC 1: interrupt when SSP2 interrupt is asserted. 0: Deasserted
2	0b RO	**RSVD2:** Reserved
1	0b RO	**LPE_IA_IPC_Request_Status:** IPCD Interrupt Request 1: interrupt when LPE writes a message into IPCD register with bit 63 set 0: Deasserted
0	0b RO	**LPE_IA_IPC_Done_Status:** IPCX Interrupt Request 1: interrupt when LPE writes a message into IPCX register with bit 62 set is asserted 0: Deasserted.

3.23.5 reg_ISRD_type (ISRD)—Offset 20h

ISRD

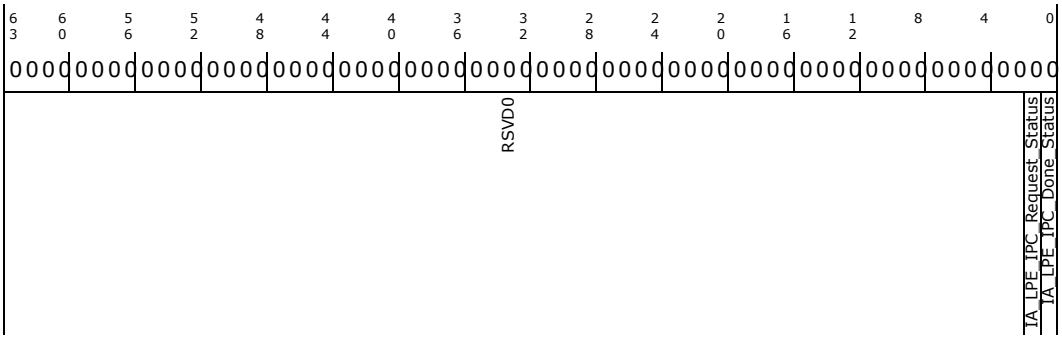
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

ISRD: [BAR + 140000h] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RO	**IA_LPE_IPC_Request_Status:** IPCIA Interrupt Request to LPE 1: interrupt when IA-32 CPU writes a message into IPCIA register with bit 63 set. 0: Deasserted
0	0b RO	**IA_LPE_IPC_Done_Status:** IPCLPEIA Interrupt Request to LPE 1: interrupt when IA-32 CPU writes a message into IPCLPEIA register with bit 62 set is asserted 0: Deasserted.

3.23.6 reg_IA_PIMR_type (IMRX)—Offset 28h

PIMR

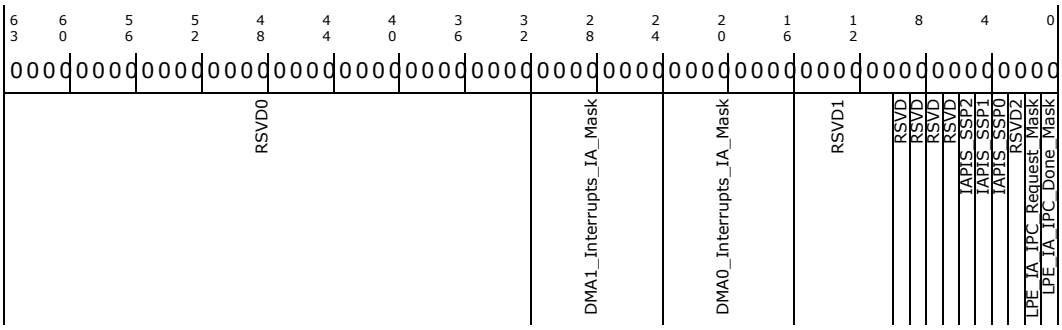
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IMRX: [BAR + 140000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:24	0b RW	**DMA1_Interrupts_IA_Mask:** DMA 1 interrupts mask
23:16	0b RW	**DMA0_Interrupts_IA_Mask:** DMA 0 interrupts mask
15:10	0b RO	**RSVD1:** Reserved
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
7	0b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RW	**IAPIS_SSP2:** SSP2 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
4	0b RW	**IAPIS_SSP1:** SSP1 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
3	0b RW	**IAPIS_SSP0:** SSP0 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
2	0b RO	**RSVD2:** Reserved
1	0b RW	**LPE_IA_IPC_Request_Mask:** LPE to IA IPC Request Mask 1: Interrupt is masked 0: Interrupt is unmasked
0	0b RW	**LPE_IA_IPC_Done_Mask:** LPE to IA IPC Done Mask 1: Interrupt is masked 0: Interrupt is unmasked

3.23.7 reg_IMRD_type (IMRD)—Offset 30h

IMRD

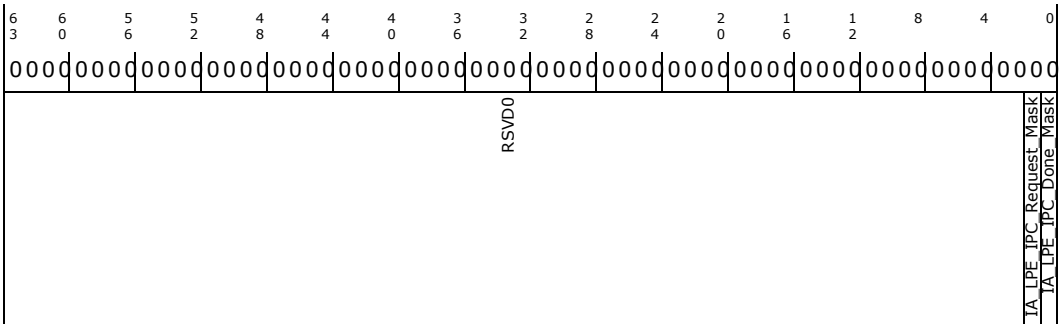
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IMRD: [BAR + 140000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RW	**IA_LPE_IPC_Request_Mask:** IPCIA interrupt Enable to LPE

Bit Range	Default & Access	Description
0	0b RW	**IA_LPE_IPC_Done_Mask:** IPCLPEIA interrupt Enable to LPE

3.23.8 reg_IPCX_type (IPCX)—Offset 38h

The Inter-process Status and Message register for IA-32 contains a message sent from the IA-32 CPU to LPE. The format of the CPU message bits (61:0) is not defined in the HW specs. It is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When the message is written in this register, the software must set bit 63 to indicate that the IPCIA is not empty. Setting Busy also asserts interrupt request to LPE if the interrupt is enabled in the IMRLPEIA. After LPE reads the message code from the register, it must perform a write with bit 63 cleared. The IA-32 CPU must not attempt to write into IPCIA if bit 63 is set.

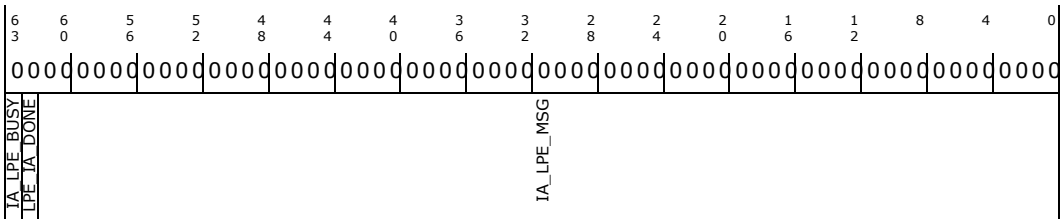
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IPCX: [BAR + 140000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**IA_LPE_BUSY:** Busy. When this bit is cleared, the LPE Ready to accept a message
62	0b RW	**LPE_IA_DONE:** Done. When the bit is set, the LPE completed the operation and requests attention
61:0	00000000 0000000h RW	**IA_LPE_MSG:** IA-32 to LPE Message

3.23.9 reg_IPCD_type (IPCD)—Offset 40h

Inter-process Status and Message register for LPE contains a message sent from LPE to IA-32 CPU. The format of the CPU message bits 29:0 is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When software writes the message is in this register, it should set bit 63 to indicate that the new data is written. When IA-32 CPU reads the

message code from the register, and writes back with the bit 63 cleared. When the IA-32 CPU processes the message sent by LPE, it may set bit 63 in IPCD to assert interrupt request to LPE. The LPE must not attempt to write into IPCLPEIA if bit 63 is set.

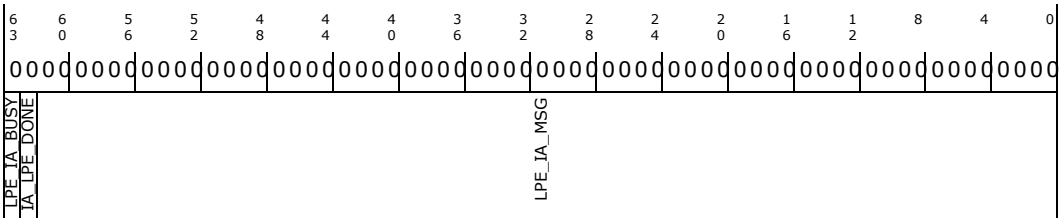
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IPCD: [BAR + 140000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**LPE_IA_BUSY:** Busy. When this bit is cleared, the IA CPU is Ready to accept a new message
62	0b RW	**IA_LPE_DONE:** Done. When the bit is set, the IA CPU completed operation and requests attention from LPE
61:0	00000000000000h RW	**LPE_IA_MSG:** LPE to IA CPU Message

3.23.10 reg_ISRSC_type (ISRSC)—Offset 48h

ISRSC

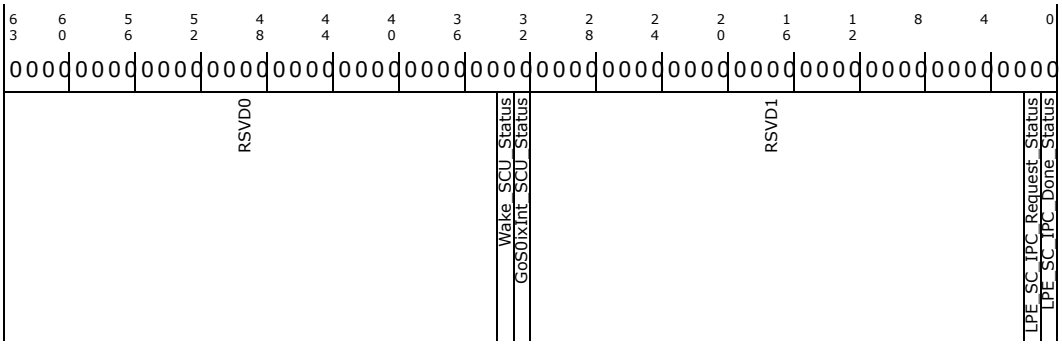
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

ISRSC: [BAR + 140000h] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:34	0b RO	**RSVD0:** Reserved
33	0b RW/1C	**Wake_SCU_Status:** This bit is set by hardware when a blocked transaction is detected. It generates a wake to the SCU
32	0b RW/1C	**GoS0ixInt_SCU_Status:** This bit is set by expiry of the Re-entry timer. The bit gets set only if GoS0ixInt_En bit is set and this interrupt is unmasked.
31:2	0b RO	**RSVD1:** Reserved
1	0b RO	**LPE_SC_IPC_Request_Status:** IPCLPESC Interrupt Request 1: interrupt when LPE writes a message into IPCLPESC register with bit 63 set 0: Deasserted
0	0b RW/1C	**LPE_SC_IPC_Done_Status:** IPCSC Interrupt Request 1: interrupt when LPE writes a message into IPCSC register with bit 62 set is asserted 0: Deasserted.

3.23.11 reg_ISRLPESC_type (ISRLPESC)—Offset 50h

ISRLPESC

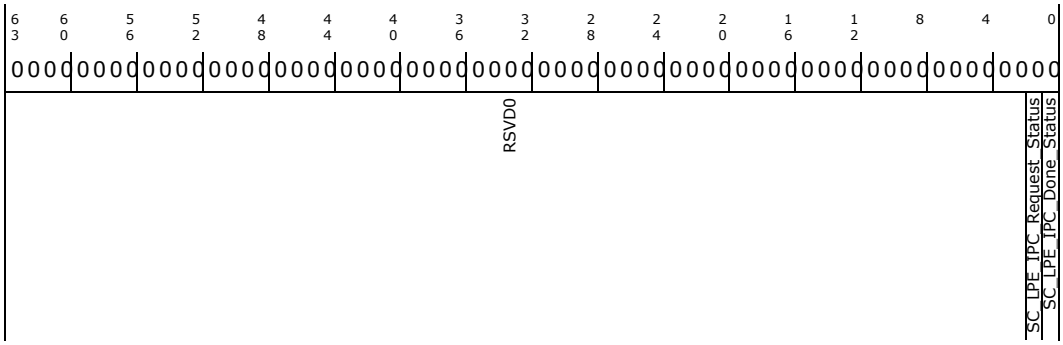
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

ISRLPESC: [BAR + 140000h] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RO	**SC_LPE_IPC_Request_Status:** IPCSC Interrupt Request to LPE 1: interrupt when SC writes a message into IPCSC register with bit 63 set. 0: Deasserted

Bit Range	Default & Access	Description
0	0b RO	**SC_LPE_IPC_Done_Status:** IPCLPESC Interrupt Request to LPE 1: interrupt when SC CPU writes a message into IPCLPEIA register with bit 62 set is asserted 0: Deasserted.

3.23.12 reg_IMRSC_type (IMRSC)—Offset 58h

IMRSC

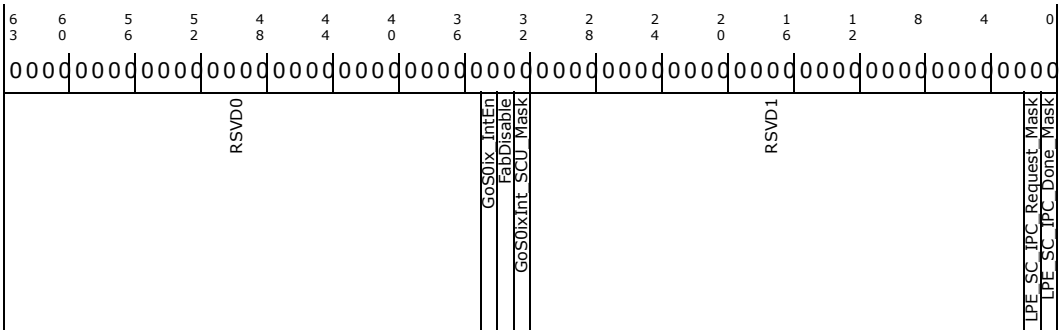
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IMRSC: [BAR + 140000h] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:35	0b RO	**RSVD0:** Reserved
34	0b RW/1C	**GoS0ix_IntEn:** This bit indicates that Reentry to S0iX interrupts to SCU are enabled. The bit is set by hardware when a transaction is blocked at the Audio to Secondary interface due to the secondary fabric being gated and the fabdisable bit being set. Software is expected to clear this bit along with the Secondary Fabric Reject bit. This disables the interrupts.
33	0b RW	**FabDisable:** This bit is used to generate the wake interrupt to SCU. When set the interrupt generation is enabled. When cleared the interrupt generation is disabled
32	0b RW	**GoS0ixInt_SCU_Mask:** Mask bit for S0ix Reentry interrupt to SCU
31:2	0b RO	**RSVD1:** Reserved
1	0b RW	**LPE_SC_IPC_Request_Mask:** IPCLPESC Interrupt Enable to SC CPU
0	0b RW	**LPE_SC_IPC_Done_Mask:** IPCSC Interrupt Enable to SC CPU

3.23.13 reg_IMRLPESC_type (IMRLPESC)—Offset 60h

IMRLPRESC

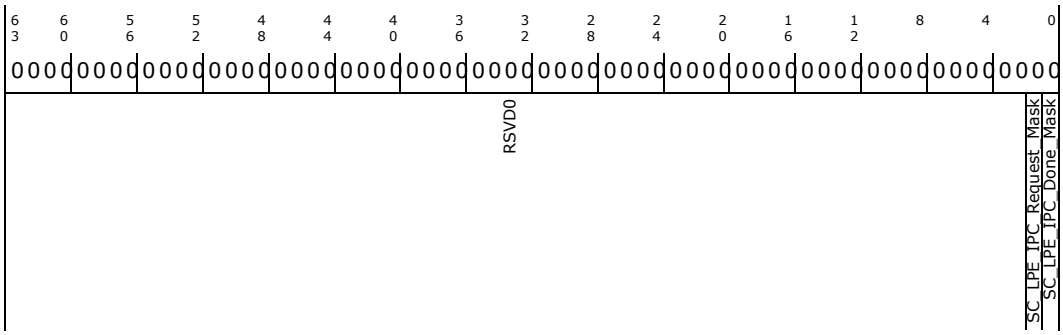
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IMRLPESC: [BAR + 140000h] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RW	**SC_LPE_IPC_Request_Mask:** IPCSC interrupt Enable to LPE
0	0b RW	**SC_LPE_IPC_Done_Mask:** IPCLPESC interrupt Enable to LPE

3.23.14 reg_IPCSC_type (IPCSC)—Offset 68h

The Inter-process Status and Message register for SC contains a message sent from the SC CPU to LPE. The format of the CPU message bits (29:0) is not defined in the HW specs. It is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When the message is written in this register, the software must set bit 63 to indicate that the IPCSC is not empty. Setting Busy also asserts interrupt request to LPE if the interrupt is enabled in the IMRLPESC. After LPE reads the message code from the register, it must perform a write with bit 63 cleared. The SC CPU must not attempt to write into IPCIA if bit 63 is set.

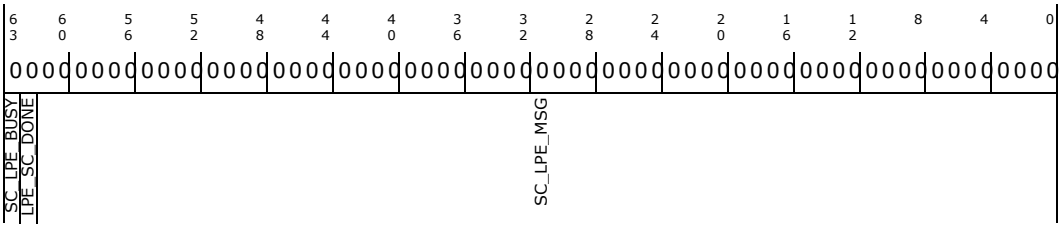
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IPCSC: [BAR + 140000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**SC_LPE_BUSY:** Busy. When this bit is cleared, the LPE Ready to accept a message
62	0b RW	**LPE_SC_DONE:** Done. When the bit is set, the LPE completed the operation and requests attention
61:0	00000000000000000h RW	**SC_LPE_MSG:** SC to LPE Message

3.23.15 reg_IPCLPESC_type (IPCLPESC)—Offset 70h

Inter-process Status and Message register for LPE contains a message sent from LPE to SC. The format of the CPU message bits 29:0 is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When software writes the message is in this register, it should set bit 63 to indicate that the new data is written. When SC reads the message code from the register, and writes back with the bit 63 cleared. When the SC CPU processes the message sent by LPE, it may set bit 62 in IPCLPESC to assert interrupt request to LPE. The LPE must not attempt to write into IPCD if bit 63 is set.

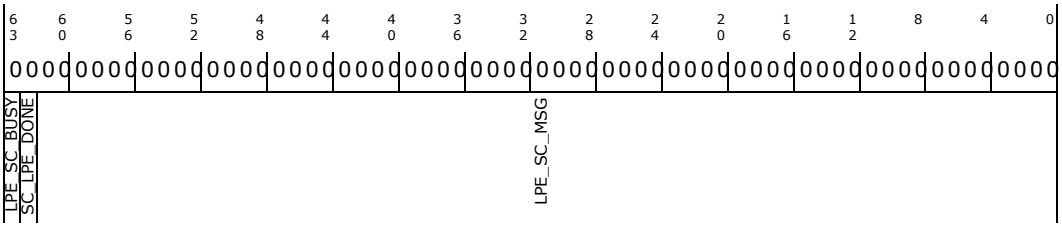
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IPCLPESC: [BAR + 140000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**LPE_SC_BUSY:** Busy. When this bit is cleared, the SC CPU is Ready to accept a new message

Bit Range	Default & Access	Description
62	0b RW	**SC_LPE_DONE:** Done. When the bit is set, the SC CPU completed operation and requests attention from LPE
61:0	0h RW	**LPE_SC_MSG:** LPE to SC CPU Message

3.23.16 reg_CLKCTL_type (CLKCTL)—Offset 78h

LPE Clock Control Register

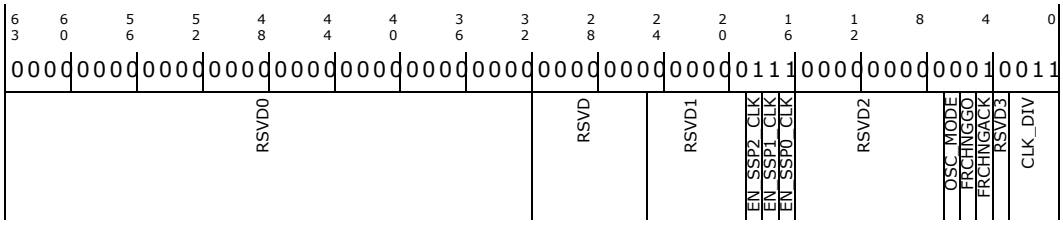
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

CLKCTL: [BAR + 140000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000070013h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:25	0000000b RO	**RSVD:** Reserved
24:19	0b RO	**RSVD1:** Reserved
18	1b RW	**EN_SSP2_CLK:** clock output enable
17	1b RW	**EN_SSP1_CLK:** clock output enable
16	1b RW	**EN_SSP0_CLK:** clock output enable
15:7	0b RO	**RSVD2:** Reserved
6	0b RO	**OSC_MODE:** 1 indicates that PLL is turned off
5	0b RW/1S	**FRCHNGGO:** Go bit indicating that the value in 2:0 can be applied to core. This bit will get cleared on the rising edge of the ack from Clock Control Unit.

Bit Range	Default & Access	Description
4	1b RO	**FRCHNGACK:** Sets on the falling edge of ack. A 1'b1 indicates that the frequency change is done. The bit auto clears on the rising edge of frequency change request.
3	0b RO	**RSVD3:** Reserved
2:0	011b RW	**CLK_DIV:** 000: 25 MHz(XTAL) 001: 25 Mhz(XTAL) 010: 50 Mhz(2xXTAL) 011: 50 Mhz(default) 100: 100 MHz 101: 200 MHz 110: 267 MHz 111: 343 MHz

3.23.17 reg_FR_LAT_REQ_type (FR_LAT_REQ)—Offset 80h

LPE

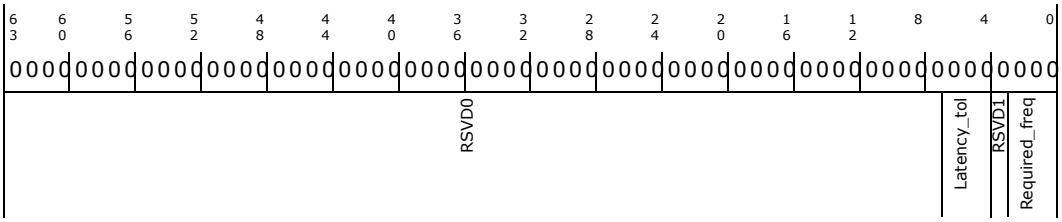
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

FR_LAT_REQ: [BAR + 140000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:7	0b RO	**RSVD0:** Reserved
6:4	0b RW	**Latency_tol:** Latency tolerance for Cache Misses is listed here. SCU firmware is required to read this register and make a decision on whether it can enter a lower power state and still meet the latency tolerance.
3	0b RO	**RSVD1:** Reserved
2:0	0b RW	**Required_freq:** The following encoding specifies the frequency that the Audio Cluster requires for current operations. 000: 25 MHz(XTAL) 001: 25 Mhz(XTAL) 010: 50 Mhz(2xXTAL) 011: 50 Mhz(default) 100: 100 MHz 101: 200 MHz 110: 267 MHz 111: 343 MHz Please note, that this does not guarantee that this frequency will be generated from the CCU. The SCU firmware is required to read this register before making a decision on entering lower power states.

3.23.18 reg_CHICKEN_BITS_type (CHICKEN_BITS)—Offset 88h

LPE

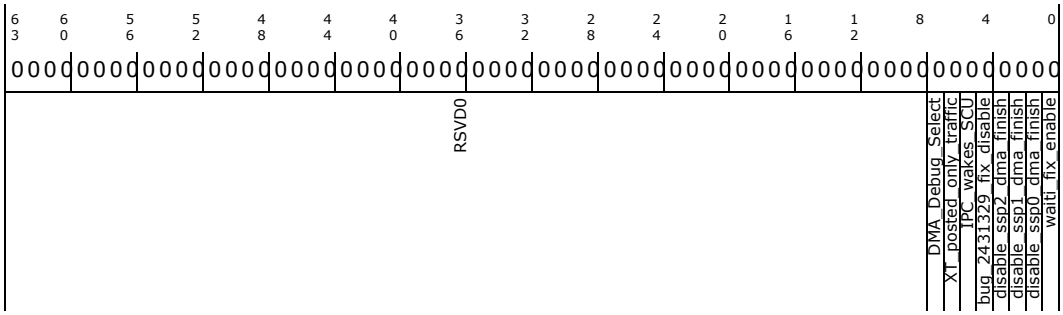
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

CHICKEN_BITS: [BAR + 140000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:8	0b RO	**RSVD0:** Reserved
7	0b RW	**DMA_Debug_Select:** Setting this bit will select DMA 1 debug signals to be routed to the VISA Mux.
6	0b RW	**XT_posted_only_traffic:** Setting this bit will select make all the traffic from Tensilica to be posted.
5	0b RW	**IPC_wakes_SCU:** Setting this to 1 will cause the IPC to be fed into the wake cone for SCU.
4	0b RW	**bug_2431329_fix_disable:** Setting this to 1 will disable the synopsys compatible hardware handshake mechanism. Keep this set to 0 for regular hardware handshake operation.
3	0b RW	**disable_ssp2_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
2	0b RW	**disable_ssp1_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
1	0b RW	**disable_ssp0_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
0	0b RW	**waiti_fix_enable:** Setting this bit to 1 makes the frequency change request to be valid only if the core is in WAITI.

3.23.19 reg_ISRPSH_type (ISRPSH)—Offset 90h

ISRPSH

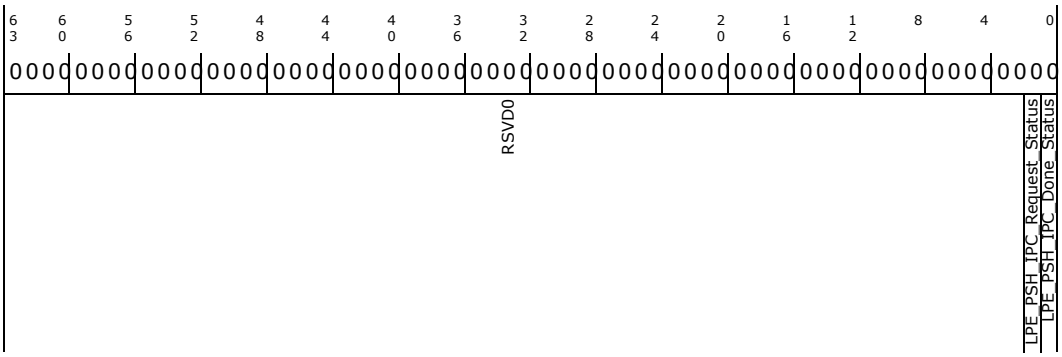
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

ISRPSH: [BAR + 140000h] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RO	**LPE_PSH_IPC_Request_Status:** IPCLPEPSH Interrupt Request 1: interrupt when LPE writes a message into IPCLPEPSH register with bit 63 set 0: Deasserted
0	0b RW/1C	**LPE_PSH_IPC_Done_Status:** IPCPSH Interrupt Request 1: interrupt when LPE writes a message into IPCPSH register with bit 62 set is asserted 0: Deasserted.

3.23.20 reg_ISRLPEPSH_type (ISRLPEPSH)—Offset 98h

ISRLPEPSH

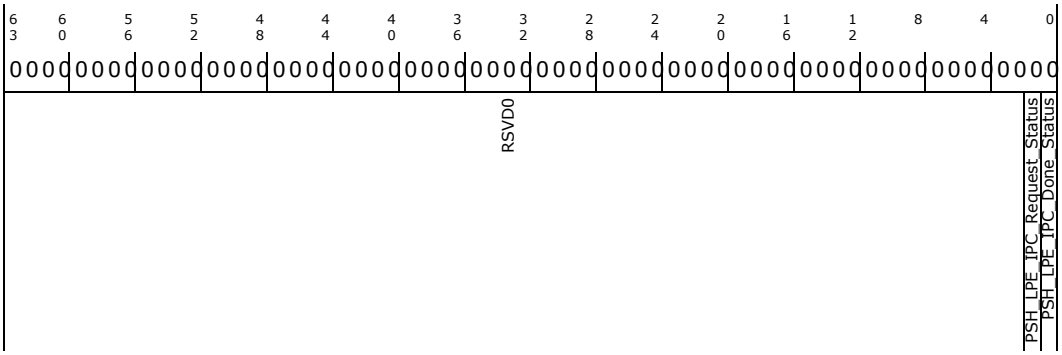
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

ISRLPEPSH: [BAR + 140000h] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RO	**PSH_LPE_IPC_Request_Status:** IPCPSH Interrupt Request to LPE 1: interrupt when PSH writes a message into IPCPSH register with bit 63 set. 0: Deasserted
0	0b RO	**PSH_LPE_IPC_Done_Status:** IPCLPEPSH Interrupt Request to LPE 1: interrupt when PSH CPU writes a message into IPCLPEIA register with bit 62 set is asserted 0: Deasserted.

3.23.21 reg_IMRPSH_type (IMRPSH)—Offset A0h

IMRPSH

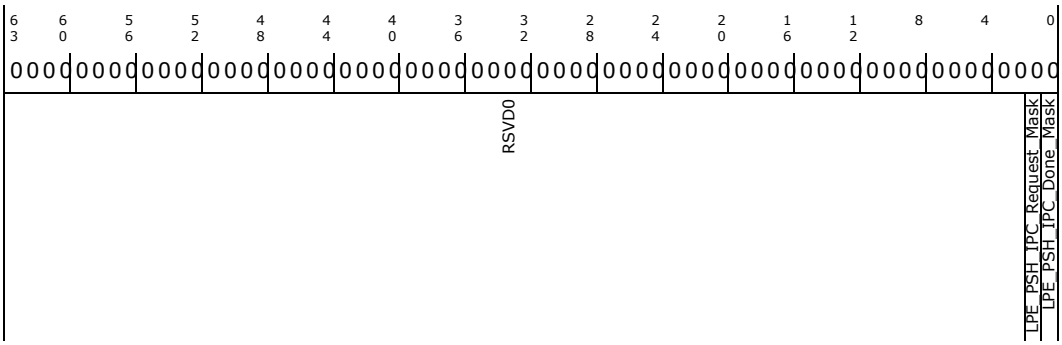
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IMRPSH: [BAR + 140000h] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RW	**LPE_PSH_IPC_Request_Mask:** IPCLPEPSH Interrupt Enable to PSH CPU
0	0b RW	**LPE_PSH_IPC_Done_Mask:** IPCPSH Interrupt Enable to PSH CPU

3.23.22 reg_IMRLPEPSH_type (IMRLPEPSH)—Offset A8h

IMRLPEPSH

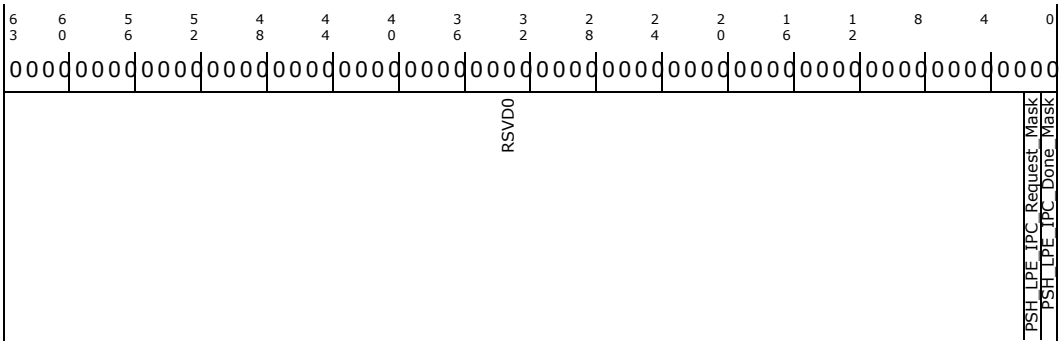
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IMRLPEPSH: [BAR + 140000h] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RW	**PSH_LPE_IPC_Request_Mask:** IPCPSH interrupt Enable to LPE
0	0b RW	**PSH_LPE_IPC_Done_Mask:** IPCLPEPSH interrupt Enable to LPE

3.23.23 reg_IPCPSH_type (IPCPSH)—Offset B0h

The Inter-process Status and Message register for PSH contains a message sent from the PSH CPU to LPE. The format of the CPU message bits (29:0) is not defined in the HW specs. It is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When the message is written in this register, the software must set bit 63 to indicate that the IPCPSH is not empty. Setting Busy also asserts interrupt request to LPE if the interrupt is enabled in the IMRLPEPSH. After LPE reads the message code from the register, it must perform a write with bit 63 cleared. The PSH CPU must not attempt to write into IPCIA if bit 63 is set.

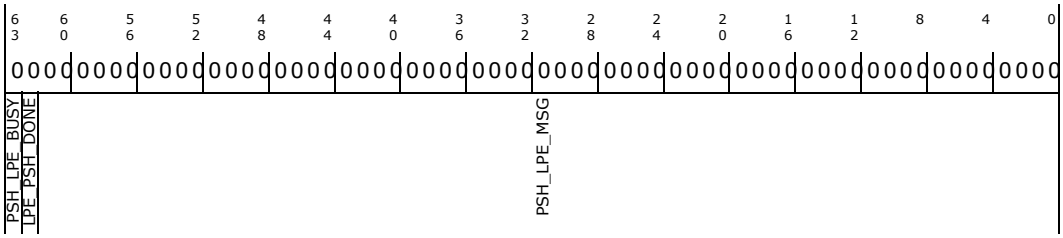
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IPCPSH: [BAR + 140000h] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**PSH_LPE_BUSY:** Busy. When this bit is cleared, the LPE Ready to accept a message
62	0b RW	**LPE_PSH_DONE:** Done. When the bit is set, the LPE completed the operation and requests attention
61:0	00000000000000h RW	**PSH_LPE_MSG:** PSH to LPE Message

3.23.24 reg_IPCLPEPSH_type (IPCLPEPSH)—Offset B8h

Inter-process Status and Message register for LPE contains a message sent from LPE to PSH. The format of the CPU message bits 29:0 is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When software writes the message is in this register, it should set bit 63 to indicate that the new data is written. When PSH reads the message code from the register, and writes back with the bit 63 cleared. When the PSH CPU processes the message sent by LPE, it may set bit 62 in IPCLPEPSH to assert interrupt request to LPE. The LPE must not attempt to write into IPCD if bit 63 is set.

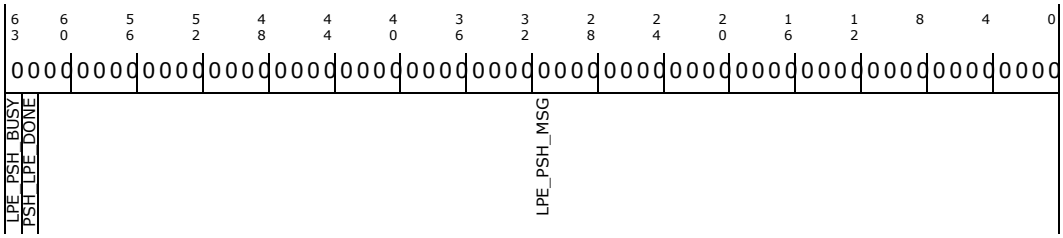
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IPCLPEPSH: [BAR + 140000h] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**LPE_PSH_BUSY:** Busy. When this bit is cleared, the PSH CPU is Ready to accept a new message

Bit Range	Default & Access	Description
62	0b RW	**PSH_LPE_DONE:** Done. When the bit is set, the PSH CPU completed operation and requests attention from LPE
61:0	0h RW	**LPE_PSH_MSG:** LPE to PSH CPU Message

3.23.25 reg_EXT_TIMER_CNTL_type (EXT_TIMER_CNTL)—Offset C0h

External Timer Control Register

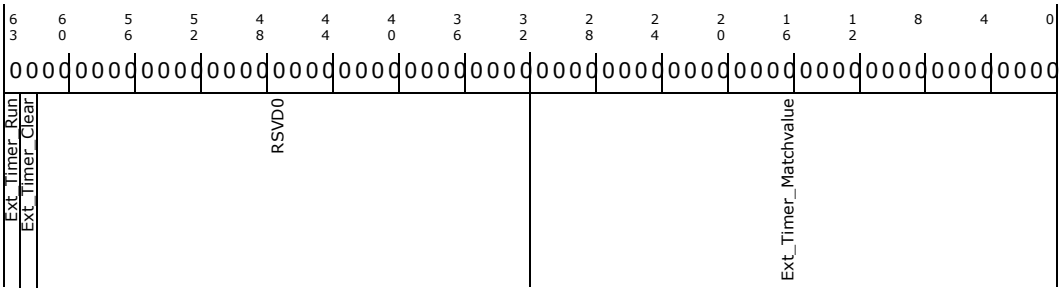
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

EXT_TIMER_CNTL: [BAR + 140000h] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**Ext_Timer_Run:** Timer Run bit. The timer runs only when this bit is set. It resumes running from the current value in the readvalue bits. Clearing the bit pauses the timer.
62	0b RW/S	**Ext_Timer_Clear:** Timer Clear bit. Clears the timer and sets the value back to zero. This should also be reflected in the readvalue bits
61:32	0b RO	**RSVD0:** Reserved
31:0	0b RW	**Ext_Timer_Matchvalue:** The timer will generate a pulse when the Readvalue reaches Matchvalue. The pulse causes a level interrupt to get set in the PISR register. The PISR interrupt needs to be cleared before the next pulse is generated. The timer keeps counting beyond the Readvalue. Setting the Matchvalue to zero makes this a free running timer and no interrupt will be generated in this case. For correct operation, the ISR should either set a new Matchvalue or set it to zero. If nothing is done, the timer will roll over and trigger an interrupt again when it reaches the Matchvalue.

3.23.26 reg_EXT_TIMER_STAT_type (EXT_TIMER_STAT)—Offset C8h

External Timer Control Register

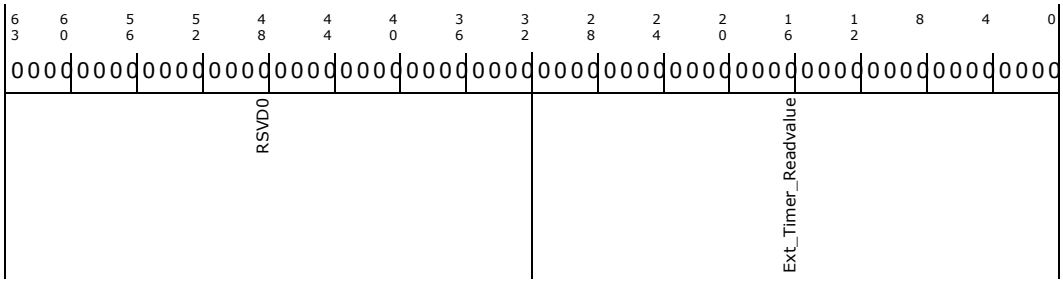
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

EXT_TIMER_STAT: [BAR + 140000h] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:0	0b RO	**Ext_Timer_Readvalue:** Shows the current count value of the timer

3.23.27 reg_S0ix_TIMER_CNTL_type (S0ix_TIMER_CNTL)—Offset D0h

External Timer Control Register

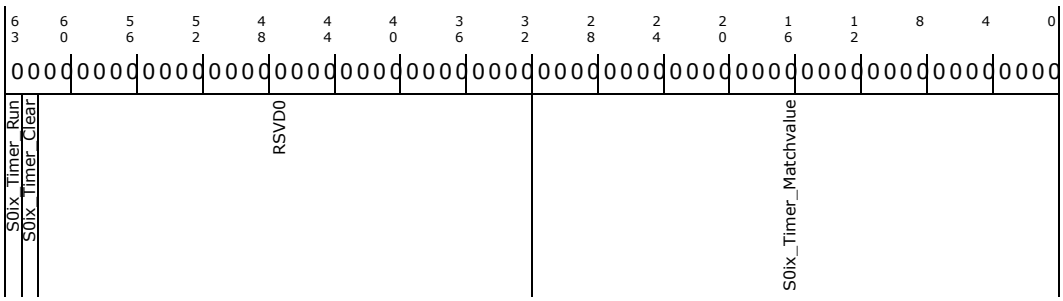
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

S0ix_TIMER_CNTL: [BAR + 140000h] + D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**S0ix_Timer_Run:** Timer Run bit. The timer runs only when this bit is set. It resumes running from the current value in the readvalue bits. Clearing the bit pauses the timer.
62	0b RW/S	**S0ix_Timer_Clear:** Timer Clear bit. Clears the timer and sets the value back to zero. This should also be reflected in the readvalue bits
61:32	0b RO	**RSVD0:** Reserved
31:0	0b RW	**S0ix_Timer_Matchvalue:** The timer will generate a pulse when the Readvalue reaches Matchvalue. The pulse causes a level interrupt to get set in the PISR register. The PISR interrupt needs to be cleared before the next pulse is generated. The timer keeps counting beyond the Readvalue. Setting the Matchvalue to zero makes this a free running timer and no interrupt will be generated in this case. For correct operation, the ISR should either set a new Matchvalue or set it to zero. If nothing is done, the timer will roll over and trigger an interrupt again when it reaches the Matchvalue.

3.23.28 reg_S0ix_TIMER_STAT_type (S0ix_TIMER_STAT)—Offset D8h

External Timer Control Register

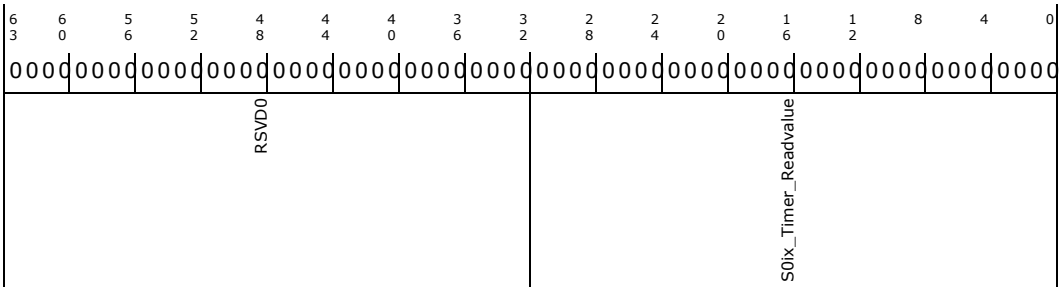
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

S0ix_TIMER_STAT: [BAR + 140000h] + D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:0	0b RO	**S0ix_Timer_Readvalue:** Shows the current count value of the timer

3.23.29 reg_RAW_PISR_type (XT_RAW_PISR)—Offset E0h

RAW PISR

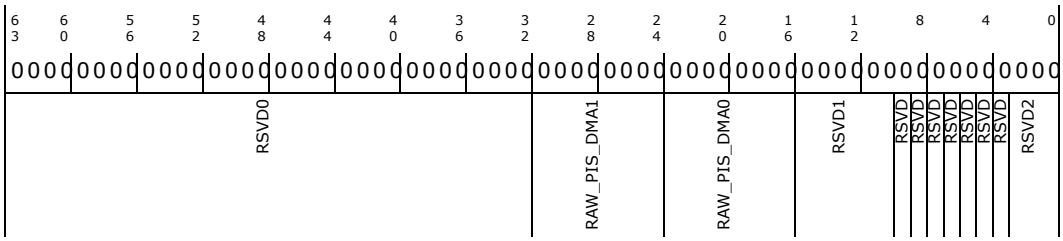
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

XT_RAW_PISR: [BAR + 140000h] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:24	00000000b RO	**RAW_PIS_DMA1:** DMA 1 interrupts
23:16	00000000b RO	**RAW_PIS_DMA0:** DMA 0 interrupts
15:10	0b RO	**RSVD1:** Reserved
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	0b RO	**RSVD2:** Reserved

3.23.30 reg_SSP0_DIV_CTRL_type (SSP0_DIV_CTRL)—Offset E8h

SSP0 M/N Clock Divider control - Add for VLV

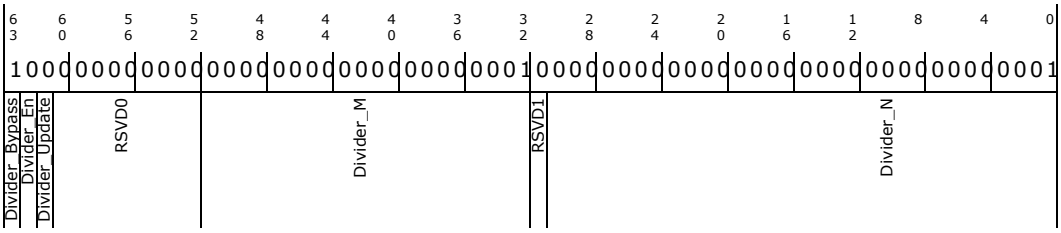
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

SSP0_DIV_CTRL: [BAR + 140000h] + E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 8000000100000001h



Bit Range	Default & Access	Description
63	1b RW	**Divider_Bypass:** SSP0 Bypass divider
62	0b RW	**Divider_En:** SSP0 Enable divider
61	0b RW	**Divider_Update:** SSP0 Update divider
60:52	0b RO	**RSVD0:** Reserved
51:32	1b RW	**Divider_M:** SSP0 Nominator value
31:20	0b RO	**RSVD1:** Reserved
19:0	1b RW	**Divider_N:** SSP0 Denominator value

3.23.31 reg_SSP1_DIV_CTRL_type (SSP1_DIV_CTRL)—Offset F0h

SSP1 M/N Clock Divider control - Add for VLV

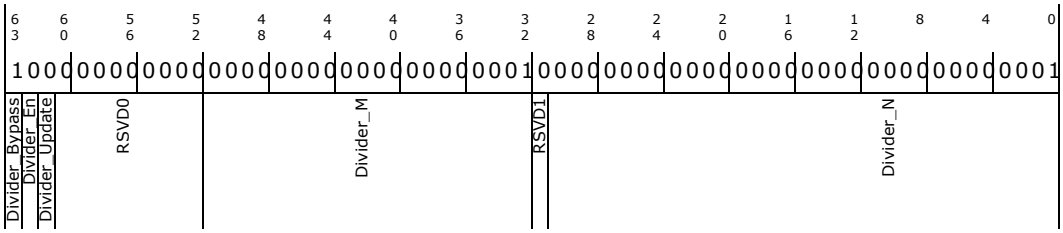
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

SSP1_DIV_CTRL: [BAR + 140000h] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 8000000100000001h



Bit Range	Default & Access	Description
63	1b RW	**Divider_Bypass:** SSP1 Bypass divider
62	0b RW	**Divider_En:** SSP1 Enable divider
61	0b RW	**Divider_Update:** SSP1 Update divider
60:52	0b RO	**RSVD0:** Reserved
51:32	1b RW	**Divider_M:** SSP1 Nominator value
31:20	0b RO	**RSVD1:** Reserved
19:0	1b RW	**Divider_N:** SSP1 Denominator value

3.23.32 reg_SSP2_DIV_CTRL_type (SSP2_DIV_CTRL)—Offset F8h

SSP2 M/N Clock Divider control - Add for VLV

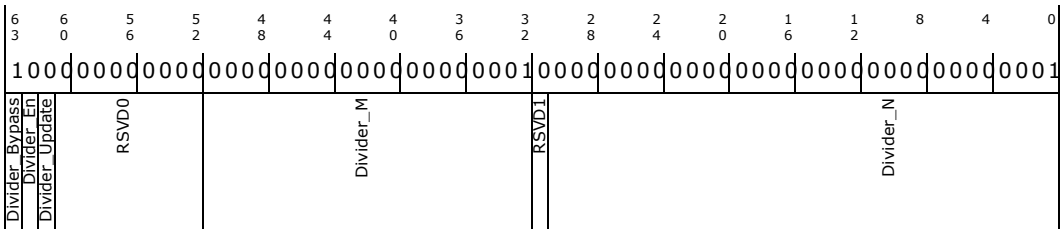
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

SSP2_DIV_CTRL: [BAR + 140000h] + F8h

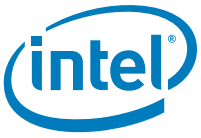
BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 8000000100000001h



Bit Range	Default & Access	Description
63	1b RW	**Divider_Bypass:** SSP2 Bypass divider

Bit Range	Default & Access	Description
62	0b RW	**Divider_En:** SSP2 Enable divider
61	0b RW	**Divider_Update:** SSP2 Update divider
60:52	0b RO	**RSVD0:** Reserved
51:32	1b RW	**Divider_M:** SSP2 Nominator value
31:20	0b RO	**RSVD1:** Reserved
19:0	1b RW	**Divider_N:** SSP2 Denominator value



3.24 Low Power Audio PCI Configuration Registers

Table 32. Summary of Low Power Audio PCI Configuration Registers—0/21/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 2084	0F288086h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 2085	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 2086	04010000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 2086	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 2087	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 2088	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 2089	00000000h
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2089	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 2090	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 2090	00000100h
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 2091	00030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 2092	00000008h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 2093	01000F00h

3.24.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

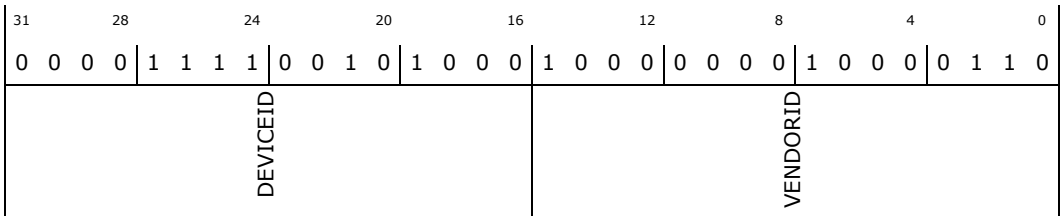
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEVVENDID: [0/21/0] + 0h

Default: 0F288086h



Bit Range	Default & Access	Description
31:16	0F28h RO	**DEVICEID:** Device ID

Bit Range	Default & Access	Description
15:0	8086h RO	**VENDORID:** Vendor ID

3.24.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

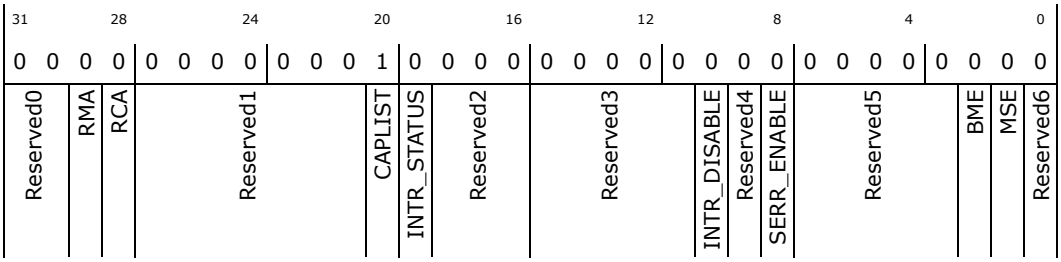
STATUSCOMMAND- Status and Command

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STATUSCOMMAND: [0/21/0] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** reserved
29	0h RW/1C	**RMA:** Received Master Abort: Not Implemented
28	0h RW/1C	**RCA:** Received Target Abort: Not Implemented
27:21	00h RO	**Reserved1:** reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** reserved
15:11	00h RO	**Reserved3:** reserved

Bit Range	Default & Access	Description
10	0h RW	**INTR_DISABLE:** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does not send Interrupt Assert message through the IOSF Sideband Channel. Reset value of this bit is 0. This bit has no connection with the interrupt status bit
9	0h RO	**Reserved4:** reserved
8	0h RW	**SERR_ENABLE:** not implemented
7:3	00h RO	**Reserved5:** reserved
2	0h RW	**BME:** If this bit is 0,the Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**MSE:** Memory Space Enable: This bit controls Bridge response to downstream memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0h RO	**Reserved6:** reserved

3.24.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

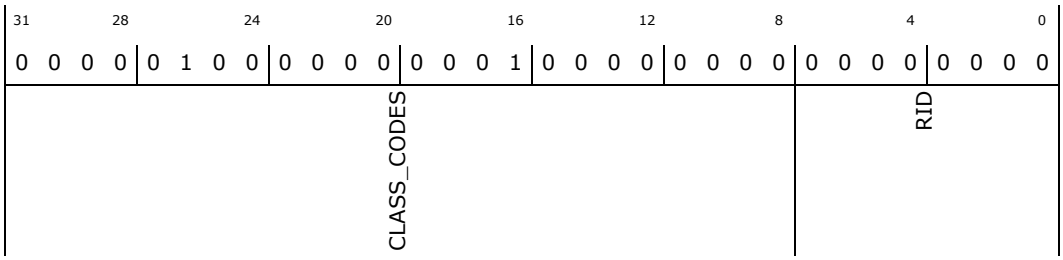
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

REVCLASSCODE: [0/21/0] + 8h

Default: 04010000h



Bit Range	Default & Access	Description
31:8	040100h RO	**CLASS_CODES:** Class Code
7:0	00h RO	**RID:** Revision ID

3.24.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

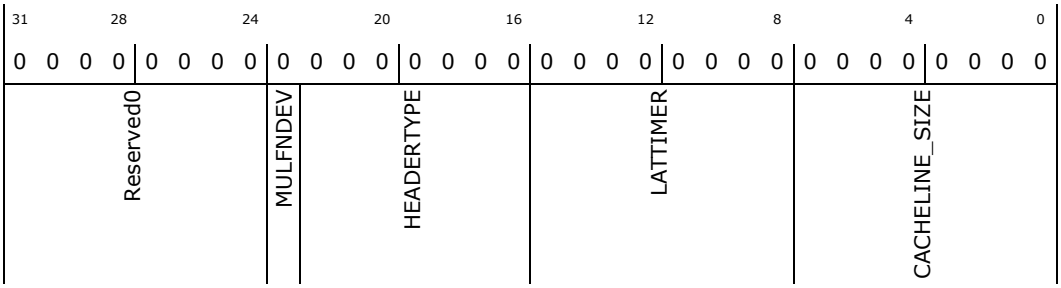
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CLLATHEADERBIST: [0/21/0] + Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved
23	0h RO	**MULFNDEV:** MULFNDEV
22:16	00h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	00h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0. Similar to other Intel IPs.
7:0	00h RW	**CACHELINE_SIZE:** Cacheline Size: This register is implemented as R/W with default as 0. Similar to other Intel IPs.

3.24.5 reg_BAR_type (BAR)—Offset 10h

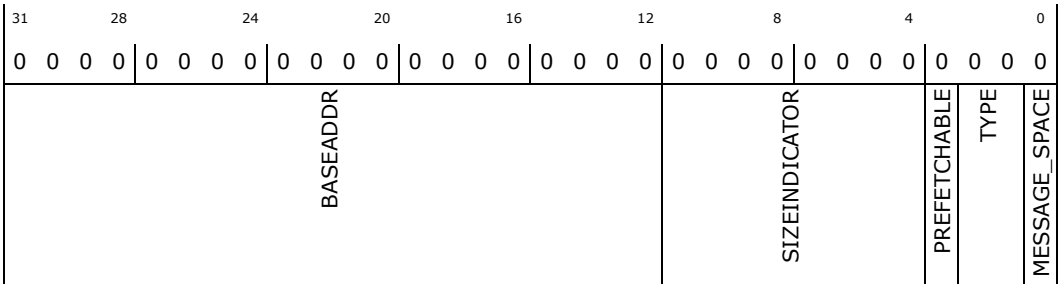
BAR -Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BAR: [0/21/0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Base Address register
11:4	00h RO	**SIZEINDICATOR:** Size indicator
3	0h RO	**PREFETCHABLE:** Indicates that this BAR is not prefetchable.
2:1	0h RO	**TYPE:** 00 indicates BAR lies in 32bit address range
0	0h RO	**MESSAGE_SPACE:** message space

3.24.6 reg_BAR1_type (BAR1)—Offset 14h

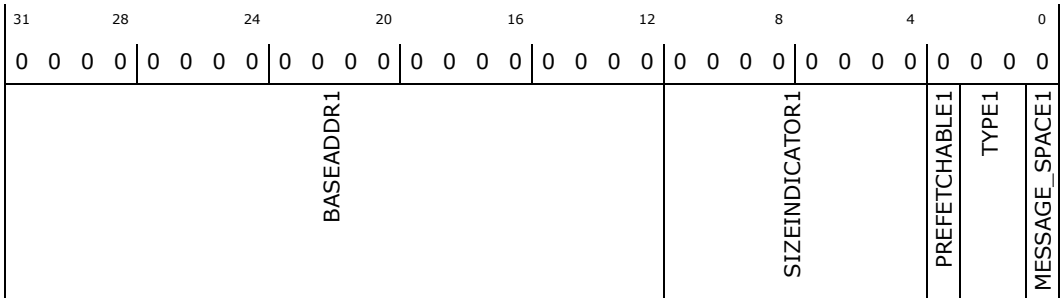
BAR1 -Base Address Register1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BAR1: [0/21/0] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** This field is present if BAR1 is enabled through private configuration space. Memory accesses to BAR1 region are aliased to the PCI configuration space. The BAR1 region is always 4K.
11:4	00h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Indicates that this BAR is not prefetchable
2:1	0h RO	**TYPE1:** 00 indicates BAR lies in 32bit address range
0	0h RO	**MESSAGE_SPACE1:** message space

3.24.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

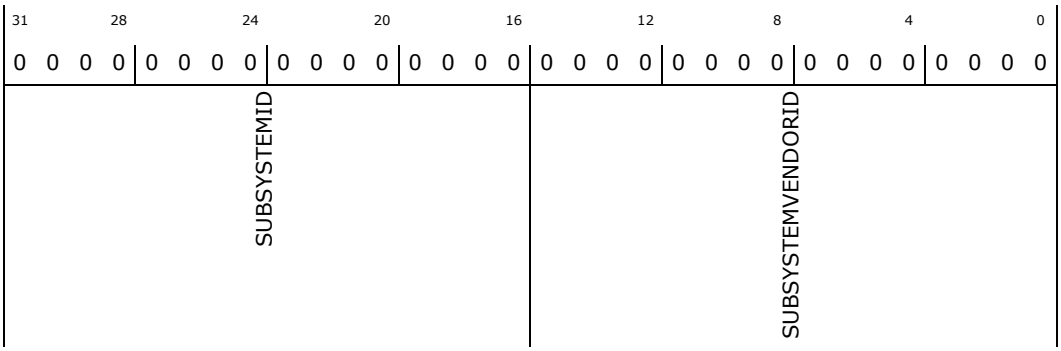
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SUBSYSTEMID: [0/21/0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Subsystem ID
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor

3.24.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

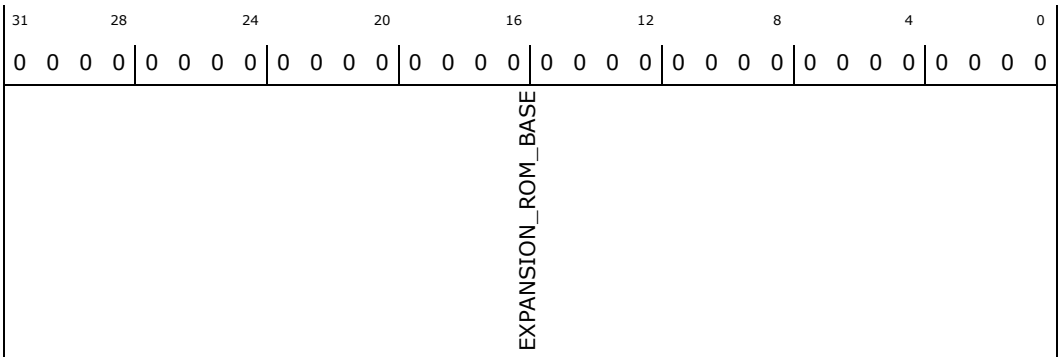
EXPANSION ROM base address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [0/21/0] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Value of all zeros indicates no support for Expansion ROM

3.24.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

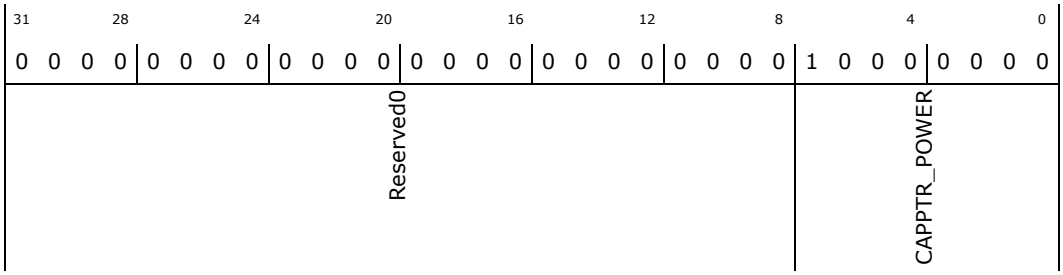
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITYPTR: [0/21/0] + 34h

Default: 00000080h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** reserved
7:0	80h RO	**CAPPTR_POWER:** Indicates what the next capability is. This capability points to the PM Capability, 0x80, structure.

3.24.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

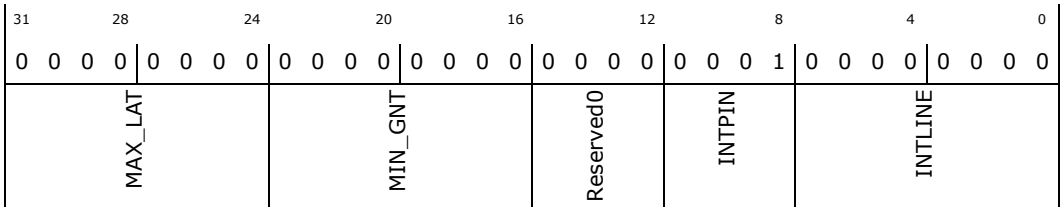
INTERRUPTREG - Interrupt Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

INTERRUPTREG: [0/21/0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** reserved
11:8	1h RO	**INTPIN:** Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space. For a single function device, this ideally is INTA
7:0	00h RW	**INTLINE:** Bridge does not use this field directly. It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

3.24.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

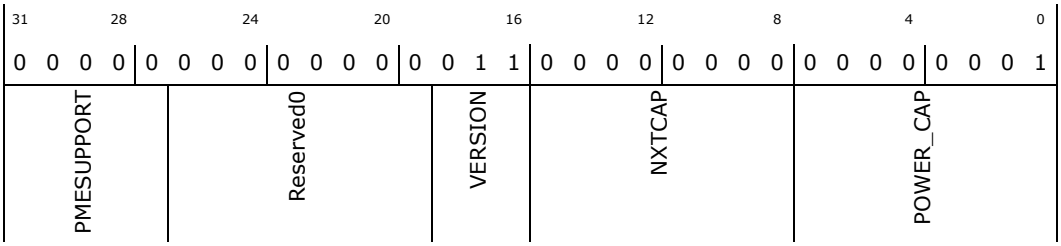
POWERCAPID - PowerManagement Capability ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

POWERCAPID: [0/21/0] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal at the same time in that power state. bit 11 X XXX1b: PME# can be asserted from D0 bit 12 X XX1Xb: PME# can be asserted from D1. Bridge does not support this state. bit 13 X X1XXb: PME# can be asserted from D2. Bridge does not support this state. bit 14 X 1XXXb:PME# can be asserted from D3hot bit 15 1 XXXXb:PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	00h RO	**Reserved0:** reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**NXTCAP:** Points to the next capability structure. This points to NULL

Bit Range	Default & Access	Description
7:0	01h RO	**POWER_CAP:** Indicates this is power management capability.

3.24.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

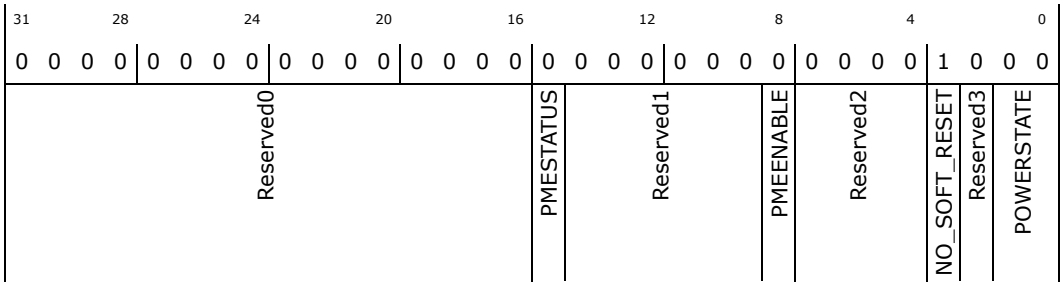
reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PMECTRLSTATUS: [0/21/0] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** reserved
15	0h RW/1C	**PMESTATUS:** 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PME Enable bit
14:9	00h RO	**Reserved1:** reserved
8	0h RW	**PMEENABLE:** pme enable
7:4	0h RO	**Reserved2:** reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset.Configuration Context is preserved.
2	0h RO	**Reserved3:** reserved

Bit Range	Default & Access	Description
1:0	0h RW	**POWERSTATE:** This field is used both to determine the current power state and to set a new power state.[BR]The values are: 00 D0 state 11 D3HOT state Others Reserved Note: If the software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally. The data is discarded and no state change occurs. Note: When in the D3HOT states, interrupts are blocked. D3Hot cannot be used for downstream decode on fabric ports.

3.24.13 reg_MANID_type (MANID)—Offset F8h

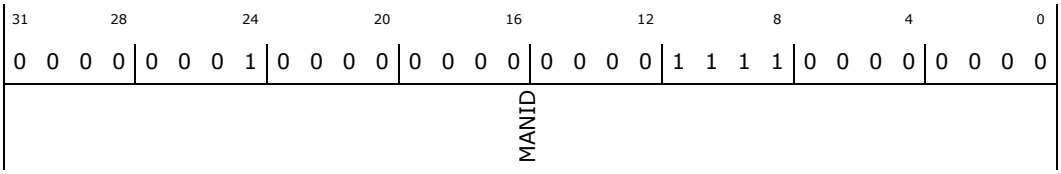
Manufacturers ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MANID: [0/21/0] + F8h

Default: 01000F00h



Bit Range	Default & Access	Description
31:0	01000f00h RO	**MANID:** Manufacturing ID

3.25 pci_mem Address Map

Table 33. Summary of Memory Mapped I/O Registers—0/21/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 2094	0F288086h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 2094	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 2096	04010000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 2096	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 2097	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 2097	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 2098	00000000h

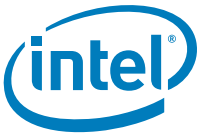


Table 33. Summary of Memory Mapped I/O Registers—0/21/0 (Continued)

Offset	Size	Register ID—Description	Default Value
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2099	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 2099	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 2100	00000100h
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 2101	00030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 2101	00000008h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 2102	01000F00h

3.25.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

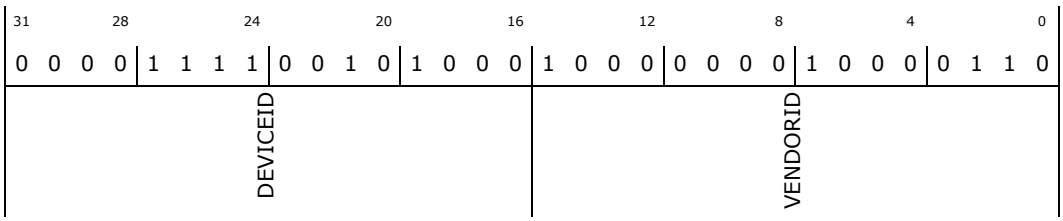
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEVVENDID: [0/21/0] + 0h

Default: 0F288086h



Bit Range	Default & Access	Description
31:16	0F28h RO	**DEVICEID:** Device ID
15:0	8086h RO	**VENDORID:** Vendor ID

3.25.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

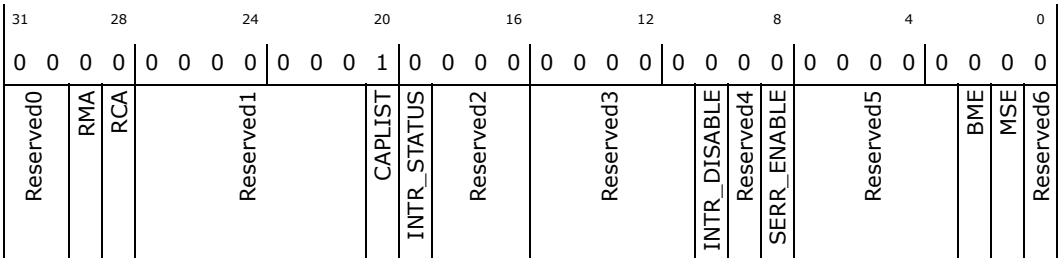
STATUSCOMMAND- Status and Command

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STATUSCOMMAND: [0/21/0] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** reserved
29	0h RW/1C	**RMA:** Received Master Abort: Not Implemented
28	0h RW/1C	**RCA:** Received Target Abort: Not Implemented
27:21	00h RO	**Reserved1:** reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** reserved
15:11	00h RO	**Reserved3:** reserved
10	0h RW	**INTR_DISABLE:** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does not send Interrupt Assert message through the IOSF Sideband Channel. Reset value of this bit is 0. This bit has no connection with the interrupt status bit
9	0h RO	**Reserved4:** reserved
8	0h RW	**SERR_ENABLE:** not implemented
7:3	00h RO	**Reserved5:** reserved
2	0h RW	**BME:** If this bit is 0,the Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**MSE:** Memory Space Enable: This bit controls Bridge response to downstream memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0h RO	**Reserved6:** reserved

3.25.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

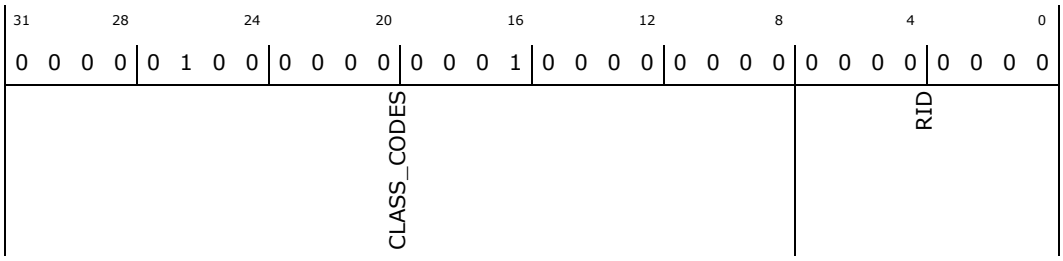
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

REVCLASSCODE: [0/21/0] + 8h

Default: 04010000h



Bit Range	Default & Access	Description
31:8	040100h RO	**CLASS_CODES:** Class Code
7:0	00h RO	**RID:** Revision ID

3.25.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

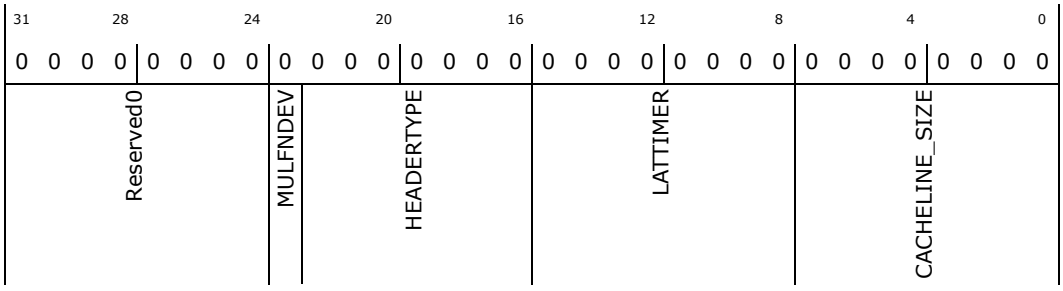
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CLLATHEADERBIST: [0/21/0] + Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved

Bit Range	Default & Access	Description
23	0h RO	**MULFNDEV:** MULFNDEV
22:16	00h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	00h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0. Similar to other Intel IPs.
7:0	00h RW	**CACHELINE_SIZE:** Cacheline Size: This register is implemented as R/W with default as 0. Similar to other Intel IPs.

3.25.5 reg_BAR_type (BAR)—Offset 10h

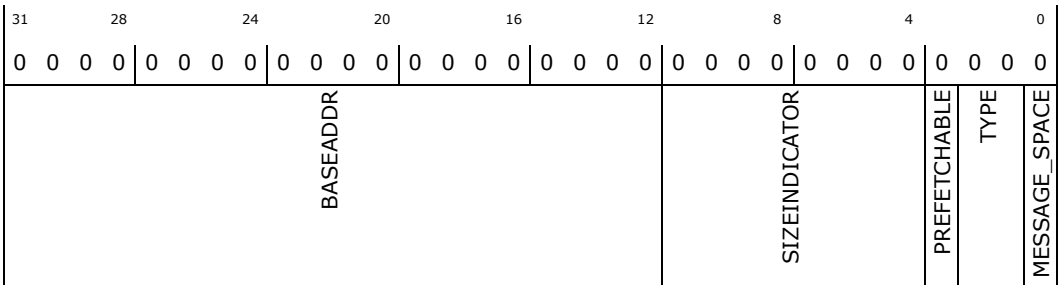
BAR -Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BAR: [0/21/0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Base Address register
11:4	00h RO	**SIZEINDICATOR:** Size indicator
3	0h RO	**PREFETCHABLE:** Indicates that this BAR is not prefetchable.
2:1	0h RO	**TYPE:** 00 indicates BAR lies in 32bit address range
0	0h RO	**MESSAGE_SPACE:** message space

3.25.6 reg_BAR1_type (BAR1)—Offset 14h

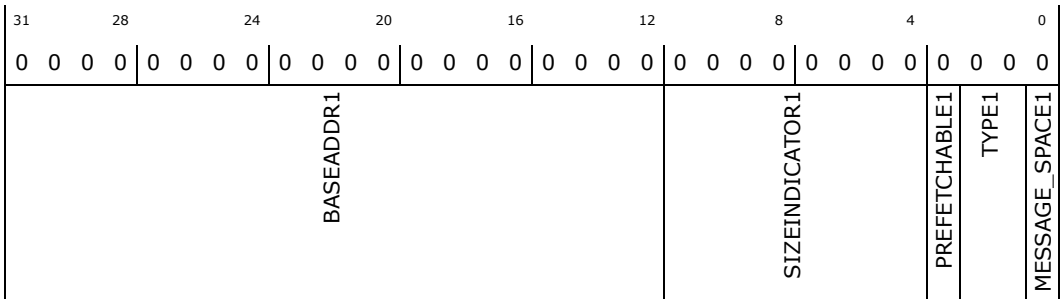
BAR1 -Base Address Register1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BAR1: [0/21/0] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** This field is present if BAR1 is enabled through private configuration space. Memory accesses to BAR1 region are aliased to the PCI configuration space. The BAR1 region is always 4K.
11:4	00h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Indicates that this BAR is not prefetchable
2:1	0h RO	**TYPE1:** 00 indicates BAR lies in 32bit address range
0	0h RO	**MESSAGE_SPACE1:** message space

3.25.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

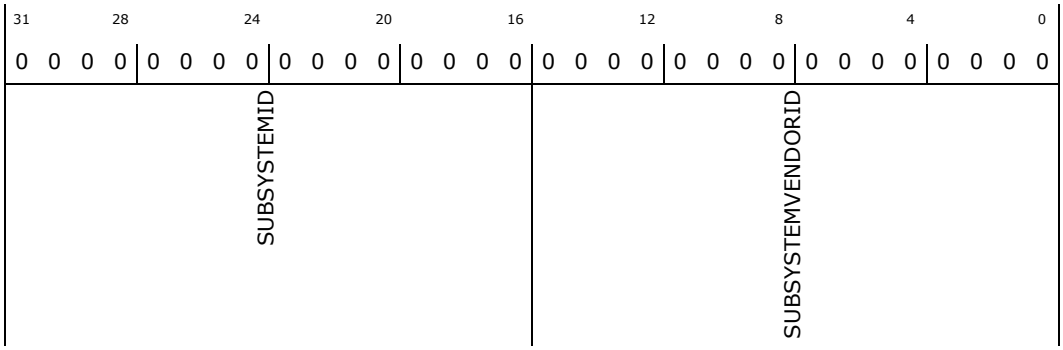
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SUBSYSTEMID: [0/21/0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Subsystem ID
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor

3.25.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

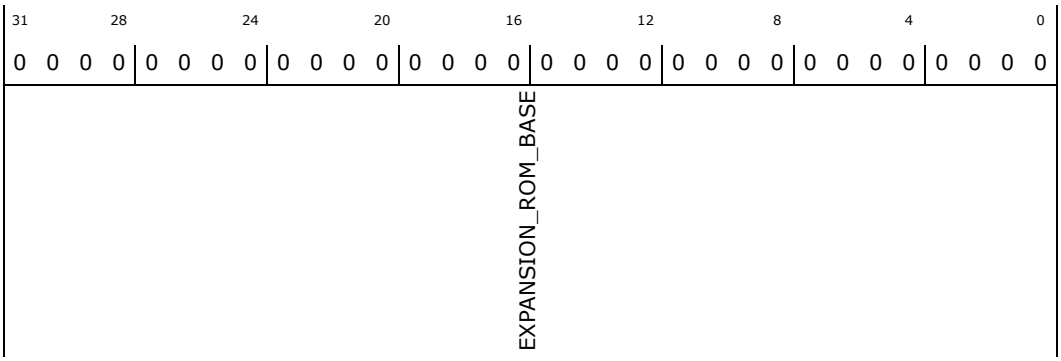
EXPANSION ROM base address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [0/21/0] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Value of all zeros indicates no support for Expansion ROM

3.25.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

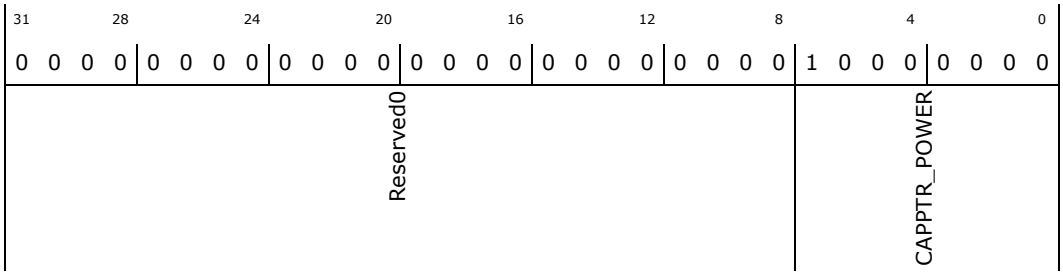
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITYPTR: [0/21/0] + 34h

Default: 00000080h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** reserved
7:0	80h RO	**CAPPTR_POWER:** Indicates what the next capability is. This capability points to the PM Capability, 0x80, structure.

3.25.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

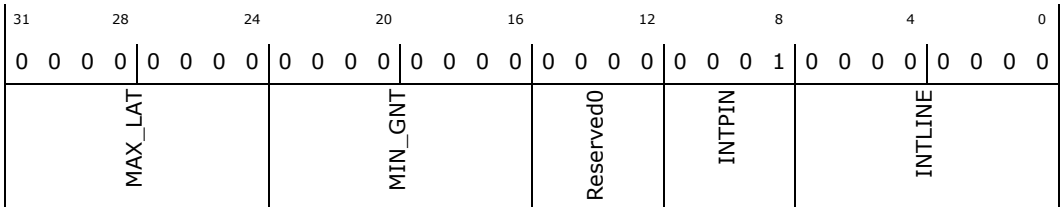
INTERRUPTREG - Interrupt Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

INTERRUPTREG: [0/21/0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** reserved
11:8	1h RO	**INTPIN:** Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space. For a single function device, this ideally is INTA
7:0	00h RW	**INTLINE:** Bridge does not use this field directly. It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

3.25.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

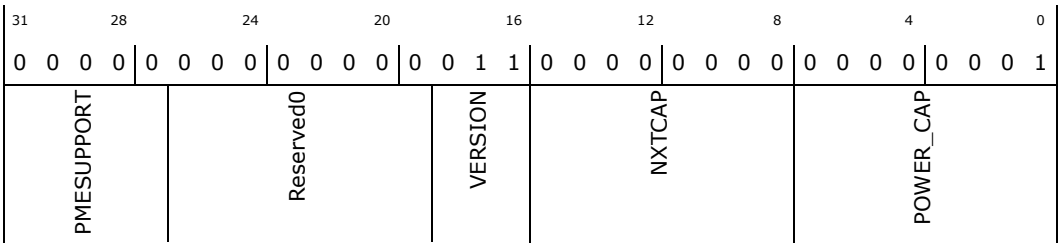
POWERCAPID - PowerManagement Capability ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

POWERCAPID: [0/21/0] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal at the same time in that power state. bit 11 X XXX1b: PME# can be asserted from D0 bit 12 X XX1Xb: PME# can be asserted from D1. Bridge does not support this state. bit 13 X X1XXb: PME# can be asserted from D2. Bridge does not support this state. bit 14 X 1XXXb:PME# can be asserted from D3hot bit 15 1 XXXXb:PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	00h RO	**Reserved0:** reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**NXTCAP:** Points to the next capability structure. This points to NULL
7:0	01h RO	**POWER_CAP:** Indicates this is power management capability.

3.25.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

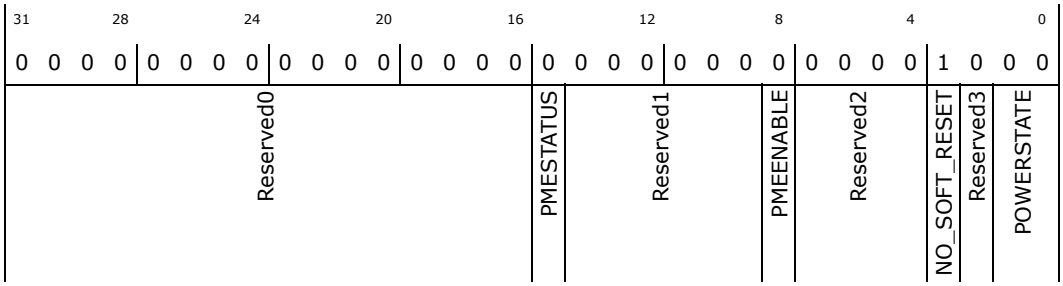
reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PMECTRLSTATUS: [0/21/0] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** reserved
15	0h RW/1C	**PMESTATUS:** 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PME Enable bit
14:9	00h RO	**Reserved1:** reserved
8	0h RW	**PMEENABLE:** pme enable
7:4	0h RO	**Reserved2:** reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset.Configuration Context is preserved.
2	0h RO	**Reserved3:** reserved
1:0	0h RW	**POWERSTATE:** This field is used both to determine the current power state and to set a new power state.[BR]The values are: 00 D0 state 11 D3HOT state Others Reserved Note: If the software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally. The data is discarded and no state change occurs. Note: When in the D3HOT states, interrupts are blocked. D3Hot cannot be used for downstream decode on fabric ports.

3.25.13 reg_MANID_type (MANID)—Offset F8h

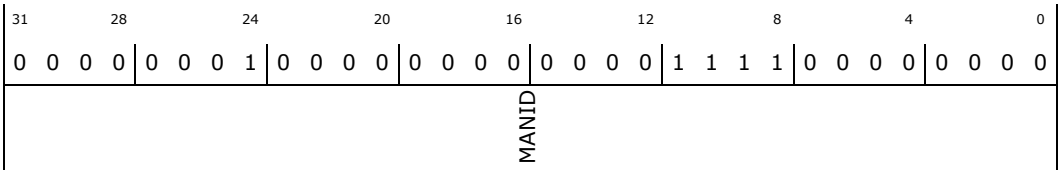
Manufacturers ID

Access Method

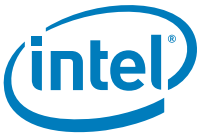
Type: Memory Mapped I/O Register (Size: 32 bits)

MANID: [0/21/0] + F8h

Default: 01000F00h



Bit Range	Default & Access	Description
31:0	01000f00h RO	**MANID:** Manufacturing ID



3.26 SIO HSUART, PWM, and SPI DMA PCI Configuration Registers

Table 34. Summary of SIO HSUART, PWM, and SPI DMA PCI Configuration Registers—0/30/0

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2104	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2105	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2106	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2107	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2108	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2108	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2109	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2110	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2110	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2111	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2111	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2112	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2113	00000000h

3.26.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:30, F:0] + 0h

Default: 00008086h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

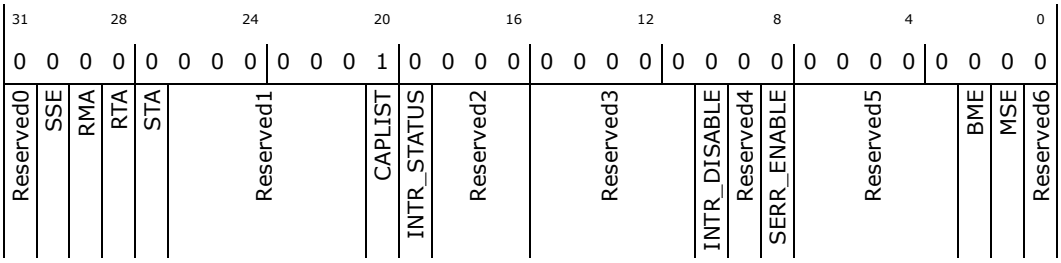
3.26.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:30, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.

Bit Range	Default & Access	Description
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

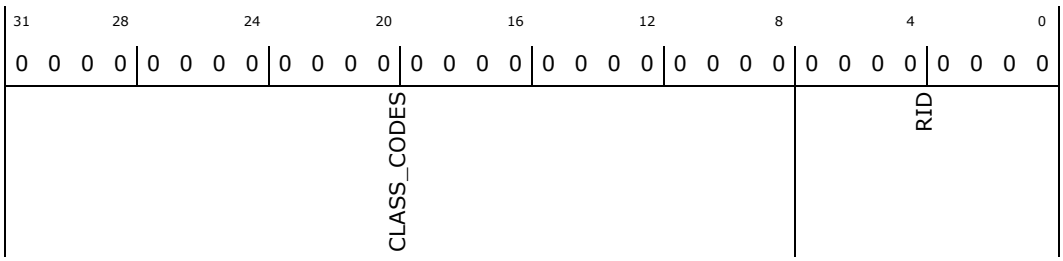
3.26.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:30, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

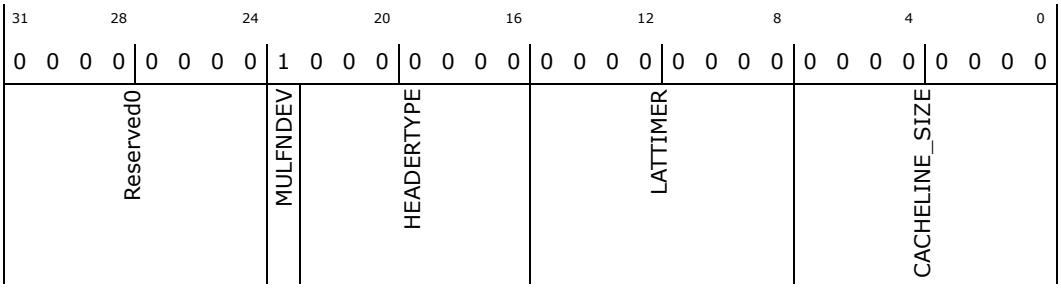
3.26.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:30, F:0] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

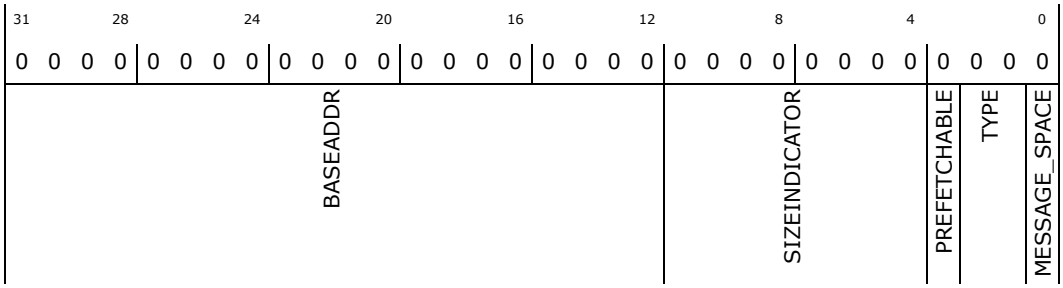
3.26.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

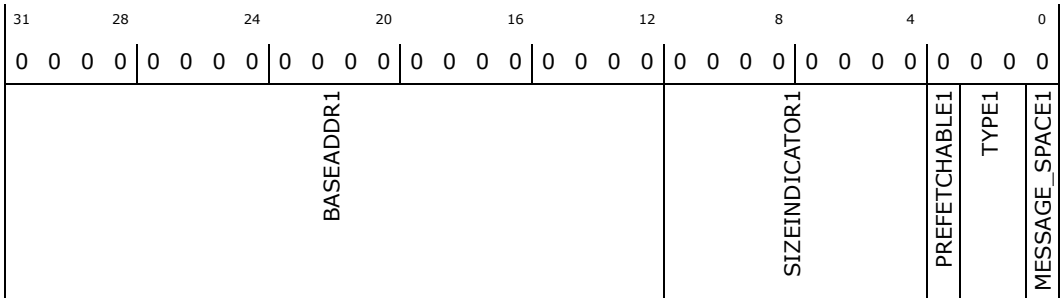
3.26.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:30, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

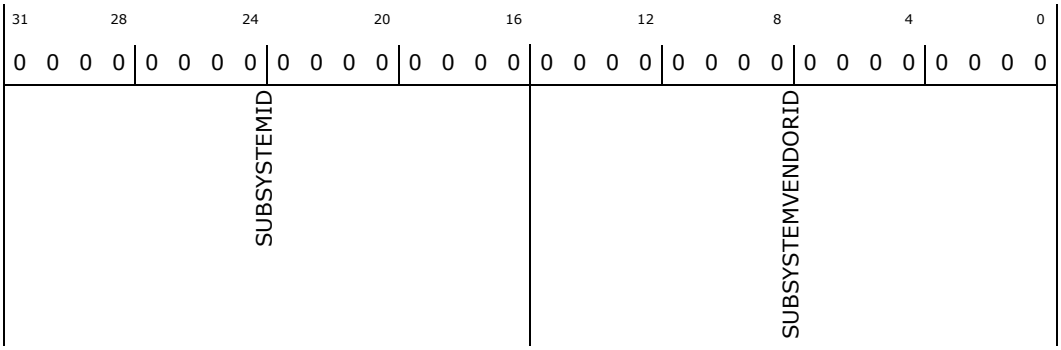
3.26.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:30, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

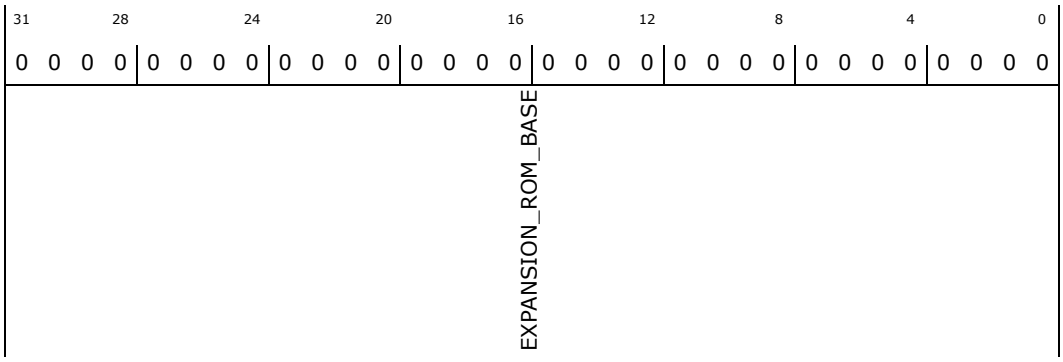
3.26.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:30, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

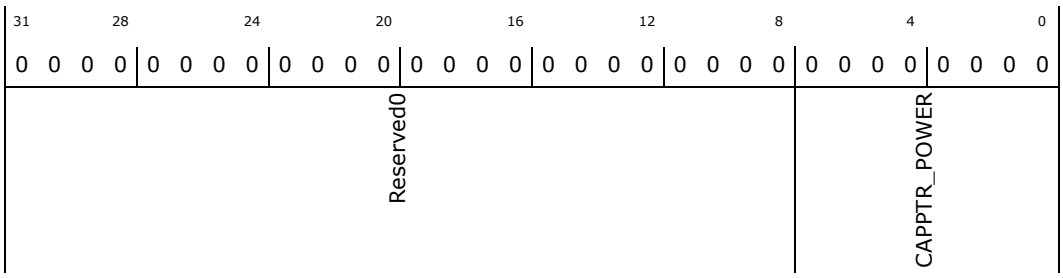
3.26.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:30, F:0] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

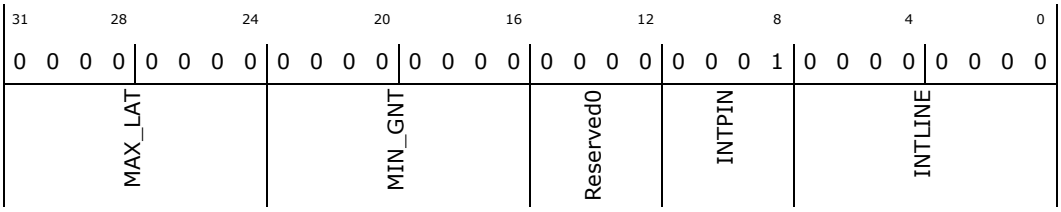
3.26.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

INTERRUPTREG: [B:0, D:30, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

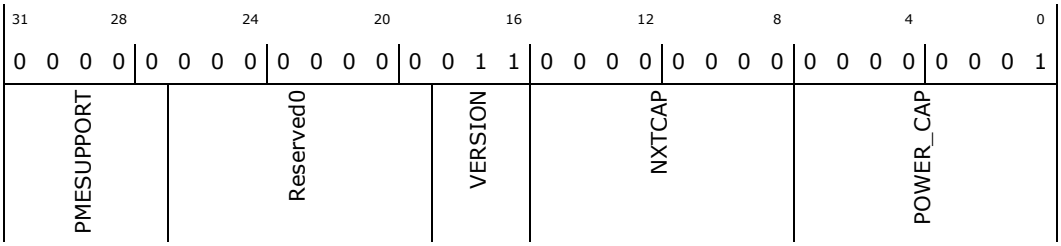
3.26.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

POWERCAPID: [B:0, D:30, F:0] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

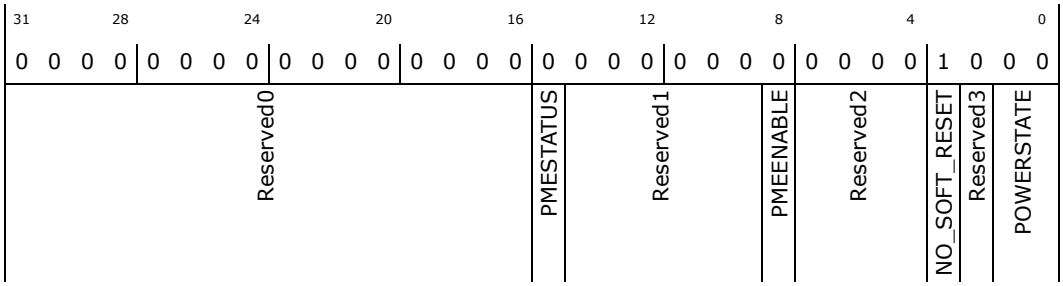
3.26.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:30, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

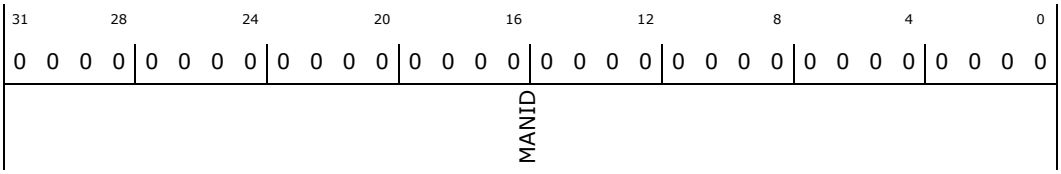
3.26.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:30, F:0] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

3.27 SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers

Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"Source Address Register for Channel 0 - Low (SAR0_LO)—Offset 0h" on page 2126	00000000h
4h	4	"Source Address Register for Channel 0 - High (SAR0_HI)—Offset 4h" on page 2126	00000000h
8h	4	"Destination Address Register for Channel 0 - Low (DAR0_LO)—Offset 8h" on page 2127	00000000h
Ch	4	"Destination Address Register for Channel 0 - High (DAR0_HI)—Offset Ch" on page 2127	00000000h
10h	4	"Linked List Pointer Register for Channel 0 - Low (LLP0_LO)—Offset 10h" on page 2128	00000000h
14h	4	"Linked List Pointer Register for Channel 0 - High (LLP0_HI)—Offset 14h" on page 2128	00000000h
18h	4	"Control Register for Channel 0 - Low (CTL0_LO)—Offset 18h" on page 2129	00304801h
1Ch	4	"Control Register for Channel 0 - High (CTL0_HI)—Offset 1Ch" on page 2131	00000002h
20h	4	"Source Status Register for Channel 0 - Low (SSTAT0_LO)—Offset 20h" on page 2132	00000000h
24h	4	"Source Status Register for Channel 0 - High (SSTAT0_HI)—Offset 24h" on page 2132	00000000h
28h	4	"Dest Status Register for Channel 0 - Low (DSTAT0_LO)—Offset 28h" on page 2133	00000000h
2Ch	4	"Dest Status Register for Channel 0 - High (DSTAT0_HI)—Offset 2Ch" on page 2133	00000000h
30h	4	"Source Status Address Register for Channel 0 - Low (SSTATAR0_LO)—Offset 30h" on page 2134	00000000h
34h	4	"Source Status Address Register for Channel 0 - High (SSTATAR0_HI)—Offset 34h" on page 2134	00000000h
38h	4	"Dest Status Address Register for Channel 0 - Low (DSTATAR0_LO)—Offset 38h" on page 2135	00000000h
3Ch	4	"Dest Status Address Register for Channel 0 - High (DSTATAR0_HI)—Offset 3Ch" on page 2135	00000000h
40h	4	"Configuration Register for Channel 0 - Low (CFG0_LO)—Offset 40h" on page 2136	00000E00h
44h	4	"Configuration Register for Channel 0 - High (CFG0_HI)—Offset 44h" on page 2137	00000004h
48h	4	"Source Gather Register for Channel 0 - Low (SGR0_LO)—Offset 48h" on page 2139	00000000h

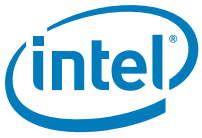


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
4Ch	4	"Source Gather Register for Channel 0 - High (SGR0_HI)—Offset 4Ch" on page 2139	00000000h
50h	4	"Destination Scatter Register for Channel 0 - Low (DSR0_LO)—Offset 50h" on page 2140	00000000h
54h	4	"Dest Scatter Register for Channel 0 - High (DSR0_HI)—Offset 54h" on page 2140	00000000h
58h	4	"Source Address Register for Channel 1 - Low (SAR1_LO)—Offset 58h" on page 2141	00000000h
5Ch	4	"Source Address Register for Channel 1 - High (SAR1_HI)—Offset 5Ch" on page 2141	00000000h
60h	4	"Destination Address Register for Channel 1 - Low (DAR1_LO)—Offset 60h" on page 2142	00000000h
64h	4	"Destination Address Register for Channel 1 - High (DAR1_HI)—Offset 64h" on page 2142	00000000h
68h	4	"Linked List Pointer Register for Channel 1 - Low (LLP1_LO)—Offset 68h" on page 2143	00000000h
6Ch	4	"Linked List Pointer Register for Channel 1 - High (LLP1_HI)—Offset 6Ch" on page 2143	00000000h
70h	4	"Control Register for Channel 1 - Low (CTL1_LO)—Offset 70h" on page 2144	00304801h
74h	4	"Control Register for Channel 1 - High (CTL1_HI)—Offset 74h" on page 2145	00000002h
78h	4	"Source Status Register for Channel 1 - Low (SSTAT1_LO)—Offset 78h" on page 2146	00000000h
7Ch	4	"Source Status Register for Channel 1 - High (SSTAT1_HI)—Offset 7Ch" on page 2146	00000000h
80h	4	"Dest Status Register for Channel 1 - Low (DSTAT1_LO)—Offset 80h" on page 2147	00000000h
84h	4	"Dest Status Register for Channel 1 - High (DSTAT1_HI)—Offset 84h" on page 2147	00000000h
88h	4	"Source Status Address Register for Channel 1 - Low (SSTATAR1_LO)—Offset 88h" on page 2148	00000000h
8Ch	4	"Source Status Address Register for Channel 1 - High (SSTATAR1_HI)—Offset 8Ch" on page 2148	00000000h
90h	4	"Dest Status Address Register for Channel 1 - Low (DSTATAR1_LO)—Offset 90h" on page 2149	00000000h
94h	4	"Dest Status Address Register for Channel 1 - High (DSTATAR1_HI)—Offset 94h" on page 2149	00000000h
98h	4	"Configuration Register for Channel 1 - Low (CFG1_LO)—Offset 98h" on page 2150	00000E20h
9Ch	4	"Configuration Register for Channel 1 - High (CFG1_HI)—Offset 9Ch" on page 2151	00000004h

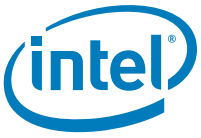


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
A0h	4	"Source Gather Register for Channel 1 - Low (SGR1_LO)—Offset A0h" on page 2153	00000000h
A4h	4	"Source Gather Register for Channel 1 - High (SGR1_HI)—Offset A4h" on page 2153	00000000h
A8h	4	"Destination Scatter Register for Channel 1 - Low (DSR1_LO)—Offset A8h" on page 2154	00000000h
ACh	4	"Dest Scatter Register for Channel 1 - High (DSR1_HI)—Offset ACh" on page 2154	00000000h
B0h	4	"Source Address Register for Channel 2 - Low (SAR2_LO)—Offset B0h" on page 2155	00000000h
B4h	4	"Source Address Register for Channel 2 - High (SAR2_HI)—Offset B4h" on page 2155	00000000h
B8h	4	"Destination Address Register for Channel 2 - Low (DAR2_LO)—Offset B8h" on page 2156	00000000h
BCh	4	"Destination Address Register for Channel 2 - High (DAR2_HI)—Offset BCh" on page 2156	00000000h
C0h	4	"Linked List Pointer Register for Channel 2 - Low (LLP2_LO)—Offset C0h" on page 2157	00000000h
C4h	4	"Linked List Pointer Register for Channel 2 - High (LLP2_HI)—Offset C4h" on page 2157	00000000h
C8h	4	"Control Register for Channel 2 - Low (CTL2_LO)—Offset C8h" on page 2158	00304801h
CCh	4	"Control Register for Channel 2 - High (CTL2_HI)—Offset CCh" on page 2159	00000002h
D0h	4	"Source Status Register for Channel 2 - Low (SSTAT2_LO)—Offset D0h" on page 2160	00000000h
D4h	4	"Source Status Register for Channel 2 - High (SSTAT2_HI)—Offset D4h" on page 2160	00000000h
D8h	4	"Dest Status Register for Channel 2 - Low (DSTAT2_LO)—Offset D8h" on page 2161	00000000h
DCh	4	"Dest Status Register for Channel 2 - High (DSTAT2_HI)—Offset DCh" on page 2161	00000000h
E0h	4	"Source Status Address Register for Channel 2 - Low (SSTATAR2_LO)—Offset E0h" on page 2162	00000000h
E4h	4	"Source Status Address Register for Channel 2 - High (SSTATAR2_HI)—Offset E4h" on page 2162	00000000h
E8h	4	"Dest Status Address Register for Channel 2 - Low (DSTATAR2_LO)—Offset E8h" on page 2163	00000000h
ECh	4	"Dest Status Address Register for Channel 2 - High (DSTATAR2_HI)—Offset ECh" on page 2163	00000000h
F0h	4	"Configuration Register for Channel 2 - Low (CFG2_LO)—Offset F0h" on page 2164	00000E40h

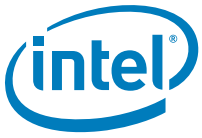


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
F4h	4	"Configuration Register for Channel 2 - High (CFG2_HI)—Offset F4h" on page 2165	00000004h
F8h	4	"Source Gather Register for Channel 2 - Low (SGR2_LO)—Offset F8h" on page 2166	00000000h
FCh	4	"Source Gather Register for Channel 2 - High (SGR2_HI)—Offset FCh" on page 2167	00000000h
100h	4	"Destination Scatter Register for Channel 2 - Low (DSR2_LO)—Offset 100h" on page 2167	00000000h
104h	4	"Dest Scatter Register for Channel 2 - High (DSR2_HI)—Offset 104h" on page 2168	00000000h
108h	4	"Source Address Register for Channel 3 - Low (SAR3_LO)—Offset 108h" on page 2168	00000000h
10Ch	4	"Source Address Register for Channel 3 - High (SAR3_HI)—Offset 10Ch" on page 2169	00000000h
110h	4	"Destination Address Register for Channel 3 - Low (DAR3_LO)—Offset 110h" on page 2169	00000000h
114h	4	"Destination Address Register for Channel 3 - High (DAR3_HI)—Offset 114h" on page 2170	00000000h
118h	4	"Linked List Pointer Register for Channel 3 - Low (LLP3_LO)—Offset 118h" on page 2170	00000000h
11Ch	4	"Linked List Pointer Register for Channel 3 - High (LLP3_HI)—Offset 11Ch" on page 2171	00000000h
120h	4	"Control Register for Channel 3 - Low (CTL3_LO)—Offset 120h" on page 2171	00304801h
124h	4	"Control Register for Channel 3 - High (CTL3_HI)—Offset 124h" on page 2173	00000002h
128h	4	"Source Status Register for Channel 3 - Low (SSTAT3_LO)—Offset 128h" on page 2173	00000000h
12Ch	4	"Source Status Register for Channel 3 - High (SSTAT3_HI)—Offset 12Ch" on page 2174	00000000h
130h	4	"Dest Status Register for Channel 3 - Low (DSTAT3_LO)—Offset 130h" on page 2174	00000000h
134h	4	"Dest Status Register for Channel 3 - High (DSTAT3_HI)—Offset 134h" on page 2175	00000000h
138h	4	"Source Status Address Register for Channel 3 - Low (SSTATAR3_LO)—Offset 138h" on page 2175	00000000h
13Ch	4	"Source Status Address Register for Channel 3 - High (SSTATAR3_HI)—Offset 13Ch" on page 2176	00000000h
140h	4	"Dest Status Address Register for Channel 3 - Low (DSTATAR3_LO)—Offset 140h" on page 2176	00000000h
144h	4	"Dest Status Address Register for Channel 3 - High (DSTATAR3_HI)—Offset 144h" on page 2177	00000000h

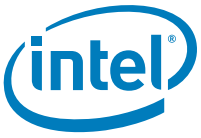


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
148h	4	"Configuration Register for Channel 3 - Low (CFG3_LO)—Offset 148h" on page 2177	00000E60h
14Ch	4	"Configuration Register for Channel 3 - High (CFG3_HI)—Offset 14Ch" on page 2179	00000004h
150h	4	"Source Gather Register for Channel 3 - Low (SGR3_LO)—Offset 150h" on page 2180	00000000h
154h	4	"Source Gather Register for Channel 3 - High (SGR3_HI)—Offset 154h" on page 2180	00000000h
158h	4	"Destination Scatter Register for Channel 3 - Low (DSR3_LO)—Offset 158h" on page 2181	00000000h
15Ch	4	"Dest Scatter Register for Channel 3 - High (DSR3_HI)—Offset 15Ch" on page 2181	00000000h
160h	4	"Source Address Register for Channel 4 - Low (SAR4_LO)—Offset 160h" on page 2182	00000000h
164h	4	"Source Address Register for Channel 4 - High (SAR4_HI)—Offset 164h" on page 2182	00000000h
168h	4	"Destination Address Register for Channel 4 - Low (DAR4_LO)—Offset 168h" on page 2183	00000000h
16Ch	4	"Destination Address Register for Channel 4 - High (DAR4_HI)—Offset 16Ch" on page 2183	00000000h
170h	4	"Linked List Pointer Register for Channel 4 - Low (LLP4_LO)—Offset 170h" on page 2184	00000000h
174h	4	"Linked List Pointer Register for Channel 4 - High (LLP4_HI)—Offset 174h" on page 2184	00000000h
178h	4	"Control Register for Channel 4 - Low (CTL4_LO)—Offset 178h" on page 2185	00304801h
17Ch	4	"Control Register for Channel 4 - High (CTL4_HI)—Offset 17Ch" on page 2186	00000002h
180h	4	"Source Status Register for Channel 4 - Low (SSTAT4_LO)—Offset 180h" on page 2187	00000000h
184h	4	"Source Status Register for Channel 4 - High (SSTAT4_HI)—Offset 184h" on page 2187	00000000h
188h	4	"Dest Status Register for Channel 4 - Low (DSTAT4_LO)—Offset 188h" on page 2188	00000000h
18Ch	4	"Dest Status Register for Channel 4 - High (DSTAT4_HI)—Offset 18Ch" on page 2188	00000000h
190h	4	"Source Status Address Register for Channel 4 - Low (SSTATAR4_LO)—Offset 190h" on page 2189	00000000h
194h	4	"Source Status Address Register for Channel 4 - High (SSTATAR4_HI)—Offset 194h" on page 2189	00000000h
198h	4	"Dest Status Address Register for Channel 4 - Low (DSTATAR4_LO)—Offset 198h" on page 2190	00000000h

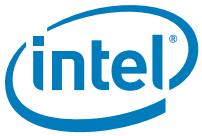


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
19Ch	4	"Dest Status Address Register for Channel 4 - High (DSTATAR4_HI)—Offset 19Ch" on page 2190	00000000h
1A0h	4	"Configuration Register for Channel 4 - Low (CFG4_LO)—Offset 1A0h" on page 2191	00000E80h
1A4h	4	"Configuration Register for Channel 4 - High (CFG4_HI)—Offset 1A4h" on page 2192	00000004h
1A8h	4	"Source Gather Register for Channel 4 - Low (SGR4_LO)—Offset 1A8h" on page 2194	00000000h
1ACh	4	"Source Gather Register for Channel 4 - High (SGR4_HI)—Offset 1ACh" on page 2194	00000000h
1B0h	4	"Destination Scatter Register for Channel 4 - Low (DSR4_LO)—Offset 1B0h" on page 2195	00000000h
1B4h	4	"Dest Scatter Register for Channel 4 - High (DSR4_HI)—Offset 1B4h" on page 2195	00000000h
1B8h	4	"Source Address Register for Channel 5 - Low (SAR5_LO)—Offset 1B8h" on page 2196	00000000h
1BCh	4	"Source Address Register for Channel 5 - High (SAR5_HI)—Offset 1BCh" on page 2196	00000000h
1C0h	4	"Destination Address Register for Channel 5 - Low (DAR5_LO)—Offset 1C0h" on page 2197	00000000h
1C4h	4	"Destination Address Register for Channel 5 - High (DAR5_HI)—Offset 1C4h" on page 2197	00000000h
1C8h	4	"Linked List Pointer Register for Channel 5 - Low (LLP5_LO)—Offset 1C8h" on page 2198	00000000h
1CCh	4	"Linked List Pointer Register for Channel 5 - High (LLP5_HI)—Offset 1CCh" on page 2198	00000000h
1D0h	4	"Control Register for Channel 5 - Low (CTL5_LO)—Offset 1D0h" on page 2199	00304801h
1D4h	4	"Control Register for Channel 5 - High (CTL5_HI)—Offset 1D4h" on page 2200	00000002h
1D8h	4	"Source Status Register for Channel 5 - Low (SSTAT5_LO)—Offset 1D8h" on page 2201	00000000h
1DCh	4	"Source Status Register for Channel 5 - High (SSTAT5_HI)—Offset 1DCh" on page 2201	00000000h
1E0h	4	"Dest Status Register for Channel 5 - Low (DSTAT5_LO)—Offset 1E0h" on page 2202	00000000h
1E4h	4	"Dest Status Register for Channel 5 - High (DSTAT5_HI)—Offset 1E4h" on page 2202	00000000h
1E8h	4	"Source Status Address Register for Channel 5 - Low (SSTATAR5_LO)—Offset 1E8h" on page 2203	00000000h
1ECh	4	"Source Status Address Register for Channel 5 - High (SSTATAR5_HI)—Offset 1ECh" on page 2203	00000000h

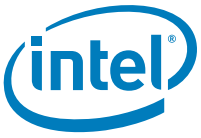


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
1F0h	4	"Dest Status Address Register for Channel 5 - Low (DSTATAR5_LO)—Offset 1F0h" on page 2204	00000000h
1F4h	4	"Dest Status Address Register for Channel 5 - High (DSTATAR5_HI)—Offset 1F4h" on page 2204	00000000h
1F8h	4	"Configuration Register for Channel 5 - Low (CFG5_LO)—Offset 1F8h" on page 2205	00000EA0h
1FCh	4	"Configuration Register for Channel 5 - High (CFG5_HI)—Offset 1FCh" on page 2206	00000004h
200h	4	"Source Gather Register for Channel 5 - Low (SGR5_LO)—Offset 200h" on page 2207	00000000h
204h	4	"Source Gather Register for Channel 5 - High (SGR5_HI)—Offset 204h" on page 2208	00000000h
208h	4	"Destination Scatter Register for Channel 5 - Low (DSR5_LO)—Offset 208h" on page 2208	00000000h
20Ch	4	"Dest Scatter Register for Channel 5 - High (DSR5_HI)—Offset 20Ch" on page 2209	00000000h
210h	4	"Source Address Register for Channel 6 - Low (SAR6_LO)—Offset 210h" on page 2209	00000000h
214h	4	"Source Address Register for Channel 6 - High (SAR6_HI)—Offset 214h" on page 2210	00000000h
218h	4	"Destination Address Register for Channel 6 - Low (DAR6_LO)—Offset 218h" on page 2210	00000000h
21Ch	4	"Destination Address Register for Channel 6 - High (DAR6_HI)—Offset 21Ch" on page 2211	00000000h
220h	4	"Linked List Pointer Register for Channel 6 - Low (LLP6_LO)—Offset 220h" on page 2211	00000000h
224h	4	"Linked List Pointer Register for Channel 6 - High (LLP6_HI)—Offset 224h" on page 2212	00000000h
228h	4	"Control Register for Channel 6 - Low (CTL6_LO)—Offset 228h" on page 2212	00304801h
22Ch	4	"Control Register for Channel 6 - High (CTL6_HI)—Offset 22Ch" on page 2214	00000002h
230h	4	"Source Status Register for Channel 6 - Low (SSTAT6_LO)—Offset 230h" on page 2214	00000000h
234h	4	"Source Status Register for Channel 6 - High (SSTAT6_HI)—Offset 234h" on page 2215	00000000h
238h	4	"Dest Status Register for Channel 6 - Low (DSTAT6_LO)—Offset 238h" on page 2215	00000000h
23Ch	4	"Dest Status Register for Channel 6 - High (DSTAT6_HI)—Offset 23Ch" on page 2216	00000000h
240h	4	"Source Status Address Register for Channel 6 - Low (SSTATAR6_LO)—Offset 240h" on page 2216	00000000h

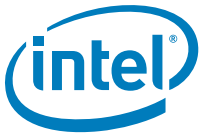


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
244h	4	"Source Status Address Register for Channel 6 - High (SSTATAR6_HI)—Offset 244h" on page 2217	00000000h
248h	4	"Dest Status Address Register for Channel 6 - Low (DSTATAR6_LO)—Offset 248h" on page 2217	00000000h
24Ch	4	"Dest Status Address Register for Channel 6 - High (DSTATAR6_HI)—Offset 24Ch" on page 2218	00000000h
250h	4	"Configuration Register for Channel 6 - Low (CFG6_LO)—Offset 250h" on page 2218	00000EC0h
254h	4	"Configuration Register for Channel 6 - High (CFG6_HI)—Offset 254h" on page 2220	00000004h
258h	4	"Source Gather Register for Channel 6 - Low (SGR6_LO)—Offset 258h" on page 2221	00000000h
25Ch	4	"Source Gather Register for Channel 6 - High (SGR6_HI)—Offset 25Ch" on page 2221	00000000h
260h	4	"Destination Scatter Register for Channel 6 - Low (DSR6_LO)—Offset 260h" on page 2222	00000000h
264h	4	"Dest Scatter Register for Channel 6 - High (DSR6_HI)—Offset 264h" on page 2222	00000000h
268h	4	"Source Address Register for Channel 7 - Low (SAR7_LO)—Offset 268h" on page 2223	00000000h
26Ch	4	"Source Address Register for Channel 7 - High (SAR7_HI)—Offset 26Ch" on page 2223	00000000h
270h	4	"Destination Address Register for Channel 7 - Low (DAR7_LO)—Offset 270h" on page 2224	00000000h
274h	4	"Destination Address Register for Channel 7 - High (DAR7_HI)—Offset 274h" on page 2224	00000000h
278h	4	"Linked List Pointer Register for Channel 7 - Low (LLP7_LO)—Offset 278h" on page 2225	00000000h
27Ch	4	"Linked List Pointer Register for Channel 7 - High (LLP7_HI)—Offset 27Ch" on page 2225	00000000h
280h	4	"Control Register for Channel 7 - Low (CTL7_LO)—Offset 280h" on page 2226	00304801h
284h	4	"Control Register for Channel 7 - High (CTL7_HI)—Offset 284h" on page 2227	00000002h
288h	4	"Source Status Register for Channel 7 - Low (SSTAT7_LO)—Offset 288h" on page 2228	00000000h
28Ch	4	"Source Status Register for Channel 7 - High (SSTAT7_HI)—Offset 28Ch" on page 2228	00000000h
290h	4	"Dest Status Register for Channel 7 - Low (DSTAT7_LO)—Offset 290h" on page 2229	00000000h
294h	4	"Dest Status Register for Channel 7 - High (DSTAT7_HI)—Offset 294h" on page 2229	00000000h

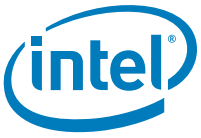


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
298h	4	"Source Status Address Register for Channel 7 - Low (SSTATAR7_LO)—Offset 298h" on page 2230	00000000h
29Ch	4	"Source Status Address Register for Channel 7 - High (SSTATAR7_HI)—Offset 29Ch" on page 2230	00000000h
2A0h	4	"Dest Status Address Register for Channel 7 - Low (DSTATAR7_LO)—Offset 2A0h" on page 2231	00000000h
2A4h	4	"Dest Status Address Register for Channel 7 - High (DSTATAR7_HI)—Offset 2A4h" on page 2231	00000000h
2A8h	4	"Configuration Register for Channel 7 - Low (CFG7_LO)—Offset 2A8h" on page 2232	00000EE0h
2ACh	4	"Configuration Register for Channel 7 - High (CFG7_HI)—Offset 2ACh" on page 2233	00000004h
2B0h	4	"Source Gather Register for Channel 7 - Low (SGR7_LO)—Offset 2B0h" on page 2235	00000000h
2B4h	4	"Source Gather Register for Channel 7 - High (SGR7_HI)—Offset 2B4h" on page 2235	00000000h
2B8h	4	"Destination Scatter Register for Channel 7 - Low (DSR7_LO)—Offset 2B8h" on page 2236	00000000h
2BCh	4	"Dest Scatter Register for Channel 7 - High (DSR7_HI)—Offset 2BCh" on page 2236	00000000h
2C0h	4	"Interrupt Raw Status Registers - Low (RawTfr_LO)—Offset 2C0h" on page 2237	00000000h
2C4h	4	"Interrupt Raw Status Registers - High (RawTfr_HI)—Offset 2C4h" on page 2237	00000000h
2C8h	4	"Interrupt Raw Status Registers - Low (RawBlock_LO)—Offset 2C8h" on page 2238	00000000h
2CCh	4	"Interrupt Raw Status Registers - High (RawBlock_HI)—Offset 2CCh" on page 2238	00000000h
2D0h	4	"Interrupt Raw Status Registers - Low (RawSrcTran_LO)—Offset 2D0h" on page 2239	00000000h
2D4h	4	"Interrupt Raw Status Registers - High (RawSrcTran_HI)—Offset 2D4h" on page 2239	00000000h
2D8h	4	"Interrupt Raw Status Registers - Low (RawDstTran_LO)—Offset 2D8h" on page 2240	00000000h
2DCh	4	"Interrupt Raw Status Registers - High (RawDstTran_HI)—Offset 2DCh" on page 2240	00000000h
2E0h	4	"Interrupt Raw Status Registers - Low (RawErr_LO)—Offset 2E0h" on page 2241	00000000h
2E4h	4	"Interrupt Raw Status Registers - High (RawErr_HI)—Offset 2E4h" on page 2241	00000000h
2E8h	4	"Interrupt Status Registers - Low (StatusTfr_LO)—Offset 2E8h" on page 2242	00000000h

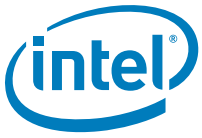


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
2ECh	4	"Interrupt Status Registers - High (StatusTfr_HI)—Offset 2ECh" on page 2243	00000000h
2F0h	4	"Interrupt Status Registers - Low (StatusBlock_LO)—Offset 2F0h" on page 2243	00000000h
2F4h	4	"Interrupt Status Registers - High (StatusBlock_HI)—Offset 2F4h" on page 2244	00000000h
2F8h	4	"Interrupt Status Registers - Low (StatusSrcTran_LO)—Offset 2F8h" on page 2244	00000000h
2FCh	4	"Interrupt Status Registers - High (StatusSrcTran_HI)—Offset 2FCh" on page 2245	00000000h
300h	4	"Interrupt Status Registers - Low (StatusDstTran_LO)—Offset 300h" on page 2245	00000000h
304h	4	"Interrupt Status Registers - High (StatusDstTran_HI)—Offset 304h" on page 2246	00000000h
308h	4	"Interrupt Status Registers - Low (StatusErr_LO)—Offset 308h" on page 2246	00000000h
30Ch	4	"Interrupt Status Registers - High (StatusErr_HI)—Offset 30Ch" on page 2247	00000000h
310h	4	"Interrupt Mask Registers - Low (MaskTfr_LO)—Offset 310h" on page 2247	00000000h
314h	4	"Interrupt Mask Registers - High (MaskTfr_HI)—Offset 314h" on page 2248	00000000h
318h	4	"Interrupt Mask Registers - Low (MaskBlock_LO)—Offset 318h" on page 2249	00000000h
31Ch	4	"Interrupt Mask Registers - High (MaskBlock_HI)—Offset 31Ch" on page 2249	00000000h
320h	4	"Interrupt Mask Registers - Low (MaskSrcTran_LO)—Offset 320h" on page 2250	00000000h
324h	4	"Interrupt Mask Registers - High (MaskSrcTran_HI)—Offset 324h" on page 2251	00000000h
328h	4	"Interrupt Mask Registers - Low (MaskDstTran_LO)—Offset 328h" on page 2251	00000000h
32Ch	4	"Interrupt Mask Registers - High (MaskDstTran_HI)—Offset 32Ch" on page 2252	00000000h
330h	4	"Interrupt Mask Registers - Low (MaskErr_LO)—Offset 330h" on page 2252	00000000h
334h	4	"Interrupt Mask Registers - High (MaskErr_HI)—Offset 334h" on page 2253	00000000h
338h	4	"Interrupt Clear Registers - Low (ClearTfr_LO)—Offset 338h" on page 2254	00000000h
33Ch	4	"Interrupt Clear Registers - High (ClearTfr_HI)—Offset 33Ch" on page 2254	00000000h

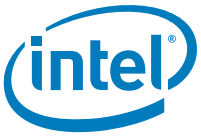


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
340h	4	"Interrupt Clear Registers - Low (ClearBlock_LO)—Offset 340h" on page 2255	00000000h
344h	4	"Interrupt Clear Registers (ClearBlock_HI)—Offset 344h" on page 2255	00000000h
348h	4	"Interrupt Clear Registers - Low (ClearSrcTran_LO)—Offset 348h" on page 2256	00000000h
34Ch	4	"Interrupt Clear RegistersClearSrc - High (ClearSrcTran_HI)—Offset 34Ch" on page 2256	00000000h
350h	4	"Interrupt Clear Registers - Low (ClearDstTran_LO)—Offset 350h" on page 2257	00000000h
354h	4	"Interrupt Clear Registers - High (ClearDstTran_HI)—Offset 354h" on page 2257	00000000h
358h	4	"Interrupt Clear Registers - Low (ClearErr_LO)—Offset 358h" on page 2258	00000000h
35Ch	4	"Interrupt Clear Registers - High (ClearErr_HI)—Offset 35Ch" on page 2259	00000000h
360h	4	"Combined Interrupt Status Register - Low (StatusInt_LO)—Offset 360h" on page 2259	00000000h
364h	4	"Combined Interrupt Status Register - High (StatusInt_HI)—Offset 364h" on page 2260	00000000h
368h	4	"Source Software Transaction Request Register - Low (ReqSrcReg_LO)—Offset 368h" on page 2260	00000000h
36Ch	4	"Source Software Transaction Request Register - High (ReqSrcReg_HI)—Offset 36Ch" on page 2261	00000000h
370h	4	"Destination Software Transaction Request Register - Low (ReqDstReg_LO)—Offset 370h" on page 2262	00000000h
374h	4	"Destination Software Transaction Request Register - High (ReqDstReg_HI)—Offset 374h" on page 2262	00000000h
378h	4	"Single Source Software Transaction Request Register - Low (SglRqSrcReg_LO)—Offset 378h" on page 2263	00000000h
37Ch	4	"Single Source Software Transaction Request Register - High (SglRqSrcReg_HI)—Offset 37Ch" on page 2264	00000000h
380h	4	"Single Destination Software Transaction Request Register - Low (SglRqDstReg_LO)—Offset 380h" on page 2264	00000000h
384h	4	"Single Destination Software Transaction Request Register - High (SglRqDstReg_HI)—Offset 384h" on page 2265	00000000h
388h	4	"Last Source Transaction Request Register - Low (LstSrcReg_LO)—Offset 388h" on page 2265	00000000h
38Ch	4	"Last Source Transaction Request Register - High (LstSrcReg_HI)—Offset 38Ch" on page 2266	00000000h
390h	4	"Last Destination Transaction Request Register - Low (LstDstReg_LO)—Offset 390h" on page 2267	00000000h

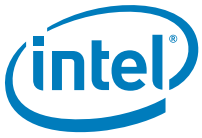


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
394h	4	"Last Destination Transaction Request Register - High (LstDstReg_HI)—Offset 394h" on page 2267	00000000h
398h	4	"DW_ahb_dmac Configuration Register - Low (DmaCfgReg_LO)—Offset 398h" on page 2268	00000000h
39Ch	4	"DW_ahb_dmac Configuration Register - High (DmaCfgReg_HI)—Offset 39Ch" on page 2268	00000000h
3A0h	4	"DW_ahb_dmac Channel Enable Register - Low (ChEnReg_LO)—Offset 3A0h" on page 2269	00000000h
3A4h	4	"DW_ahb_dmac Channel Enable Register - High (ChEnReg_HI)—Offset 3A4h" on page 2270	00000000h
3A8h	4	"DW_ahb_dmac ID Register - Low (DmaIdReg_LO)—Offset 3A8h" on page 2270	C0CAC01Ah
3ACh	4	"DW_ahb_dmac ID Register - High (DmaIdReg_HI)—Offset 3ACh" on page 2271	00000000h
3B0h	4	"DW_ahb_dmac Test Register - Low (DmaTestReg_LO)—Offset 3B0h" on page 2271	00000000h
3B4h	4	"DW_ahb_dmac Test Register - High (DmaTestReg_HI)—Offset 3B4h" on page 2272	00000000h
3C8h	4	"DW_ahb_dmac Component Parameters Register 6 - Low (DMA_COMP_PARAMS_6_LO)—Offset 3C8h" on page 2273	00000000h
3CCh	4	"DW_ahb_dmac Component Parameters Register 6 - High (DMA_COMP_PARAMS_6_HI)—Offset 3CCh" on page 2273	38220300h
3D0h	4	"DW_ahb_dmac Component Parameters Register 5 - Low (DMA_COMP_PARAMS_5_LO)—Offset 3D0h" on page 2276	38220300h
3D4h	4	"DW_ahb_dmac Component Parameters Register 5 - High (DMA_COMP_PARAMS_5_HI)—Offset 3D4h" on page 2279	38220300h
3D8h	4	"DW_ahb_dmac Component Parameters Register 4 - Low (DMA_COMP_PARAMS_4_LO)—Offset 3D8h" on page 2281	38220300h
3DCh	4	"DW_ahb_dmac Component Parameters Register 4 - High (DMA_COMP_PARAMS_4_HI)—Offset 3DCh" on page 2284	38220300h
3E0h	4	"DW_ahb_dmac Component Parameters Register 3 - Low (DMA_COMP_PARAMS_3_LO)—Offset 3E0h" on page 2287	38220300h
3E4h	4	"DW_ahb_dmac Component Parameters Register 3 - High (DMA_COMP_PARAMS_3_HI)—Offset 3E4h" on page 2290	38220300h
3E8h	4	"DW_ahb_dmac Component Parameters Register 2 - Low (DMA_COMP_PARAMS_2_LO)—Offset 3E8h" on page 2293	38220300h
3ECh	4	"DW_ahb_dmac Component Parameters Register 2 - High (DMA_COMP_PARAMS_2_HI)—Offset 3ECh" on page 2296	00000000h
3F0h	4	"DW_ahb_dmac Component Parameters Register 1 - Low (DMA_COMP_PARAMS_1_LO)—Offset 3F0h" on page 2298	AAAAAAAAh

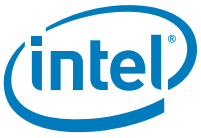


Table 35. Summary of SIO HSUART, PWM, and SPI DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
3F4h	4	"DW_ahb_dmac Component Parameters Register 1 - High (DMA_COMP_PARAMS_1_HI)—Offset 3F4h" on page 2299	37000F04h
3F8h	4	"DMA Component ID RegisterDma - Low (DmaCompsID_LO)—Offset 3F8h" on page 2302	44571110h
3FCh	4	"DMA Component ID Register - High (DmaCompsID_HI)—Offset 3FCh" on page 2302	3231362Ah

3.27.1 Source Address Register for Channel 0 - Low (SAR0_LO)—Offset 0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current AHB transfer.

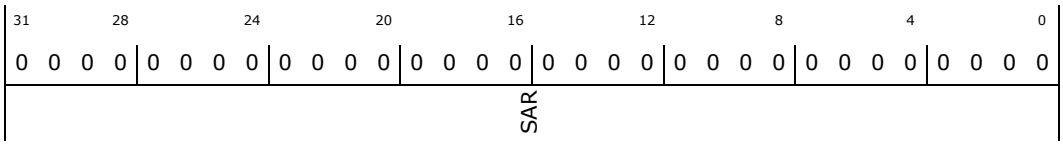
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR0_LO: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.27.2 Source Address Register for Channel 0 - High (SAR0_HI)—Offset 4h

Refer to the description for register Source Address Register for Channel 0 - Low.

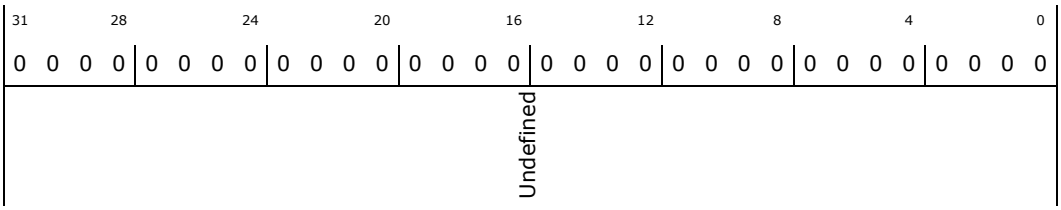
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR0_HI: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.3 Destination Address Register for Channel 0 - Low (DAR0_LO)—Offset 8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current AHB transfer.

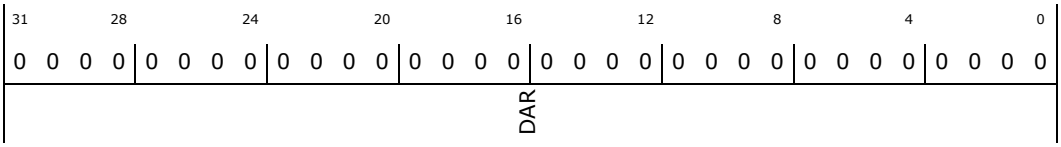
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR0_LO: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.27.4 Destination Address Register for Channel 0 - High (DAR0_HI)—Offset Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

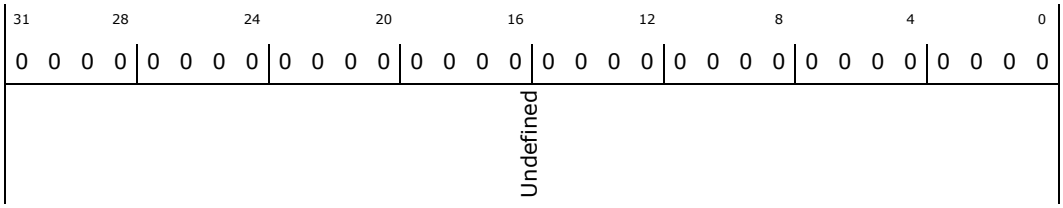
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR0_HI: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.5 Linked List Pointer Register for Channel 0 - Low (LLP0_LO)—Offset 10h

This register does not exist if the DMAH_CHx_HC_LLP configuration parameter is set to True. For further details, refer to the DesignWare DW_ahb_dmac Databook.

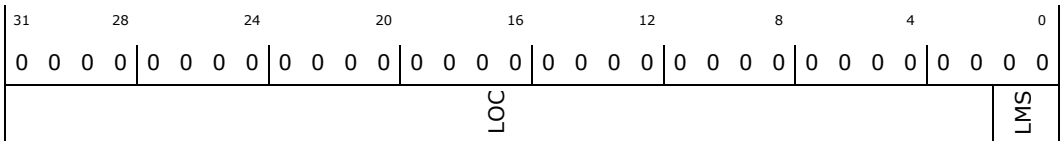
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP0_LO: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.27.6 Linked List Pointer Register for Channel 0 - High (LLP0_HI)—Offset 14h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

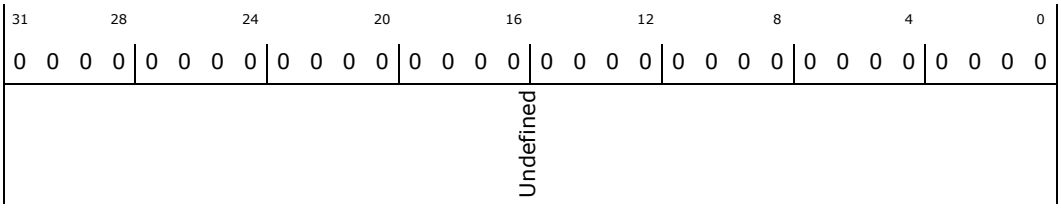
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP0_HI: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.7 Control Register for Channel 0 - Low (CTL0_LO)—Offset 18h

This register contains fields that control the DMA transfer. Refer to the DesignWare DW_ahb_dmac Databook for further details.

Note: You need to program this register prior to enabling the channel.

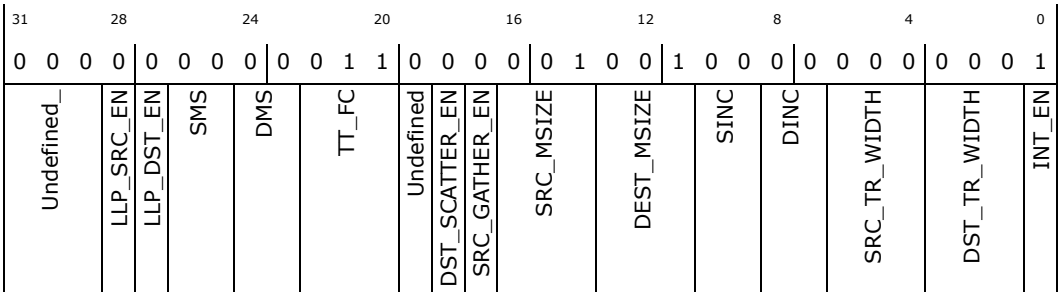
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL0_LO: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero

Bit Range	Default & Access	Description
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** The following transfer types are supported. • Memory to Memory • Memory to Peripheral • Peripheral to Memory • Peripheral to Peripheral Flow Control can be assigned to the DW_ahb_dmac, the source peripheral, or the destination peripheral. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Number of data items, each of width CTLx.SRC_TR_WIDTH, to be read from the source every time a source burst transaction request is made from either the corresponding hardware or software handshaking interface. Refer to the DesignWare DW_ahb_dmac Databook for further details.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Number of data items, each of width CTLx.DST_TR_WIDTH, to be written to the destination every time a destination burst transaction request is made from either the corresponding hardware or software handshaking interface. Refer to the DesignWare DW_ahb_dmac Databook for further details.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.

Bit Range	Default & Access	Description
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.27.8 Control Register for Channel 0 - High (CTL0_HI)—Offset 1Ch

Refer to the register description for Control Register for Channel 0 - Low.

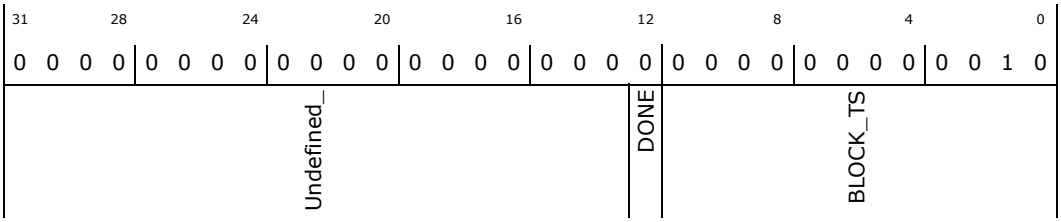
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL0_HI: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** If status write-back is enabled, the upper word of the control register, CTLx[63:32], is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTLx.DONE bit to see when a block transfer is complete. The LLI CTLx.DONE bit should be cleared when the linked lists are set up in memory, prior to enabling the channel. LLI accesses are always 32-bit accesses (Hsize = 2) aligned to 32-bit boundaries and cannot be changed or programmed to anything other than 32-bit. For more information, refer to the DesignWare DW_ahb_dmac Databook.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.27.9 Source Status Register for Channel 0 - Low (SSTAT0_LO)—Offset 20h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Refer to the DesignWare DW_ahb_dmac Databook for further details.

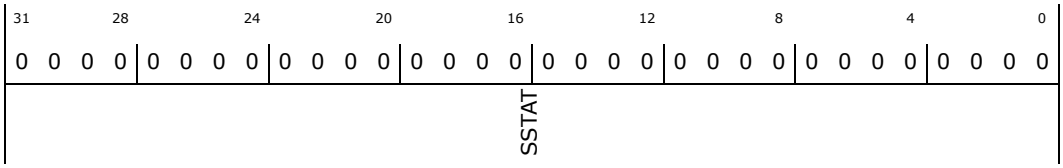
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT0_LO: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.27.10 Source Status Register for Channel 0 - High (SSTAT0_HI)—Offset 24h

Refer to the description for Source Status Register for Channel 0 - Low.

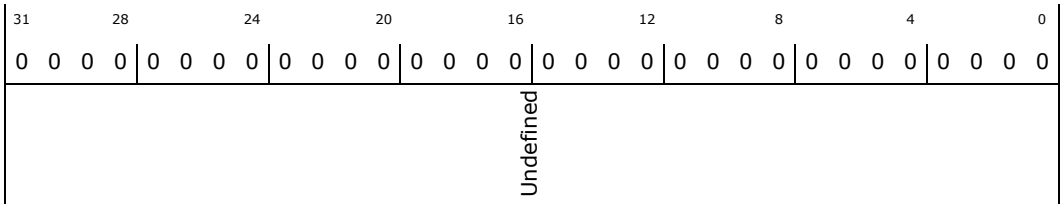
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT0_HI: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.11 Dest Status Register for Channel 0 - Low (DSTAT0_LO)—Offset 28h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI (refer to the DesignWare DW_ahb_dmac Databook for further details) before the start of the next block. For conditions under which the destination status information is fetched, refer to the abovementioned spec.

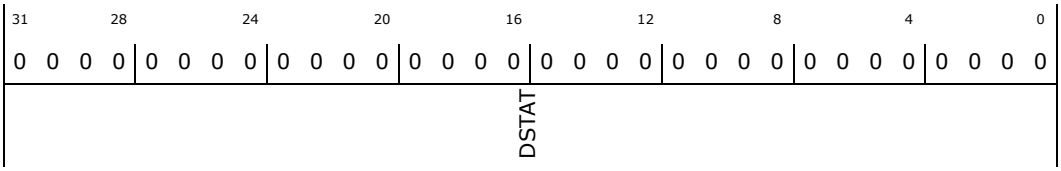
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT0_LO: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

3.27.12 Dest Status Register for Channel 0 - High (DSTAT0_HI)—Offset 2Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

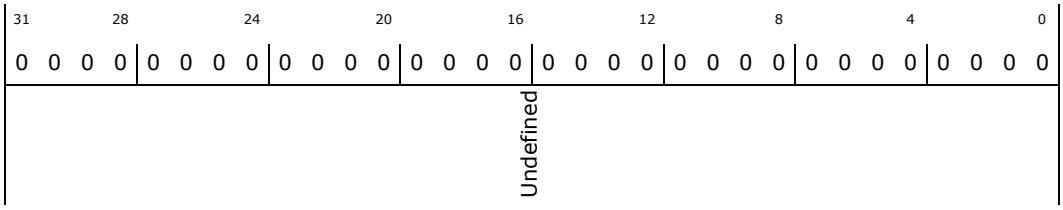
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT0_HI: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.13 Source Status Address Register for Channel 0 - Low (SSTATAR0_LO)—Offset 30h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

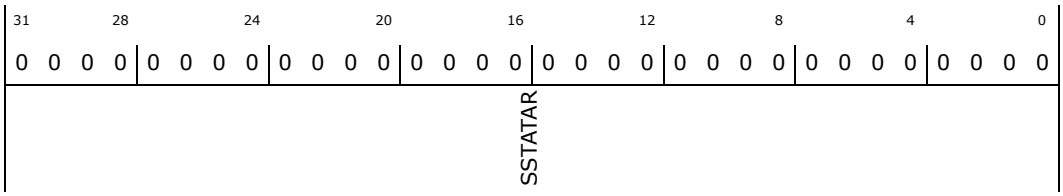
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR0_LO: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.14 Source Status Address Register for Channel 0 - High (SSTATAR0_HI)—Offset 34h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

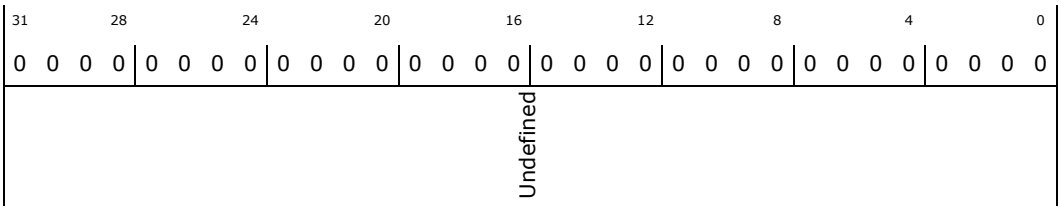
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR0_HI: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.15 Dest Status Address Register for Channel 0 - Low (DSTATAR0_LO)—Offset 38h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. Refer to the DesignWare DW_ahb_dmac Databook for further details.

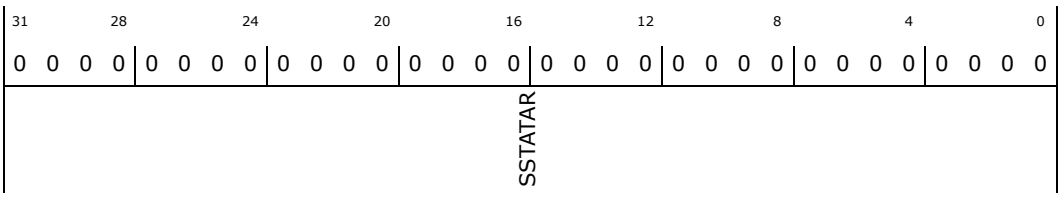
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR0_LO: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.16 Dest Status Address Register for Channel 0 - High (DSTATAR0_HI)—Offset 3Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

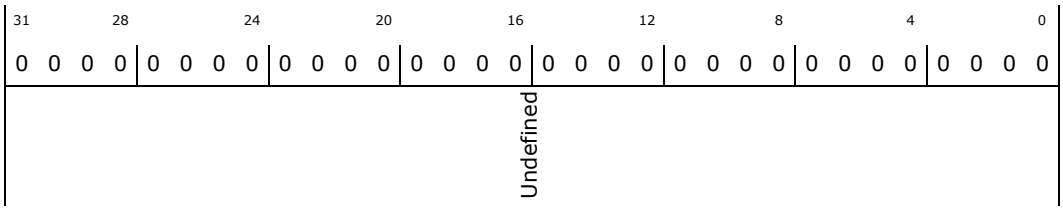
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR0_HI: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.17 Configuration Register for Channel 0 - Low (CFG0_LO)—Offset 40h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.

Note: You need to program this register prior to enabling the channel.

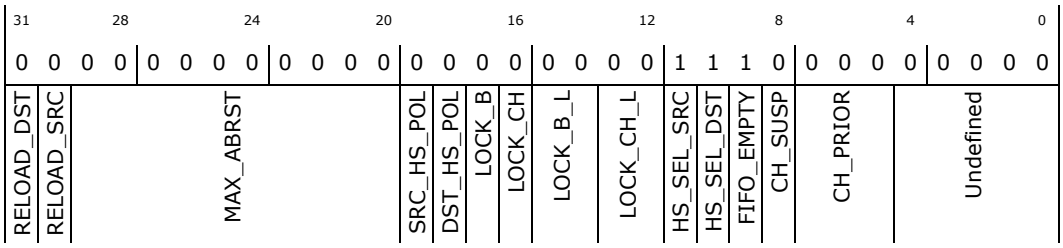
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG0_LO: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E00h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.

Bit Range	Default & Access	Description
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	0h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.27.18 Configuration Register for Channel 0 - High (CFG0_HI)—Offset 44h

Refer to the register description for Configuration Register for Channel 0 - Low.

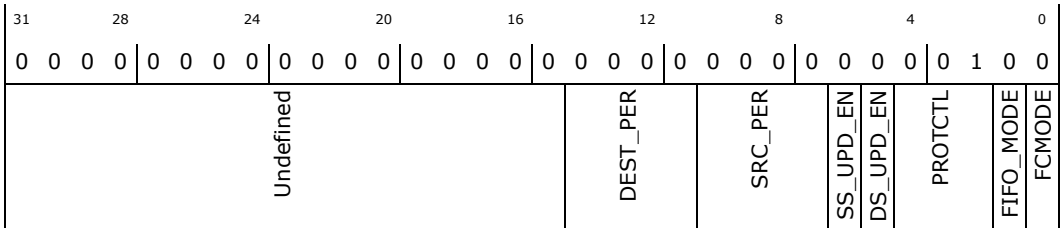
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG0_HI: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.27.19 Source Gather Register for Channel 0 - Low (SGR0_LO)—Offset 48h

The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored. This register does not exist if the configuration parameter DMAH_CHx_SRC_GAT_EN is set to False. For more information, refer to the DesignWare DW_ahb_dmac Databook.

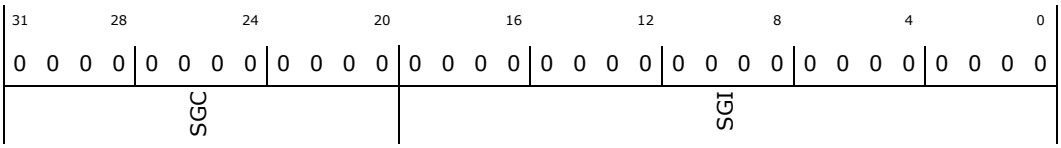
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR0_LO: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Specifies the source address increment/ decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer.

3.27.20 Source Gather Register for Channel 0 - High (SGR0_HI)—Offset 4Ch

Refer to the register description for Source Gather Register for Channel 0 - Low.

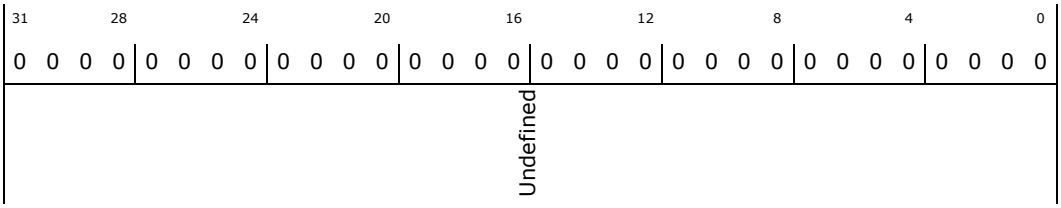
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR0_HI: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.21 Destination Scatter Register for Channel 0 - Low (DSR0_LO)—Offset 50h

The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored. This register does not exist if the configuration parameter DMAH_CHx_DST_SCA_EN is set to False. For more information, refer to the DesignWare DW_ahb_dmac Databook.

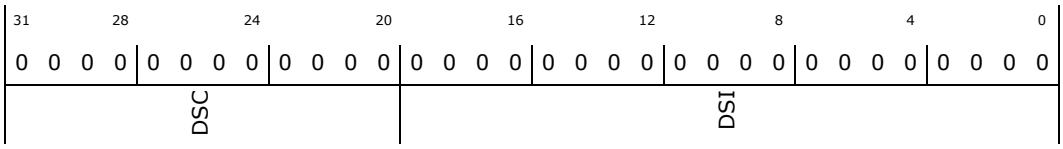
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR0_LO: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Specifies the destination address increment/ decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary, when scatter mode is enabled for the destination transfer.

3.27.22 Dest Scatter Register for Channel 0 - High (DSR0_HI)—Offset 54h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

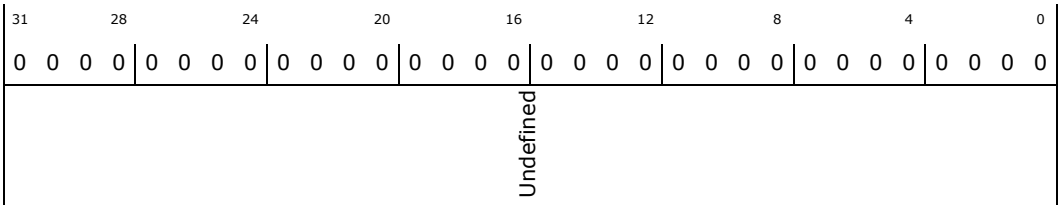
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR0_HI: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.23 Source Address Register for Channel 1 - Low (SAR1_LO)—Offset 58h

Refer to the description for register Source Address Register for Channel 0 - Low.

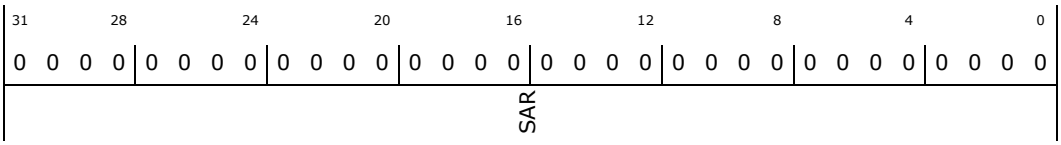
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR1_LO: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.27.24 Source Address Register for Channel 1 - High (SAR1_HI)—Offset 5Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

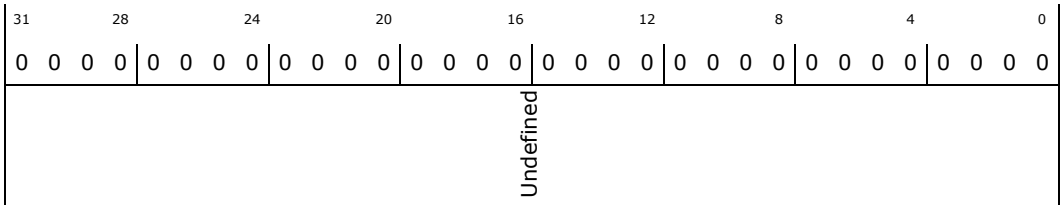
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR1_HI: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.25 Destination Address Register for Channel 1 - Low (DAR1_LO)—Offset 60h

Refer to the description for register Destination Address Register for Channel 0 - Low.

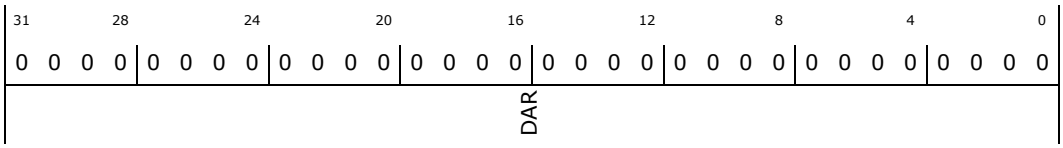
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR1_LO: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.27.26 Destination Address Register for Channel 1 - High (DAR1_HI)—Offset 64h

Refer to the description for register Destination Address Register for Channel 0 - Low.

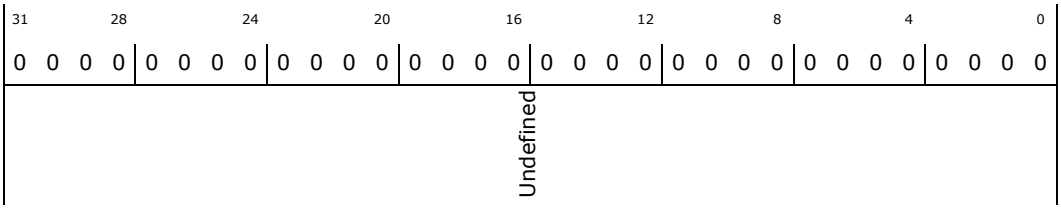
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR1_HI: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.27 Linked List Pointer Register for Channel 1 - Low (LLP1_LO)—Offset 68h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

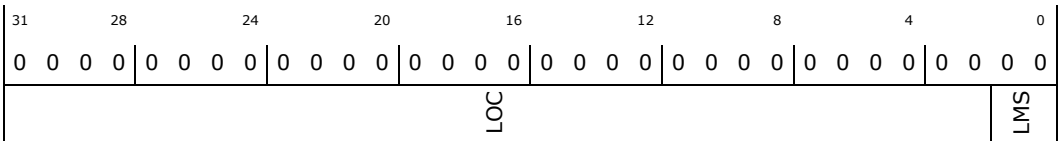
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP1_LO: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.27.28 Linked List Pointer Register for Channel 1 - High (LLP1_HI)—Offset 6Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

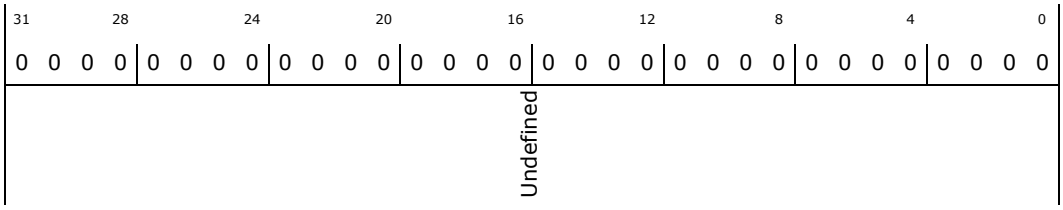
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP1_HI: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.29 Control Register for Channel 1 - Low (CTL1_LO)—Offset 70h

Refer to the register description for Control Register for Channel 0 - Low.

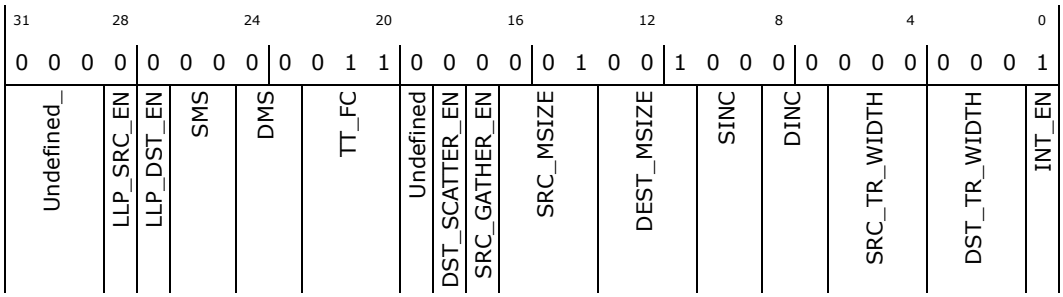
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL1_LO: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.

Bit Range	Default & Access	Description
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.27.30 Control Register for Channel 1 - High (CTL1_HI)—Offset 74h

Refer to the register description for Control Register for Channel 0 - Low.

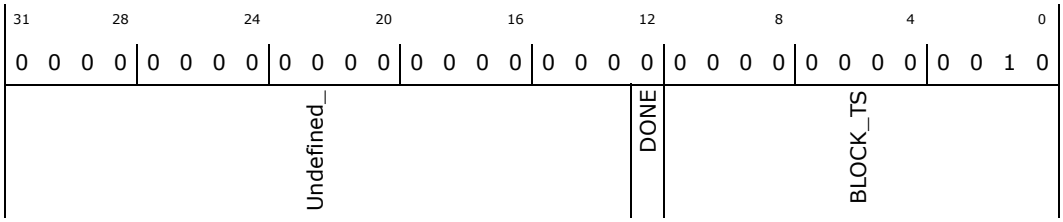
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL1_HI: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled, to indicate the block size.

3.27.31 Source Status Register for Channel 1 - Low (SSTAT1_LO)—Offset 78h

Refer to the register description for Source Status Register for Channel 0 - Low.

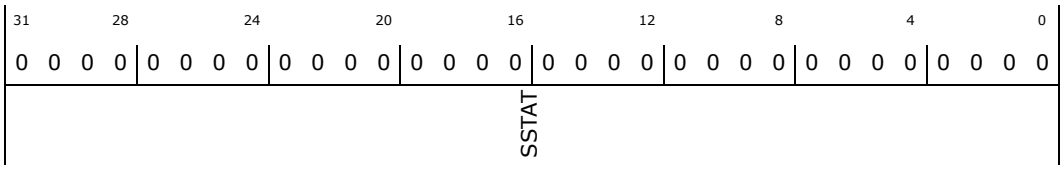
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT1_LO: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.27.32 Source Status Register for Channel 1 - High (SSTAT1_HI)—Offset 7Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

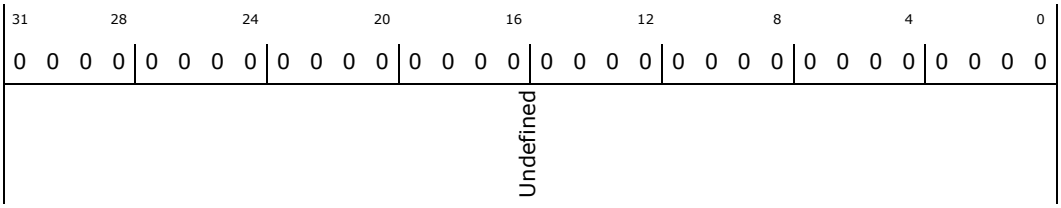
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT1_HI: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.33 Dest Status Register for Channel 1 - Low (DSTAT1_LO)—Offset 80h

Refer to the register description for Dest Status Register for Channel 0 - Low.

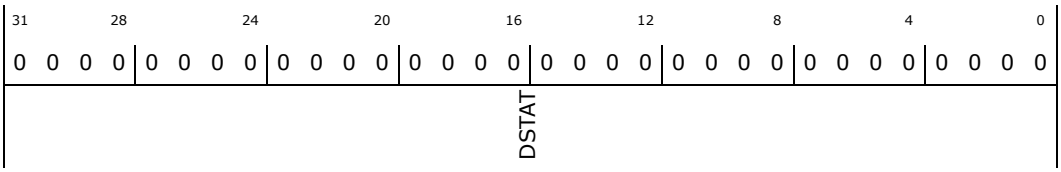
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT1_LO: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest. status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

3.27.34 Dest Status Register for Channel 1 - High (DSTAT1_HI)—Offset 84h

Refer to the register description for Dest Status Register for Channel 0 - Low.

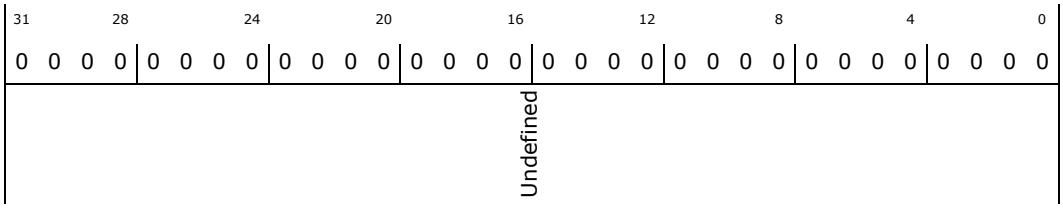
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT1_HI: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.35 Source Status Address Register for Channel 1 - Low (SSTATAR1_LO)—Offset 88h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

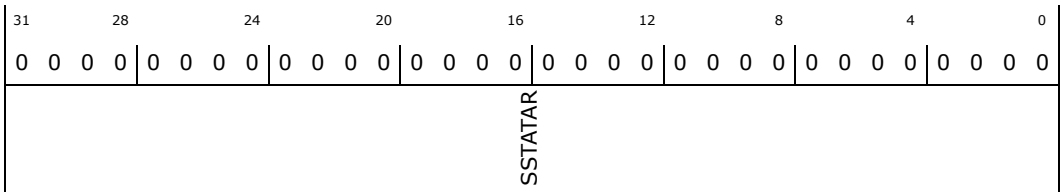
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR1_LO: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.36 Source Status Address Register for Channel 1 - High (SSTATAR1_HI)—Offset 8Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

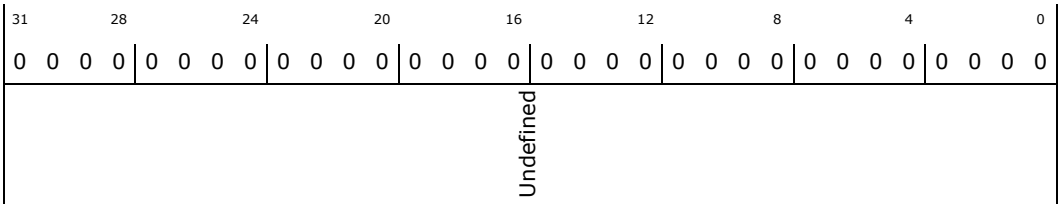
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR1_HI: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.37 Dest Status Address Register for Channel 1 - Low (DSTATAR1_LO)—Offset 90h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

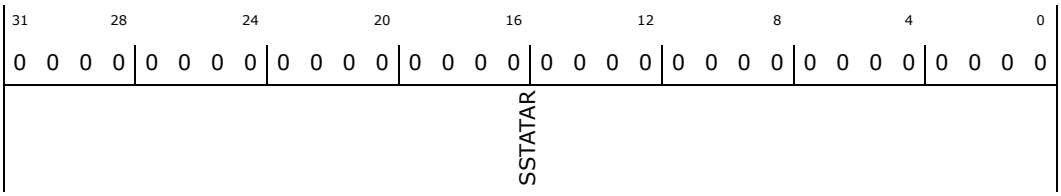
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR1_LO: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.38 Dest Status Address Register for Channel 1 - High (DSTATAR1_HI)—Offset 94h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

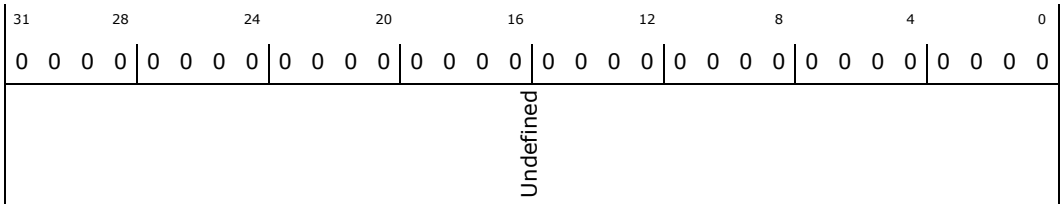
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR1_HI: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.39 Configuration Register for Channel 1 - Low (CFG1_LO)—Offset 98h

Refer to the register description for Configuration Register for Channel 0 - Low.

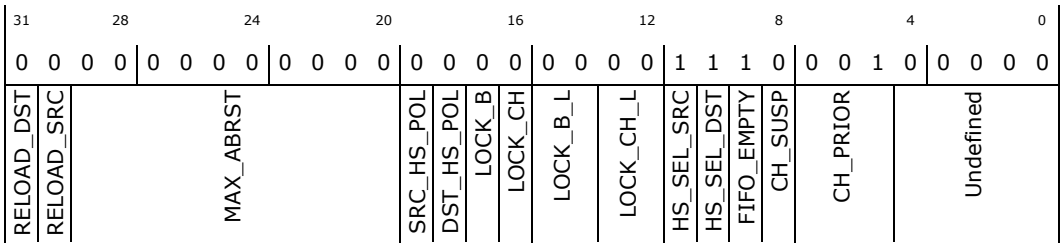
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG1_LO: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E20h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.

Bit Range	Default & Access	Description
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	1h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.27.40 Configuration Register for Channel 1 - High (CFG1_HI)—Offset 9Ch

Refer to the register description for Configuration Register for Channel 0 - Low.

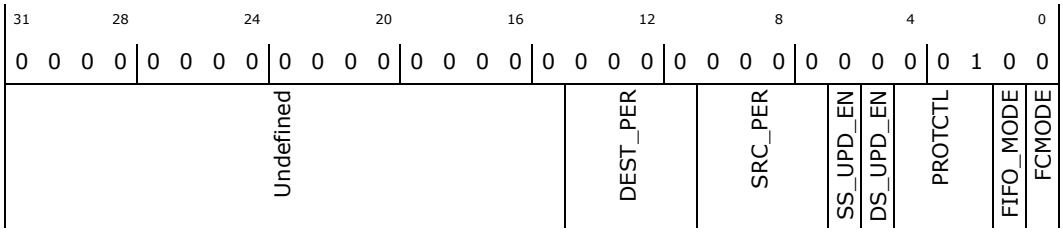
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG1_HI: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.27.41 Source Gather Register for Channel 1 - Low (SGR1_LO)—Offset A0h

Refer to the register description for Source Gather Register for Channel 0 - Low.

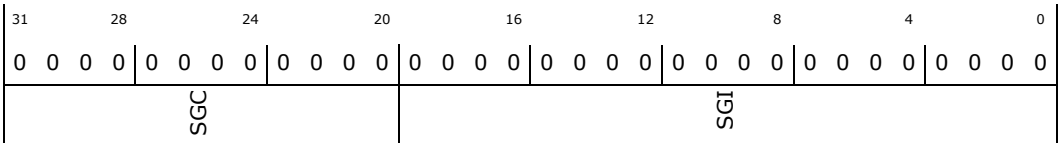
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR1_LO: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.27.42 Source Gather Register for Channel 1 - High (SGR1_HI)—Offset A4h

Refer to the register description for Source Gather Register for Channel 0 - Low.

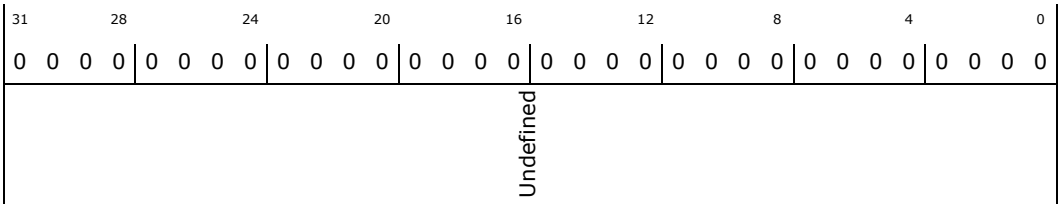
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR1_HI: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.43 Destination Scatter Register for Channel 1 - Low (DSR1_LO)—Offset A8h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

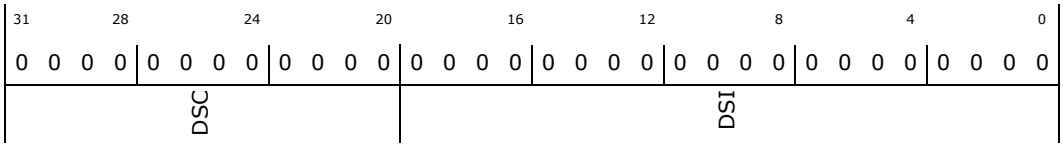
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR1_LO: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.27.44 Dest Scatter Register for Channel 1 - High (DSR1_HI)—Offset ACh

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

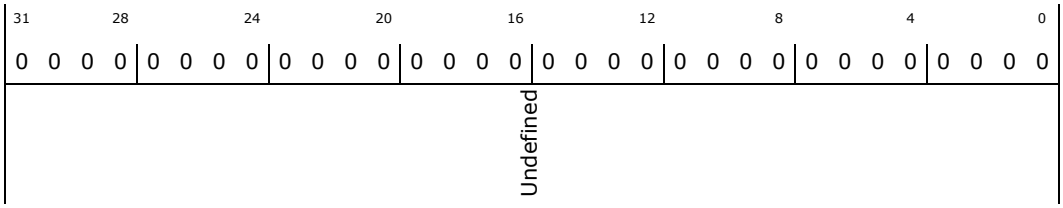
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR1_HI: [BAR] + ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.45 Source Address Register for Channel 2 - Low (SAR2_LO)—Offset B0h

Refer to the description for register Source Address Register for Channel 0 - Low.

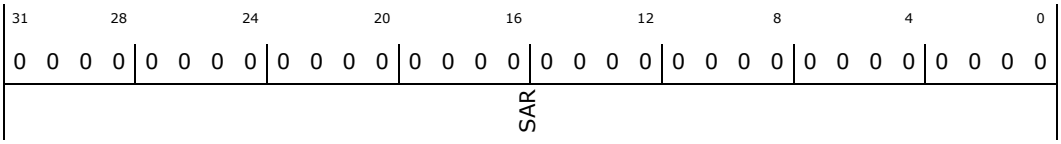
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR2_LO: [BAR] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.27.46 Source Address Register for Channel 2 - High (SAR2_HI)—Offset B4h

Refer to the description for register Source Address Register for Channel 0 - Low.

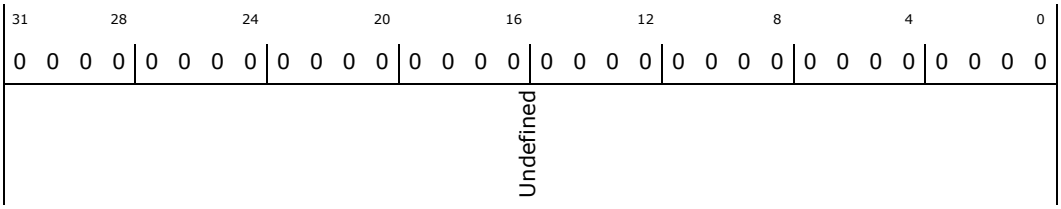
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR2_HI: [BAR] + B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.47 Destination Address Register for Channel 2 - Low (DAR2_LO)—Offset B8h

Refer to the description for register Destination Address Register for Channel 0 - Low.

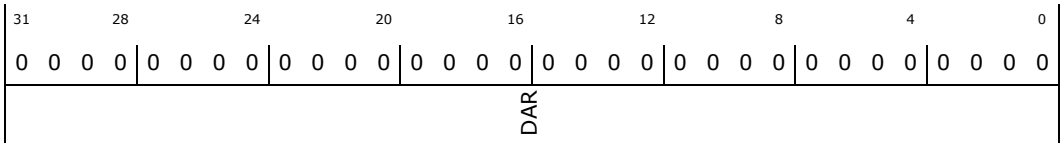
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR2_LO: [BAR] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.27.48 Destination Address Register for Channel 2 - High (DAR2_HI)—Offset BCh

Refer to the description for register Destination Address Register for Channel 0 - Low.

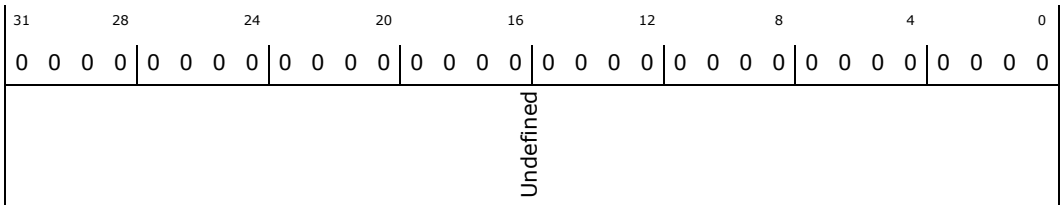
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR2_HI: [BAR] + BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.49 Linked List Pointer Register for Channel 2 - Low (LLP2_LO)—Offset C0h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

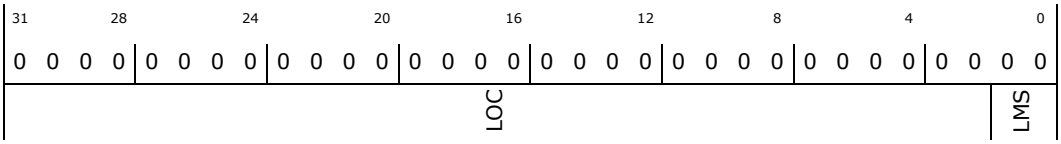
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP2_LO: [BAR] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.27.50 Linked List Pointer Register for Channel 2 - High (LLP2_HI)—Offset C4h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

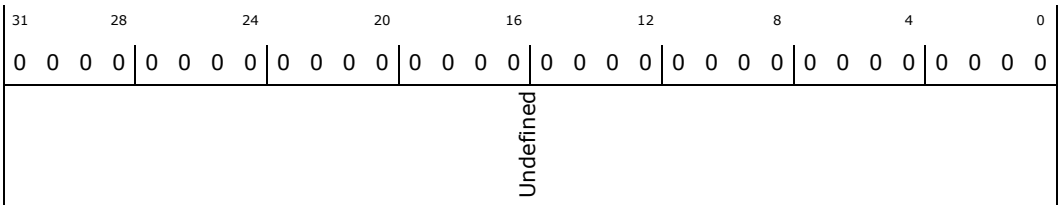
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP2_HI: [BAR] + C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.51 Control Register for Channel 2 - Low (CTL2_LO)—Offset C8h

Refer to the register description for Control Register for Channel 0 - Low.

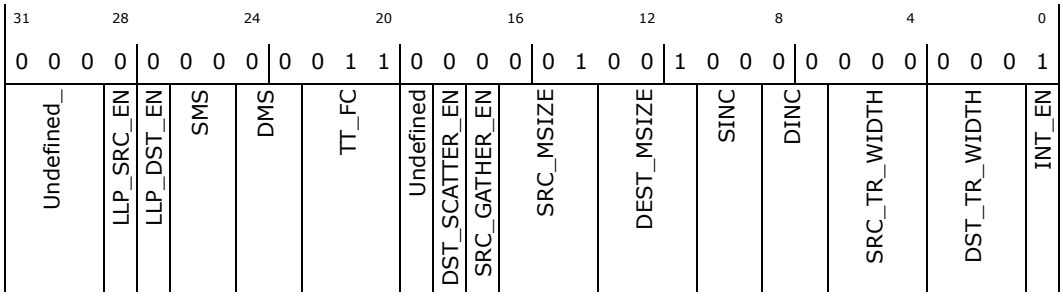
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL2_LO: [BAR] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.

Bit Range	Default & Access	Description
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.27.52 Control Register for Channel 2 - High (CTL2_HI)—Offset CCh

Refer to the register description for Control Register for Channel 0 - Low.

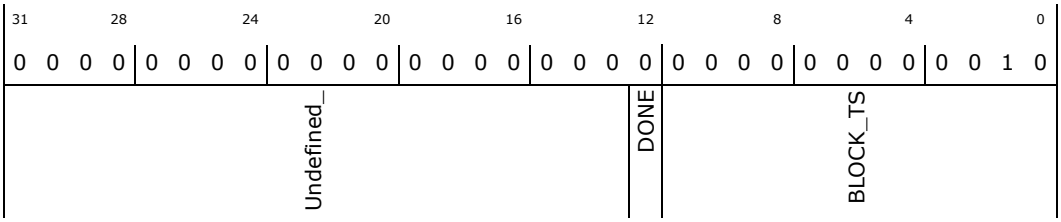
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL2_HI: [BAR] + CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.27.53 Source Status Register for Channel 2 - Low (SSTAT2_LO)—Offset D0h

Refer to the register description for Source Status Register for Channel 0 - Low.

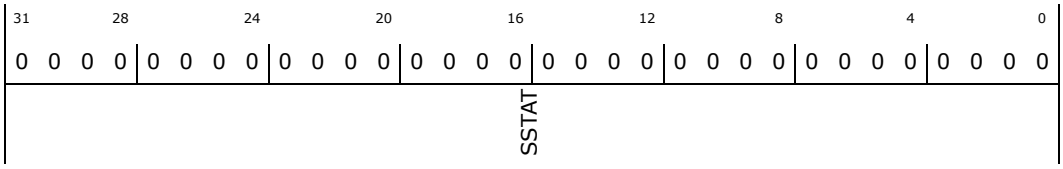
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT2_LO: [BAR] + D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register.

3.27.54 Source Status Register for Channel 2 - High (SSTAT2_HI)—Offset D4h

Refer to the register description for Source Status Register for Channel 0 - Low.

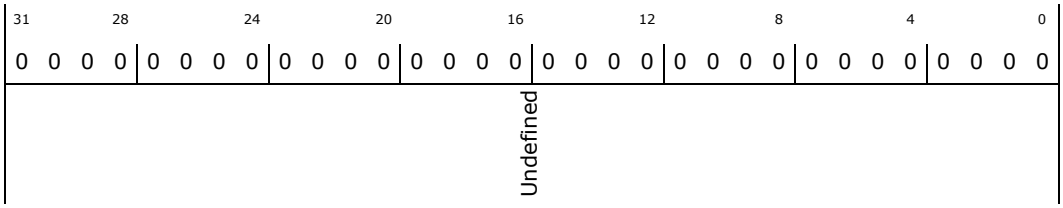
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT2_HI: [BAR] + D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.55 Dest Status Register for Channel 2 - Low (DSTAT2_LO)—Offset D8h

Refer to the register description for Dest Status Register for Channel 0 - Low.

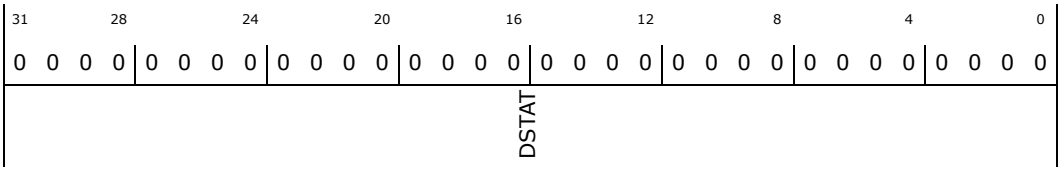
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT2_LO: [BAR] + D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

3.27.56 Dest Status Register for Channel 2 - High (DSTAT2_HI)—Offset DCh

Refer to the register description for Dest Status Register for Channel 0 - Low.

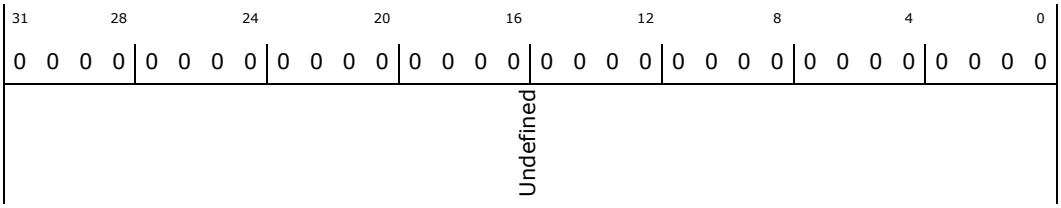
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT2_HI: [BAR] + DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.57 Source Status Address Register for Channel 2 - Low (SSTATAR2_LO)—Offset E0h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

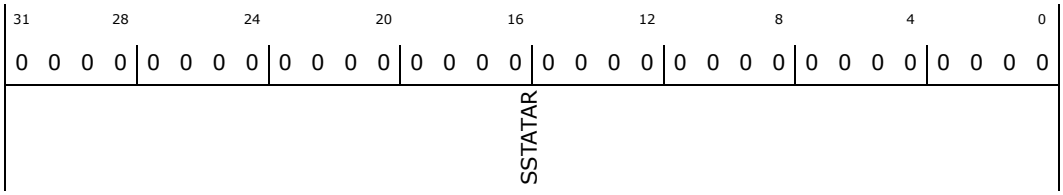
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR2_LO: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.58 Source Status Address Register for Channel 2 - High (SSTATAR2_HI)—Offset E4h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

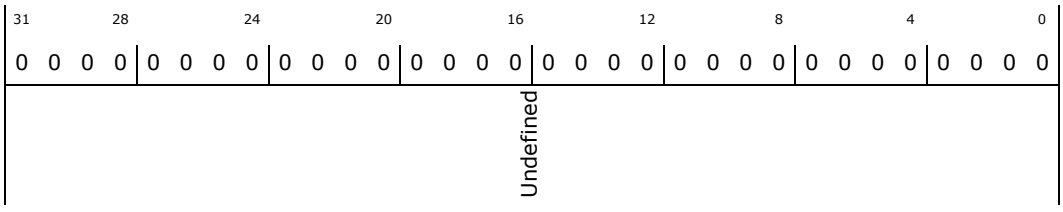
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR2_HI: [BAR] + E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.59 Dest Status Address Register for Channel 2 - Low (DSTATAR2_LO)—Offset E8h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

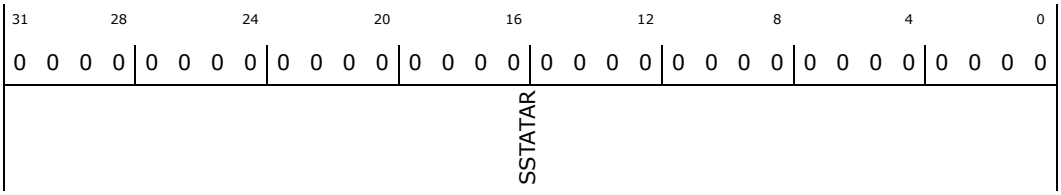
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR2_LO: [BAR] + E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.60 Dest Status Address Register for Channel 2 - High (DSTATAR2_HI)—Offset ECh

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

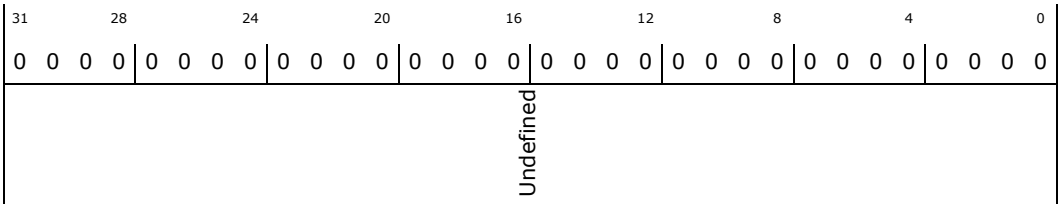
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR2_HI: [BAR] + ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.61 Configuration Register for Channel 2 - Low (CFG2_LO)—Offset F0h

Refer to the register description for Configuration Register for Channel 0 - Low.

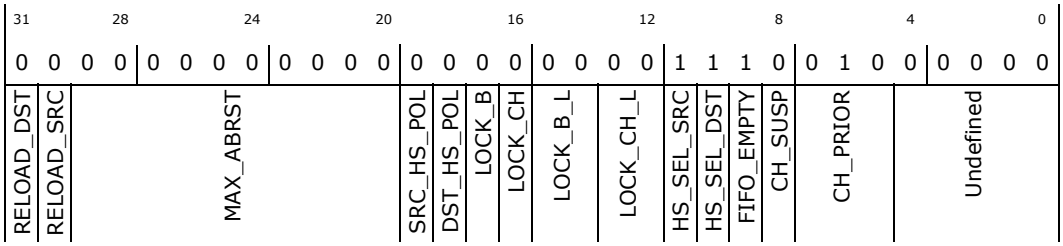
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG2_LO: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E40h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.

Bit Range	Default & Access	Description
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	2h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.27.62 Configuration Register for Channel 2 - High (CFG2_HI)—Offset F4h

Refer to the register description for Configuration Register for Channel 0 - Low.

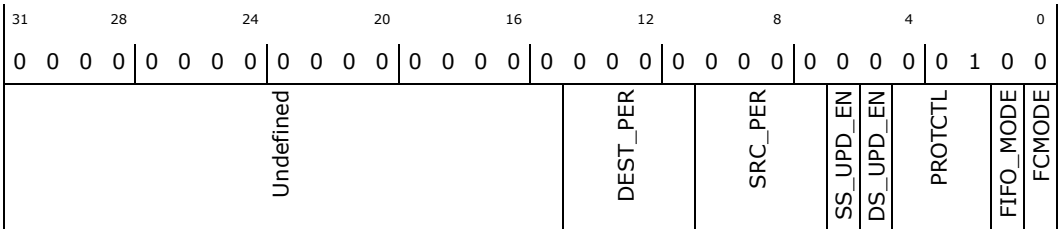
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG2_HI: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.27.63 Source Gather Register for Channel 2 - Low (SGR2_LO)—Offset F8h

Refer to the register description for Source Gather Register for Channel 0 - Low.

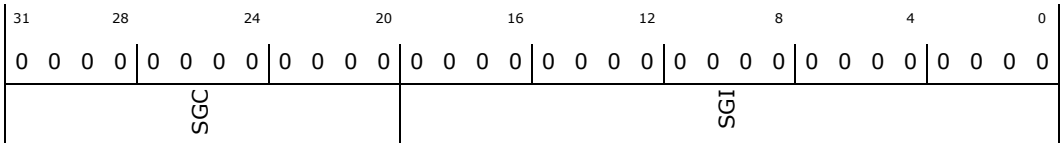
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR2_LO: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.27.64 Source Gather Register for Channel 2 - High (SGR2_HI)—Offset FCh

Refer to the register description for Source Gather Register for Channel 0 - Low.

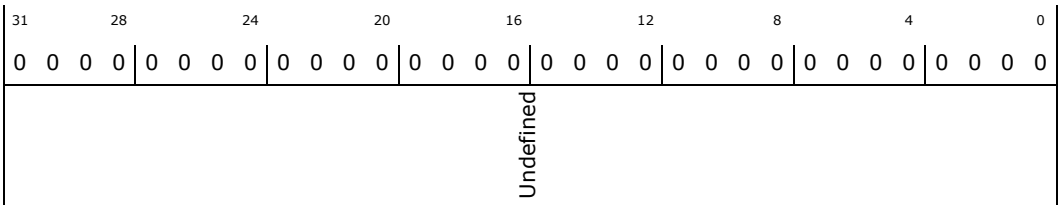
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR2_HI: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.65 Destination Scatter Register for Channel 2 - Low (DSR2_LO)—Offset 100h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

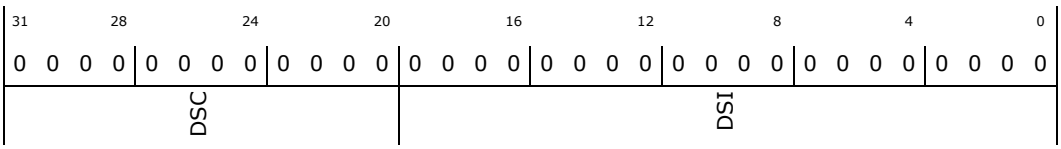
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR2_LO: [BAR] + 100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.27.66 Dest Scatter Register for Channel 2 - High (DSR2_HI)—Offset 104h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

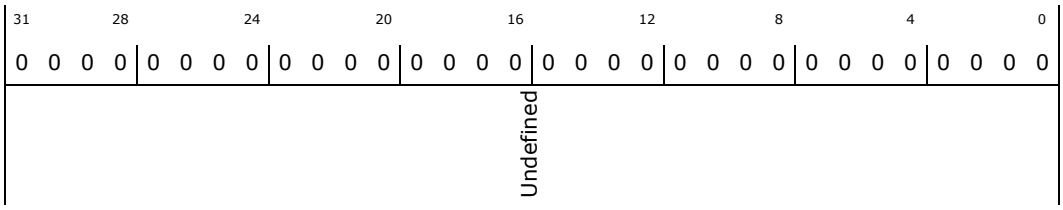
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR2_HI: [BAR] + 104h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.67 Source Address Register for Channel 3 - Low (SAR3_LO)—Offset 108h

Refer to the description for register Source Address Register for Channel 0 - Low.

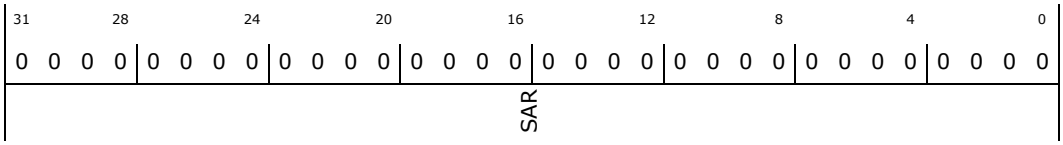
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR3_LO: [BAR] + 108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.27.68 Source Address Register for Channel 3 - High (SAR3_HI)—Offset 10Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

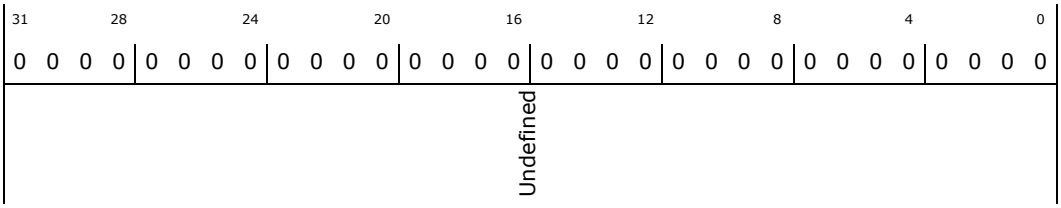
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR3_HI: [BAR] + 10Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.69 Destination Address Register for Channel 3 - Low (DAR3_LO)—Offset 110h

Refer to the description for register Destination Address Register for Channel 0 - Low.

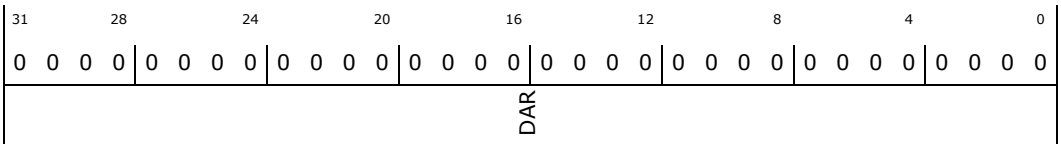
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR3_LO: [BAR] + 110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.27.70 Destination Address Register for Channel 3 - High (DAR3_HI)—Offset 114h

Refer to the description for register Destination Address Register for Channel 0 - Low.

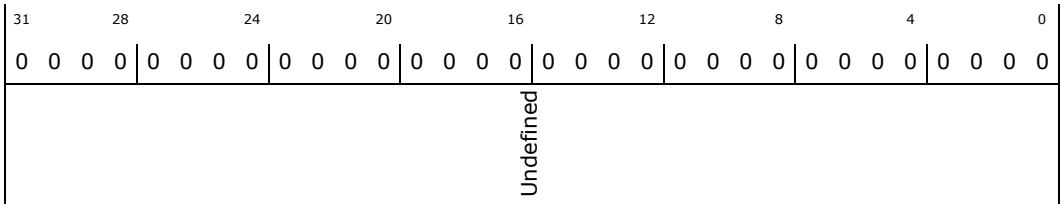
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR3_HI: [BAR] + 114h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.71 Linked List Pointer Register for Channel 3 - Low (LLP3_LO)—Offset 118h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

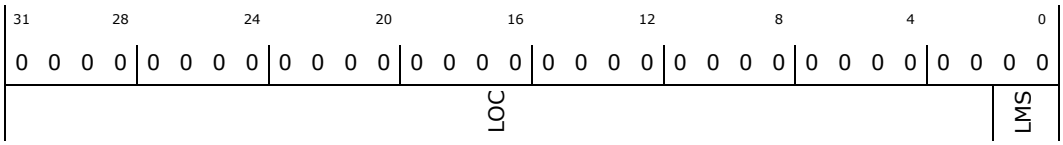
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP3_LO: [BAR] + 118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.27.72 Linked List Pointer Register for Channel 3 - High (LLP3_HI)—Offset 11Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

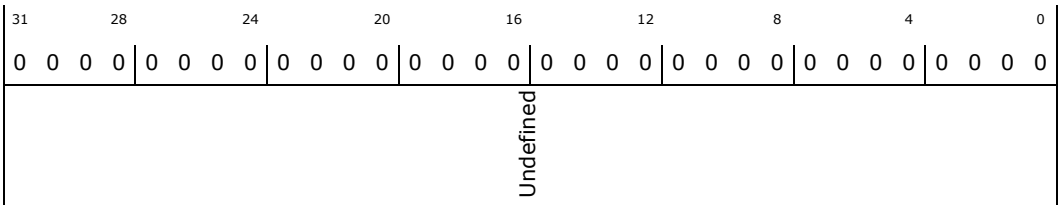
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP3_HI: [BAR] + 11Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.73 Control Register for Channel 3 - Low (CTL3_LO)—Offset 120h

Refer to the register description for Control Register for Channel 0 - Low.

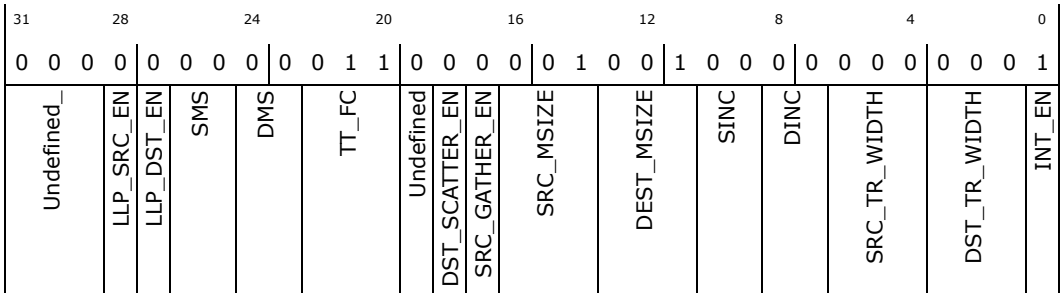
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL3_LO: [BAR] + 120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.

Bit Range	Default & Access	Description
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.27.74 Control Register for Channel 3 - High (CTL3_HI)—Offset 124h

Refer to the register description for Control Register for Channel 0 - Low.

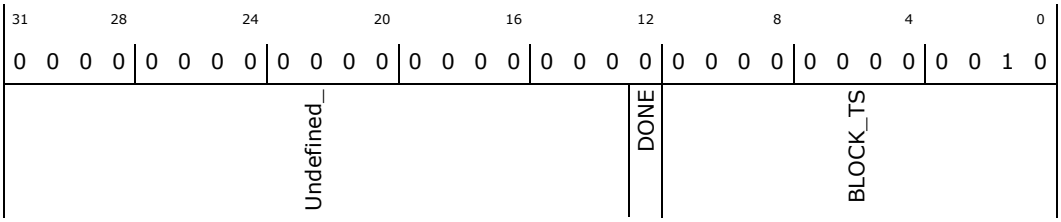
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL3_HI: [BAR] + 124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.27.75 Source Status Register for Channel 3 - Low (SSTAT3_LO)—Offset 128h

Refer to the register description for Source Status Register for Channel 0 - Low.

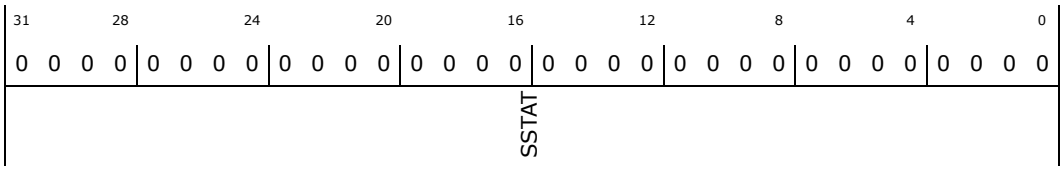
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT3_LO: [BAR] + 128h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.27.76 Source Status Register for Channel 3 - High (SSTAT3_HI)—Offset 12Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

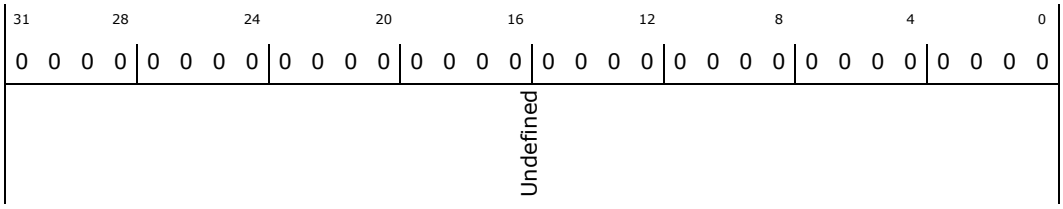
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT3_HI: [BAR] + 12Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.77 Dest Status Register for Channel 3 - Low (DSTAT3_LO)—Offset 130h

Refer to the register description for Dest Status Register for Channel 0 - Low.

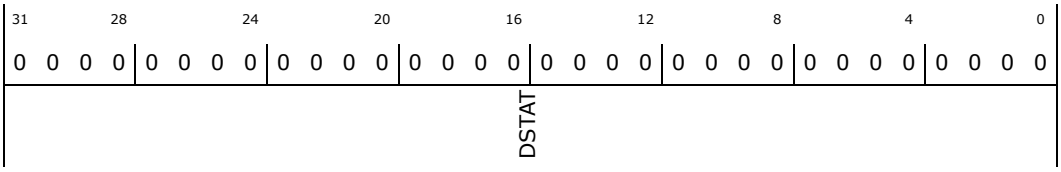
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT3_LO: [BAR] + 130h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

3.27.78 Dest Status Register for Channel 3 - High (DSTAT3_HI)—Offset 134h

Refer to the register description for Dest Status Register for Channel 0 - Low.

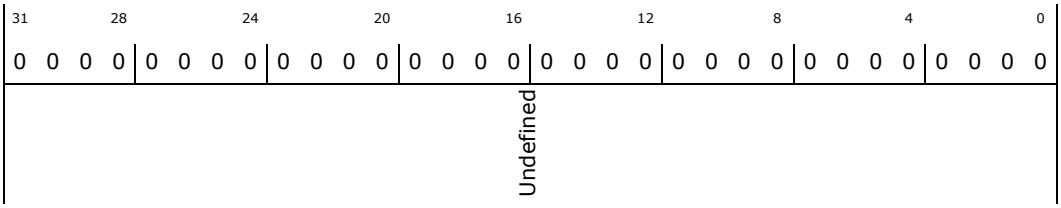
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT3_HI: [BAR] + 134h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.79 Source Status Address Register for Channel 3 - Low (SSTATAR3_LO)—Offset 138h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

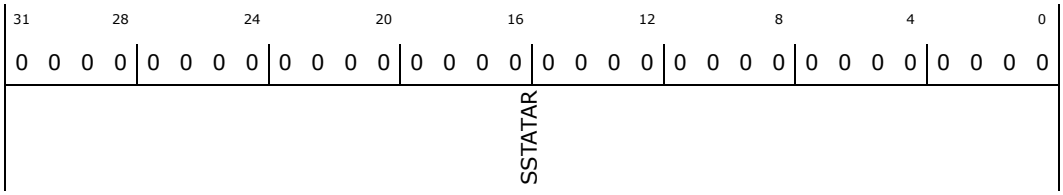
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR3_LO: [BAR] + 138h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.80 Source Status Address Register for Channel 3 - High (SSTATAR3_HI)—Offset 13Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

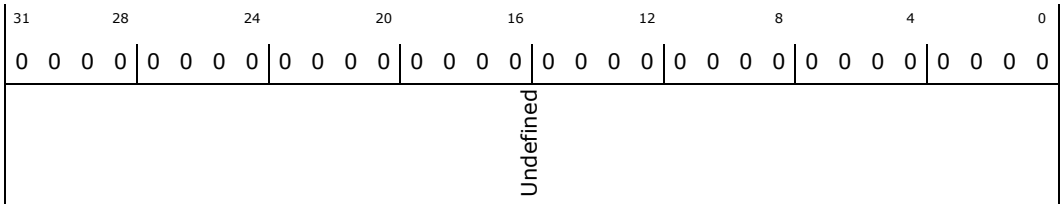
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR3_HI: [BAR] + 13Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.81 Dest Status Address Register for Channel 3 - Low (DSTATAR3_LO)—Offset 140h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

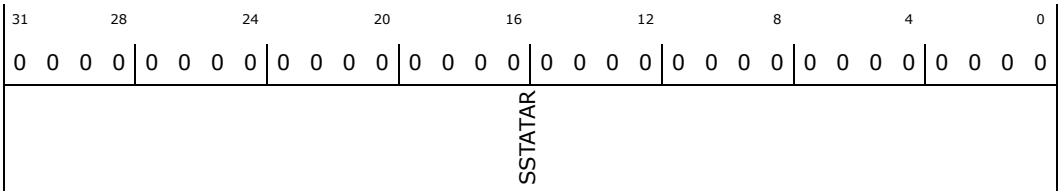
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR3_LO: [BAR] + 140h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.82 Dest Status Address Register for Channel 3 - High (DSTATAR3_HI)—Offset 144h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

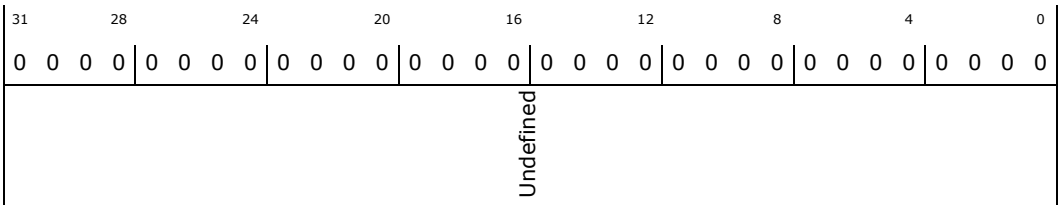
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR3_HI: [BAR] + 144h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.83 Configuration Register for Channel 3 - Low (CFG3_LO)—Offset 148h

Refer to the register description for Configuration Register for Channel 0 - Low.

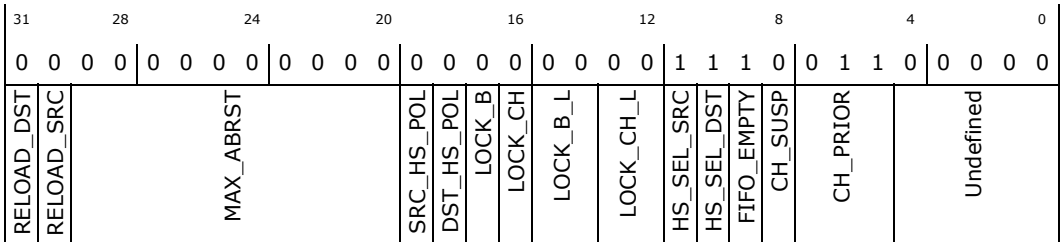
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG3_LO: [BAR] + 148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E60h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking

Bit Range	Default & Access	Description
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	3h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.27.84 Configuration Register for Channel 3 - High (CFG3_HI)—Offset 14Ch

Refer to the register description for Configuration Register for Channel 0 - Low.

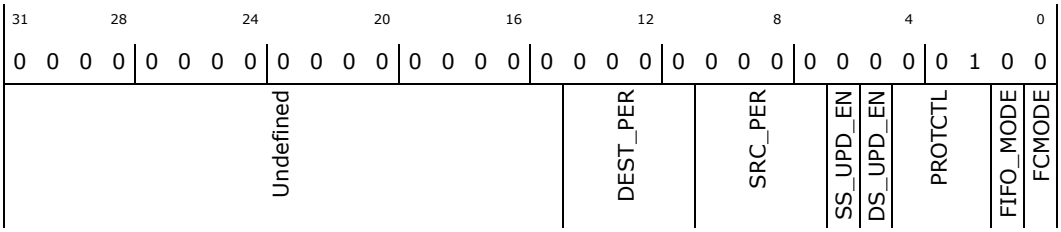
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG3_HI: [BAR] + 14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.

Bit Range	Default & Access	Description
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced, when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.27.85 Source Gather Register for Channel 3 - Low (SGR3_LO)—Offset 150h

Refer to the register description for Source Gather Register for Channel 0 - Low.

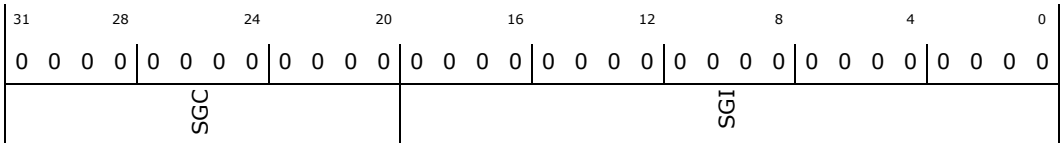
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR3_LO: [BAR] + 150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.27.86 Source Gather Register for Channel 3 - High (SGR3_HI)—Offset 154h

Refer to the register description for Source Gather Register for Channel 0 - Low.

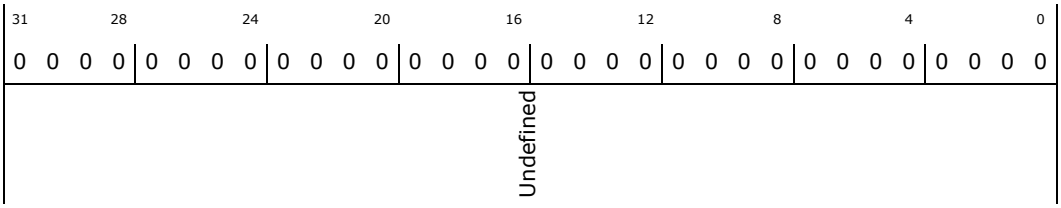
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR3_HI: [BAR] + 154h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.87 Destination Scatter Register for Channel 3 - Low (DSR3_LO)—Offset 158h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

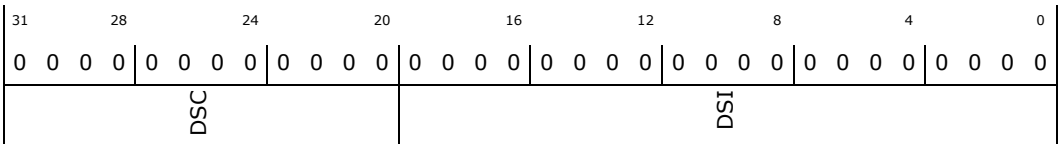
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR3_LO: [BAR] + 158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.27.88 Dest Scatter Register for Channel 3 - High (DSR3_HI)—Offset 15Ch

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

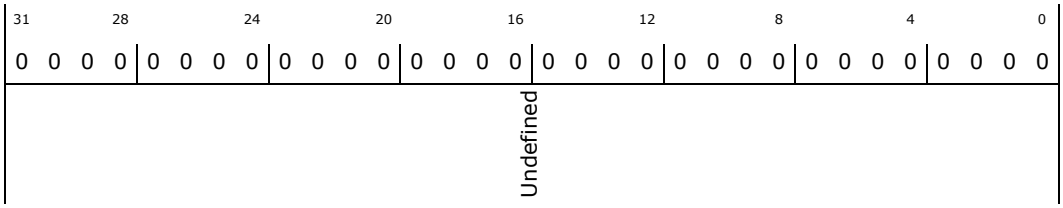
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR3_HI: [BAR] + 15Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.89 Source Address Register for Channel 4 - Low (SAR4_LO)—Offset 160h

Refer to the description for register Source Address Register for Channel 0 - Low.

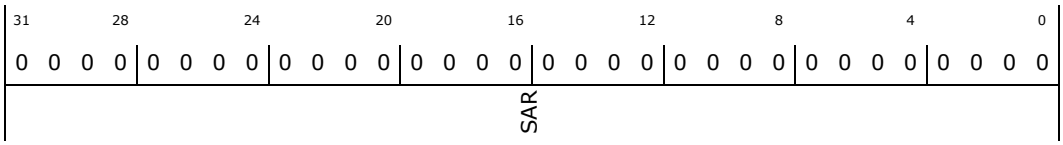
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR4_LO: [BAR] + 160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.27.90 Source Address Register for Channel 4 - High (SAR4_HI)—Offset 164h

Refer to the description for register Source Address Register for Channel 0 - Low.

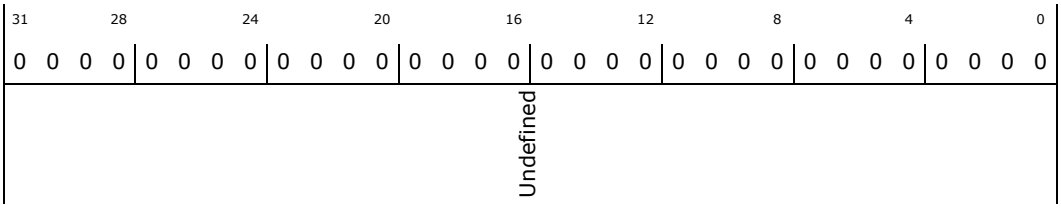
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR4_HI: [BAR] + 164h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.91 Destination Address Register for Channel 4 - Low (DAR4_LO)—Offset 168h

Refer to the description for register Destination Address Register for Channel 0 - Low.

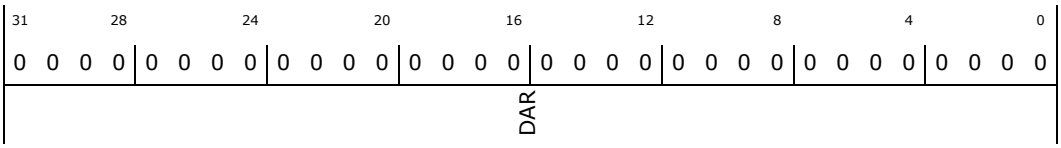
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR4_LO: [BAR] + 168h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.27.92 Destination Address Register for Channel 4 - High (DAR4_HI)—Offset 16Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

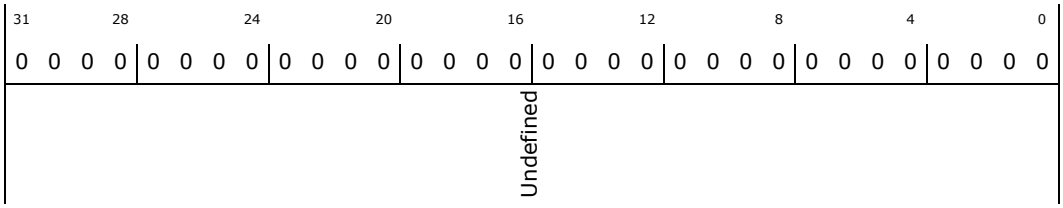
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR4_HI: [BAR] + 16Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.93 Linked List Pointer Register for Channel 4 - Low (LLP4_LO)—Offset 170h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

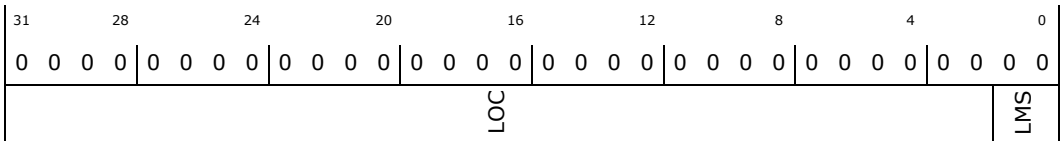
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP4_LO: [BAR] + 170h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.27.94 Linked List Pointer Register for Channel 4 - High (LLP4_HI)—Offset 174h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

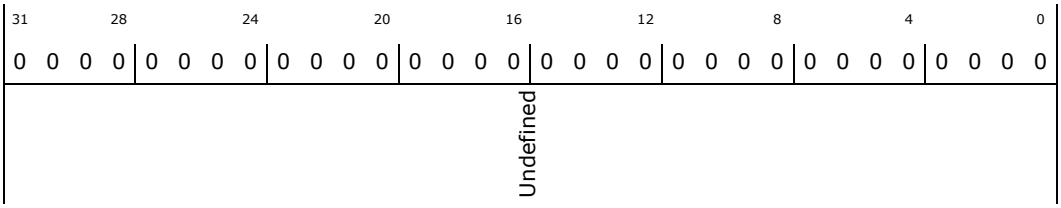
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP4_HI: [BAR] + 174h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.95 Control Register for Channel 4 - Low (CTL4_LO)—Offset 178h

Refer to the register description for Control Register for Channel 0 - Low.

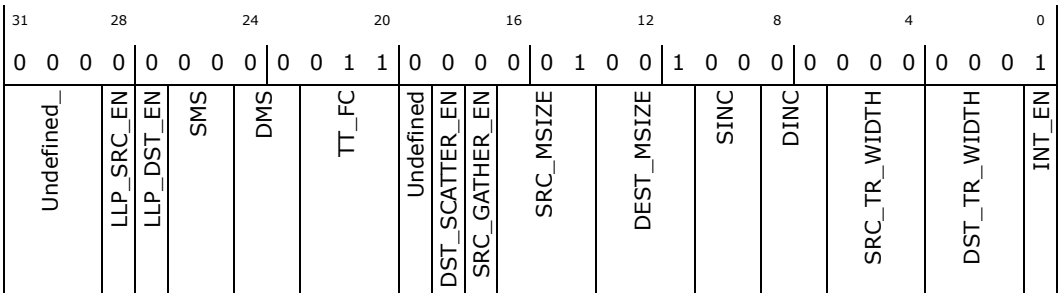
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL4_LO: [BAR] + 178h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.

Bit Range	Default & Access	Description
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.27.96 Control Register for Channel 4 - High (CTL4_HI)—Offset 17Ch

Refer to the register description for Control Register for Channel 0 - Low.

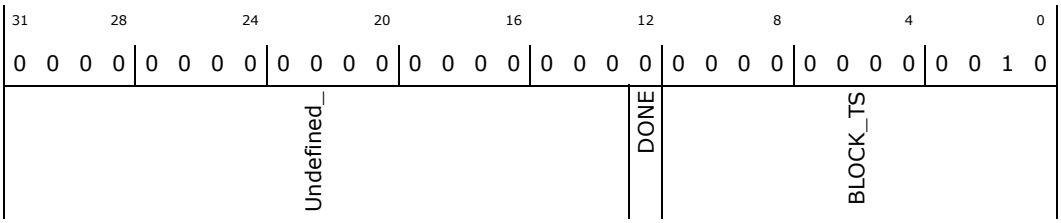
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL4_HI: [BAR] + 17Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.27.97 Source Status Register for Channel 4 - Low (SSTAT4_LO)—Offset 180h

Refer to the register description for Source Status Register for Channel 0 - Low.

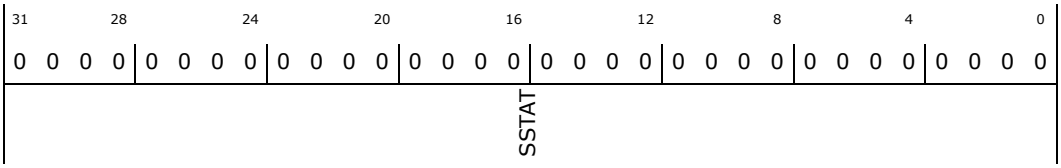
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT4_LO: [BAR] + 180h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register.

3.27.98 Source Status Register for Channel 4 - High (SSTAT4_HI)—Offset 184h

Refer to the register description for Source Status Register for Channel 0 - Low.

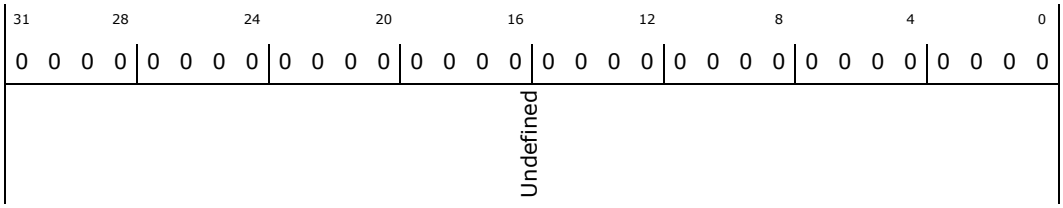
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT4_HI: [BAR] + 184h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.99 Dest Status Register for Channel 4 - Low (DSTAT4_LO)—Offset 188h

Refer to the register description for Dest Status Register for Channel 0 - Low.

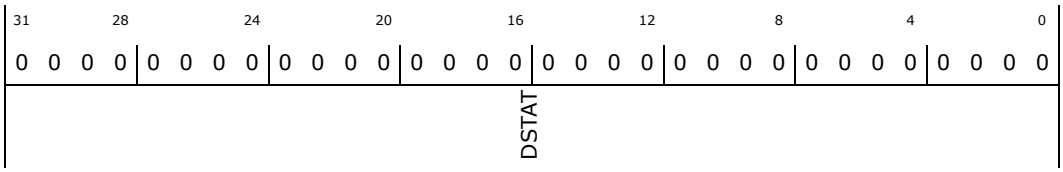
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT4_LO: [BAR] + 188h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

3.27.100 Dest Status Register for Channel 4 - High (DSTAT4_HI)—Offset 18Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

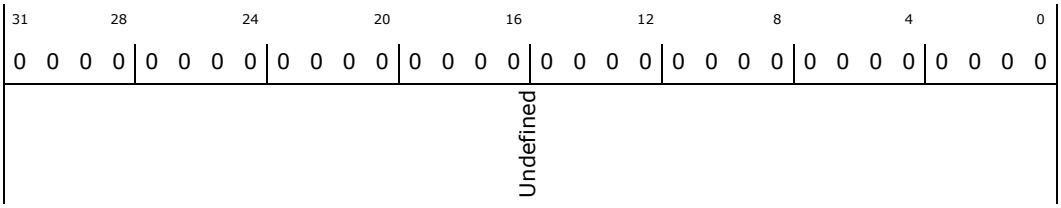
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT4_HI: [BAR] + 18Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.101 Source Status Address Register for Channel 4 - Low (SSTATAR4_LO)—Offset 190h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

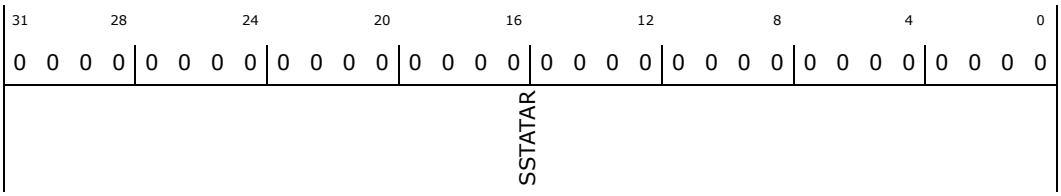
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR4_LO: [BAR] + 190h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.102 Source Status Address Register for Channel 4 - High (SSTATAR4_HI)—Offset 194h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

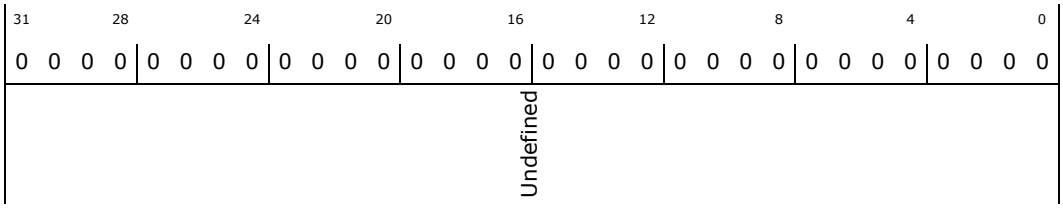
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR4_HI: [BAR] + 194h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.103 Dest Status Address Register for Channel 4 - Low (DSTATAR4_LO)—Offset 198h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

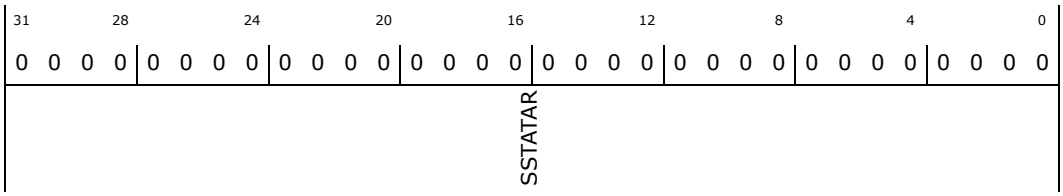
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR4_LO: [BAR] + 198h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.104 Dest Status Address Register for Channel 4 - High (DSTATAR4_HI)—Offset 19Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

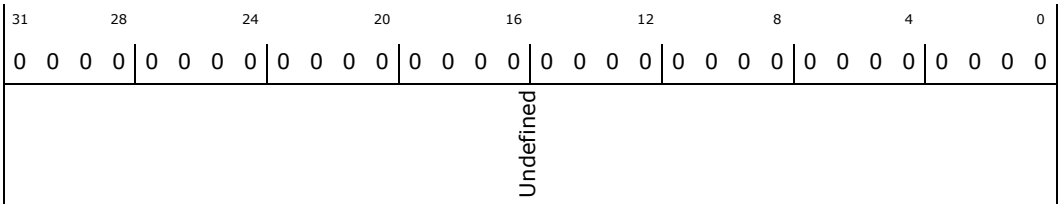
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR4_HI: [BAR] + 19Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.105 Configuration Register for Channel 4 - Low (CFG4_LO)—Offset 1A0h

Refer to the register description for Configuration Register for Channel 0 - Low.

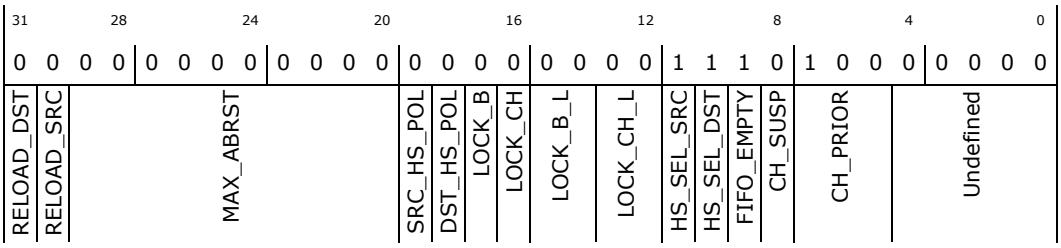
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG4_LO: [BAR] + 1A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E80h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.

Bit Range	Default & Access	Description
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	4h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.27.106 Configuration Register for Channel 4 - High (CFG4_HI)—Offset 1A4h

Refer to the register description for Configuration Register for Channel 0 - Low.

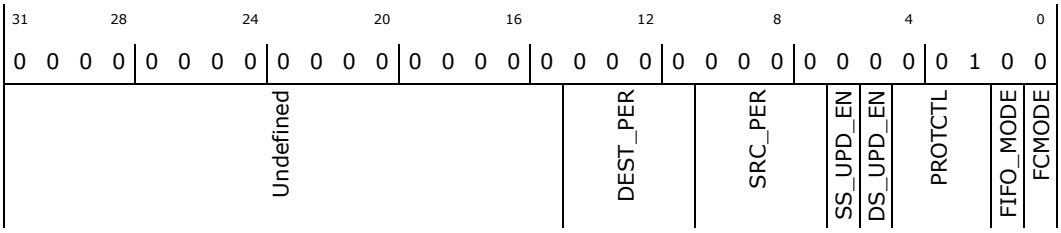
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG4_HI: [BAR] + 1A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.27.107 Source Gather Register for Channel 4 - Low (SGR4_LO)—Offset 1A8h

Refer to the register description for Source Gather Register for Channel 0 - Low.

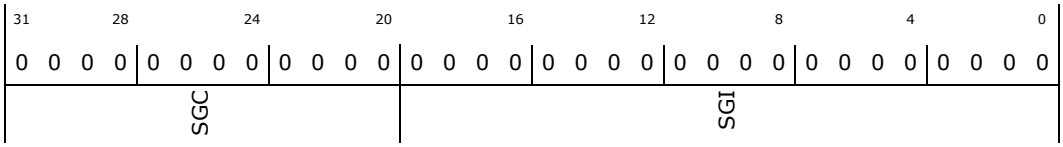
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR4_LO: [BAR] + 1A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.27.108 Source Gather Register for Channel 4 - High (SGR4_HI)—Offset 1ACh

Refer to the register description for Source Gather Register for Channel 0 - Low.

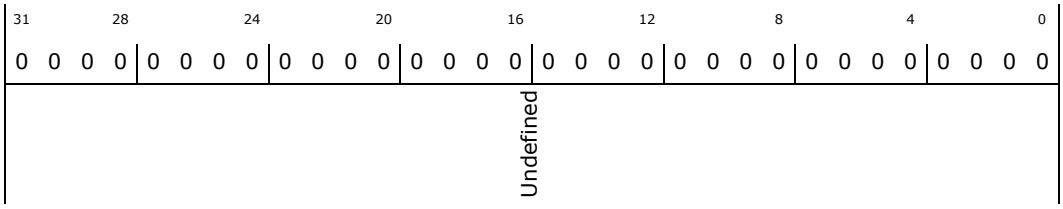
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR4_HI: [BAR] + 1ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.109 Destination Scatter Register for Channel 4 - Low (DSR4_LO)—Offset 1B0h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

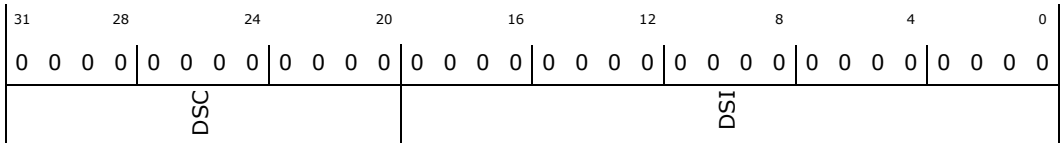
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR4_LO: [BAR] + 1B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.27.110 Dest Scatter Register for Channel 4 - High (DSR4_HI)—Offset 1B4h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

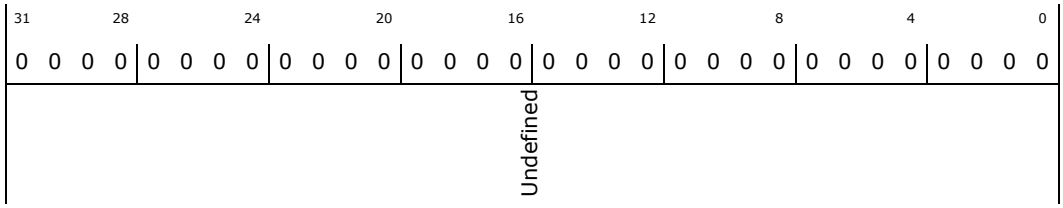
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR4_HI: [BAR] + 1B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.111 Source Address Register for Channel 5 - Low (SAR5_LO)—Offset 1B8h

Refer to the description for register Source Address Register for Channel 0 - Low.

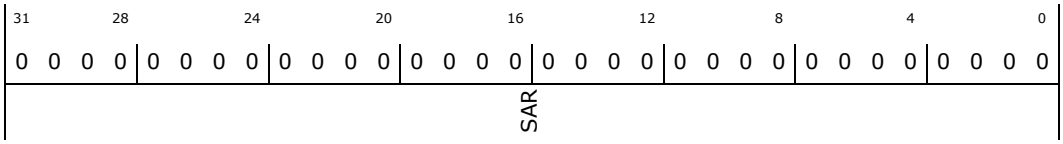
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR5_LO: [BAR] + 1B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.27.112 Source Address Register for Channel 5 - High (SAR5_HI)—Offset 1BCh

Refer to the description for register Source Address Register for Channel 0 - Low.

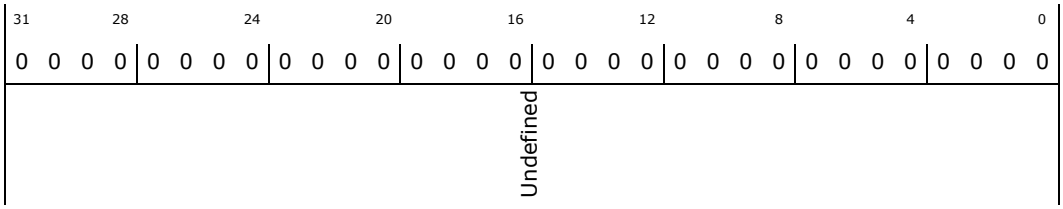
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR5_HI: [BAR] + 1BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.113 Destination Address Register for Channel 5 - Low (DAR5_LO)—Offset 1C0h

Refer to the description for register Destination Address Register for Channel 0 - Low.

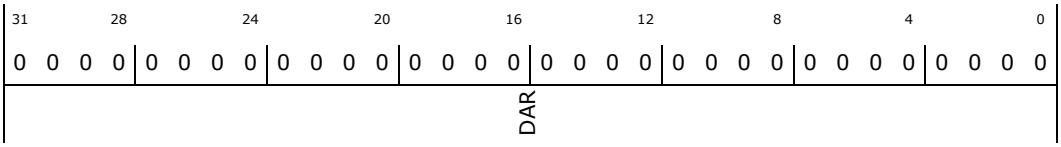
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR5_LO: [BAR] + 1C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.27.114 Destination Address Register for Channel 5 - High (DAR5_HI)—Offset 1C4h

Refer to the description for register Destination Address Register for Channel 0 - Low.

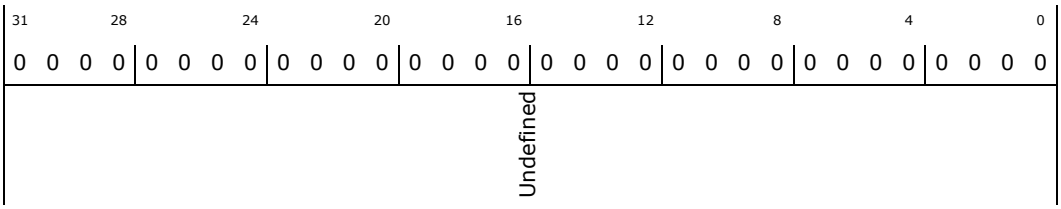
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR5_HI: [BAR] + 1C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.115 Linked List Pointer Register for Channel 5 - Low (LLP5_LO)—Offset 1C8h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

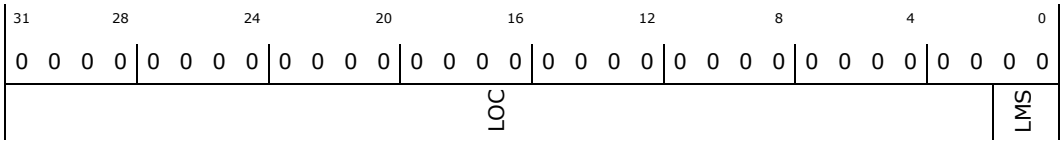
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP5_LO: [BAR] + 1C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.27.116 Linked List Pointer Register for Channel 5 - High (LLP5_HI)—Offset 1CCh

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

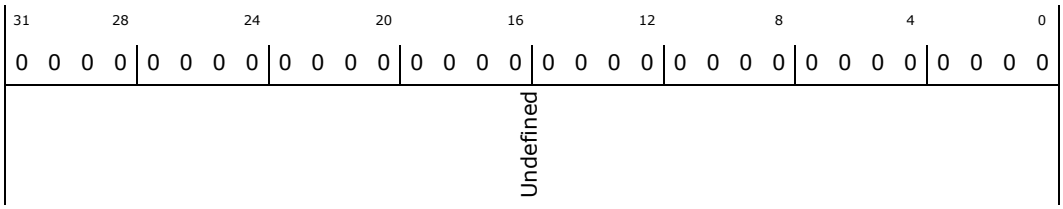
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP5_HI: [BAR] + 1CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.117 Control Register for Channel 5 - Low (CTL5_LO)—Offset 1D0h

Refer to the register description for Control Register for Channel 0 - Low.

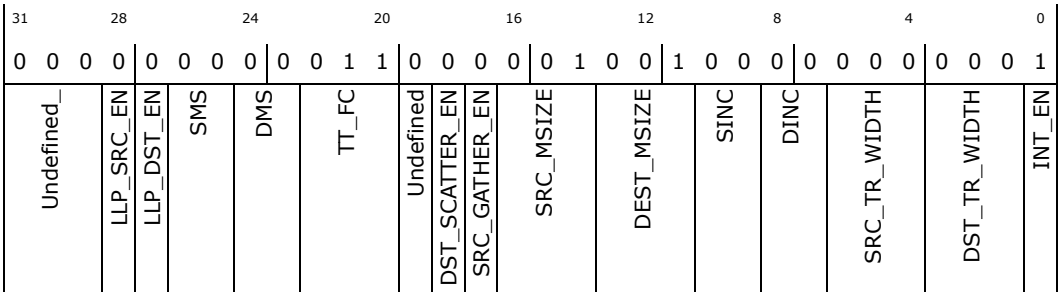
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL5_LO: [BAR] + 1D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.

Bit Range	Default & Access	Description
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.27.118 Control Register for Channel 5 - High (CTL5_HI)—Offset 1D4h

Refer to the register description for Control Register for Channel 0 - Low.

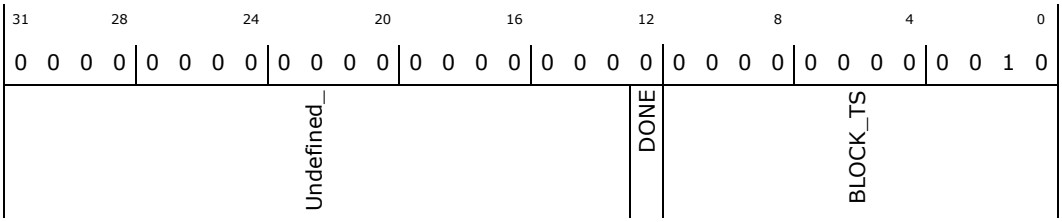
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL5_HI: [BAR] + 1D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.27.119 Source Status Register for Channel 5 - Low (SSTAT5_LO)—Offset 1D8h

Refer to the register description for Source Status Register for Channel 0 - Low.

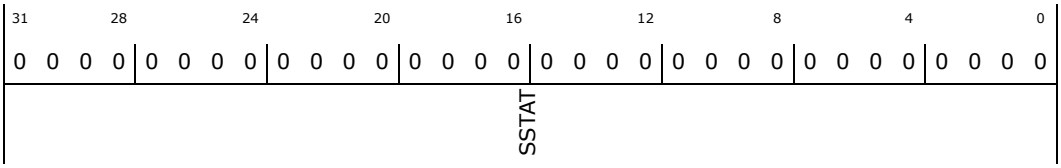
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT5_LO: [BAR] + 1D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.27.120 Source Status Register for Channel 5 - High (SSTAT5_HI)—Offset 1DCh

Refer to the register description for Source Status Register for Channel 0 - Low.

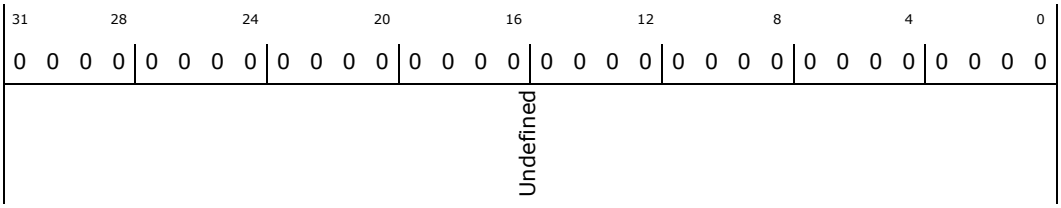
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT5_HI: [BAR] + 1DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.121 Dest Status Register for Channel 5 - Low (DSTAT5_LO)—Offset 1E0h

Refer to the register description for Dest Status Register for Channel 0 - Low.

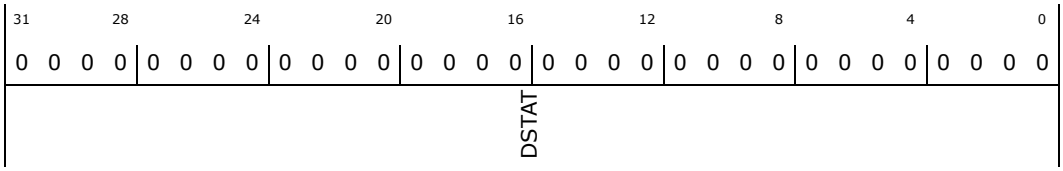
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT5_LO: [BAR] + 1E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

3.27.122 Dest Status Register for Channel 5 - High (DSTAT5_HI)—Offset 1E4h

Refer to the register description for Dest Status Register for Channel 0 - Low.

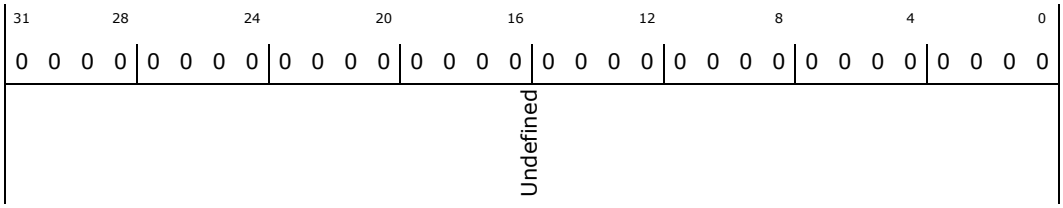
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT5_HI: [BAR] + 1E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.123 Source Status Address Register for Channel 5 - Low (SSTATAR5_LO)—Offset 1E8h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

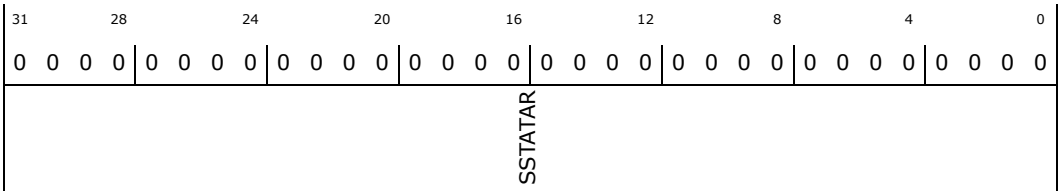
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR5_LO: [BAR] + 1E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.124 Source Status Address Register for Channel 5 - High (SSTATAR5_HI)—Offset 1ECh

Refer to the description for register Source Status Address Register for Channel 0 - Low.

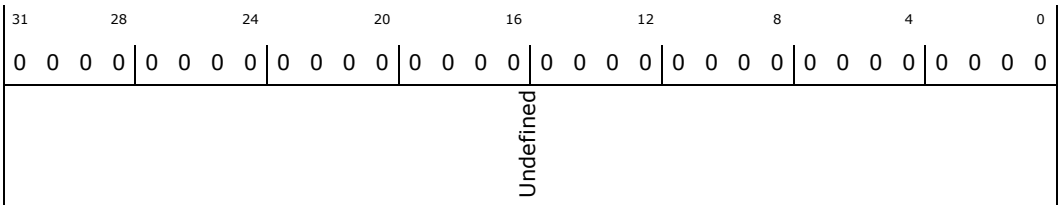
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR5_HI: [BAR] + 1ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.125 Dest Status Address Register for Channel 5 - Low (DSTATAR5_LO)—Offset 1F0h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

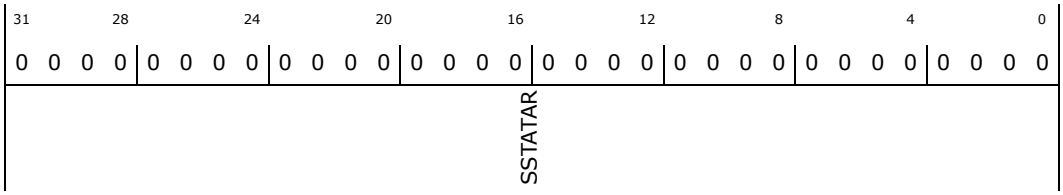
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR5_LO: [BAR] + 1F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.126 Dest Status Address Register for Channel 5 - High (DSTATAR5_HI)—Offset 1F4h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

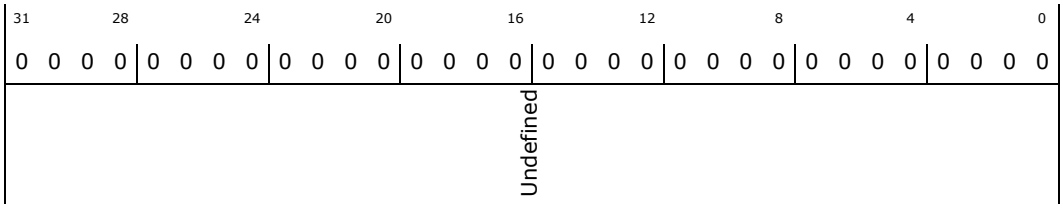
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR5_HI: [BAR] + 1F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.127 Configuration Register for Channel 5 - Low (CFG5_LO)—Offset 1F8h

Refer to the register description for Configuration Register for Channel 0 - Low.

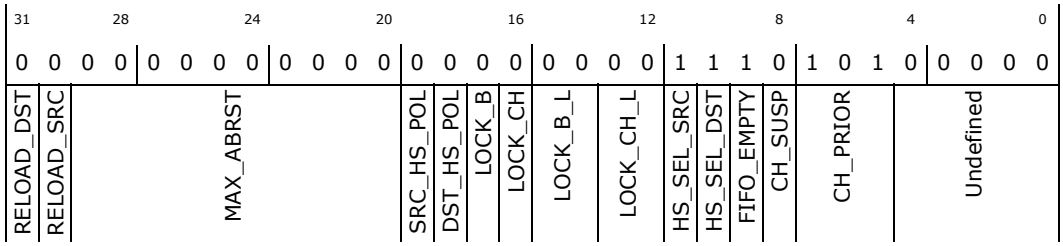
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG5_LO: [BAR] + 1F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000EA0h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface, and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.

Bit Range	Default & Access	Description
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	5h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.27.128 Configuration Register for Channel 5 - High (CFG5_HI)—Offset 1FCh

Refer to the register description for Configuration Register for Channel 0 - Low.

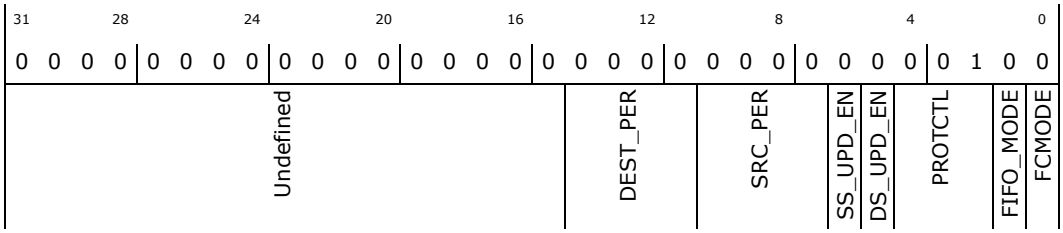
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG5_HI: [BAR] + 1FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the FIFO depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.27.129 Source Gather Register for Channel 5 - Low (SGR5_LO)—Offset 200h

Refer to the register description for Source Gather Register for Channel 0 - Low.

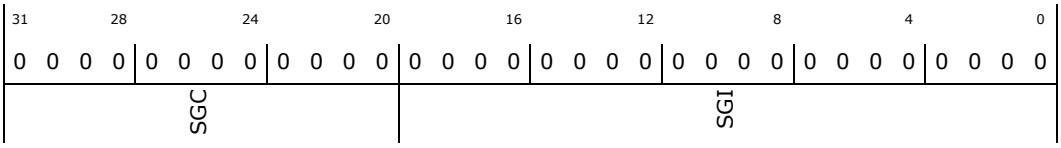
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR5_LO: [BAR] + 200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.27.130 Source Gather Register for Channel 5 - High (SGR5_HI)—Offset 204h

Refer to the register description for Source Gather Register for Channel 0 - Low.

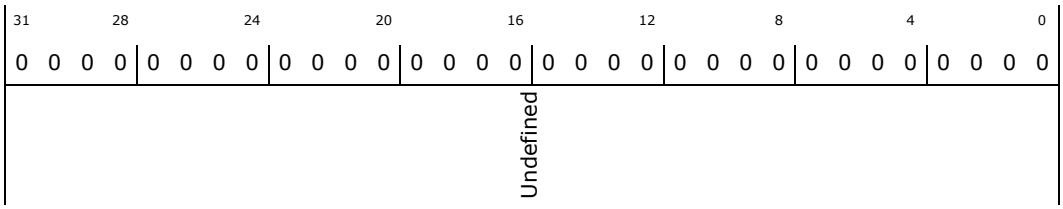
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR5_HI: [BAR] + 204h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.131 Destination Scatter Register for Channel 5 - Low (DSR5_LO)—Offset 208h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

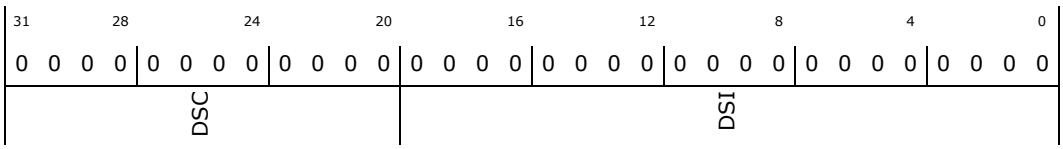
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR5_LO: [BAR] + 208h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.27.132 Dest Scatter Register for Channel 5 - High (DSR5_HI)—Offset 20Ch

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

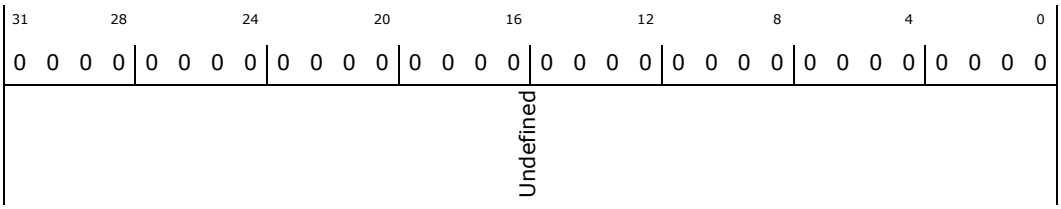
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR5_HI: [BAR] + 20Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.133 Source Address Register for Channel 6 - Low (SAR6_LO)—Offset 210h

Refer to the description for register Source Address Register for Channel 0 - Low.

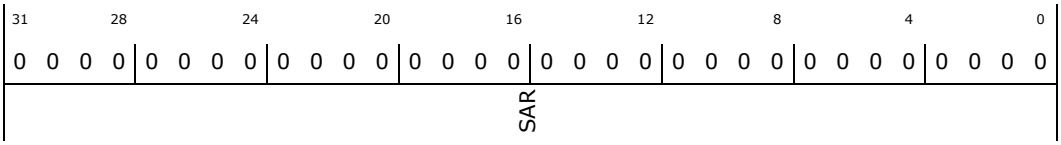
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR6_LO: [BAR] + 210h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.27.134 Source Address Register for Channel 6 - High (SAR6_HI)—Offset 214h

Refer to the description for register Source Address Register for Channel 0 - Low.

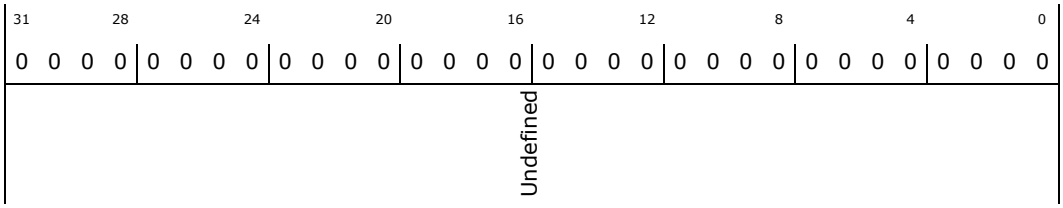
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR6_HI: [BAR] + 214h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.135 Destination Address Register for Channel 6 - Low (DAR6_LO)—Offset 218h

Refer to the description for register Destination Address Register for Channel 0 - Low.

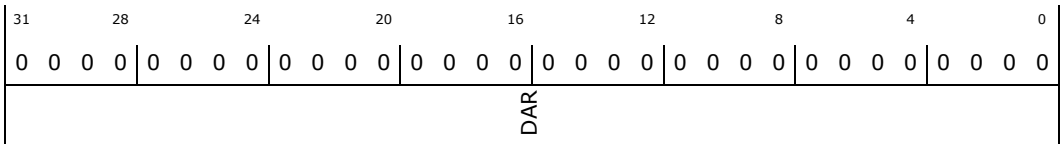
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR6_LO: [BAR] + 218h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.27.136 Destination Address Register for Channel 6 - High (DAR6_HI)—Offset 21Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

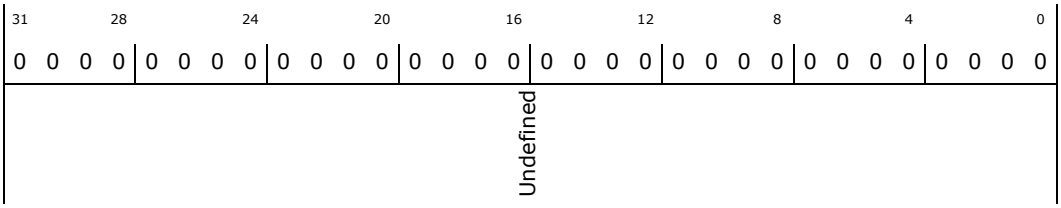
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR6_HI: [BAR] + 21Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.137 Linked List Pointer Register for Channel 6 - Low (LLP6_LO)—Offset 220h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

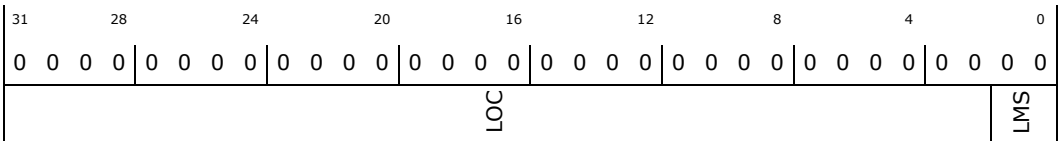
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP6_LO: [BAR] + 220h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.27.138 Linked List Pointer Register for Channel 6 - High (LLP6_HI)—Offset 224h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

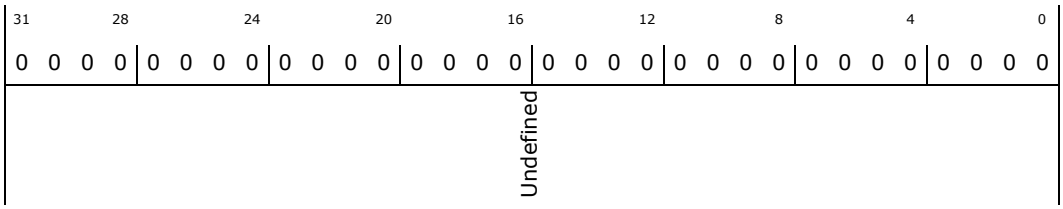
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP6_HI: [BAR] + 224h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.139 Control Register for Channel 6 - Low (CTL6_LO)—Offset 228h

Refer to the register description for Control Register for Channel 0 - Low.

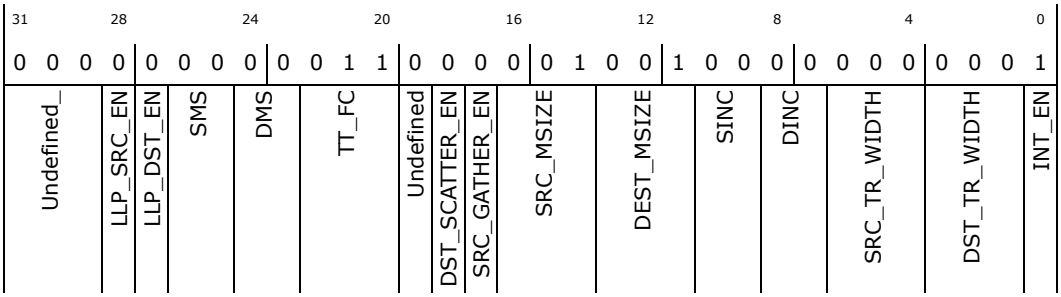
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL6_LO: [BAR] + 228h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.

Bit Range	Default & Access	Description
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.27.140 Control Register for Channel 6 - High (CTL6_HI)—Offset 22Ch

Refer to the register description for Control Register for Channel 0 - Low.

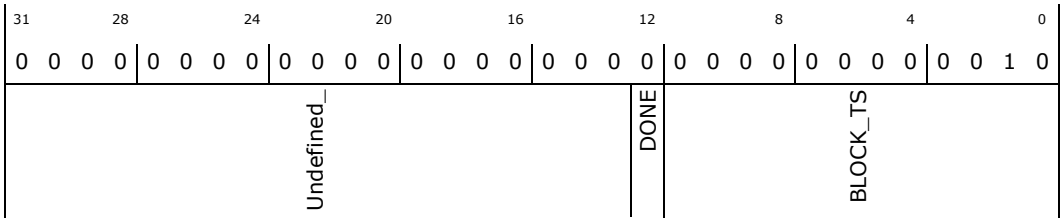
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL6_HI: [BAR] + 22Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.27.141 Source Status Register for Channel 6 - Low (SSTAT6_LO)—Offset 230h

Refer to the register description for Source Status Register for Channel 0 - Low.

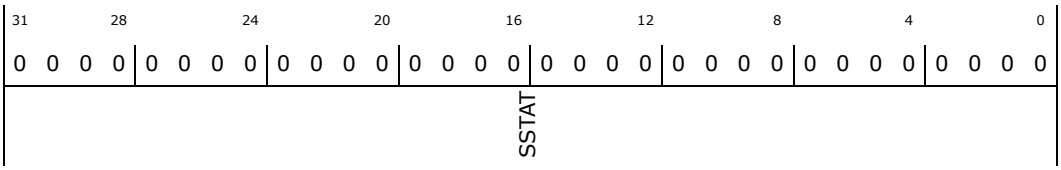
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT6_LO: [BAR] + 230h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.27.142 Source Status Register for Channel 6 - High (SSTAT6_HI)—Offset 234h

Refer to the register description for Source Status Register for Channel 0 - Low.

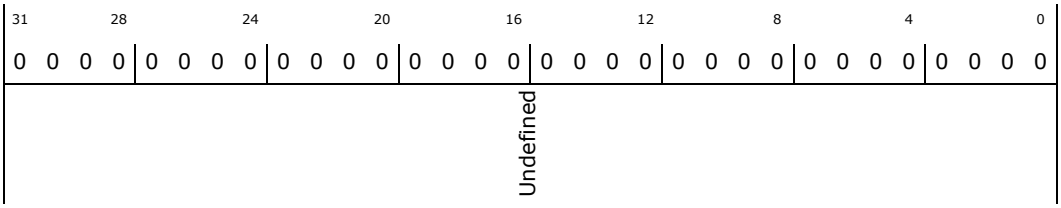
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT6_HI: [BAR] + 234h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.143 Dest Status Register for Channel 6 - Low (DSTAT6_LO)—Offset 238h

Refer to the register description for Dest Status Register for Channel 0 - Low.

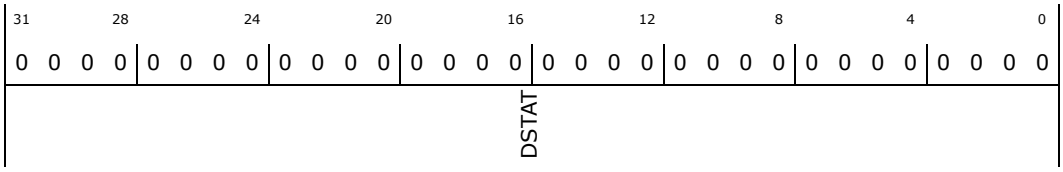
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT6_LO: [BAR] + 238h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

3.27.144 Dest Status Register for Channel 6 - High (DSTAT6_HI)—Offset 23Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

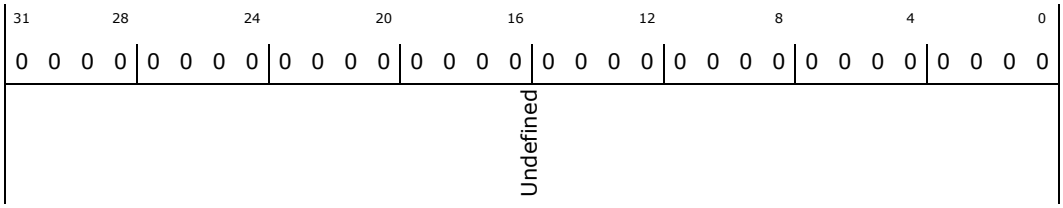
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT6_HI: [BAR] + 23Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.145 Source Status Address Register for Channel 6 - Low (SSTATAR6_LO)—Offset 240h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

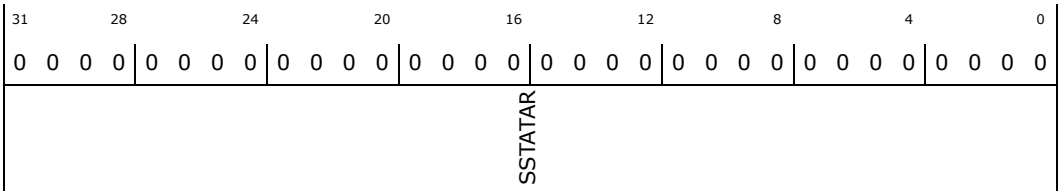
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR6_LO: [BAR] + 240h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.146 Source Status Address Register for Channel 6 - High (SSTATAR6_HI)—Offset 244h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

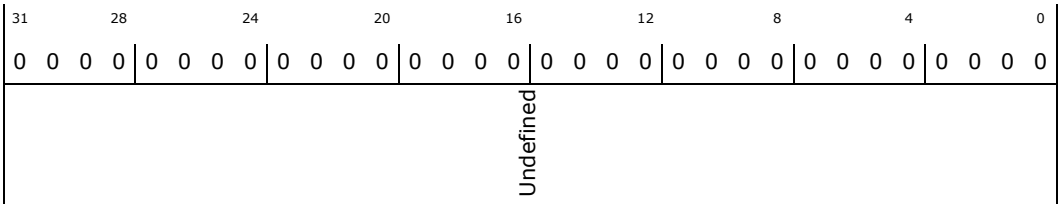
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR6_HI: [BAR] + 244h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.147 Dest Status Address Register for Channel 6 - Low (DSTATAR6_LO)—Offset 248h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

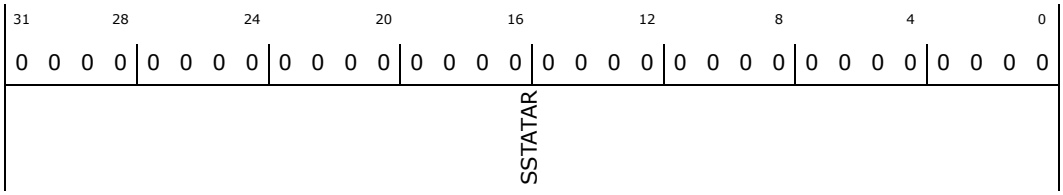
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR6_LO: [BAR] + 248h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.148 Dest Status Address Register for Channel 6 - High (DSTATAR6_HI)—Offset 24Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

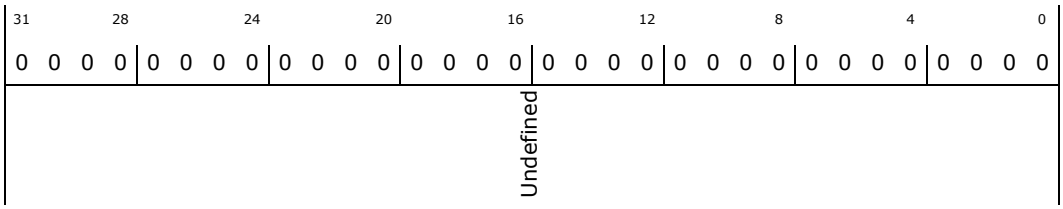
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR6_HI: [BAR] + 24Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.149 Configuration Register for Channel 6 - Low (CFG6_LO)—Offset 250h

Refer to the register description for Configuration Register for Channel 0 - Low.

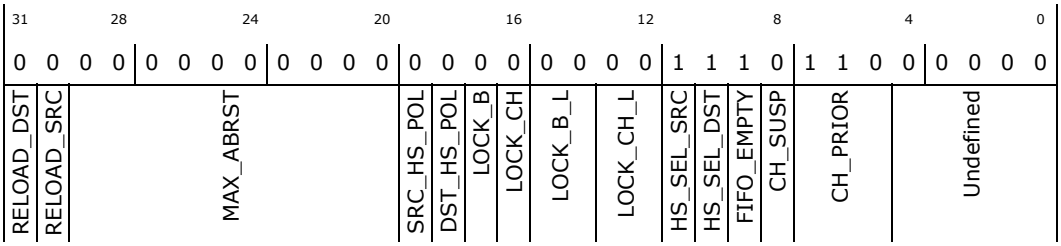
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG6_LO: [BAR] + 250h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000EC0h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking

Bit Range	Default & Access	Description
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	6h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.27.150 Configuration Register for Channel 6 - High (CFG6_HI)—Offset 254h

Refer to the register description for Configuration Register for Channel 0 - Low.

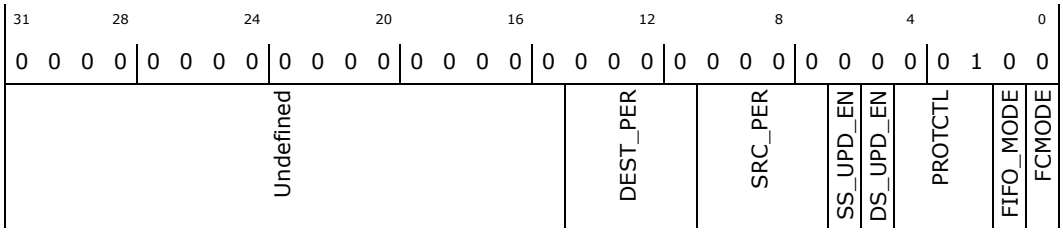
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG6_HI: [BAR] + 254h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.

Bit Range	Default & Access	Description
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.27.151 Source Gather Register for Channel 6 - Low (SGR6_LO)—Offset 258h

Refer to the register description for Source Gather Register for Channel 0 - Low.

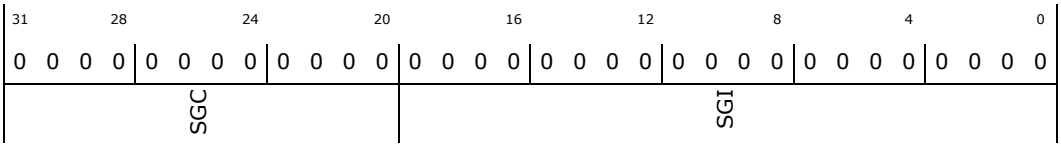
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR6_LO: [BAR] + 258h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.27.152 Source Gather Register for Channel 6 - High (SGR6_HI)—Offset 25Ch

Refer to the register description for Source Gather Register for Channel 0 - Low.

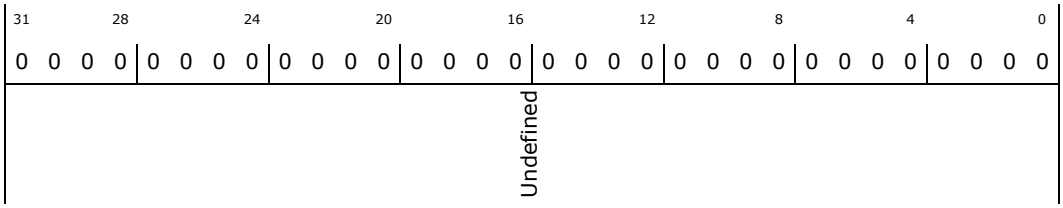
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR6_HI: [BAR] + 25Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.153 Destination Scatter Register for Channel 6 - Low (DSR6_LO)—Offset 260h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

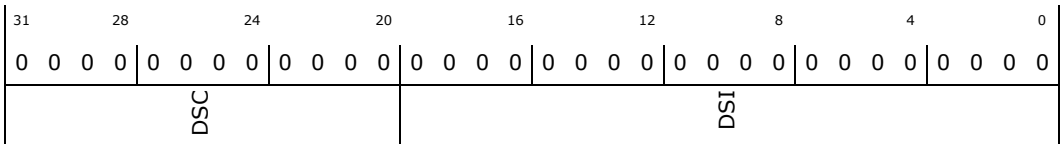
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR6_LO: [BAR] + 260h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.27.154 Dest Scatter Register for Channel 6 - High (DSR6_HI)—Offset 264h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

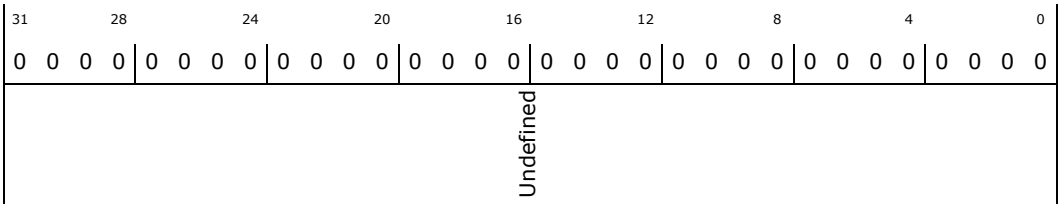
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR6_HI: [BAR] + 264h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.155 Source Address Register for Channel 7 - Low (SAR7_LO)—Offset 268h

Refer to the description for register Source Address Register for Channel 0 - Low.

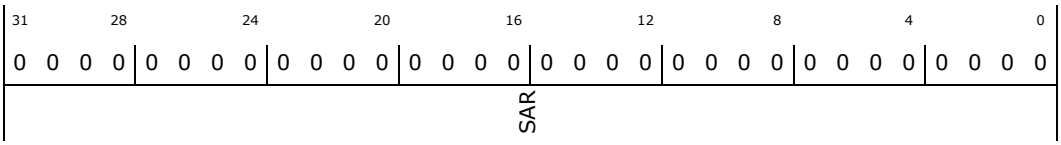
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR7_LO: [BAR] + 268h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.27.156 Source Address Register for Channel 7 - High (SAR7_HI)—Offset 26Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

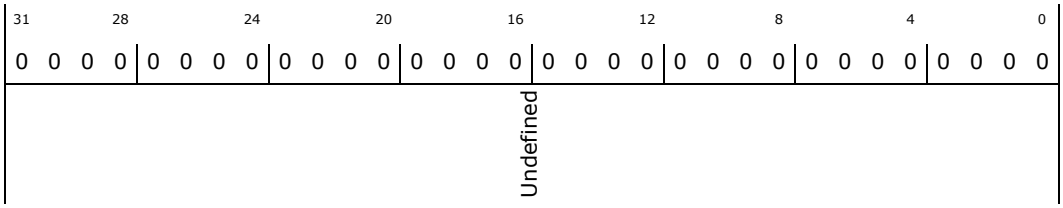
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR7_HI: [BAR] + 26Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.157 Destination Address Register for Channel 7 - Low (DAR7_LO)—Offset 270h

Refer to the description for register Destination Address Register for Channel 0 - Low.

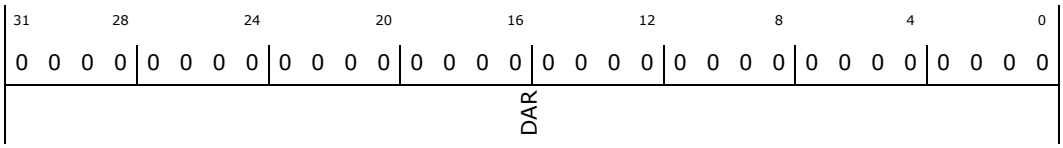
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR7_LO: [BAR] + 270h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.27.158 Destination Address Register for Channel 7 - High (DAR7_HI)—Offset 274h

Refer to the description for register Destination Address Register for Channel 0 - Low.

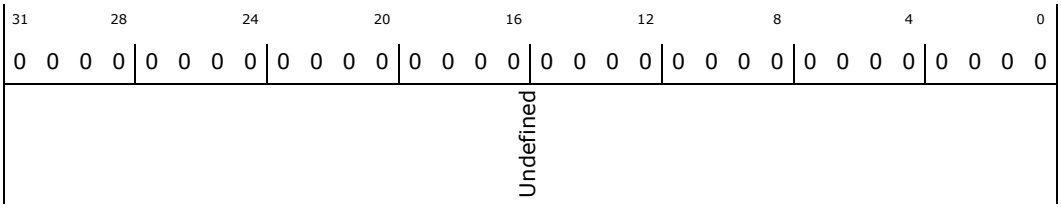
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR7_HI: [BAR] + 274h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.159 Linked List Pointer Register for Channel 7 - Low (LLP7_LO)—Offset 278h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

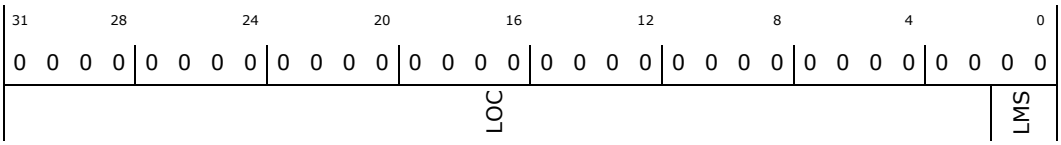
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP7_LO: [BAR] + 278h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.27.160 Linked List Pointer Register for Channel 7 - High (LLP7_HI)—Offset 27Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

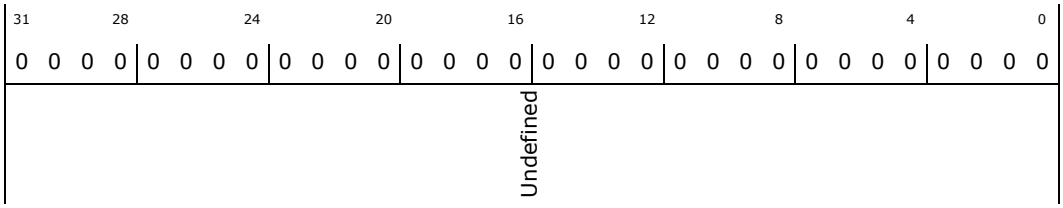
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP7_HI: [BAR] + 27Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.161 Control Register for Channel 7 - Low (CTL7_LO)—Offset 280h

Refer to the register description for Control Register for Channel 0 - Low.

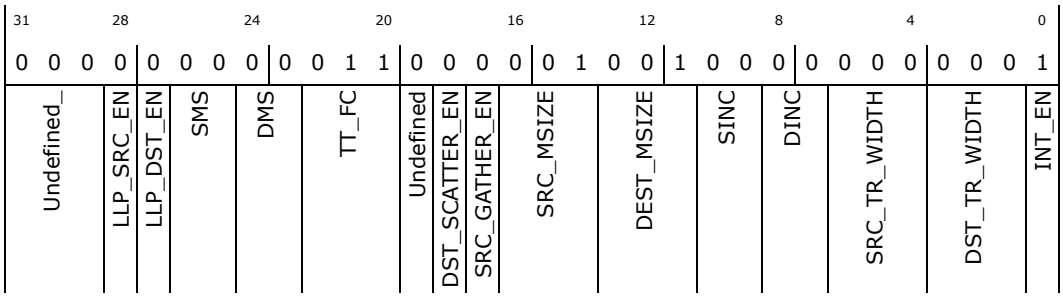
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL7_LO: [BAR] + 280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.

Bit Range	Default & Access	Description
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.27.162 Control Register for Channel 7 - High (CTL7_HI)—Offset 284h

Refer to the register description for Control Register for Channel 0 - Low.

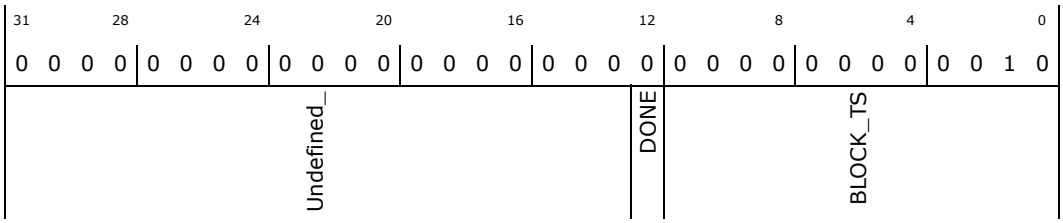
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL7_HI: [BAR] + 284h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.27.163 Source Status Register for Channel 7 - Low (SSTAT7_LO)—Offset 288h

Refer to the register description for Source Status Register for Channel 0 - Low.

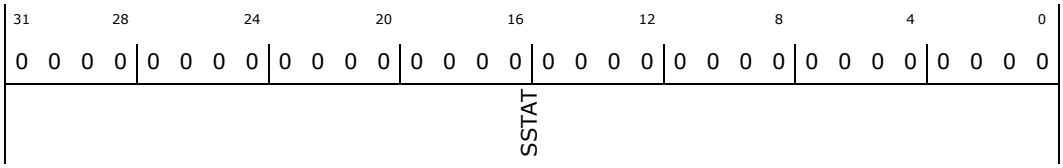
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT7_LO: [BAR] + 288h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.27.164 Source Status Register for Channel 7 - High (SSTAT7_HI)—Offset 28Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

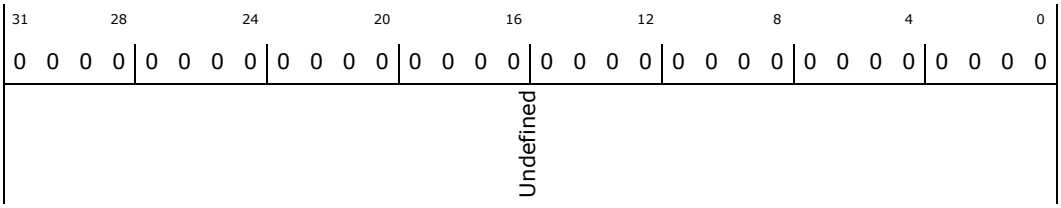
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT7_HI: [BAR] + 28Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.165 Dest Status Register for Channel 7 - Low (DSTAT7_LO)—Offset 290h

Refer to the register description for Dest Status Register for Channel 0 - Low.

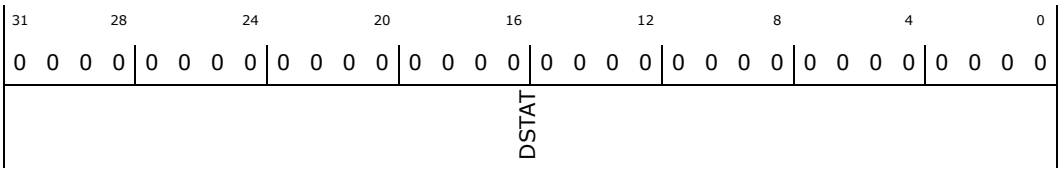
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT7_LO: [BAR] + 290h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

3.27.166 Dest Status Register for Channel 7 - High (DSTAT7_HI)—Offset 294h

Refer to the register description for Dest Status Register for Channel 0 - Low.

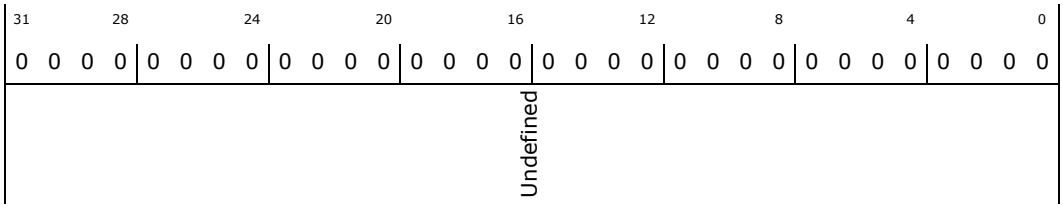
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT7_HI: [BAR] + 294h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.167 Source Status Address Register for Channel 7 - Low (SSTATAR7_LO)—Offset 298h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

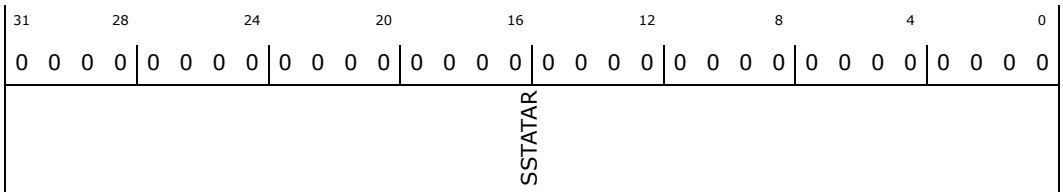
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR7_LO: [BAR] + 298h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.168 Source Status Address Register for Channel 7 - High (SSTATAR7_HI)—Offset 29Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

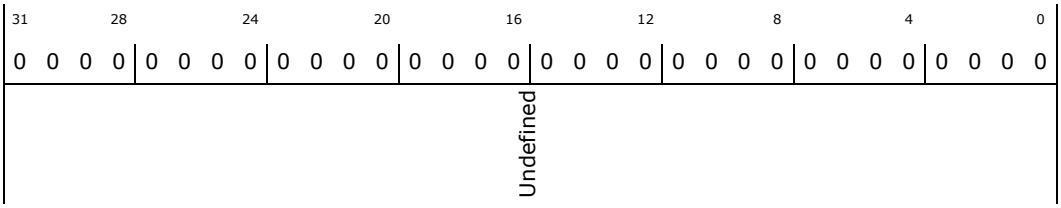
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR7_HI: [BAR] + 29Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.169 Dest Status Address Register for Channel 7 - Low (DSTATAR7_LO)—Offset 2A0h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

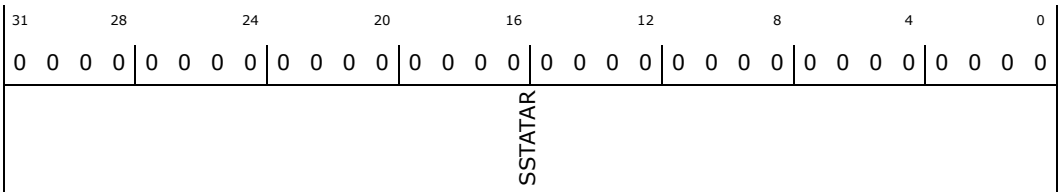
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR7_LO: [BAR] + 2A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.27.170 Dest Status Address Register for Channel 7 - High (DSTATAR7_HI)—Offset 2A4h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

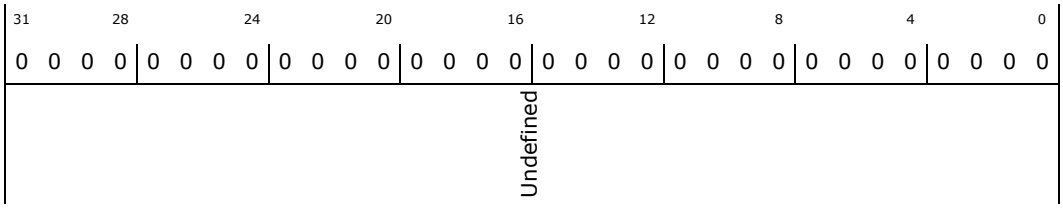
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR7_HI: [BAR] + 2A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.27.171 Configuration Register for Channel 7 - Low (CFG7_LO)—Offset 2A8h

Refer to the register description for Configuration Register for Channel 0 - Low.

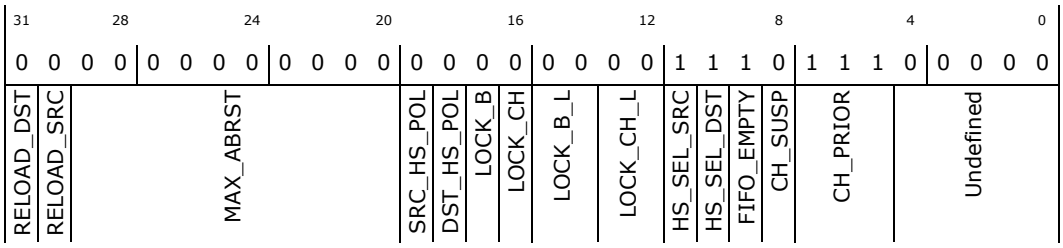
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

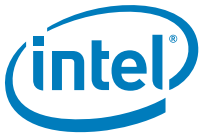
CFG7_LO: [BAR] + 2A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000EE0h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.



Bit Range	Default & Access	Description
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	7h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.27.172 Configuration Register for Channel 7 - High (CFG7_HI)—Offset 2ACh

Refer to the register description for Configuration Register for Channel 0 - Low.

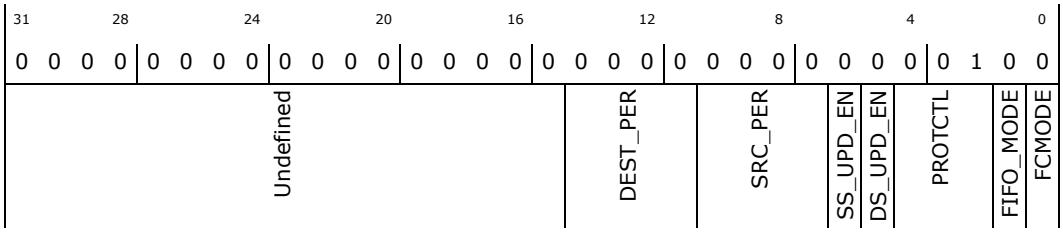
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG7_HI: [BAR] + 2ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.27.173 Source Gather Register for Channel 7 - Low (SGR7_LO)—Offset 2B0h

Refer to the register description for Source Gather Register for Channel 0 - Low.

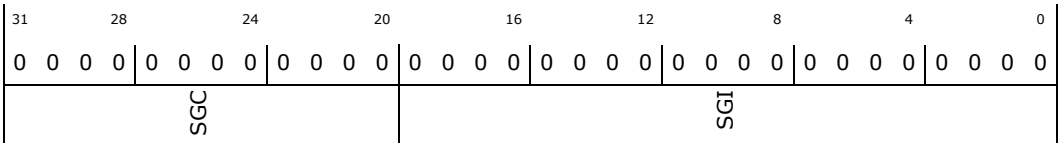
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR7_LO: [BAR] + 2B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.27.174 Source Gather Register for Channel 7 - High (SGR7_HI)—Offset 2B4h

Refer to the register description for Source Gather Register for Channel 0 - Low.

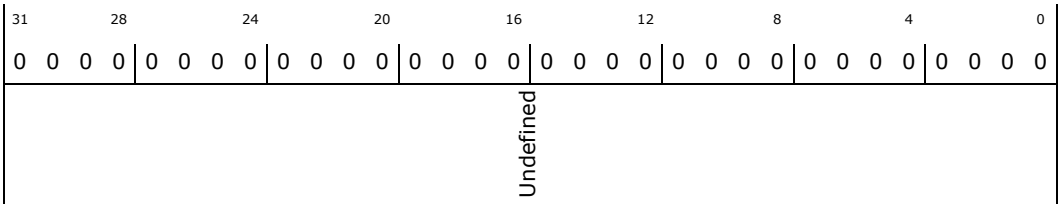
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR7_HI: [BAR] + 2B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.175 Destination Scatter Register for Channel 7 - Low (DSR7_LO)—Offset 2B8h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

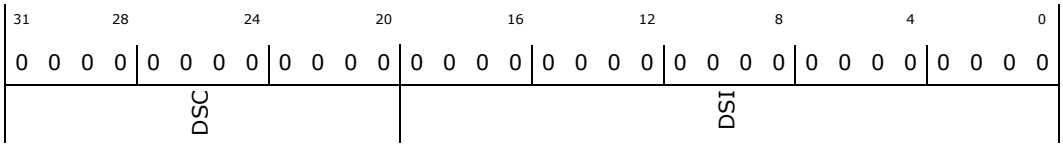
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR7_LO: [BAR] + 2B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.27.176 Dest Scatter Register for Channel 7 - High (DSR7_HI)—Offset 2BCh

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

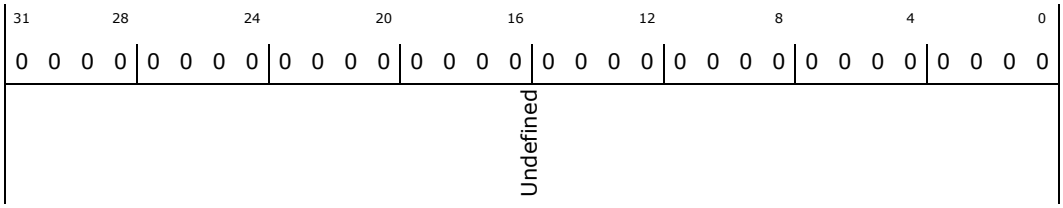
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR7_HI: [BAR] + 2BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.177 Interrupt Raw Status Registers - Low (RawTfr_LO)—Offset 2C0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel; for example, RawTfr[2] is the Channel 2 raw transfer complete interrupt.

Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

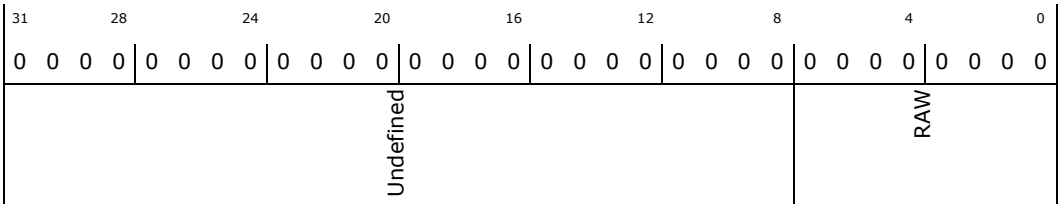
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawTfr_LO: [BAR] + 2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

3.27.178 Interrupt Raw Status Registers - High (RawTfr_HI)—Offset 2C4h

Refer to the description for Interrupt Raw Status Registers - Low.

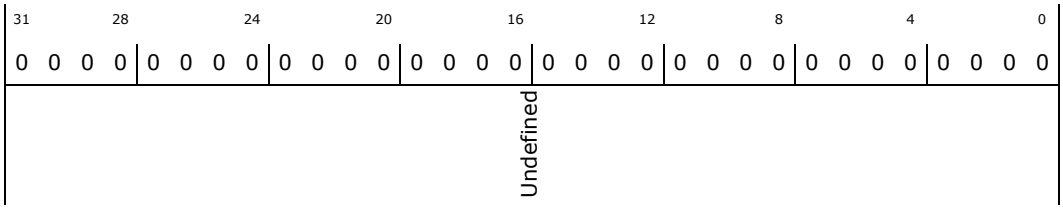
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawTfr_HI: [BAR] + 2C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.179 Interrupt Raw Status Registers - Low (RawBlock_LO)—Offset 2C8h

Refer to the description of the register with short name RawTfr_LO.

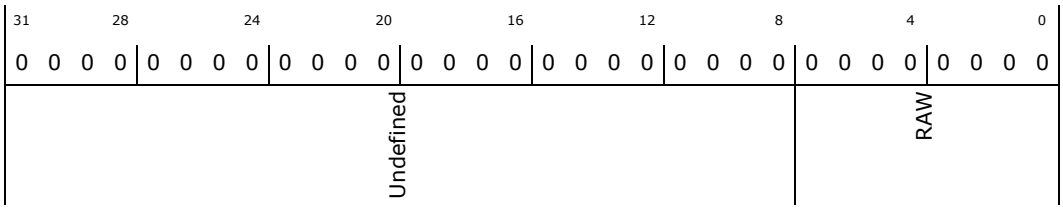
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawBlock_LO: [BAR] + 2C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

3.27.180 Interrupt Raw Status Registers - High (RawBlock_HI)—Offset 2CCh

Refer to the description of the register with short name RawTfr_LO.

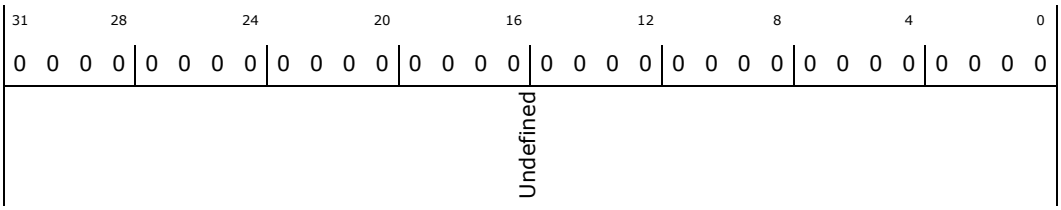
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawBlock_HI: [BAR] + 2CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.181 Interrupt Raw Status Registers - Low (RawSrcTran_LO)—Offset 2D0h

Refer to the description of the register with short name RawTfr_LO.

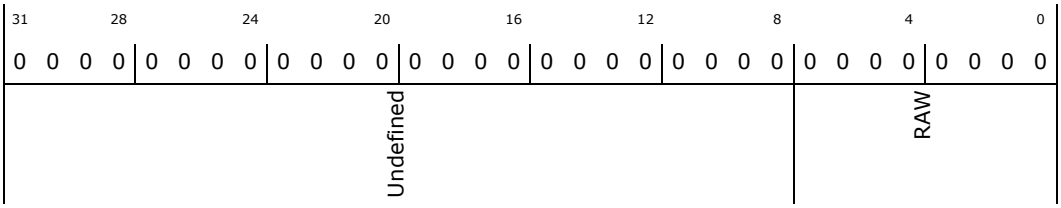
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawSrcTran_LO: [BAR] + 2D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

3.27.182 Interrupt Raw Status Registers - High (RawSrcTran_HI)—Offset 2D4h

Refer to the description of the register with short name RawTfr_LO.

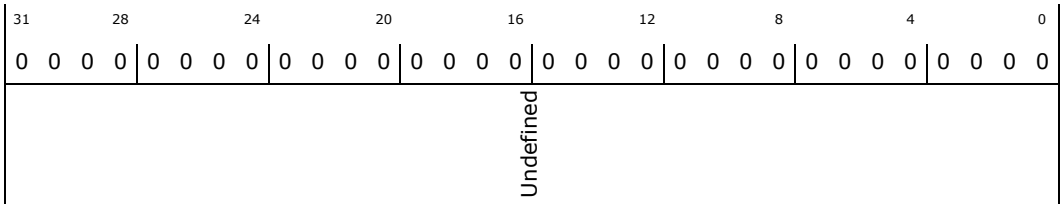
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawSrcTran_HI: [BAR] + 2D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.183 Interrupt Raw Status Registers - Low (RawDstTran_LO)—Offset 2D8h

Refer to the description of the register with short name RawTfr_LO.

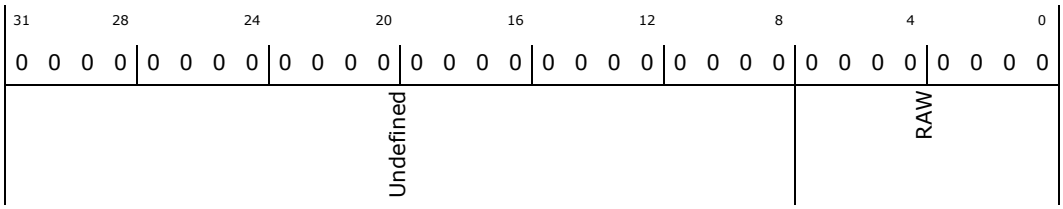
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawDstTran_LO: [BAR] + 2D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

3.27.184 Interrupt Raw Status Registers - High (RawDstTran_HI)—Offset 2DCh

Refer to the description of the register with short name RawTfr_LO.

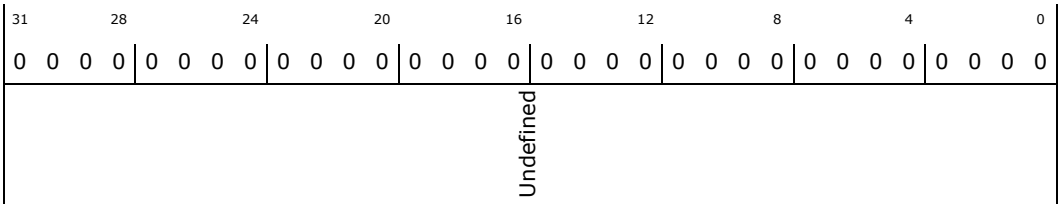
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawDstTran_HI: [BAR] + 2DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.185 Interrupt Raw Status Registers - Low (RawErr_LO)—Offset 2E0h

Refer to the description of the register with short name RawTfr_LO.

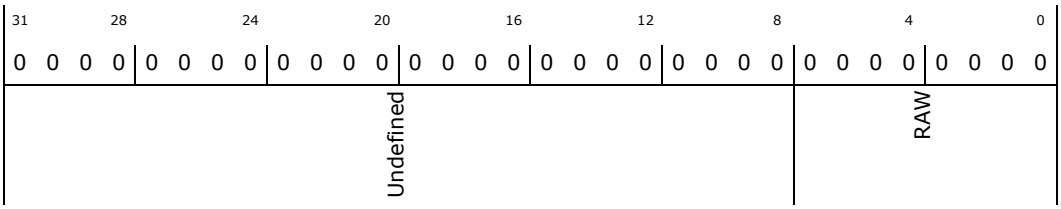
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawErr_LO: [BAR] + 2E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

3.27.186 Interrupt Raw Status Registers - High (RawErr_HI)—Offset 2E4h

Refer to the description of the register with short name RawTfr_LO.

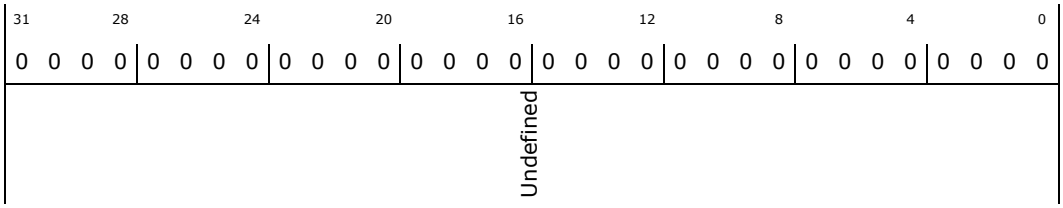
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawErr_HI: [BAR] + 2E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.187 Interrupt Status Registers - Low (StatusTfr_LO)—Offset 2E8h

Refer to the description for register StatusTfr_HI.

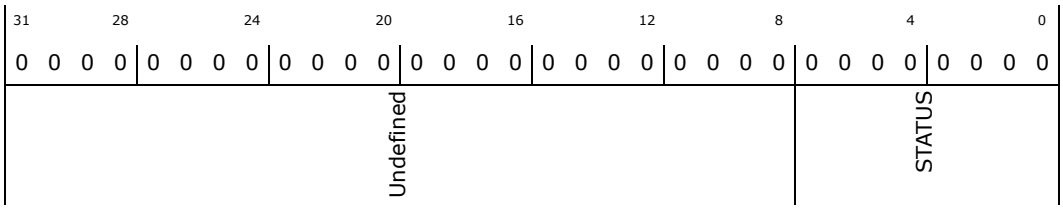
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusTfr_LO: [BAR] + 2E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

3.27.188 Interrupt Status Registers - High (StatusTfr_HI)—Offset 2ECh

All interrupt events from all channels are stored in these Interrupt Status registers after masking: StatusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel; for example, StatusTfr[2] is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DW_ahb_dmac.

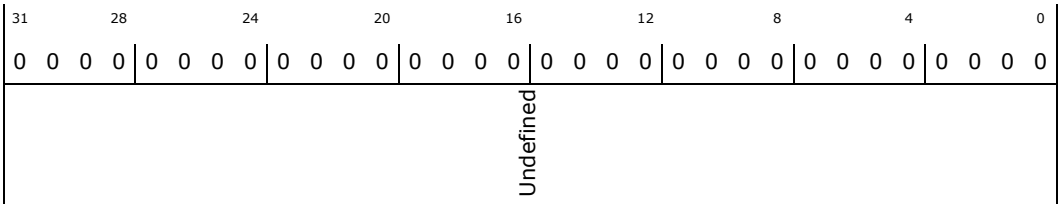
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusTfr_HI: [BAR] + 2ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.189 Interrupt Status Registers - Low (StatusBlock_LO)—Offset 2F0h

Refer to the description for register StatusTfr_HI.

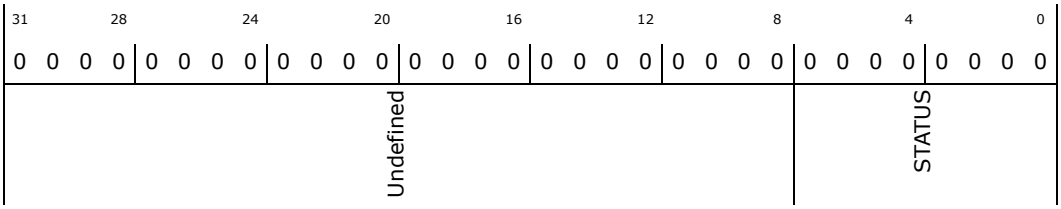
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusBlock_LO: [BAR] + 2F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

3.27.190 Interrupt Status Registers - High (StatusBlock_HI)—Offset 2F4h

Refer to the description for register StatusTfr_HI.

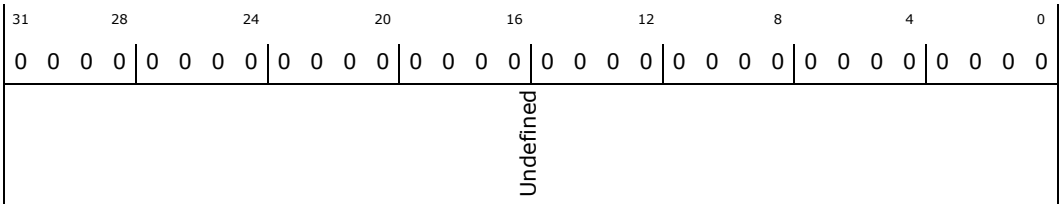
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusBlock_HI: [BAR] + 2F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.191 Interrupt Status Registers - Low (StatusSrcTran_LO)—Offset 2F8h

Refer to the description for register StatusTfr_HI.

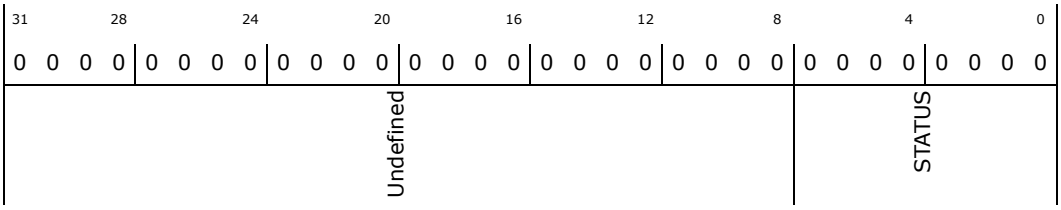
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusSrcTran_LO: [BAR] + 2F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

3.27.192 Interrupt Status Registers - High (StatusSrcTran_HI)—Offset 2FCh

Refer to the description for register StatusTfr_HI.

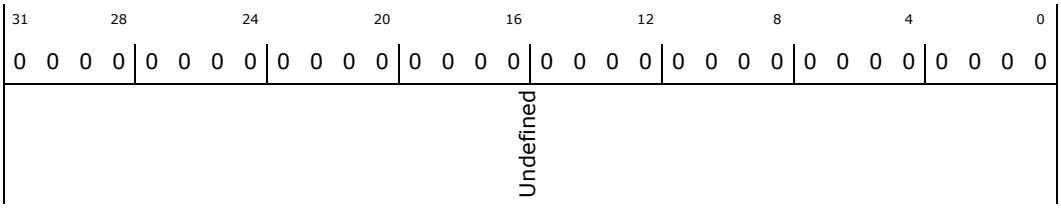
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusSrcTran_HI: [BAR] + 2FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.193 Interrupt Status Registers - Low (StatusDstTran_LO)—Offset 300h

Refer to the description for register StatusTfr_HI.

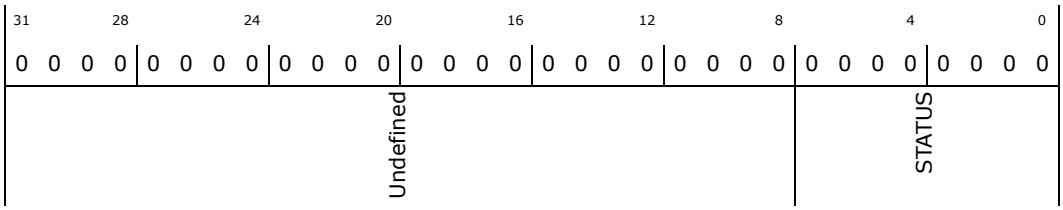
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusDstTran_LO: [BAR] + 300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

3.27.194 Interrupt Status Registers - High (StatusDstTran_HI)—Offset 304h

Refer to the description for register StatusTfr_HI.

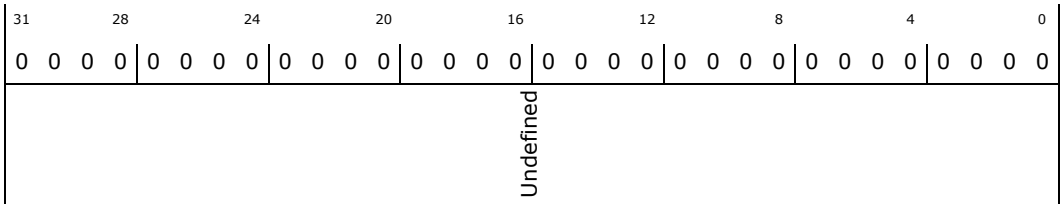
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusDstTran_HI: [BAR] + 304h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.195 Interrupt Status Registers - Low (StatusErr_LO)—Offset 308h

Refer to the description for register StatusTfr_HI.

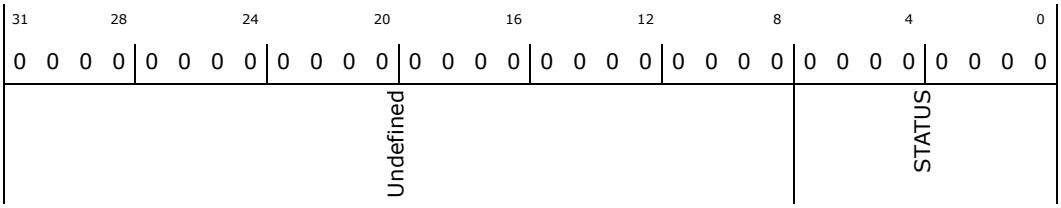
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusErr_LO: [BAR] + 308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

3.27.196 Interrupt Status Registers - High (StatusErr_HI)—Offset 30Ch

Refer to the description for register StatusTfr_HI.

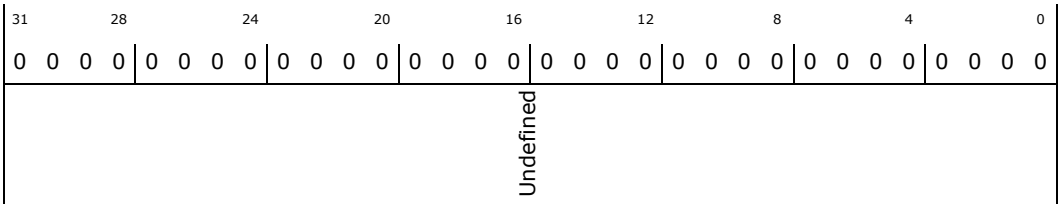
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusErr_HI: [BAR] + 30Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.197 Interrupt Mask Registers - Low (MaskTfr_LO)—Offset 310h

Refer to the description for register MaskBlock_LO.

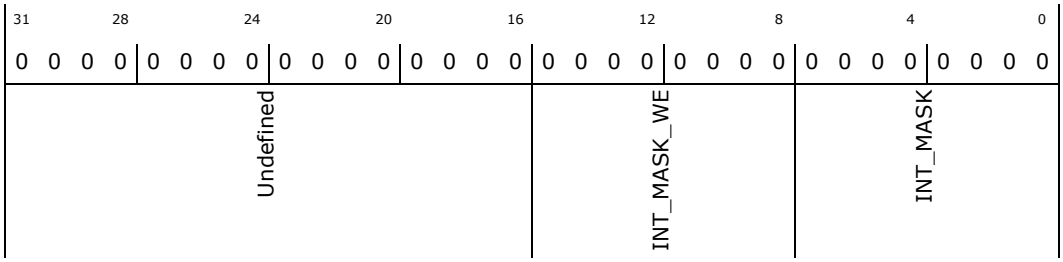
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskTfr_LO: [BAR] + 310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h RW	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

3.27.198 Interrupt Mask Registers - High (MaskTfr_HI)—Offset 314h

Refer to the description for register MaskBlock_LO.

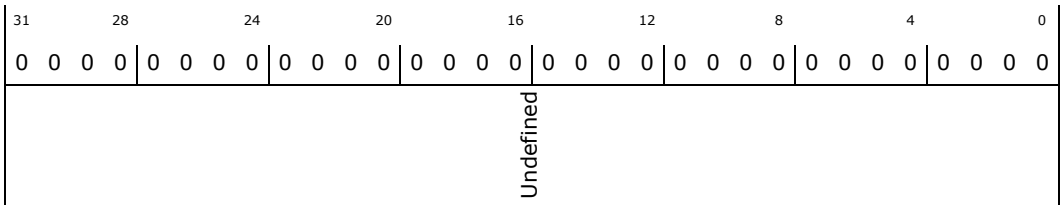
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskTfr_HI: [BAR] + 314h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.199 Interrupt Mask Registers - Low (MaskBlock_LO)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel; for example, MaskTfr[2] is the mask bit for the Channel 2 transfer complete interrupt. Refer to the DesignWare SW_ahb_dmac Databook for details.

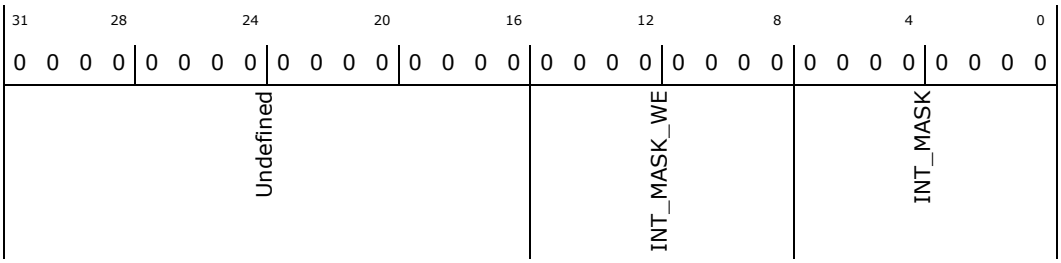
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskBlock_LO: [BAR] + 318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt Mask • 0 = masked • 1 = unmasked

3.27.200 Interrupt Mask Registers - High (MaskBlock_HI)—Offset 31Ch

Refer to the description for register MaskBlock_LO.

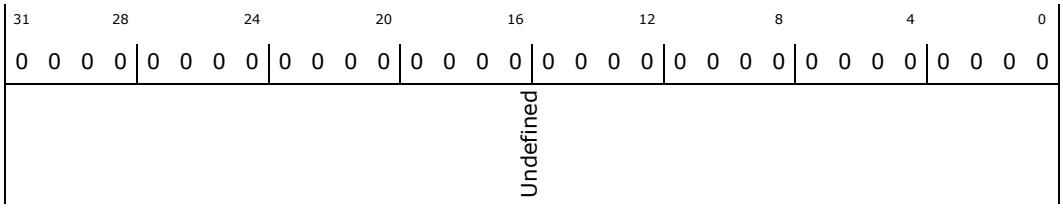
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskBlock_HI: [BAR] + 31Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.201 Interrupt Mask Registers - Low (MaskSrcTran_LO)—Offset 320h

Refer to the description for register MaskBlock_LO.

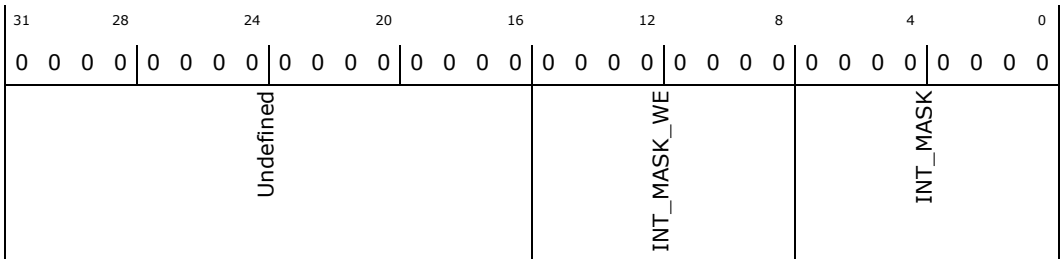
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskSrcTran_LO: [BAR] + 320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

3.27.202 Interrupt Mask Registers - High (MaskSrcTran_HI)—Offset 324h

Refer to the description for register MaskBlock_LO.

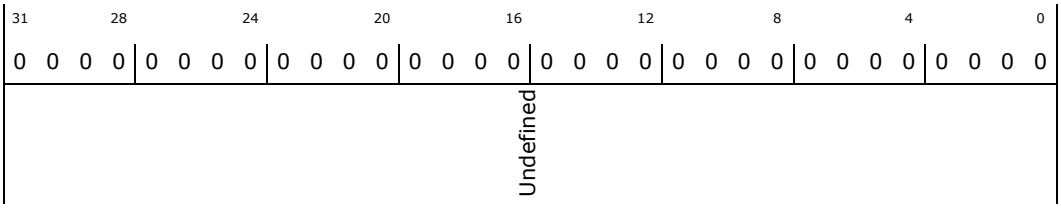
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskSrcTran_HI: [BAR] + 324h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.203 Interrupt Mask Registers - Low (MaskDstTran_LO)—Offset 328h

Refer to the description for register MaskBlock_LO.

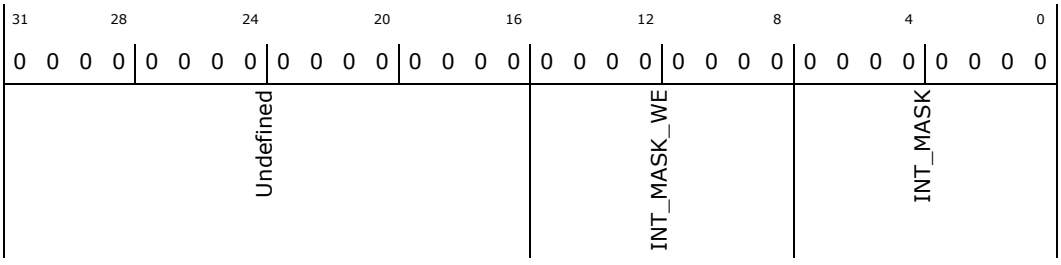
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskDstTran_LO: [BAR] + 328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Description
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

3.27.204 Interrupt Mask Registers - High (MaskDstTran_HI)—Offset 32Ch

Refer to the description for register MaskBlock_LO.

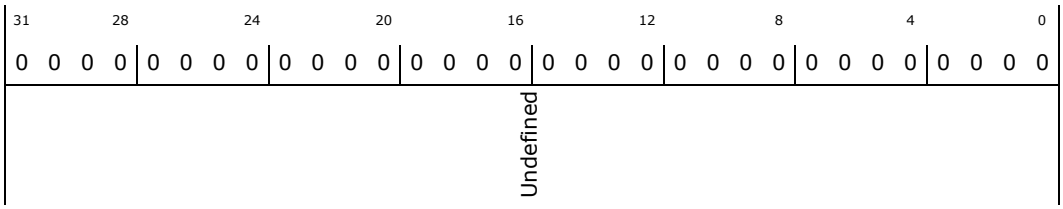
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskDstTran_HI: [BAR] + 32Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.205 Interrupt Mask Registers - Low (MaskErr_LO)—Offset 330h

Refer to the description for register MaskBlock_LO.

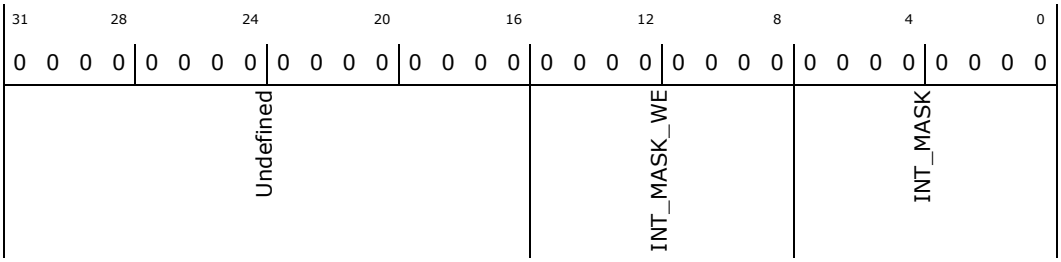
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskErr_LO: [BAR] + 330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

3.27.206 Interrupt Mask Registers - High (MaskErr_HI)—Offset 334h

Refer to the description for register MaskBlock_LO.

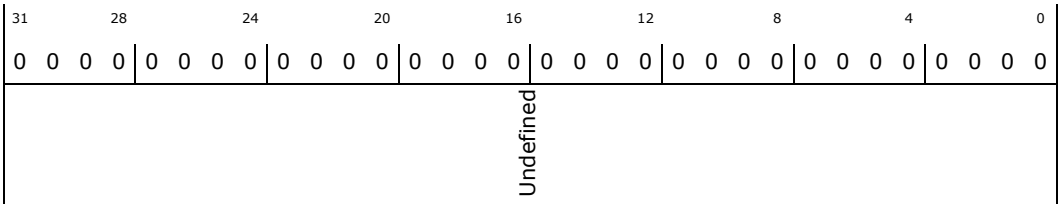
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskErr_HI: [BAR] + 334h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.207 Interrupt Clear Registers - Low (ClearTfr_LO)—Offset 338h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel; for example, ClearTfr[2] is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

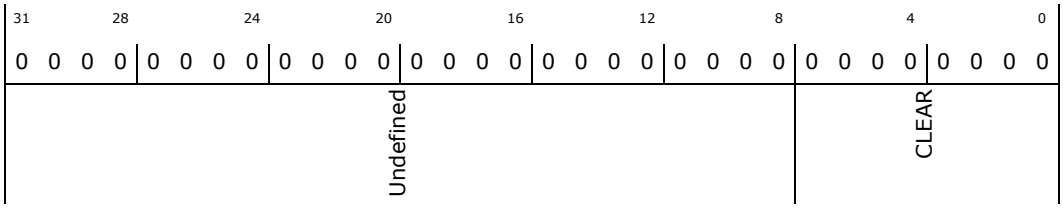
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearTfr_LO: [BAR] + 338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

3.27.208 Interrupt Clear Registers - High (ClearTfr_HI)—Offset 33Ch

Refer to the description for register ClearTfr_HI.

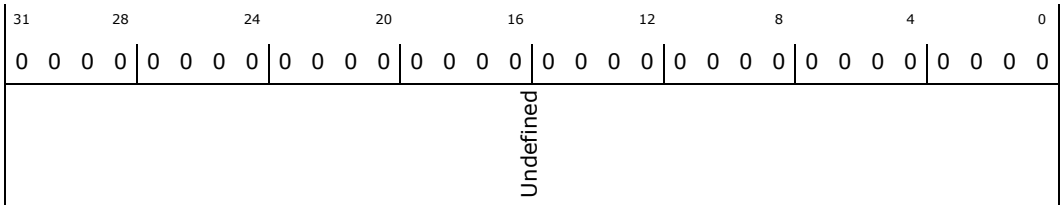
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearTfr_HI: [BAR] + 33Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.209 Interrupt Clear Registers - Low (ClearBlock_LO)—Offset 340h

Refer to the description for register ClearTfr_HI.

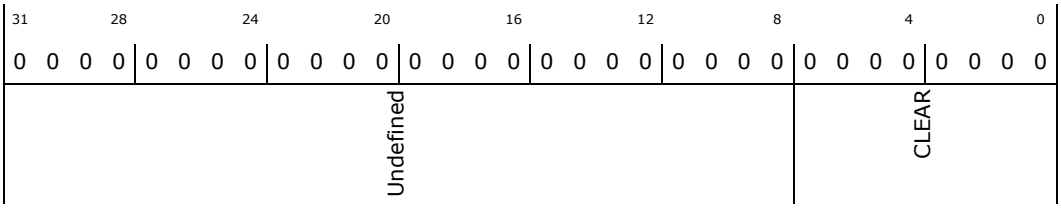
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearBlock_LO: [BAR] + 340h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

3.27.210 Interrupt Clear Registers (ClearBlock_HI)—Offset 344h

Refer to the description for register ClearTfr_HI.

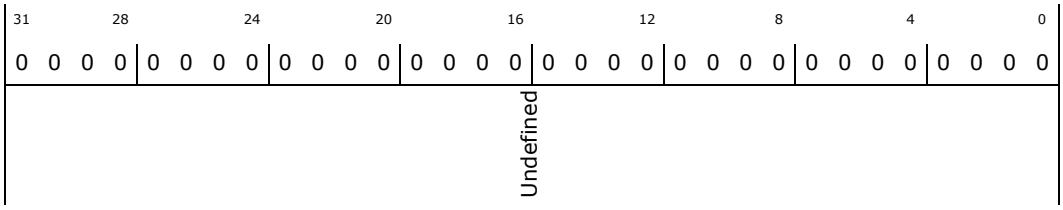
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearBlock_HI: [BAR] + 344h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.211 Interrupt Clear Registers - Low (ClearSrcTran_LO)—Offset 348h

Refer to the description for register ClearTfr_HI.

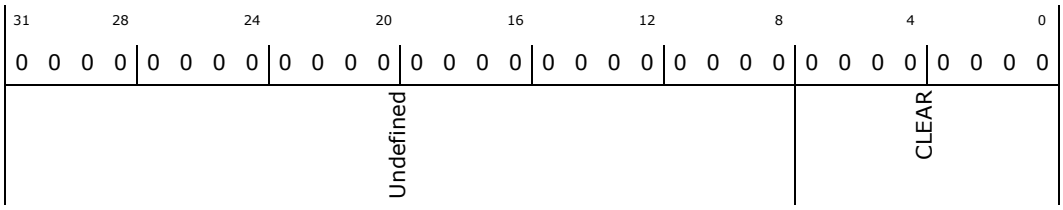
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearSrcTran_LO: [BAR] + 348h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

3.27.212 Interrupt Clear RegistersClearSrc - High (ClearSrcTran_HI)—Offset 34Ch

Refer to the description for register ClearTfr_HI.

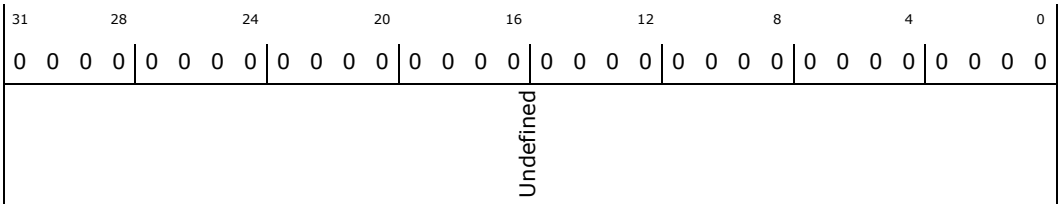
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearSrcTran_HI: [BAR] + 34Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.213 Interrupt Clear Registers - Low (ClearDstTran_LO)—Offset 350h

Refer to the description for register ClearTfr_HI.

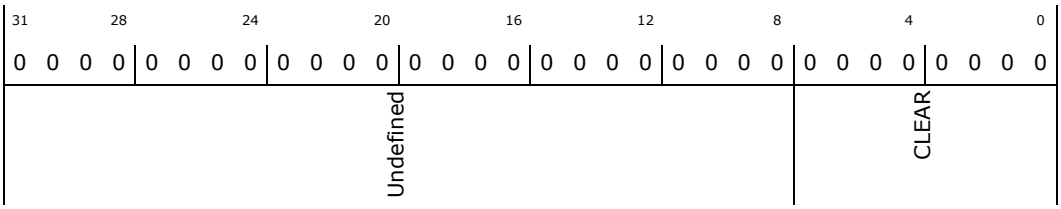
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearDstTran_LO: [BAR] + 350h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

3.27.214 Interrupt Clear Registers - High (ClearDstTran_HI)—Offset 354h

Refer to the description for register ClearTfr_HI.

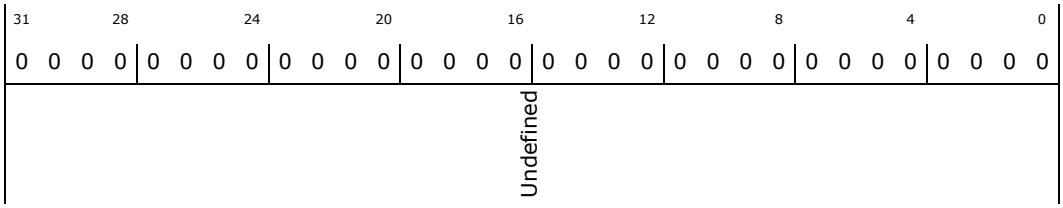
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearDstTran_HI: [BAR] + 354h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.215 Interrupt Clear Registers - Low (ClearErr_LO)—Offset 358h

Refer to the description for register ClearTfr_HI.

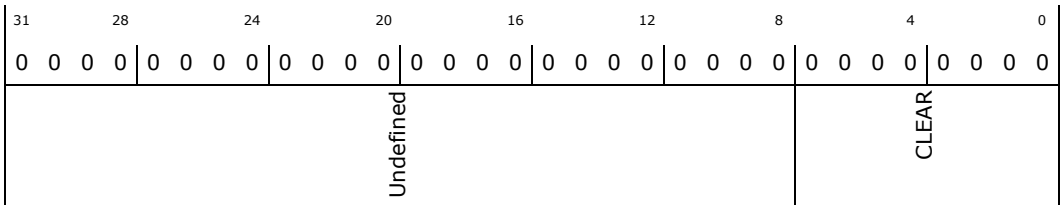
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearErr_LO: [BAR] + 358h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

3.27.216 Interrupt Clear Registers - High (ClearErr_HI)—Offset 35Ch

Refer to the description for register ClearTfr_HI.

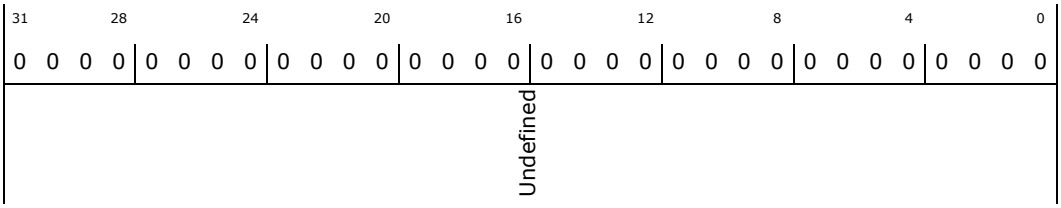
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearErr_HI: [BAR] + 35Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.217 Combined Interrupt Status Register - Low (StatusInt_LO)—Offset 360h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

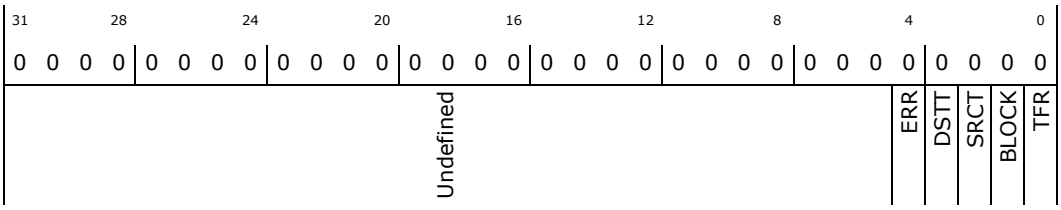
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusInt_LO: [BAR] + 360h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Description
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register.
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

3.27.218 Combined Interrupt Status Register - High (StatusInt_HI)—Offset 364h

Refer to the description for register StatusInt_LO.

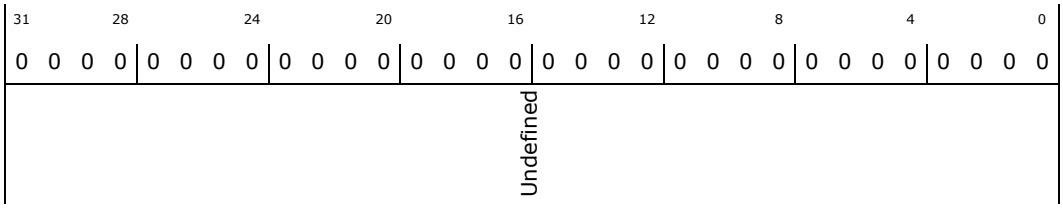
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusInt_HI: [BAR] + 364h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.219 Source Software Transaction Request Register - Low (ReqSrcReg_LO)—Offset 368h

A bit is assigned for each channel in this register. ReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

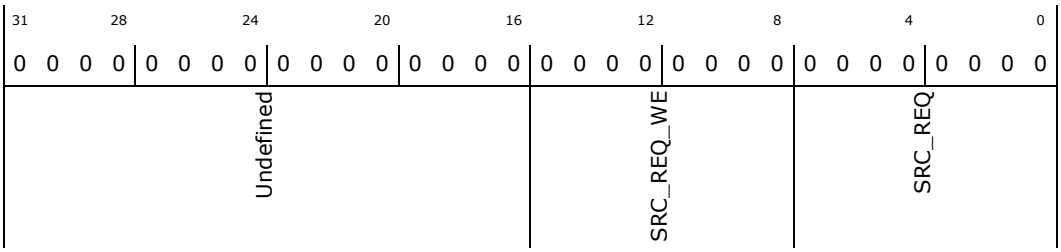
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ReqSrcReg_LO: [BAR] + 368h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Source Req Write Enable (SRC_REQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Source Request (SRC_REQ):** A channel SRC_REQ bit is written only if the corresponding channel write enable bit in the SRC_REQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register. For an example and further details, refer to the DesignWare DW_ahb_dmac Databook.

3.27.220 Source Software Transaction Request Register - High (ReqSrcReg_HI)—Offset 36Ch

A bit is assigned for each channel in this register. ReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

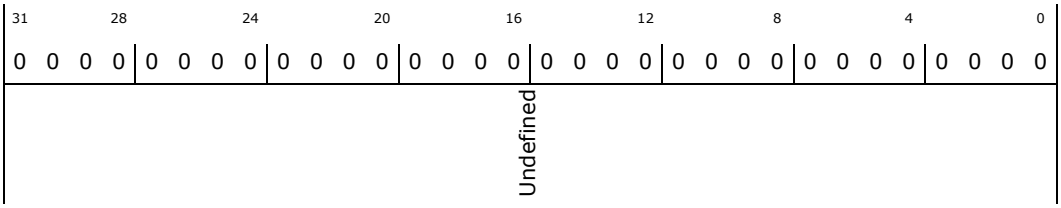
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ReqSrcReg_HI: [BAR] + 36Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.221 Destination Software Transaction Request Register - Low (ReqDstReg_LO)—Offset 370h

A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

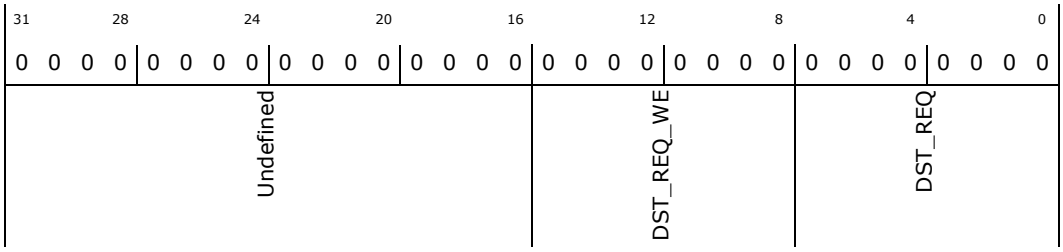
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ReqDstReg_LO: [BAR] + 370h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Destination Request Write Enable (DST_REQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Request (DST_REQ):** A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

3.27.222 Destination Software Transaction Request Register - High (ReqDstReg_HI)—Offset 374h

A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

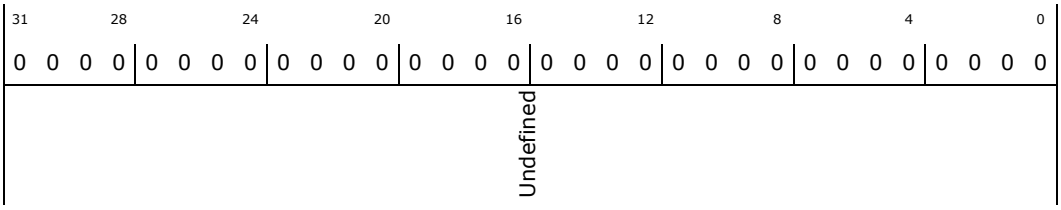
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ReqDstReg_HI: [BAR] + 374h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.223 Single Source Software Transaction Request Register - Low (SglRqSrcReg_LO)—Offset 378h

A bit is assigned for each channel in this register. SglReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

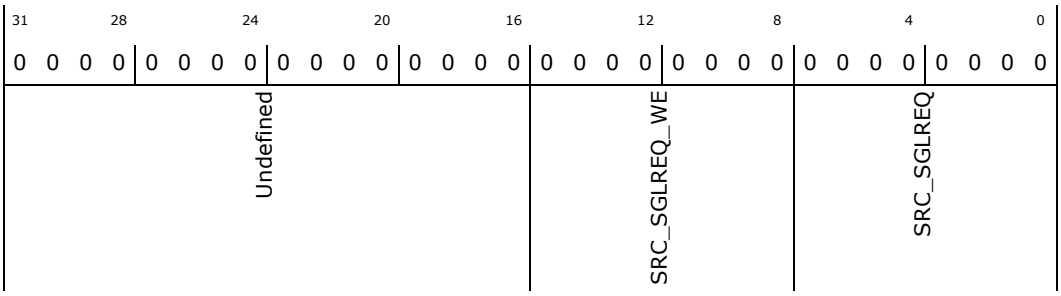
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SglRqSrcReg_LO: [BAR] + 378h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Source Req Write Enable (SRC_SGLREQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Source Single Request (SRC_SGLREQ):** A channel SRC_SGLREQ bit is written only if the corresponding channel write enable bit in the SRC_SGLREQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

3.27.224 Single Source Software Transaction Request Register - High (SglRqSrcReg_HI)—Offset 37Ch

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

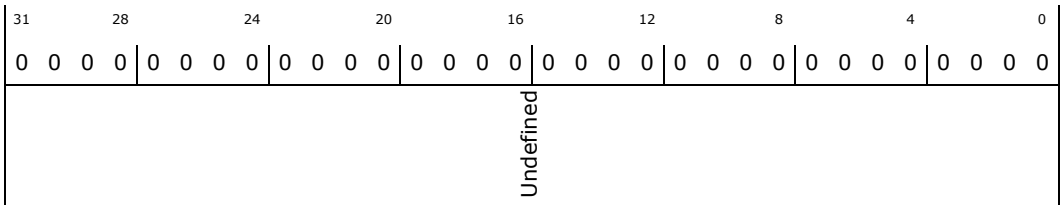
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SglRqSrcReg_HI: [BAR] + 37Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.225 Single Destination Software Transaction Request Register - Low (SglRqDstReg_LO)—Offset 380h

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

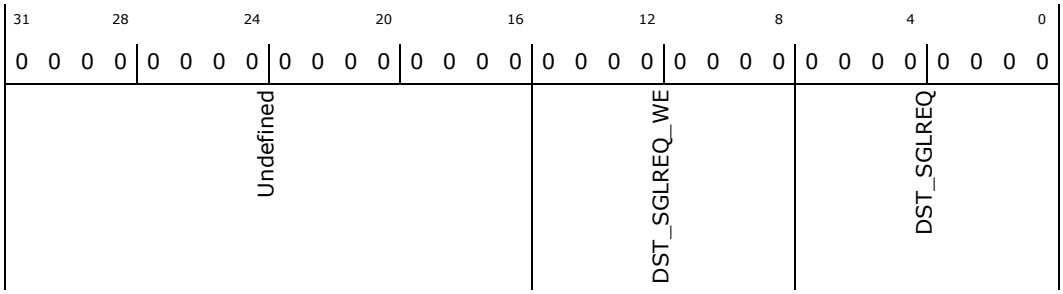
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SglRqDstReg_LO: [BAR] + 380h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Destination Request Write Enable (DST_SGLREQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Single or Burst Request (DST_SGLREQ):** A channel DST_SGLREQ bit is written only if the corresponding channel write enable bit in the DST_SGLREQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

3.27.226 Single Destination Software Transaction Request Register - High (SglRqDstReg_HI)—Offset 384h

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

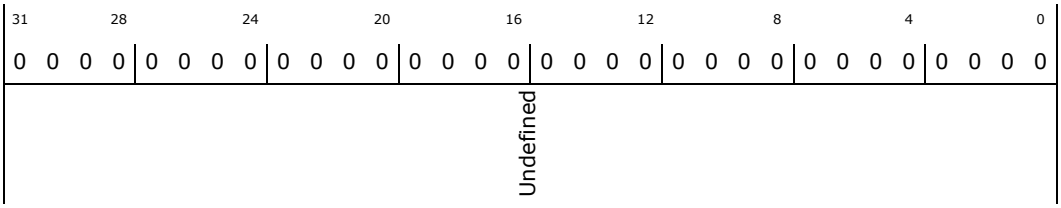
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SglRqDstReg_HI: [BAR] + 384h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.227 Last Source Transaction Request Register - Low (LstSrcReg_LO)—Offset 388h

A bit is assigned for each channel in this register. LstSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n, or when the source of channel n is not a flow controller.

A channel LSTSRC bit is written only if the corresponding channel write enable bit in the LSTSRC_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

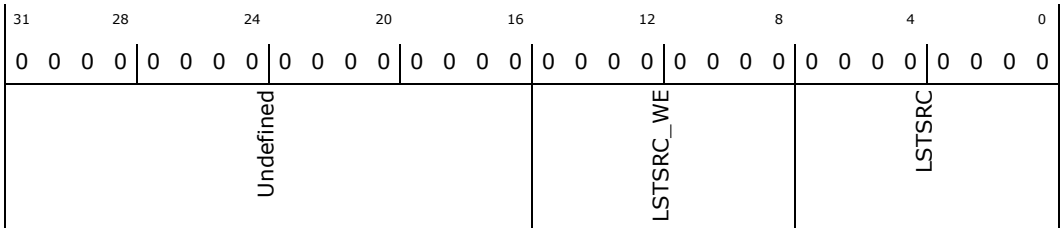
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LstSrcReg_LO: [BAR] + 388h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Last Source Transaction Request Write Enable (LSTSRC_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Last Source Transaction Request (LSTSRC):** • 0 = Not last transaction in current block • 1 = Last transaction in current block

3.27.228 Last Source Transaction Request Register - High (LstSrcReg_HI)—Offset 38Ch

Refer to description for Last Source Transaction Request Register - Low.

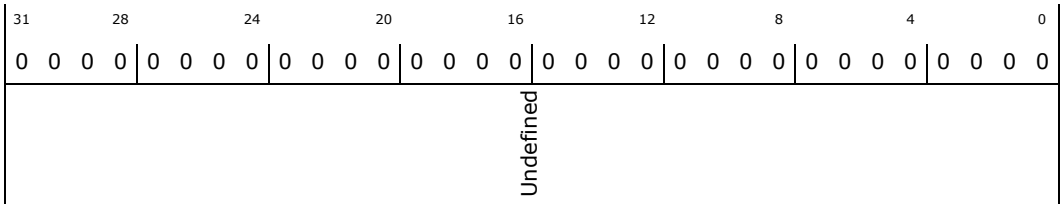
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LstSrcReg_HI: [BAR] + 38Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.229 Last Destination Transaction Request Register - Low (LstDstReg_LO)—Offset 390h

A bit is assigned for each channel in this register. LstDstReg[n] is ignored when software handshaking is not enabled for the destination of channel n or when the destination of channel n is not a flow controller.

A channel LSTDST bit is written only if the corresponding channel write enable bit in the LSTDST_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

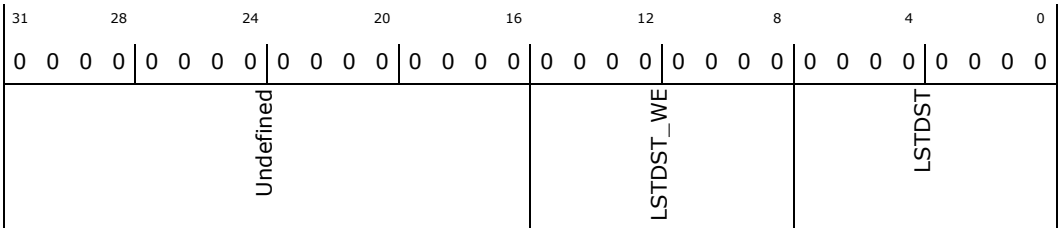
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LstDstReg_LO: [BAR] + 390h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Last Destination Transaction Request Write Enable (LSTDST_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Last Transaction Request (LSTDST):** • 0 = Not last transaction in current block • 1 = Last transaction in current block

3.27.230 Last Destination Transaction Request Register - High (LstDstReg_HI)—Offset 394h

Refer to description for Last Destination Transaction Request Register - Low.

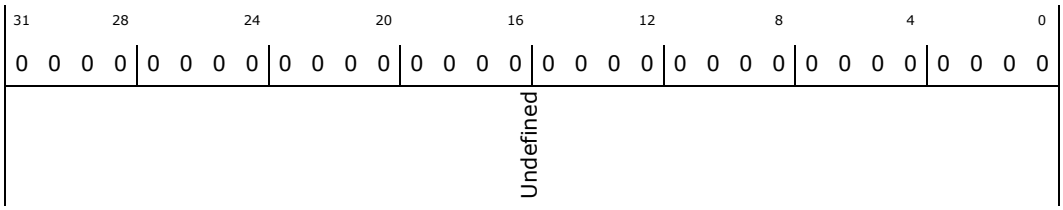
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LstDstReg_HI: [BAR] + 394h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.231 DW_ahb_dmac Configuration Register - Low (DmaCfgReg_LO)—Offset 398h

This register is used to enable the DW_ahb_dmac, which must be done before any channel activity can begin.

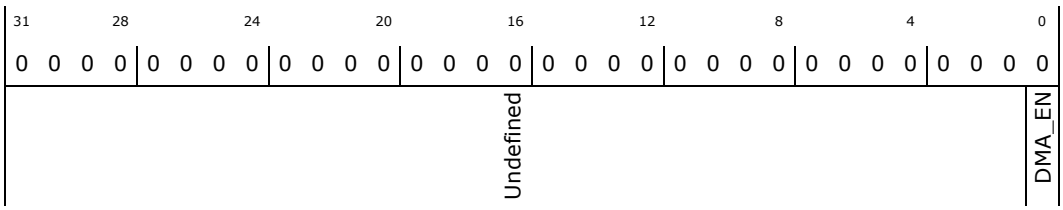
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaCfgReg_LO: [BAR] + 398h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**Undefined:** Reserved.
0	0h RW	**DW_ahb_dmac Enable Bit (DMA_EN):** • 0 = DW_ahb_dmac Disabled • 1 = DW_ahb_dmac Enabled

3.27.232 DW_ahb_dmac Configuration Register - High (DmaCfgReg_HI)—Offset 39Ch

Refer to description for DW_ahb_dmac Configuration Register - Low.

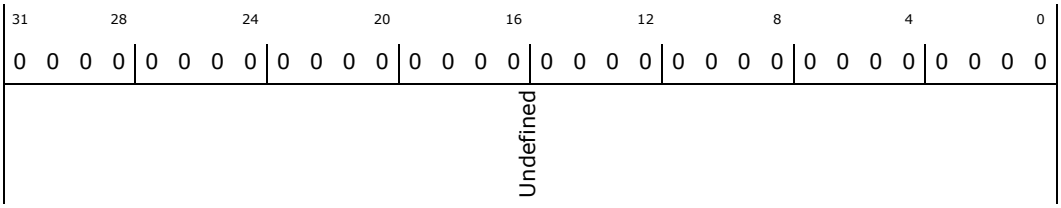
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaCfgReg_HI: [BAR] + 39Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.233 DW_ahb_dmac Channel Enable Register - Low (ChEnReg_LO)—Offset 3A0h

This is the DW_ahb_dmac Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive; it can then enable an inactive channel with the required priority.

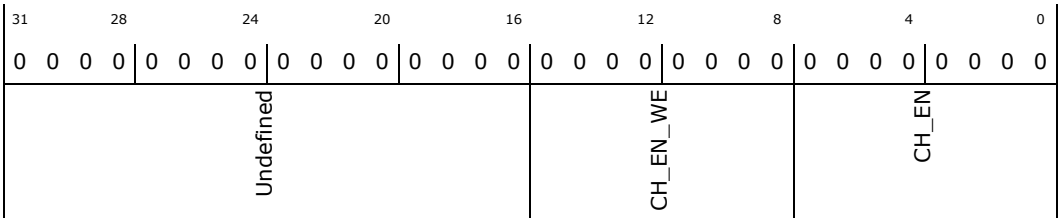
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ChEnReg_LO: [BAR] + 3A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Channel Enable Write Enable (CH_EN_WE):** The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE (this bit), is asserted on the same AHB write transfer.

Bit Range	Default & Access	Description
7:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel; clearing this bit disables the channel. • 0 = Disable the Channel • 1 = Enable the Channel

3.27.234 DW_ahb_dmac Channel Enable Register - High (ChEnReg_HI)—Offset 3A4h

Refer to the description for DW_ahb_dmac Channel Enable Register - Low.

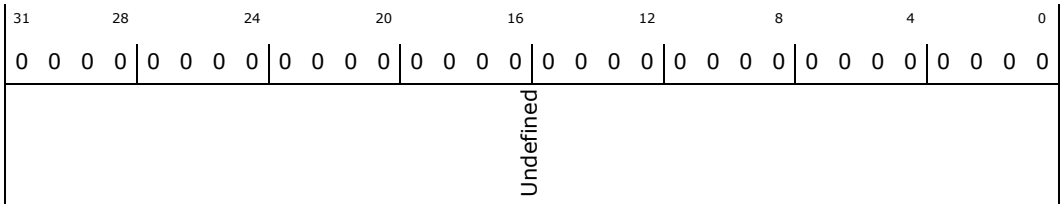
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ChEnReg_HI: [BAR] + 3A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.235 DW_ahb_dmac ID Register - Low (DmaIdReg_LO)—Offset 3A8h

This is a read-only register that reads back the coreConsultant-configured hardcoded ID number, DMAH_ID_NUM.

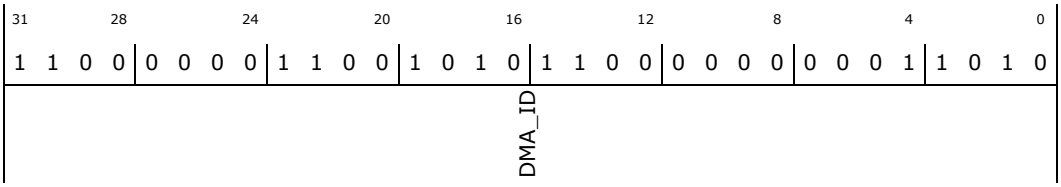
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaIdReg_LO: [BAR] + 3A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: C0CAC01Ah



Bit Range	Default & Access	Description
31:0	c0cac01ah RO	**Hardcoded DW_ahb_dmac Peripheral ID (DMA_ID):** coreConsultantconfigured hardcoded ID number DMAH_ID_NUM.

3.27.236 DW_ahb_dmac ID Register - High (DmaIdReg_HI)—Offset 3ACh

Refer to the description of DW_ahb_dmac ID Register - Low.

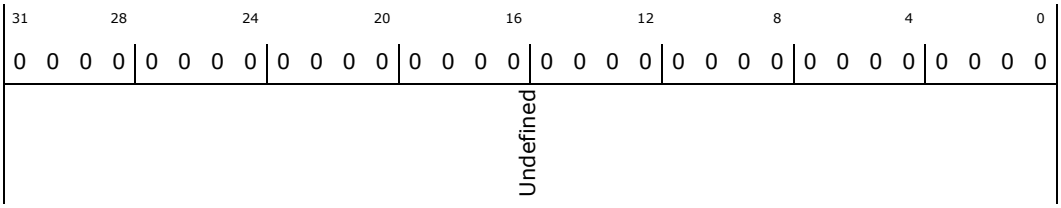
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaIdReg_HI: [BAR] + 3ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.237 DW_ahb_dmac Test Register - Low (DmaTestReg_LO)—Offset 3B0h

This register is used to put the AHB slave interface into test mode, during which the readback value of the writable registers match the value written, assuming the DW_ahb_dmac configuration has not optimized the same registers. In normal operation, the readback value of some registers is a function of the DW_ahb_dmac state, and does not match the value written.

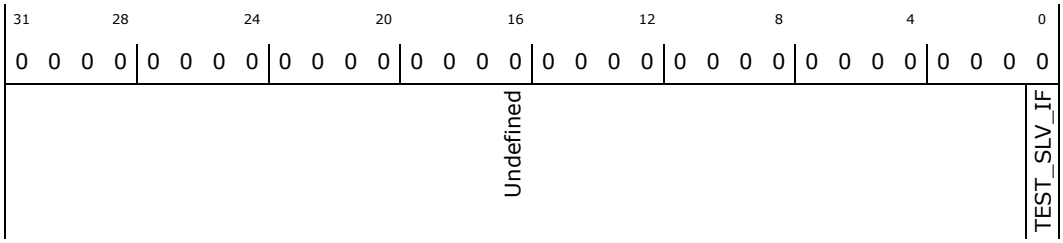
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaTestReg_LO: [BAR] + 3B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**Undefined:** Reserved.
0	0h RW	**TEST_SLV_IF:** Puts the AHB slave interface into test mode. In this mode, the readback value of the writable registers always matches the value written. This bit does not allow writing to read-only registers. • 0 = Normal mode • 1 = Test mode

3.27.238 DW_ahb_dmac Test Register - High (DmaTestReg_HI)—Offset 3B4h

Refer to the description of DW_ahb_dmac Test Register - Low.

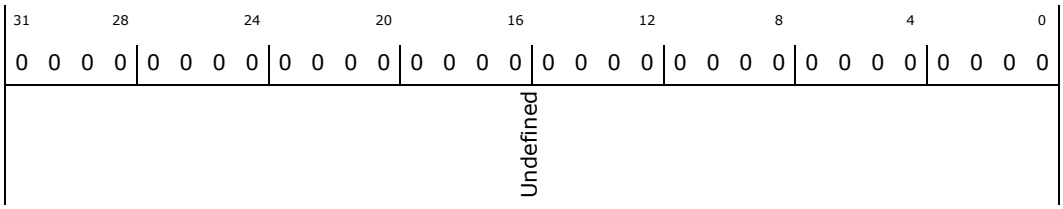
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaTestReg_HI: [BAR] + 3B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.239 DW_ahb_dmac Component Parameters Register 6 - Low (DMA_COMP_PARAMS_6_LO)—Offset 3C8h

Refer to the description for DW_ahb_dmac Component Parameters Register 6 - High.

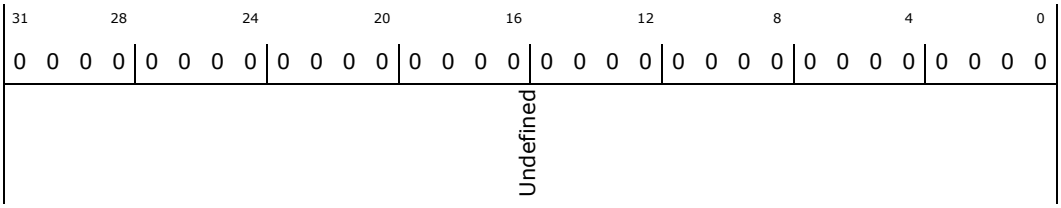
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_6_LO: [BAR] + 3C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.27.240 DW_ahb_dmac Component Parameters Register 6 - High (DMA_COMP_PARAMS_6_HI)—Offset 3CCh

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 7. The reset value depends on coreConsultant parameter(s).

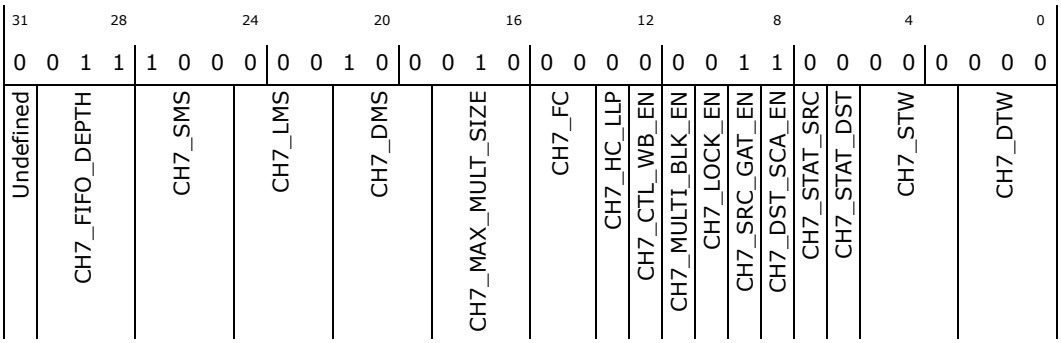
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_6_HI: [BAR] + 3CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH7_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH7_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH7_SMS:** The value of this register is derived from the DMAH_CH7_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH7_LMS:** The value of this register is derived from the DMAH_CH7_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH7_DMS:** The value of this register is derived from the DMAH_CH7_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH7_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH7_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH7_FC:** The value of this register is derived from the DMAH_CH7_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY

Bit Range	Default & Access	Description
13	0h RO	**CH7_HC_LLP:** The value of this register is derived from the DMAH_CH7_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH7_CTL_WB_EN:** The value of this register is derived from the DMAH_CH7_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH7_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH7_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH7_LOCK_EN:** The value of this register is derived from the DMAH_CH7_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH7_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH7_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH7_DST_SCA_EN:** The value of this register is derived from the DMAH_CH7_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH7_STAT_SRC:** The value of this register is derived from the DMAH_CH7_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH7_STAT_DST:** The value of this register is derived from the DMAH_CH7_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH7_STW:** The value of this register is derived from the DMAH_CH7_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

Bit Range	Default & Access	Description
2:0	0h RO	**CH7_DTW:** The value of this register is derived from the DMAH_CH7_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.27.241 DW_ahb_dmac Component Parameters Register 5 - Low (DMA_COMP_PARAMS_5_LO)—Offset 3D0h

Refer to the description for DW_ahb_dmac Component Parameters Register 5 - High.

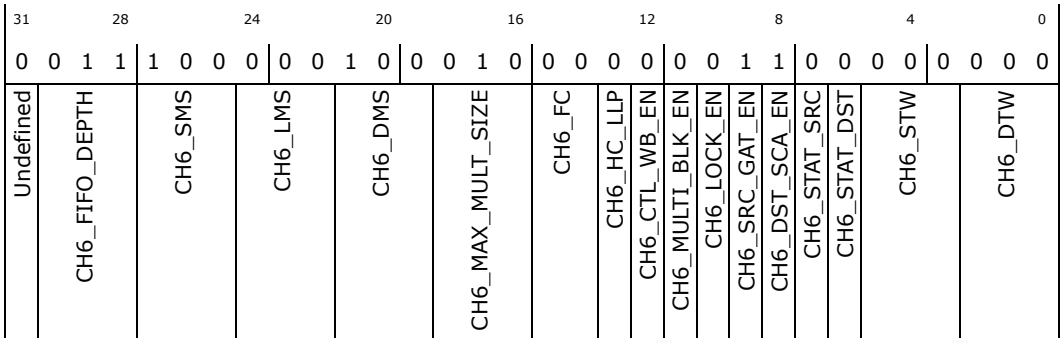
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_5_LO: [BAR] + 3D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH6_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH6_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128

Bit Range	Default & Access	Description
27:25	4h RO	**CH6_SMS:** The value of this register is derived from the DMAH_CH6_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH6_LMS:** The value of this register is derived from the DMAH_CH6_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH6_DMS:** The value of this register is derived from the DMAH_CH6_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH6_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH6_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH6_FC:** The value of this register is derived from the DMAH_CH6_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH6_HC_LLP:** The value of this register is derived from the DMAH_CH6_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH6_CTL_WB_EN:** The value of this register is derived from the DMAH_CH6_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
11	0h RO	**CH6_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH6_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH6_LOCK_EN:** The value of this register is derived from the DMAH_CH6_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH6_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH6_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH6_DST_SCA_EN:** The value of this register is derived from the DMAH_CH6_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH6_STAT_SRC:** The value of this register is derived from the DMAH_CH6_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH6_STAT_DST:** The value of this register is derived from the DMAH_CH6_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH6_STW:** The value of this register is derived from the DMAH_CH6_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH6_DTW:** The value of this register is derived from the DMAH_CH6_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.27.242 DW_ahb_dmac Component Parameters Register 5 - High (DMA_COMP_PARAMS_5_HI)—Offset 3D4h

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 5 and Channel 6. The reset value depends on coreConsultant parameter(s).

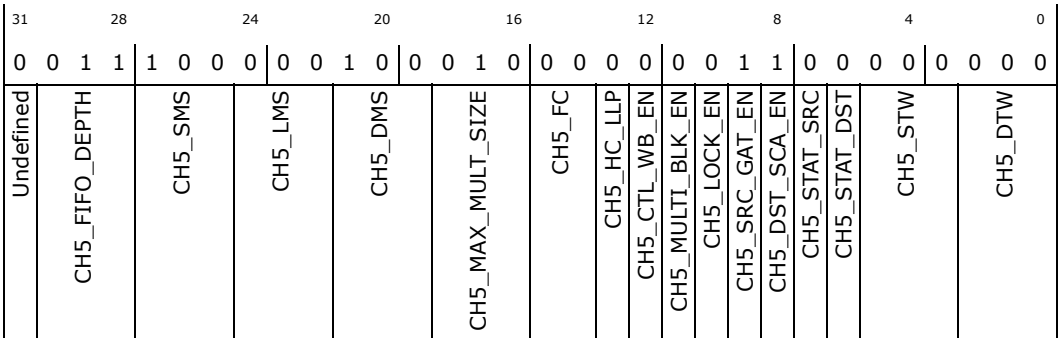
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_5_HI: [BAR] + 3D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH5_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH5_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH5_SMS:** The value of this register is derived from the DMAH_CH5_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH5_LMS:** The value of this register is derived from the DMAH_CH5_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
21:19	4h RO	**CH5_DMS:** The value of this register is derived from the DMAH_CH5_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH5_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH5_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH5_FC:** The value of this register is derived from the DMAH_CH5_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH5_HC_LLP:** The value of this register is derived from the DMAH_CH5_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH5_CTL_WB_EN:** The value of this register is derived from the DMAH_CH5_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH5_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH5_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH5_LOCK_EN:** The value of this register is derived from the DMAH_CH5_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH5_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH5_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
8	1h RO	**CH5_DST_SCA_EN:** The value of this register is derived from the DMAH_CH5_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH5_STAT_SRC:** The value of this register is derived from the DMAH_CH5_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH5_STAT_DST:** The value of this register is derived from the DMAH_CH5_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH5_STW:** The value of this register is derived from the DMAH_CH5_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH5_DTW:** The value of this register is derived from the DMAH_CH5_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.27.243 DW_ahb_dmac Component Parameters Register 4 - Low (DMA_COMP_PARAMS_4_LO)—Offset 3D8h

Refer to the description for DW_ahb_dmac Component Parameters Register 4 - High.

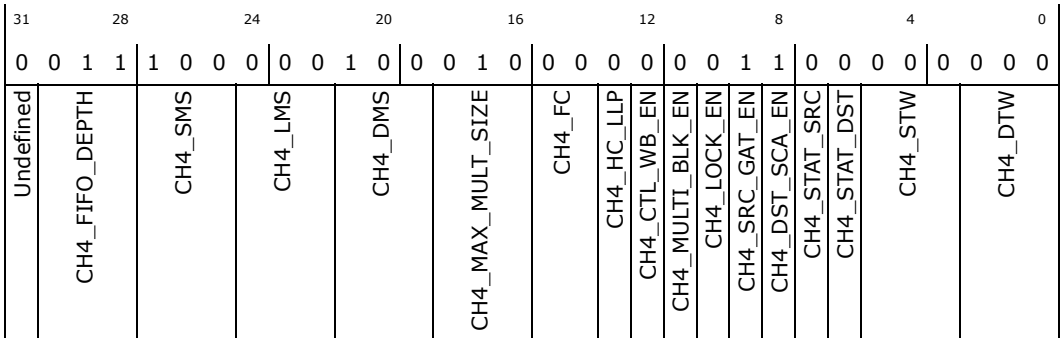
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_4_LO: [BAR] + 3D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH4_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH4_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH4_SMS:** The value of this register is derived from the DMAH_CH4_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH4_LMS:** The value of this register is derived from the DMAH_CH4_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH4_DMS:** The value of this register is derived from the DMAH_CH4_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
18:16	2h RO	**CH4_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH4_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH4_FC:** The value of this register is derived from the DMAH_CH4_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH4_HC_LLP:** The value of this register is derived from the DMAH_CH4_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH4_CTL_WB_EN:** The value of this register is derived from the DMAH_CH4_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH4_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH4_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH4_LOCK_EN:** The value of this register is derived from the DMAH_CH4_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH4_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH4_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH4_DST_SCA_EN:** The value of this register is derived from the DMAH_CH4_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
7	0h RO	**CH4_STAT_SRC:** The value of this register is derived from the DMAH_CH4_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH4_STAT_DST:** The value of this register is derived from the DMAH_CH4_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH4_STW:** The value of this register is derived from the DMAH_CH4_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH4_DTW:** The value of this register is derived from the DMAH_CH4_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.27.244 DW_ahb_dmac Component Parameters Register 4 - High (DMA_COMP_PARAMS_4_HI)—Offset 3DCh

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 3 and Channel 4. The reset value depends on coreConsultant parameter(s).

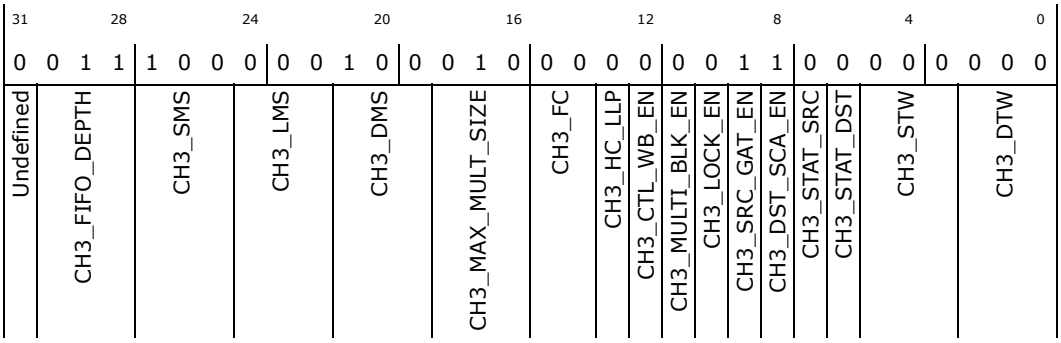
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_4_HI: [BAR] + 3DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH3_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH3_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH3_SMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH3_LMS:** The value of this register is derived from the DMAH_CH3_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH3_DMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
18:16	2h RO	**CH3_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH3_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH3_FC:** The value of this register is derived from the DMAH_CH3_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH3_HC_LLP:** The value of this register is derived from the DMAH_CH3_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH3_CTL_WB_EN:** The value of this register is derived from the DMAH_CH3_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH3_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH3_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH3_LOCK_EN:** The value of this register is derived from the DMAH_CH3_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH3_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH3_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH3_DST_SCA_EN:** The value of this register is derived from the DMAH_CH3_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
7	0h RO	**CH3_STAT_SRC:** he value of this register is derived from the DMAH_CH3_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH3_STAT_DST:** The value of this register is derived from the DMAH_CH3_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH3_STW:** The value of this register is derived from the DMAH_CH3_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH3_DTW:** The value of this register is derived from the DMAH_CH3_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.27.245 DW_ahb_dmac Component Parameters Register 3 - Low (DMA_COMP_PARAMS_3_LO)—Offset 3E0h

Refer to the description for DW_ahb_dmac Component Parameters Register 3 - High.

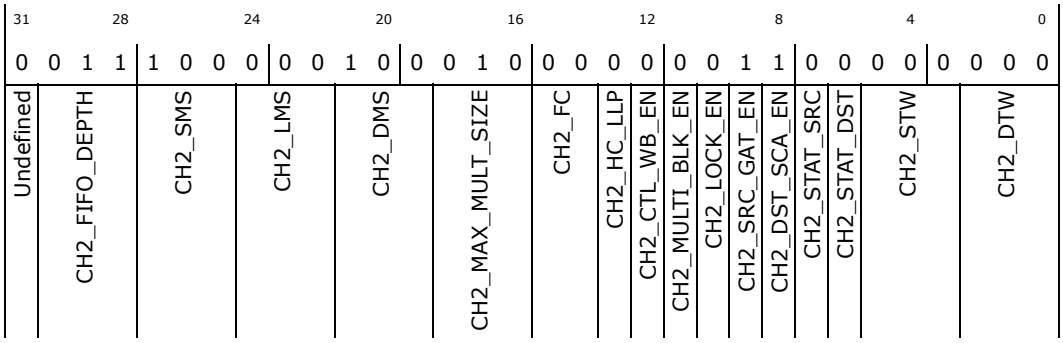
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_3_LO: [BAR] + 3E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH2_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH2_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH2_SMS:** The value of this register is derived from the DMAH_CH2_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH2_LMS:** The value of this register is derived from the DMAH_CH2_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH2_DMS:** The value of this register is derived from the DMAH_CH2_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
18:16	2h RO	**CH2_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH2_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH2_FC:** The value of this register is derived from the DMAH_CH2_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH2_HC_LLP:** The value of this register is derived from the DMAH_CH2_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH2_CTL_WB_EN:** The value of this register is derived from the DMAH_CH2_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH2_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH2_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to the spec. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH2_LOCK_EN:** The value of this register is derived from the DMAH_CH2_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH2_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH2_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH2_DST_SCA_EN:** The value of this register is derived from the DMAH_CH2_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
7	0h RO	**CH2_STAT_SRC:** The value of this register is derived from the DMAH_CH2_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH2_STAT_DST:** The value of this register is derived from the DMAH_CH2_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH2_STW:** The value of this register is derived from the DMAH_CH2_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH2_DTW:** The value of this register is derived from the DMAH_CH2_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.27.246 DW_ahb_dmac Component Parameters Register 3 - High (DMA_COMP_PARAMS_3_HI)—Offset 3E4h

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 1 and Channel 2. The reset value depends on coreConsultant parameter(s).

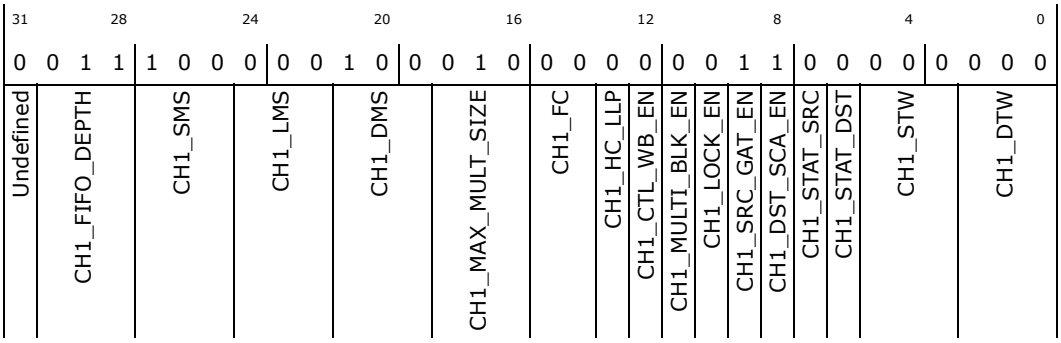
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_3_HI: [BAR] + 3E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH1_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH1_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH1_SMS:** The value of this register is derived from the DMAH_CH1_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH1_LMS:** The value of this register is derived from the DMAH_CH1_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH1_DMS:** The value of this register is derived from the DMAH_CH1_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
18:16	2h RO	**CH1_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH1_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH1_FC:** The value of this register is derived from the DMAH_CH1_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH1_HC_LLP:** The value of this register is derived from the DMAH_CH1_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH1_CTL_WB_EN:** The value of this register is derived from the DMAH_CH1_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH1_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH1_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH1_LOCK_EN:** The value of this register is derived from the DMAH_CH1_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH1_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH1_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH1_DST_SCA_EN:** The value of this register is derived from the DMAH_CH1_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
7	0h RO	**CH1_STAT_SRC:** The value of this register is derived from the DMAH_CH1_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH1_STAT_DST:** The value of this register is derived from the DMAH_CH1_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH1_STW:** The value of this register is derived from the DMAH_CH1_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH1_DTW:** The value of this register is derived from the DMAH_CH1_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.27.247 DW_ahb_dmac Component Parameters Register 2 - Low (DMA_COMP_PARAMS_2_LO)—Offset 3E8h

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

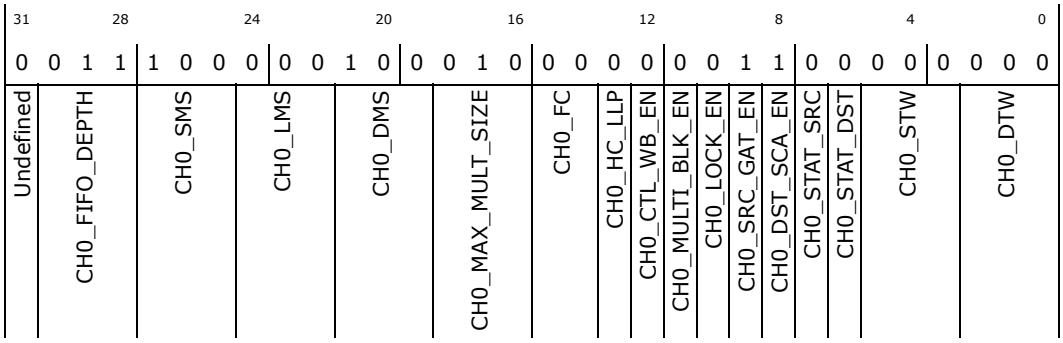
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_2_LO: [BAR] + 3E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH0_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH0_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH0_SMS:** The value of this register is derived from the DMAH_CH0_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH0_LMS:** The value of this register is derived from the DMAH_CH0_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH0_DMS:** The value of this register is derived from the DMAH_CH0_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
18:16	2h RO	**CH0_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH0_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH0_FC:** The value of this register is derived from the DMAH_CH0_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH0_HC_LLP:** The value of this register is derived from the DMAH_CH0_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH0_CTL_WB_EN:** The value of this register is derived from the DMAH_CH0_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH0_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH0_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH0_LOCK_EN:** The value of this register is derived from the DMAH_CH0_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH0_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH0_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH0_DST_SCA_EN:** The value of this register is derived from the DMAH_CH0_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
7	0h RO	**CH0_STAT_SRC:** The value of this register is derived from the DMAH_CH0_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH0_STAT_DST:** The value of this register is derived from the DMAH_CH0_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH0_STW:** Refer to the description for bit field DMA_COMP_PARAMS_2_LO.CH0_DTW
2:0	0h RO	**CH0_DTW:** The value of this register is derived from the DMAH_CH0_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.27.248 DW_ahb_dmac Component Parameters Register 2 - High (DMA_COMP_PARAMS_2_HI)—Offset 3ECh

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

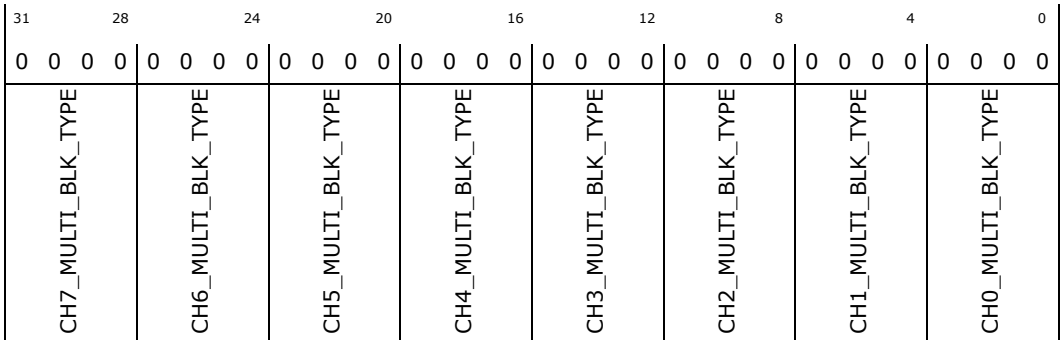
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_2_HI: [BAR] + 3ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RO	**CH7_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
27:24	0h RO	**CH6_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
23:20	0h RO	**CH5_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
19:16	0h RO	**CH4_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP

Bit Range	Default & Access	Description
15:12	0h RO	**CH3_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
11:8	0h RO	**CH2_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
7:4	0h RO	**CH1_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
3:0	0h RO	**CH0_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP

3.27.249 DW_ahb_dmac Component Parameters Register 1 - Low (DMA_COMP_PARAMS_1_LO)—Offset 3F0h

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

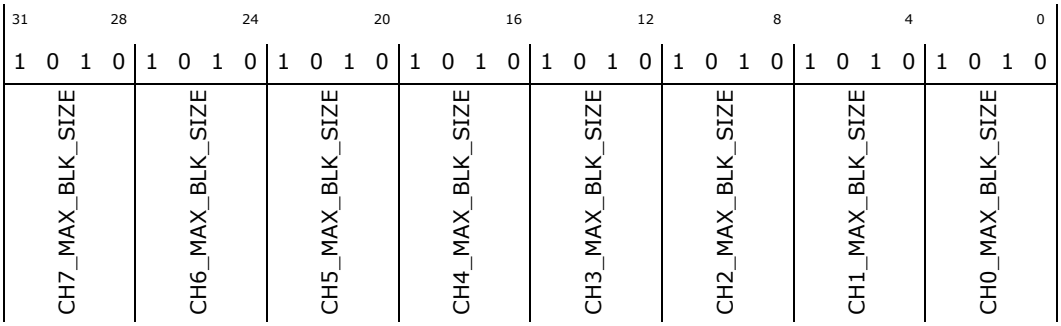
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_1_LO: [BAR] + 3F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: AAAAAAAAh



Bit Range	Default & Access	Description
31:28	ah RO	**CH7_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. • 0h = 3 • 1h = 7 • 2h = 15 • 3h = 31 • 4h = 63 • 5h = 127 • 6h = 255 • 7h = 511 • 8h = 1023 • 9h = 2047 • Ah = 4095
27:24	ah RO	**CH6_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
23:20	ah RO	**CH5_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
19:16	ah RO	**CH4_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
15:12	ah RO	**CH3_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
11:8	ah RO	**CH2_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
7:4	ah RO	**CH1_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
3:0	ah RO	**CH0_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.

3.27.250 DW_ahb_dmac Component Parameters Register 1 - High (DMA_COMP_PARAMS_1_HI)—Offset 3F4h

Refer to the description for DW_ahb_dmac Component Parameters Register 1 - Low.

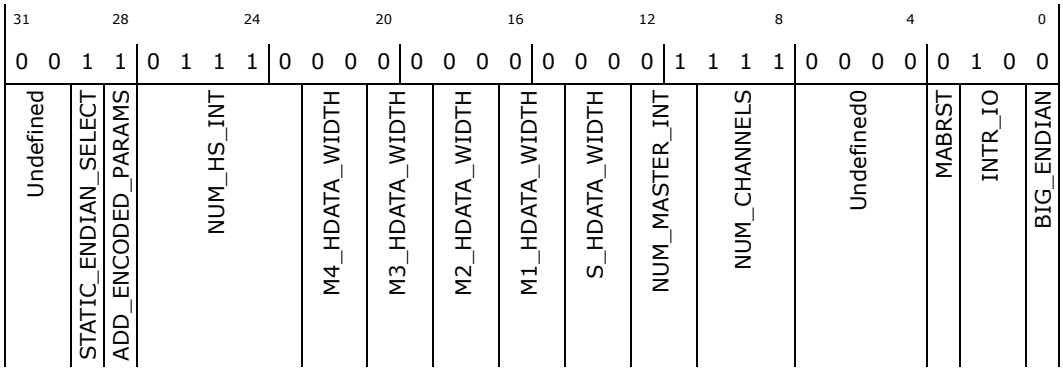
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_1_HI: [BAR] + 3F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 37000F04h



Bit Range	Default & Access	Description
31:30	0h RW	**Undefined:** Reserved.
29	1h RO	**STATIC_ENDIAN_SELECT:** The value of this register is derived from the DMAH_STATIC_ENDIAN_SELECT coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE
28	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the DMAH_ADD_ENCODED_PARAMS coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE
27:23	0eh RO	**NUM_HS_INT:** The value of this register is derived from the DMAH_NUM_HS_INT coreConsultant parameter. For a description of this parameter, refer to page 102. • 0h0 = 0 • to • 1h0 = 16
22:21	0h RO	**M4_HDATA_WIDTH:** The value of this register is derived from the DMAH_M4_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits

Bit Range	Default & Access	Description
20:19	0h RO	**M3_HDATA_WIDTH:** The value of this register is derived from the DMAH_M3_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
18:17	0h RO	**M2_HDATA_WIDTH:** The value of this register is derived from the DMAH_M2_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
16:15	0h RO	**M1_HDATA_WIDTH:** The value of this register is derived from the DMAH_M1_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
14:13	0h RO	**S_HDATA_WIDTH:** The value of this register is derived from the DMAH_S_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
12:11	01h RO	**NUM_MASTER_INT:** The value of this register is derived from the DMAH_NUM_MASTER_INT coreConsultant parameter. For a description of this parameter, refer to page 102. 0h = 1 to 3h = 4
10:8	7h RO	**NUM_CHANNELS:** The value of this register is derived from the DMAH_NUM_CHANNELS coreConsultant parameter. For a description of this parameter, refer to page 102. 0h = 1 to 7h = 8
7:4	0h RW	**Undefined0:** Reserved.
3	0h RO	**MABRST:** The value of this register is derived from the DMAH_MABRST coreConsultant parameter. For a description of this parameter, refer to page 103. • 0 = FALSE • 1 = TRUE
2:1	2h RO	**INTR_IO:** The value of this register is derived from the DMAH_INTR_IO coreConsultant parameter. For a description of this parameter, refer to page 103. • 0h = ALL • 1h = TYPE • 2h = COMBINED • 3h = reserved

Bit Range	Default & Access	Description
0	0h RO	**BIG_ENDIAN:** The value of this register is derived from the DMAH_BIG_ENDIAN coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE

3.27.251 DMA Component ID RegisterDma - Low (DmaCompsID_LO)—Offset 3F8h

This is the DW_ahb_dmac Component Version register, which is a read-only register that specifies the version of the packaged component in the upper 32 bits and the component type in the lower 32 bits.

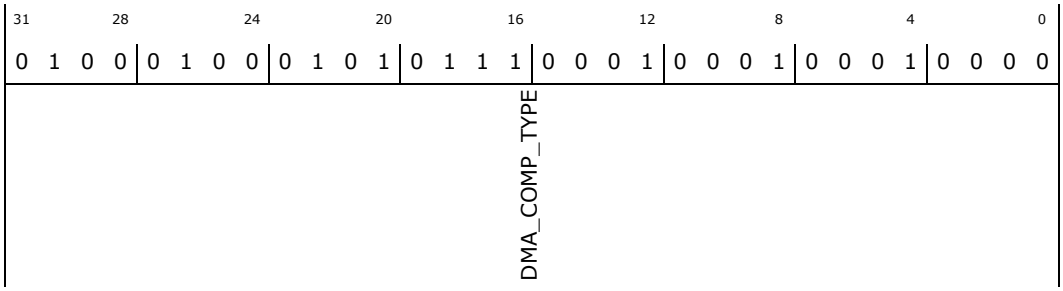
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaCompsID_LO: [BAR] + 3F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 44571110h



Bit Range	Default & Access	Description
31:0	44571110h RO	**Designware Component Type (DMA_COMP_TYPE):** Designware Component Type number = 0x44_57_11_10. This assigned unique hex value is constant and is derived from the two ASCII letters -DW- followed by a 32-bit unsigned number.

3.27.252 DMA Component ID Register - High (DmaCompsID_HI)—Offset 3FCh

This is the DW_ahb_dmac Component Version register, which is a read-only register that specifies the version of the packaged component in the upper 32 bits and the component type in the lower 32 bits.

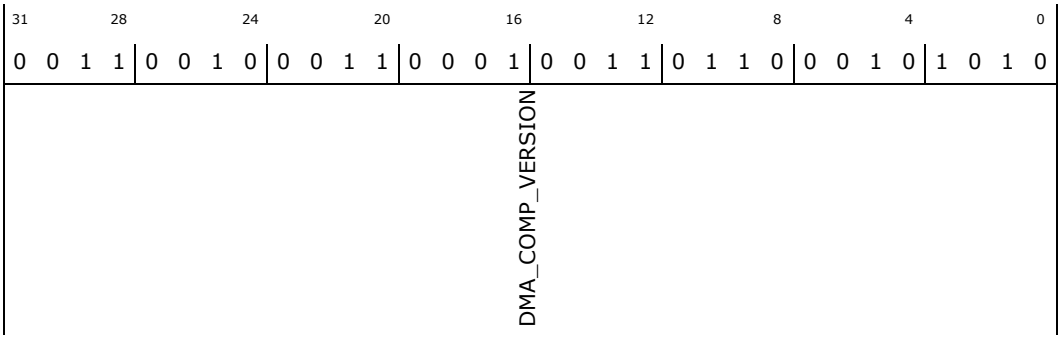
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaCompsID_HI: [BAR] + 3FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 3231362Ah



Bit Range	Default & Access	Description
31:0	3231362ah RO	**Version of the Component (DMA_COMP_VERSION):** Reserved.

3.28 SIO I²C DMA PCI Configuration Registers

Table 36. Summary of I²C DMA PCI Configuration Registers—0/24/0

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2304	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2305	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2306	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2307	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2308	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2308	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2309	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2310	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2310	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2311	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2311	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2312	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2313	00000000h

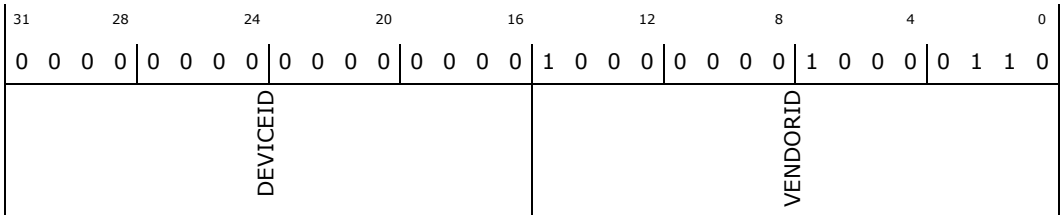
3.28.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:24, F:0] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

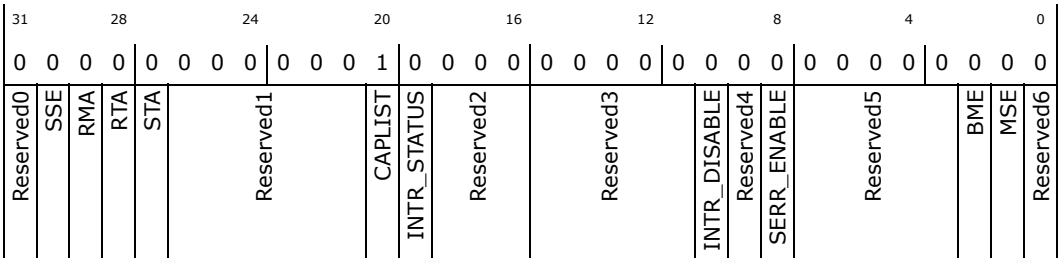
3.28.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:24, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

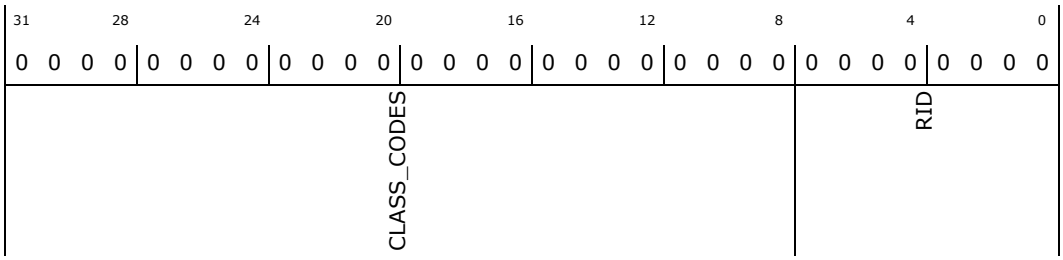
3.28.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:24, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

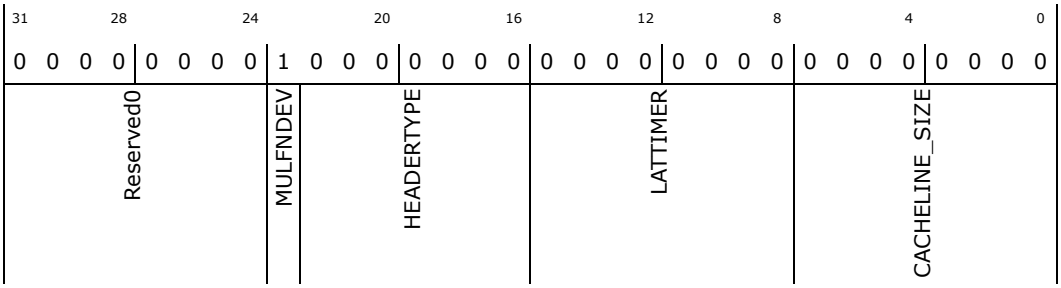
3.28.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:24, F:0] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

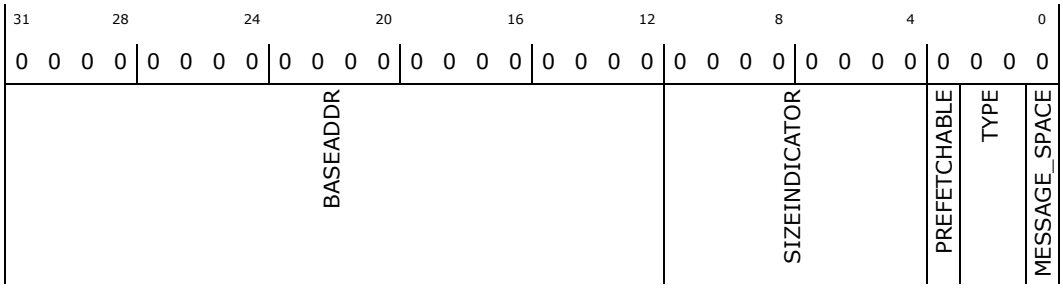
3.28.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

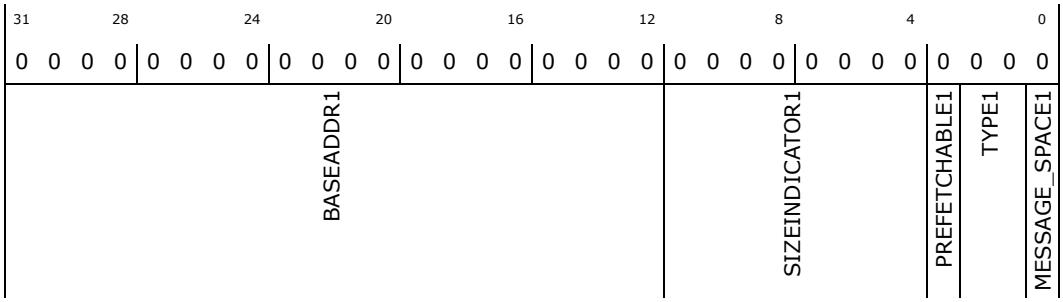
3.28.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:24, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

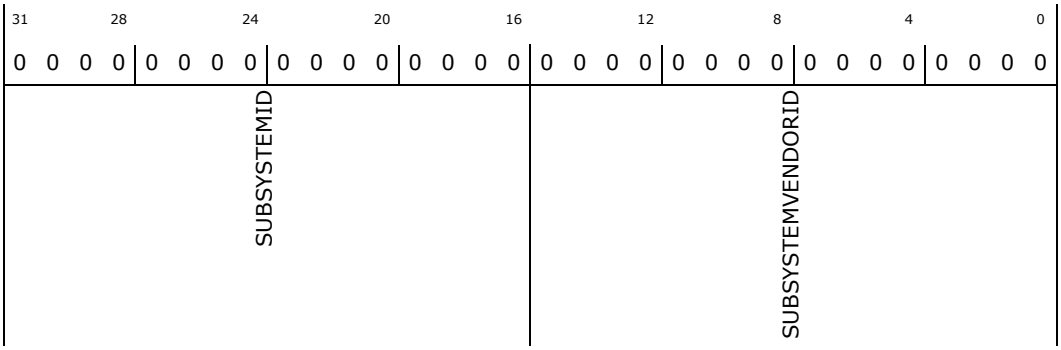
3.28.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:24, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

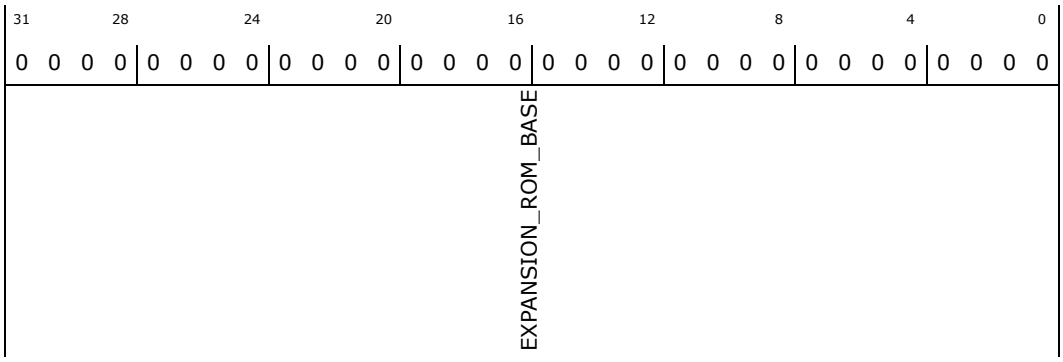
3.28.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:24, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

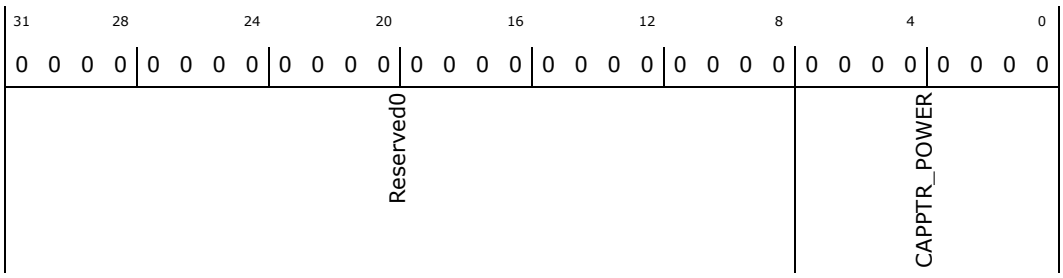
3.28.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:24, F:0] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

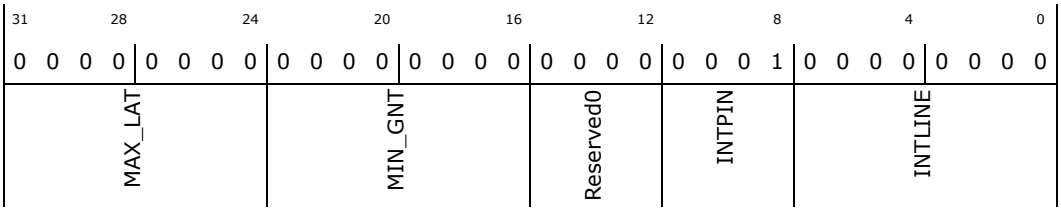
3.28.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

INTERRUPTREG: [B:0, D:24, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

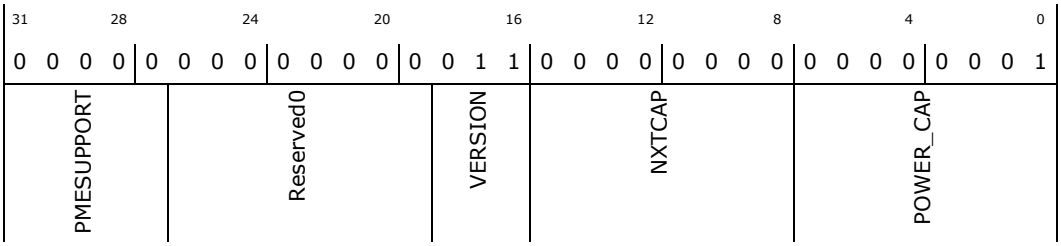
3.28.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

POWERCAPID: [B:0, D:24, F:0] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

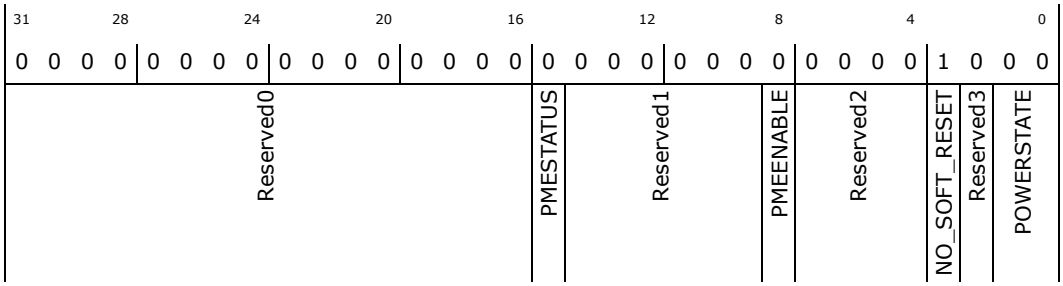
3.28.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:24, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

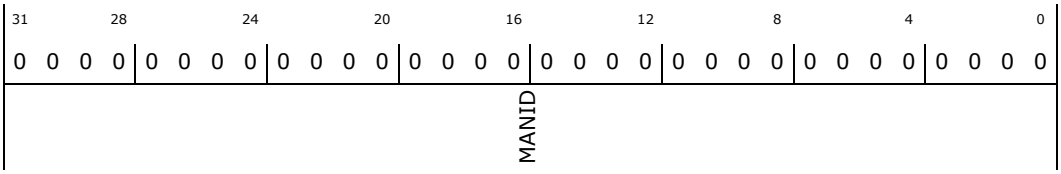
3.28.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:24, F:0] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

3.29 SIO I2C DMA Memory Mapped IO Registers

Table 37. Summary of SIO I2C DMA Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"Source Address Register for Channel 0 - Low (SAR0_LO)—Offset 0h" on page 2326	00000000h
4h	4	"Source Address Register for Channel 0 - High (SAR0_HI)—Offset 4h" on page 2326	00000000h
8h	4	"Destination Address Register for Channel 0 - Low (DAR0_LO)—Offset 8h" on page 2327	00000000h
Ch	4	"Destination Address Register for Channel 0 - High (DAR0_HI)—Offset Ch" on page 2327	00000000h
10h	4	"Linked List Pointer Register for Channel 0 - Low (LLP0_LO)—Offset 10h" on page 2328	00000000h
14h	4	"Linked List Pointer Register for Channel 0 - High (LLP0_HI)—Offset 14h" on page 2328	00000000h
18h	4	"Control Register for Channel 0 - Low (CTL0_LO)—Offset 18h" on page 2329	00304801h
1Ch	4	"Control Register for Channel 0 - High (CTL0_HI)—Offset 1Ch" on page 2331	00000002h
20h	4	"Source Status Register for Channel 0 - Low (SSTAT0_LO)—Offset 20h" on page 2331	00000000h
24h	4	"Source Status Register for Channel 0 - High (SSTAT0_HI)—Offset 24h" on page 2332	00000000h
28h	4	"Dest Status Register for Channel 0 - Low (DSTAT0_LO)—Offset 28h" on page 2332	00000000h
2Ch	4	"Dest Status Register for Channel 0 - High (DSTAT0_HI)—Offset 2Ch" on page 2333	00000000h
30h	4	"Source Status Address Register for Channel 0 - Low (SSTATAR0_LO)—Offset 30h" on page 2334	00000000h
34h	4	"Source Status Address Register for Channel 0 - High (SSTATAR0_HI)—Offset 34h" on page 2334	00000000h
38h	4	"Dest Status Address Register for Channel 0 - Low (DSTATAR0_LO)—Offset 38h" on page 2335	00000000h
3Ch	4	"Dest Status Address Register for Channel 0 - High (DSTATAR0_HI)—Offset 3Ch" on page 2335	00000000h
40h	4	"Configuration Register for Channel 0 - Low (CFG0_LO)—Offset 40h" on page 2336	00000E00h
44h	4	"Configuration Register for Channel 0 - High (CFG0_HI)—Offset 44h" on page 2337	00000004h
48h	4	"Source Gather Register for Channel 0 - Low (SGR0_LO)—Offset 48h" on page 2338	00000000h
4Ch	4	"Source Gather Register for Channel 0 - High (SGR0_HI)—Offset 4Ch" on page 2339	00000000h

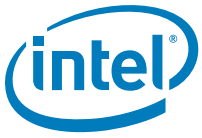


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
50h	4	"Destination Scatter Register for Channel 0 - Low (DSR0_LO)—Offset 50h" on page 2339	00000000h
54h	4	"Dest Scatter Register for Channel 0 - High (DSR0_HI)—Offset 54h" on page 2340	00000000h
58h	4	"Source Address Register for Channel 1 - Low (SAR1_LO)—Offset 58h" on page 2340	00000000h
5Ch	4	"Source Address Register for Channel 1 - High (SAR1_HI)—Offset 5Ch" on page 2341	00000000h
60h	4	"Destination Address Register for Channel 1 - Low (DAR1_LO)—Offset 60h" on page 2341	00000000h
64h	4	"Destination Address Register for Channel 1 - High (DAR1_HI)—Offset 64h" on page 2342	00000000h
68h	4	"Linked List Pointer Register for Channel 1 - Low (LLP1_LO)—Offset 68h" on page 2342	00000000h
6Ch	4	"Linked List Pointer Register for Channel 1 - High (LLP1_HI)—Offset 6Ch" on page 2343	00000000h
70h	4	"Control Register for Channel 1 - Low (CTL1_LO)—Offset 70h" on page 2343	00304801h
74h	4	"Control Register for Channel 1 - High (CTL1_HI)—Offset 74h" on page 2345	00000002h
78h	4	"Source Status Register for Channel 1 - Low (SSTAT1_LO)—Offset 78h" on page 2346	00000000h
7Ch	4	"Source Status Register for Channel 1 - High (SSTAT1_HI)—Offset 7Ch" on page 2346	00000000h
80h	4	"Dest Status Register for Channel 1 - Low (DSTAT1_LO)—Offset 80h" on page 2347	00000000h
84h	4	"Dest Status Register for Channel 1 - High (DSTAT1_HI)—Offset 84h" on page 2347	00000000h
88h	4	"Source Status Address Register for Channel 1 - Low (SSTATAR1_LO)—Offset 88h" on page 2348	00000000h
8Ch	4	"Source Status Address Register for Channel 1 - High (SSTATAR1_HI)—Offset 8Ch" on page 2348	00000000h
90h	4	"Dest Status Address Register for Channel 1 - Low (DSTATAR1_LO)—Offset 90h" on page 2349	00000000h
94h	4	"Dest Status Address Register for Channel 1 - High (DSTATAR1_HI)—Offset 94h" on page 2349	00000000h
98h	4	"Configuration Register for Channel 1 - Low (CFG1_LO)—Offset 98h" on page 2350	00000E20h
9Ch	4	"Configuration Register for Channel 1 - High (CFG1_HI)—Offset 9Ch" on page 2351	00000004h
A0h	4	"Source Gather Register for Channel 1 - Low (SGR1_LO)—Offset A0h" on page 2352	00000000h

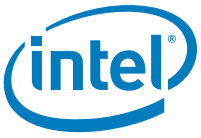


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
A4h	4	"Source Gather Register for Channel 1 - High (SGR1_HI)—Offset A4h" on page 2353	00000000h
A8h	4	"Destination Scatter Register for Channel 1 - Low (DSR1_LO)—Offset A8h" on page 2353	00000000h
ACh	4	"Dest Scatter Register for Channel 1 - High (DSR1_HI)—Offset ACh" on page 2354	00000000h
B0h	4	"Source Address Register for Channel 2 - Low (SAR2_LO)—Offset B0h" on page 2354	00000000h
B4h	4	"Source Address Register for Channel 2 - High (SAR2_HI)—Offset B4h" on page 2355	00000000h
B8h	4	"Destination Address Register for Channel 2 - Low (DAR2_LO)—Offset B8h" on page 2355	00000000h
BCh	4	"Destination Address Register for Channel 2 - High (DAR2_HI)—Offset BCh" on page 2356	00000000h
C0h	4	"Linked List Pointer Register for Channel 2 - Low (LLP2_LO)—Offset C0h" on page 2356	00000000h
C4h	4	"Linked List Pointer Register for Channel 2 - High (LLP2_HI)—Offset C4h" on page 2357	00000000h
C8h	4	"Control Register for Channel 2 - Low (CTL2_LO)—Offset C8h" on page 2357	00304801h
CCh	4	"Control Register for Channel 2 - High (CTL2_HI)—Offset CCh" on page 2359	00000002h
D0h	4	"Source Status Register for Channel 2 - Low (SSTAT2_LO)—Offset D0h" on page 2359	00000000h
D4h	4	"Source Status Register for Channel 2 - High (SSTAT2_HI)—Offset D4h" on page 2360	00000000h
D8h	4	"Dest Status Register for Channel 2 - Low (DSTAT2_LO)—Offset D8h" on page 2360	00000000h
DCh	4	"Dest Status Register for Channel 2 - High (DSTAT2_HI)—Offset DCh" on page 2361	00000000h
E0h	4	"Source Status Address Register for Channel 2 - Low (SSTATAR2_LO)—Offset E0h" on page 2361	00000000h
E4h	4	"Source Status Address Register for Channel 2 - High (SSTATAR2_HI)—Offset E4h" on page 2362	00000000h
E8h	4	"Dest Status Address Register for Channel 2 - Low (DSTATAR2_LO)—Offset E8h" on page 2362	00000000h
ECh	4	"Dest Status Address Register for Channel 2 - High (DSTATAR2_HI)—Offset ECh" on page 2363	00000000h
F0h	4	"Configuration Register for Channel 2 - Low (CFG2_LO)—Offset F0h" on page 2363	00000E40h
F4h	4	"Configuration Register for Channel 2 - High (CFG2_HI)—Offset F4h" on page 2365	00000004h

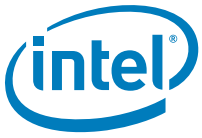


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
F8h	4	"Source Gather Register for Channel 2 - Low (SGR2_LO)—Offset F8h" on page 2366	00000000h
FCh	4	"Source Gather Register for Channel 2 - High (SGR2_HI)—Offset FCh" on page 2366	00000000h
100h	4	"Destination Scatter Register for Channel 2 - Low (DSR2_LO)—Offset 100h" on page 2367	00000000h
104h	4	"Dest Scatter Register for Channel 2 - High (DSR2_HI)—Offset 104h" on page 2367	00000000h
108h	4	"Source Address Register for Channel 3 - Low (SAR3_LO)—Offset 108h" on page 2368	00000000h
10Ch	4	"Source Address Register for Channel 3 - High (SAR3_HI)—Offset 10Ch" on page 2368	00000000h
110h	4	"Destination Address Register for Channel 3 - Low (DAR3_LO)—Offset 110h" on page 2369	00000000h
114h	4	"Destination Address Register for Channel 3 - High (DAR3_HI)—Offset 114h" on page 2369	00000000h
118h	4	"Linked List Pointer Register for Channel 3 - Low (LLP3_LO)—Offset 118h" on page 2370	00000000h
11Ch	4	"Linked List Pointer Register for Channel 3 - High (LLP3_HI)—Offset 11Ch" on page 2370	00000000h
120h	4	"Control Register for Channel 3 - Low (CTL3_LO)—Offset 120h" on page 2371	00304801h
124h	4	"Control Register for Channel 3 - High (CTL3_HI)—Offset 124h" on page 2372	00000002h
128h	4	"Source Status Register for Channel 3 - Low (SSTAT3_LO)—Offset 128h" on page 2373	00000000h
12Ch	4	"Source Status Register for Channel 3 - High (SSTAT3_HI)—Offset 12Ch" on page 2373	00000000h
130h	4	"Dest Status Register for Channel 3 - Low (DSTAT3_LO)—Offset 130h" on page 2374	00000000h
134h	4	"Dest Status Register for Channel 3 - High (DSTAT3_HI)—Offset 134h" on page 2374	00000000h
138h	4	"Source Status Address Register for Channel 3 - Low (SSTATAR3_LO)—Offset 138h" on page 2375	00000000h
13Ch	4	"Source Status Address Register for Channel 3 - High (SSTATAR3_HI)—Offset 13Ch" on page 2375	00000000h
140h	4	"Dest Status Address Register for Channel 3 - Low (DSTATAR3_LO)—Offset 140h" on page 2376	00000000h
144h	4	"Dest Status Address Register for Channel 3 - High (DSTATAR3_HI)—Offset 144h" on page 2376	00000000h
148h	4	"Configuration Register for Channel 3 - Low (CFG3_LO)—Offset 148h" on page 2377	00000E60h

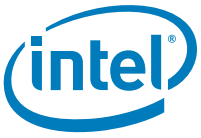


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
14Ch	4	"Configuration Register for Channel 3 - High (CFG3_HI)—Offset 14Ch" on page 2378	00000004h
150h	4	"Source Gather Register for Channel 3 - Low (SGR3_LO)—Offset 150h" on page 2380	00000000h
154h	4	"Source Gather Register for Channel 3 - High (SGR3_HI)—Offset 154h" on page 2380	00000000h
158h	4	"Destination Scatter Register for Channel 3 - Low (DSR3_LO)—Offset 158h" on page 2381	00000000h
15Ch	4	"Dest Scatter Register for Channel 3 - High (DSR3_HI)—Offset 15Ch" on page 2381	00000000h
160h	4	"Source Address Register for Channel 4 - Low (SAR4_LO)—Offset 160h" on page 2382	00000000h
164h	4	"Source Address Register for Channel 4 - High (SAR4_HI)—Offset 164h" on page 2382	00000000h
168h	4	"Destination Address Register for Channel 4 - Low (DAR4_LO)—Offset 168h" on page 2383	00000000h
16Ch	4	"Destination Address Register for Channel 4 - High (DAR4_HI)—Offset 16Ch" on page 2383	00000000h
170h	4	"Linked List Pointer Register for Channel 4 - Low (LLP4_LO)—Offset 170h" on page 2384	00000000h
174h	4	"Linked List Pointer Register for Channel 4 - High (LLP4_HI)—Offset 174h" on page 2384	00000000h
178h	4	"Control Register for Channel 4 - Low (CTL4_LO)—Offset 178h" on page 2385	00304801h
17Ch	4	"Control Register for Channel 4 - High (CTL4_HI)—Offset 17Ch" on page 2386	00000002h
180h	4	"Source Status Register for Channel 4 - Low (SSTAT4_LO)—Offset 180h" on page 2387	00000000h
184h	4	"Source Status Register for Channel 4 - High (SSTAT4_HI)—Offset 184h" on page 2387	00000000h
188h	4	"Dest Status Register for Channel 4 - Low (DSTAT4_LO)—Offset 188h" on page 2388	00000000h
18Ch	4	"Dest Status Register for Channel 4 - High (DSTAT4_HI)—Offset 18Ch" on page 2388	00000000h
190h	4	"Source Status Address Register for Channel 4 - Low (SSTATAR4_LO)—Offset 190h" on page 2389	00000000h
194h	4	"Source Status Address Register for Channel 4 - High (SSTATAR4_HI)—Offset 194h" on page 2389	00000000h
198h	4	"Dest Status Address Register for Channel 4 - Low (DSTATAR4_LO)—Offset 198h" on page 2390	00000000h
19Ch	4	"Dest Status Address Register for Channel 4 - High (DSTATAR4_HI)—Offset 19Ch" on page 2390	00000000h

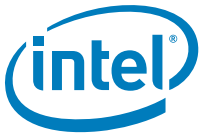


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
1A0h	4	"Configuration Register for Channel 4 - Low (CFG4_LO)—Offset 1A0h" on page 2391	00000E80h
1A4h	4	"Configuration Register for Channel 4 - High (CFG4_HI)—Offset 1A4h" on page 2392	00000004h
1A8h	4	"Source Gather Register for Channel 4 - Low (SGR4_LO)—Offset 1A8h" on page 2393	00000000h
1ACh	4	"Source Gather Register for Channel 4 - High (SGR4_HI)—Offset 1ACh" on page 2394	00000000h
1B0h	4	"Destination Scatter Register for Channel 4 - Low (DSR4_LO)—Offset 1B0h" on page 2394	00000000h
1B4h	4	"Dest Scatter Register for Channel 4 - High (DSR4_HI)—Offset 1B4h" on page 2395	00000000h
1B8h	4	"Source Address Register for Channel 5 - Low (SAR5_LO)—Offset 1B8h" on page 2395	00000000h
1BCh	4	"Source Address Register for Channel 5 - High (SAR5_HI)—Offset 1BCh" on page 2396	00000000h
1C0h	4	"Destination Address Register for Channel 5 - Low (DAR5_LO)—Offset 1C0h" on page 2396	00000000h
1C4h	4	"Destination Address Register for Channel 5 - High (DAR5_HI)—Offset 1C4h" on page 2397	00000000h
1C8h	4	"Linked List Pointer Register for Channel 5 - Low (LLP5_LO)—Offset 1C8h" on page 2397	00000000h
1CCh	4	"Linked List Pointer Register for Channel 5 - High (LLP5_HI)—Offset 1CCh" on page 2398	00000000h
1D0h	4	"Control Register for Channel 5 - Low (CTL5_LO)—Offset 1D0h" on page 2398	00304801h
1D4h	4	"Control Register for Channel 5 - High (CTL5_HI)—Offset 1D4h" on page 2400	00000002h
1D8h	4	"Source Status Register for Channel 5 - Low (SSTAT5_LO)—Offset 1D8h" on page 2400	00000000h
1DCh	4	"Source Status Register for Channel 5 - High (SSTAT5_HI)—Offset 1DCh" on page 2401	00000000h
1E0h	4	"Dest Status Register for Channel 5 - Low (DSTAT5_LO)—Offset 1E0h" on page 2401	00000000h
1E4h	4	"Dest Status Register for Channel 5 - High (DSTAT5_HI)—Offset 1E4h" on page 2402	00000000h
1E8h	4	"Source Status Address Register for Channel 5 - Low (SSTATAR5_LO)—Offset 1E8h" on page 2402	00000000h
1ECh	4	"Source Status Address Register for Channel 5 - High (SSTATAR5_HI)—Offset 1ECh" on page 2403	00000000h
1F0h	4	"Dest Status Address Register for Channel 5 - Low (DSTATAR5_LO)—Offset 1F0h" on page 2403	00000000h

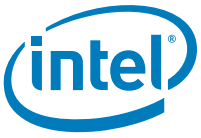


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
1F4h	4	"Dest Status Address Register for Channel 5 - High (DSTATAR5_HI)—Offset 1F4h" on page 2404	00000000h
1F8h	4	"Configuration Register for Channel 5 - Low (CFG5_LO)—Offset 1F8h" on page 2404	00000EA0h
1FCh	4	"Configuration Register for Channel 5 - High (CFG5_HI)—Offset 1FCh" on page 2406	00000004h
200h	4	"Source Gather Register for Channel 5 - Low (SGR5_LO)—Offset 200h" on page 2407	00000000h
204h	4	"Source Gather Register for Channel 5 - High (SGR5_HI)—Offset 204h" on page 2408	00000000h
208h	4	"Destination Scatter Register for Channel 5 - Low (DSR5_LO)—Offset 208h" on page 2408	00000000h
20Ch	4	"Dest Scatter Register for Channel 5 - High (DSR5_HI)—Offset 20Ch" on page 2409	00000000h
210h	4	"Source Address Register for Channel 6 - Low (SAR6_LO)—Offset 210h" on page 2409	00000000h
214h	4	"Source Address Register for Channel 6 - High (SAR6_HI)—Offset 214h" on page 2410	00000000h
218h	4	"Destination Address Register for Channel 6 - Low (DAR6_LO)—Offset 218h" on page 2410	00000000h
21Ch	4	"Destination Address Register for Channel 6 - High (DAR6_HI)—Offset 21Ch" on page 2411	00000000h
220h	4	"Linked List Pointer Register for Channel 6 - Low (LLP6_LO)—Offset 220h" on page 2411	00000000h
224h	4	"Linked List Pointer Register for Channel 6 - High (LLP6_HI)—Offset 224h" on page 2412	00000000h
228h	4	"Control Register for Channel 6 - Low (CTL6_LO)—Offset 228h" on page 2412	00304801h
22Ch	4	"Control Register for Channel 6 - High (CTL6_HI)—Offset 22Ch" on page 2413	00000002h
230h	4	"Source Status Register for Channel 6 - Low (SSTAT6_LO)—Offset 230h" on page 2414	00000000h
234h	4	"Source Status Register for Channel 6 - High (SSTAT6_HI)—Offset 234h" on page 2415	00000000h
238h	4	"Dest Status Register for Channel 6 - Low (DSTAT6_LO)—Offset 238h" on page 2415	00000000h
23Ch	4	"Dest Status Register for Channel 6 - High (DSTAT6_HI)—Offset 23Ch" on page 2416	00000000h
240h	4	"Source Status Address Register for Channel 6 - Low (SSTATAR6_LO)—Offset 240h" on page 2416	00000000h
244h	4	"Source Status Address Register for Channel 6 - High (SSTATAR6_HI)—Offset 244h" on page 2417	00000000h

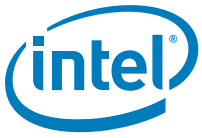


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
248h	4	"Dest Status Address Register for Channel 6 - Low (DSTATAR6_LO)—Offset 248h" on page 2417	00000000h
24Ch	4	"Dest Status Address Register for Channel 6 - High (DSTATAR6_HI)—Offset 24Ch" on page 2418	00000000h
250h	4	"Configuration Register for Channel 6 - Low (CFG6_LO)—Offset 250h" on page 2418	00000EC0h
254h	4	"Configuration Register for Channel 6 - High (CFG6_HI)—Offset 254h" on page 2420	00000004h
258h	4	"Source Gather Register for Channel 6 - Low (SGR6_LO)—Offset 258h" on page 2421	00000000h
25Ch	4	"Source Gather Register for Channel 6 - High (SGR6_HI)—Offset 25Ch" on page 2421	00000000h
260h	4	"Destination Scatter Register for Channel 6 - Low (DSR6_LO)—Offset 260h" on page 2422	00000000h
264h	4	"Dest Scatter Register for Channel 6 - High (DSR6_HI)—Offset 264h" on page 2422	00000000h
268h	4	"Source Address Register for Channel 7 - Low (SAR7_LO)—Offset 268h" on page 2423	00000000h
26Ch	4	"Source Address Register for Channel 7 - High (SAR7_HI)—Offset 26Ch" on page 2423	00000000h
270h	4	"Destination Address Register for Channel 7 - Low (DAR7_LO)—Offset 270h" on page 2424	00000000h
274h	4	"Destination Address Register for Channel 7 - High (DAR7_HI)—Offset 274h" on page 2424	00000000h
278h	4	"Linked List Pointer Register for Channel 7 - Low (LLP7_LO)—Offset 278h" on page 2425	00000000h
27Ch	4	"Linked List Pointer Register for Channel 7 - High (LLP7_HI)—Offset 27Ch" on page 2425	00000000h
280h	4	"Control Register for Channel 7 - Low (CTL7_LO)—Offset 280h" on page 2426	00304801h
284h	4	"Control Register for Channel 7 - High (CTL7_HI)—Offset 284h" on page 2427	00000002h
288h	4	"Source Status Register for Channel 7 - Low (SSTAT7_LO)—Offset 288h" on page 2428	00000000h
28Ch	4	"Source Status Register for Channel 7 - High (SSTAT7_HI)—Offset 28Ch" on page 2428	00000000h
290h	4	"Dest Status Register for Channel 7 - Low (DSTAT7_LO)—Offset 290h" on page 2429	00000000h
294h	4	"Dest Status Register for Channel 7 - High (DSTAT7_HI)—Offset 294h" on page 2429	00000000h
298h	4	"Source Status Address Register for Channel 7 - Low (SSTATAR7_LO)—Offset 298h" on page 2430	00000000h

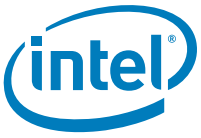


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
29Ch	4	"Source Status Address Register for Channel 7 - High (SSTATAR7_HI)—Offset 29Ch" on page 2430	00000000h
2A0h	4	"Dest Status Address Register for Channel 7 - Low (DSTATAR7_LO)—Offset 2A0h" on page 2431	00000000h
2A4h	4	"Dest Status Address Register for Channel 7 - High (DSTATAR7_HI)—Offset 2A4h" on page 2431	00000000h
2A8h	4	"Configuration Register for Channel 7 - Low (CFG7_LO)—Offset 2A8h" on page 2432	00000EE0h
2ACh	4	"Configuration Register for Channel 7 - High (CFG7_HI)—Offset 2ACh" on page 2433	00000004h
2B0h	4	"Source Gather Register for Channel 7 - Low (SGR7_LO)—Offset 2B0h" on page 2435	00000000h
2B4h	4	"Source Gather Register for Channel 7 - High (SGR7_HI)—Offset 2B4h" on page 2435	00000000h
2B8h	4	"Destination Scatter Register for Channel 7 - Low (DSR7_LO)—Offset 2B8h" on page 2436	00000000h
2BCh	4	"Dest Scatter Register for Channel 7 - High (DSR7_HI)—Offset 2BCh" on page 2436	00000000h
2C0h	4	"Interrupt Raw Status Registers - Low (RawTfr_LO)—Offset 2C0h" on page 2437	00000000h
2C4h	4	"Interrupt Raw Status Registers - High (RawTfr_HI)—Offset 2C4h" on page 2437	00000000h
2C8h	4	"Interrupt Raw Status Registers - Low (RawBlock_LO)—Offset 2C8h" on page 2438	00000000h
2CCh	4	"Interrupt Raw Status Registers - High (RawBlock_HI)—Offset 2CCh" on page 2438	00000000h
2D0h	4	"Interrupt Raw Status Registers - Low (RawSrcTran_LO)—Offset 2D0h" on page 2439	00000000h
2D4h	4	"Interrupt Raw Status Registers - High (RawSrcTran_HI)—Offset 2D4h" on page 2439	00000000h
2D8h	4	"Interrupt Raw Status Registers - Low (RawDstTran_LO)—Offset 2D8h" on page 2440	00000000h
2DCh	4	"Interrupt Raw Status Registers - High (RawDstTran_HI)—Offset 2DCh" on page 2440	00000000h
2E0h	4	"Interrupt Raw Status Registers - Low (RawErr_LO)—Offset 2E0h" on page 2441	00000000h
2E4h	4	"Interrupt Raw Status Registers - High (RawErr_HI)—Offset 2E4h" on page 2441	00000000h
2E8h	4	"Interrupt Status Registers - Low (StatusTfr_LO)—Offset 2E8h" on page 2442	00000000h
2ECh	4	"Interrupt Status Registers - High (StatusTfr_HI)—Offset 2ECh" on page 2443	00000000h

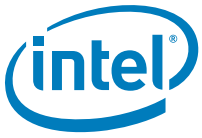


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
2F0h	4	"Interrupt Status Registers - Low (StatusBlock_LO)—Offset 2F0h" on page 2443	00000000h
2F4h	4	"Interrupt Status Registers - High (StatusBlock_HI)—Offset 2F4h" on page 2444	00000000h
2F8h	4	"Interrupt Status Registers - Low (StatusSrcTran_LO)—Offset 2F8h" on page 2444	00000000h
2FCh	4	"Interrupt Status Registers - High (StatusSrcTran_HI)—Offset 2FCh" on page 2445	00000000h
300h	4	"Interrupt Status Registers - Low (StatusDstTran_LO)—Offset 300h" on page 2445	00000000h
304h	4	"Interrupt Status Registers - High (StatusDstTran_HI)—Offset 304h" on page 2446	00000000h
308h	4	"Interrupt Status Registers - Low (StatusErr_LO)—Offset 308h" on page 2446	00000000h
30Ch	4	"Interrupt Status Registers - High (StatusErr_HI)—Offset 30Ch" on page 2447	00000000h
310h	4	"Interrupt Mask Registers - Low (MaskTfr_LO)—Offset 310h" on page 2447	00000000h
314h	4	"Interrupt Mask Registers - High (MaskTfr_HI)—Offset 314h" on page 2448	00000000h
318h	4	"Interrupt Mask Registers - Low (MaskBlock_LO)—Offset 318h" on page 2449	00000000h
31Ch	4	"Interrupt Mask Registers - High (MaskBlock_HI)—Offset 31Ch" on page 2449	00000000h
320h	4	"Interrupt Mask Registers - Low (MaskSrcTran_LO)—Offset 320h" on page 2450	00000000h
324h	4	"Interrupt Mask Registers - High (MaskSrcTran_HI)—Offset 324h" on page 2451	00000000h
328h	4	"Interrupt Mask Registers - Low (MaskDstTran_LO)—Offset 328h" on page 2451	00000000h
32Ch	4	"Interrupt Mask Registers - High (MaskDstTran_HI)—Offset 32Ch" on page 2452	00000000h
330h	4	"Interrupt Mask Registers - Low (MaskErr_LO)—Offset 330h" on page 2452	00000000h
334h	4	"Interrupt Mask Registers - High (MaskErr_HI)—Offset 334h" on page 2453	00000000h
338h	4	"Interrupt Clear Registers - Low (ClearTfr_LO)—Offset 338h" on page 2454	00000000h
33Ch	4	"Interrupt Clear Registers - High (ClearTfr_HI)—Offset 33Ch" on page 2454	00000000h
340h	4	"Interrupt Clear Registers - Low (ClearBlock_LO)—Offset 340h" on page 2455	00000000h
344h	4	"Interrupt Clear Registers (ClearBlock_HI)—Offset 344h" on page 2455	00000000h

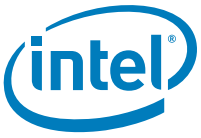


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
348h	4	"Interrupt Clear Registers - Low (ClearSrcTran_LO)—Offset 348h" on page 2456	00000000h
34Ch	4	"Interrupt Clear RegistersClearSrc - High (ClearSrcTran_HI)—Offset 34Ch" on page 2456	00000000h
350h	4	"Interrupt Clear Registers - Low (ClearDstTran_LO)—Offset 350h" on page 2457	00000000h
354h	4	"Interrupt Clear Registers - High (ClearDstTran_HI)—Offset 354h" on page 2457	00000000h
358h	4	"Interrupt Clear Registers - Low (ClearErr_LO)—Offset 358h" on page 2458	00000000h
35Ch	4	"Interrupt Clear Registers - High (ClearErr_HI)—Offset 35Ch" on page 2459	00000000h
360h	4	"Combined Interrupt Status Register - Low (StatusInt_LO)—Offset 360h" on page 2459	00000000h
364h	4	"Combined Interrupt Status Register - High (StatusInt_HI)—Offset 364h" on page 2460	00000000h
368h	4	"Source Software Transaction Request Register - Low (ReqSrcReg_LO)—Offset 368h" on page 2460	00000000h
36Ch	4	"Source Software Transaction Request Register - High (ReqSrcReg_HI)—Offset 36Ch" on page 2461	00000000h
370h	4	"Destination Software Transaction Request Register - Low (ReqDstReg_LO)—Offset 370h" on page 2462	00000000h
374h	4	"Destination Software Transaction Request Register - High (ReqDstReg_HI)—Offset 374h" on page 2462	00000000h
378h	4	"Single Source Software Transaction Request Register - Low (SglRqSrcReg_LO)—Offset 378h" on page 2463	00000000h
37Ch	4	"Single Source Software Transaction Request Register - High (SglRqSrcReg_HI)—Offset 37Ch" on page 2464	00000000h
380h	4	"Single Destination Software Transaction Request Register - Low (SglRqDstReg_LO)—Offset 380h" on page 2464	00000000h
384h	4	"Single Destination Software Transaction Request Register - High (SglRqDstReg_HI)—Offset 384h" on page 2465	00000000h
388h	4	"Last Source Transaction Request Register - Low (LstSrcReg_LO)—Offset 388h" on page 2465	00000000h
38Ch	4	"Last Source Transaction Request Register - High (LstSrcReg_HI)—Offset 38Ch" on page 2466	00000000h
390h	4	"Last Destination Transaction Request Register - Low (LstDstReg_LO)—Offset 390h" on page 2467	00000000h
394h	4	"Last Destination Transaction Request Register - High (LstDstReg_HI)—Offset 394h" on page 2467	00000000h
398h	4	"DW_ahb_dmac Configuration Register - Low (DmaCfgReg_LO)—Offset 398h" on page 2468	00000000h

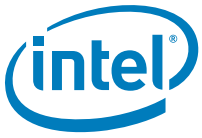


Table 37. Summary of SIO I²C DMA Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
39Ch	4	"DW_ahb_dmac Configuration Register - High (DmaCfgReg_HI)—Offset 39Ch" on page 2468	00000000h
3A0h	4	"DW_ahb_dmac Channel Enable Register - Low (ChEnReg_LO)—Offset 3A0h" on page 2469	00000000h
3A4h	4	"DW_ahb_dmac Channel Enable Register - High (ChEnReg_HI)—Offset 3A4h" on page 2470	00000000h
3A8h	4	"DW_ahb_dmac ID Register - Low (DmaIdReg_LO)—Offset 3A8h" on page 2470	C0CAC01Ah
3ACh	4	"DW_ahb_dmac ID Register - High (DmaIdReg_HI)—Offset 3ACh" on page 2471	00000000h
3B0h	4	"DW_ahb_dmac Test Register - Low (DmaTestReg_LO)—Offset 3B0h" on page 2471	00000000h
3B4h	4	"DW_ahb_dmac Test Register - High (DmaTestReg_HI)—Offset 3B4h" on page 2472	00000000h
3C8h	4	"DW_ahb_dmac Component Parameters Register 6 - Low (DMA_COMP_PARAMS_6_LO)—Offset 3C8h" on page 2473	00000000h
3CCh	4	"DW_ahb_dmac Component Parameters Register 6 - High (DMA_COMP_PARAMS_6_HI)—Offset 3CCh" on page 2473	38220300h
3D0h	4	"DW_ahb_dmac Component Parameters Register 5 - Low (DMA_COMP_PARAMS_5_LO)—Offset 3D0h" on page 2476	38220300h
3D4h	4	"DW_ahb_dmac Component Parameters Register 5 - High (DMA_COMP_PARAMS_5_HI)—Offset 3D4h" on page 2479	38220300h
3D8h	4	"DW_ahb_dmac Component Parameters Register 4 - Low (DMA_COMP_PARAMS_4_LO)—Offset 3D8h" on page 2481	38220300h
3DCh	4	"DW_ahb_dmac Component Parameters Register 4 - High (DMA_COMP_PARAMS_4_HI)—Offset 3DCh" on page 2484	38220300h
3E0h	4	"DW_ahb_dmac Component Parameters Register 3 - Low (DMA_COMP_PARAMS_3_LO)—Offset 3E0h" on page 2487	38220300h
3E4h	4	"DW_ahb_dmac Component Parameters Register 3 - High (DMA_COMP_PARAMS_3_HI)—Offset 3E4h" on page 2490	38220300h
3E8h	4	"DW_ahb_dmac Component Parameters Register 2 - Low (DMA_COMP_PARAMS_2_LO)—Offset 3E8h" on page 2493	38220300h
3ECh	4	"DW_ahb_dmac Component Parameters Register 2 - High (DMA_COMP_PARAMS_2_HI)—Offset 3ECh" on page 2496	00000000h
3F0h	4	"DW_ahb_dmac Component Parameters Register 1 - Low (DMA_COMP_PARAMS_1_LO)—Offset 3F0h" on page 2498	AAAAAAAAh
3F4h	4	"DW_ahb_dmac Component Parameters Register 1 - High (DMA_COMP_PARAMS_1_HI)—Offset 3F4h" on page 2499	37000F04h
3F8h	4	"DMA Component ID RegisterDma - Low (DmaCompsID_LO)—Offset 3F8h" on page 2502	44571110h
3FCh	4	"DMA Component ID Register - High (DmaCompsID_HI)—Offset 3FCh" on page 2502	3231362Ah

3.29.1 Source Address Register for Channel 0 - Low (SAR0_LO)—Offset 0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current AHB transfer.

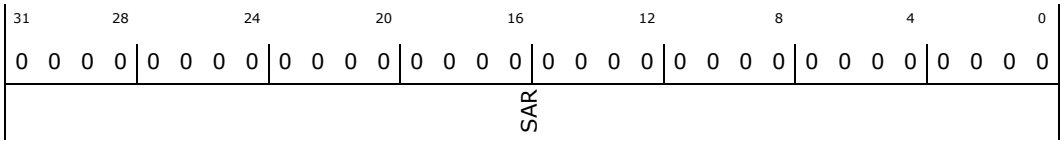
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR0_LO: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.29.2 Source Address Register for Channel 0 - High (SAR0_HI)—Offset 4h

Refer to the description for register Source Address Register for Channel 0 - Low.

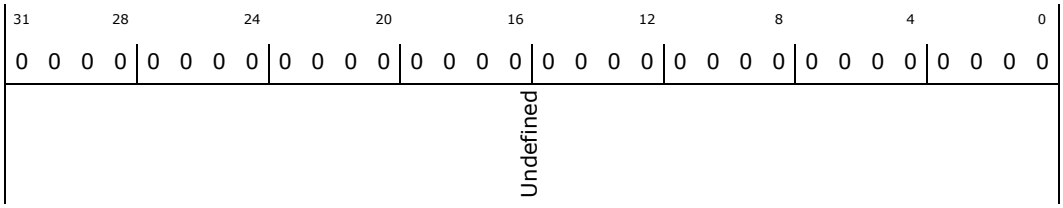
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR0_HI: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.3 Destination Address Register for Channel 0 - Low (DAR0_LO)—Offset 8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current AHB transfer.

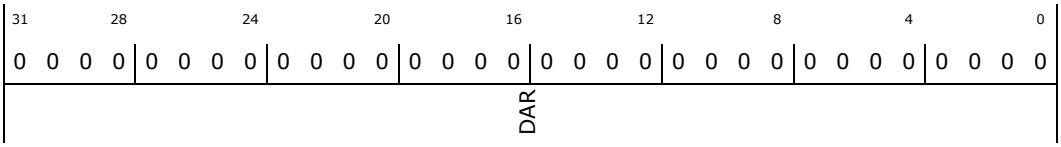
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR0_LO: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.29.4 Destination Address Register for Channel 0 - High (DAR0_HI)—Offset Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

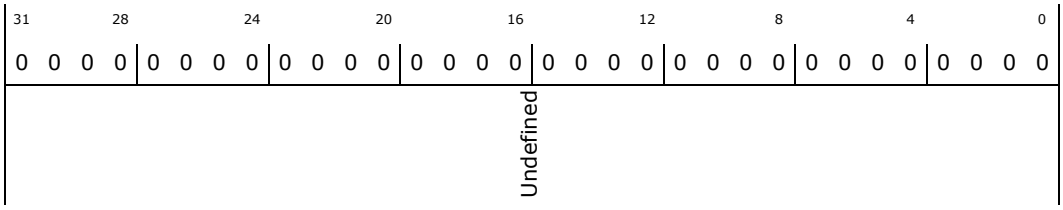
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR0_HI: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.5 Linked List Pointer Register for Channel 0 - Low (LLP0_LO)—Offset 10h

This register does not exist if the DMAH_CHx_HC_LLP configuration parameter is set to True. For further details, refer to the DesignWare DW_ahb_dmac Databook.

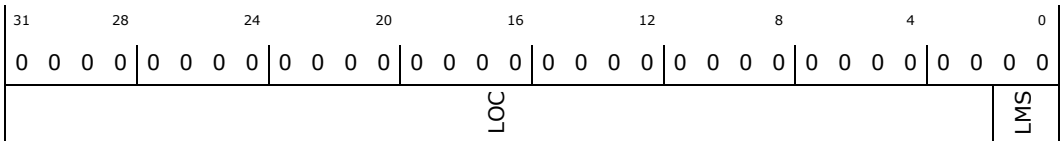
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP0_LO: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.29.6 Linked List Pointer Register for Channel 0 - High (LLP0_HI)—Offset 14h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

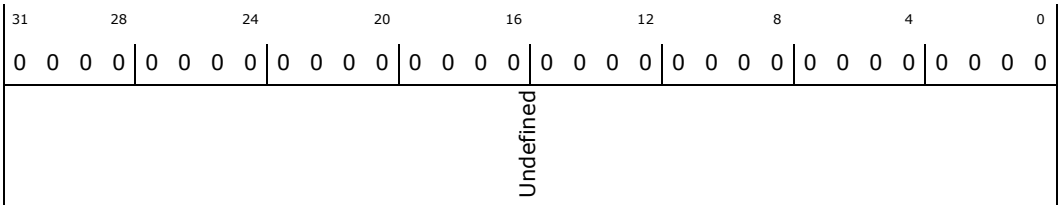
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP0_HI: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.7 Control Register for Channel 0 - Low (CTL0_LO)—Offset 18h

This register contains fields that control the DMA transfer. Refer to the DesignWare DW_ahb_dmac Databook for further details.

Note: You need to program this register prior to enabling the channel.

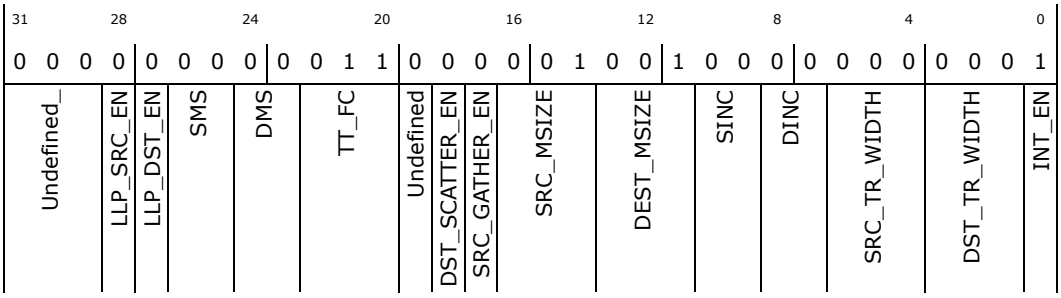
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL0_LO: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.

Bit Range	Default & Access	Description
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** The following transfer types are supported. • Memory to Memory • Memory to Peripheral • Peripheral to Memory • Peripheral to Peripheral Flow Control can be assigned to the DW_ahb_dmac, the source peripheral, or the destination peripheral. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Number of data items, each of width CTLx.SRC_TR_WIDTH, to be read from the source every time a source burst transaction request is made from either the corresponding hardware or software handshaking interface. Refer to the DesignWare DW_ahb_dmac Databook for further details.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Number of data items, each of width CTLx.DST_TR_WIDTH, to be written to the destination every time a destination burst transaction request is made from either the corresponding hardware or software handshaking interface. Refer to the DesignWare DW_ahb_dmac Databook for further details.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.29.8 Control Register for Channel 0 - High (CTL0_HI)—Offset 1Ch

Refer to the register description for Control Register for Channel 0 - Low.

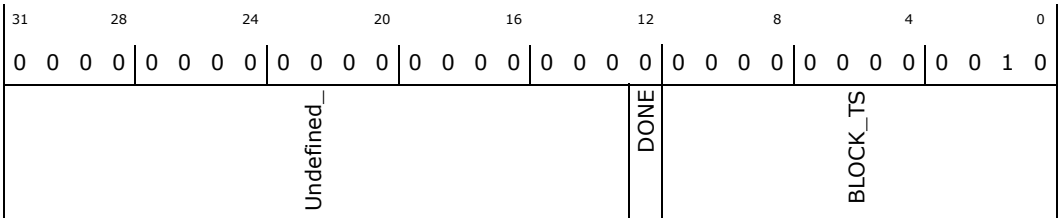
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL0_HI: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** If status write-back is enabled, the upper word of the control register, CTLx[63:32], is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTLx.DONE bit to see when a block transfer is complete. The LLI CTLx.DONE bit should be cleared when the linked lists are set up in memory, prior to enabling the channel. LLI accesses are always 32-bit accesses (Hsize = 2) aligned to 32-bit boundaries and cannot be changed or programmed to anything other than 32-bit. For more information, refer to the DesignWare DW_ahb_dmac Databook.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.29.9 Source Status Register for Channel 0 - Low (SSTAT0_LO)—Offset 20h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Refer to the DesignWare DW_ahb_dmac Databook for further details.

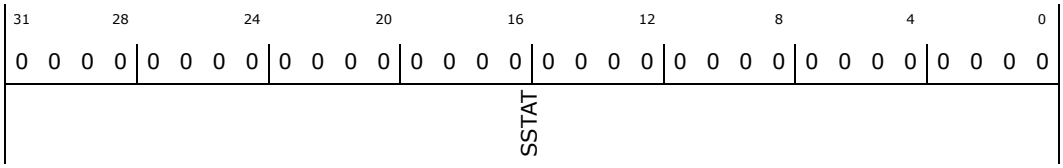
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT0_LO: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.29.10 Source Status Register for Channel 0 - High (SSTAT0_HI)—Offset 24h

Refer to the description for Source Status Register for Channel 0 - Low.

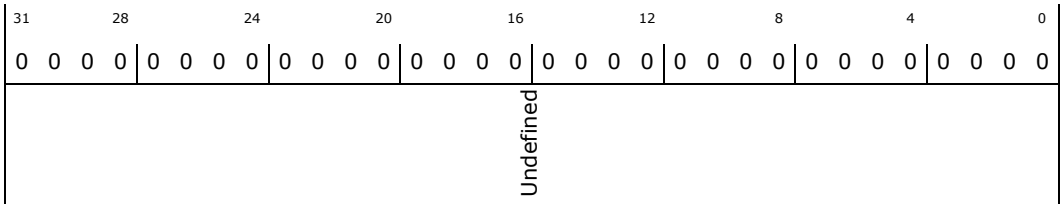
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT0_HI: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.11 Dest Status Register for Channel 0 - Low (DSTAT0_LO)—Offset 28h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to

the DSTATx register location of the LLI (refer to the DesignWare DW_ahb_dmac Databook for further details) before the start of the next block. For conditions under which the destination status information is fetched, refer to the above mentioned spec.

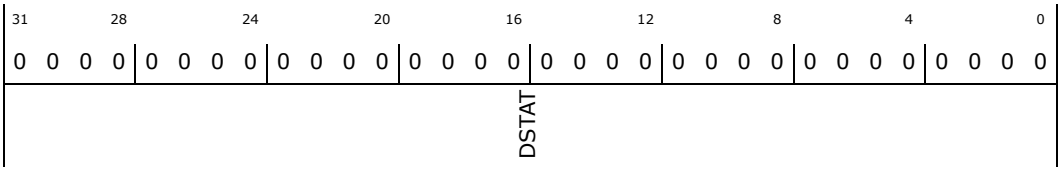
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT0_LO: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

3.29.12 Dest Status Register for Channel 0 - High (DSTAT0_HI)—Offset 2Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

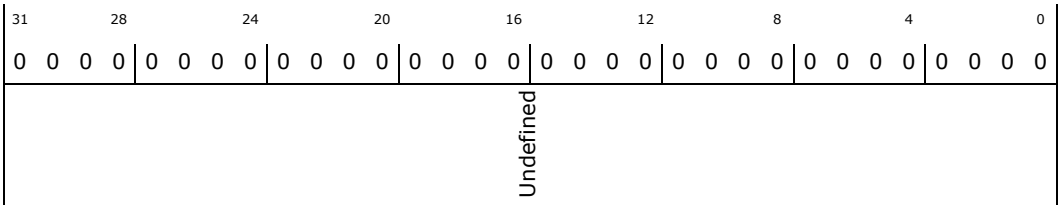
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT0_HI: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.13 Source Status Address Register for Channel 0 - Low (SSTATAR0_LO)—Offset 30h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

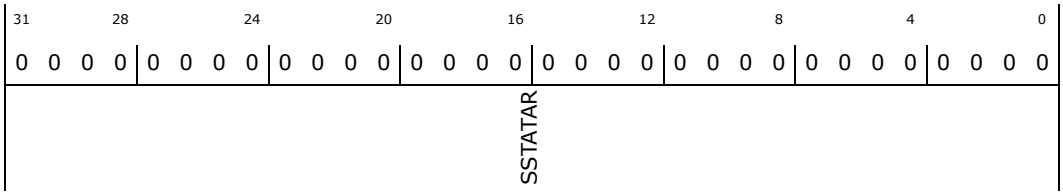
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR0_LO: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.14 Source Status Address Register for Channel 0 - High (SSTATAR0_HI)—Offset 34h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

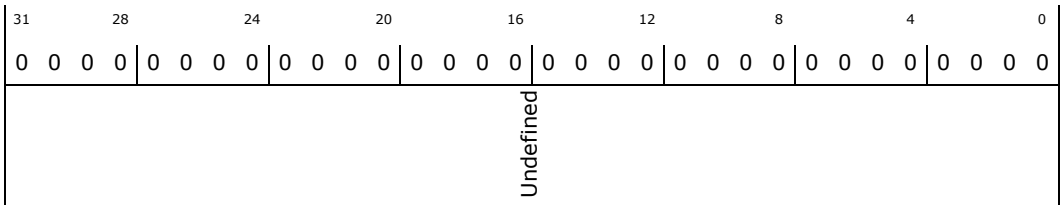
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR0_HI: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.15 Dest Status Address Register for Channel 0 - Low (DSTATAR0_LO)—Offset 38h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. Refer to the DesignWare DW_ahb_dmac Databook for further details.

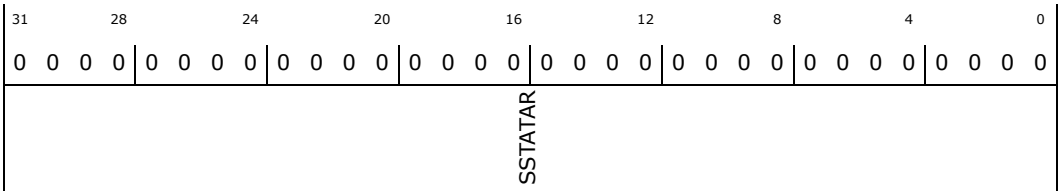
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR0_LO: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.16 Dest Status Address Register for Channel 0 - High (DSTATAR0_HI)—Offset 3Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

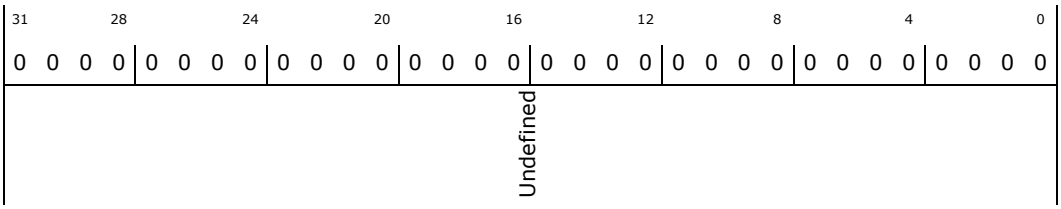
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR0_HI: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.17 Configuration Register for Channel 0 - Low (CFG0_LO)—Offset 40h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.

Note: You need to program this register prior to enabling the channel.

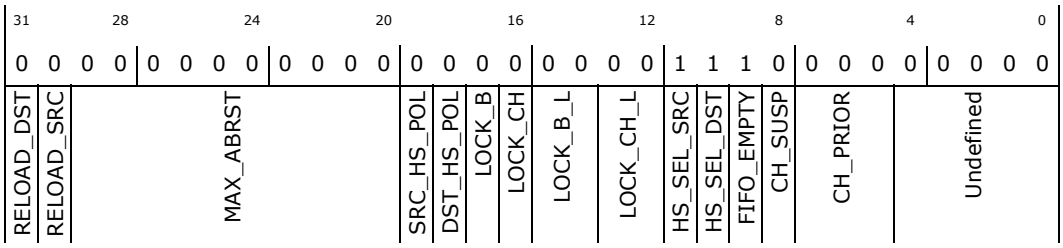
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG0_LO: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E00h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.

Bit Range	Default & Access	Description
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	0h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.29.18 Configuration Register for Channel 0 - High (CFG0_HI)—Offset 44h

Refer to the register description for Configuration Register for Channel 0 - Low.

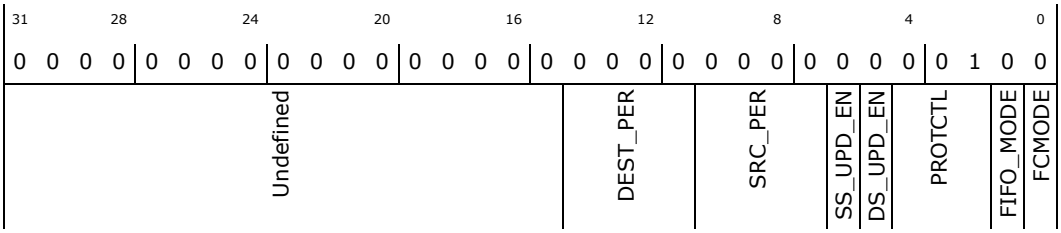
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG0_HI: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.29.19 Source Gather Register for Channel 0 - Low (SGR0_LO)—Offset 48h

The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored. This register does not exist if the configuration parameter DMAH_CHx_SRC_GAT_EN is set to False. For more information, refer to the DesignWare DW_ahb_dmac Databook.

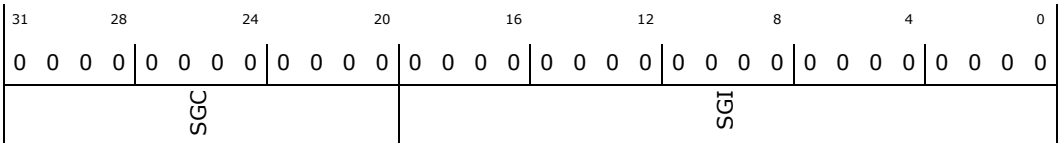
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR0_LO: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Specifies the source address increment/ decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer.

3.29.20 Source Gather Register for Channel 0 - High (SGR0_HI)—Offset 4Ch

Refer to the register description for Source Gather Register for Channel 0 - Low.

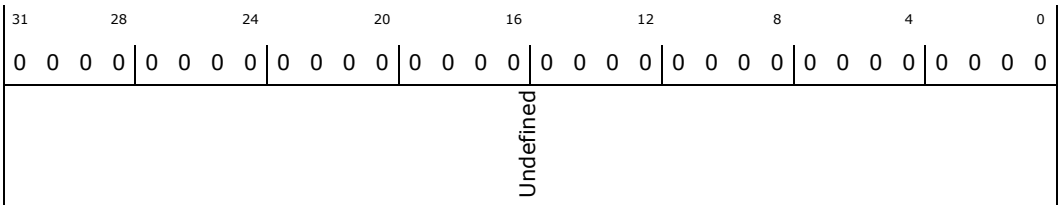
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR0_HI: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.21 Destination Scatter Register for Channel 0 - Low (DSR0_LO)—Offset 50h

The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored. This register does not exist if the configuration parameter DMAH_CHx_DST_SCA_EN is set to False. For more information, refer to the DesignWare DW_ahb_dmac Databook.

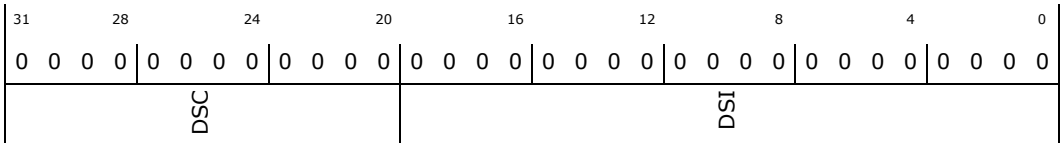
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR0_LO: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Specifies the destination address increment/ decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary, when scatter mode is enabled for the destination transfer.

3.29.22 Dest Scatter Register for Channel 0 - High (DSR0_HI)—Offset 54h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

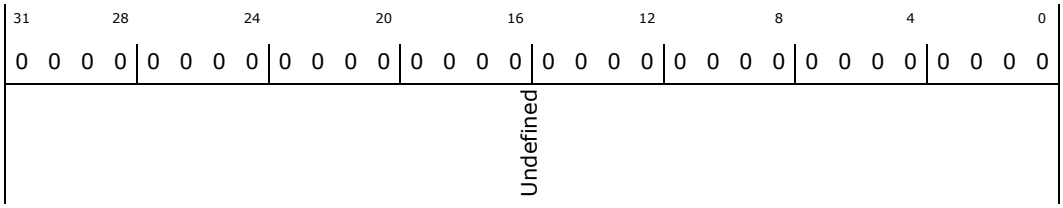
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR0_HI: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.23 Source Address Register for Channel 1 - Low (SAR1_LO)—Offset 58h

Refer to the description for register Source Address Register for Channel 0 - Low.

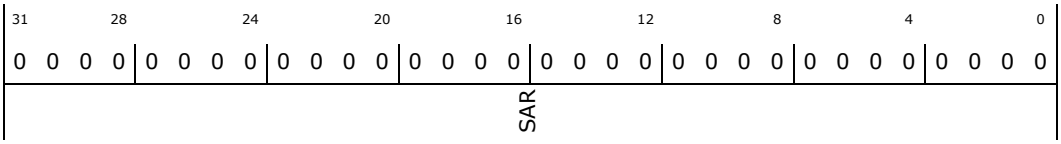
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR1_LO: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.29.24 Source Address Register for Channel 1 - High (SAR1_HI)—Offset 5Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

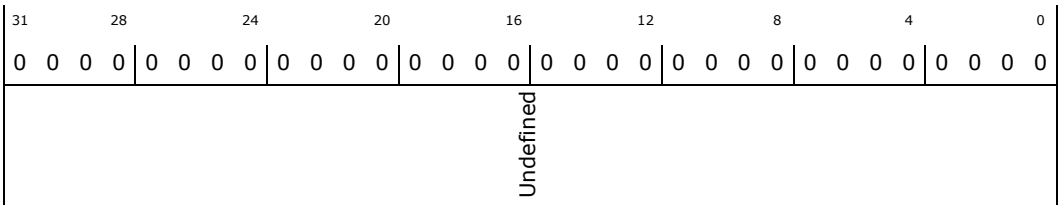
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR1_HI: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.25 Destination Address Register for Channel 1 - Low (DAR1_LO)—Offset 60h

Refer to the description for register Destination Address Register for Channel 0 - Low.

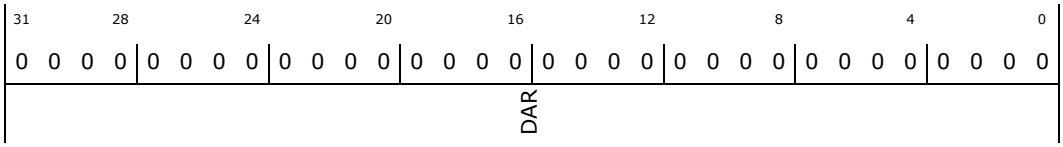
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR1_LO: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.29.26 Destination Address Register for Channel 1 - High (DAR1_HI)—Offset 64h

Refer to the description for register Destination Address Register for Channel 0 - Low.

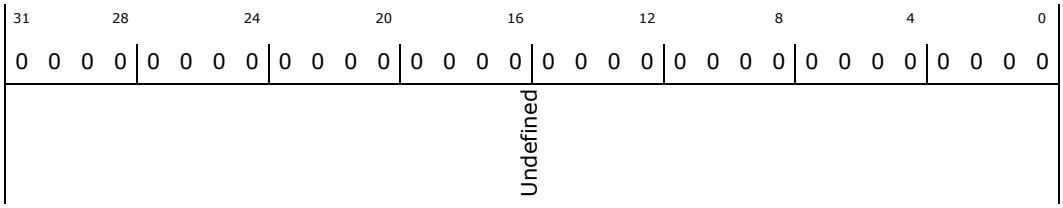
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR1_HI: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.27 Linked List Pointer Register for Channel 1 - Low (LLP1_LO)—Offset 68h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

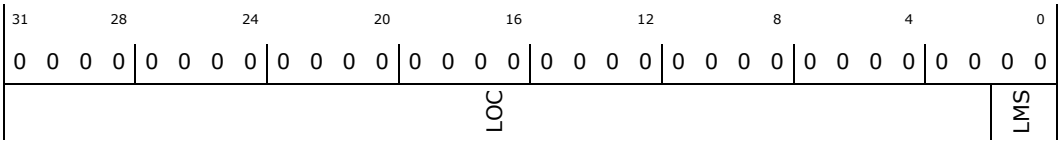
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP1_LO: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.29.28 Linked List Pointer Register for Channel 1 - High (LLP1_HI)—Offset 6Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

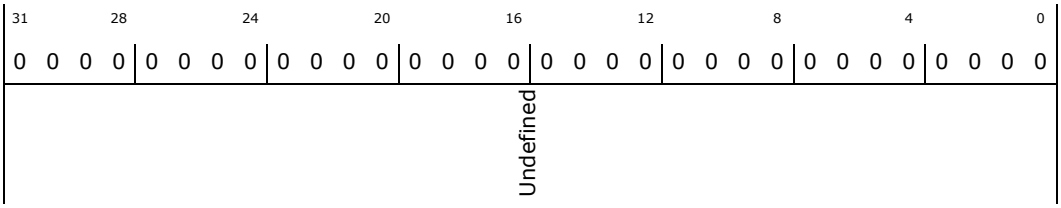
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP1_HI: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.29 Control Register for Channel 1 - Low (CTL1_LO)—Offset 70h

Refer to the register description for Control Register for Channel 0 - Low.

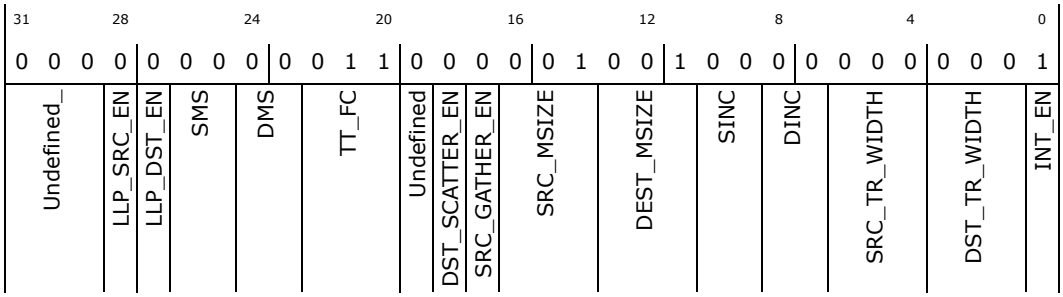
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL1_LO: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change

Bit Range	Default & Access	Description
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.29.30 Control Register for Channel 1 - High (CTL1_HI)—Offset 74h

Refer to the register description for Control Register for Channel 0 - Low.

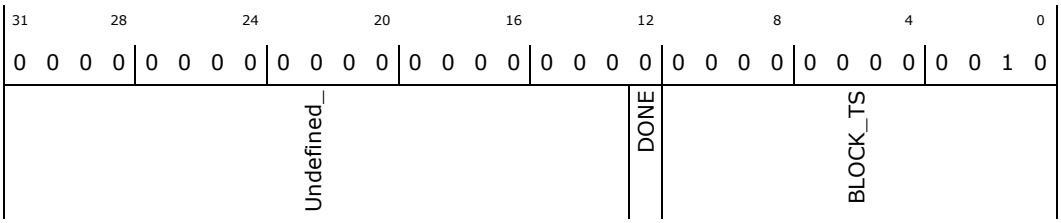
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL1_HI: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled, to indicate the block size.

3.29.31 Source Status Register for Channel 1 - Low (SSTAT1_LO)—Offset 78h

Refer to the register description for Source Status Register for Channel 0 - Low.

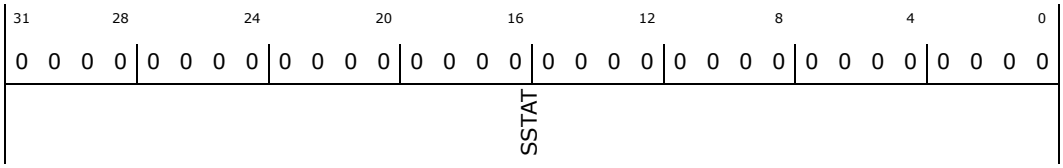
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT1_LO: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.29.32 Source Status Register for Channel 1 - High (SSTAT1_HI)—Offset 7Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

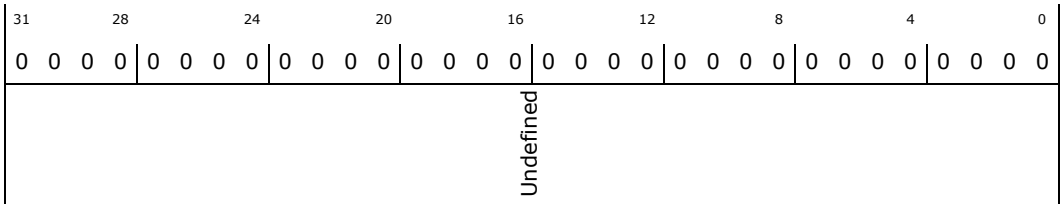
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT1_HI: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.33 Dest Status Register for Channel 1 - Low (DSTAT1_LO)—Offset 80h

Refer to the register description for Dest Status Register for Channel 0 - Low.

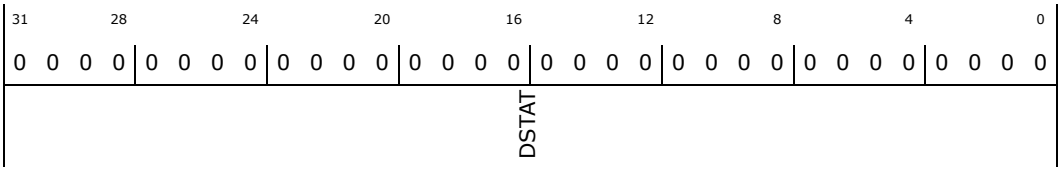
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT1_LO: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest. status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

3.29.34 Dest Status Register for Channel 1 - High (DSTAT1_HI)—Offset 84h

Refer to the register description for Dest Status Register for Channel 0 - Low.

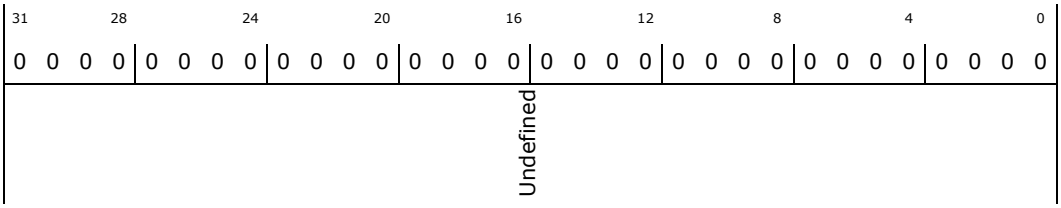
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT1_HI: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.35 Source Status Address Register for Channel 1 - Low (SSTATAR1_LO)—Offset 88h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

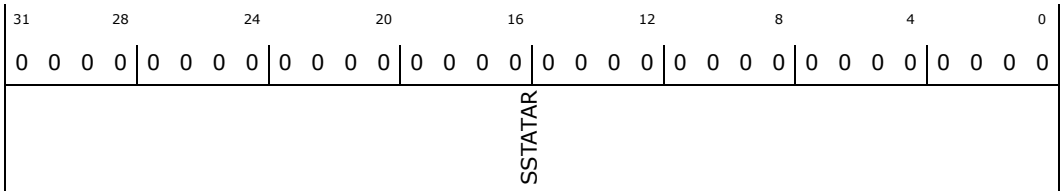
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR1_LO: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.36 Source Status Address Register for Channel 1 - High (SSTATAR1_HI)—Offset 8Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

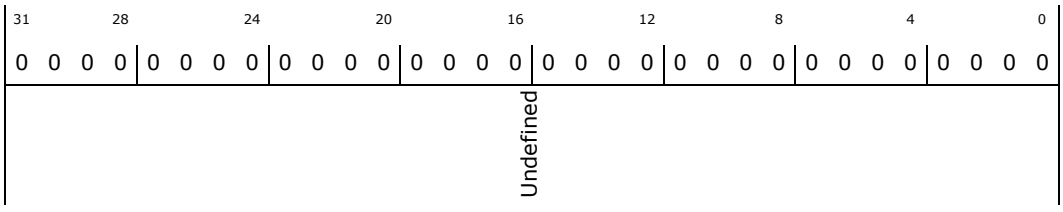
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR1_HI: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.37 Dest Status Address Register for Channel 1 - Low (DSTATAR1_LO)—Offset 90h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

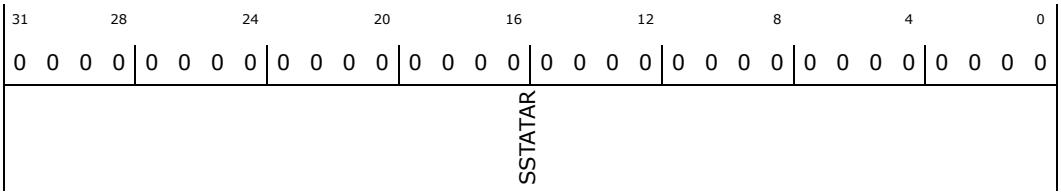
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR1_LO: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.38 Dest Status Address Register for Channel 1 - High (DSTATAR1_HI)—Offset 94h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

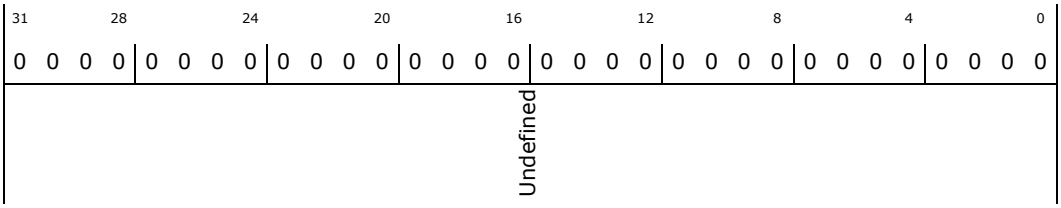
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR1_HI: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.39 Configuration Register for Channel 1 - Low (CFG1_LO)—Offset 98h

Refer to the register description for Configuration Register for Channel 0 - Low.

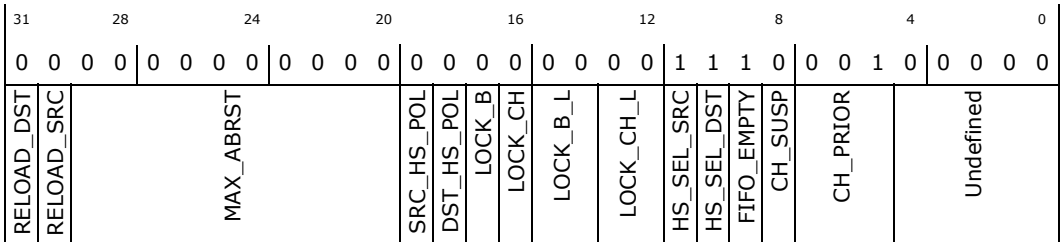
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG1_LO: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E20h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.

Bit Range	Default & Access	Description
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	1h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.29.40 Configuration Register for Channel 1 - High (CFG1_HI)—Offset 9Ch

Refer to the register description for Configuration Register for Channel 0 - Low.

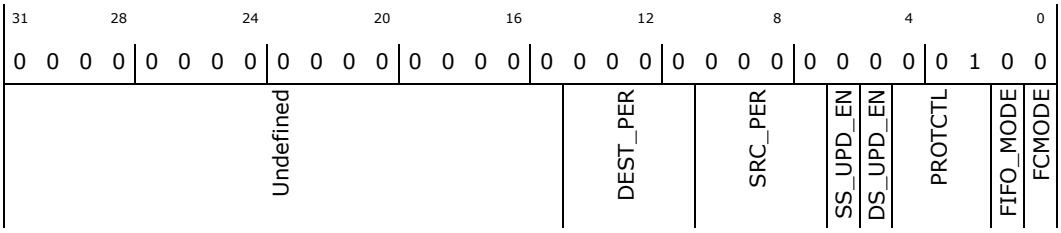
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG1_HI: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.29.41 Source Gather Register for Channel 1 - Low (SGR1_LO)—Offset A0h

Refer to the register description for Source Gather Register for Channel 0 - Low.

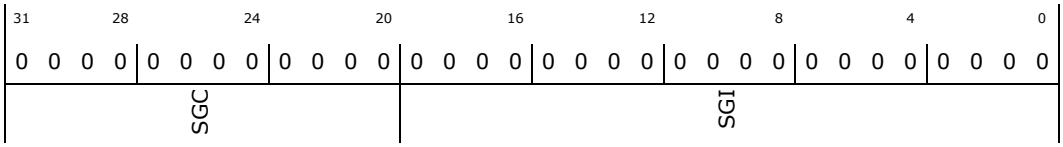
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR1_LO: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.29.42 Source Gather Register for Channel 1 - High (SGR1_HI)—Offset A4h

Refer to the register description for Source Gather Register for Channel 0 - Low.

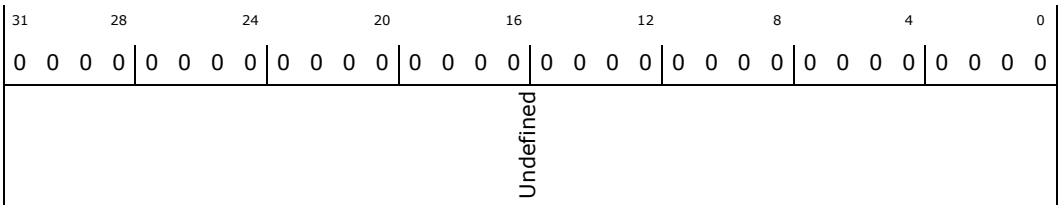
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR1_HI: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.43 Destination Scatter Register for Channel 1 - Low (DSR1_LO)—Offset A8h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

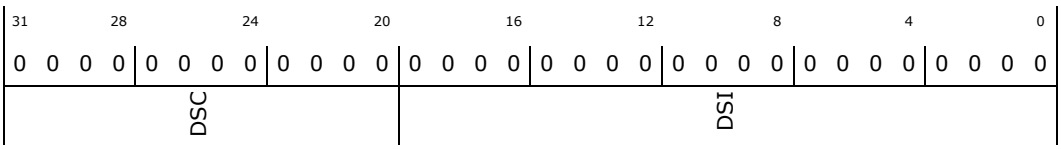
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR1_LO: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.29.44 Dest Scatter Register for Channel 1 - High (DSR1_HI)—Offset ACh

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

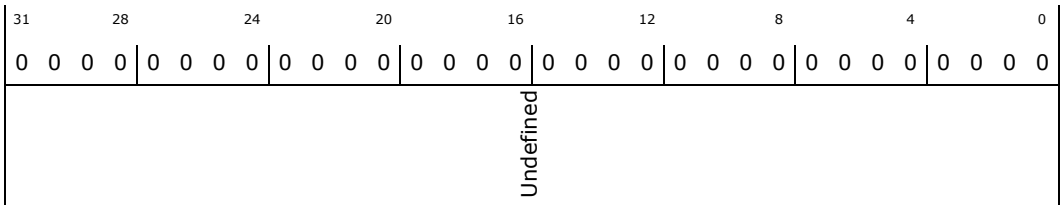
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR1_HI: [BAR] + ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.45 Source Address Register for Channel 2 - Low (SAR2_LO)—Offset B0h

Refer to the description for register Source Address Register for Channel 0 - Low.

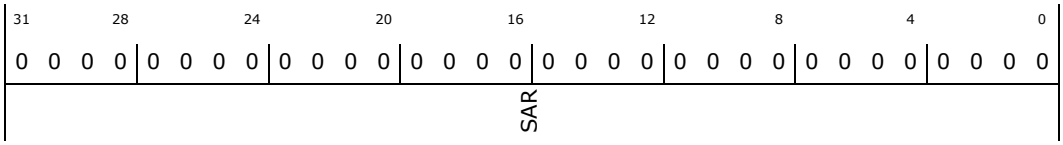
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR2_LO: [BAR] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.29.46 Source Address Register for Channel 2 - High (SAR2_HI)—Offset B4h

Refer to the description for register Source Address Register for Channel 0 - Low.

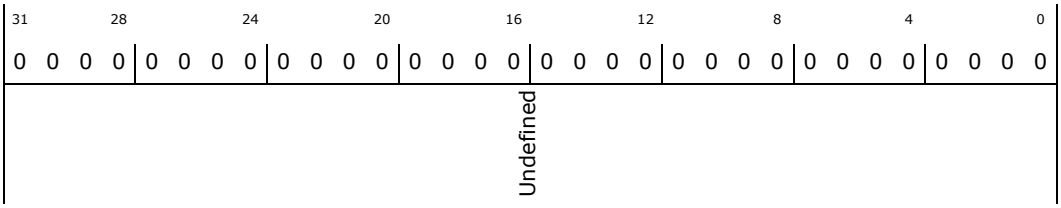
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR2_HI: [BAR] + B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.47 Destination Address Register for Channel 2 - Low (DAR2_LO)—Offset B8h

Refer to the description for register Destination Address Register for Channel 0 - Low.

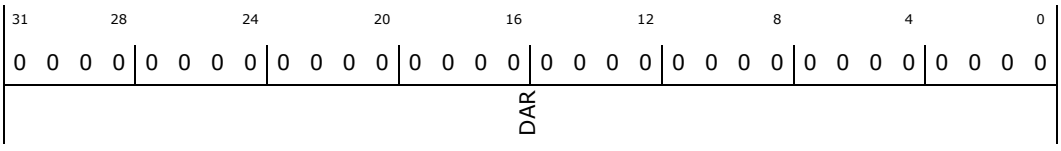
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR2_LO: [BAR] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.29.48 Destination Address Register for Channel 2 - High (DAR2_HI)—Offset BCh

Refer to the description for register Destination Address Register for Channel 0 - Low.

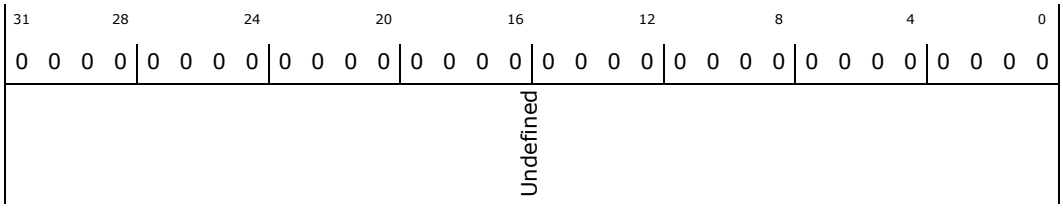
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR2_HI: [BAR] + BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.49 Linked List Pointer Register for Channel 2 - Low (LLP2_LO)—Offset C0h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

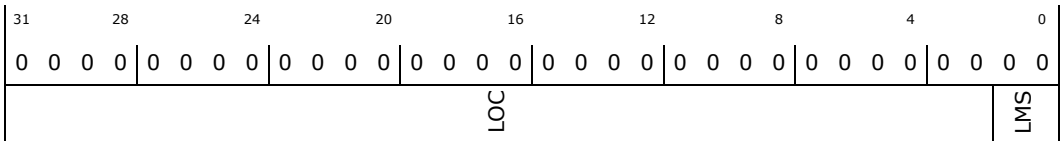
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP2_LO: [BAR] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.29.50 Linked List Pointer Register for Channel 2 - High (LLP2_HI)—Offset C4h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

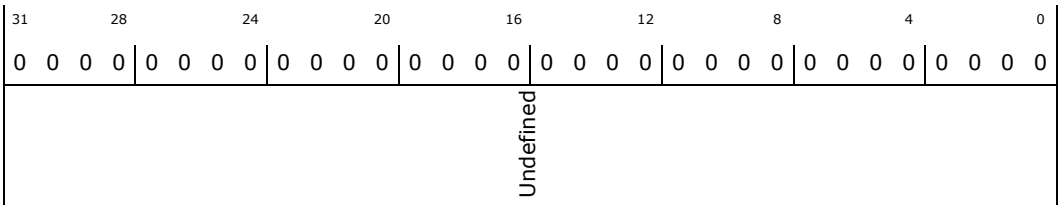
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP2_HI: [BAR] + C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.51 Control Register for Channel 2 - Low (CTL2_LO)—Offset C8h

Refer to the register description for Control Register for Channel 0 - Low.

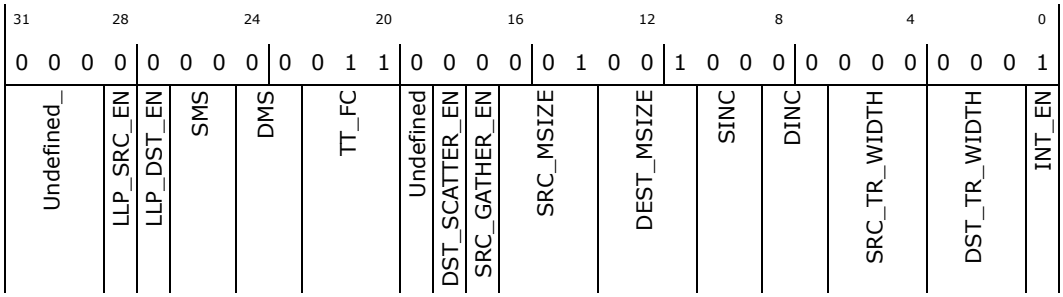
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL2_LO: [BAR] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.

Bit Range	Default & Access	Description
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.29.52 Control Register for Channel 2 - High (CTL2_HI)—Offset CCh

Refer to the register description for Control Register for Channel 0 - Low.

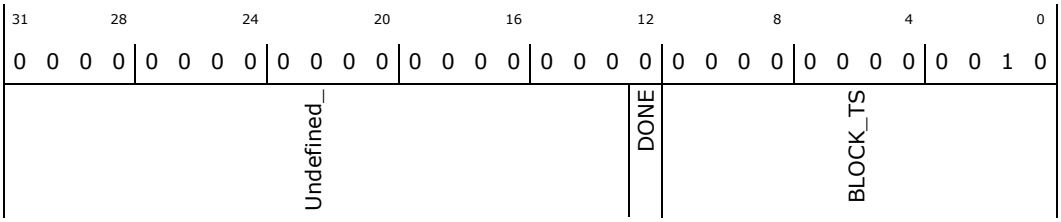
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL2_HI: [BAR] + CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.29.53 Source Status Register for Channel 2 - Low (SSTAT2_LO)—Offset D0h

Refer to the register description for Source Status Register for Channel 0 - Low.

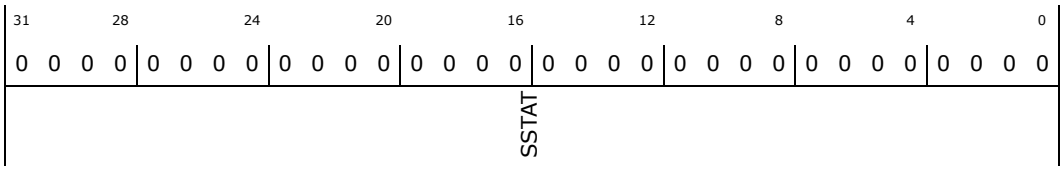
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT2_LO: [BAR] + D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register.

3.29.54 Source Status Register for Channel 2 - High (SSTAT2_HI)—Offset D4h

Refer to the register description for Source Status Register for Channel 0 - Low.

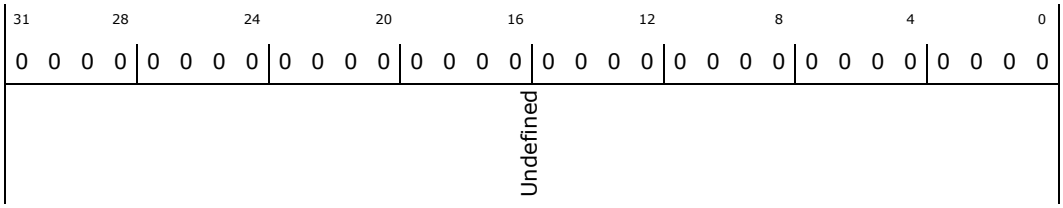
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT2_HI: [BAR] + D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.55 Dest Status Register for Channel 2 - Low (DSTAT2_LO)—Offset D8h

Refer to the register description for Dest Status Register for Channel 0 - Low.

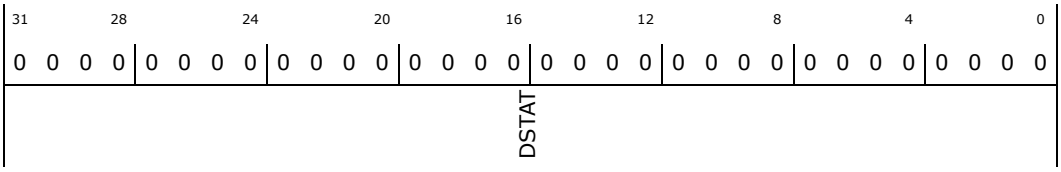
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT2_LO: [BAR] + D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

3.29.56 Dest Status Register for Channel 2 - High (DSTAT2_HI)—Offset DCh

Refer to the register description for Dest Status Register for Channel 0 - Low.

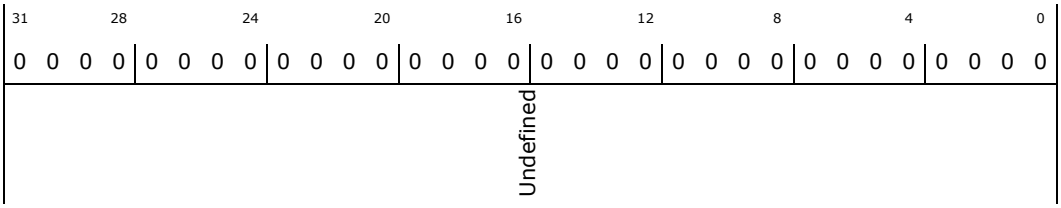
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT2_HI: [BAR] + DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.57 Source Status Address Register for Channel 2 - Low (SSTATAR2_LO)—Offset E0h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

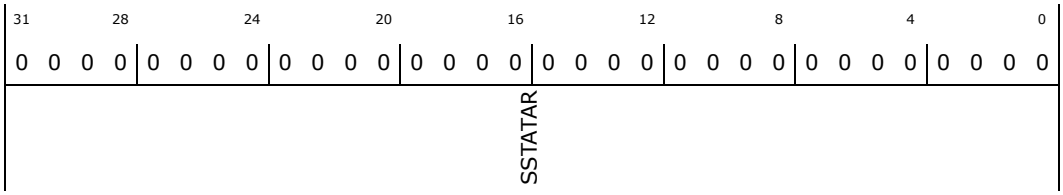
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR2_LO: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.58 Source Status Address Register for Channel 2 - High (SSTATAR2_HI)—Offset E4h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

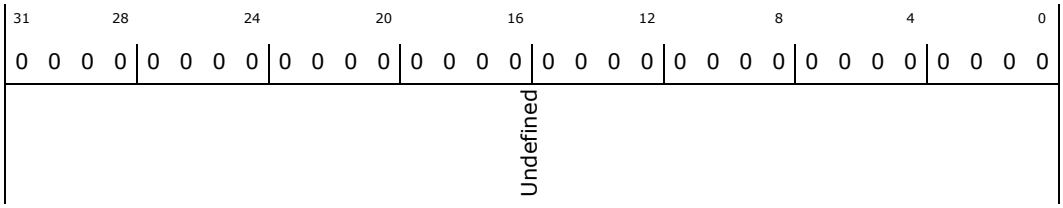
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR2_HI: [BAR] + E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.59 Dest Status Address Register for Channel 2 - Low (DSTATAR2_LO)—Offset E8h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

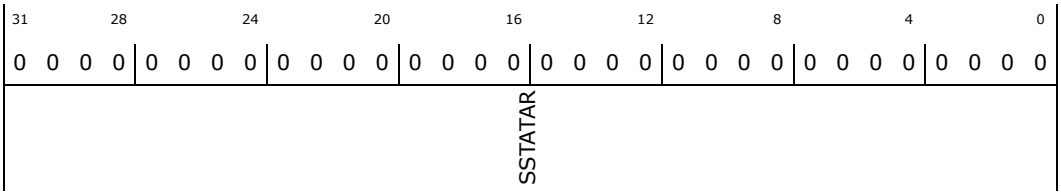
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR2_LO: [BAR] + E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.60 Dest Status Address Register for Channel 2 - High (DSTATAR2_HI)—Offset ECh

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

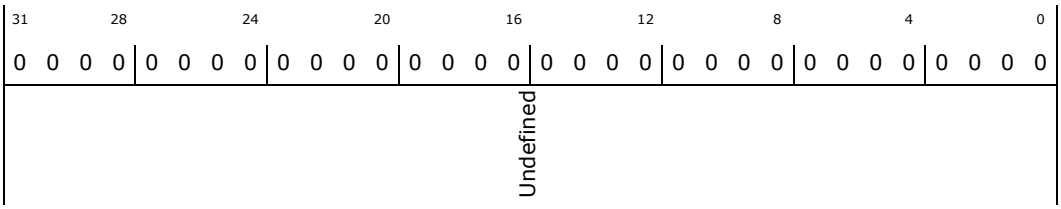
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR2_HI: [BAR] + ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.61 Configuration Register for Channel 2 - Low (CFG2_LO)—Offset F0h

Refer to the register description for Configuration Register for Channel 0 - Low.

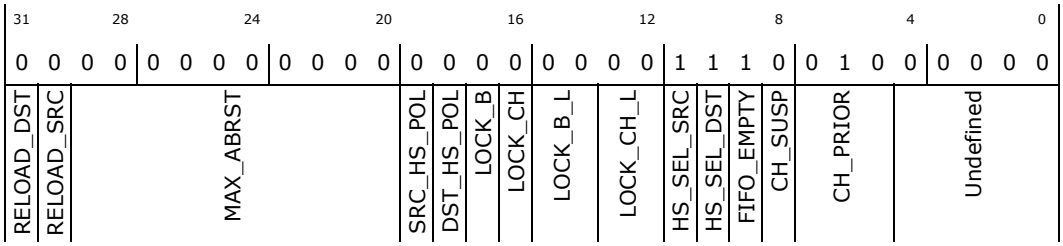
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG2_LO: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E40h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking

Bit Range	Default & Access	Description
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	2h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.29.62 Configuration Register for Channel 2 - High (CFG2_HI)—Offset F4h

Refer to the register description for Configuration Register for Channel 0 - Low.

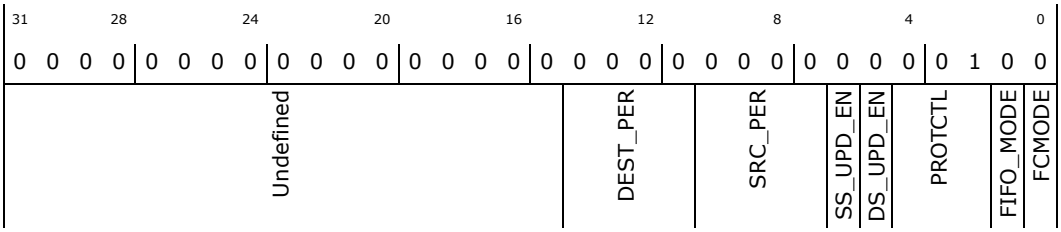
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG2_HI: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.

Bit Range	Default & Access	Description
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.29.63 Source Gather Register for Channel 2 - Low (SGR2_LO)—Offset F8h

Refer to the register description for Source Gather Register for Channel 0 - Low.

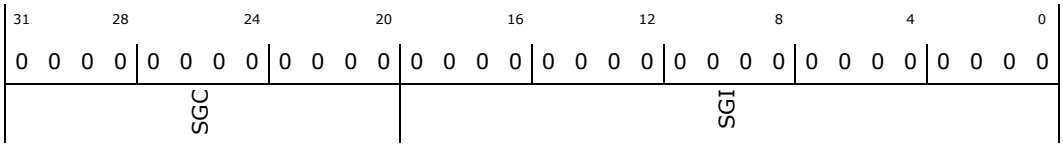
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR2_LO: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.29.64 Source Gather Register for Channel 2 - High (SGR2_HI)—Offset FCh

Refer to the register description for Source Gather Register for Channel 0 - Low.

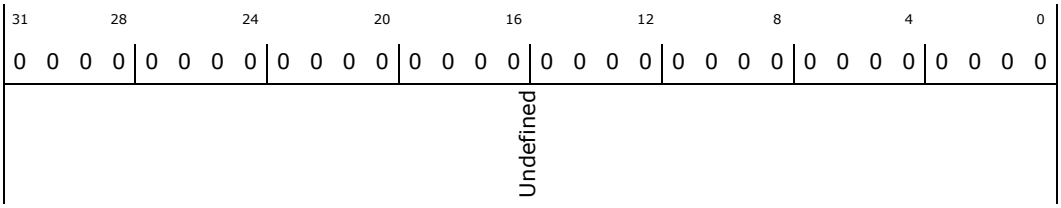
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR2_HI: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.65 Destination Scatter Register for Channel 2 - Low (DSR2_LO)—Offset 100h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

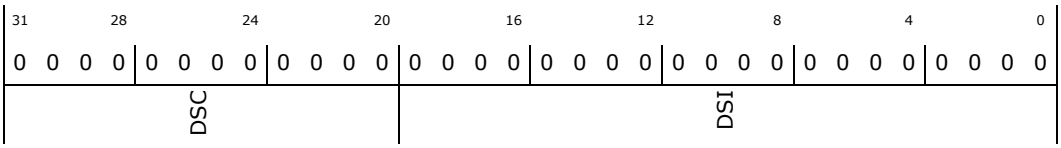
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR2_LO: [BAR] + 100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.29.66 Dest Scatter Register for Channel 2 - High (DSR2_HI)—Offset 104h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

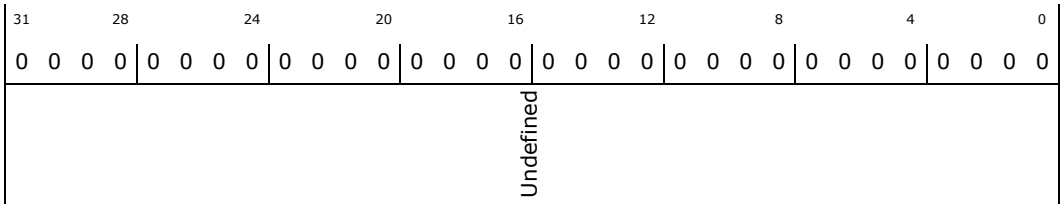
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR2_HI: [BAR] + 104h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.67 Source Address Register for Channel 3 - Low (SAR3_LO)—Offset 108h

Refer to the description for register Source Address Register for Channel 0 - Low.

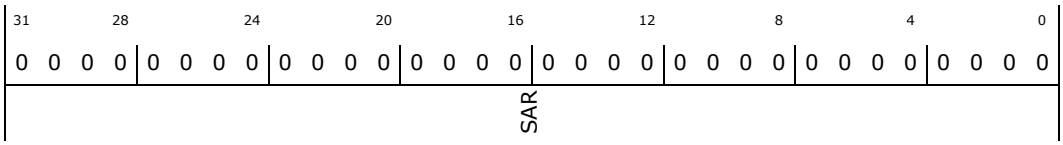
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR3_LO: [BAR] + 108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.29.68 Source Address Register for Channel 3 - High (SAR3_HI)—Offset 10Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

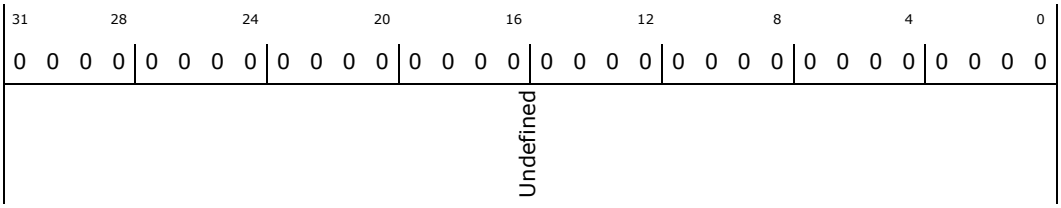
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR3_HI: [BAR] + 10Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.69 Destination Address Register for Channel 3 - Low (DAR3_LO)—Offset 110h

Refer to the description for register Destination Address Register for Channel 0 - Low.

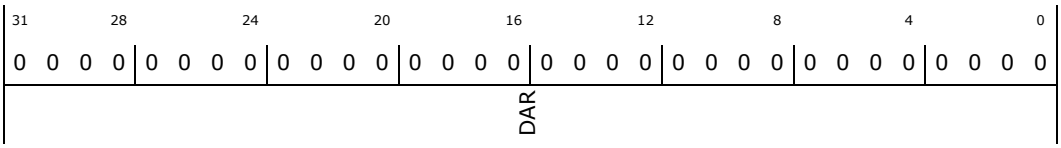
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR3_LO: [BAR] + 110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.29.70 Destination Address Register for Channel 3 - High (DAR3_HI)—Offset 114h

Refer to the description for register Destination Address Register for Channel 0 - Low.

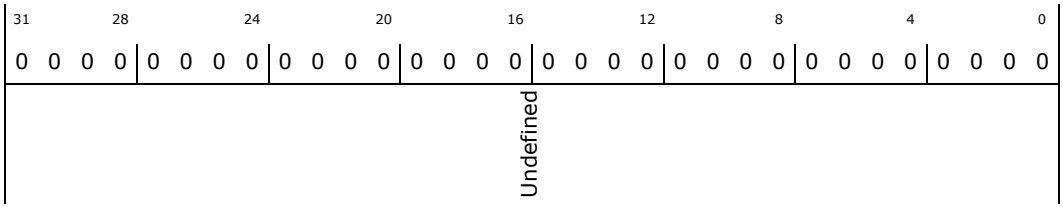
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR3_HI: [BAR] + 114h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.71 Linked List Pointer Register for Channel 3 - Low (LLP3_LO)—Offset 118h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

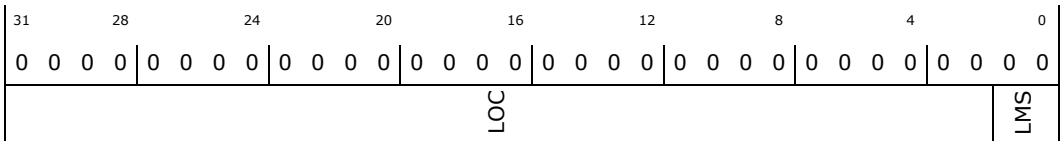
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP3_LO: [BAR] + 118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.29.72 Linked List Pointer Register for Channel 3 - High (LLP3_HI)—Offset 11Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

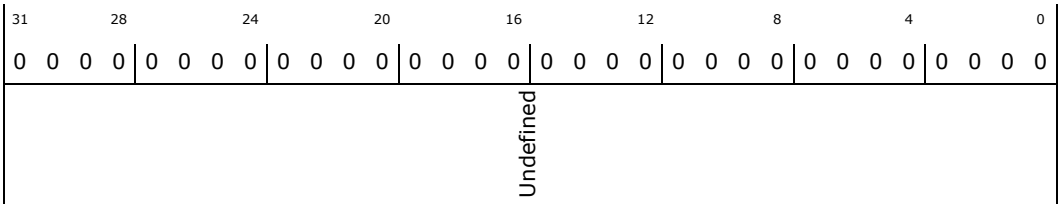
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP3_HI: [BAR] + 11Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.73 Control Register for Channel 3 - Low (CTL3_LO)—Offset 120h

Refer to the register description for Control Register for Channel 0 - Low.

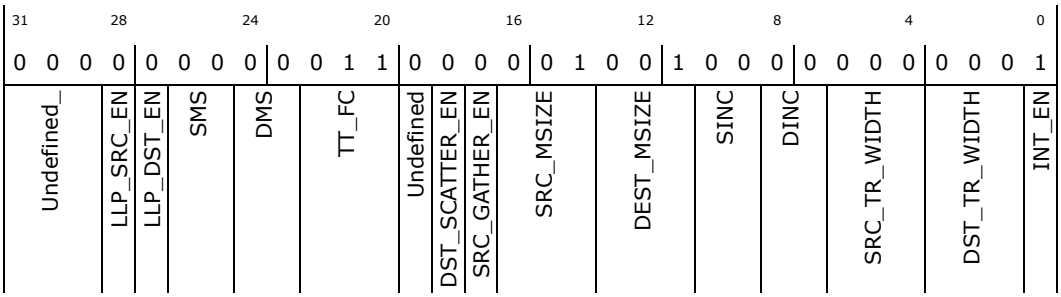
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL3_LO: [BAR] + 120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.

Bit Range	Default & Access	Description
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.29.74 Control Register for Channel 3 - High (CTL3_HI)—Offset 124h

Refer to the register description for Control Register for Channel 0 - Low.

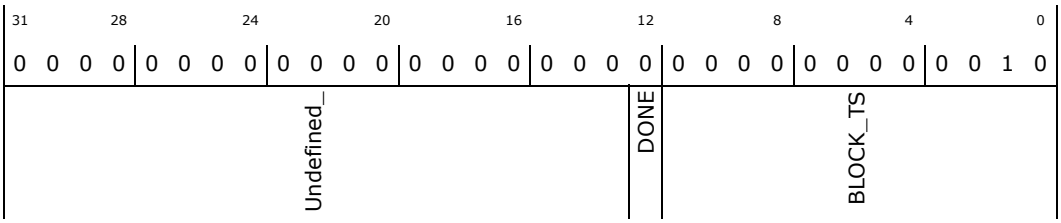
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL3_HI: [BAR] + 124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.29.75 Source Status Register for Channel 3 - Low (SSTAT3_LO)—Offset 128h

Refer to the register description for Source Status Register for Channel 0 - Low.

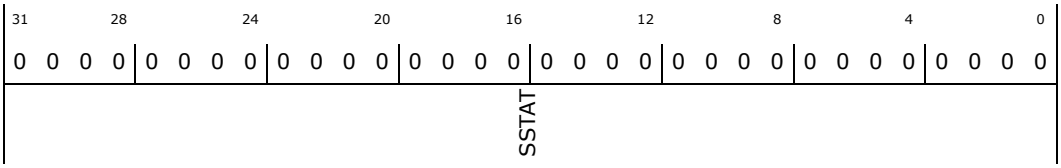
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT3_LO: [BAR] + 128h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.29.76 Source Status Register for Channel 3 - High (SSTAT3_HI)—Offset 12Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

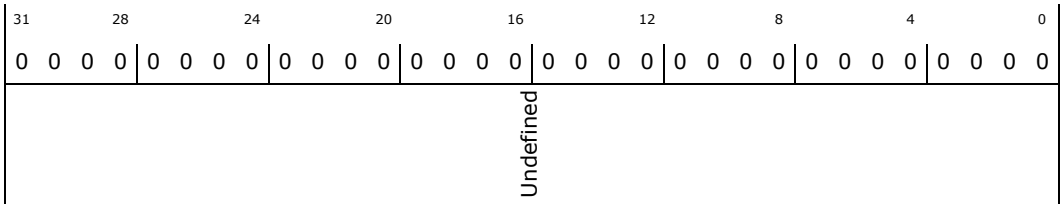
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT3_HI: [BAR] + 12Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.77 Dest Status Register for Channel 3 - Low (DSTAT3_LO)—Offset 130h

Refer to the register description for Dest Status Register for Channel 0 - Low.

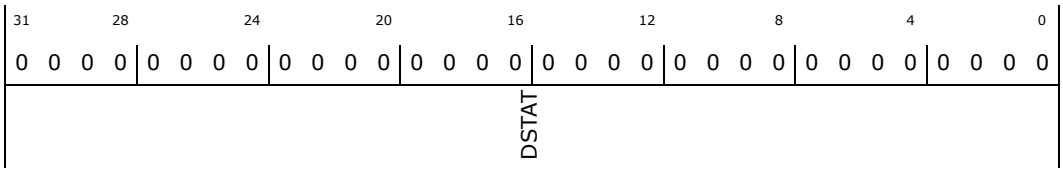
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT3_LO: [BAR] + 130h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

3.29.78 Dest Status Register for Channel 3 - High (DSTAT3_HI)—Offset 134h

Refer to the register description for Dest Status Register for Channel 0 - Low.

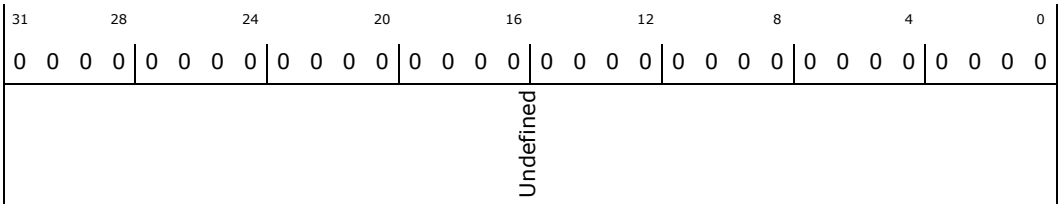
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT3_HI: [BAR] + 134h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.79 Source Status Address Register for Channel 3 - Low (SSTATAR3_LO)—Offset 138h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

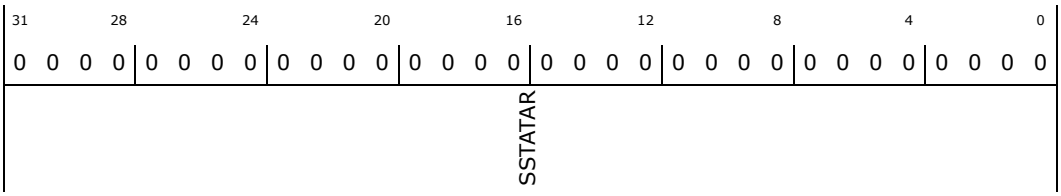
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR3_LO: [BAR] + 138h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.80 Source Status Address Register for Channel 3 - High (SSTATAR3_HI)—Offset 13Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

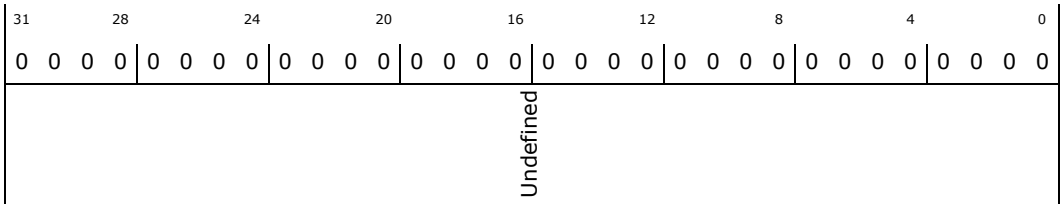
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR3_HI: [BAR] + 13Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.81 Dest Status Address Register for Channel 3 - Low (DSTATAR3_LO)—Offset 140h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

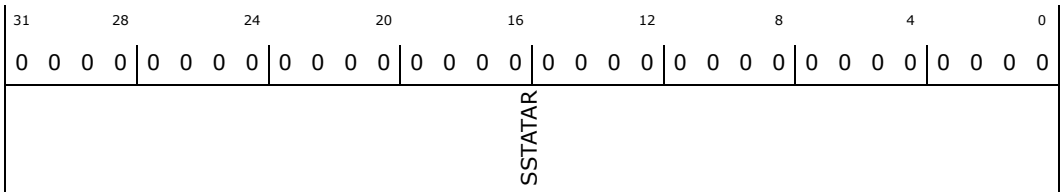
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR3_LO: [BAR] + 140h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.82 Dest Status Address Register for Channel 3 - High (DSTATAR3_HI)—Offset 144h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

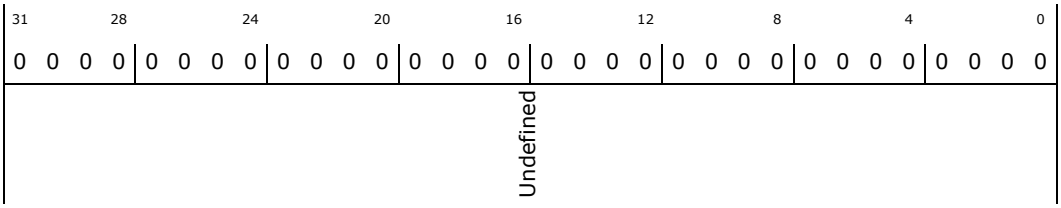
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR3_HI: [BAR] + 144h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.83 Configuration Register for Channel 3 - Low (CFG3_LO)—Offset 148h

Refer to the register description for Configuration Register for Channel 0 - Low.

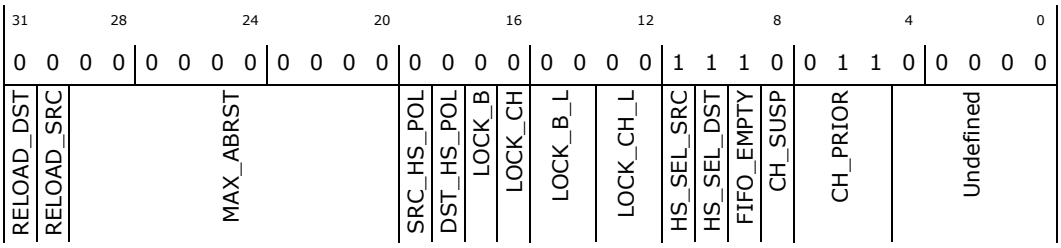
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG3_LO: [BAR] + 148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E60h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.

Bit Range	Default & Access	Description
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	3h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.29.84 Configuration Register for Channel 3 - High (CFG3_HI)—Offset 14Ch

Refer to the register description for Configuration Register for Channel 0 - Low.

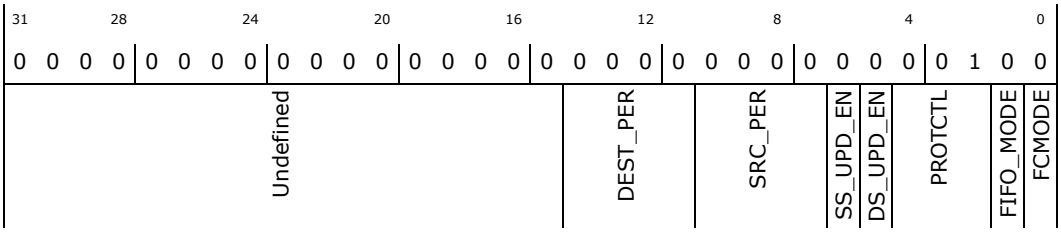
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG3_HI: [BAR] + 14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced, when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.29.85 Source Gather Register for Channel 3 - Low (SGR3_LO)—Offset 150h

Refer to the register description for Source Gather Register for Channel 0 - Low.

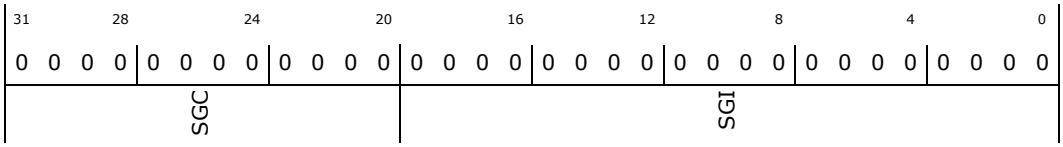
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR3_LO: [BAR] + 150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.29.86 Source Gather Register for Channel 3 - High (SGR3_HI)—Offset 154h

Refer to the register description for Source Gather Register for Channel 0 - Low.

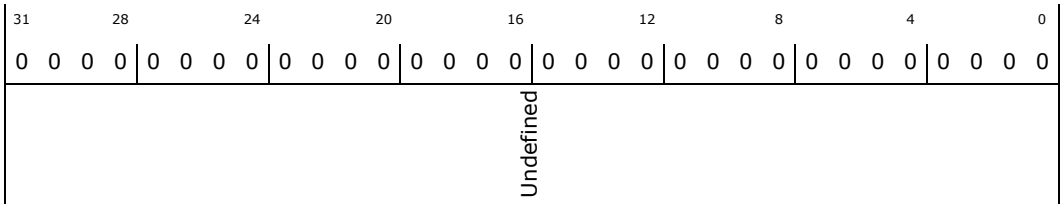
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR3_HI: [BAR] + 154h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.87 Destination Scatter Register for Channel 3 - Low (DSR3_LO)—Offset 158h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

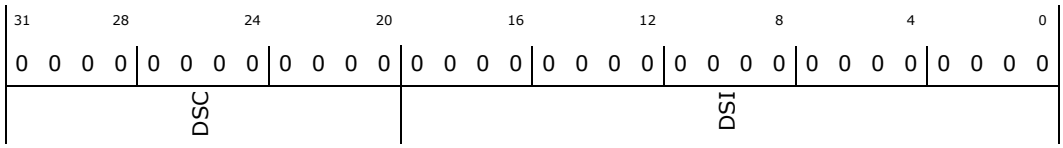
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR3_LO: [BAR] + 158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.29.88 Dest Scatter Register for Channel 3 - High (DSR3_HI)—Offset 15Ch

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

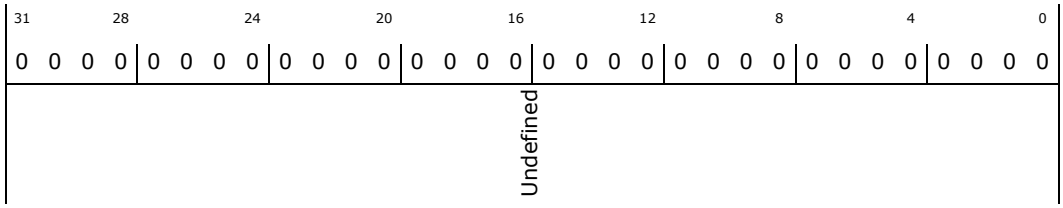
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR3_HI: [BAR] + 15Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.89 Source Address Register for Channel 4 - Low (SAR4_LO)—Offset 160h

Refer to the description for register Source Address Register for Channel 0 - Low.

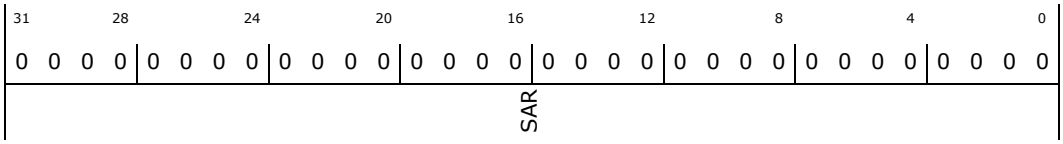
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR4_LO: [BAR] + 160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.29.90 Source Address Register for Channel 4 - High (SAR4_HI)—Offset 164h

Refer to the description for register Source Address Register for Channel 0 - Low.

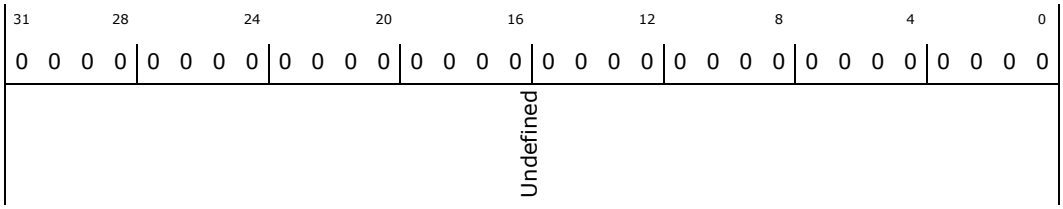
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR4_HI: [BAR] + 164h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.91 Destination Address Register for Channel 4 - Low (DAR4_LO)—Offset 168h

Refer to the description for register Destination Address Register for Channel 0 - Low.

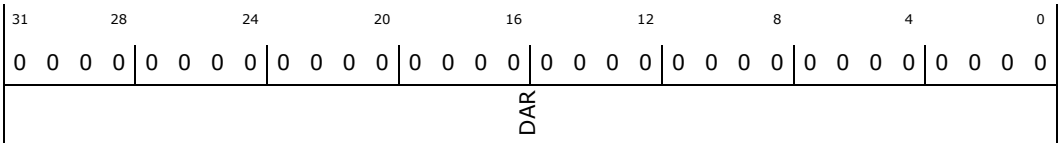
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR4_LO: [BAR] + 168h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.29.92 Destination Address Register for Channel 4 - High (DAR4_HI)—Offset 16Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

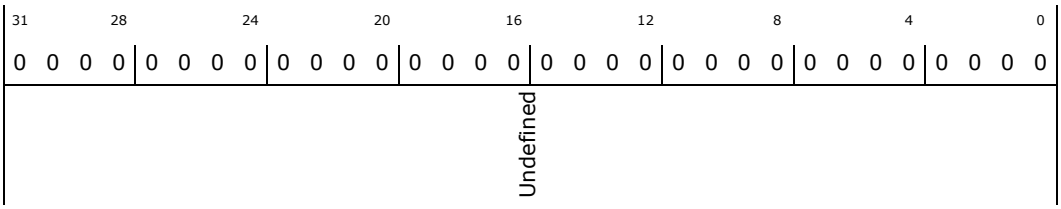
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR4_HI: [BAR] + 16Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.93 Linked List Pointer Register for Channel 4 - Low (LLP4_LO)—Offset 170h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

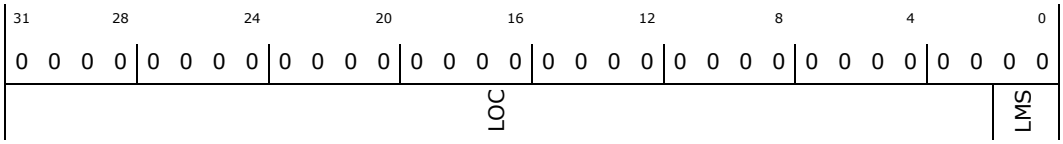
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP4_LO: [BAR] + 170h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.29.94 Linked List Pointer Register for Channel 4 - High (LLP4_HI)—Offset 174h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

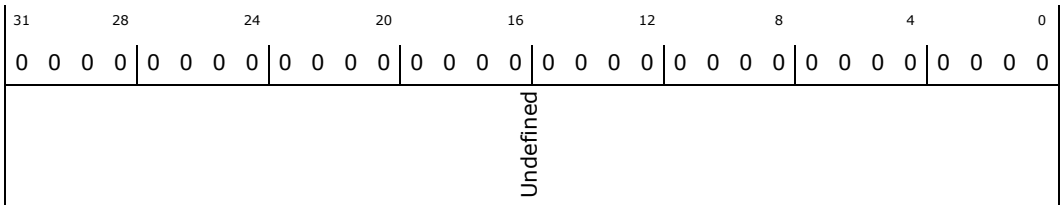
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP4_HI: [BAR] + 174h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.95 Control Register for Channel 4 - Low (CTL4_LO)—Offset 178h

Refer to the register description for Control Register for Channel 0 - Low.

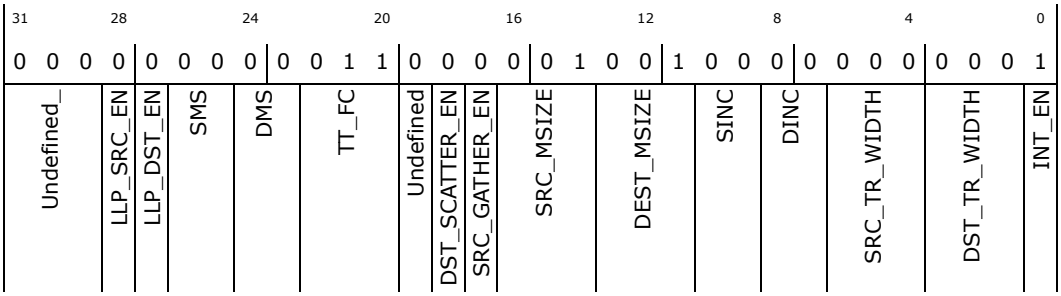
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL4_LO: [BAR] + 178h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.

Bit Range	Default & Access	Description
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.29.96 Control Register for Channel 4 - High (CTL4_HI)—Offset 17Ch

Refer to the register description for Control Register for Channel 0 - Low.

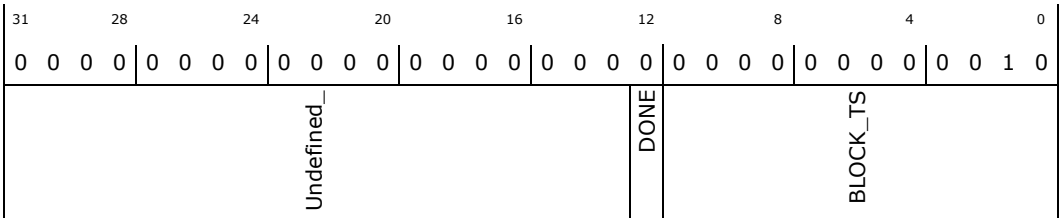
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL4_HI: [BAR] + 17Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.29.97 Source Status Register for Channel 4 - Low (SSTAT4_LO)—Offset 180h

Refer to the register description for Source Status Register for Channel 0 - Low.

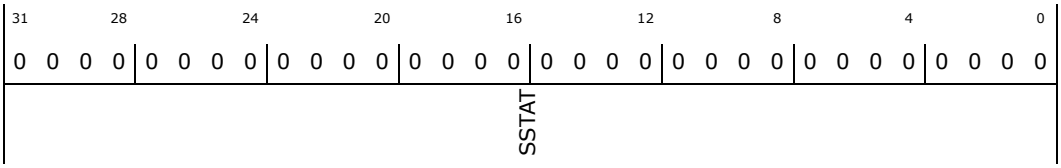
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT4_LO: [BAR] + 180h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register.

3.29.98 Source Status Register for Channel 4 - High (SSTAT4_HI)—Offset 184h

Refer to the register description for Source Status Register for Channel 0 - Low.

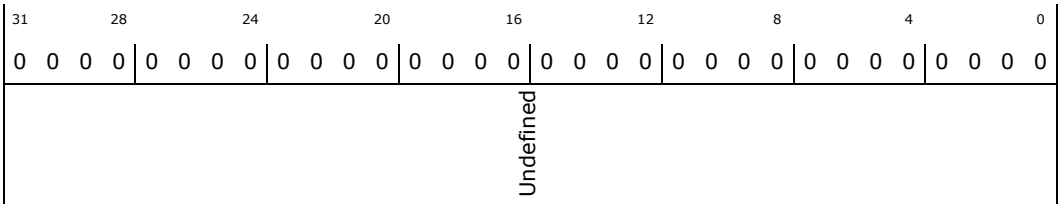
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT4_HI: [BAR] + 184h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.99 Dest Status Register for Channel 4 - Low (DSTAT4_LO)—Offset 188h

Refer to the register description for Dest Status Register for Channel 0 - Low.

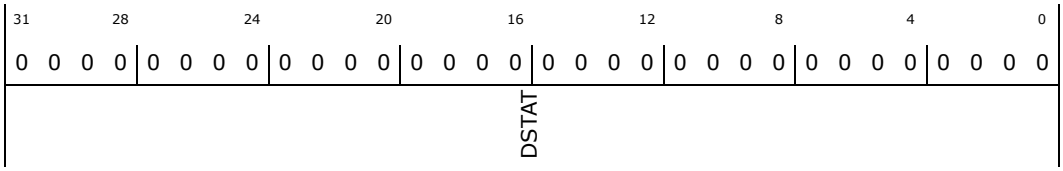
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT4_LO: [BAR] + 188h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

3.29.100 Dest Status Register for Channel 4 - High (DSTAT4_HI)—Offset 18Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

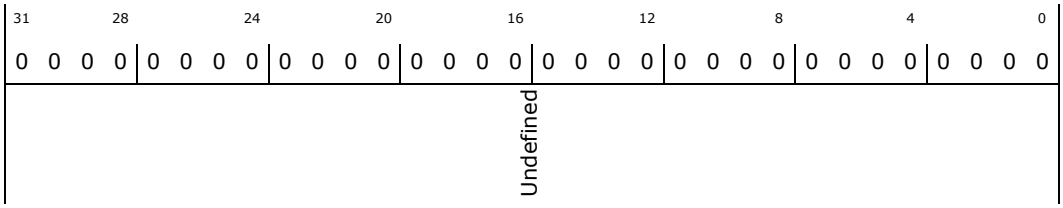
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT4_HI: [BAR] + 18Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.101 Source Status Address Register for Channel 4 - Low (SSTATAR4_LO)—Offset 190h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

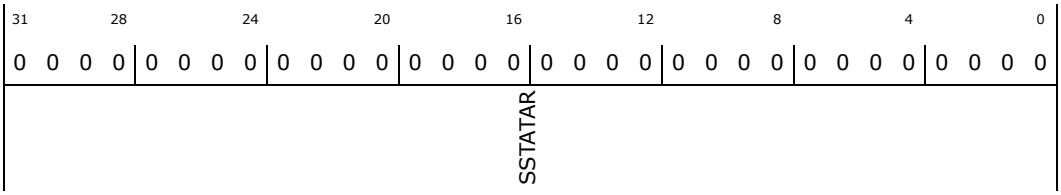
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR4_LO: [BAR] + 190h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.102 Source Status Address Register for Channel 4 - High (SSTATAR4_HI)—Offset 194h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

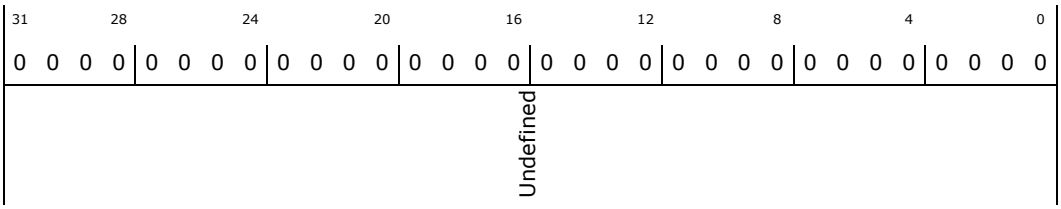
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR4_HI: [BAR] + 194h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.103 Dest Status Address Register for Channel 4 - Low (DSTATAR4_LO)—Offset 198h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

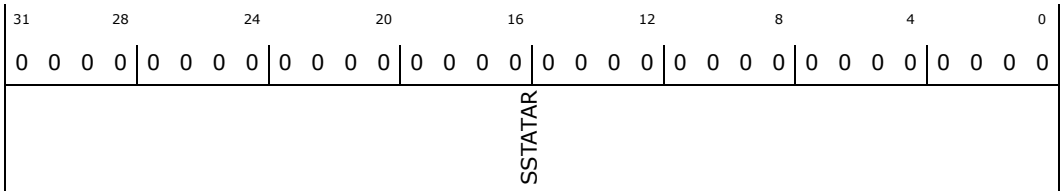
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR4_LO: [BAR] + 198h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.104 Dest Status Address Register for Channel 4 - High (DSTATAR4_HI)—Offset 19Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

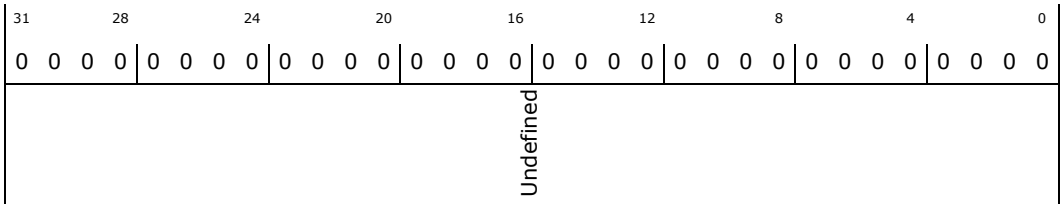
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR4_HI: [BAR] + 19Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.105 Configuration Register for Channel 4 - Low (CFG4_LO)—Offset 1A0h

Refer to the register description for Configuration Register for Channel 0 - Low.

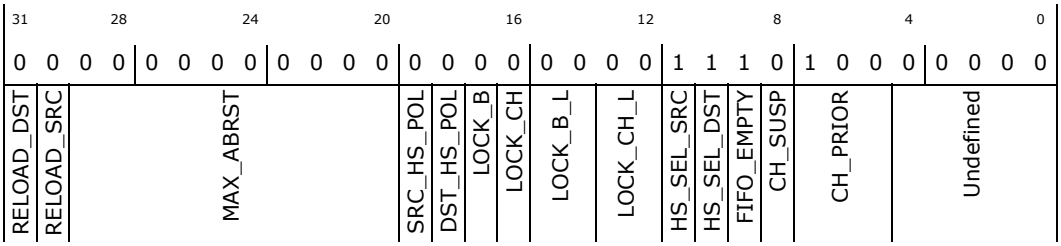
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG4_LO: [BAR] + 1A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E80h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.

Bit Range	Default & Access	Description
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	4h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.29.106 Configuration Register for Channel 4 - High (CFG4_HI)—Offset 1A4h

Refer to the register description for Configuration Register for Channel 0 - Low.

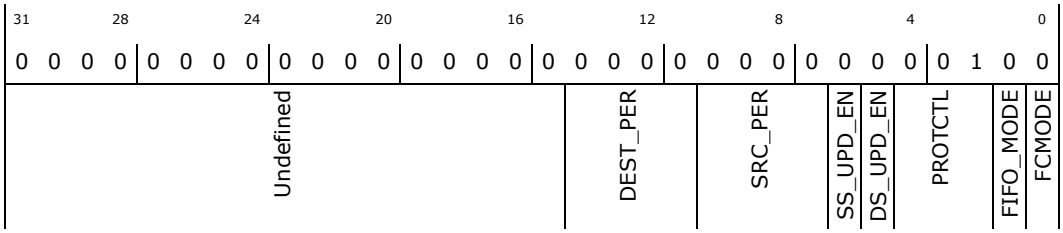
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG4_HI: [BAR] + 1A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.29.107 Source Gather Register for Channel 4 - Low (SGR4_LO)—Offset 1A8h

Refer to the register description for Source Gather Register for Channel 0 - Low.

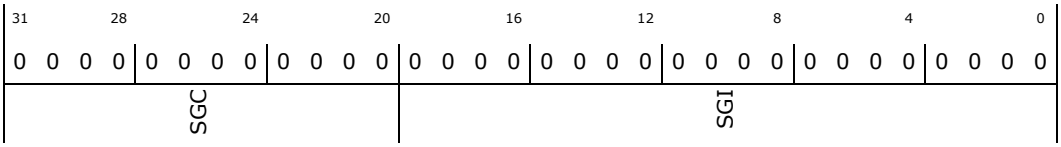
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR4_LO: [BAR] + 1A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.29.108 Source Gather Register for Channel 4 - High (SGR4_HI)—Offset 1ACh

Refer to the register description for Source Gather Register for Channel 0 - Low.

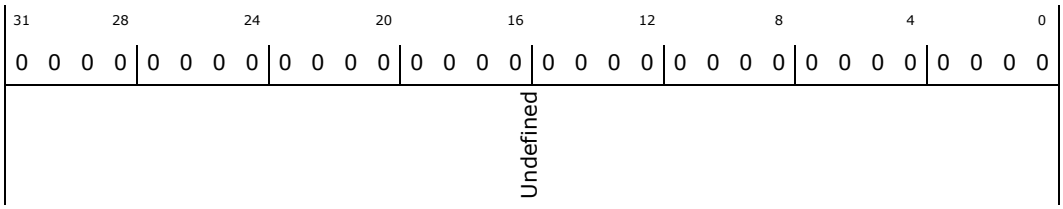
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR4_HI: [BAR] + 1ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.109 Destination Scatter Register for Channel 4 - Low (DSR4_LO)—Offset 1B0h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

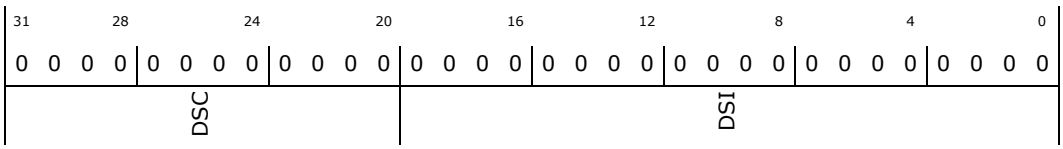
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR4_LO: [BAR] + 1B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.29.110 Dest Scatter Register for Channel 4 - High (DSR4_HI)—Offset 1B4h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

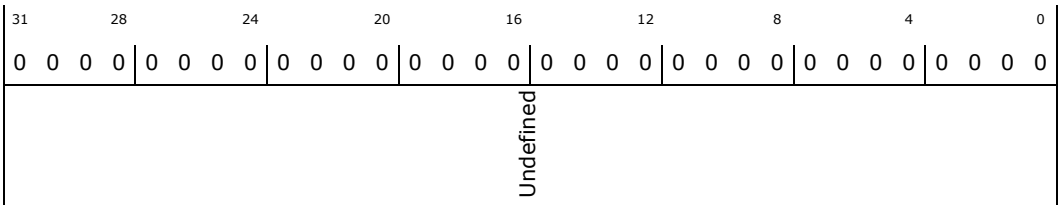
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR4_HI: [BAR] + 1B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.111 Source Address Register for Channel 5 - Low (SAR5_LO)—Offset 1B8h

Refer to the description for register Source Address Register for Channel 0 - Low.

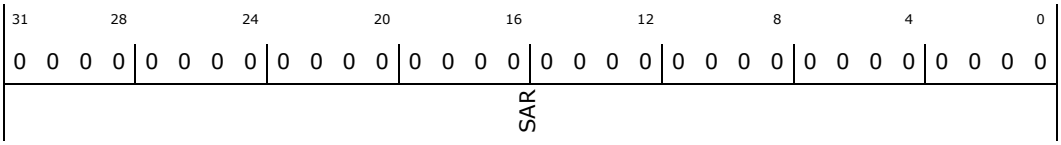
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR5_LO: [BAR] + 1B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.29.112 Source Address Register for Channel 5 - High (SAR5_HI)—Offset 1BCh

Refer to the description for register Source Address Register for Channel 0 - Low.

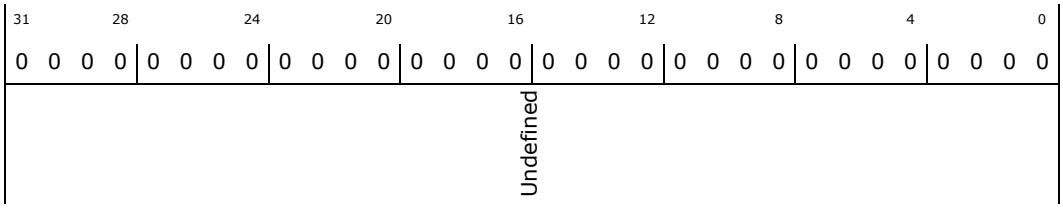
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR5_HI: [BAR] + 1BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.113 Destination Address Register for Channel 5 - Low (DAR5_LO)—Offset 1C0h

Refer to the description for register Destination Address Register for Channel 0 - Low.

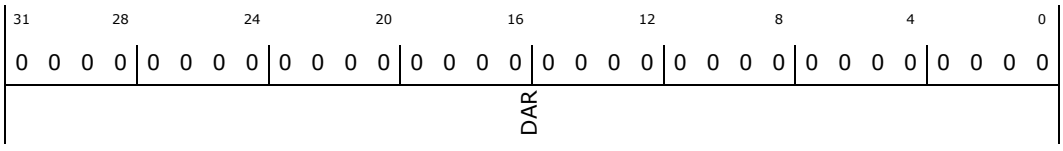
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR5_LO: [BAR] + 1C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.29.114 Destination Address Register for Channel 5 - High (DAR5_HI)—Offset 1C4h

Refer to the description for register Destination Address Register for Channel 0 - Low.

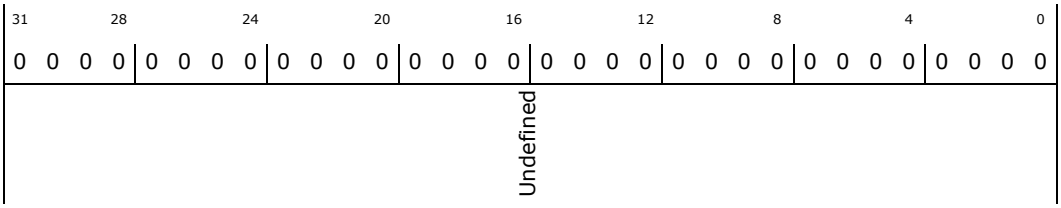
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR5_HI: [BAR] + 1C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.115 Linked List Pointer Register for Channel 5 - Low (LLP5_LO)—Offset 1C8h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

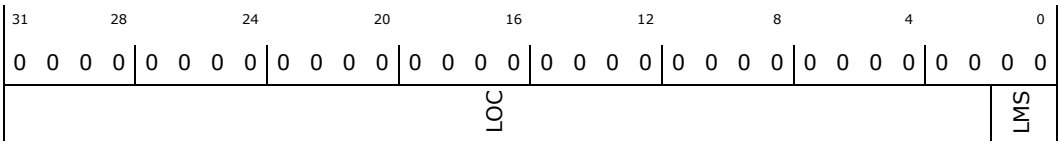
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP5_LO: [BAR] + 1C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.29.116 Linked List Pointer Register for Channel 5 - High (LLP5_HI)—Offset 1CCh

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

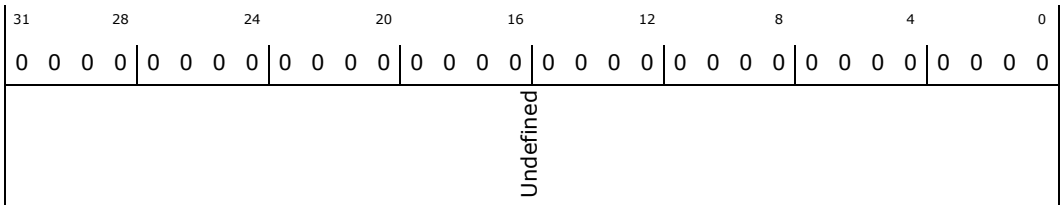
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP5_HI: [BAR] + 1CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.117 Control Register for Channel 5 - Low (CTL5_LO)—Offset 1D0h

Refer to the register description for Control Register for Channel 0 - Low.

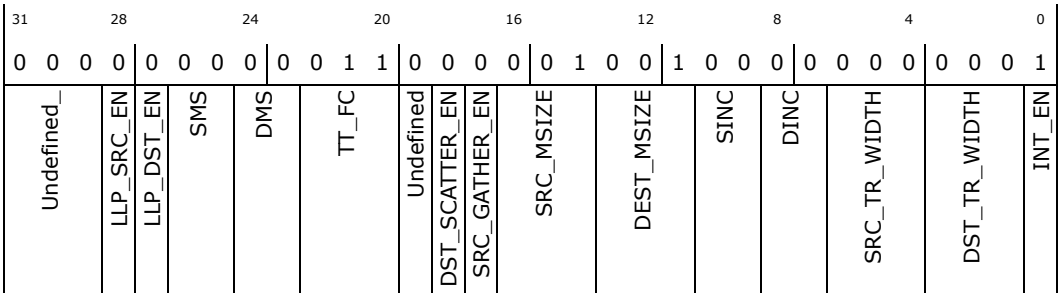
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL5_LO: [BAR] + 1D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.

Bit Range	Default & Access	Description
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.29.118 Control Register for Channel 5 - High (CTL5_HI)—Offset 1D4h

Refer to the register description for Control Register for Channel 0 - Low.

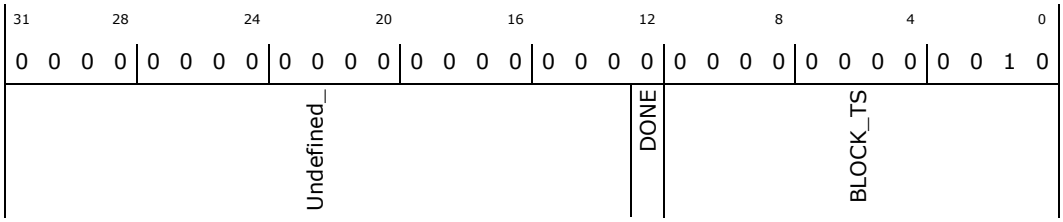
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL5_HI: [BAR] + 1D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.29.119 Source Status Register for Channel 5 - Low (SSTAT5_LO)—Offset 1D8h

Refer to the register description for Source Status Register for Channel 0 - Low.

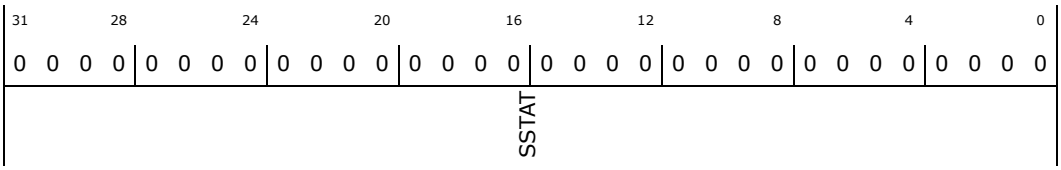
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT5_LO: [BAR] + 1D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.29.120 Source Status Register for Channel 5 - High (SSTAT5_HI)—Offset 1DCh

Refer to the register description for Source Status Register for Channel 0 - Low.

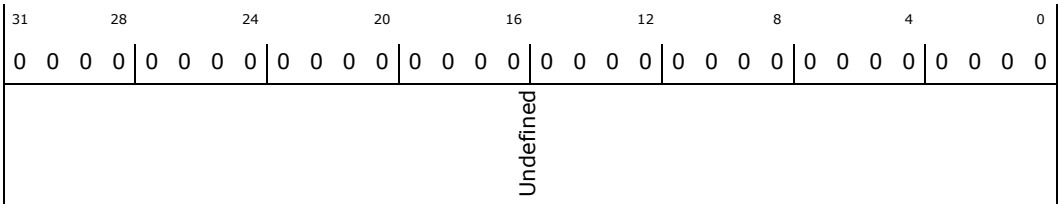
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT5_HI: [BAR] + 1DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.121 Dest Status Register for Channel 5 - Low (DSTAT5_LO)—Offset 1E0h

Refer to the register description for Dest Status Register for Channel 0 - Low.

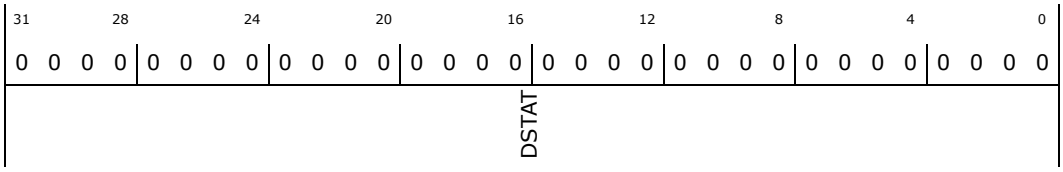
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT5_LO: [BAR] + 1E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

3.29.122 Dest Status Register for Channel 5 - High (DSTAT5_HI)—Offset 1E4h

Refer to the register description for Dest Status Register for Channel 0 - Low.

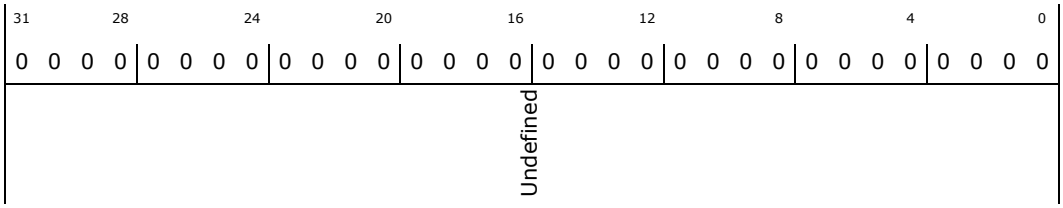
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT5_HI: [BAR] + 1E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.123 Source Status Address Register for Channel 5 - Low (SSTATAR5_LO)—Offset 1E8h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

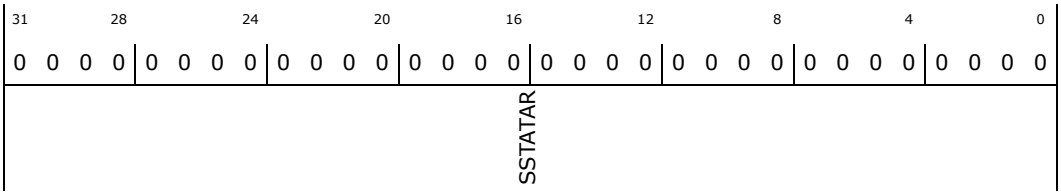
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR5_LO: [BAR] + 1E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.124 Source Status Address Register for Channel 5 - High (SSTATAR5_HI)—Offset 1ECh

Refer to the description for register Source Status Address Register for Channel 0 - Low.

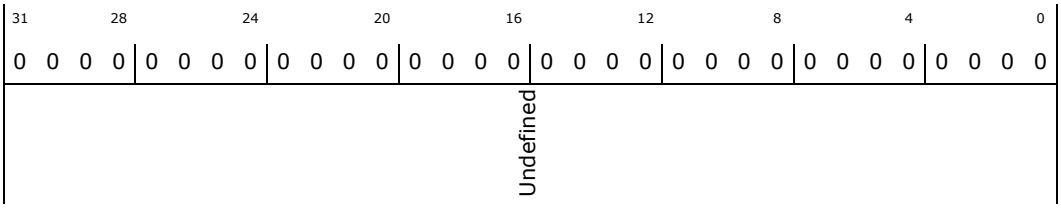
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR5_HI: [BAR] + 1ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.125 Dest Status Address Register for Channel 5 - Low (DSTATAR5_LO)—Offset 1F0h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

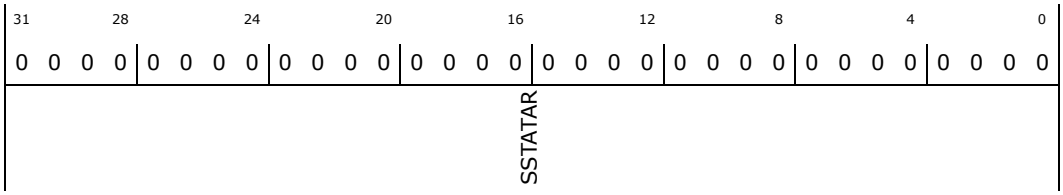
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR5_LO: [BAR] + 1F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.126 Dest Status Address Register for Channel 5 - High (DSTATAR5_HI)—Offset 1F4h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

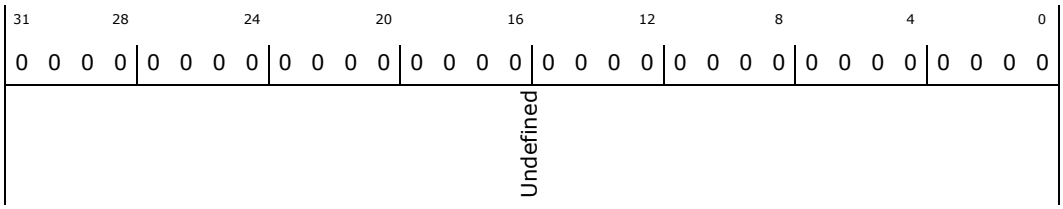
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR5_HI: [BAR] + 1F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.127 Configuration Register for Channel 5 - Low (CFG5_LO)—Offset 1F8h

Refer to the register description for Configuration Register for Channel 0 - Low.

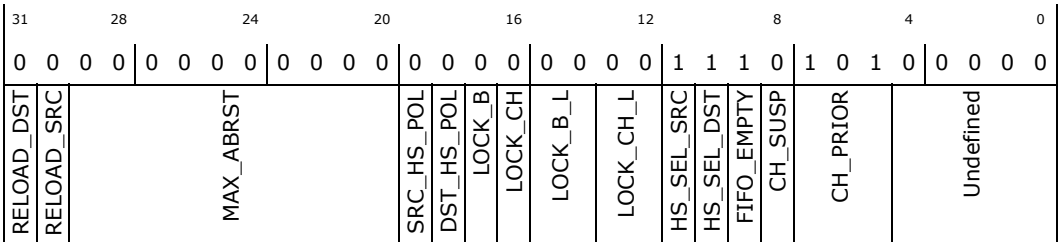
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG5_LO: [BAR] + 1F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000EA0h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface, and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking

Bit Range	Default & Access	Description
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	5h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.29.128 Configuration Register for Channel 5 - High (CFG5_HI)—Offset 1FCh

Refer to the register description for Configuration Register for Channel 0 - Low.

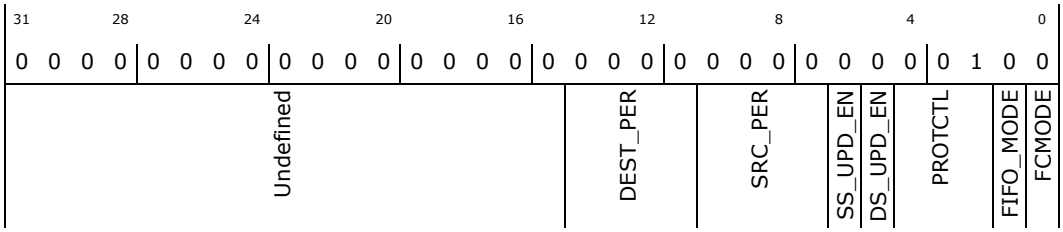
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG5_HI: [BAR] + 1FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.

Bit Range	Default & Access	Description
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the FIFO depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.29.129 Source Gather Register for Channel 5 - Low (SGR5_LO)—Offset 200h

Refer to the register description for Source Gather Register for Channel 0 - Low.

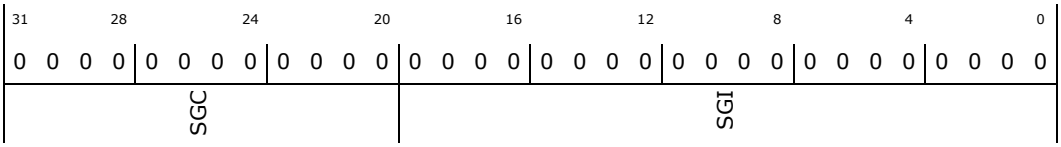
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR5_LO: [BAR] + 200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.29.130 Source Gather Register for Channel 5 - High (SGR5_HI)—Offset 204h

Refer to the register description for Source Gather Register for Channel 0 - Low.

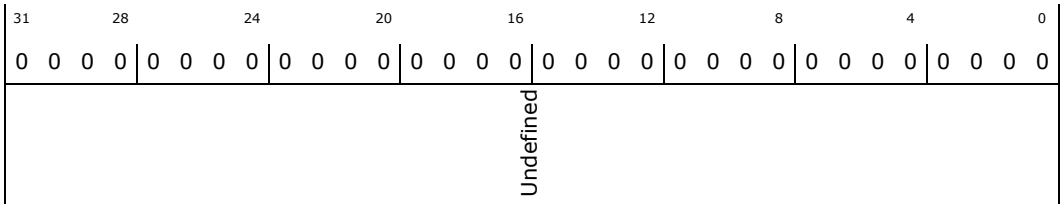
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR5_HI: [BAR] + 204h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.131 Destination Scatter Register for Channel 5 - Low (DSR5_LO)—Offset 208h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

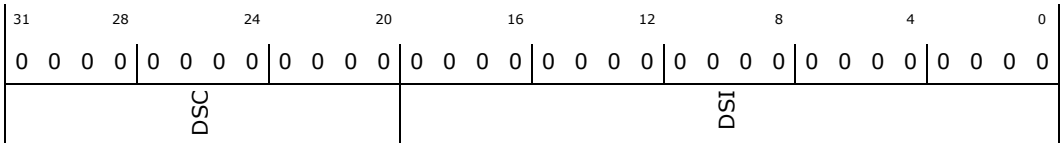
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR5_LO: [BAR] + 208h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.29.132 Dest Scatter Register for Channel 5 - High (DSR5_HI)—Offset 20Ch

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

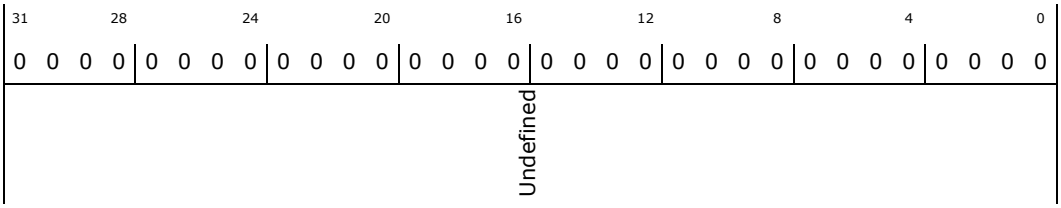
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR5_HI: [BAR] + 20Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.133 Source Address Register for Channel 6 - Low (SAR6_LO)—Offset 210h

Refer to the description for register Source Address Register for Channel 0 - Low.

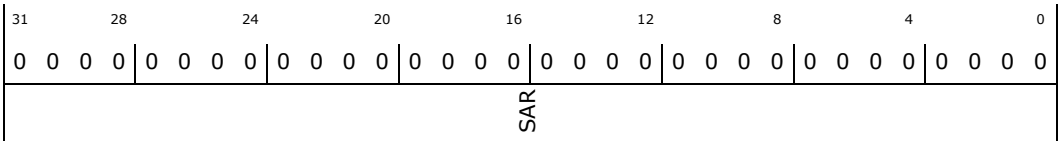
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR6_LO: [BAR] + 210h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.29.134 Source Address Register for Channel 6 - High (SAR6_HI)—Offset 214h

Refer to the description for register Source Address Register for Channel 0 - Low.

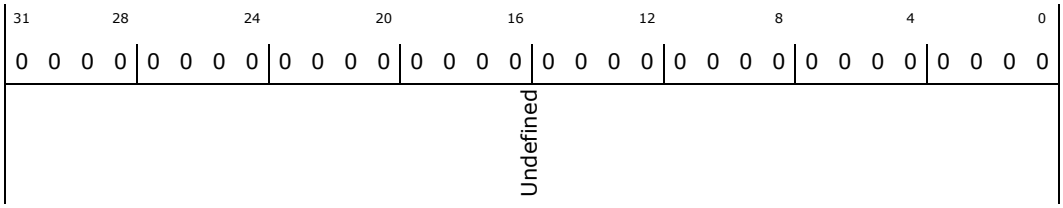
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR6_HI: [BAR] + 214h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.135 Destination Address Register for Channel 6 - Low (DAR6_LO)—Offset 218h

Refer to the description for register Destination Address Register for Channel 0 - Low.

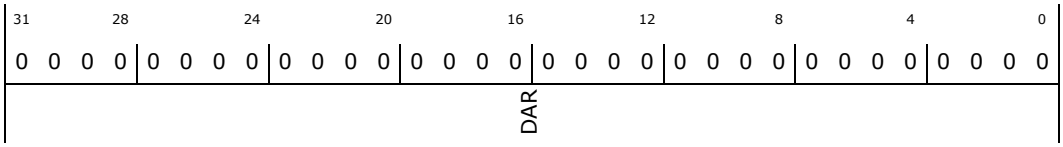
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR6_LO: [BAR] + 218h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.29.136 Destination Address Register for Channel 6 - High (DAR6_HI)—Offset 21Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

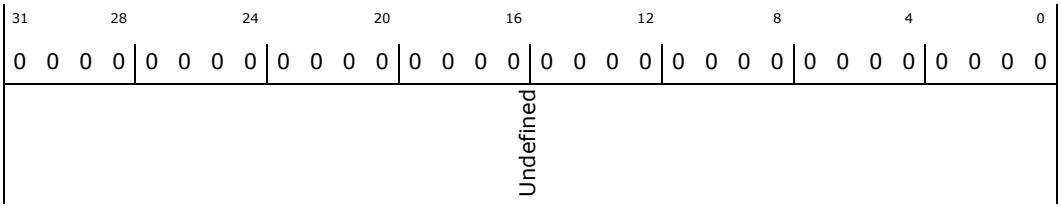
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR6_HI: [BAR] + 21Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.137 Linked List Pointer Register for Channel 6 - Low (LLP6_LO)—Offset 220h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

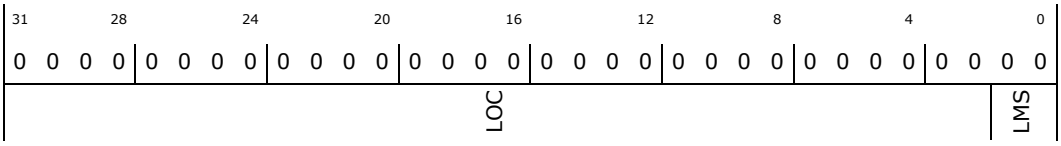
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP6_LO: [BAR] + 220h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.29.138 Linked List Pointer Register for Channel 6 - High (LLP6_HI)—Offset 224h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

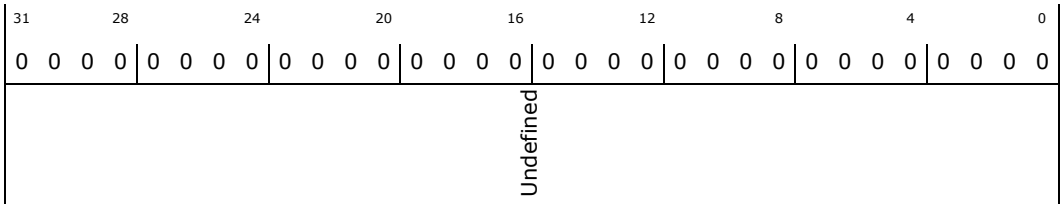
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP6_HI: [BAR] + 224h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.139 Control Register for Channel 6 - Low (CTL6_LO)—Offset 228h

Refer to the register description for Control Register for Channel 0 - Low.

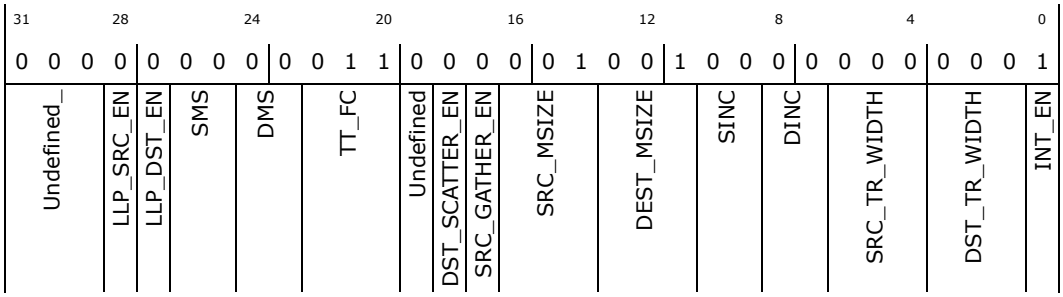
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL6_LO: [BAR] + 228h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.29.140 Control Register for Channel 6 - High (CTL6_HI)—Offset 22Ch

Refer to the register description for Control Register for Channel 0 - Low.

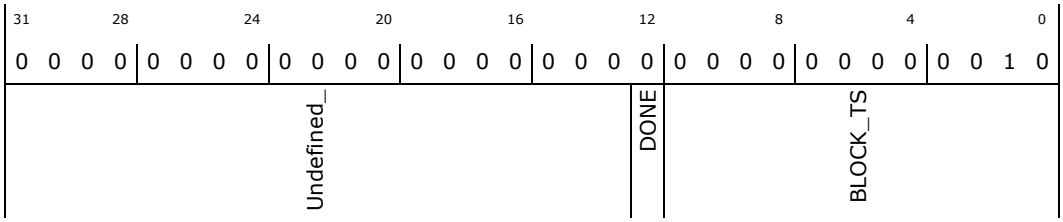
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL6_HI: [BAR] + 22Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.29.141 Source Status Register for Channel 6 - Low (SSTAT6_LO)—Offset 230h

Refer to the register description for Source Status Register for Channel 0 - Low.

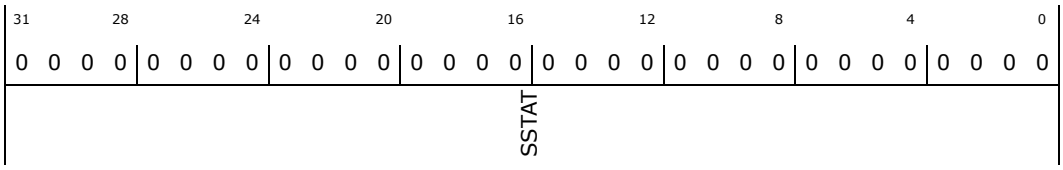
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT6_LO: [BAR] + 230h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.29.142 Source Status Register for Channel 6 - High (SSTAT6_HI)—Offset 234h

Refer to the register description for Source Status Register for Channel 0 - Low.

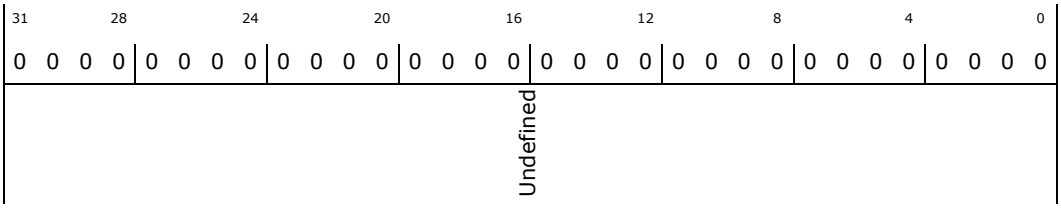
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT6_HI: [BAR] + 234h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.143 Dest Status Register for Channel 6 - Low (DSTAT6_LO)—Offset 238h

Refer to the register description for Dest Status Register for Channel 0 - Low.

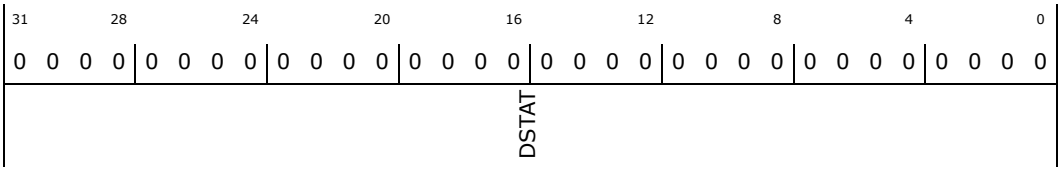
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT6_LO: [BAR] + 238h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

3.29.144 Dest Status Register for Channel 6 - High (DSTAT6_HI)—Offset 23Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

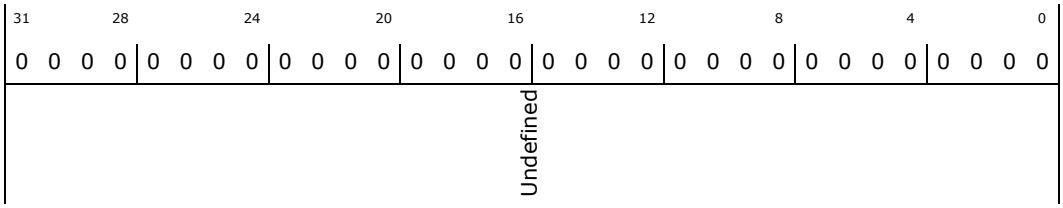
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT6_HI: [BAR] + 23Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.145 Source Status Address Register for Channel 6 - Low (SSTATAR6_LO)—Offset 240h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

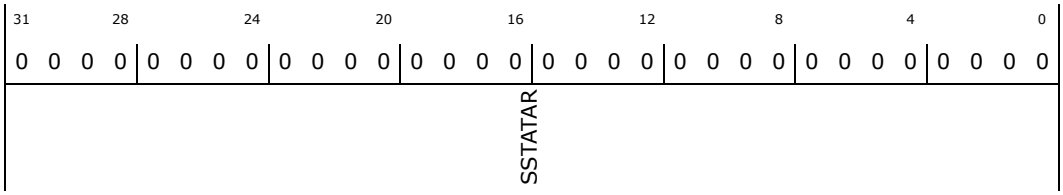
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR6_LO: [BAR] + 240h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.146 Source Status Address Register for Channel 6 - High (SSTATAR6_HI)—Offset 244h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

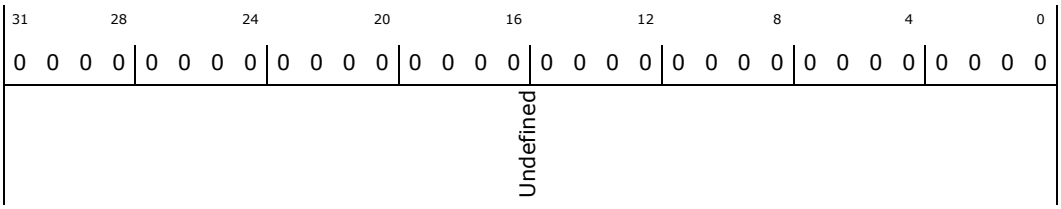
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR6_HI: [BAR] + 244h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.147 Dest Status Address Register for Channel 6 - Low (DSTATAR6_LO)—Offset 248h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

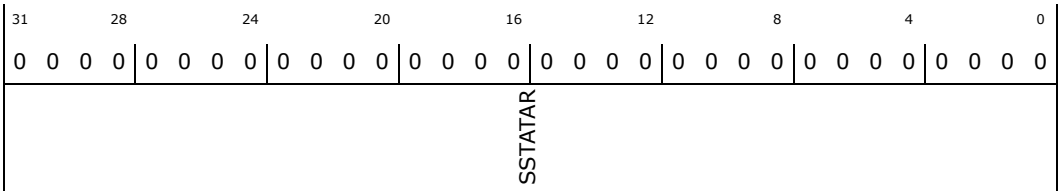
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR6_LO: [BAR] + 248h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.148 Dest Status Address Register for Channel 6 - High (DSTATAR6_HI)—Offset 24Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

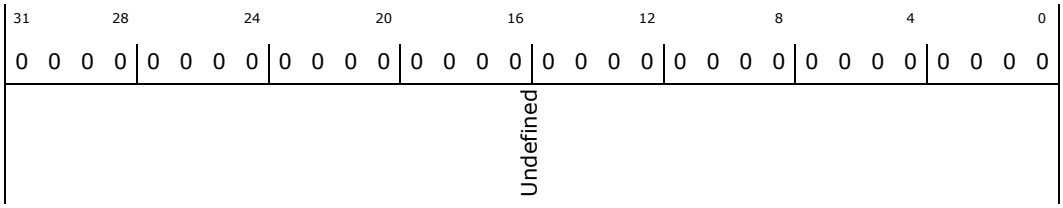
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR6_HI: [BAR] + 24Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.149 Configuration Register for Channel 6 - Low (CFG6_LO)—Offset 250h

Refer to the register description for Configuration Register for Channel 0 - Low.

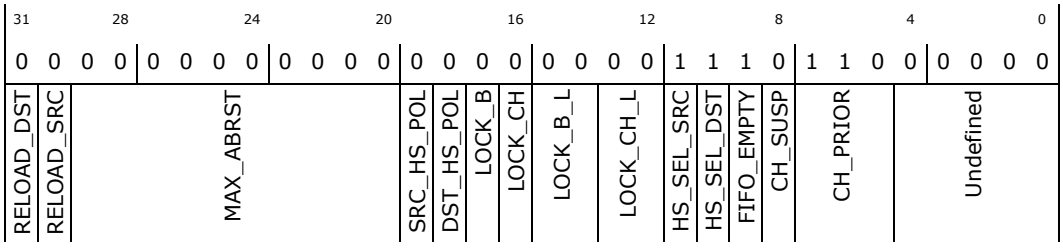
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG6_LO: [BAR] + 250h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000EC0h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.

Bit Range	Default & Access	Description
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	6h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.29.150 Configuration Register for Channel 6 - High (CFG6_HI)—Offset 254h

Refer to the register description for Configuration Register for Channel 0 - Low.

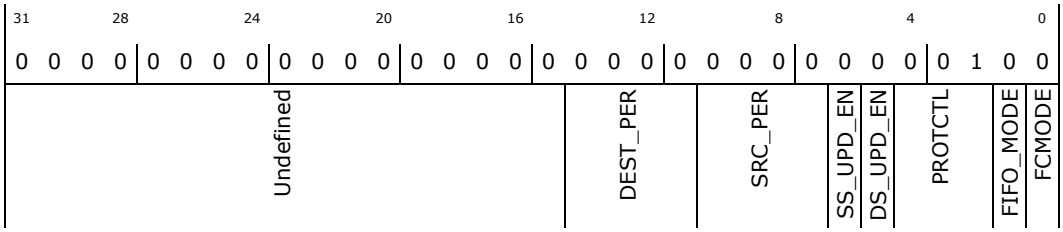
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG6_HI: [BAR] + 254h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.

Bit Range	Default & Access	Description
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.29.151 Source Gather Register for Channel 6 - Low (SGR6_LO)—Offset 258h

Refer to the register description for Source Gather Register for Channel 0 - Low.

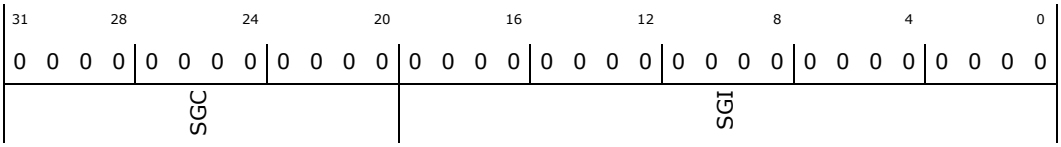
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR6_LO: [BAR] + 258h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.29.152 Source Gather Register for Channel 6 - High (SGR6_HI)—Offset 25Ch

Refer to the register description for Source Gather Register for Channel 0 - Low.

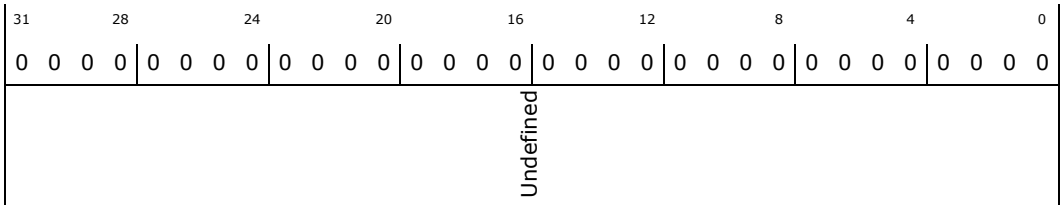
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR6_HI: [BAR] + 25Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.153 Destination Scatter Register for Channel 6 - Low (DSR6_LO)—Offset 260h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

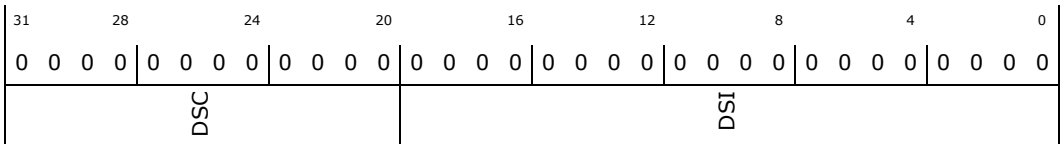
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR6_LO: [BAR] + 260h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.29.154 Dest Scatter Register for Channel 6 - High (DSR6_HI)—Offset 264h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

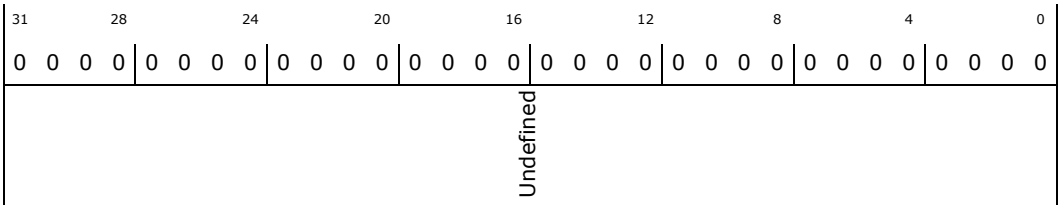
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR6_HI: [BAR] + 264h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.155 Source Address Register for Channel 7 - Low (SAR7_LO)—Offset 268h

Refer to the description for register Source Address Register for Channel 0 - Low.

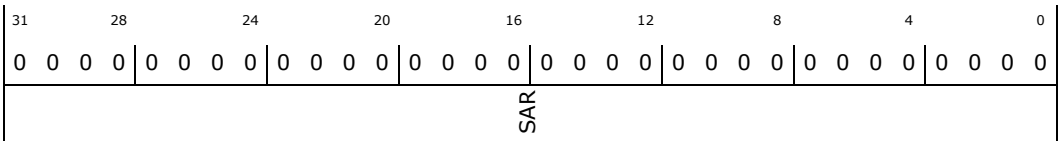
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR7_LO: [BAR] + 268h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

3.29.156 Source Address Register for Channel 7 - High (SAR7_HI)—Offset 26Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

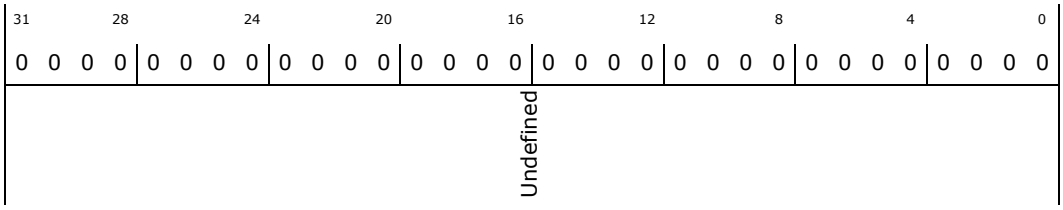
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR7_HI: [BAR] + 26Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.157 Destination Address Register for Channel 7 - Low (DAR7_LO)—Offset 270h

Refer to the description for register Destination Address Register for Channel 0 - Low.

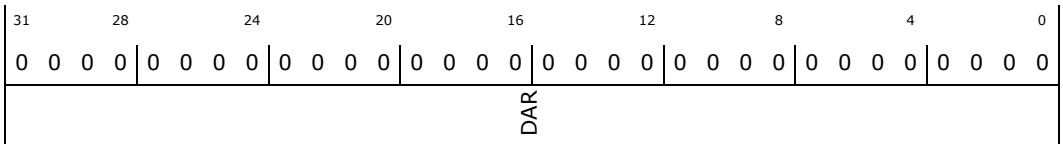
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR7_LO: [BAR] + 270h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

3.29.158 Destination Address Register for Channel 7 - High (DAR7_HI)—Offset 274h

Refer to the description for register Destination Address Register for Channel 0 - Low.

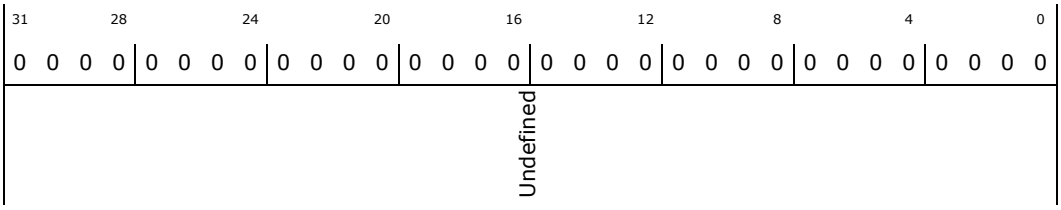
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR7_HI: [BAR] + 274h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.159 Linked List Pointer Register for Channel 7 - Low (LLP7_LO)—Offset 278h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

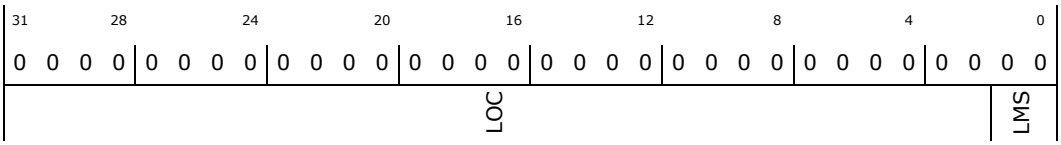
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP7_LO: [BAR] + 278h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

3.29.160 Linked List Pointer Register for Channel 7 - High (LLP7_HI)—Offset 27Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

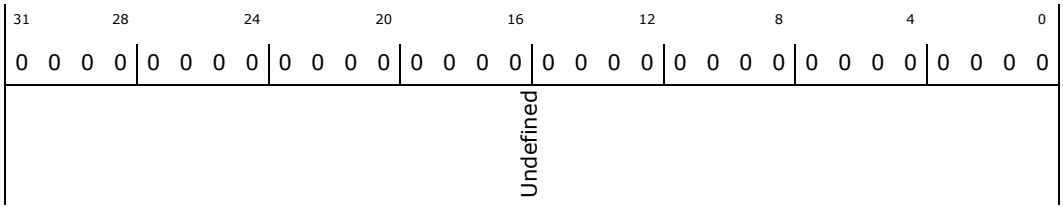
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LLP7_HI: [BAR] + 27Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.161 Control Register for Channel 7 - Low (CTL7_LO)—Offset 280h

Refer to the register description for Control Register for Channel 0 - Low.

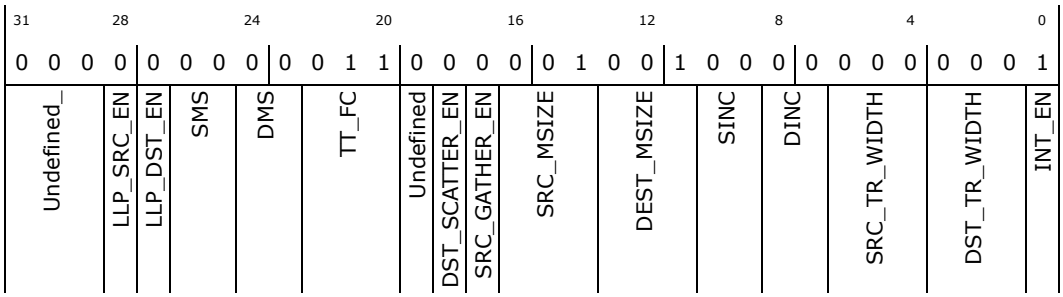
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL7_LO: [BAR] + 280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.

Bit Range	Default & Access	Description
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

3.29.162 Control Register for Channel 7 - High (CTL7_HI)—Offset 284h

Refer to the register description for Control Register for Channel 0 - Low.

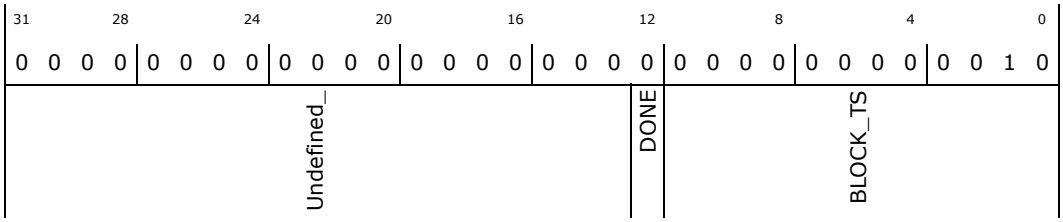
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL7_HI: [BAR] + 284h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

3.29.163 Source Status Register for Channel 7 - Low (SSTAT7_LO)—Offset 288h

Refer to the register description for Source Status Register for Channel 0 - Low.

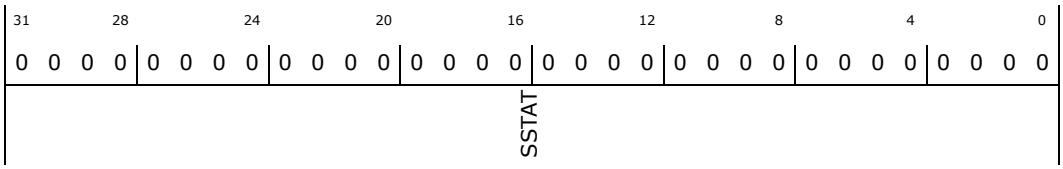
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT7_LO: [BAR] + 288h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

3.29.164 Source Status Register for Channel 7 - High (SSTAT7_HI)—Offset 28Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

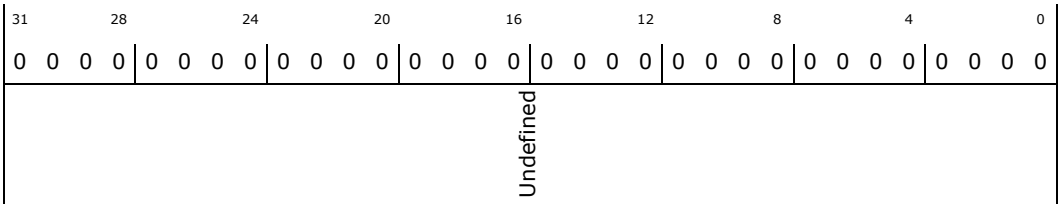
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT7_HI: [BAR] + 28Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.165 Dest Status Register for Channel 7 - Low (DSTAT7_LO)—Offset 290h

Refer to the register description for Dest Status Register for Channel 0 - Low.

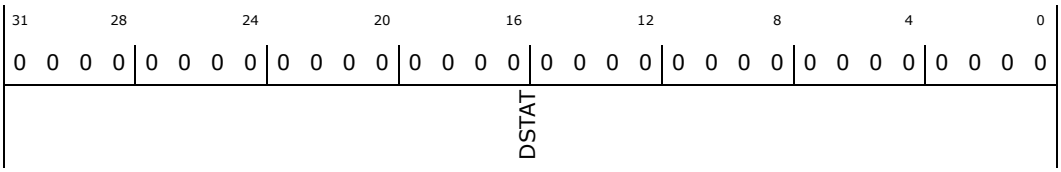
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT7_LO: [BAR] + 290h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

3.29.166 Dest Status Register for Channel 7 - High (DSTAT7_HI)—Offset 294h

Refer to the register description for Dest Status Register for Channel 0 - Low.

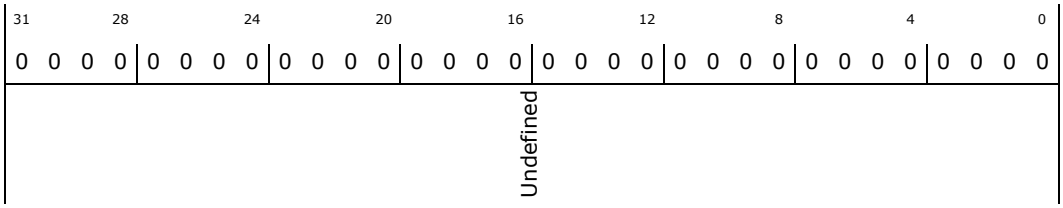
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT7_HI: [BAR] + 294h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.167 Source Status Address Register for Channel 7 - Low (SSTATAR7_LO)—Offset 298h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

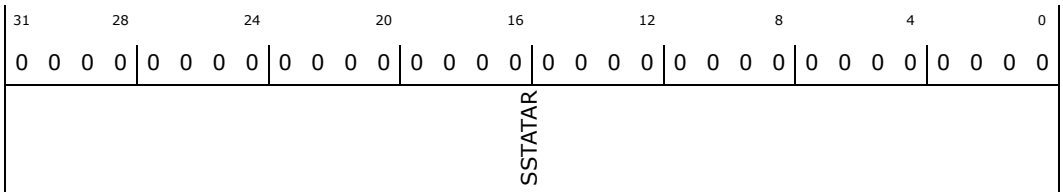
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR7_LO: [BAR] + 298h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.168 Source Status Address Register for Channel 7 - High (SSTATAR7_HI)—Offset 29Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

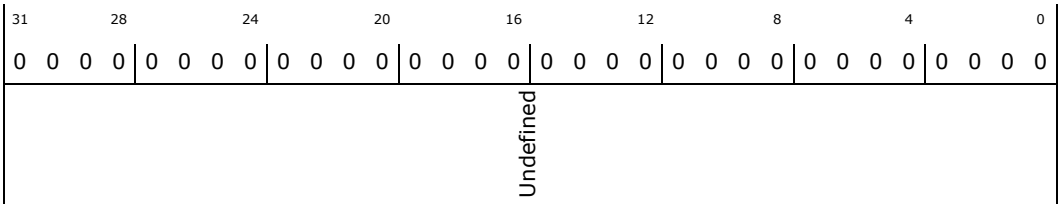
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR7_HI: [BAR] + 29Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.169 Dest Status Address Register for Channel 7 - Low (DSTATAR7_LO)—Offset 2A0h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

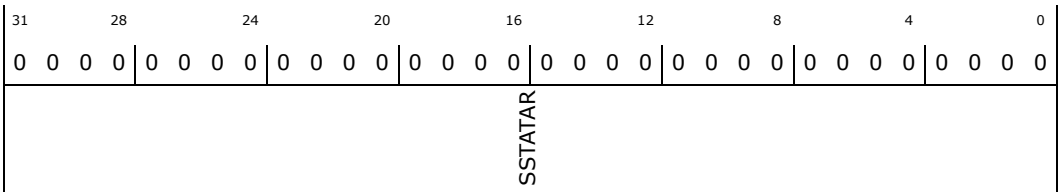
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR7_LO: [BAR] + 2A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

3.29.170 Dest Status Address Register for Channel 7 - High (DSTATAR7_HI)—Offset 2A4h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

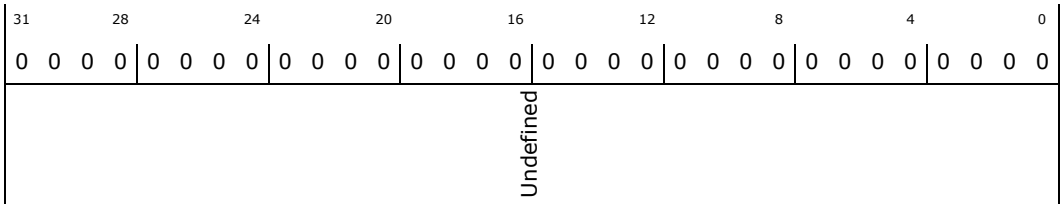
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR7_HI: [BAR] + 2A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** RESERVED

3.29.171 Configuration Register for Channel 7 - Low (CFG7_LO)—Offset 2A8h

Refer to the register description for Configuration Register for Channel 0 - Low.

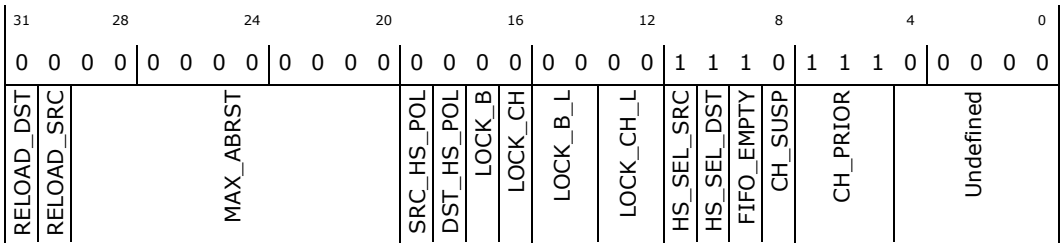
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

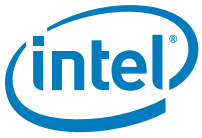
CFG7_LO: [BAR] + 2A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000EE0h



Bit Range	Default & Access	Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.



Bit Range	Default & Access	Description
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	7h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

3.29.172 Configuration Register for Channel 7 - High (CFG7_HI)—Offset 2ACh

Refer to the register description for Configuration Register for Channel 0 - Low.

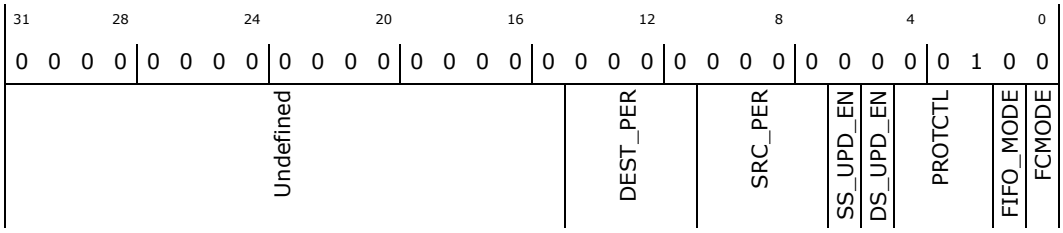
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG7_HI: [BAR] + 2ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

3.29.173 Source Gather Register for Channel 7 - Low (SGR7_LO)—Offset 2B0h

Refer to the register description for Source Gather Register for Channel 0 - Low.

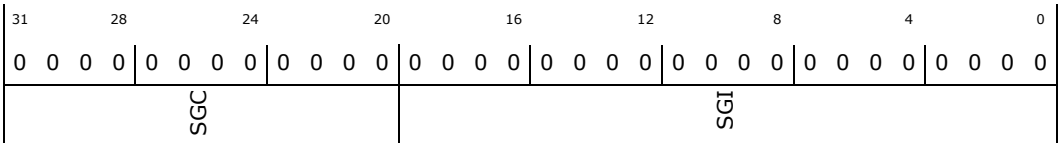
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR7_LO: [BAR] + 2B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries. Refer to the DesignWare DW_ahb_dmac Databook for further details.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

3.29.174 Source Gather Register for Channel 7 - High (SGR7_HI)—Offset 2B4h

Refer to the register description for Source Gather Register for Channel 0 - Low.

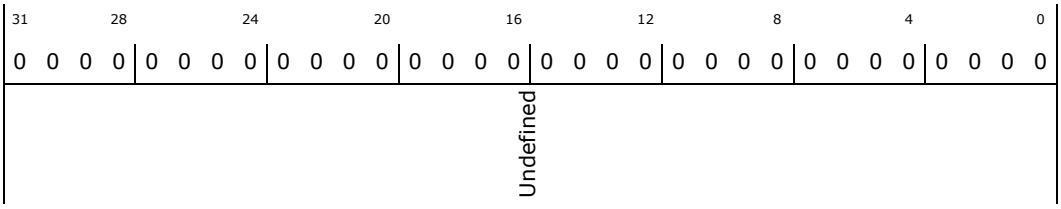
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR7_HI: [BAR] + 2B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.175 Destination Scatter Register for Channel 7 - Low (DSR7_LO)—Offset 2B8h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

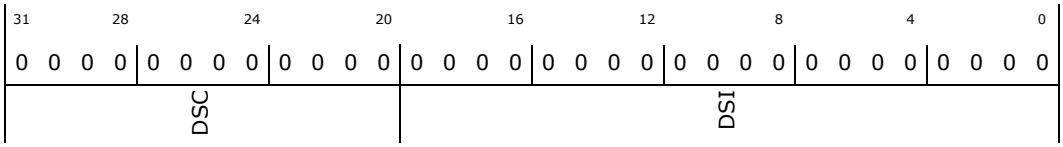
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR7_LO: [BAR] + 2B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

3.29.176 Dest Scatter Register for Channel 7 - High (DSR7_HI)—Offset 2BCh

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

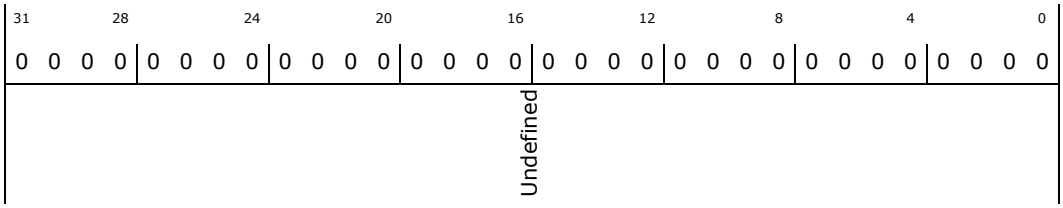
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR7_HI: [BAR] + 2BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.177 Interrupt Raw Status Registers - Low (RawTfr_LO)—Offset 2C0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel; for example, RawTfr[2] is the Channel 2 raw transfer complete interrupt.

Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

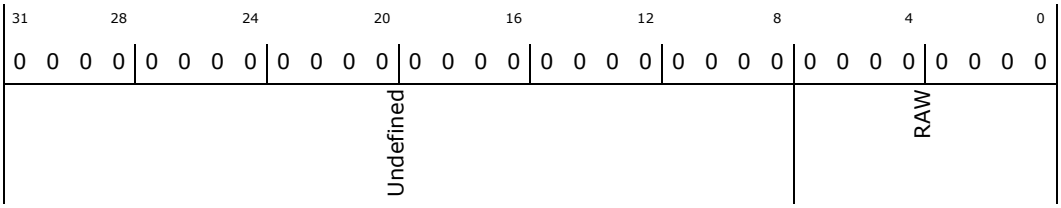
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawTfr_LO: [BAR] + 2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

3.29.178 Interrupt Raw Status Registers - High (RawTfr_HI)—Offset 2C4h

Refer to the description for Interrupt Raw Status Registers - Low.

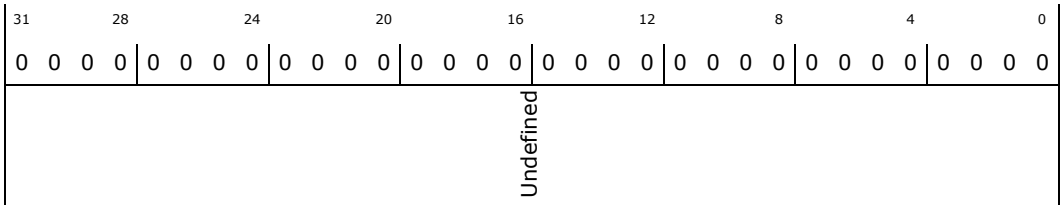
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawTfr_HI: [BAR] + 2C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.179 Interrupt Raw Status Registers - Low (RawBlock_LO)—Offset 2C8h

Refer to the description of the register with short name RawTfr_LO.

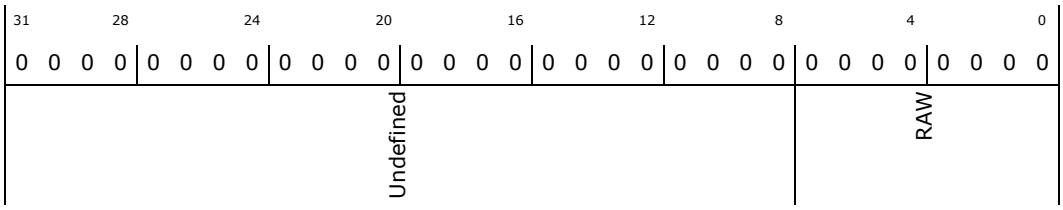
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawBlock_LO: [BAR] + 2C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

3.29.180 Interrupt Raw Status Registers - High (RawBlock_HI)—Offset 2CCh

Refer to the description of the register with short name RawTfr_LO.

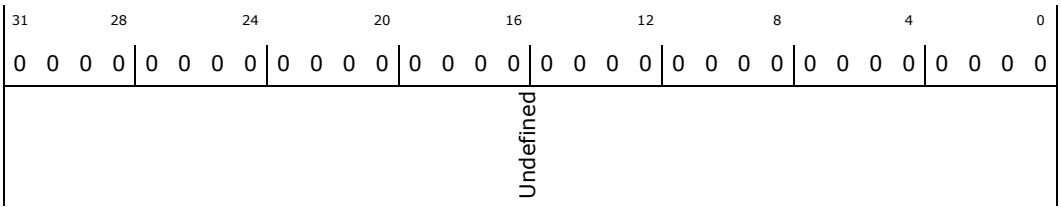
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawBlock_HI: [BAR] + 2CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.181 Interrupt Raw Status Registers - Low (RawSrcTran_LO)—Offset 2D0h

Refer to the description of the register with short name RawTfr_LO.

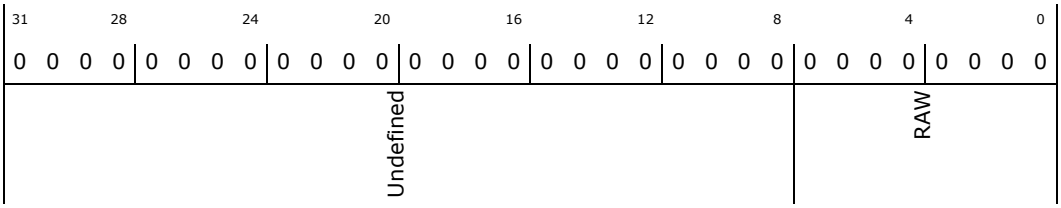
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawSrcTran_LO: [BAR] + 2D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

3.29.182 Interrupt Raw Status Registers - High (RawSrcTran_HI)—Offset 2D4h

Refer to the description of the register with short name RawTfr_LO.

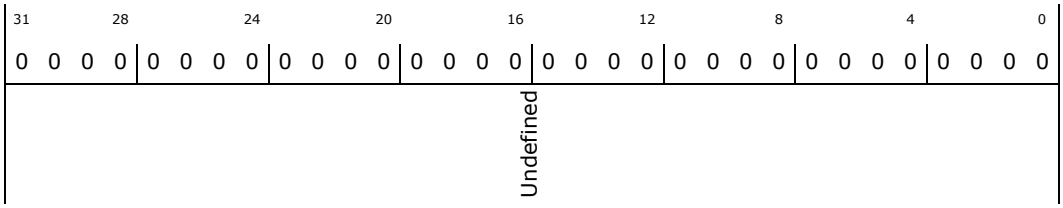
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawSrcTran_HI: [BAR] + 2D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.183 Interrupt Raw Status Registers - Low (RawDstTran_LO)—Offset 2D8h

Refer to the description of the register with short name RawTfr_LO.

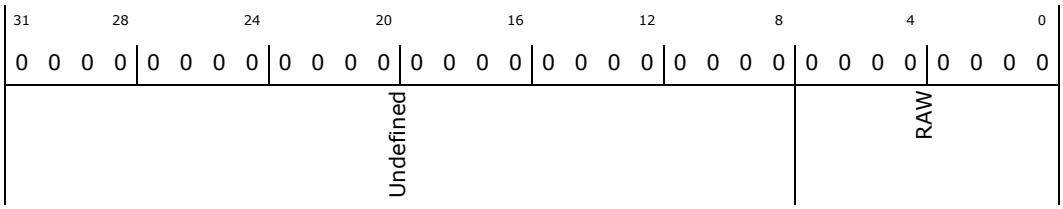
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawDstTran_LO: [BAR] + 2D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

3.29.184 Interrupt Raw Status Registers - High (RawDstTran_HI)—Offset 2DCh

Refer to the description of the register with short name RawTfr_LO.

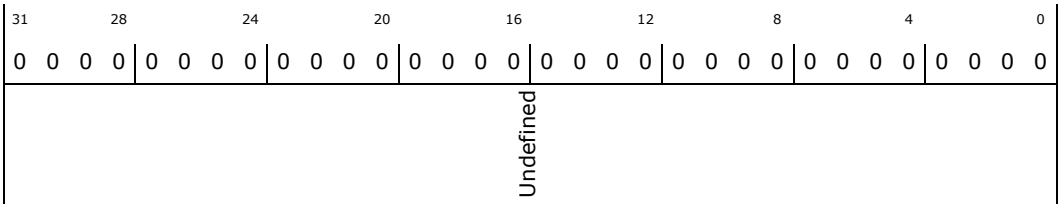
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawDstTran_HI: [BAR] + 2DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.185 Interrupt Raw Status Registers - Low (RawErr_LO)—Offset 2E0h

Refer to the description of the register with short name RawTfr_LO.

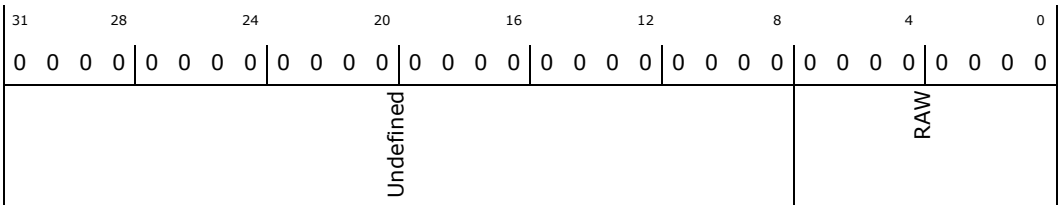
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawErr_LO: [BAR] + 2E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

3.29.186 Interrupt Raw Status Registers - High (RawErr_HI)—Offset 2E4h

Refer to the description of the register with short name RawTfr_LO.

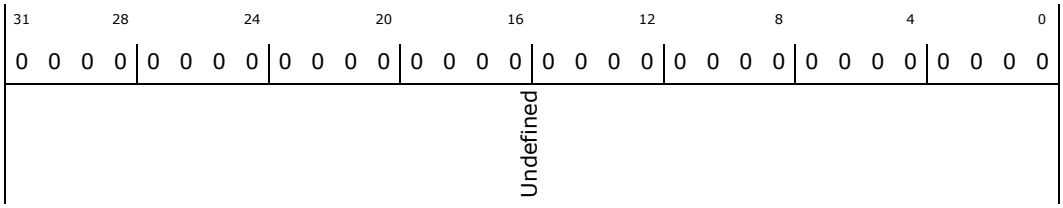
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawErr_HI: [BAR] + 2E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.187 Interrupt Status Registers - Low (StatusTfr_LO)—Offset 2E8h

Refer to the description for register StatusTfr_HI.

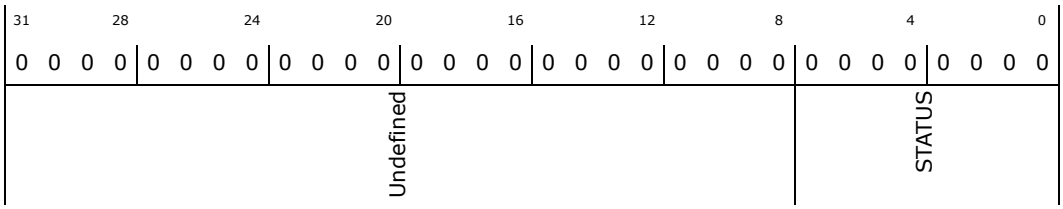
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusTfr_LO: [BAR] + 2E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

3.29.188 Interrupt Status Registers - High (StatusTfr_HI)—Offset 2ECh

All interrupt events from all channels are stored in these Interrupt Status registers after masking: StatusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel; for example, StatusTfr[2] is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DW_ahb_dmac.

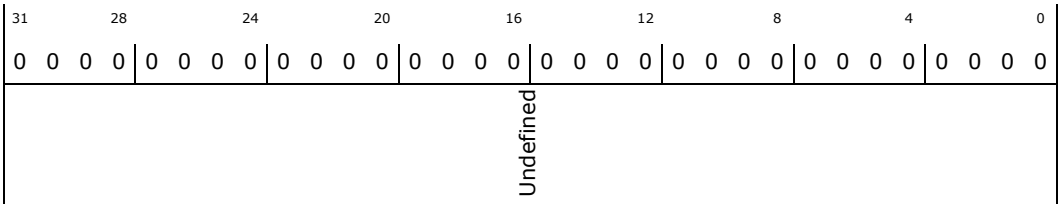
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusTfr_HI: [BAR] + 2ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.189 Interrupt Status Registers - Low (StatusBlock_LO)—Offset 2F0h

Refer to the description for register StatusTfr_HI.

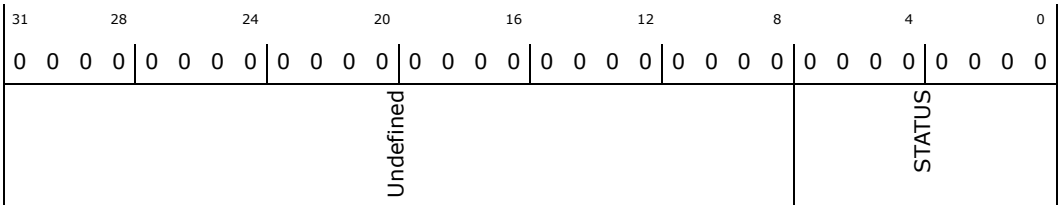
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusBlock_LO: [BAR] + 2F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

3.29.190 Interrupt Status Registers - High (StatusBlock_HI)—Offset 2F4h

Refer to the description for register StatusTfr_HI.

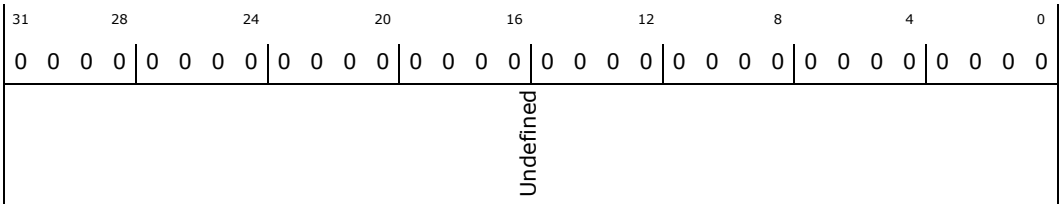
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusBlock_HI: [BAR] + 2F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.191 Interrupt Status Registers - Low (StatusSrcTran_LO)—Offset 2F8h

Refer to the description for register StatusTfr_HI.

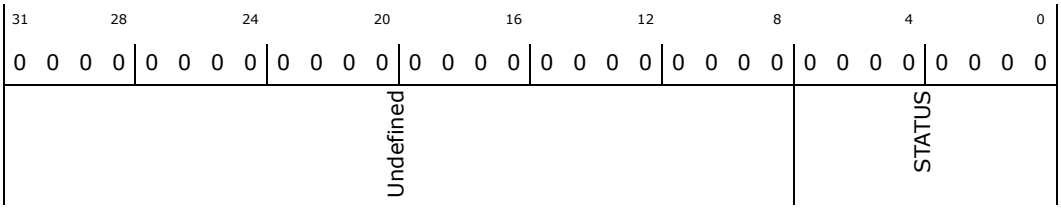
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusSrcTran_LO: [BAR] + 2F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

3.29.192 Interrupt Status Registers - High (StatusSrcTran_HI)—Offset 2FCh

Refer to the description for register StatusTfr_HI.

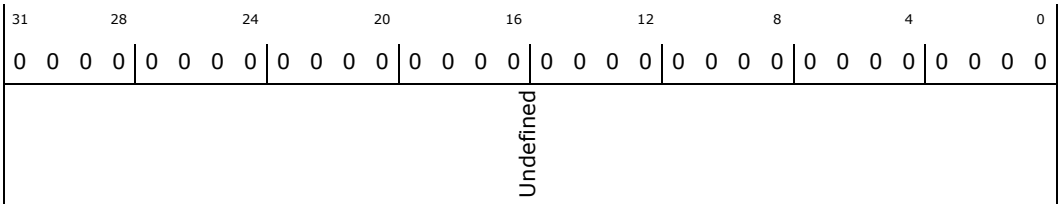
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusSrcTran_HI: [BAR] + 2FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.193 Interrupt Status Registers - Low (StatusDstTran_LO)—Offset 300h

Refer to the description for register StatusTfr_HI.

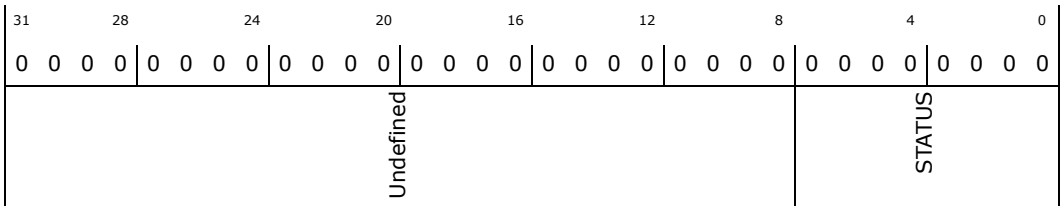
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusDstTran_LO: [BAR] + 300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

3.29.194 Interrupt Status Registers - High (StatusDstTran_HI)—Offset 304h

Refer to the description for register StatusTfr_HI.

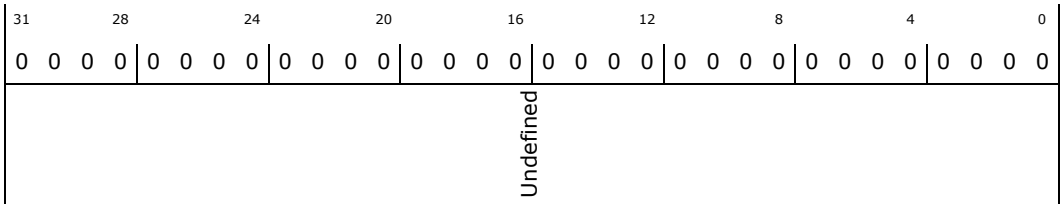
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusDstTran_HI: [BAR] + 304h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.195 Interrupt Status Registers - Low (StatusErr_LO)—Offset 308h

Refer to the description for register StatusTfr_HI.

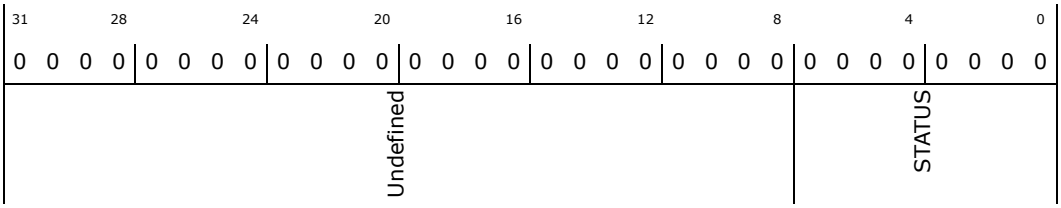
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusErr_LO: [BAR] + 308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

3.29.196 Interrupt Status Registers - High (StatusErr_HI)—Offset 30Ch

Refer to the description for register StatusTfr_HI.

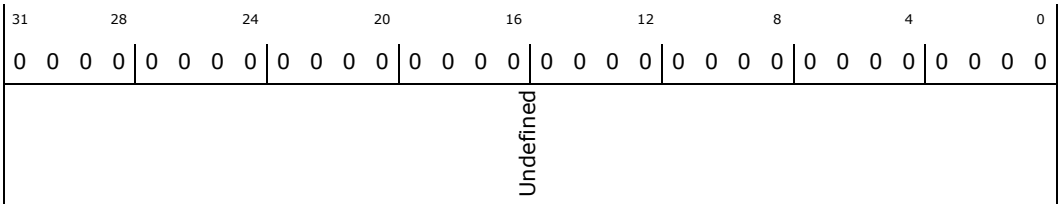
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusErr_HI: [BAR] + 30Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.197 Interrupt Mask Registers - Low (MaskTfr_LO)—Offset 310h

Refer to the description for register MaskBlock_LO.

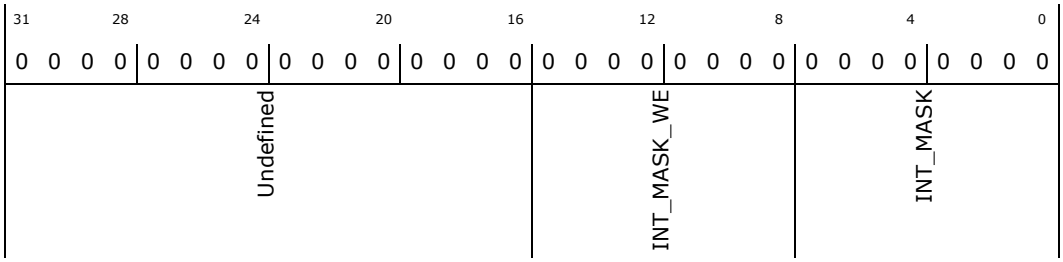
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskTfr_LO: [BAR] + 310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h RW	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

3.29.198 Interrupt Mask Registers - High (MaskTfr_HI)—Offset 314h

Refer to the description for register MaskBlock_LO.

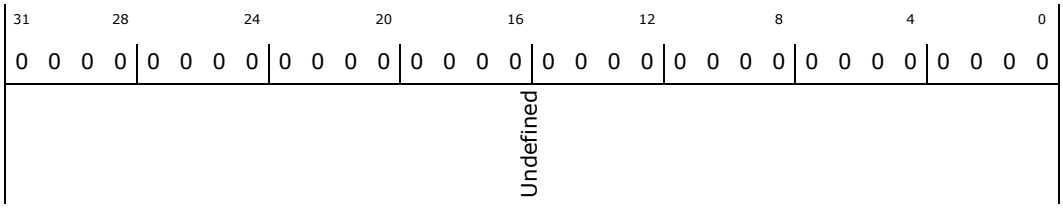
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskTfr_HI: [BAR] + 314h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.199 Interrupt Mask Registers - Low (MaskBlock_LO)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel; for example, MaskTfr[2] is the mask bit for the Channel 2 transfer complete interrupt. Refer to the DesignWare SW_ahb_dmac Databook for details.

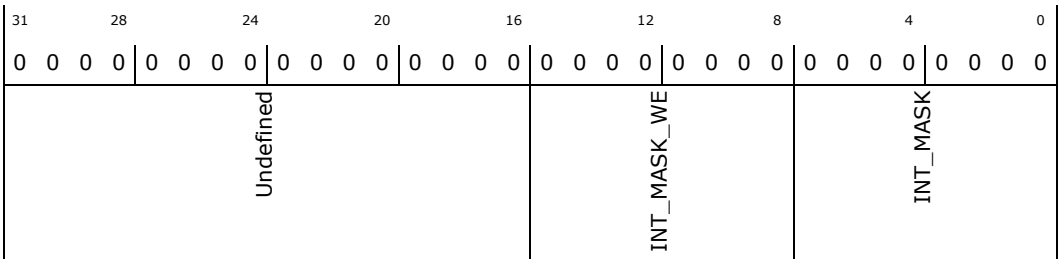
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskBlock_LO: [BAR] + 318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt Mask • 0 = masked • 1 = unmasked

3.29.200 Interrupt Mask Registers - High (MaskBlock_HI)—Offset 31Ch

Refer to the description for register MaskBlock_LO.

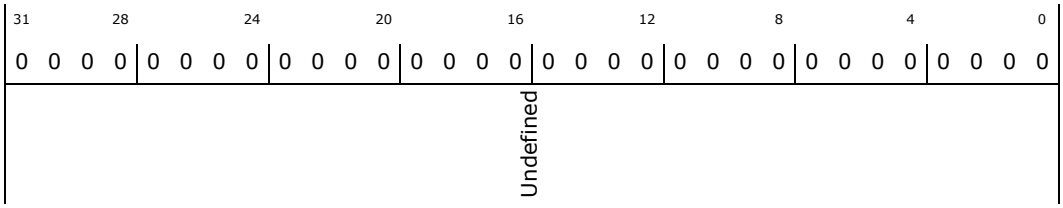
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskBlock_HI: [BAR] + 31Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.201 Interrupt Mask Registers - Low (MaskSrcTran_LO)—Offset 320h

Refer to the description for register MaskBlock_LO.

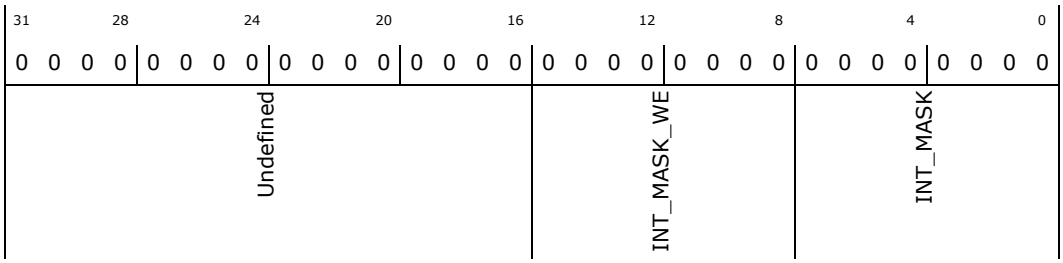
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskSrcTran_LO: [BAR] + 320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

3.29.202 Interrupt Mask Registers - High (MaskSrcTran_HI)—Offset 324h

Refer to the description for register MaskBlock_LO.

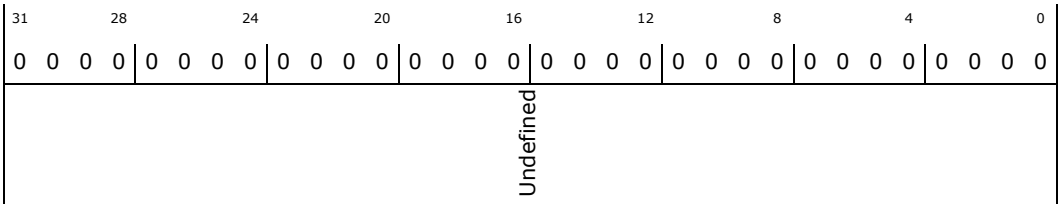
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskSrcTran_HI: [BAR] + 324h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.203 Interrupt Mask Registers - Low (MaskDstTran_LO)—Offset 328h

Refer to the description for register MaskBlock_LO.

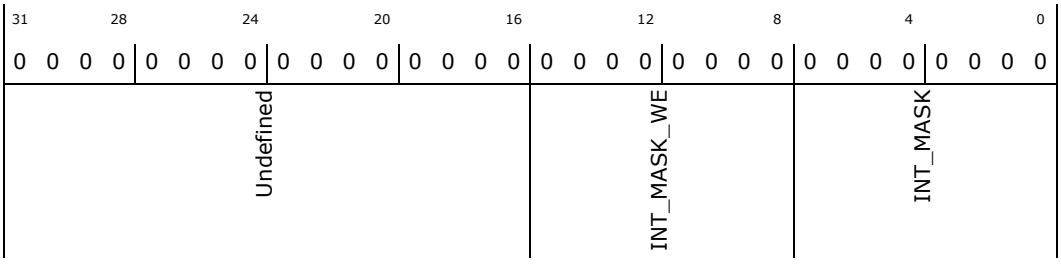
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskDstTran_LO: [BAR] + 328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Description
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

3.29.204 Interrupt Mask Registers - High (MaskDstTran_HI)—Offset 32Ch

Refer to the description for register MaskBlock_LO.

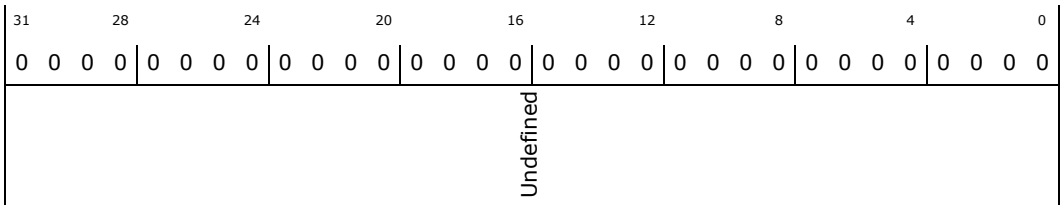
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskDstTran_HI: [BAR] + 32Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.205 Interrupt Mask Registers - Low (MaskErr_LO)—Offset 330h

Refer to the description for register MaskBlock_LO.

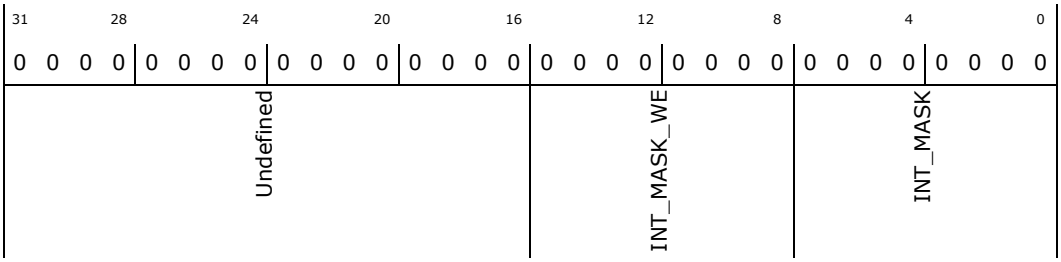
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskErr_LO: [BAR] + 330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

3.29.206 Interrupt Mask Registers - High (MaskErr_HI)—Offset 334h

Refer to the description for register MaskBlock_LO.

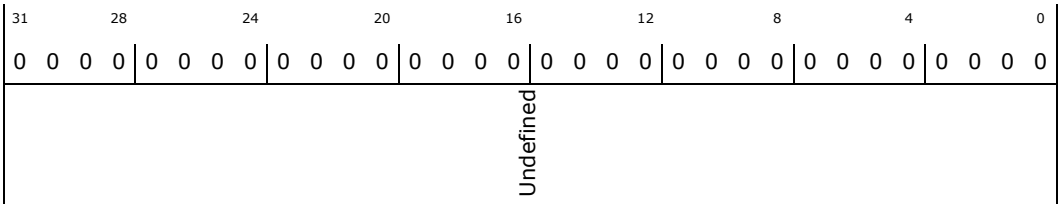
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskErr_HI: [BAR] + 334h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.207 Interrupt Clear Registers - Low (ClearTfr_LO)—Offset 338h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel; for example, ClearTfr[2] is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

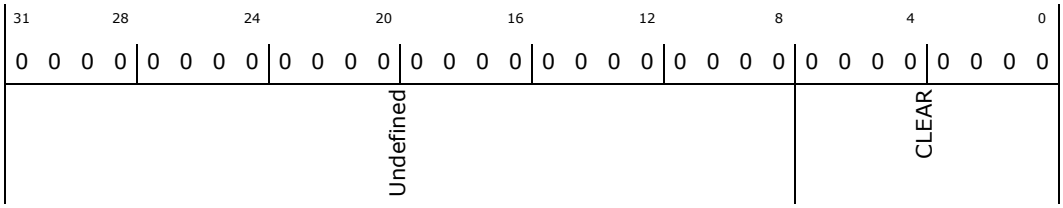
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearTfr_LO: [BAR] + 338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

3.29.208 Interrupt Clear Registers - High (ClearTfr_HI)—Offset 33Ch

Refer to the description for register ClearTfr_HI.

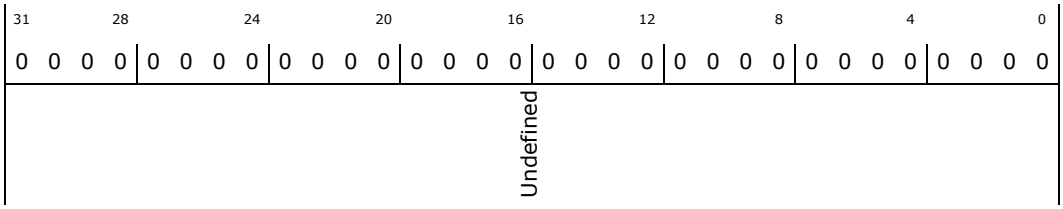
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearTfr_HI: [BAR] + 33Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.209 Interrupt Clear Registers - Low (ClearBlock_LO)—Offset 340h

Refer to the description for register ClearTfr_HI.

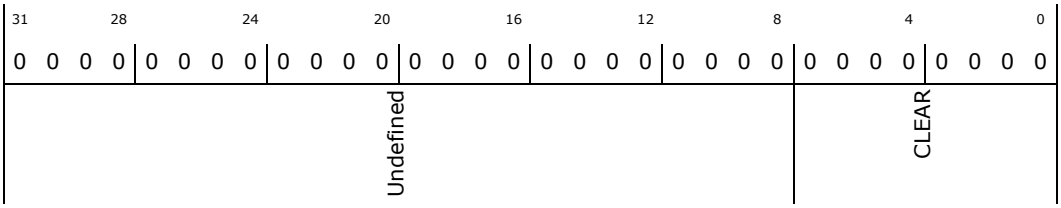
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearBlock_LO: [BAR] + 340h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

3.29.210 Interrupt Clear Registers (ClearBlock_HI)—Offset 344h

Refer to the description for register ClearTfr_HI.

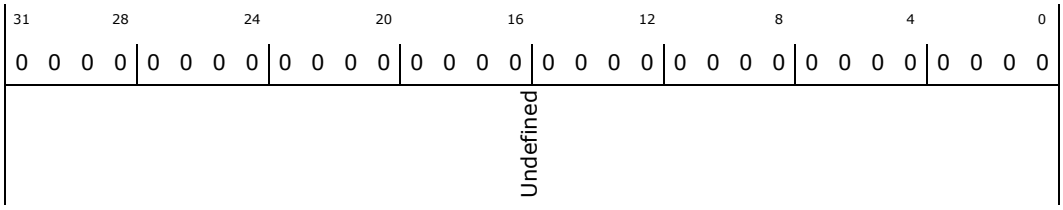
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearBlock_HI: [BAR] + 344h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.211 Interrupt Clear Registers - Low (ClearSrcTran_LO)—Offset 348h

Refer to the description for register ClearTfr_HI.

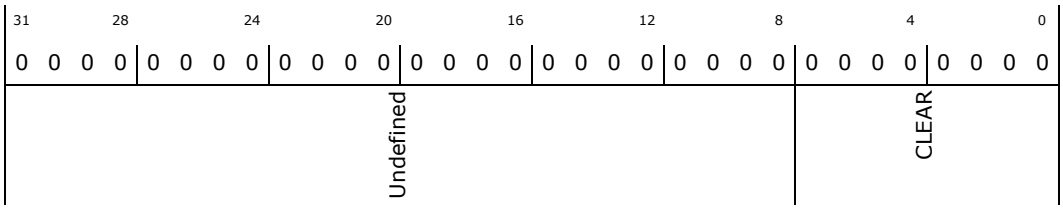
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearSrcTran_LO: [BAR] + 348h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

3.29.212 Interrupt Clear RegistersClearSrc - High (ClearSrcTran_HI)—Offset 34Ch

Refer to the description for register ClearTfr_HI.

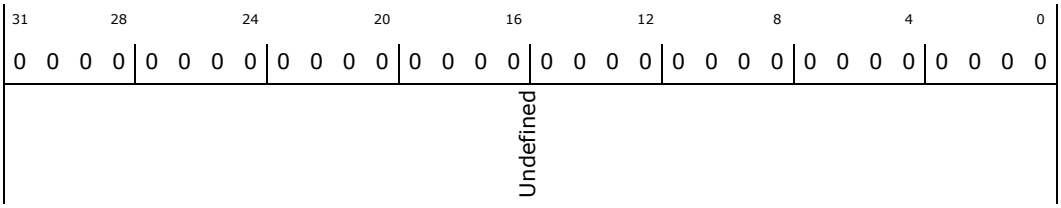
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearSrcTran_HI: [BAR] + 34Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.213 Interrupt Clear Registers - Low (ClearDstTran_LO)—Offset 350h

Refer to the description for register ClearTfr_HI.

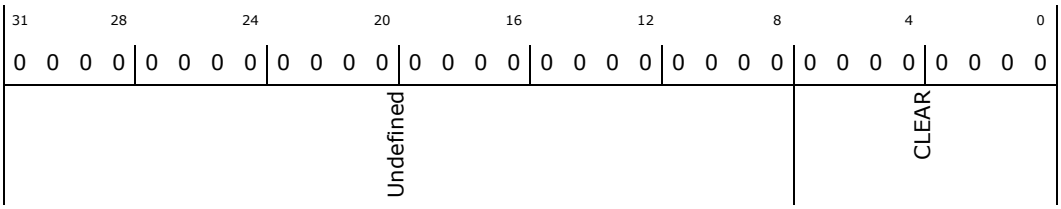
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearDstTran_LO: [BAR] + 350h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

3.29.214 Interrupt Clear Registers - High (ClearDstTran_HI)—Offset 354h

Refer to the description for register ClearTfr_HI.

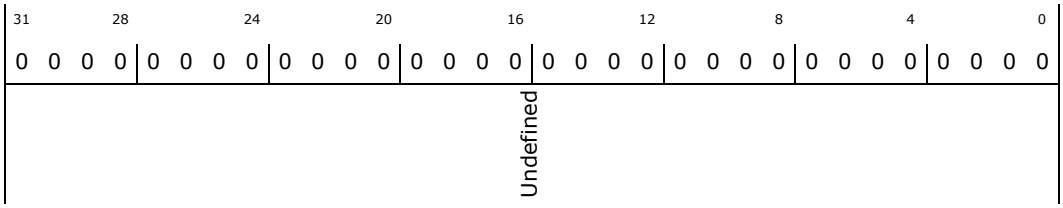
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearDstTran_HI: [BAR] + 354h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.215 Interrupt Clear Registers - Low (ClearErr_LO)—Offset 358h

Refer to the description for register ClearTfr_HI.

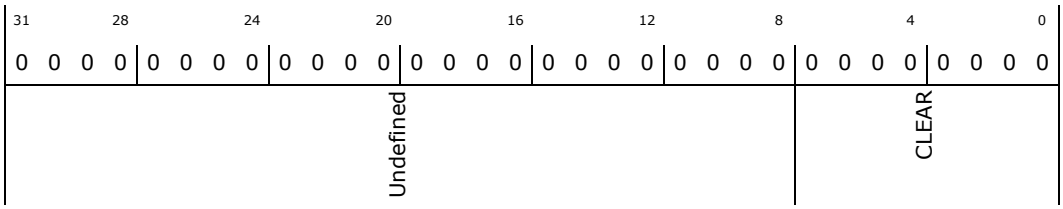
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearErr_LO: [BAR] + 358h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

3.29.216 Interrupt Clear Registers - High (ClearErr_HI)—Offset 35Ch

Refer to the description for register ClearTfr_HI.

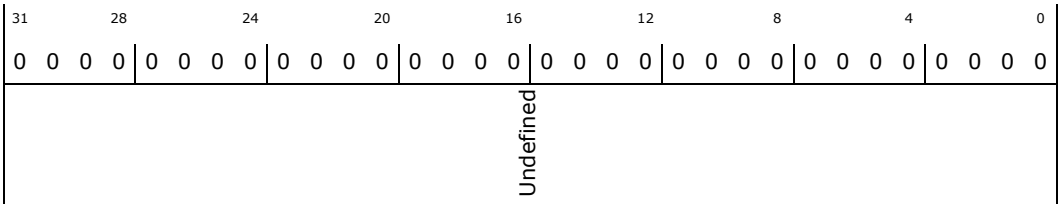
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearErr_HI: [BAR] + 35Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.217 Combined Interrupt Status Register - Low (StatusInt_LO)—Offset 360h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

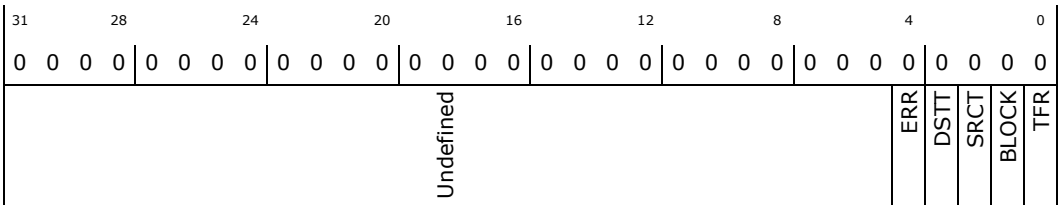
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusInt_LO: [BAR] + 360h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Description
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register.
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

3.29.218 Combined Interrupt Status Register - High (StatusInt_HI)—Offset 364h

Refer to the description for register StatusInt_LO.

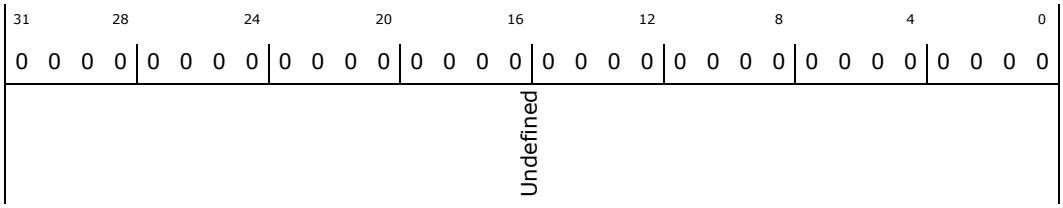
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusInt_HI: [BAR] + 364h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.219 Source Software Transaction Request Register - Low (ReqSrcReg_LO)—Offset 368h

A bit is assigned for each channel in this register. ReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

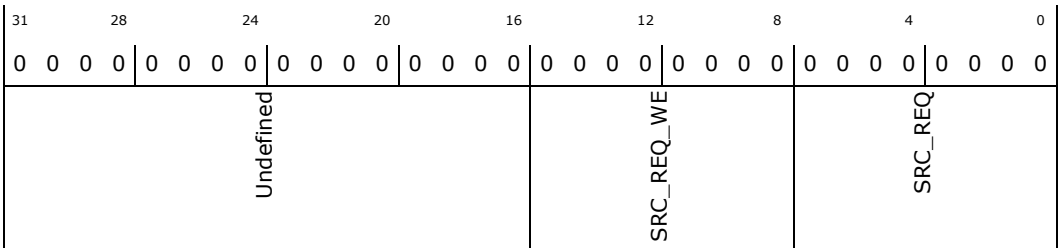
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ReqSrcReg_LO: [BAR] + 368h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Source Req Write Enable (SRC_REQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Source Request (SRC_REQ):** A channel SRC_REQ bit is written only if the corresponding channel write enable bit in the SRC_REQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register. For an example and further details, refer to the DesignWare DW_ahb_dmac Databook.

3.29.220 Source Software Transaction Request Register - High (ReqSrcReg_HI)—Offset 36Ch

A bit is assigned for each channel in this register. ReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

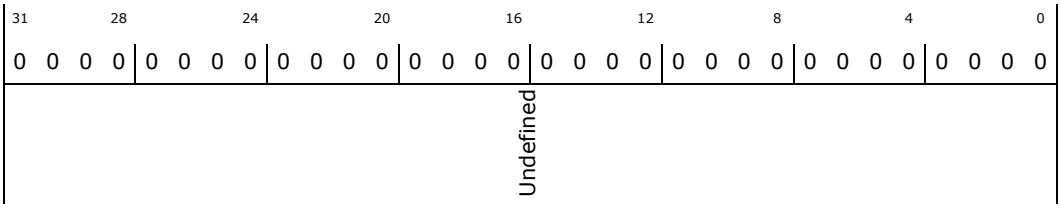
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ReqSrcReg_HI: [BAR] + 36Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.221 Destination Software Transaction Request Register - Low (ReqDstReg_LO)—Offset 370h

A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

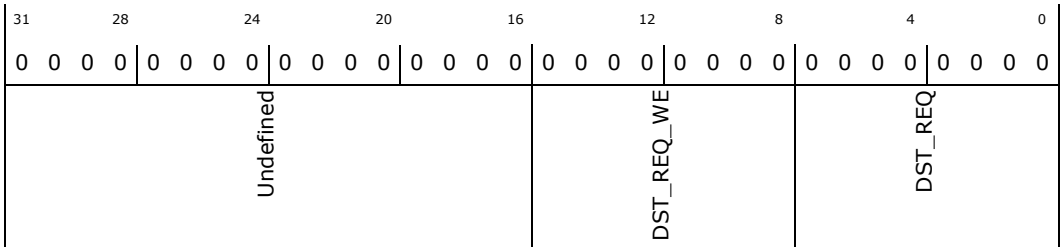
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ReqDstReg_LO: [BAR] + 370h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Destination Request Write Enable (DST_REQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Request (DST_REQ):** A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

3.29.222 Destination Software Transaction Request Register - High (ReqDstReg_HI)—Offset 374h

A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

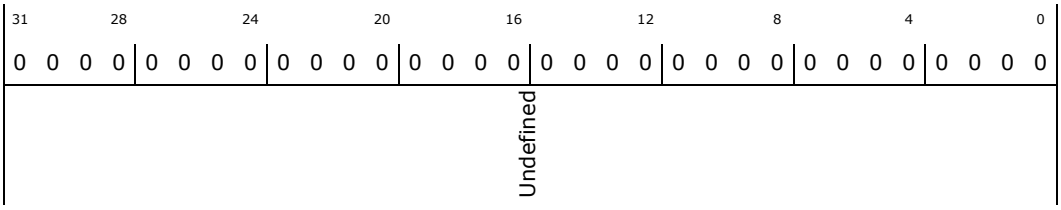
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ReqDstReg_HI: [BAR] + 374h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.223 Single Source Software Transaction Request Register - Low (SglRqSrcReg_LO)—Offset 378h

A bit is assigned for each channel in this register. SglReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

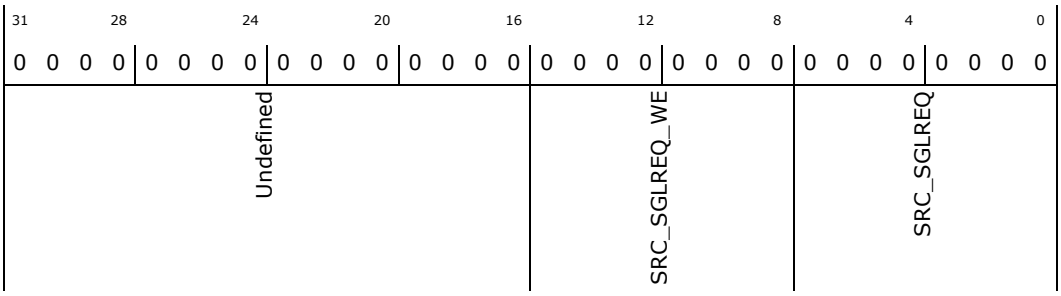
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SglRqSrcReg_LO: [BAR] + 378h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Source Req Write Enable (SRC_SGLREQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Source Single Request (SRC_SGLREQ):** A channel SRC_SGLREQ bit is written only if the corresponding channel write enable bit in the SRC_SGLREQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

3.29.224 Single Source Software Transaction Request Register - High (SglRqSrcReg_HI)—Offset 37Ch

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

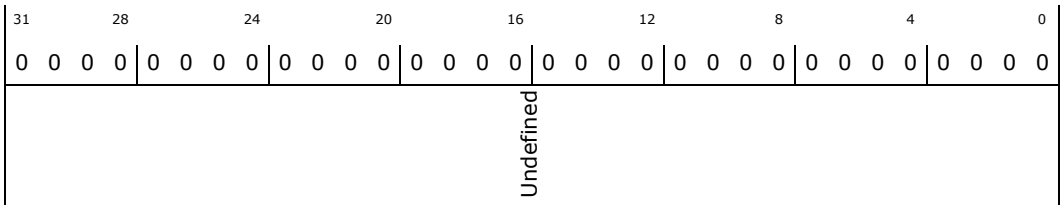
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SglRqSrcReg_HI: [BAR] + 37Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.225 Single Destination Software Transaction Request Register - Low (SglRqDstReg_LO)—Offset 380h

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

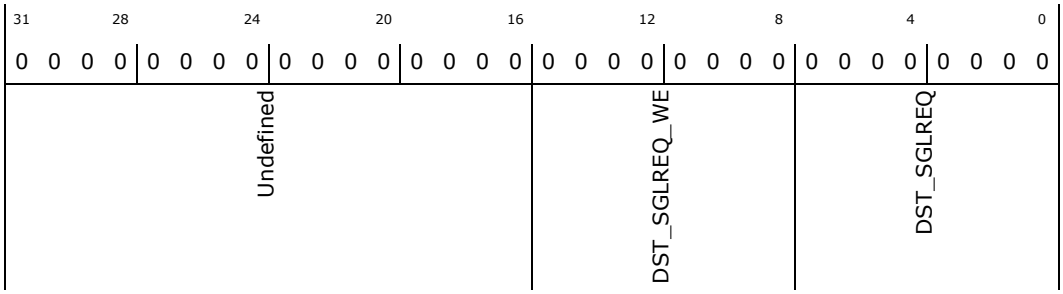
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SglRqDstReg_LO: [BAR] + 380h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Destination Request Write Enable (DST_SGLREQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Single or Burst Request (DST_SGLREQ):** A channel DST_SGLREQ bit is written only if the corresponding channel write enable bit in the DST_SGLREQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

3.29.226 Single Destination Software Transaction Request Register - High (SglRqDstReg_HI)—Offset 384h

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

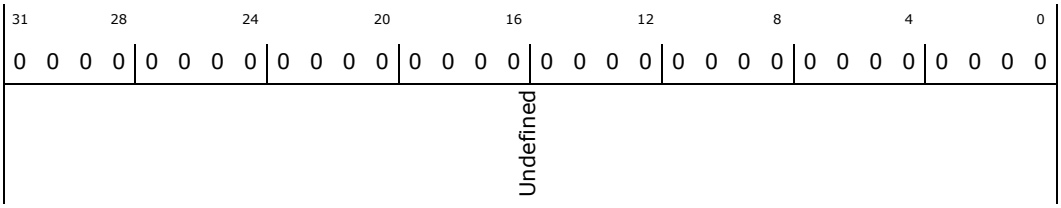
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SglRqDstReg_HI: [BAR] + 384h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.227 Last Source Transaction Request Register - Low (LstSrcReg_LO)—Offset 388h

A bit is assigned for each channel in this register. LstSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n, or when the source of channel n is not a flow controller.

A channel LSTSRC bit is written only if the corresponding channel write enable bit in the LSTSRC_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

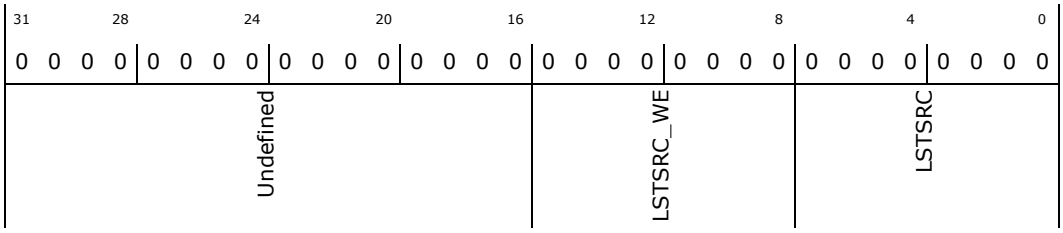
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LstSrcReg_LO: [BAR] + 388h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Last Source Transaction Request Write Enable (LSTSRC_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Last Source Transaction Request (LSTSRC):** • 0 = Not last transaction in current block • 1 = Last transaction in current block

3.29.228 Last Source Transaction Request Register - High (LstSrcReg_HI)—Offset 38Ch

Refer to description for Last Source Transaction Request Register - Low.

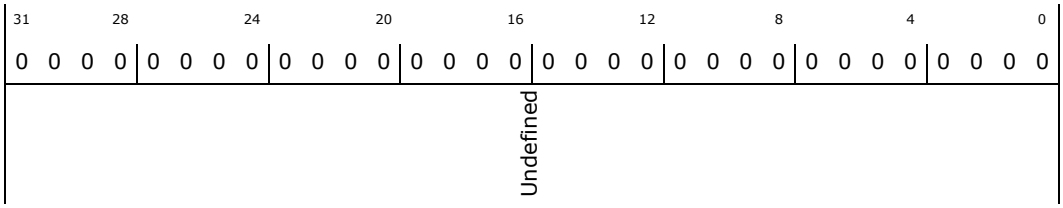
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LstSrcReg_HI: [BAR] + 38Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.229 Last Destination Transaction Request Register - Low (LstDstReg_LO)—Offset 390h

A bit is assigned for each channel in this register. LstDstReg[n] is ignored when software handshaking is not enabled for the destination of channel n or when the destination of channel n is not a flow controller.

A channel LSTDST bit is written only if the corresponding channel write enable bit in the LSTDST_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

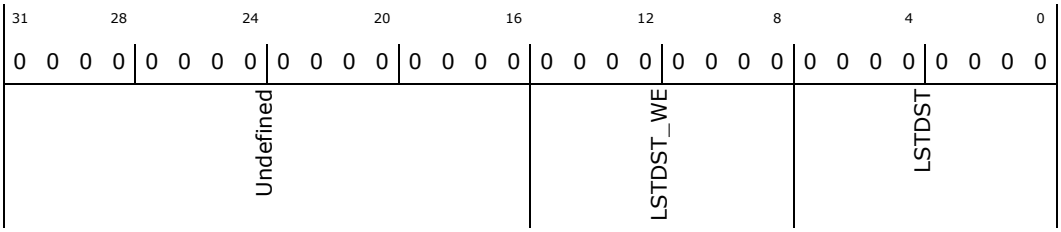
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LstDstReg_LO: [BAR] + 390h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Last Destination Transaction Request Write Enable (LSTDST_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Last Transaction Request (LSTDST):** • 0 = Not last transaction in current block • 1 = Last transaction in current block

3.29.230 Last Destination Transaction Request Register - High (LstDstReg_HI)—Offset 394h

Refer to description for Last Destination Transaction Request Register - Low.

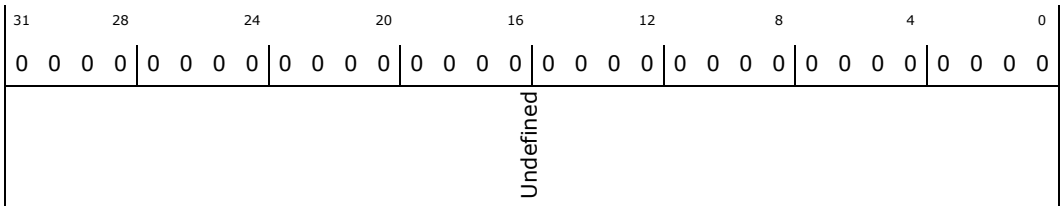
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LstDstReg_HI: [BAR] + 394h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.231 DW_ahb_dmac Configuration Register - Low (DmaCfgReg_LO)—Offset 398h

This register is used to enable the DW_ahb_dmac, which must be done before any channel activity can begin.

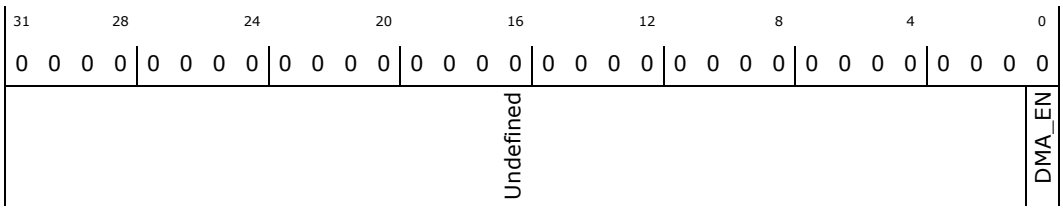
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaCfgReg_LO: [BAR] + 398h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**Undefined:** Reserved.
0	0h RW	**DW_ahb_dmac Enable Bit (DMA_EN):** • 0 = DW_ahb_dmac Disabled • 1 = DW_ahb_dmac Enabled

3.29.232 DW_ahb_dmac Configuration Register - High (DmaCfgReg_HI)—Offset 39Ch

Refer to description for DW_ahb_dmac Configuration Register - Low.

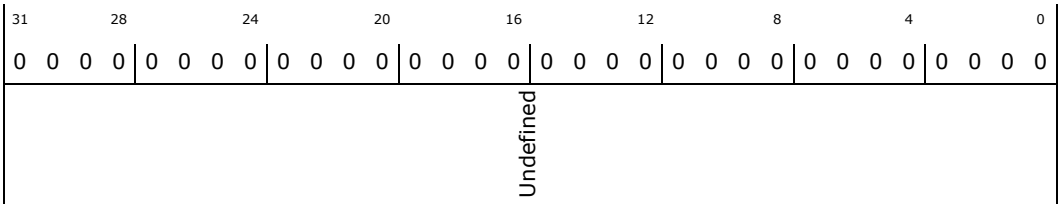
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaCfgReg_HI: [BAR] + 39Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.233 DW_ahb_dmac Channel Enable Register - Low (ChEnReg_LO)—Offset 3A0h

This is the DW_ahb_dmac Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive; it can then enable an inactive channel with the required priority.

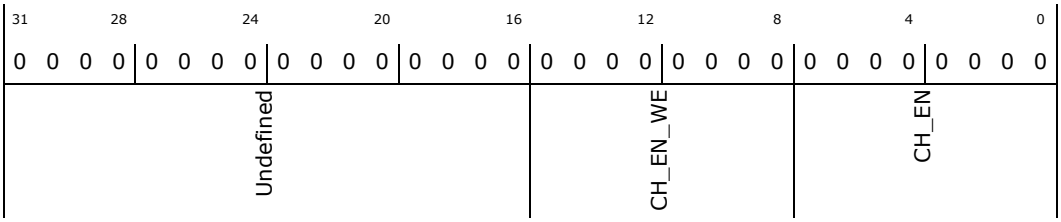
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ChEnReg_LO: [BAR] + 3A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Channel Enable Write Enable (CH_EN_WE):** The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE (this bit), is asserted on the same AHB write transfer.

Bit Range	Default & Access	Description
7:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel; clearing this bit disables the channel. • 0 = Disable the Channel • 1 = Enable the Channel

3.29.234 DW_ahb_dmac Channel Enable Register - High (ChEnReg_HI)—Offset 3A4h

Refer to the description for DW_ahb_dmac Channel Enable Register - Low.

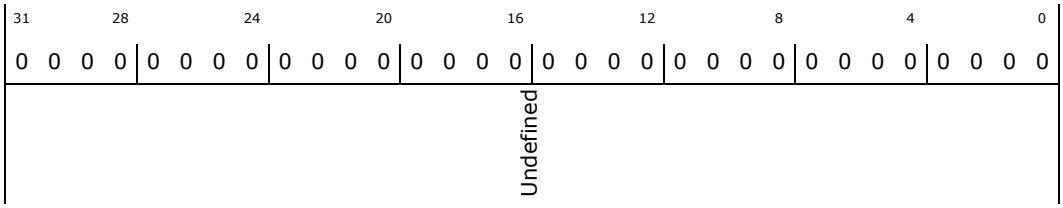
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ChEnReg_HI: [BAR] + 3A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.235 DW_ahb_dmac ID Register - Low (DmaIdReg_LO)—Offset 3A8h

This is a read-only register that reads back the coreConsultant-configured hardcoded ID number, DMAH_ID_NUM.

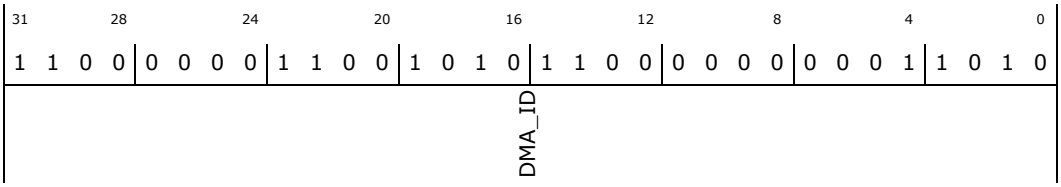
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaIdReg_LO: [BAR] + 3A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: C0CAC01Ah



Bit Range	Default & Access	Description
31:0	c0cac01ah RO	**Hardcoded DW_ahb_dmac Peripheral ID (DMA_ID):** coreConsultantconfigured hardcoded ID number DMAH_ID_NUM.

3.29.236 DW_ahb_dmac ID Register - High (DmaIdReg_HI)—Offset 3ACh

Refer to the description of DW_ahb_dmac ID Register - Low.

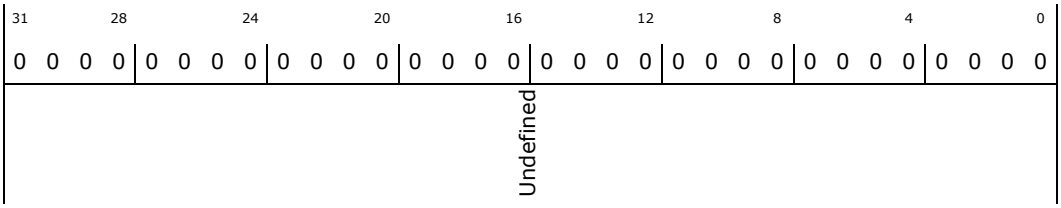
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaIdReg_HI: [BAR] + 3ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.237 DW_ahb_dmac Test Register - Low (DmaTestReg_LO)—Offset 3B0h

This register is used to put the AHB slave interface into test mode, during which the readback value of the writable registers match the value written, assuming the DW_ahb_dmac configuration has not optimized the same registers. In normal operation, the readback value of some registers is a function of the DW_ahb_dmac state, and does not match the value written.

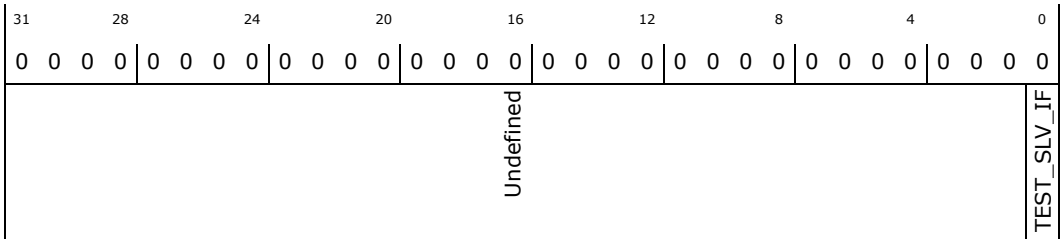
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaTestReg_LO: [BAR] + 3B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**Undefined:** Reserved.
0	0h RW	**TEST_SLV_IF:** Puts the AHB slave interface into test mode. In this mode, the readback value of the writable registers always matches the value written. This bit does not allow writing to read-only registers. • 0 = Normal mode • 1 = Test mode

3.29.238 DW_ahb_dmac Test Register - High (DmaTestReg_HI)—Offset 3B4h

Refer to the description of DW_ahb_dmac Test Register - Low.

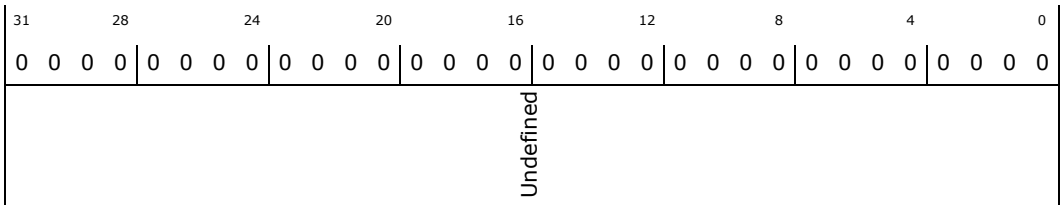
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaTestReg_HI: [BAR] + 3B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.239 DW_ahb_dmac Component Parameters Register 6 - Low (DMA_COMP_PARAMS_6_LO)—Offset 3C8h

Refer to the description for DW_ahb_dmac Component Parameters Register 6 - High.

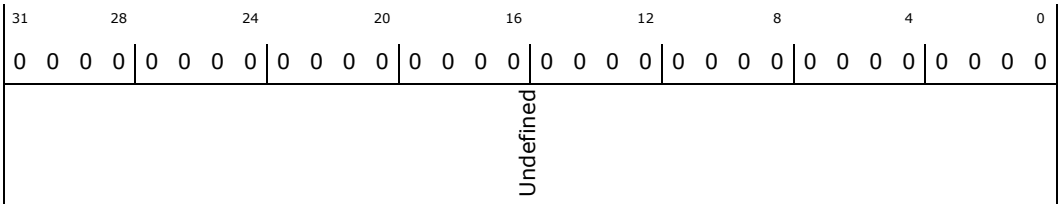
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_6_LO: [BAR] + 3C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Undefined:** Reserved.

3.29.240 DW_ahb_dmac Component Parameters Register 6 - High (DMA_COMP_PARAMS_6_HI)—Offset 3CCh

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 7. The reset value depends on coreConsultant parameter(s).

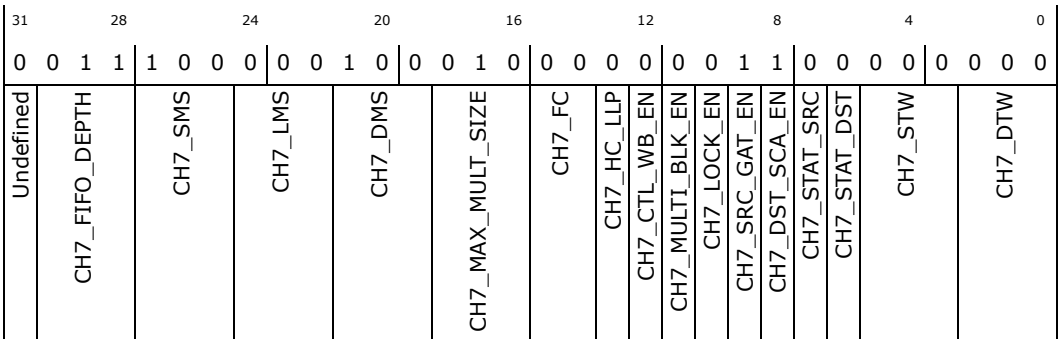
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_6_HI: [BAR] + 3CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH7_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH7_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH7_SMS:** The value of this register is derived from the DMAH_CH7_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH7_LMS:** The value of this register is derived from the DMAH_CH7_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH7_DMS:** The value of this register is derived from the DMAH_CH7_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH7_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH7_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH7_FC:** The value of this register is derived from the DMAH_CH7_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY

Bit Range	Default & Access	Description
13	0h RO	**CH7_HC_LLP:** The value of this register is derived from the DMAH_CH7_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH7_CTL_WB_EN:** The value of this register is derived from the DMAH_CH7_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH7_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH7_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH7_LOCK_EN:** The value of this register is derived from the DMAH_CH7_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH7_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH7_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH7_DST_SCA_EN:** The value of this register is derived from the DMAH_CH7_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH7_STAT_SRC:** The value of this register is derived from the DMAH_CH7_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH7_STAT_DST:** The value of this register is derived from the DMAH_CH7_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH7_STW:** The value of this register is derived from the DMAH_CH7_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

Bit Range	Default & Access	Description
2:0	0h RO	**CH7_DTW:** The value of this register is derived from the DMAH_CH7_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.29.241 DW_ahb_dmac Component Parameters Register 5 - Low (DMA_COMP_PARAMS_5_LO)—Offset 3D0h

Refer to the description for DW_ahb_dmac Component Parameters Register 5 - High.

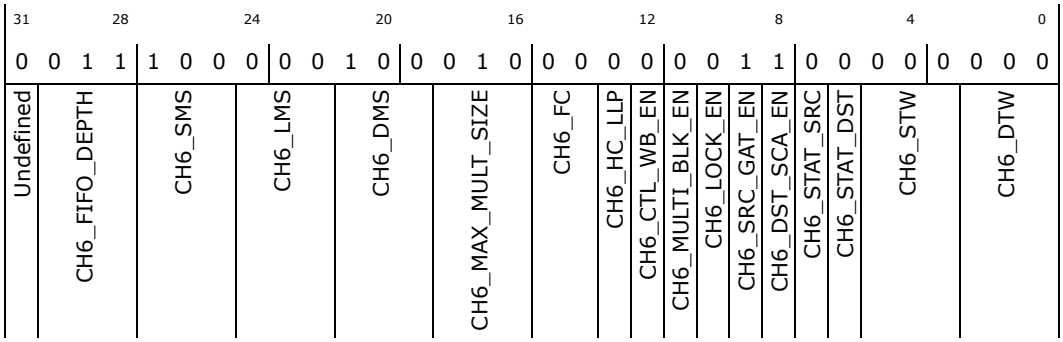
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_5_LO: [BAR] + 3D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH6_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH6_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128

Bit Range	Default & Access	Description
27:25	4h RO	**CH6_SMS:** The value of this register is derived from the DMAH_CH6_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH6_LMS:** The value of this register is derived from the DMAH_CH6_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH6_DMS:** The value of this register is derived from the DMAH_CH6_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH6_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH6_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH6_FC:** The value of this register is derived from the DMAH_CH6_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH6_HC_LLP:** The value of this register is derived from the DMAH_CH6_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH6_CTL_WB_EN:** The value of this register is derived from the DMAH_CH6_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
11	0h RO	**CH6_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH6_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH6_LOCK_EN:** The value of this register is derived from the DMAH_CH6_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH6_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH6_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH6_DST_SCA_EN:** The value of this register is derived from the DMAH_CH6_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH6_STAT_SRC:** The value of this register is derived from the DMAH_CH6_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH6_STAT_DST:** The value of this register is derived from the DMAH_CH6_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH6_STW:** The value of this register is derived from the DMAH_CH6_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH6_DTW:** The value of this register is derived from the DMAH_CH6_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.29.242 DW_ahb_dmac Component Parameters Register 5 - High (DMA_COMP_PARAMS_5_HI)—Offset 3D4h

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 5 and Channel 6. The reset value depends on coreConsultant parameter(s).

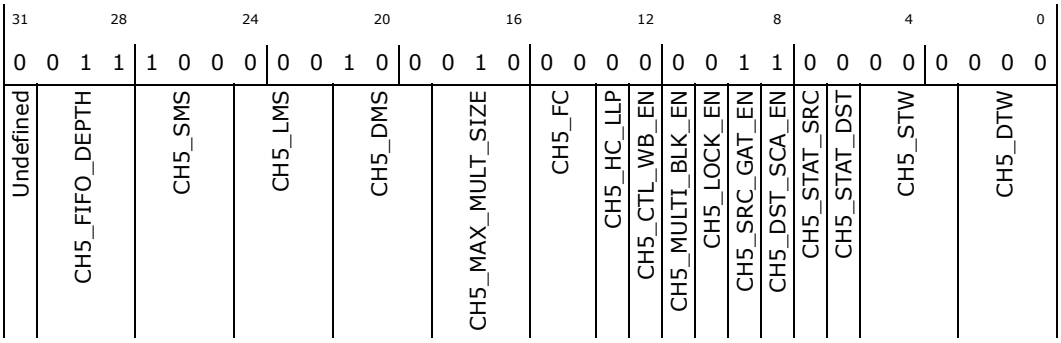
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_5_HI: [BAR] + 3D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH5_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH5_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH5_SMS:** The value of this register is derived from the DMAH_CH5_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH5_LMS:** The value of this register is derived from the DMAH_CH5_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
21:19	4h RO	**CH5_DMS:** The value of this register is derived from the DMAH_CH5_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH5_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH5_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH5_FC:** The value of this register is derived from the DMAH_CH5_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH5_HC_LLP:** The value of this register is derived from the DMAH_CH5_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH5_CTL_WB_EN:** The value of this register is derived from the DMAH_CH5_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH5_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH5_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH5_LOCK_EN:** The value of this register is derived from the DMAH_CH5_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH5_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH5_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
8	1h RO	**CH5_DST_SCA_EN:** The value of this register is derived from the DMAH_CH5_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH5_STAT_SRC:** The value of this register is derived from the DMAH_CH5_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH5_STAT_DST:** The value of this register is derived from the DMAH_CH5_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH5_STW:** The value of this register is derived from the DMAH_CH5_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH5_DTW:** The value of this register is derived from the DMAH_CH5_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.29.243 DW_ahb_dmac Component Parameters Register 4 - Low (DMA_COMP_PARAMS_4_LO)—Offset 3D8h

Refer to the description for DW_ahb_dmac Component Parameters Register 4 - High.

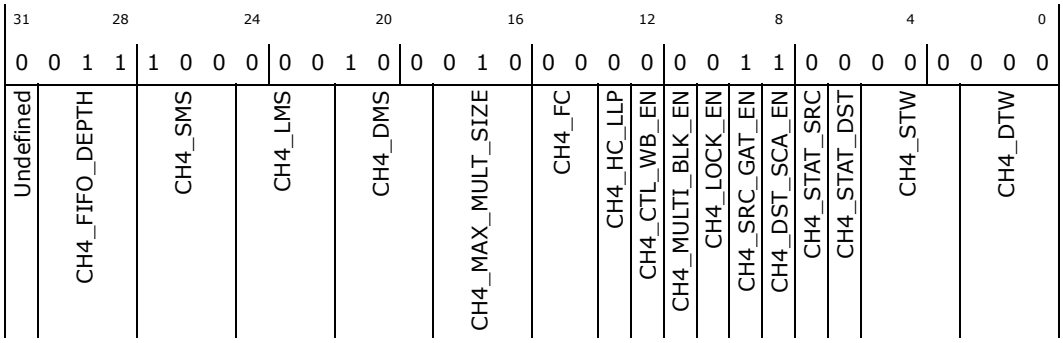
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_4_LO: [BAR] + 3D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH4_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH4_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH4_SMS:** The value of this register is derived from the DMAH_CH4_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH4_LMS:** The value of this register is derived from the DMAH_CH4_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH4_DMS:** The value of this register is derived from the DMAH_CH4_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
18:16	2h RO	**CH4_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH4_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH4_FC:** The value of this register is derived from the DMAH_CH4_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH4_HC_LLP:** The value of this register is derived from the DMAH_CH4_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH4_CTL_WB_EN:** The value of this register is derived from the DMAH_CH4_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH4_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH4_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH4_LOCK_EN:** The value of this register is derived from the DMAH_CH4_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH4_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH4_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH4_DST_SCA_EN:** The value of this register is derived from the DMAH_CH4_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
7	0h RO	**CH4_STAT_SRC:** The value of this register is derived from the DMAH_CH4_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH4_STAT_DST:** The value of this register is derived from the DMAH_CH4_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH4_STW:** The value of this register is derived from the DMAH_CH4_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH4_DTW:** The value of this register is derived from the DMAH_CH4_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.29.244 DW_ahb_dmac Component Parameters Register 4 - High (DMA_COMP_PARAMS_4_HI)—Offset 3DCh

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 3 and Channel 4. The reset value depends on coreConsultant parameter(s).

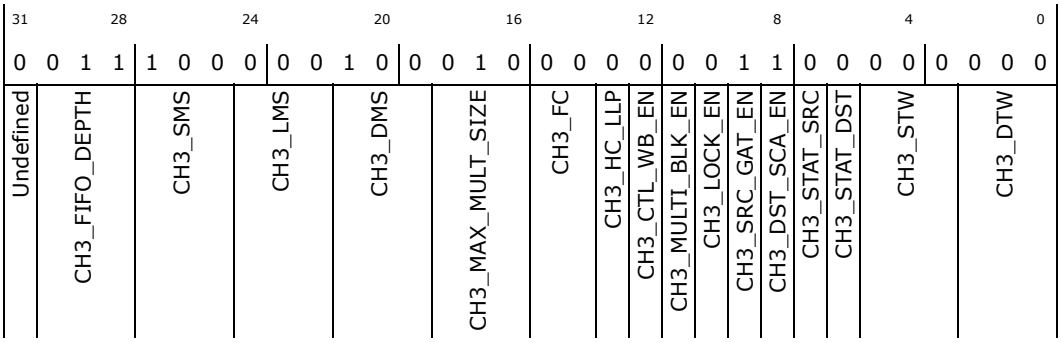
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_4_HI: [BAR] + 3DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH3_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH3_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH3_SMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH3_LMS:** The value of this register is derived from the DMAH_CH3_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH3_DMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
18:16	2h RO	**CH3_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH3_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH3_FC:** The value of this register is derived from the DMAH_CH3_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH3_HC_LLP:** The value of this register is derived from the DMAH_CH3_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH3_CTL_WB_EN:** The value of this register is derived from the DMAH_CH3_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH3_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH3_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH3_LOCK_EN:** The value of this register is derived from the DMAH_CH3_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH3_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH3_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH3_DST_SCA_EN:** The value of this register is derived from the DMAH_CH3_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
7	0h RO	**CH3_STAT_SRC:** he value of this register is derived from the DMAH_CH3_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH3_STAT_DST:** The value of this register is derived from the DMAH_CH3_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH3_STW:** The value of this register is derived from the DMAH_CH3_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH3_DTW:** The value of this register is derived from the DMAH_CH3_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.29.245 DW_ahb_dmac Component Parameters Register 3 - Low (DMA_COMP_PARAMS_3_LO)—Offset 3E0h

Refer to the description for DW_ahb_dmac Component Parameters Register 3 - High.

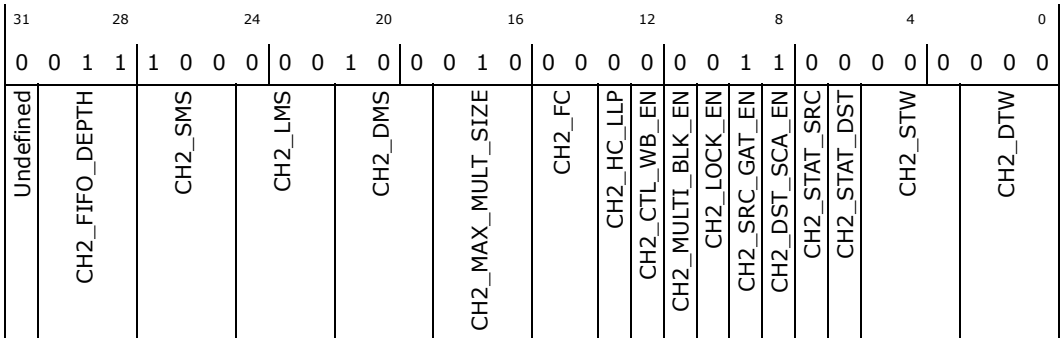
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_3_LO: [BAR] + 3E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH2_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH2_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH2_SMS:** The value of this register is derived from the DMAH_CH2_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH2_LMS:** The value of this register is derived from the DMAH_CH2_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH2_DMS:** The value of this register is derived from the DMAH_CH2_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
18:16	2h RO	**CH2_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH2_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH2_FC:** The value of this register is derived from the DMAH_CH2_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH2_HC_LLP:** The value of this register is derived from the DMAH_CH2_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH2_CTL_WB_EN:** The value of this register is derived from the DMAH_CH2_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH2_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH2_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to the spec. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH2_LOCK_EN:** The value of this register is derived from the DMAH_CH2_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH2_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH2_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH2_DST_SCA_EN:** The value of this register is derived from the DMAH_CH2_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
7	0h RO	**CH2_STAT_SRC:** The value of this register is derived from the DMAH_CH2_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH2_STAT_DST:** The value of this register is derived from the DMAH_CH2_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH2_STW:** The value of this register is derived from the DMAH_CH2_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH2_DTW:** The value of this register is derived from the DMAH_CH2_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.29.246 DW_ahb_dmac Component Parameters Register 3 - High (DMA_COMP_PARAMS_3_HI)—Offset 3E4h

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 1 and Channel 2. The reset value depends on coreConsultant parameter(s).

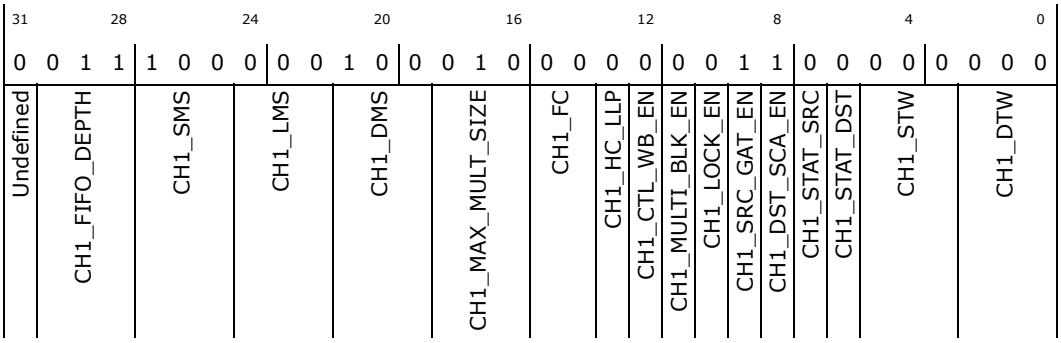
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_3_HI: [BAR] + 3E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH1_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH1_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH1_SMS:** The value of this register is derived from the DMAH_CH1_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH1_LMS:** The value of this register is derived from the DMAH_CH1_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH1_DMS:** The value of this register is derived from the DMAH_CH1_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
18:16	2h RO	**CH1_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH1_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH1_FC:** The value of this register is derived from the DMAH_CH1_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH1_HC_LLP:** The value of this register is derived from the DMAH_CH1_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH1_CTL_WB_EN:** The value of this register is derived from the DMAH_CH1_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH1_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH1_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH1_LOCK_EN:** The value of this register is derived from the DMAH_CH1_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH1_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH1_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH1_DST_SCA_EN:** The value of this register is derived from the DMAH_CH1_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
7	0h RO	**CH1_STAT_SRC:** The value of this register is derived from the DMAH_CH1_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH1_STAT_DST:** The value of this register is derived from the DMAH_CH1_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH1_STW:** The value of this register is derived from the DMAH_CH1_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH1_DTW:** The value of this register is derived from the DMAH_CH1_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.29.247 DW_ahb_dmac Component Parameters Register 2 - Low (DMA_COMP_PARAMS_2_LO)—Offset 3E8h

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

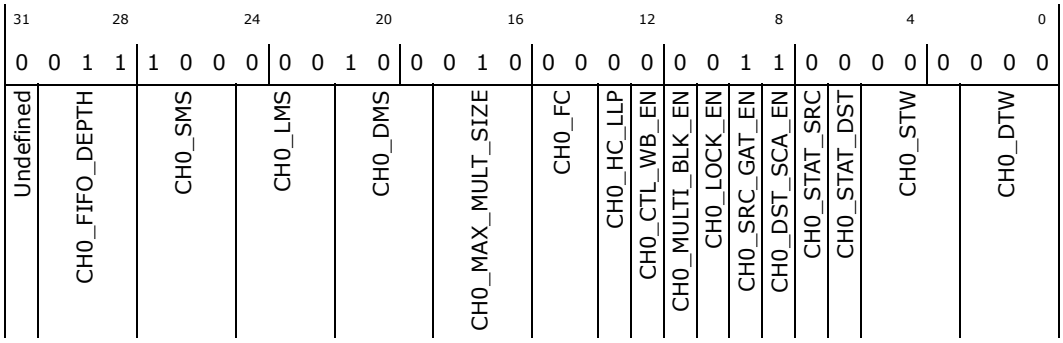
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_2_LO: [BAR] + 3E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH0_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH0_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH0_SMS:** The value of this register is derived from the DMAH_CH0_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH0_LMS:** The value of this register is derived from the DMAH_CH0_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH0_DMS:** The value of this register is derived from the DMAH_CH0_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Description
18:16	2h RO	**CH0_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH0_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH0_FC:** The value of this register is derived from the DMAH_CH0_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH0_HC_LLP:** The value of this register is derived from the DMAH_CH0_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH0_CTL_WB_EN:** The value of this register is derived from the DMAH_CH0_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH0_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH0_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH0_LOCK_EN:** The value of this register is derived from the DMAH_CH0_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH0_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH0_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH0_DST_SCA_EN:** The value of this register is derived from the DMAH_CH0_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Description
7	0h RO	**CH0_STAT_SRC:** The value of this register is derived from the DMAH_CH0_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH0_STAT_DST:** The value of this register is derived from the DMAH_CH0_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH0_STW:** Refer to the description for bit field DMA_COMP_PARAMS_2_LO.CH0_DTW
2:0	0h RO	**CH0_DTW:** The value of this register is derived from the DMAH_CH0_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

3.29.248 DW_ahb_dmac Component Parameters Register 2 - High (DMA_COMP_PARAMS_2_HI)—Offset 3ECh

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

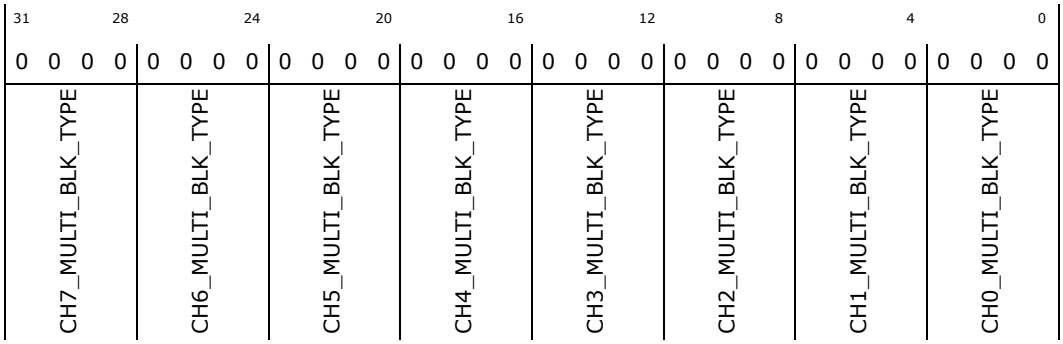
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_2_HI: [BAR] + 3ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RO	**CH7_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
27:24	0h RO	**CH6_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
23:20	0h RO	**CH5_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
19:16	0h RO	**CH4_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP

Bit Range	Default & Access	Description
15:12	0h RO	**CH3_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
11:8	0h RO	**CH2_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
7:4	0h RO	**CH1_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
3:0	0h RO	**CH0_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP

3.29.249 DW_ahb_dmac Component Parameters Register 1 - Low (DMA_COMP_PARAMS_1_LO)—Offset 3F0h

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

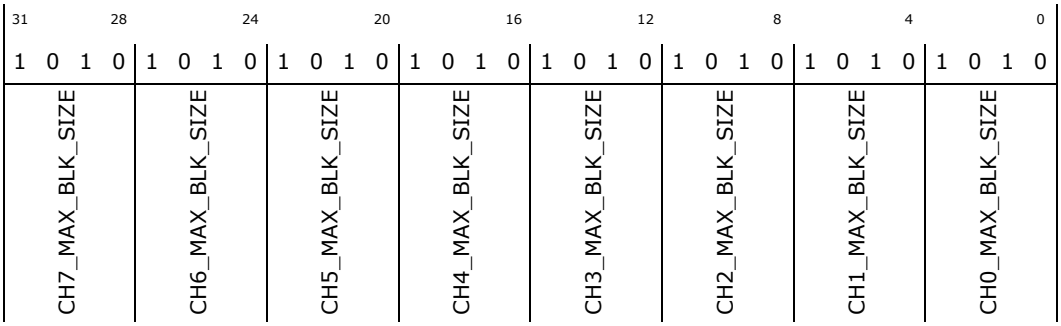
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_1_LO: [BAR] + 3F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: AAAAAAAAh



Bit Range	Default & Access	Description
31:28	ah RO	**CH7_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. • 0h = 3 • 1h = 7 • 2h = 15 • 3h = 31 • 4h = 63 • 5h = 127 • 6h = 255 • 7h = 511 • 8h = 1023 • 9h = 2047 • Ah = 4095
27:24	ah RO	**CH6_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
23:20	ah RO	**CH5_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
19:16	ah RO	**CH4_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
15:12	ah RO	**CH3_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
11:8	ah RO	**CH2_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
7:4	ah RO	**CH1_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
3:0	ah RO	**CH0_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.

3.29.250 DW_ahb_dmac Component Parameters Register 1 - High (DMA_COMP_PARAMS_1_HI)—Offset 3F4h

Refer to the description for DW_ahb_dmac Component Parameters Register 1 - Low.

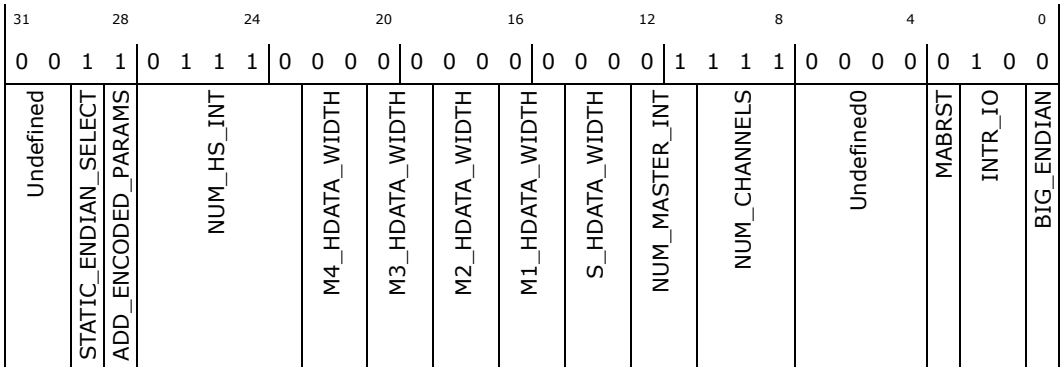
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMA_COMP_PARAMS_1_HI: [BAR] + 3F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 37000F04h



Bit Range	Default & Access	Description
31:30	0h RW	**Undefined:** Reserved.
29	1h RO	**STATIC_ENDIAN_SELECT:** The value of this register is derived from the DMAH_STATIC_ENDIAN_SELECT coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE
28	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the DMAH_ADD_ENCODED_PARAMS coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE
27:23	0eh RO	**NUM_HS_INT:** The value of this register is derived from the DMAH_NUM_HS_INT coreConsultant parameter. For a description of this parameter, refer to page 102. • 0h0 = 0 • to • 1h0 = 16
22:21	0h RO	**M4_HDATA_WIDTH:** The value of this register is derived from the DMAH_M4_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits

Bit Range	Default & Access	Description
20:19	0h RO	**M3_HDATA_WIDTH:** The value of this register is derived from the DMAH_M3_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
18:17	0h RO	**M2_HDATA_WIDTH:** The value of this register is derived from the DMAH_M2_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
16:15	0h RO	**M1_HDATA_WIDTH:** The value of this register is derived from the DMAH_M1_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
14:13	0h RO	**S_HDATA_WIDTH:** The value of this register is derived from the DMAH_S_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
12:11	01h RO	**NUM_MASTER_INT:** The value of this register is derived from the DMAH_NUM_MASTER_INT coreConsultant parameter. For a description of this parameter, refer to page 102. 0h = 1 to 3h = 4
10:8	7h RO	**NUM_CHANNELS:** The value of this register is derived from the DMAH_NUM_CHANNELS coreConsultant parameter. For a description of this parameter, refer to page 102. 0h = 1 to 7h = 8
7:4	0h RW	**Undefined0:** Reserved.
3	0h RO	**MABRST:** The value of this register is derived from the DMAH_MABRST coreConsultant parameter. For a description of this parameter, refer to page 103. • 0 = FALSE • 1 = TRUE
2:1	2h RO	**INTR_IO:** The value of this register is derived from the DMAH_INTR_IO coreConsultant parameter. For a description of this parameter, refer to page 103. • 0h = ALL • 1h = TYPE • 2h = COMBINED • 3h = reserved

Bit Range	Default & Access	Description
0	0h RO	**BIG_ENDIAN:** The value of this register is derived from the DMAH_BIG_ENDIAN coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE

3.29.251 DMA Component ID RegisterDma - Low (DmaCompsID_LO)—Offset 3F8h

This is the DW_ahb_dmac Component Version register, which is a read-only register that specifies the version of the packaged component in the upper 32 bits and the component type in the lower 32 bits.

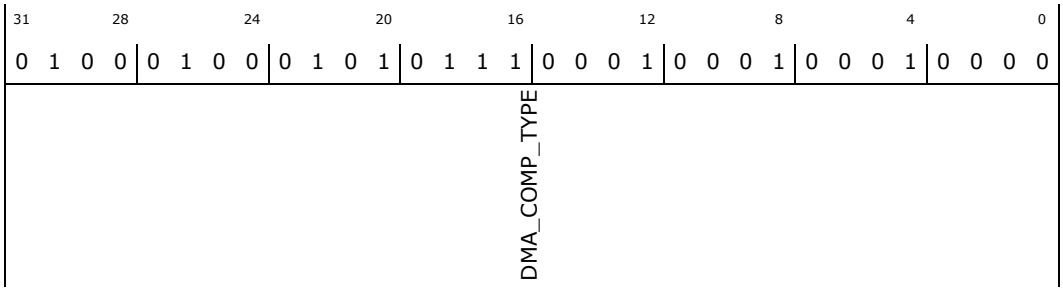
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaCompsID_LO: [BAR] + 3F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 44571110h



Bit Range	Default & Access	Description
31:0	44571110h RO	**Designware Component Type (DMA_COMP_TYPE):** Designware Component Type number = 0x44_57_11_10. This assigned unique hex value is constant and is derived from the two ASCII letters -DW- followed by a 32-bit unsigned number.

3.29.252 DMA Component ID Register - High (DmaCompsID_HI)—Offset 3FCh

This is the DW_ahb_dmac Component Version register, which is a read-only register that specifies the version of the packaged component in the upper 32 bits and the component type in the lower 32 bits.

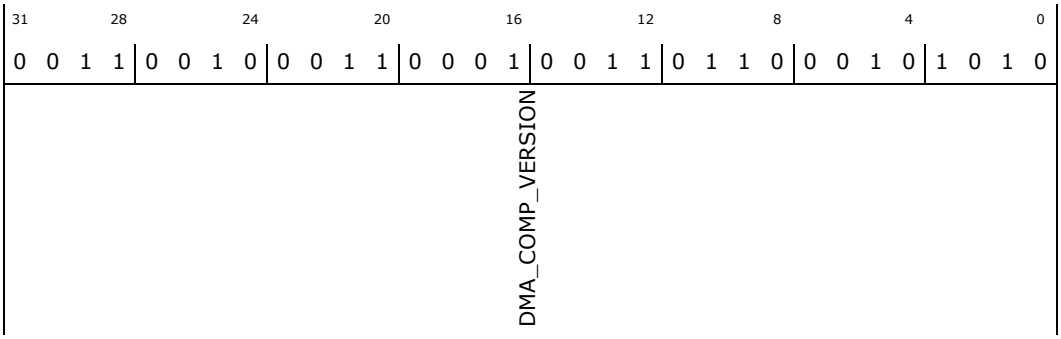
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

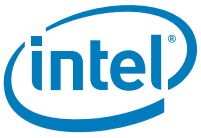
DmaCompsID_HI: [BAR] + 3FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 3231362Ah



Bit Range	Default & Access	Description
31:0	3231362ah RO	**Version of the Component (DMA_COMP_VERSION):** Reserved.



3.30 SIO SPI PCI Configuration Registers

Table 38. Summary of SIO SPI PCI Configuration Registers—0/30/5

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2504	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2505	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2506	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2507	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2508	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2508	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2509	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2510	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2510	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2511	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2511	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2512	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2513	00000000h

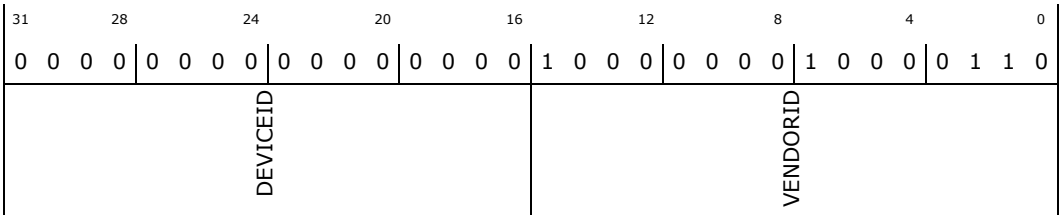
3.30.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:30, F:5] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

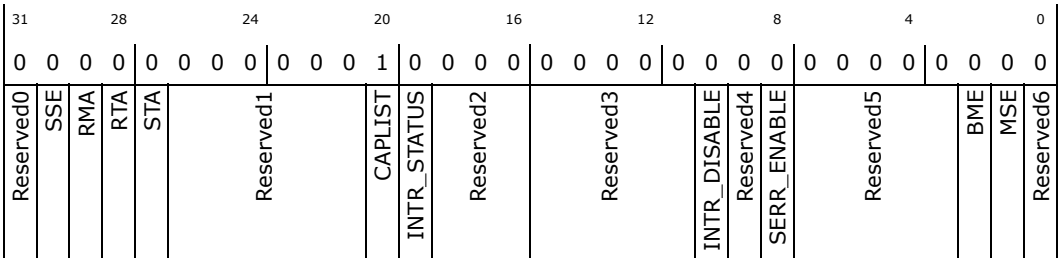
3.30.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:30, F:5] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

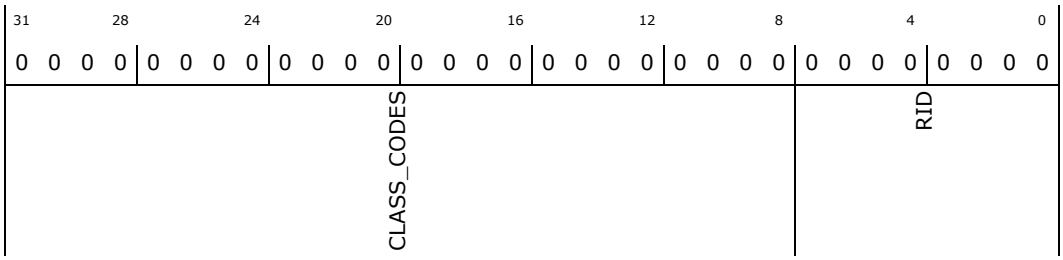
3.30.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:30, F:5] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

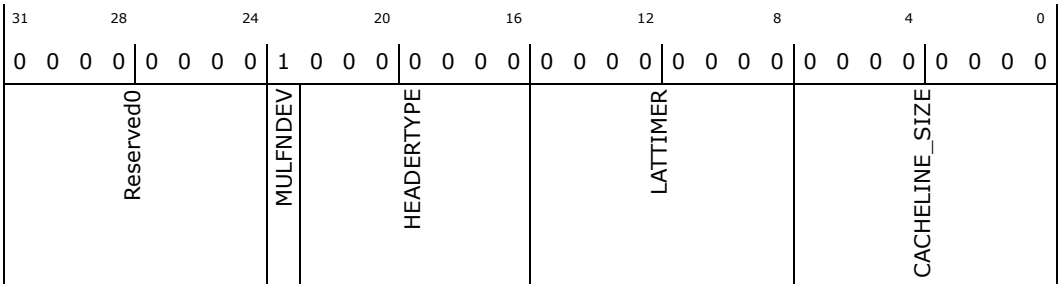
3.30.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:30, F:5] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

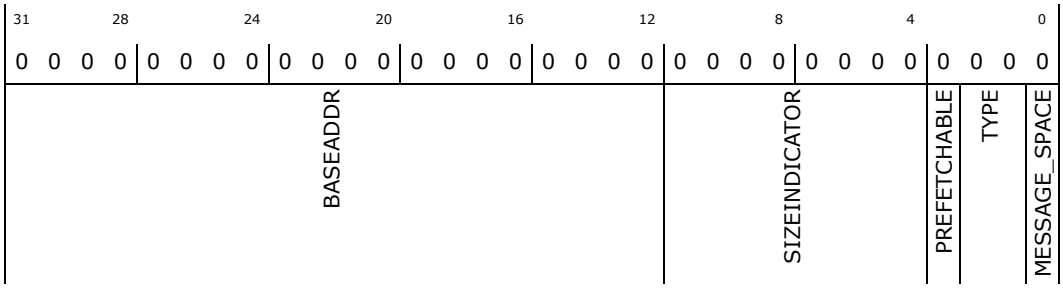
3.30.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

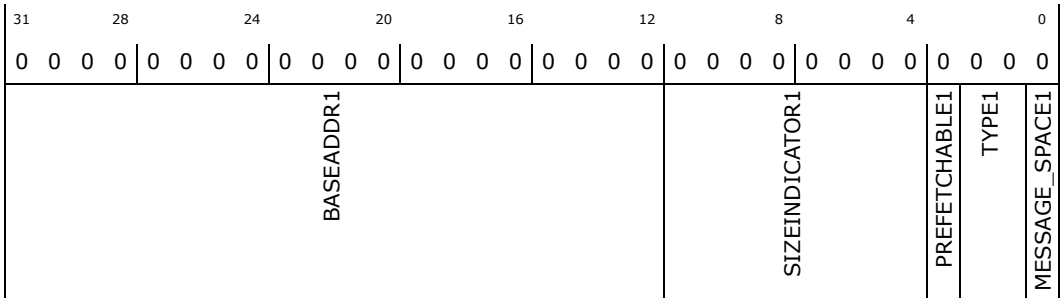
3.30.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:30, F:5] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

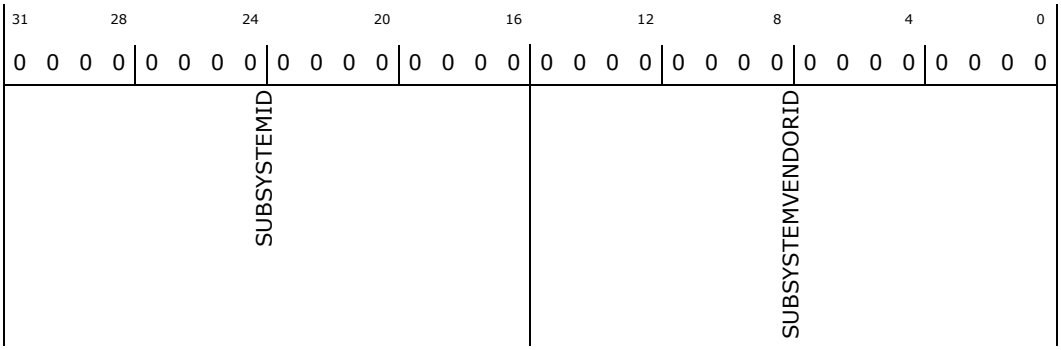
3.30.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:30, F:5] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

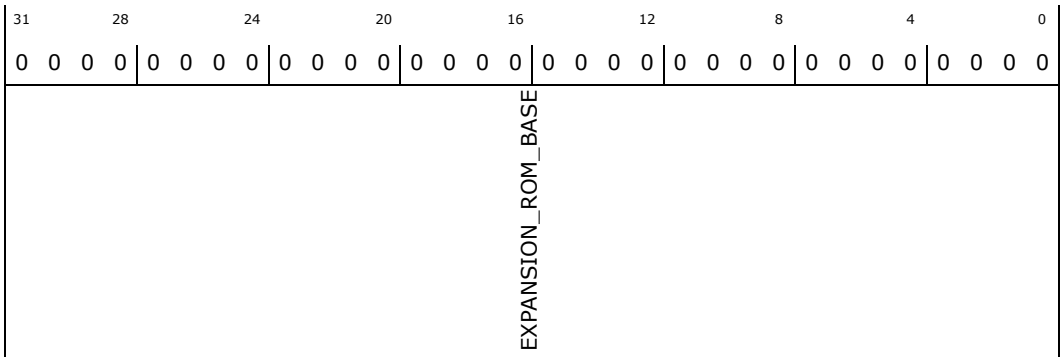
3.30.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:30, F:5] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

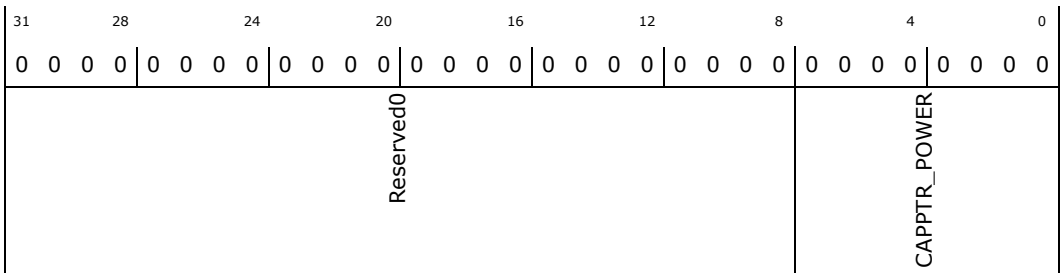
3.30.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:30, F:5] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

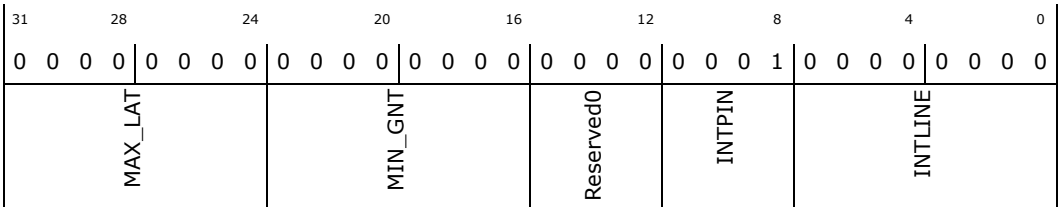
3.30.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

INTERRUPTREG: [B:0, D:30, F:5] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

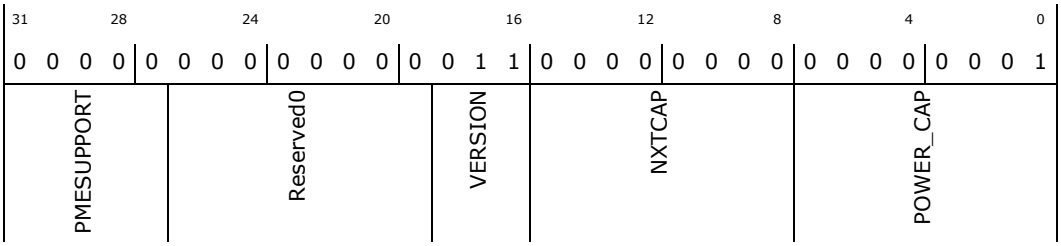
3.30.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

POWERCAPID: [B:0, D:30, F:5] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

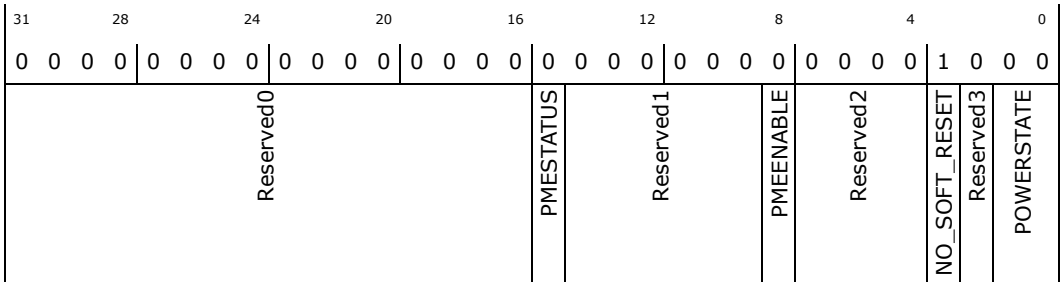
3.30.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:30, F:5] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

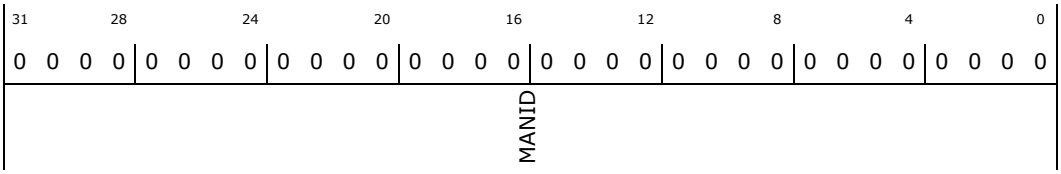
3.30.13 Manufacturer ID (MANID)—Offset F8h

Access Method

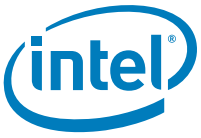
Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:30, F:5] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.



3.31 SIO SPI Memory Mapped I/O Registers

Table 39. Summary of SIO SPI Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"SSP Control Register 0 (SSCR0)—Offset 0h" on page 2514	00000000h
4h	4	"SSP Control Register 1 (SSCR1)—Offset 4h" on page 2516	00000000h
8h	4	"SSP Status Register (SSSR)—Offset 8h" on page 2518	0000F004h
Ch	4	"SSP Interrupt Test Register (SSITR)—Offset Ch" on page 2520	00000000h
10h	4	"SSP Data (SSDR)—Offset 10h" on page 2521	00000000h
28h	4	"SSP Time Out (SSTO)—Offset 28h" on page 2521	00000000h
2Ch	4	"SSP Programmable Serial Protocol (SSPSP)—Offset 2Ch" on page 2522	00000000h
30h	4	"SSP TX Time Slot Active (SSTSA)—Offset 30h" on page 2523	00000000h
34h	4	"SSP RX Time Slot Active (SSRSA)—Offset 34h" on page 2524	00000000h
38h	4	"SSP Time Slot Status (SSTSS)—Offset 38h" on page 2524	00000000h
3Ch	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 2525	00000000h
40h	4	"I2S Transmit FIFO (ITF)—Offset 40h" on page 2526	00000000h
44h	4	"SPI Transmit FIFO (SITF)—Offset 44h" on page 2527	00000000h
48h	4	"SPI Receive FIFO (SIRF)—Offset 48h" on page 2527	00000000h
400h	4	"Private Clock Params (PRV_CLOCK_PARAMS)—Offset 400h" on page 2528	00000000h
404h	4	"Software Reset (RESETS)—Offset 404h" on page 2528	00000000h
408h	4	"General Purpose Register (GENERAL)—Offset 408h" on page 2529	00000010h
40Ch	4	"reg_SSP_REG (SSP_REG)—Offset 40Ch" on page 2530	00000000h
418h	4	"reg_SPI_CS_CTRL_REG (SPI_CS_CTRL)—Offset 418h" on page 2531	00000000h

3.31.1 SSP Control Register 0 (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

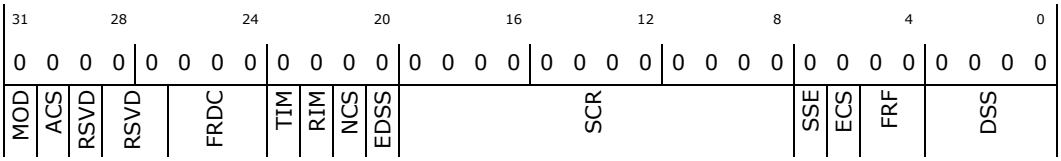
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR0: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**Mode (MOD):** • 0 = Normal SSP Mode • 1 = Network Mode
30	0b RW	**Audio Clock Select (ACS):** • 0 = Clock selection is determined by the NCS and ECS bits • 1 = Audio Clock (and Audio Clock Divider) are used to create the SSP's serial clock (SSPSCLK)
29	0b RO	**Reserved (RSVD):** Reserved.
28:27	00b RO	**RSVD:** Reserved
26:24	000b RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0b RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** • 0 = TUR events will generate an SSP interrupt • 1 = TUR events will not generate an SSP interrupt
22	0b RW	**Receive FIFO Over Run Interrupt Mask (RIM):** • 0 = ROR events will generate an SSP interrupt • 1 = ROR events will not generate an SSP interrupt
21	0b RW	**Network Clock Select (NCS):** • 0 = Clock selection is determined by ECS bit • 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0b RW	**Extended Data Size Select (EDSS):** • 0 = A zero is prepended to the DSS value, which sets the DSS range from 4-16 bits • 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	000h RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0b RW	**Synchronous Serial Port Enable (SSE):** • 0 = SSP operation disabled • 1 = SSP operation enabled
6	0b RW	**External Clock Select (ECS):** • 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) • 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	00b RW	**Frame Format (FRF):** • 00 = Motorola Serial Peripheral Interface (SPI) • 01 = Texas Instruments Synchronous Serial Protocol (SSP) • 10 = National Semiconductor Microwire • 11 = Programmable Serial Protocol (PSP)

Bit Range	Default & Access	Description
3:0	0000b RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

3.31.2 SSP Control Register 1 (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

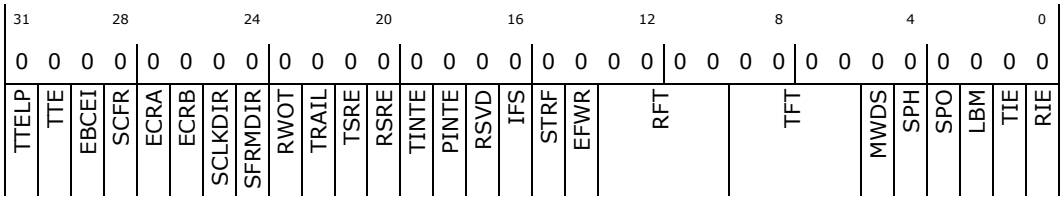
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

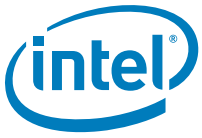
SSCR1: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**TXD Tristate Enable on Last Phase (TTELP):** • 0 = TXD line will be tristated on same clock edge as TXD is to be flopped • 1 = TXD line will be tristated clock edge after TXD is to be flopped
30	0b RW	**TXD Tristate Enable (TTE):** • 0 = TXD line will not be tristated • 1 = TXD line will be tristated when no transmitting data
29	0b RW	**Enable Bit Count Error Interrupt (EBCEI):** • 0 = Interrupt due to a bit count error is disabled • 1 = Interrupt due to a bit count error is enabled
28	0b RW	**Slave Clock Free Running (SCFR):** • 0 = clock input to SSPSCLK is continuously running • 1 = clock input to SSPSCLK is only active during transfers
27	0b RW	**Enable Clock Request A (ECRA):** • 0 = clock request from other SSP is disabled • 1 = clock request from other SSP is enabled
26	0b RW	**Enable Clock Request B (ECRB):** • 0 = clock request from other SSP is disabled • 1 = clock request from other SSP is enabled



Bit Range	Default & Access	Description
25	0b RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** • 0 = Master mode, SSP drives SSPSCLK • 1 = Slave mode, SSP receives SSPSCLK
24	0b RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** • 0 = Master mode, SSP drives SSPSFRM • 1 = Slave mode, SSP receives SSPSFRM
23	0b RW	**Receive With Out Transmit (RWOT):** • 0 = Transmit/Receive mode • 1 = Receive without Transmit mode
22	0b RW	**Trailing Byte (TRAIL):** • 0 = Processor based, trailing bytes are handled by processor • 1 = DMA based, trailing bytes are handled by DMA
21	0b RW	**Transmit Service Request Enable (TSRE):** • 0 = DMA Service Request is disabled • 1 = DMA Service Request is enabled
20	0b RW	**Receive Service Request Enable (RSRE):** • 0 = DMA Service Request is disabled • 1 = DMA Service Request is enabled
19	0b RW	**Receiver Time-out Interrupt Enable (TINTE):** • 0 = Receiver Time-out interrupts are disabled • 1 = Receiver Time-out interrupts are enabled
18	0b RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** • 0 = Peripheral Trailing Byte Interrupts are disabled • 1 = Peripheral Trailing Byte Interrupts are enabled
17	0b RW	**RSVD:** Reserved
16	0b RW	**Invert Frame Signal (IFS):** • 0 = Frame polarity is determined by SSP format and PSP polarity bits. • 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format and PSP polarity bits).
15	0b RW	**STRF:** Select FIFO for EFWR (test mode bit) (when EFWR=1) • 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) • 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0b RW	**Enable FIFO Write/Read (EFWR):** Test mode bit. • 0 = FIFO write/read special function is disabled (normal SSP operational mode) • 1 = FIFO write/read special function is enabled
13:10	0000b RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.
9:6	0000b RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.
5	0b RW	**Microwire Transmit Data Size (MWDS):** • 0 = 8-bit command words are transmitted • 1 = 16-bit command words are transmitted

Bit Range	Default & Access	Description
4	0b RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** • 0 = SSPSCLK is inactive one cycle at the start of a frame and cycle at the end of a frame • 1 = SSPSCLK is inactive cycle at the start of a frame and one cycle at the end of a frame
3	0b RW	**Motorola SPI SSPSCLK Polarity Setting (SPO):** • 0 = The inactive or idle state of SSPSCLK is low • 1 = The inactive or idle state of SSPSCLK is high
2	0b RW	**Loop-Back Mode (LBM):** Test mode bit. • 0 = Normal serial port operation enabled • 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0b RW	**Transmit FIFO Interrupt Enable (TIE):** • 0 = Transmit FIFO level interrupt is disabled • 1 = Transmit FIFO level interrupt is enabled
0	0b RW	**Receive FIFO Interrupt Enable (RIE):** • 0 = Receive FIFO level interrupt is disabled • 1 = Receive FIFO level interrupt is enabled

3.31.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

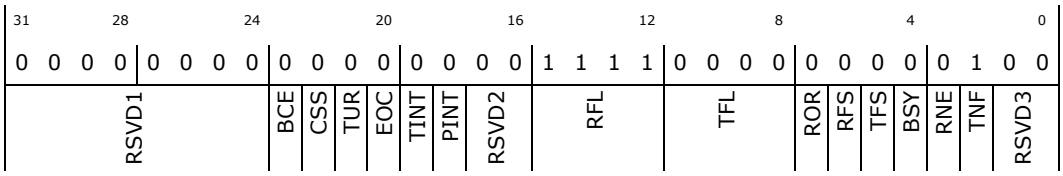
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSSR: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 0000F004h



Bit Range	Default & Access	Description
31:24	00h RO	**RSVD1:** Reserved

Bit Range	Default & Access	Description
23	0b RW1C	**Bit Count Error (BCE):** • 0 = SSP has not experienced a bit count error • 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0b RO	**Clock Synchronization Status (CSS):** • 0 = SSP is ready for slave clock operations • 1 = SSP is currently busy synchronizing slave mode signals
21	0b RW1C	**Transmit FIFO Under Run (TUR):** • 0 = Transmit FIFO has not experienced an under run • 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0b RW1C	**End of Chain (EOC):** • 0 = DMA has not signaled an end of chain condition • 1 = DMA has signaled an end of chain condition
19	0b RW1C	**Receiver Time-out Interrupt (TINT):** • 0 = No receiver time-out pending • 1 = Receiver time-out pending
18	0b RW1C	**Peripheral Trailing Byte Interrupt (PINT):** • 0 = No peripheral trailing byte interrupt pending • 1 = Peripheral trailing byte interrupt pending
17:16	00b RO	**RSVD2:** Reserved
15:12	1111b RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. **Note:** When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit.
11:8	0000b RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. **Note:** When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit.
7	0b RW1C	**Receive FIFO Overrun (ROR):** • 0 = Receive FIFO has not experienced an overrun • 1 = Attempted data write to full receive FIFO, request interrupt
6	0b RO	**Receive FIFO Service Request (RFS):** • 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled • 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0b RO	**Transmit FIFO Service Request (TFS):** • 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled • 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0b RO	**SSP Busy (BSY):** • 0 = SSP is idle or disabled • 1 = SSP currently transmitting or receiving a frame
3	0b RO	**Receive FIOF Not Empty (RNE):** • 0 = Receive FIFO is empty • 1 = Receive FIFO is not empty
2	1b RO	**Transmit FIFO Not Full (TNF):** • 0 = Transmit FIFO is full • 1 = Transmit FIFO is not full

Bit Range	Default & Access	Description
1:0	00b RO	**RSVD3:** Reserved

3.31.4 SSP Interrupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

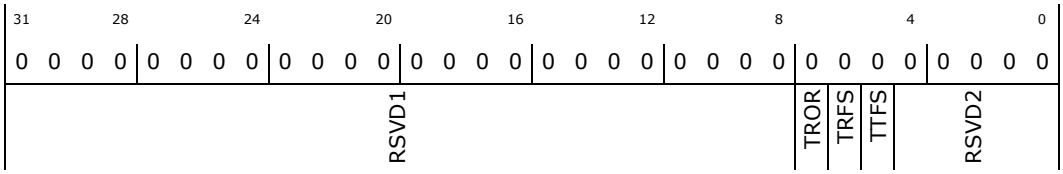
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSITR: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD1:** Reserved
7	0b RW	**Test Receive FIFO Overrun (TROR):** • 0 = No receive FIFO overrun service request • 1 = Generates non-maskable interrupt to CPU. No DMA request is generated.
6	0b RW	**Test Receive FIFO Service Request (TRFS):** • 0 = No receive FIFO service request • 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0b RW	**Test Transmit FIFO Service Request (TTFS):** • 0 = No transmit FIFO service request pending • 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	00000b RO	**RSVD2:** Reserved

3.31.5 SSP Data (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

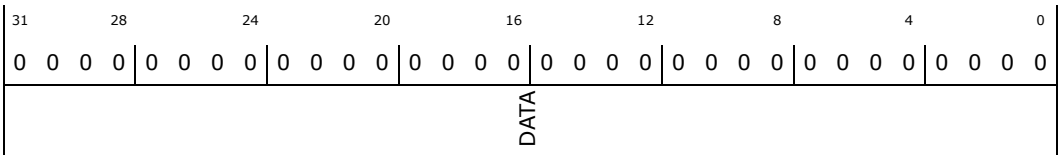
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSDR: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**DATA:** Data word to be written to/read from transmit/receive FIFO.

3.31.6 SSP Time Out (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read values of these bits are undetermined.

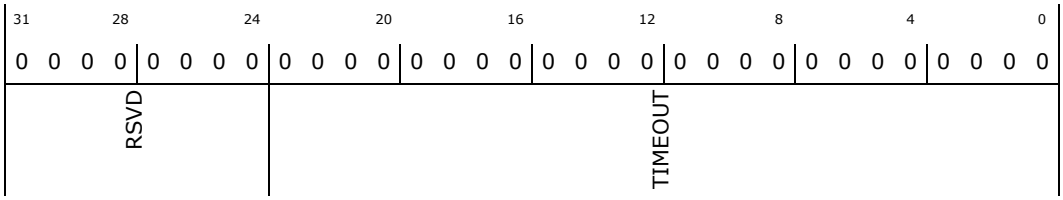
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTO: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**RSVD:** Reserved
23:0	000000h RW	**Time out Value (TIMEOUT):** This is the value that defines the time out interval, given by TIMEOUT/Peripheral Clock Frequency.

3.31.7 SSP Programmable Serial Protocol (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

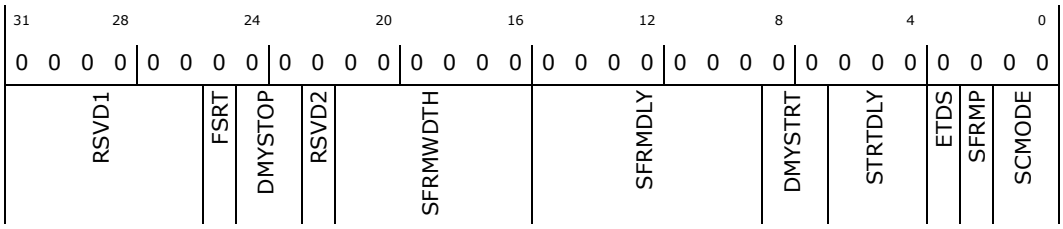
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSPSP: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	000000b RO	**RSVD1:** Reserved

Bit Range	Default & Access	Description
25	0b RW	**Frame Sync Relative Timing Bit (FSRT):** • 0 = Next frame is asserted after the end of the T4 timing • 1 = Next frame is asserted with the LSB of the previous frame
24:23	00b RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data.
22	0b RW	**RSVD2:** Reserved
21:16	000000b RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38).
15:9	0000000b RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74).
8:7	00b RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs, after STRTDLY is complete, that precede the transmit/receive data.
6:4	000b RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods).
3	0b RW	**End of Transfer Data State (ETDS):** • 0 = Low • 1 = Last value (bit 0)
2	0b RW	**Serial Frame Polarity (SFRMP):** • 0 = SSPSFRM is active low • 1 = SSPSFRM is active high
1:0	00b RW	**Serial Bit-rate Clock Mode (SCMODE):** • 00 = Data driven (falling), Data sampled (rising), Idle state (low) • 01 = Data driven (rising), Data sampled (falling), Idle state (low) • 10 = Data driven (rising), Data sampled (falling), Idle state (high) • 11 = Data driven (falling), Data sampled (rising), Idle state (high)

3.31.8 SSP TX Time Slot Active (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in. They are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

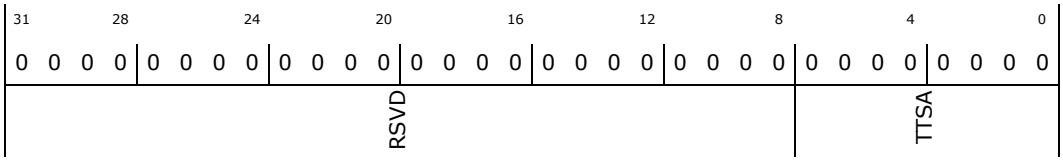
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTSA: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**TX Time Slot Active (TTSA):** • 0 = SSP will not transmit data in this time slot • 1 = SSP will transmit data in this time slot

3.31.9 SSP RX Time Slot Active (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in. They are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read values of these bits are undetermined.

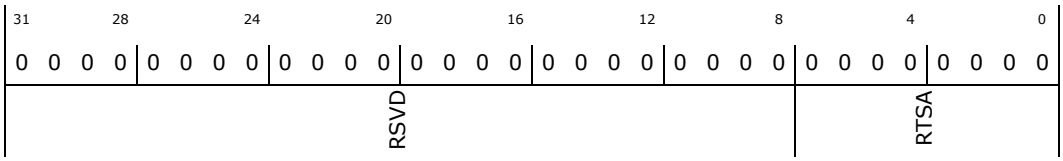
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSRSA: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**RX Time Slot Active (RTSA):** • 0 = SSP will not receive data in this time slot • 1 = SSP will receive data in this time slot

3.31.10 SSP Time Slot Status (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read values of these bits are undetermined.

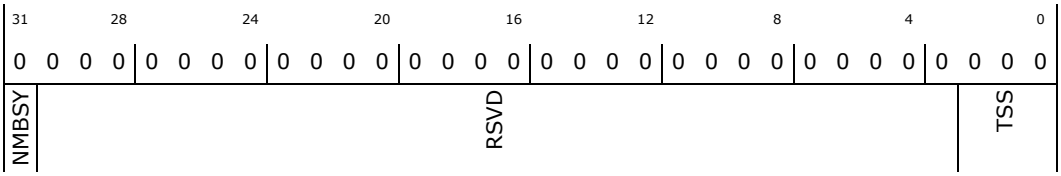
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTSS: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**Network Mode Busy (NMBSY):** • 0 = No frame is currently active (in network mode only) • 1 = SSP is in network mode and a frame is currently active
30:3	0000000h RO	**RSVD:** Reserved
2:0	000b RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active.

3.31.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read values of these bits are undetermined.

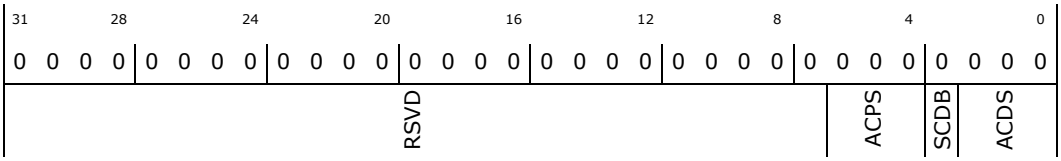
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSACD: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0000000h RO	**RSVD:** Reserved
6:4	000b RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit. • 000b = 5.622MHz • 001b = 11.345MHz • 010b = 12.235MHz • 011b = 14.857MHz • 100b = 32.842MHz • 101b = 48.000MHz • 110b, 111b = Reserved
3	0b RW	**SYSCLK Divider Bypass (SCDB):** • 0 = SYSCLK is divided by 4 before being sent to SSP • 1 = SYSCLK is not divided before being sent to SSP
2:0	000b RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

3.31.12 I2S Transmit FIFO (ITF)—Offset 40h

The I2S Transmit FIFO register is for writing the water mark for the I2S transmit FIFO, and also for reading the number of entries in the I2S transmit FIFO.

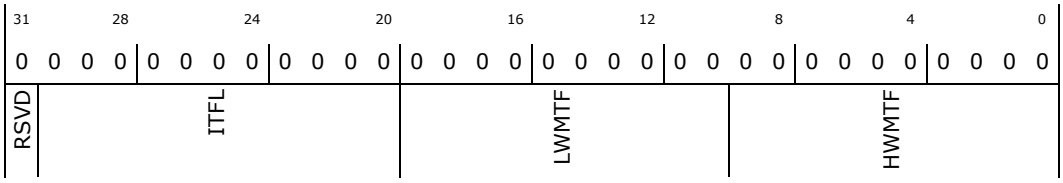
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ITF: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RO	**RSVD:** Reserved
30:20	0b RO	**I2S Transmit FIFO Level (ITFL):** Number of entries in I2S Transmit FIFO.
19:10	0b RW	**Low Water Mark Transmit FIFO (LWMTF):** Set the low water mark of the I2S transmit FIFO.
9:0	0b RW	**High Water Mark Transmit FIFO (HWMTF):** Set the high water mark of the I2S transmit FIFO.

3.31.13 SPI Transmit FIFO (SITF)—Offset 44h

The SPI Transmit FIFO register is for writing the water mark for the SPI transmit FIFO and also for reading the number of entries in the SPI transmit FIFO.

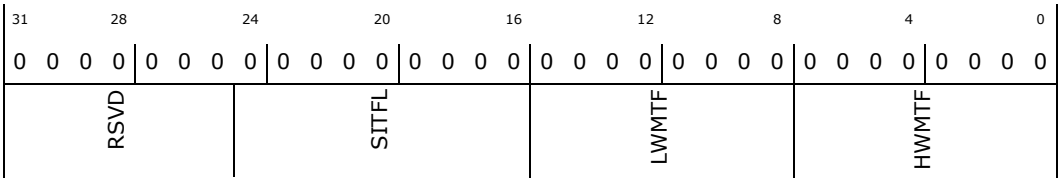
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SITF: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RO	**RSVD:** Reserved
24:16	0b RO	**SPI Transmit FIFO Level (SITFL):** Number of entries in SPI Transmit FIFO.
15:8	0b RW	**Low Water Mark Transmit FIFO (LWMTF):** Set the low water mark of the SPI transmit FIFO.
7:0	0b RW	**High Water Mark Transmit FIFO (HWMTF):** Set the high water mark of the SPI transmit FIFO.

3.31.14 SPI Receive FIFO (SIRF)—Offset 48h

The SPI Receive FIFO register is for writing the water mark for the SPI receive FIFO, and also for reading the number of entries in the SPI receive FIFO.

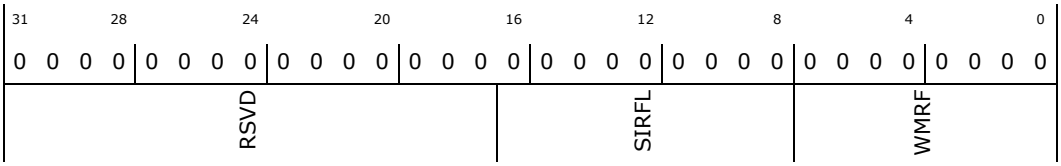
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SIRF: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:17	0h RO	**RSVD:** Reserved
16:8	0b RO	**SPI Receive FIFO Level (SIRFL):** Number of entries in SPI Receive FIFO.
7:0	0b RW	**WMRF:** Water Mark Receive FIFO. Set the water mark of the SPI receive FIFO.

3.31.15 Private Clock Params (PRV_CLOCK_PARAMS)—Offset 400h

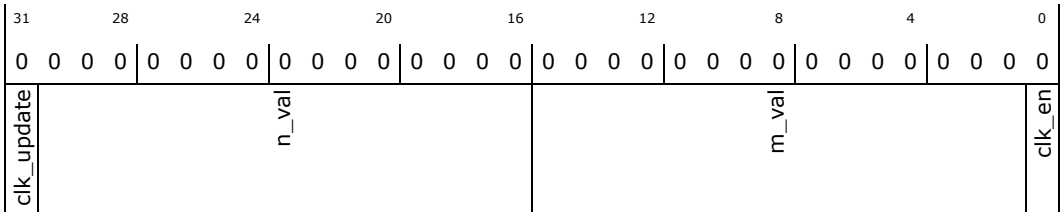
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRV_CLOCK_PARAMS: [BAR] + 400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**clk_update:** Update the clock divider after setting new m and n values.
30:16	0h RW	**N_VAL (n_val):** n value for the m over n divider.
15:1	0h RW	**M_VAL (m_val):** m value for the m over n divider.
0	0h RW	**clk_en:** clk en of the m over n divider.

3.31.16 Software Reset (RESETS)—Offset 404h

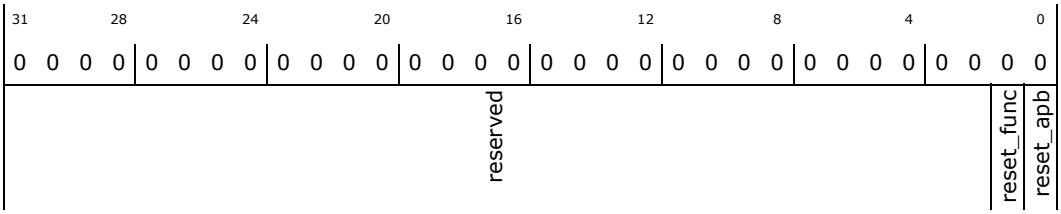
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved
1	0h RW	**reset_func:** Reset the func clock domain.
0	0h RW	**reset_apb:** Reset the apb domain.

3.31.17 General Purpose Register (GENERAL)—Offset 408h

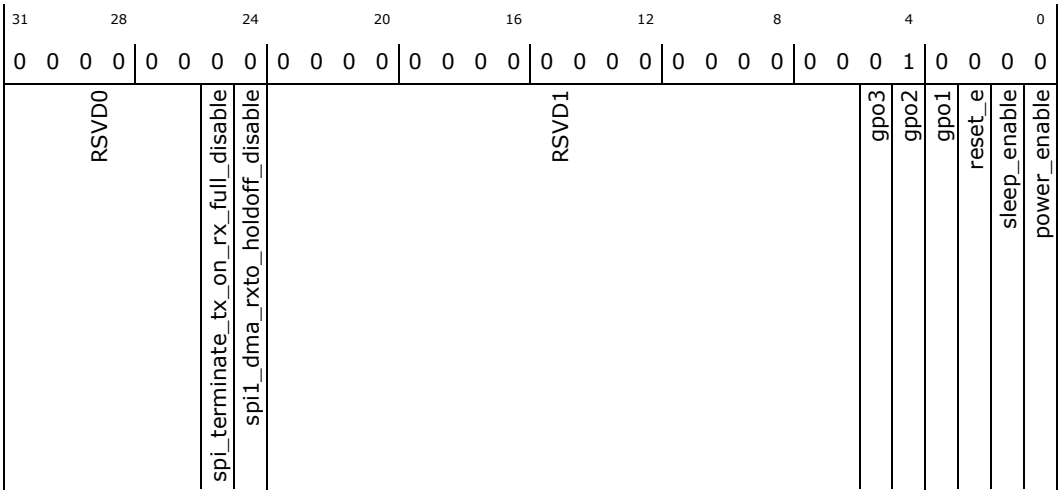
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:26	0b RO	**RSVD0:** Reserved
25	0h RW	**spi_terminate_tx_on_rx_full_disable:** disable terminate tx when rx full

Bit Range	Default & Access	Description
24	0h RW	**spi1_dma_rxto_holdoff_disable:** disable dma hold off
23:6	0b RO	**RSVD1:** Reserved
5	0h RW	**gpo3:** Not applicable.
4	1h RW	**gpo2:** Not applicable.
3	0h RW	**gpo1:** Not applicable.
2	0h RW	**reset_e:** Not applicable.
1	0h RW	**sleep_enable:** Not applicable.
0	0h RW	**power_enable:** Not applicable.

3.31.18 reg_SSP_REG (SSP_REG)—Offset 40Ch

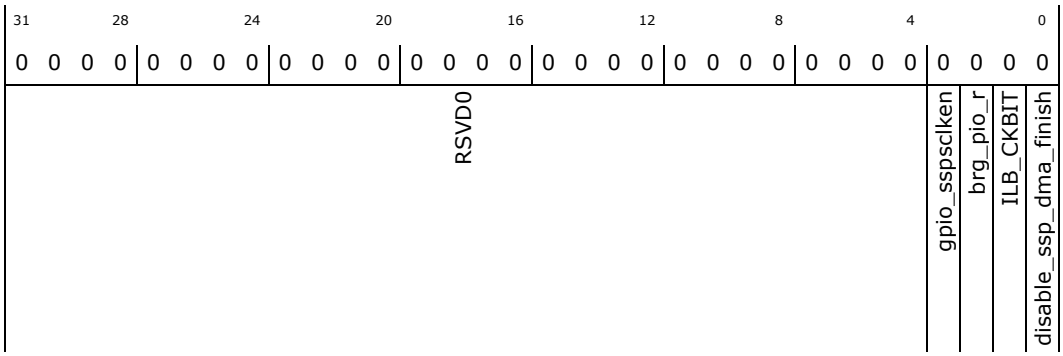
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSP_REG: [BAR] + 40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0b RO	**RSVD0:** Reserved
3	0h RW	**gpio_sspsclken:** Not applicable.
2	0h RW	**brg_pio_r:** Not applicable.

Bit Range	Default & Access	Description
1	0h RW	**ILB_CKBIT:** This bit field is a legacy (chicken bit) bug fix established in previous Intel projects. The driver should set this bit to 0b to ensure correct operation. [IntelRsvd]It is an input to SPI under the following name: bug_2431329_fix_disable.[/IntelRsvd]
0	0h RW	**disable_ssp_dma_finish:** disable ssp dma finish

3.31.19 reg_SPI_CS_CTRL_REG (SPI_CS_CTRL)—Offset 418h

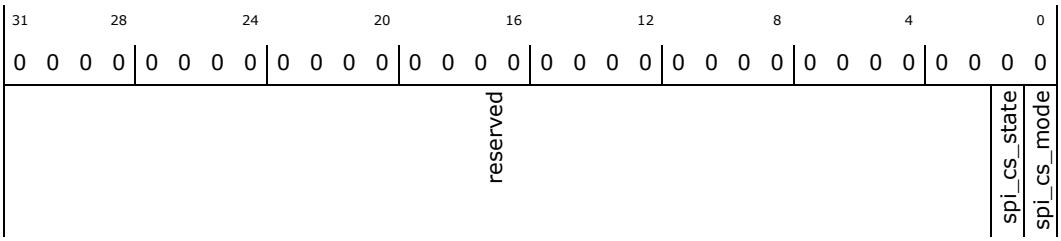
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

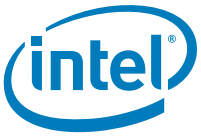
SPI_CS_CTRL: [BAR] + 418h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**reserved:** reserved
1	0h RW	**spi_cs_state:** SW override of CS line in SW mode for spi.
0	0h RW	**spi_cs_mode:** Selects HW mode or SW mode for chip select for spi.



3.32 SIO I2C0 PCI Configuration Registers

Table 40. Summary of SIO I2C0 PCI Configuration Registers—0/24/1

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2532	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2533	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2534	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2535	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2536	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2536	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2537	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2538	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2538	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2539	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2539	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2540	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2541	00000000h

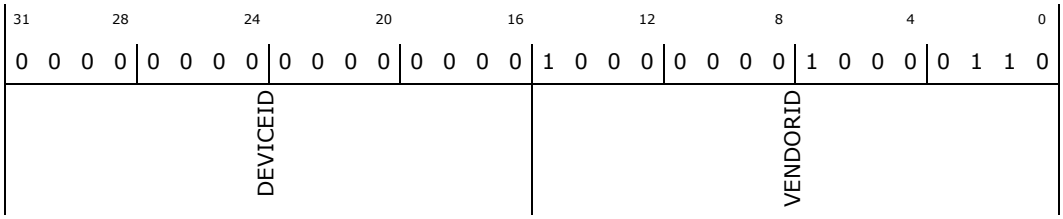
3.32.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:24, F:1] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

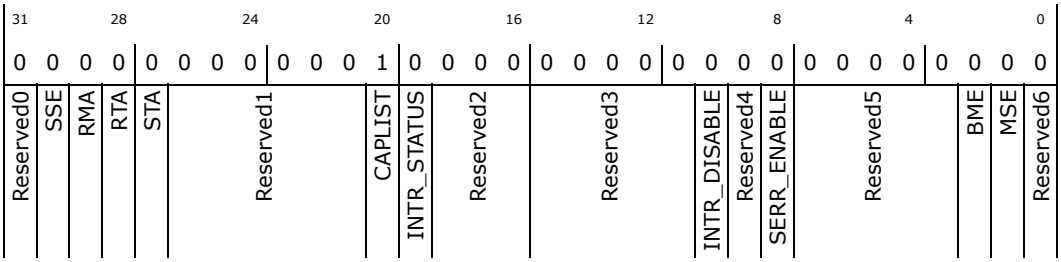
3.32.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:24, F:1] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

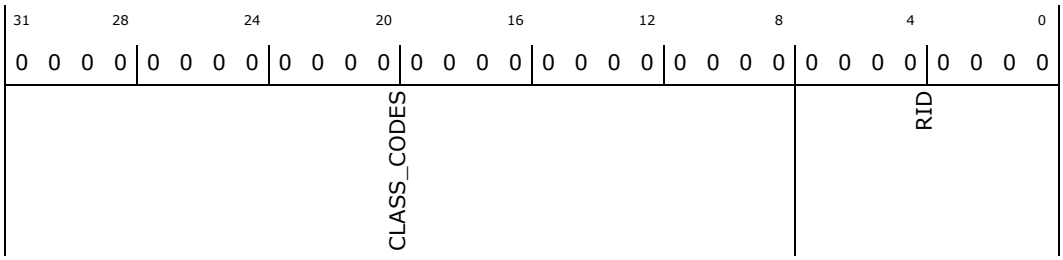
3.32.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:24, F:1] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

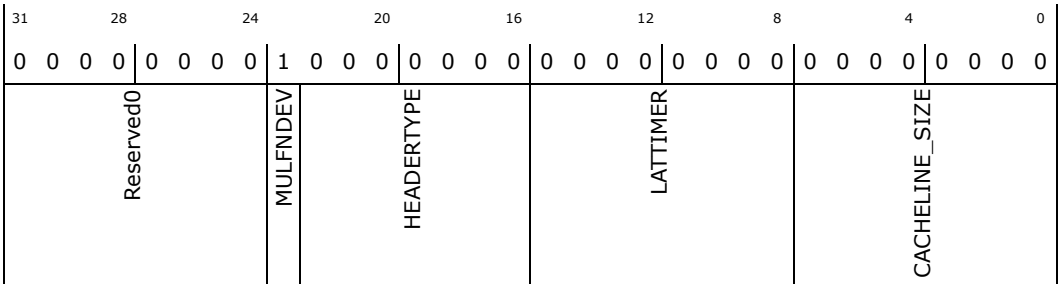
3.32.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:24, F:1] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

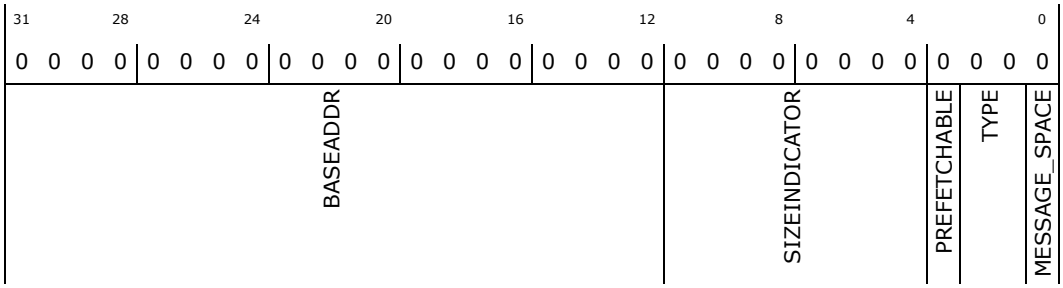
3.32.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

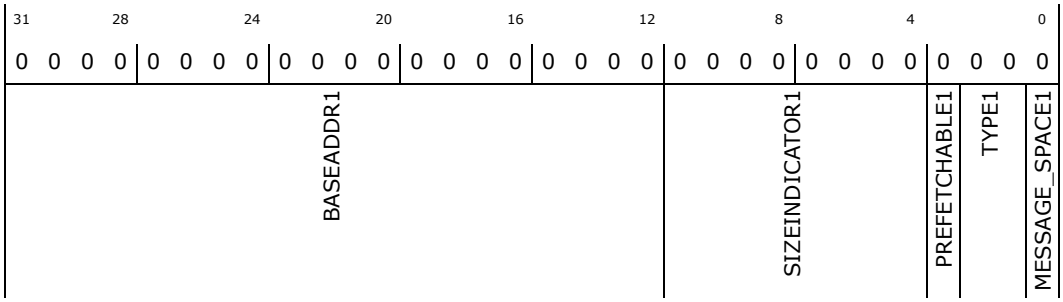
3.32.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:24, F:1] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

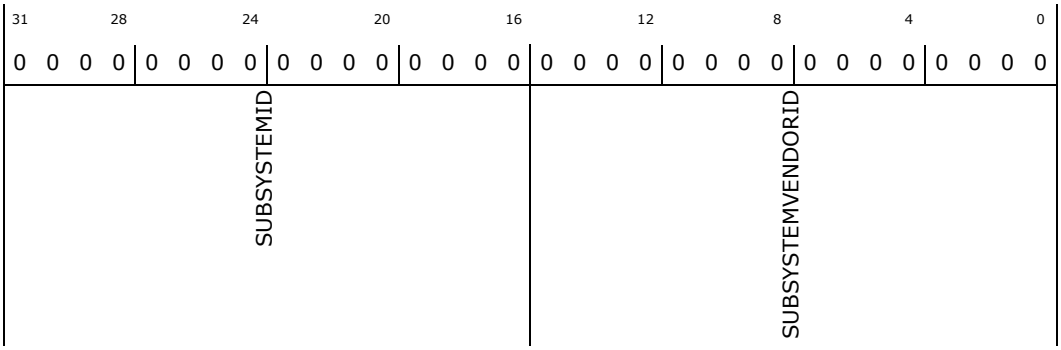
3.32.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:24, F:1] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

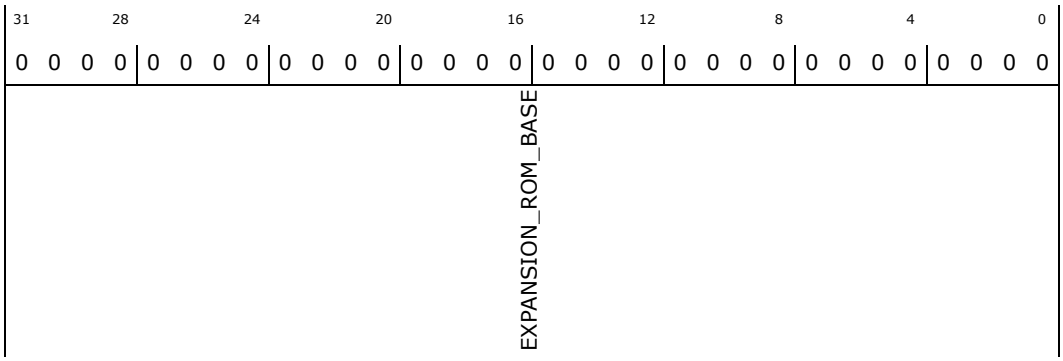
3.32.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:24, F:1] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

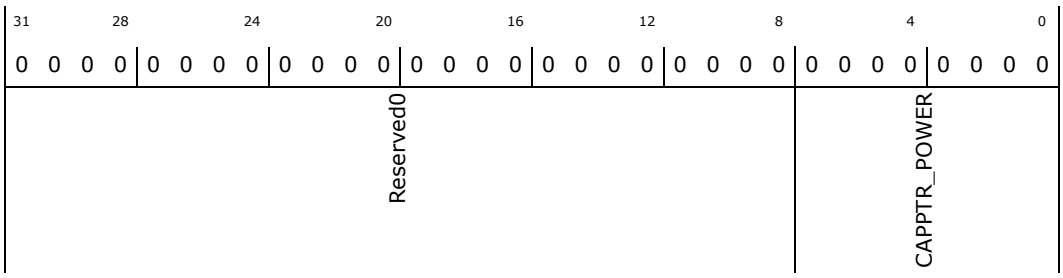
3.32.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:24, F:1] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

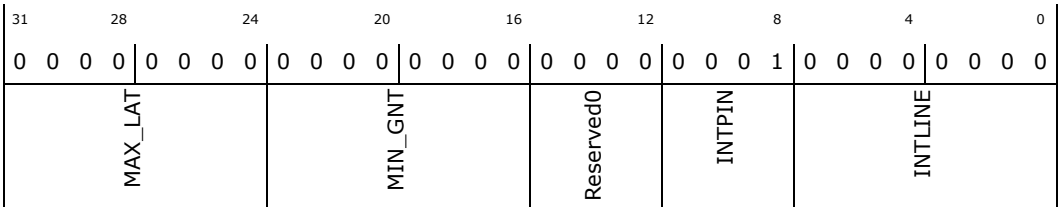
3.32.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

INTERRUPTREG: [B:0, D:24, F:1] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

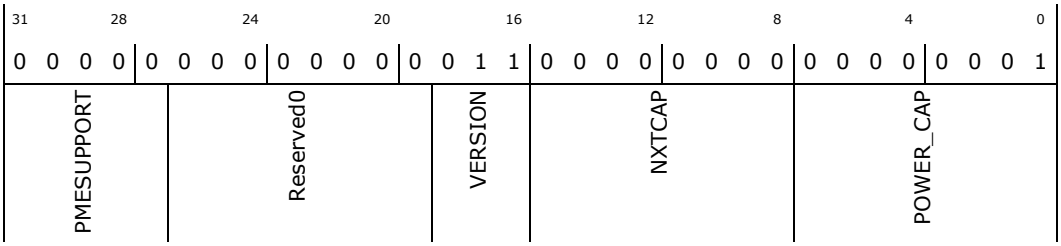
3.32.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

POWERCAPID: [B:0, D:24, F:1] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

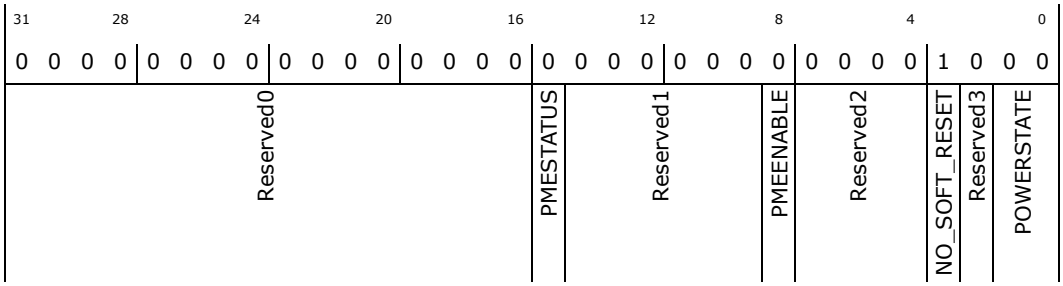
3.32.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:24, F:1] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

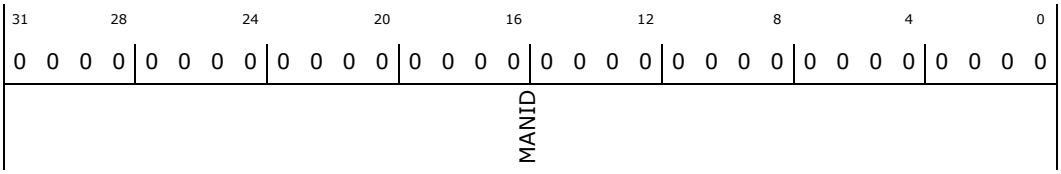
3.32.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:24, F:1] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

3.33 SIO I²C0 Memory Mapped I/O Registers

Table 41. Summary of SIO I²C0 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 2544	0000007Fh
4h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 2545	00001055h
8h	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 2546	00000055h
Ch	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 2547	00000001h
10h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 2548	00000000h
14h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 2549	00000190h
18h	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 2550	000001D6h
1Ch	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 2550	0000003Ch
20h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 2551	00000082h
24h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 2552	0000000Ch
28h	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 2553	00000020h
2Ch	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 2554	00000000h
30h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 2555	000008FFh
34h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 2556	00000000h
38h	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 2558	00000010h
3Ch	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 2558	00000010h
40h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 2559	00000000h
44h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 2559	00000000h
48h	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 2560	00000000h
4Ch	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 2560	00000000h
50h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 2561	00000000h

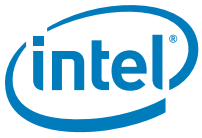


Table 41. Summary of SIO I²C0 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
54h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 2562	00000000h
58h	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 2562	00000000h
5Ch	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 2563	00000000h
60h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 2563	00000000h
64h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 2564	00000000h
68h	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 2564	00000000h
6Ch	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 2565	00000000h
70h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 2566	00000006h
74h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 2567	00000000h
78h	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 2568	00000000h
7Ch	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 2568	00000001h
80h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 2569	00000000h
84h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 2571	00000000h
88h	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 2572	00000000h
8Ch	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 2573	00000000h
90h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 2573	00000000h
94h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 2574	00000064h
98h	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 2575	00000001h
9Ch	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 2576	00000000h
A0h	4	"IC_FS_SPKLEN—Offset A0h" on page 2577	00000005h
A4h	4	"IC_HS_SPKLEN—Offset A4h" on page 2577	00000002h
F4h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 2578	00FFFFEEh
F8h	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 2579	3131352Ah
FCh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 2580	44570140h
800h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 2580	00000000h

Table 41. Summary of SIO I2C0 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
804h	4	"Software Reset (RESETS)—Offset 804h" on page 2581	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 2582	55000000h
818h	4	"I2C_ACK_COUNT—Offset 818h" on page 2583	00000000h
820h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 2584	00000000h
824h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 2584	00000000h

3.33.1 I2C Control Register (IC_CON)—Offset 0h

If configuration parameter I2C_DYNAMIC_TAR_UPDATE = 0, all bits are Read/Write.

If I2C_DYNAMIC_TAR_UPDATE = 1, bit 4 is Read-only.

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

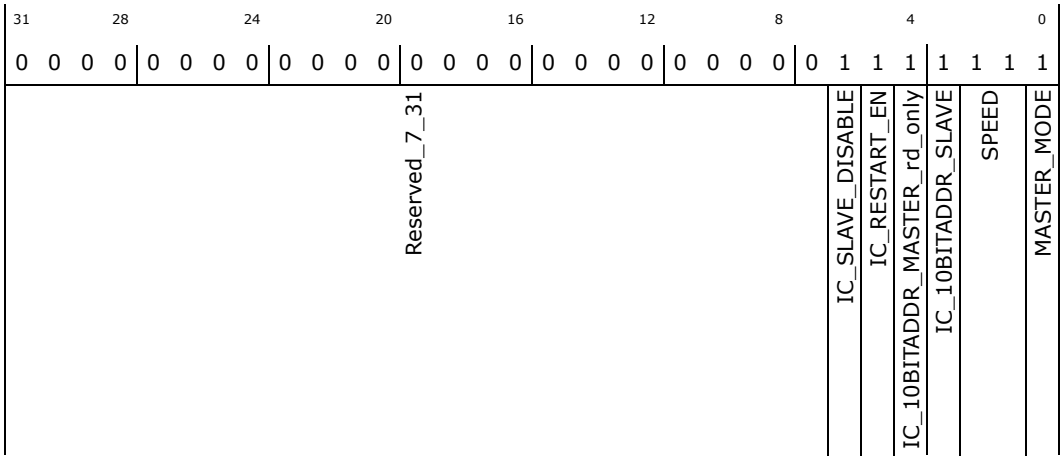
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CON: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

3.33.2 I2C Target Address Register (IC_TAR)—Offset 4h

If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to No (0), this register is 12 bits wide, and bits 15:12 are reserved. Writes to this register succeed only when IC_ENABLE is set to 0.

However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND

- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

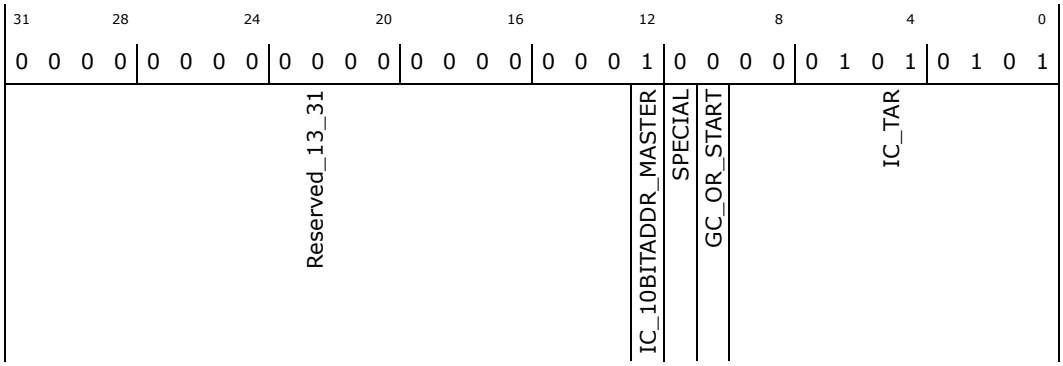
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TAR: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00001055h



Bit Range	Default & Access	Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

3.33.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

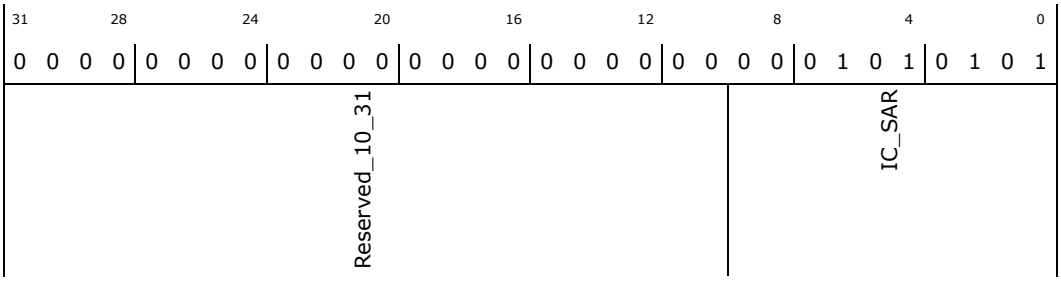
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SAR: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000055h



Bit Range	Default & Access	Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.33.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

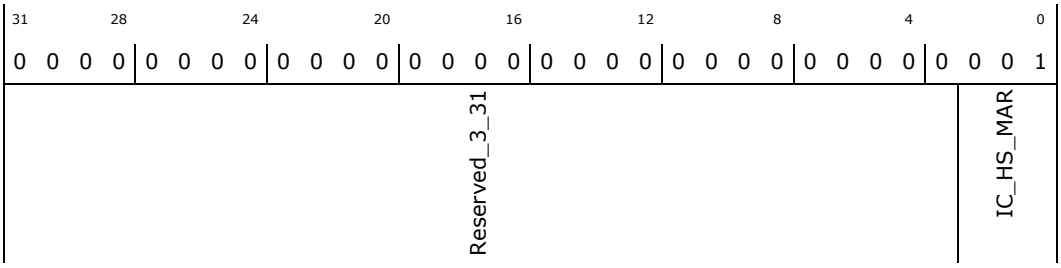
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_MADDR: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.33.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

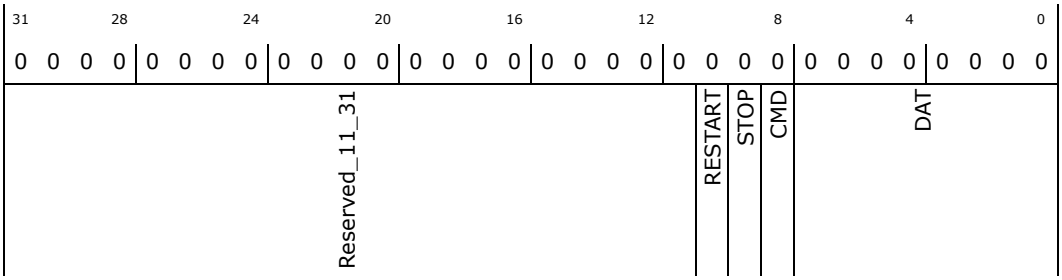
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DATA_CMD: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:11	0b RW	**Reserved_11_31:** Reserved.

Bit Range	Default & Access	Description
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/ received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

3.33.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

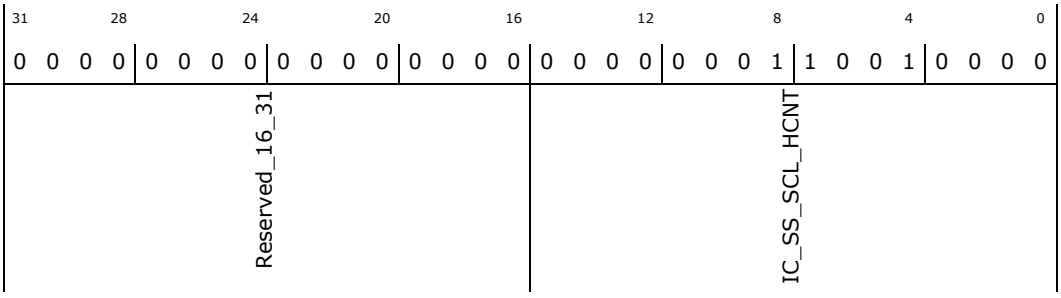
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_HCNT: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000190h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.33.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

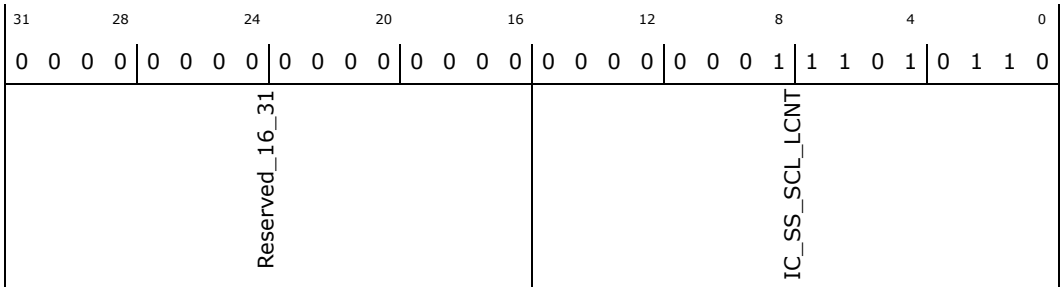
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_LCNT: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 000001D6h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.33.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

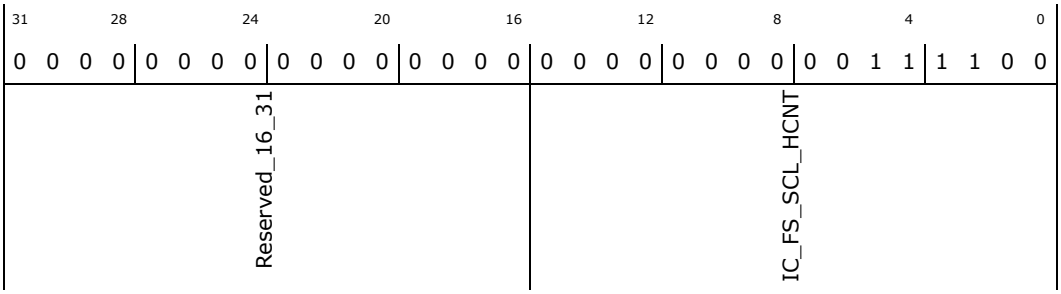
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_HCNT: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.33.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to 'IC_CLK Frequency Configuration' in the Synopsis DesignWare DW_apb_i2c Databook.

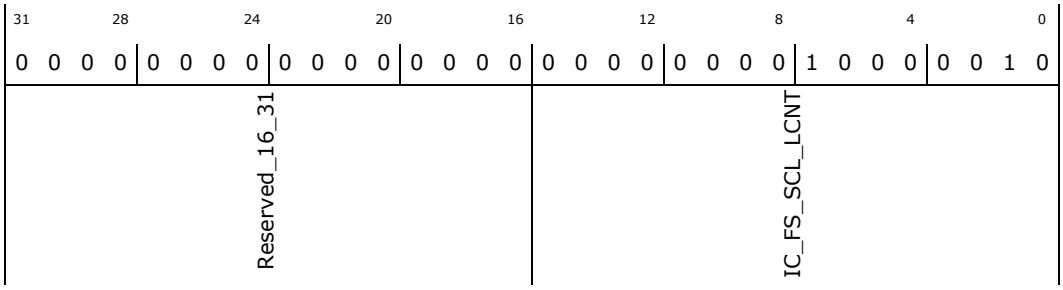
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_LCNT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000082h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.33.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* .

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

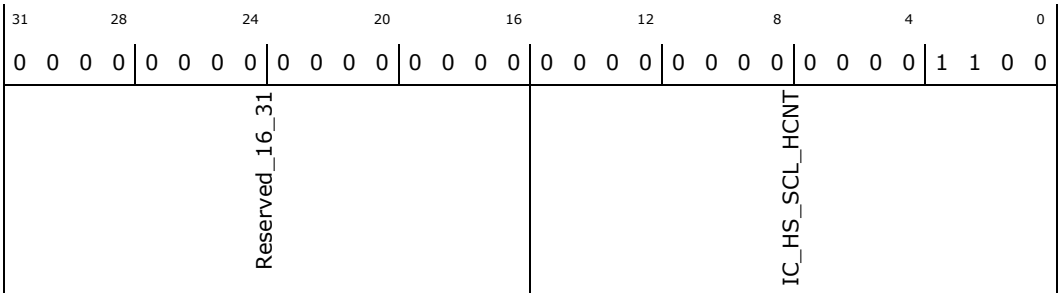
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_HCNT: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.33.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* in the Synopsis DesignWare DW_apb_i2c Databook.

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

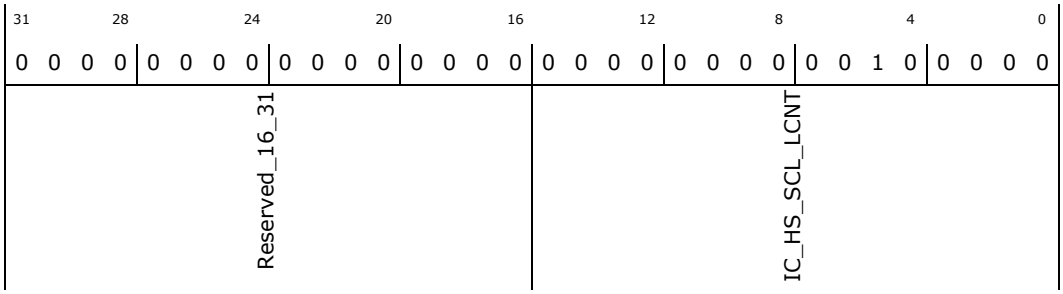
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_LCNT: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000020h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.33.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

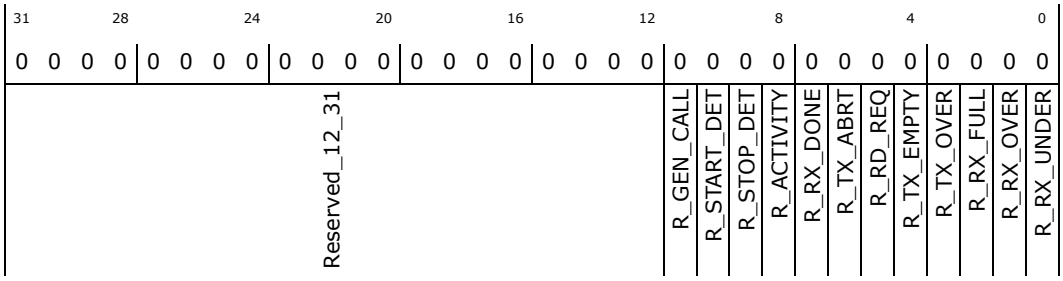
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_INTR_STAT: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.

Bit Range	Default & Access	Description
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

3.33.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

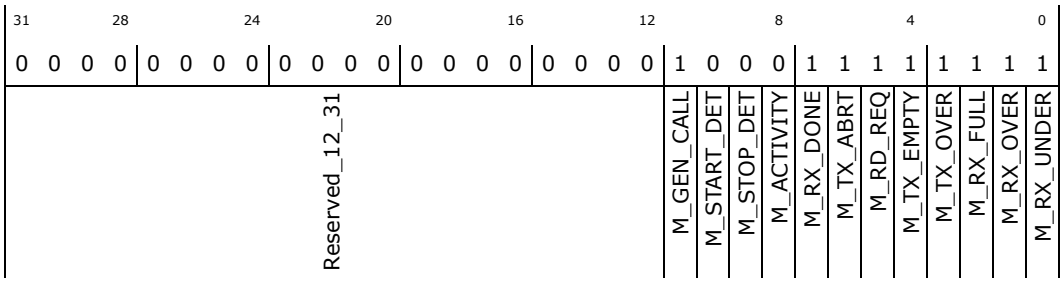
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_INTR_MASK: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 000008FFh



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

3.33.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

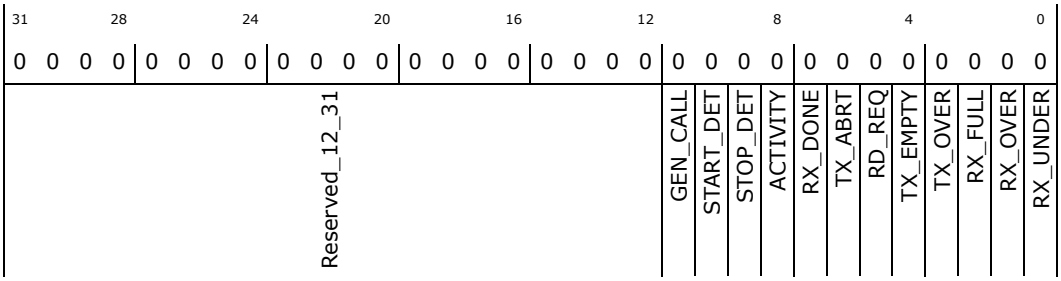
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RAW_INTR_STAT: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

3.33.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

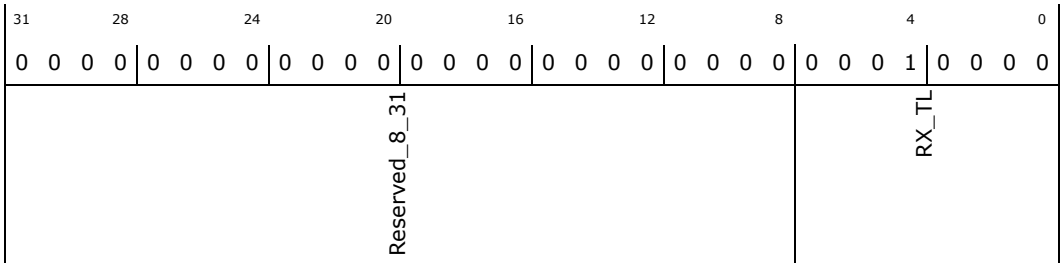
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RX_TL: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.33.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

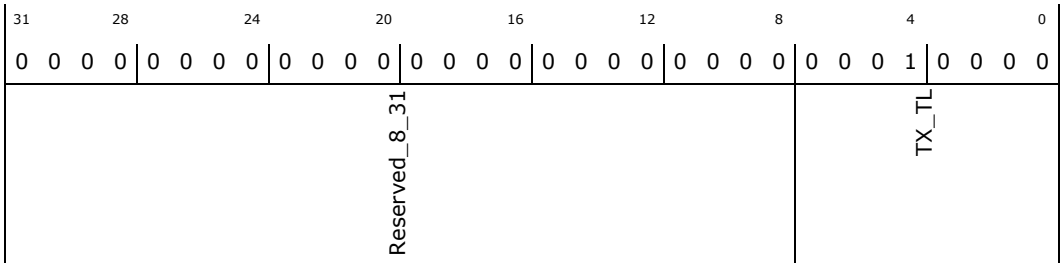
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_TL: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.33.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

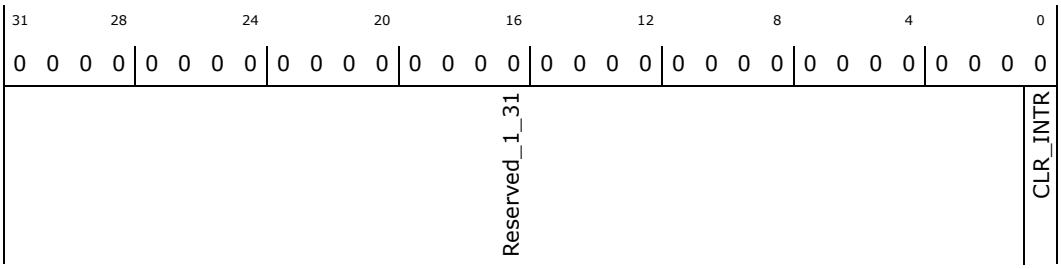
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_INTR: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

3.33.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

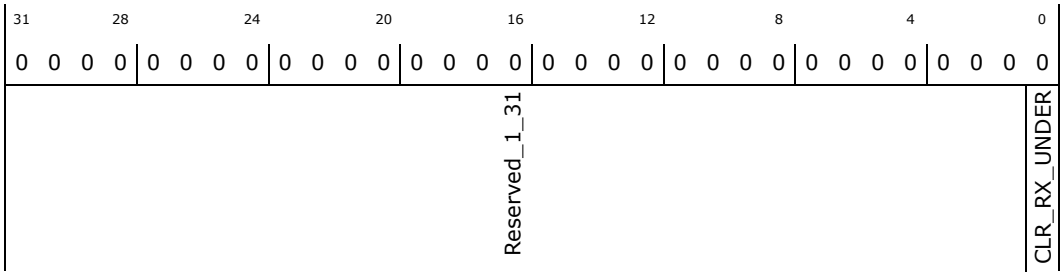
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_UNDER: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

3.33.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

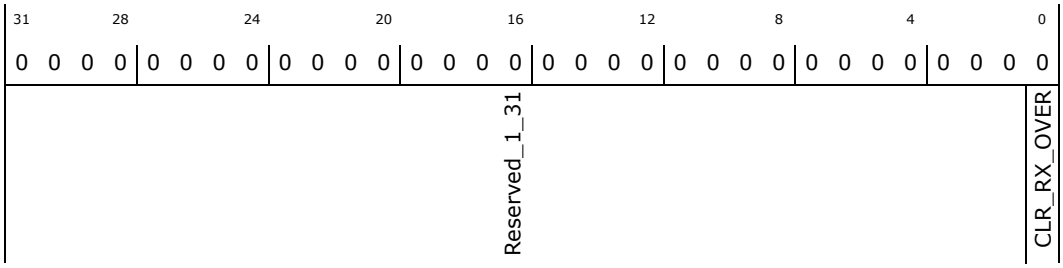
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_OVER: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

3.33.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

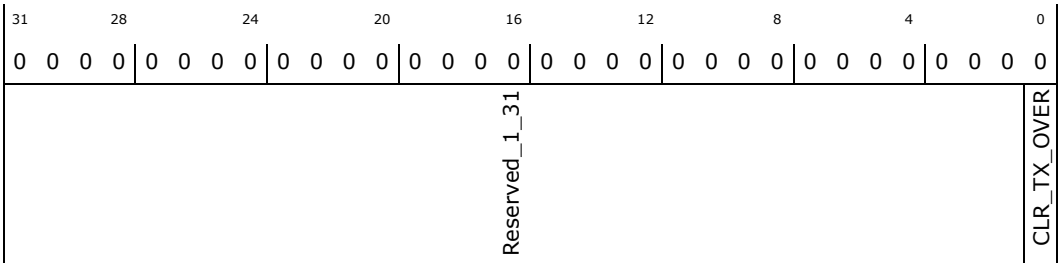
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_OVER: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

3.33.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

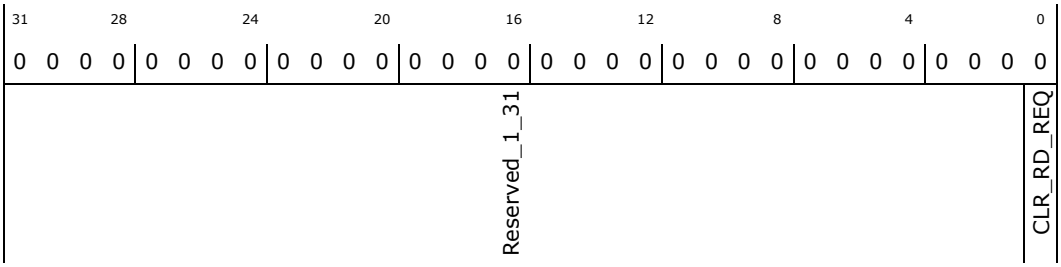
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RD_REQ: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

3.33.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

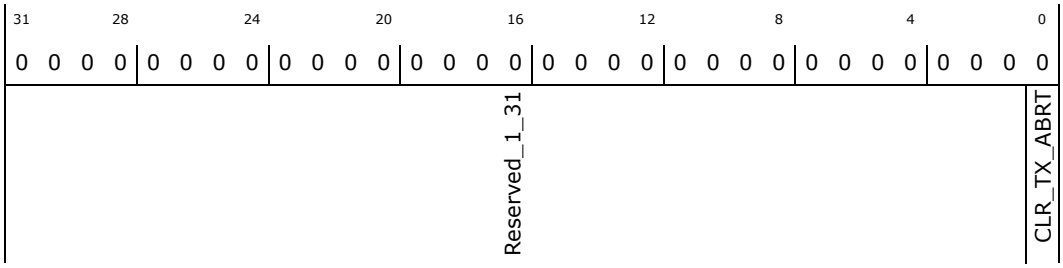
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_ABRT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

3.33.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

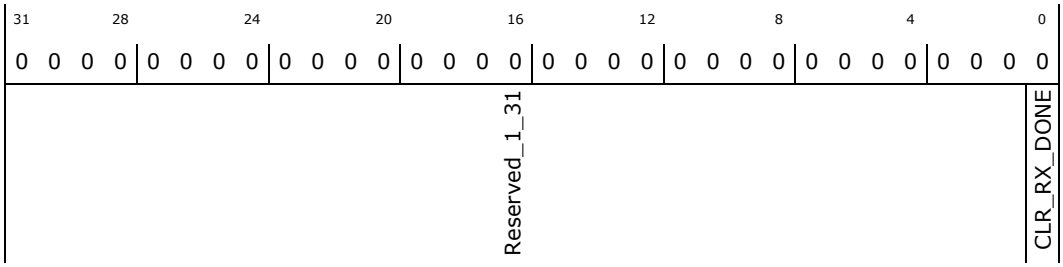
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_DONE: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

3.33.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

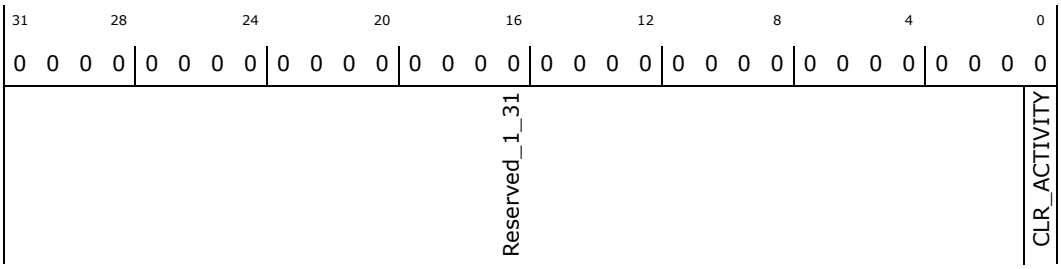
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_ACTIVITY: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

3.33.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

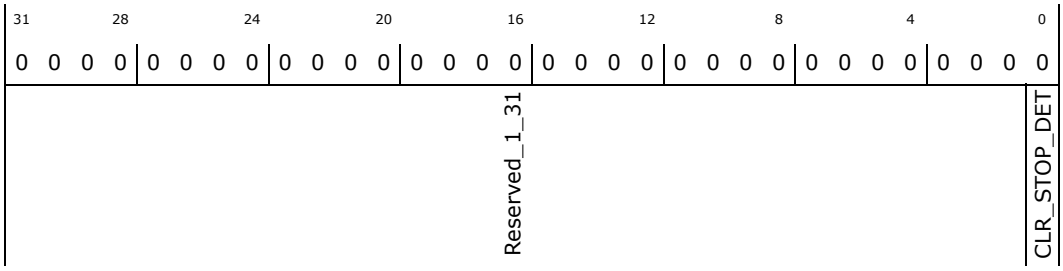
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_STOP_DET: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

3.33.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

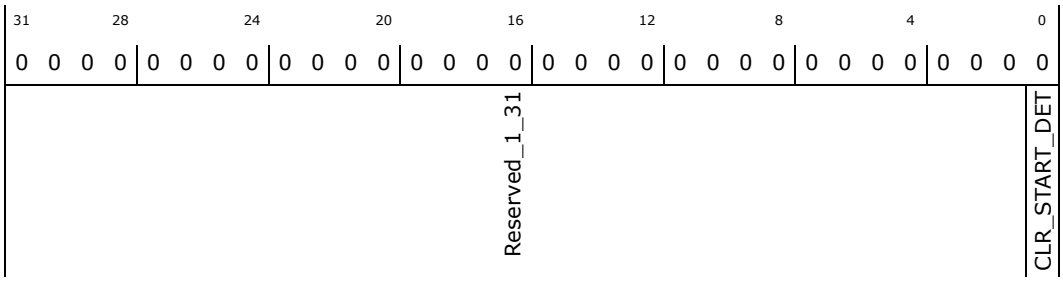
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_START_DET: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

3.33.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

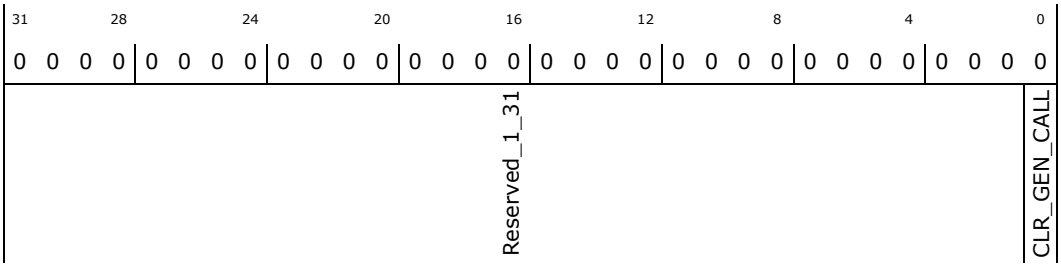
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_GEN_CALL: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

3.33.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

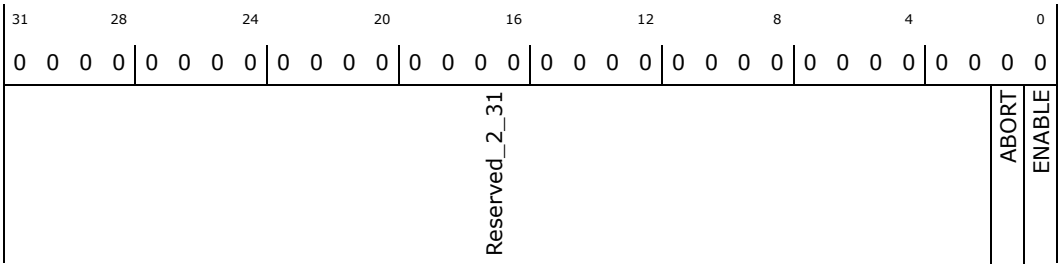
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.

Bit Range	Default & Access	Description
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

3.33.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

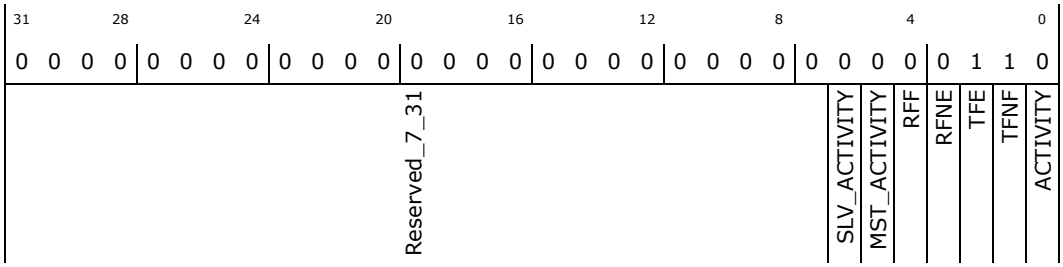
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_STATUS: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.

Bit Range	Default & Access	Description
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

3.33.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

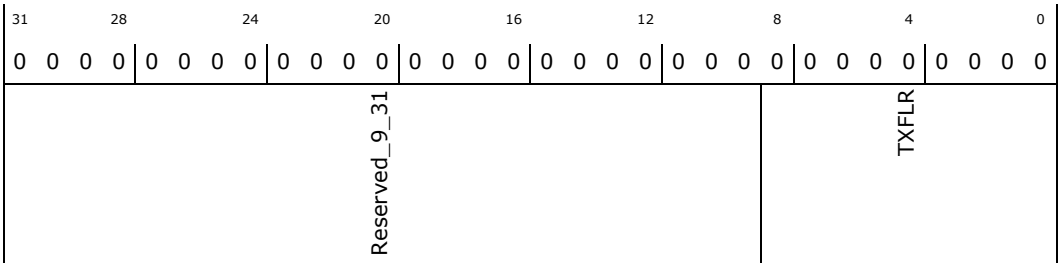
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TXFLR: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

3.33.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

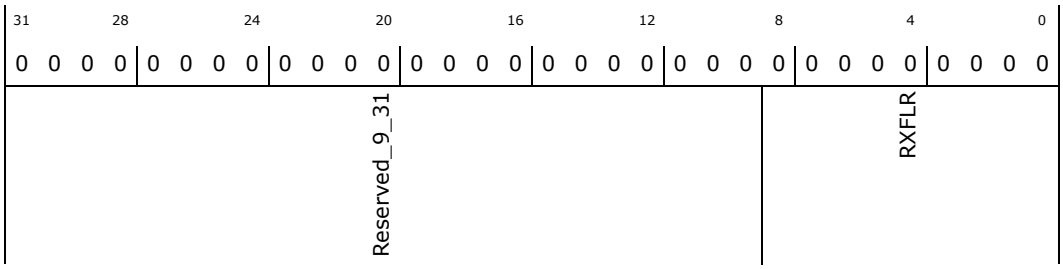
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RXFLR: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

3.33.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implementedone cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

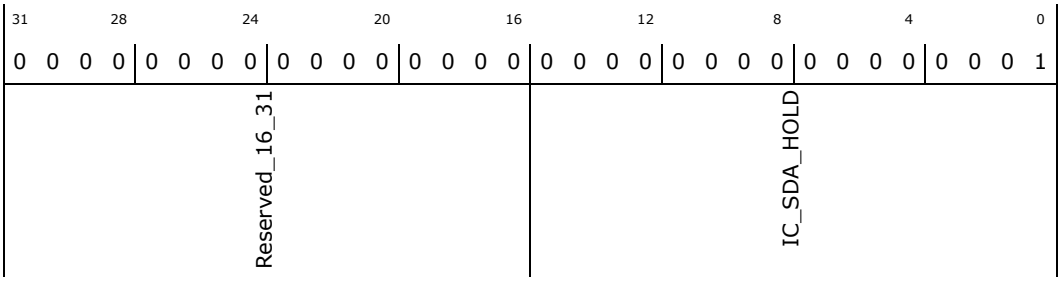
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_HOLD: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

3.33.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

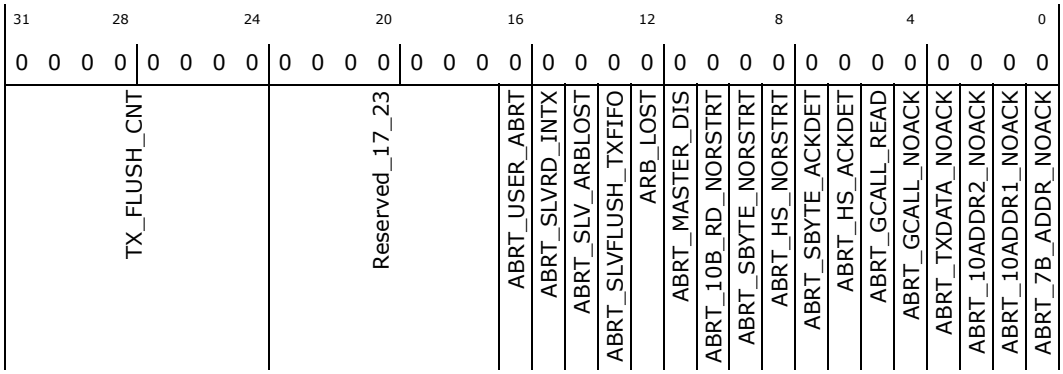
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_ABRT_SOURCE: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).

Bit Range	Default & Access	Description
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

3.33.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. This register only exists when the IC_SLV_DATA_NACK_ONLY parameter is set to 1. When this parameter disabled, this register does not exist and writing to the registers address has no effect. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

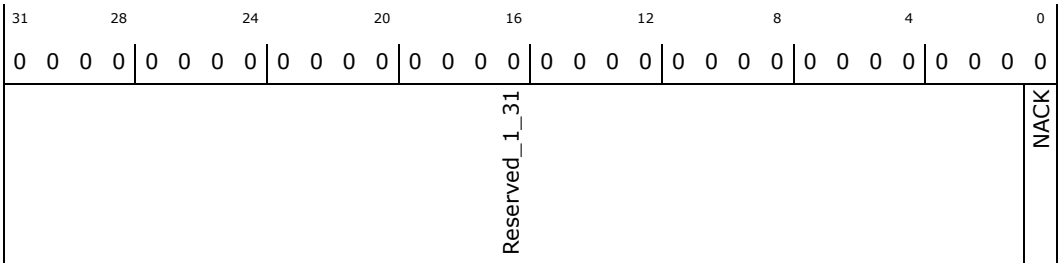
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SLV_DATA_NACK_ONLY: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

3.33.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

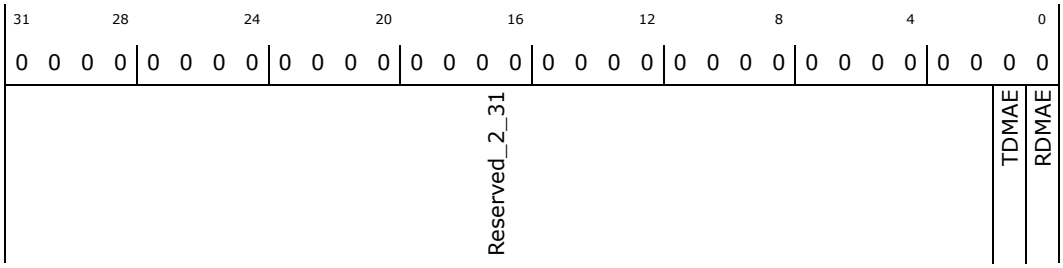
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_CR: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled

Bit Range	Default & Access	Description
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

3.33.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

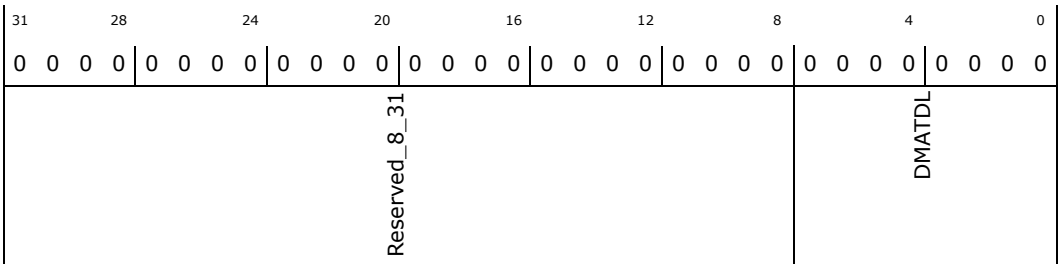
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_TDLR: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

3.33.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

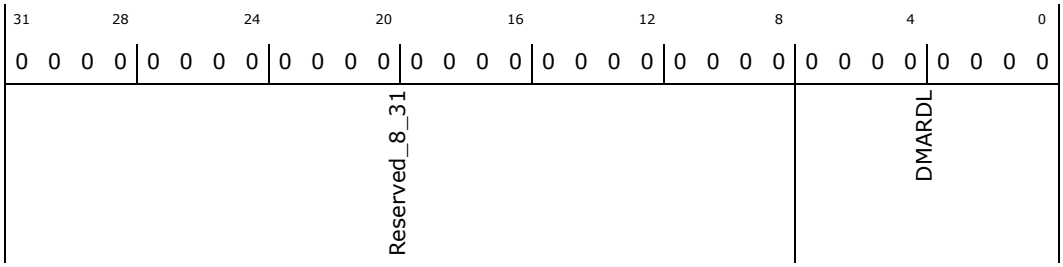
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_RDLR: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

3.33.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2.

NOTE: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

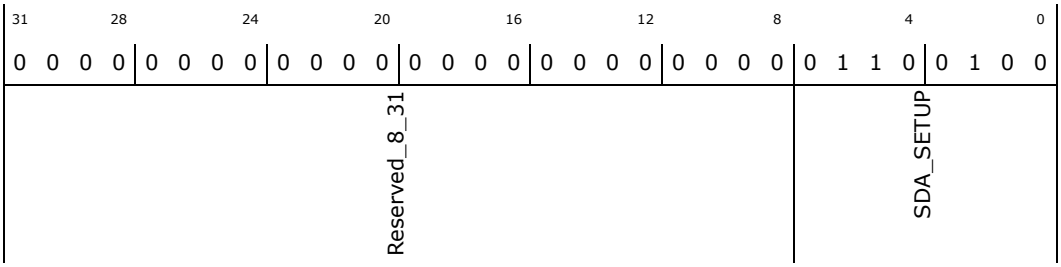
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_SETUP: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000064h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

3.33.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

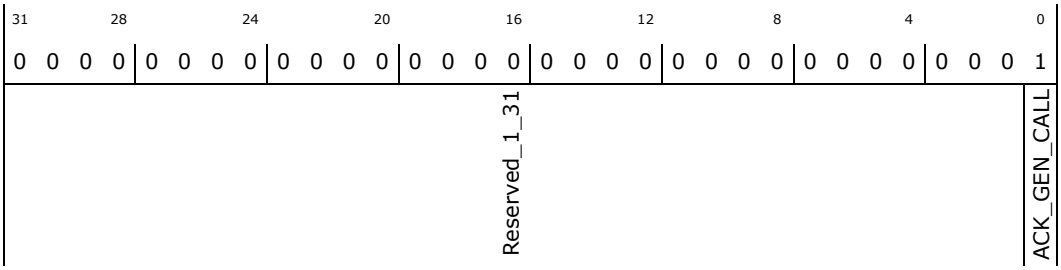
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ACK_GENERAL_CALL: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

3.33.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

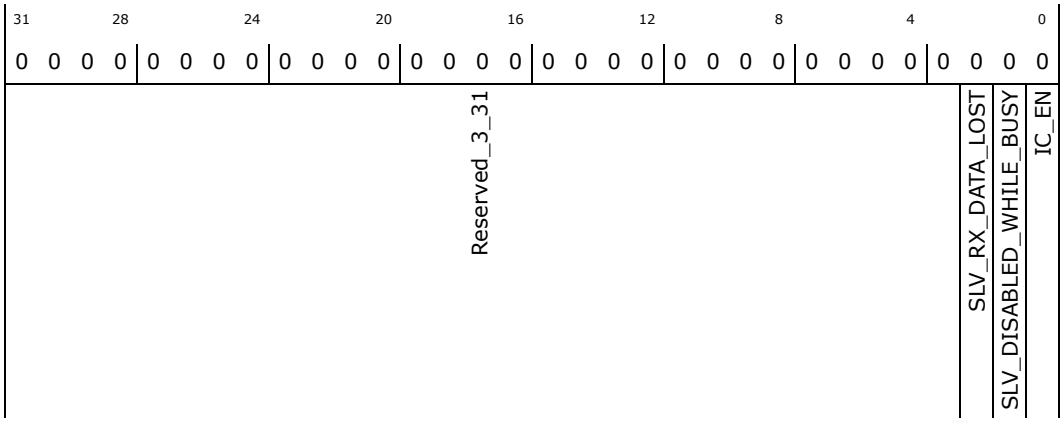
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE_STATUS: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

3.33.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

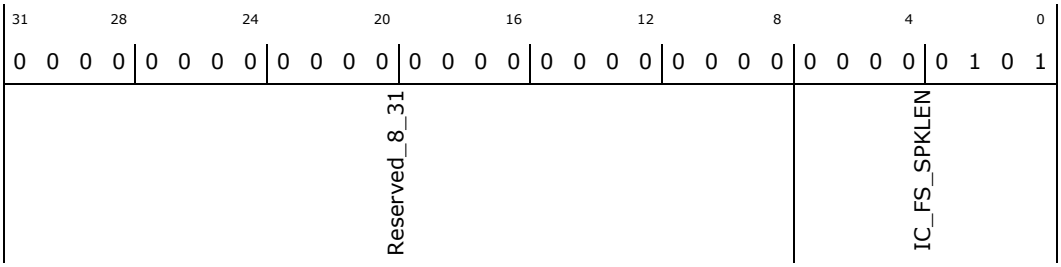
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SPKLEN: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000005h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. **Reset value:** IC_DEFAULT_FS_SPKLEN configuration parameter

3.33.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the

I2C Bus Specification. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

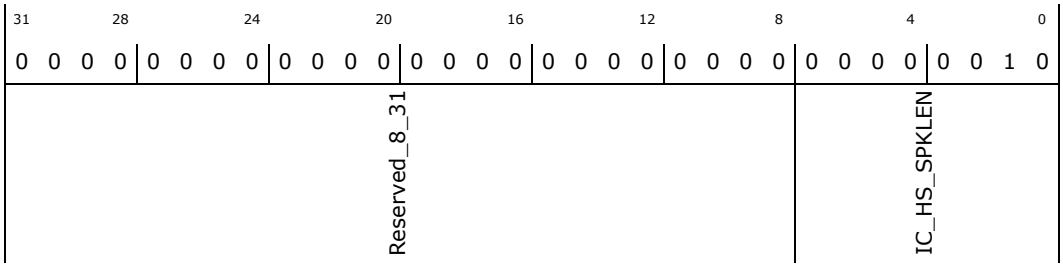
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SPKLEN: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. This register is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3. **Reset value:** IC_DEFAULT_HS_SPKLEN configuration parameter.

3.33.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

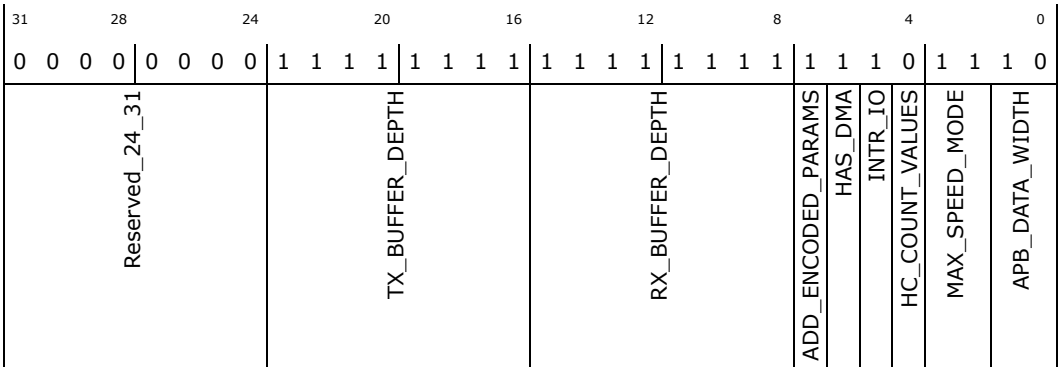
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_PARAM_1: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

3.33.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

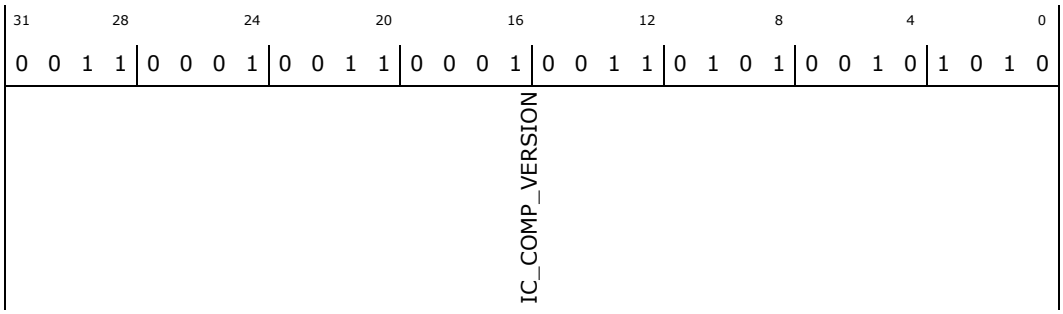
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_VERSION: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

3.33.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

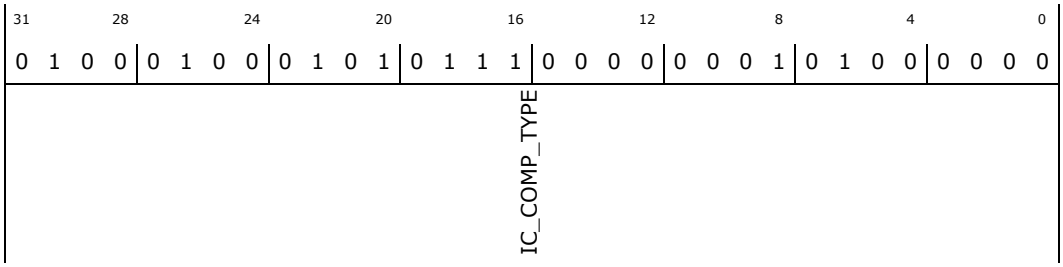
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_TYPE: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 44570140h



Bit Range	Default & Access	Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

3.33.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

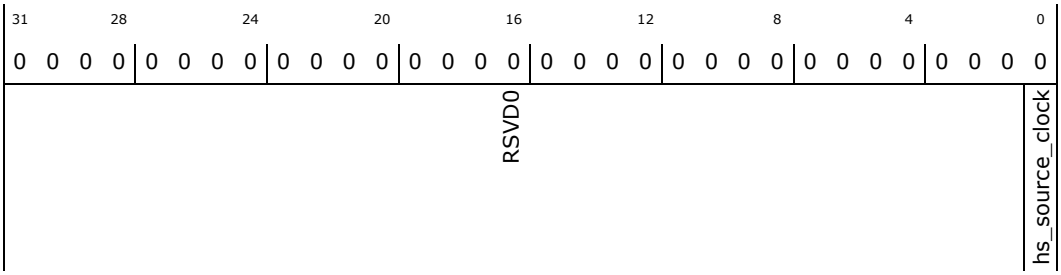
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CLOCK_PARAMS: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

3.33.47 Software Reset (RESETS)—Offset 804h

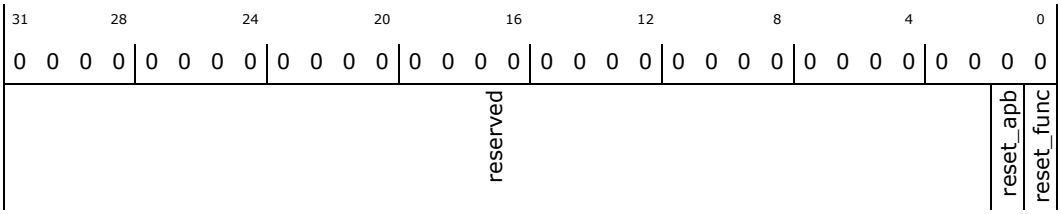
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.33.48 General Purpose Register (GENERAL)—Offset 808h

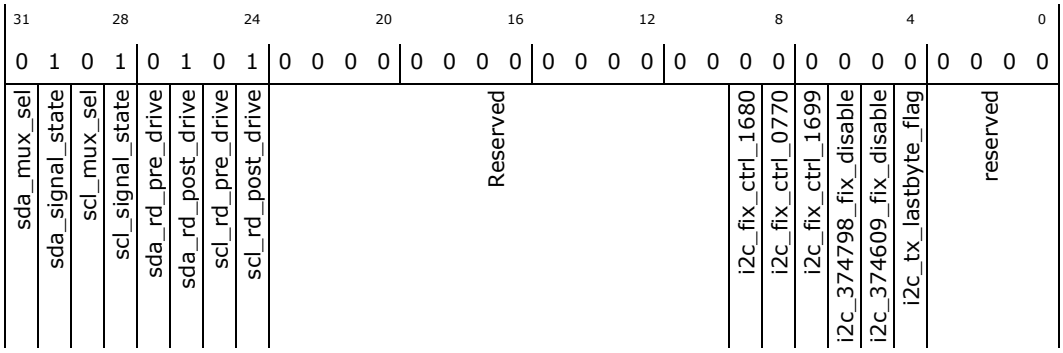
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 55000000h



Bit Range	Default & Access	Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)

Bit Range	Default & Access	Description
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

3.33.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

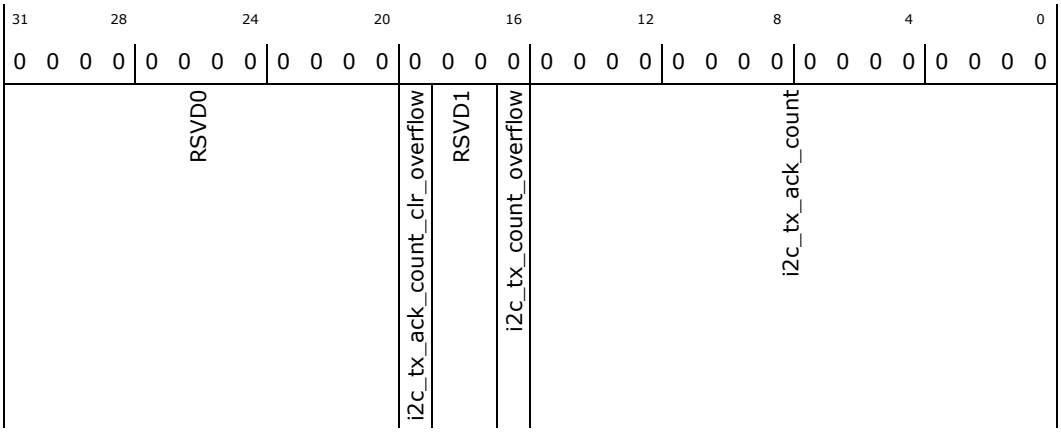
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_ACK_COUNT: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

3.33.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

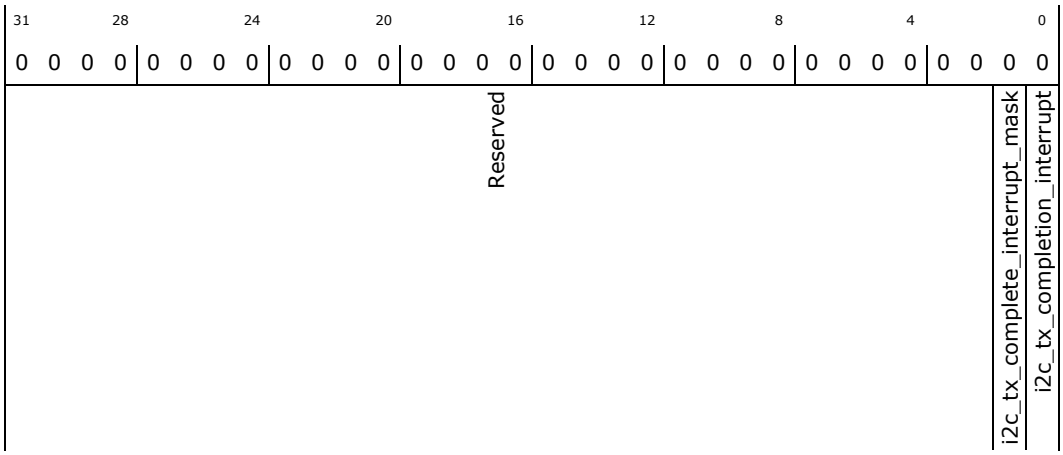
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_TX_COMPLETE_INTR_STAT: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

3.33.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

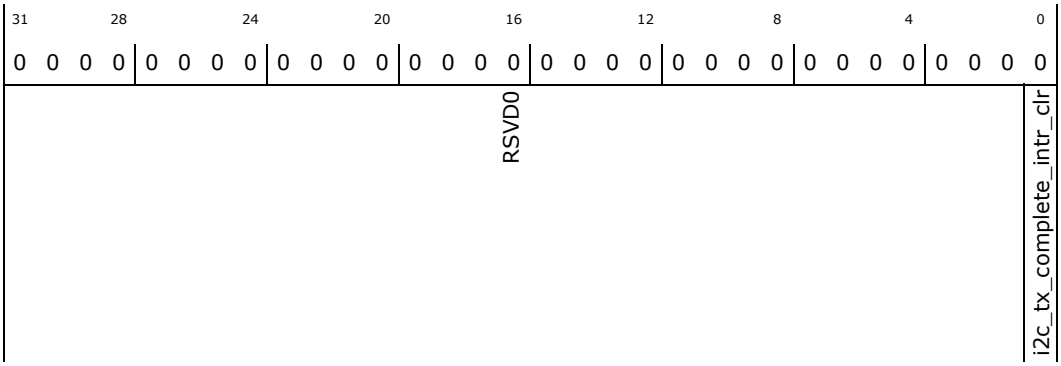
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

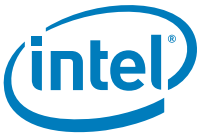
I2C_TX_COMPLETE_INTR_CLR: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt



3.34 SIO I2C1 PCI Configuration Registers

Table 42. Summary of SIO I2C1 PCI Configuration Registers—0/24/2

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2586	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2587	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2588	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2589	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2590	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2590	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2591	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2592	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2592	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2593	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2593	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2594	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2595	00000000h

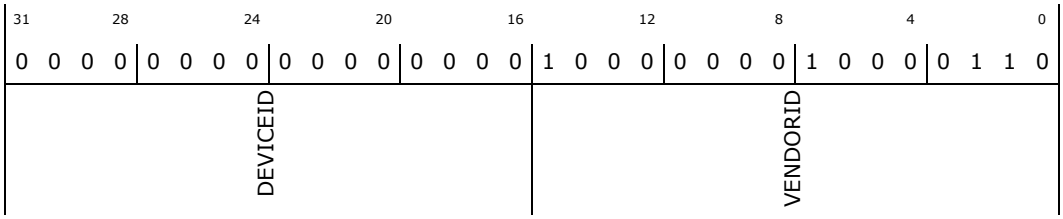
3.34.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:24, F:2] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

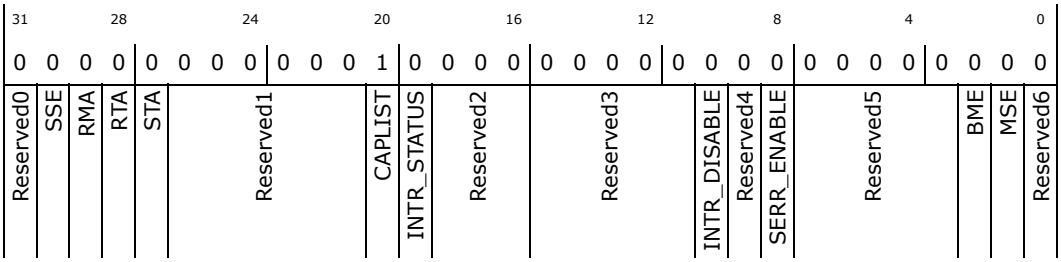
3.34.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:24, F:2] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

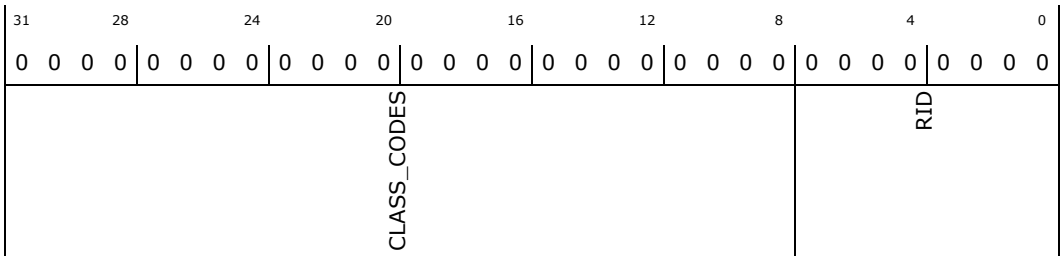
3.34.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:24, F:2] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

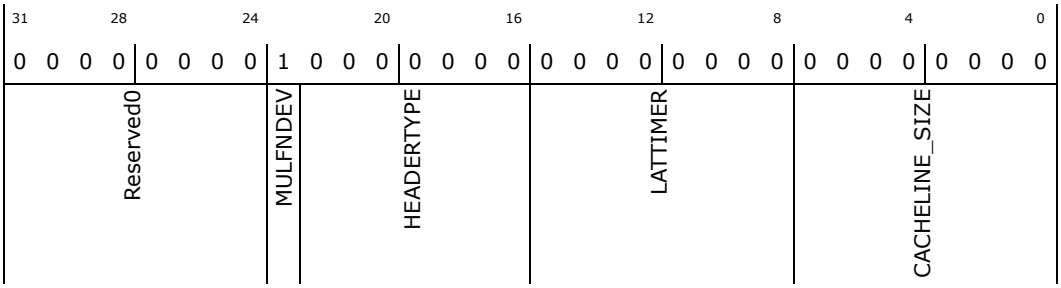
3.34.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:24, F:2] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

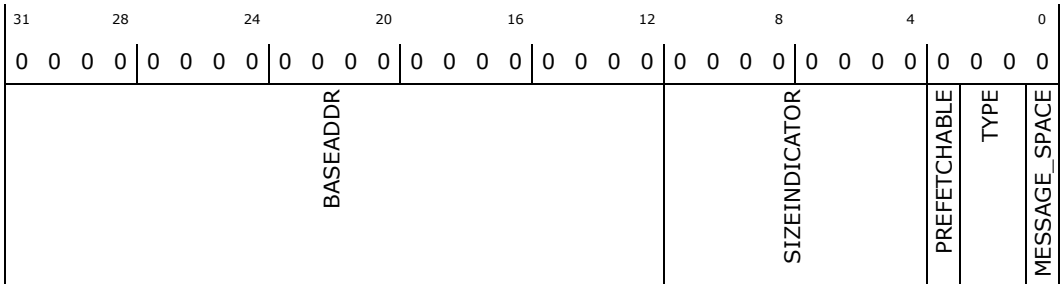
3.34.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

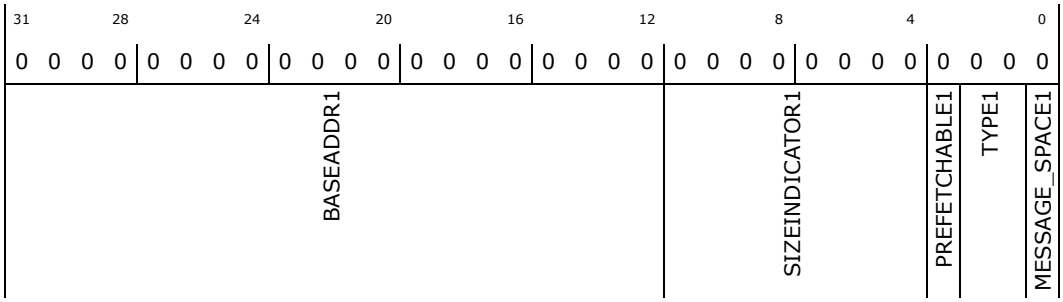
3.34.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:24, F:2] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

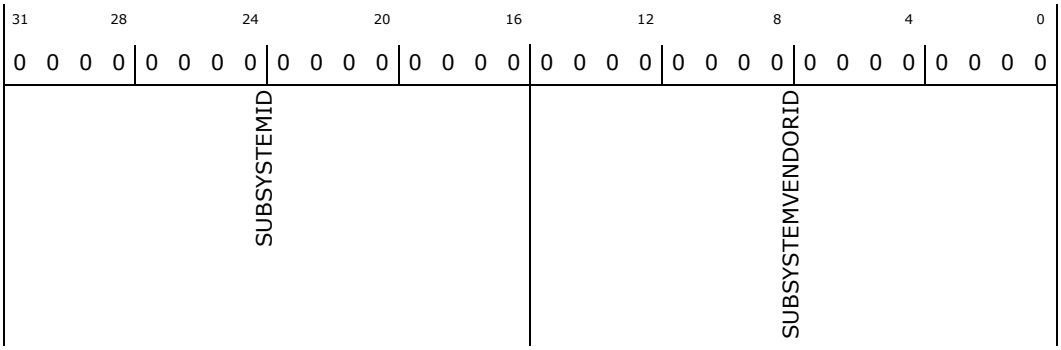
3.34.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:24, F:2] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

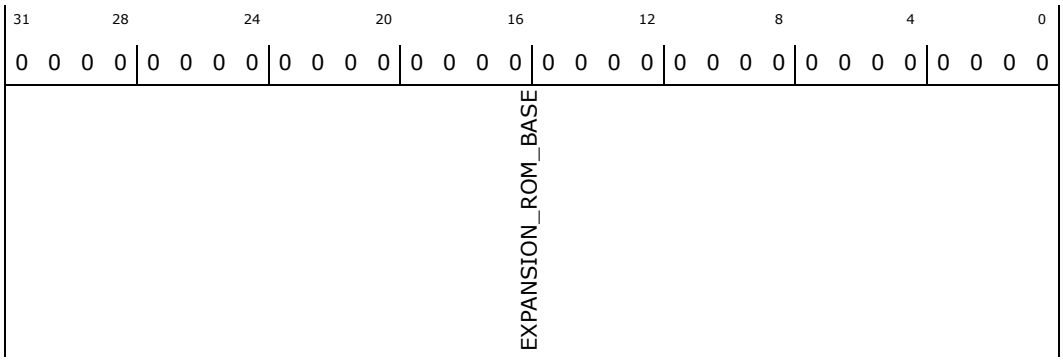
3.34.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:24, F:2] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

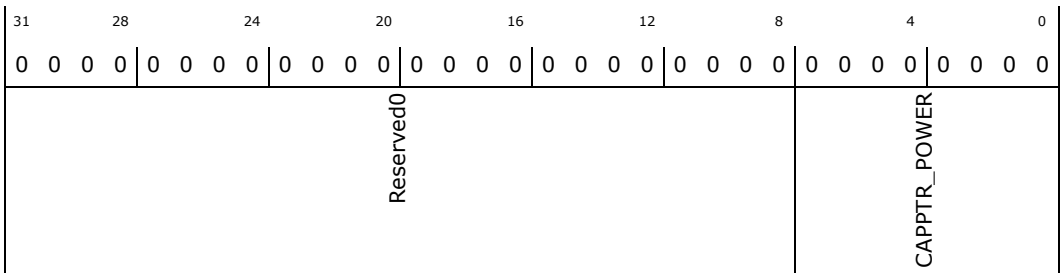
3.34.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:24, F:2] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

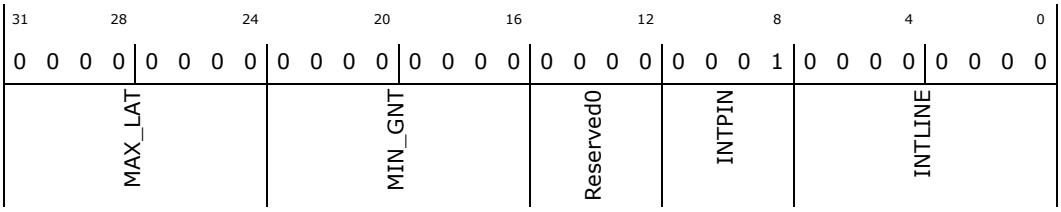
3.34.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

INTERRUPTREG: [B:0, D:24, F:2] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

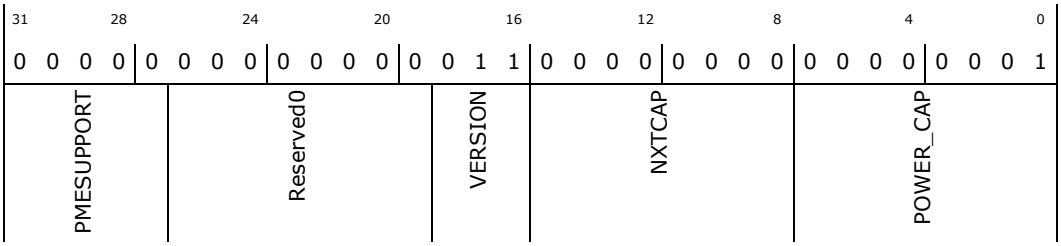
3.34.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

POWERCAPID: [B:0, D:24, F:2] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

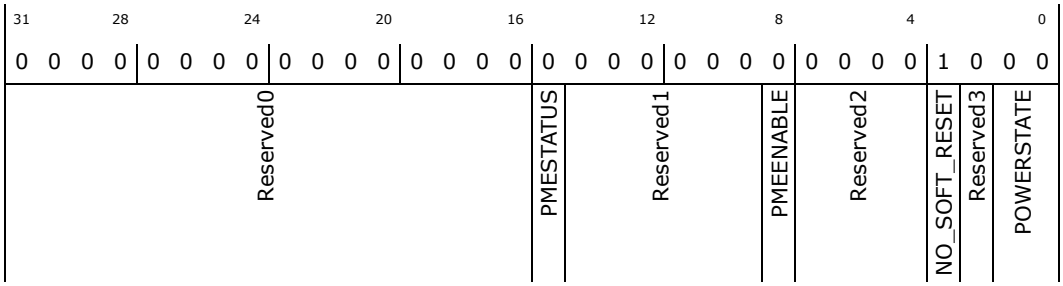
3.34.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:24, F:2] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

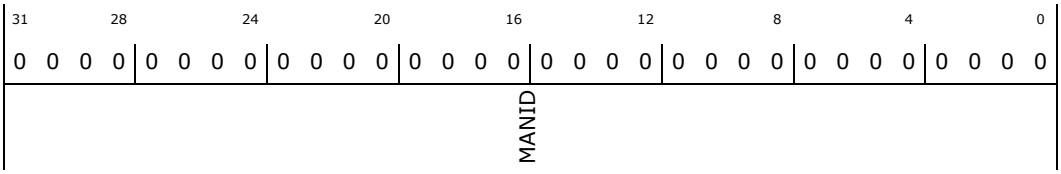
3.34.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:24, F:2] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

3.35 SIO I²C1 Memory Mapped IO Registers

Table 43. Summary of SIO I²C1 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 2598	0000007Fh
4h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 2599	00001055h
8h	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 2600	00000055h
Ch	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 2601	00000001h
10h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 2602	00000000h
14h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 2603	00000190h
18h	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 2604	000001D6h
1Ch	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 2604	0000003Ch
20h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 2605	00000082h
24h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 2606	0000000Ch
28h	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 2607	00000020h
2Ch	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 2608	00000000h
30h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 2609	000008FFh
34h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 2610	00000000h
38h	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 2612	00000010h
3Ch	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 2612	00000010h
40h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 2613	00000000h
44h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 2613	00000000h
48h	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 2614	00000000h
4Ch	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 2614	00000000h
50h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 2615	00000000h

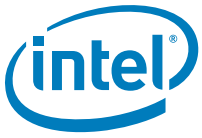


Table 43. Summary of SIO I²C1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
54h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 2616	00000000h
58h	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 2616	00000000h
5Ch	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 2617	00000000h
60h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 2617	00000000h
64h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 2618	00000000h
68h	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 2618	00000000h
6Ch	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 2619	00000000h
70h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 2620	00000006h
74h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 2621	00000000h
78h	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 2622	00000000h
7Ch	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 2622	00000001h
80h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 2623	00000000h
84h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 2625	00000000h
88h	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 2626	00000000h
8Ch	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 2627	00000000h
90h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 2627	00000000h
94h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 2628	00000064h
98h	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 2629	00000001h
9Ch	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 2630	00000000h
A0h	4	"IC_FS_SPKLEN—Offset A0h" on page 2631	00000005h
A4h	4	"IC_HS_SPKLEN—Offset A4h" on page 2631	00000002h
F4h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 2632	00FFFFEEh
F8h	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 2633	3131352Ah
FCh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 2634	44570140h
800h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 2634	00000000h

Table 43. Summary of SIO I²C1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
804h	4	"Software Reset (RESETS)—Offset 804h" on page 2635	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 2636	55000000h
818h	4	"I2C_ACK_COUNT—Offset 818h" on page 2637	00000000h
820h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 2638	00000000h
824h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 2638	00000000h

3.35.1 I2C Control Register (IC_CON)—Offset 0h

If configuration parameter I2C_DYNAMIC_TAR_UPDATE = 0, all bits are Read/Write.

If I2C_DYNAMIC_TAR_UPDATE = 1, bit 4 is Read-only.

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

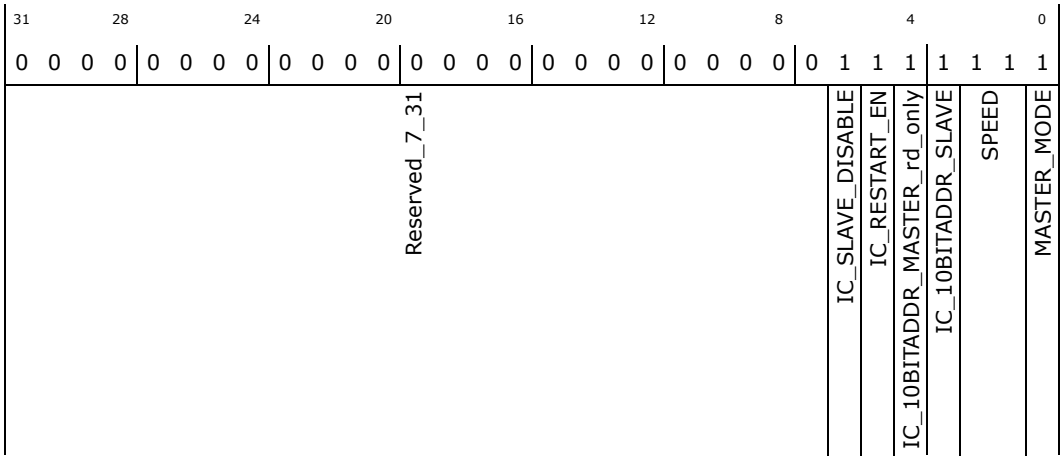
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CON: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

3.35.2 I2C Target Address Register (IC_TAR)—Offset 4h

If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to No (0), this register is 12 bits wide, and bits 15:12 are reserved. Writes to this register succeed only when IC_ENABLE is set to 0.

However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND

- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

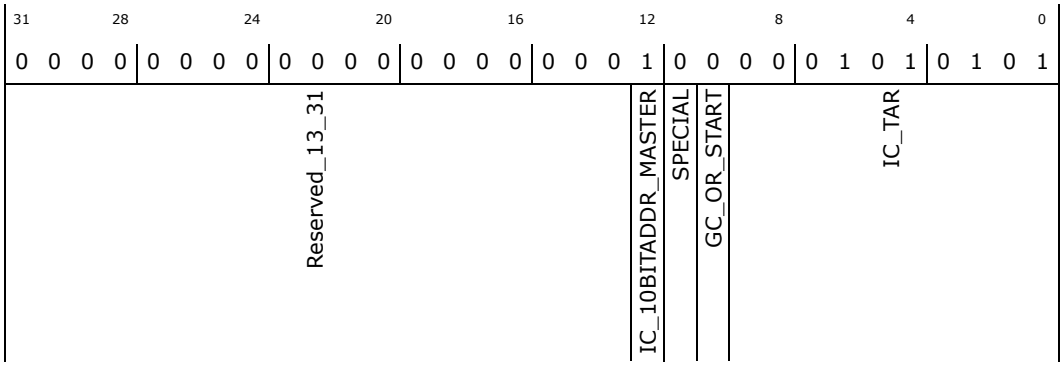
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TAR: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00001055h



Bit Range	Default & Access	Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

3.35.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

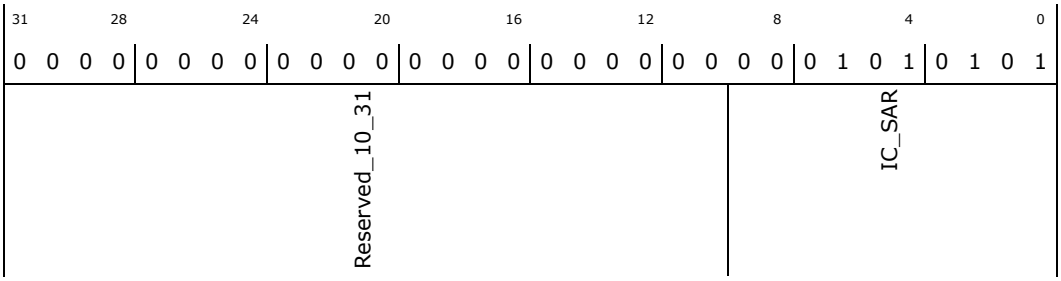
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SAR: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000055h



Bit Range	Default & Access	Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.35.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

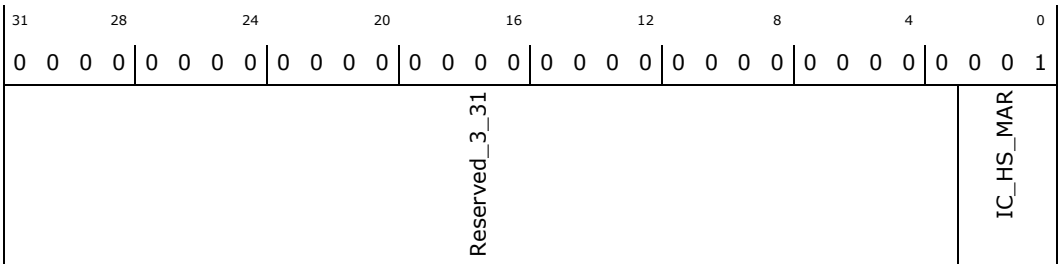
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_MADDR: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highs peed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.35.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

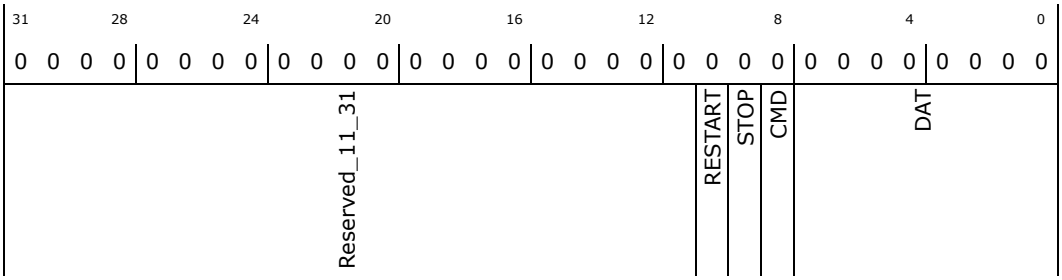
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DATA_CMD: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:11	0b RW	**Reserved_11_31:** Reserved.

Bit Range	Default & Access	Description
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/ received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

3.35.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

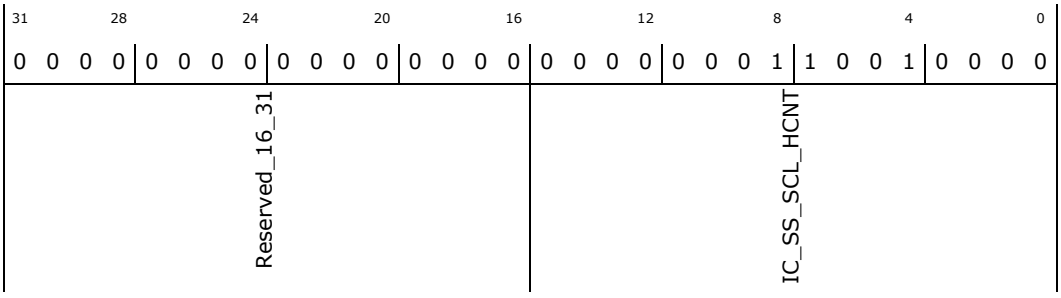
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_HCNT: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000190h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.35.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

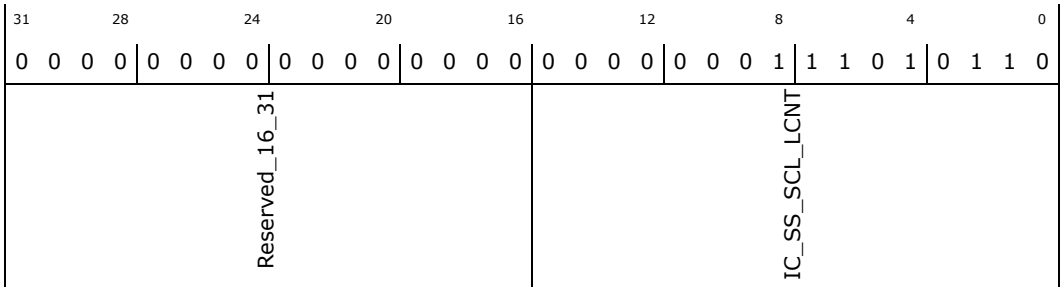
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_LCNT: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 000001D6h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.35.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

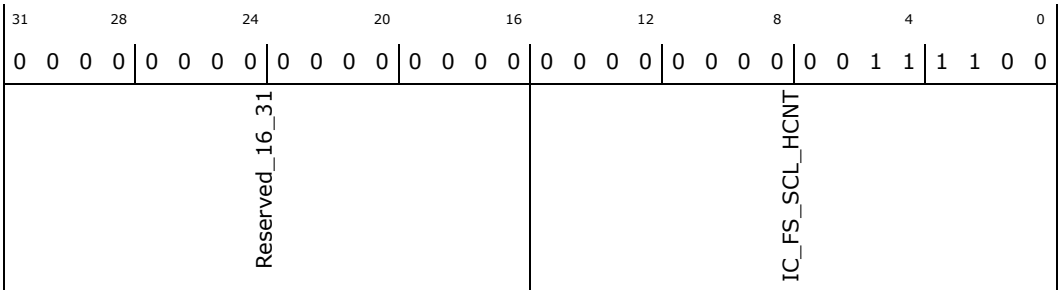
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_HCNT: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.35.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to 'IC_CLK Frequency Configuration' in the Synopsis DesignWare DW_apb_i2c Databook.

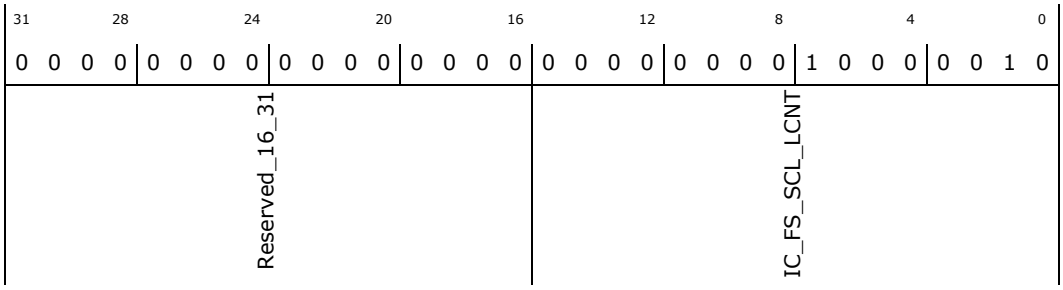
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_LCNT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000082h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.35.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* .

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

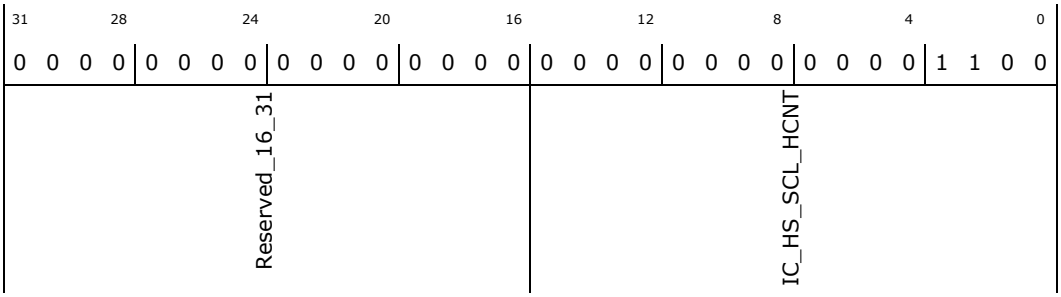
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_HCNT: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.35.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* in the Synopsis DesignWare DW_apb_i2c Databook.

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

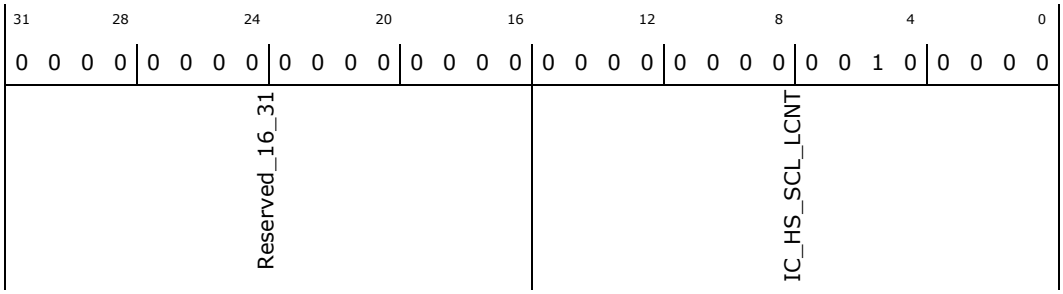
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_LCNT: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000020h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.35.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

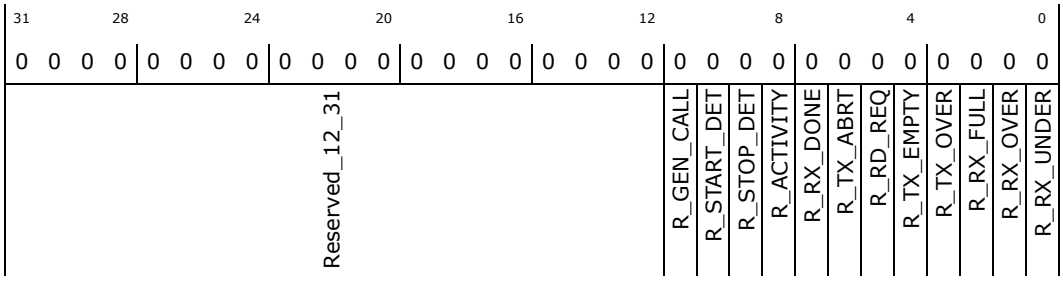
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_INTR_STAT: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.

Bit Range	Default & Access	Description
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

3.35.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

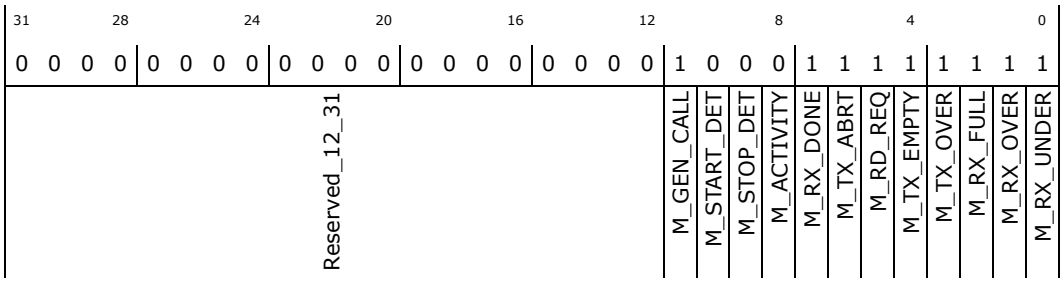
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_INTR_MASK: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 000008FFh



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

3.35.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

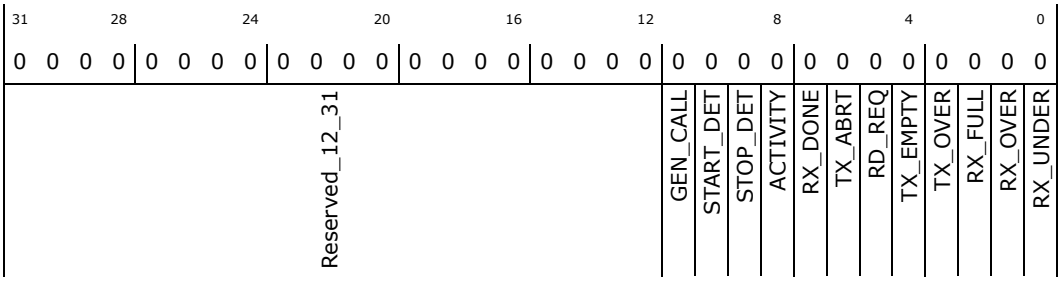
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RAW_INTR_STAT: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

3.35.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

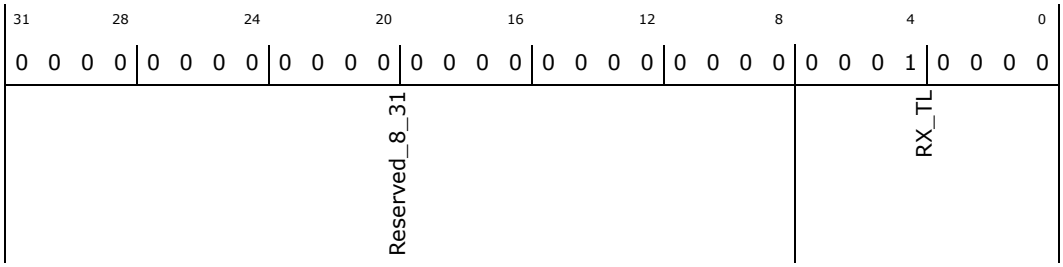
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RX_TL: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.35.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

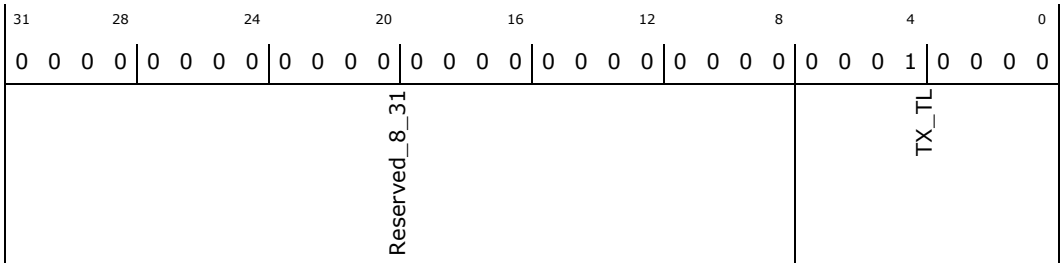
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_TL: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.35.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

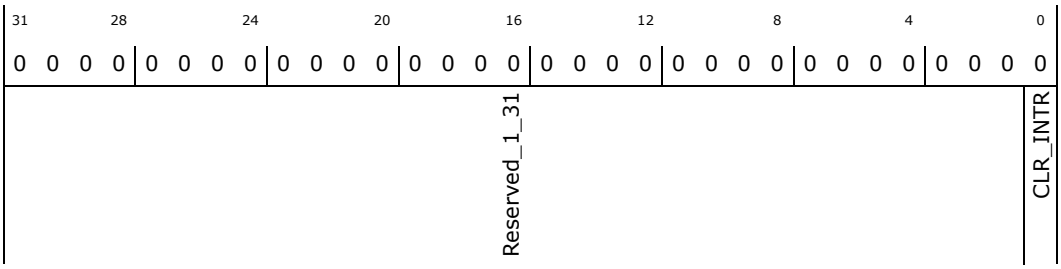
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_INTR: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

3.35.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

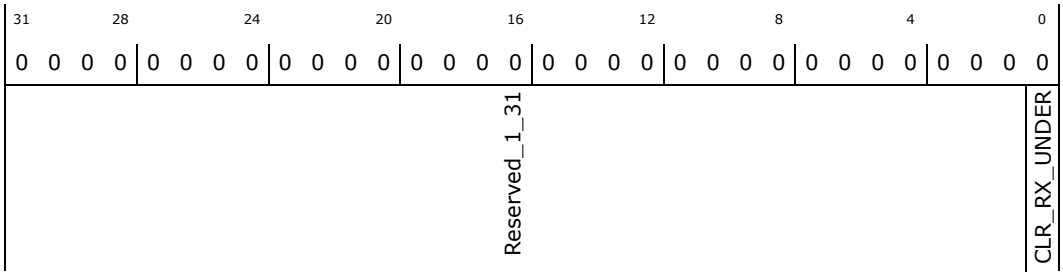
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_UNDER: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

3.35.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

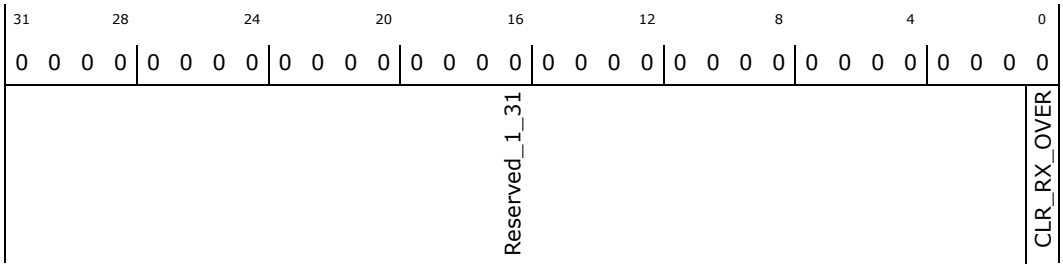
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_OVER: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

3.35.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

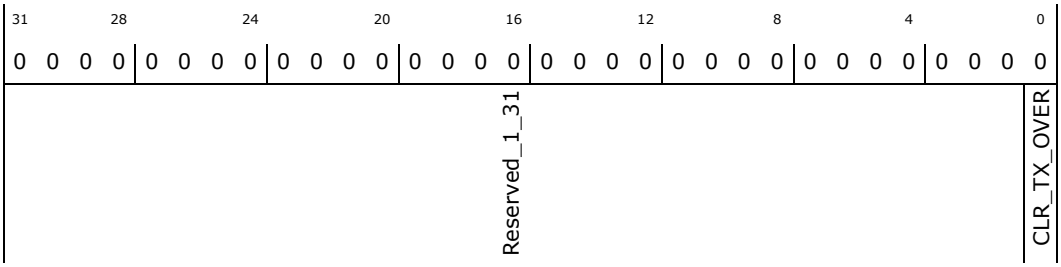
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_OVER: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

3.35.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

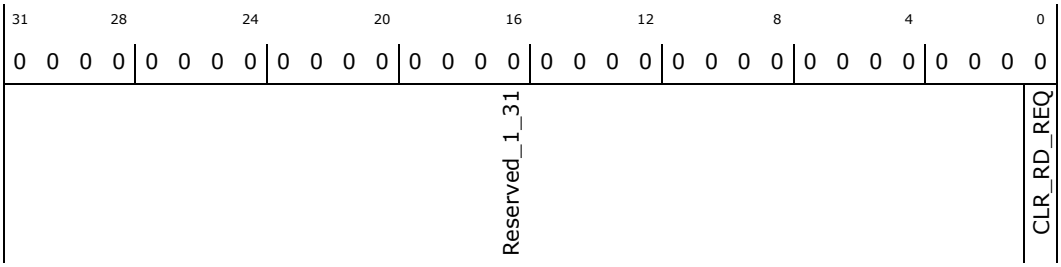
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RD_REQ: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

3.35.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

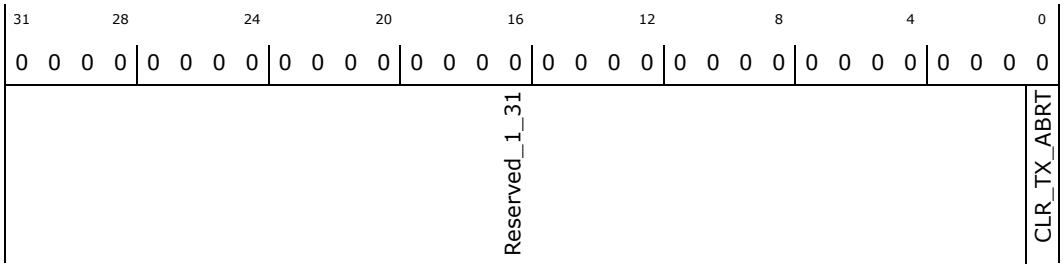
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_ABRT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

3.35.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

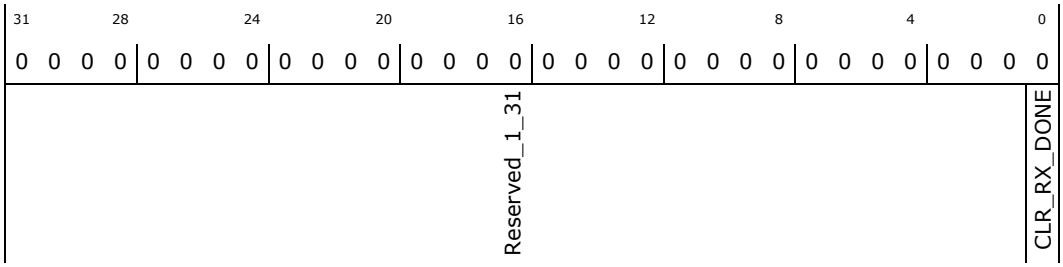
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_DONE: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

3.35.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

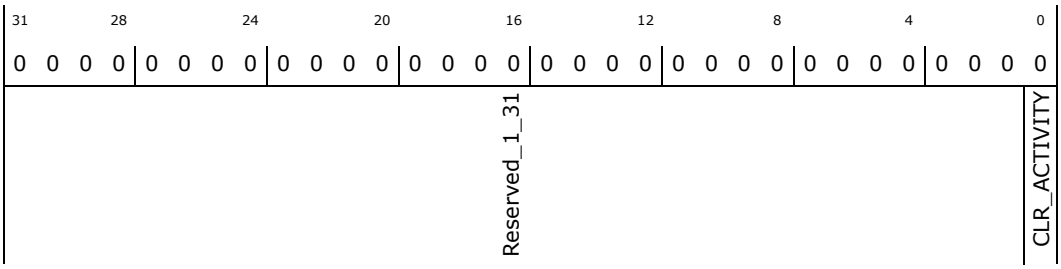
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_ACTIVITY: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

3.35.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

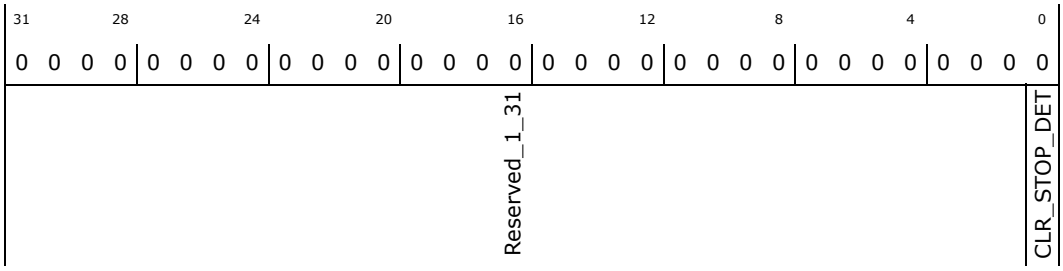
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_STOP_DET: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

3.35.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

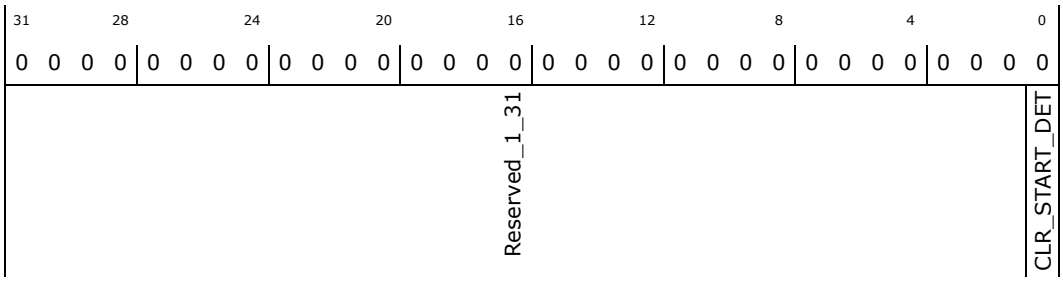
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_START_DET: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

3.35.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

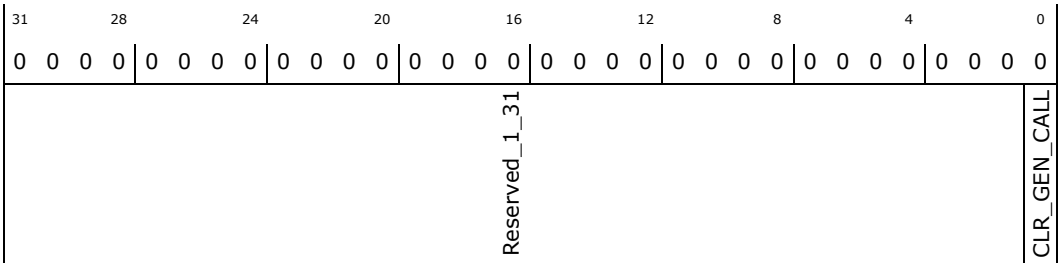
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_GEN_CALL: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

3.35.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

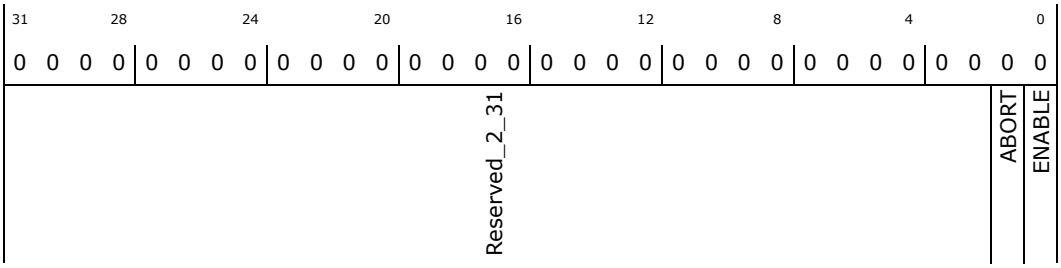
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.

Bit Range	Default & Access	Description
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

3.35.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

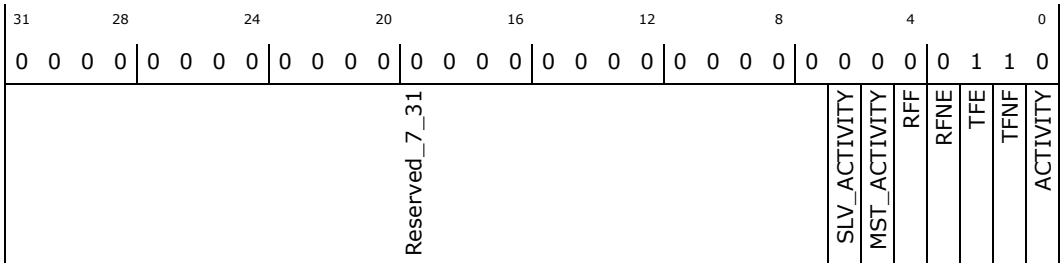
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_STATUS: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.

Bit Range	Default & Access	Description
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

3.35.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

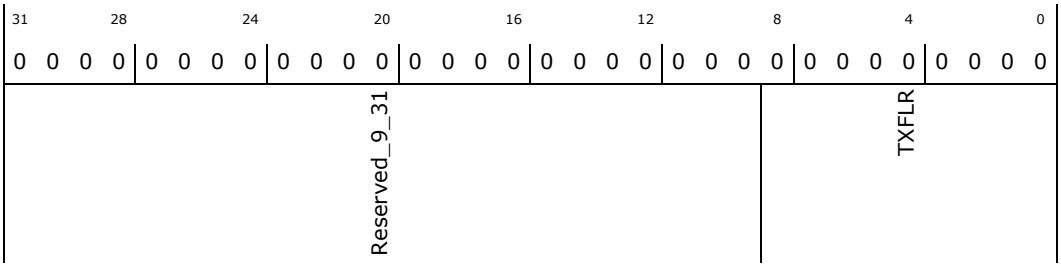
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TXFLR: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

3.35.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

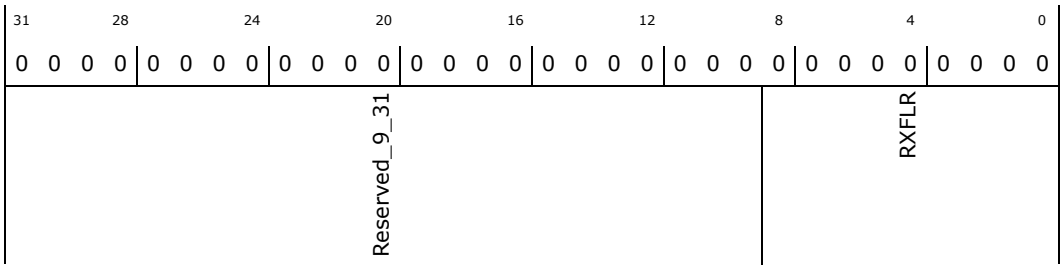
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RXFLR: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

3.35.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implemented one cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

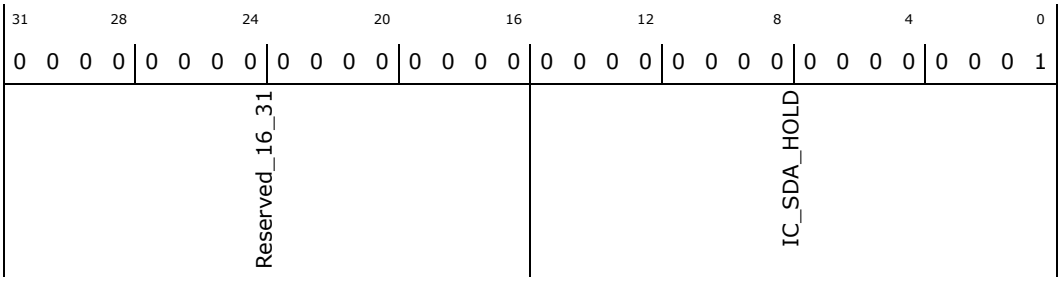
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_HOLD: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

3.35.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

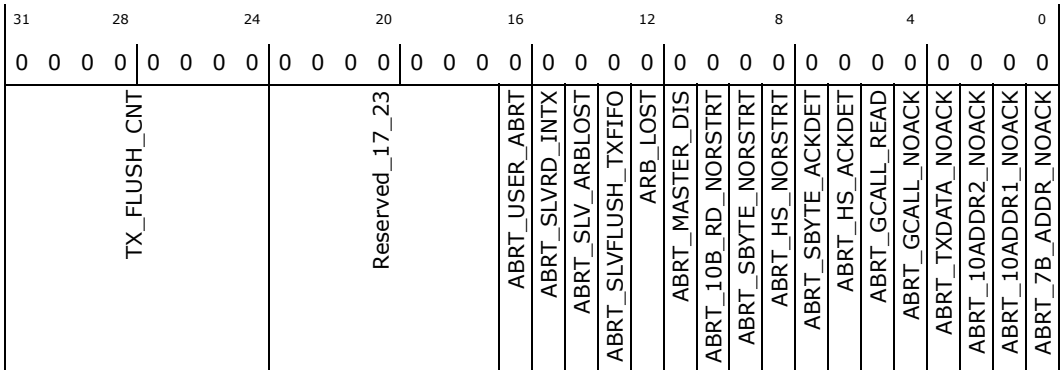
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_ABRT_SOURCE: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).

Bit Range	Default & Access	Description
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

3.35.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. This register only exists when the IC_SLV_DATA_NACK_ONLY parameter is set to 1. When this parameter disabled, this register does not exist and writing to the registers address has no effect. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

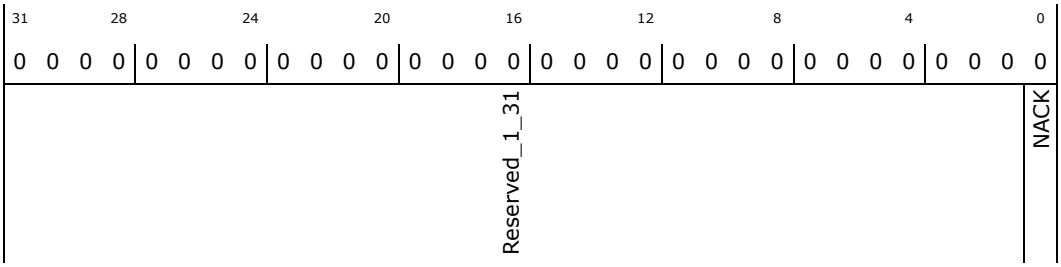
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SLV_DATA_NACK_ONLY: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slave receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

3.35.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

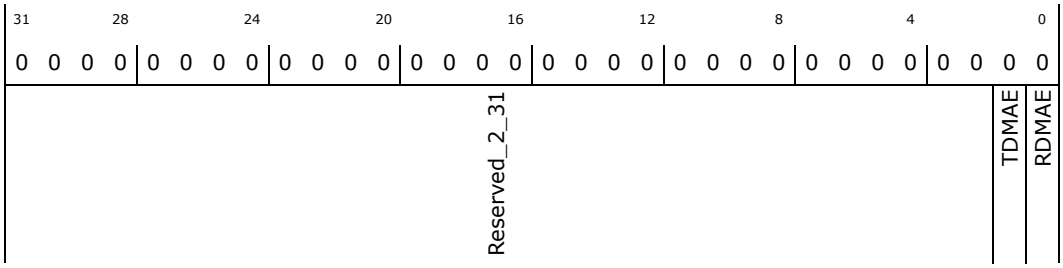
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_CR: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled

Bit Range	Default & Access	Description
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

3.35.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

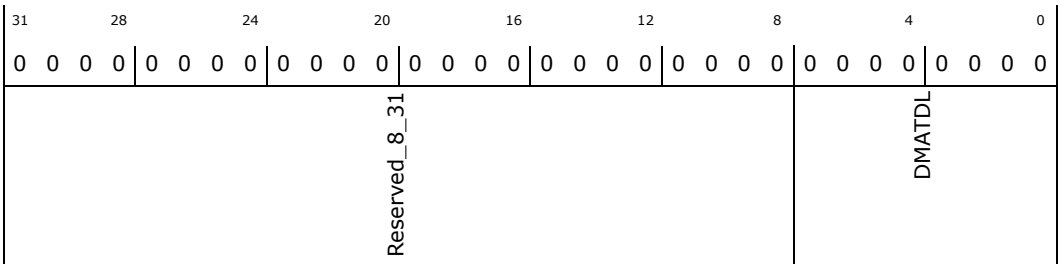
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_TDLR: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

3.35.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

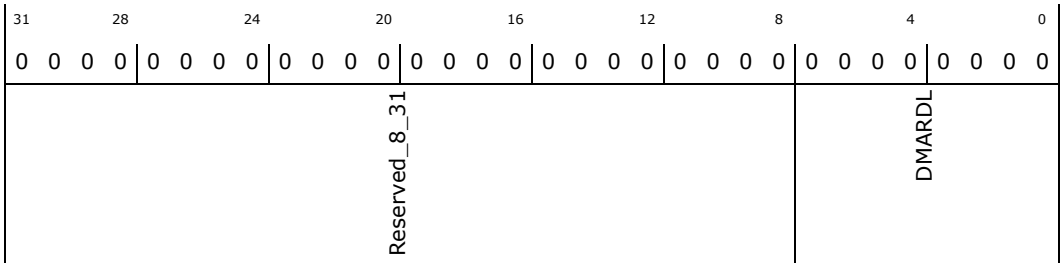
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_RDLR: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

3.35.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2.

NOTE: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

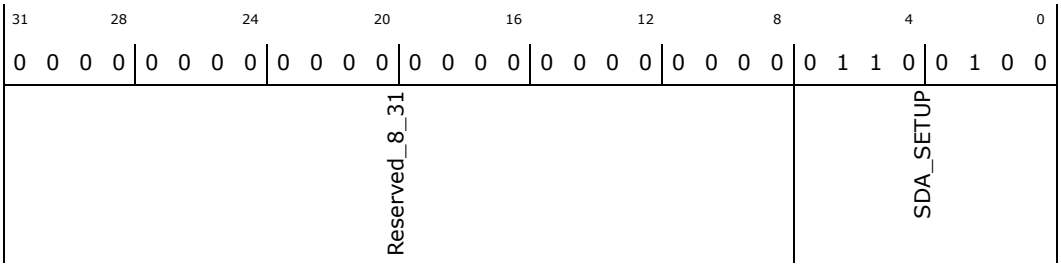
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_SETUP: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000064h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

3.35.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

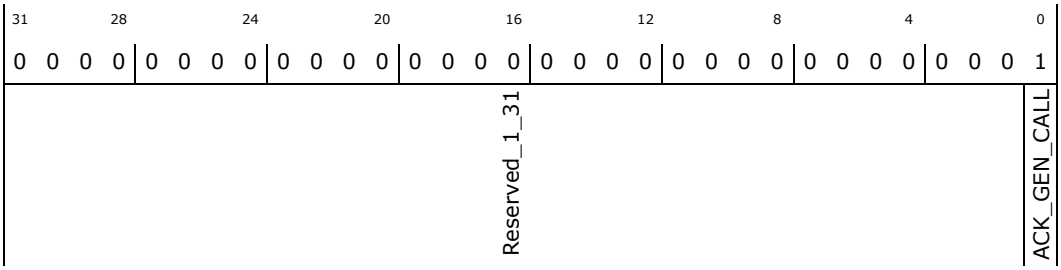
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ACK_GENERAL_CALL: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

3.35.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

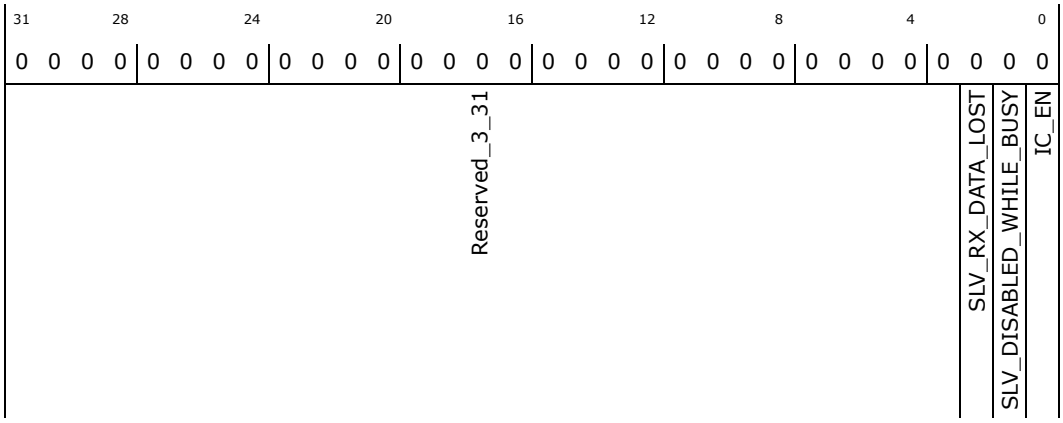
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE_STATUS: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

3.35.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

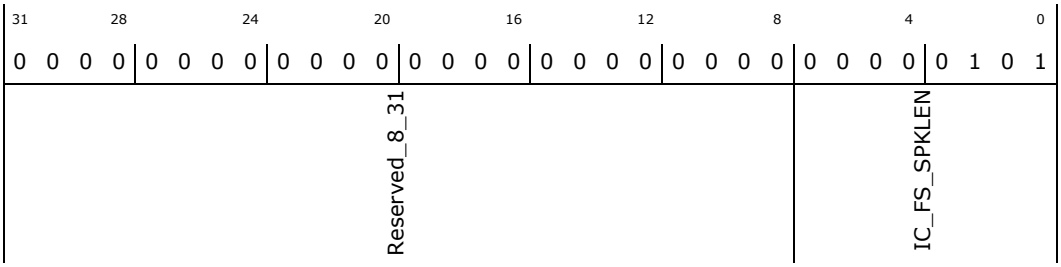
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SPKLEN: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000005h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. **Reset value:** IC_DEFAULT_FS_SPKLEN configuration parameter

3.35.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the

I2C Bus Specification. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

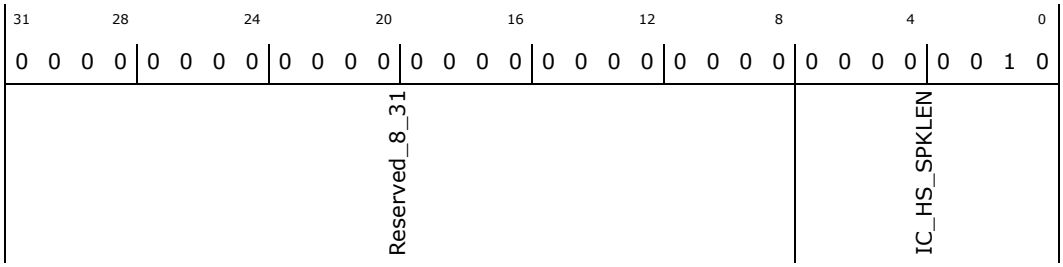
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SPKLEN: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. This register is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3. **Reset value:** IC_DEFAULT_HS_SPKLEN configuration parameter.

3.35.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

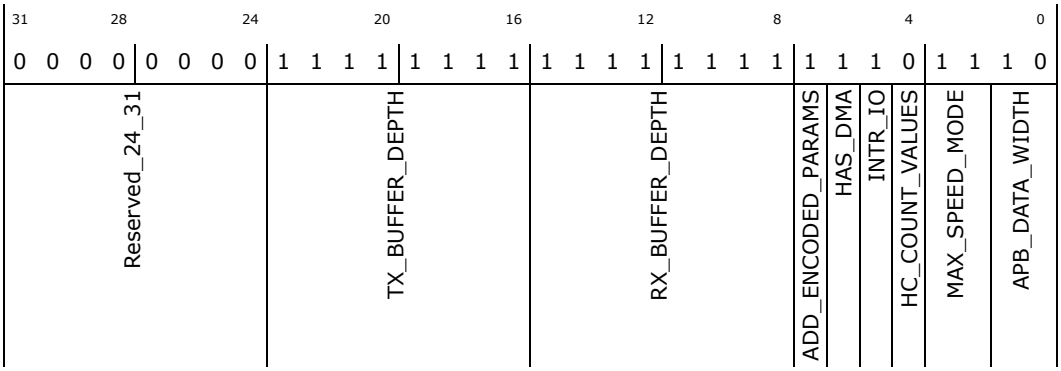
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_PARAM_1: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

3.35.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

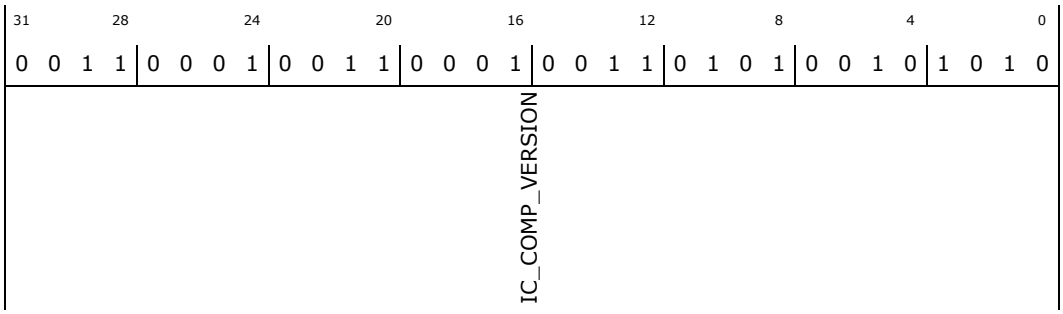
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_VERSION: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

3.35.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

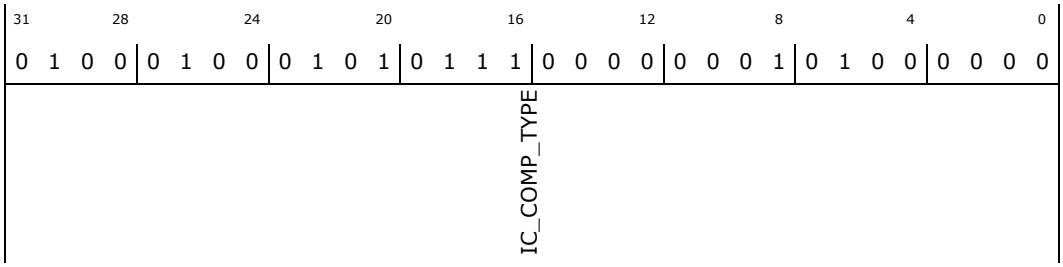
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_TYPE: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 44570140h



Bit Range	Default & Access	Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

3.35.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

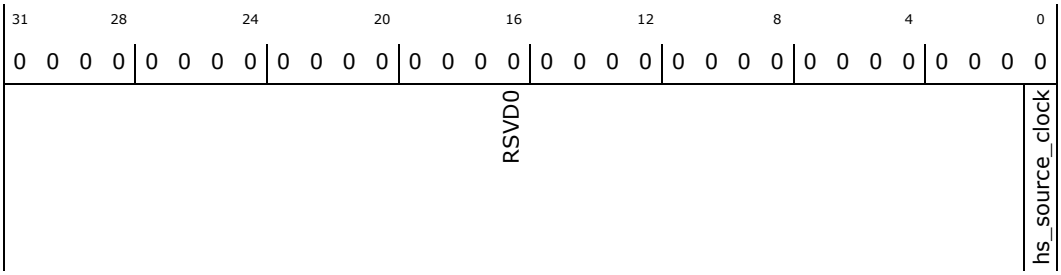
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CLOCK_PARAMS: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

3.35.47 Software Reset (RESETS)—Offset 804h

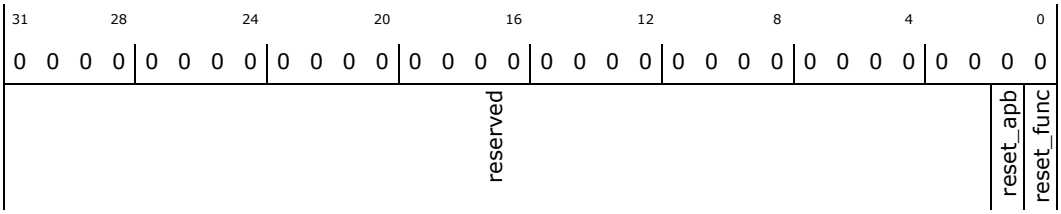
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.35.48 General Purpose Register (GENERAL)—Offset 808h

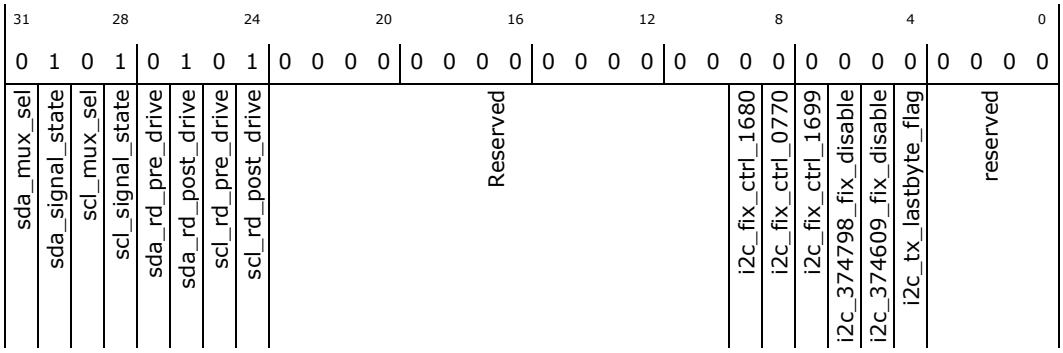
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 55000000h



Bit Range	Default & Access	Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)

Bit Range	Default & Access	Description
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

3.35.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

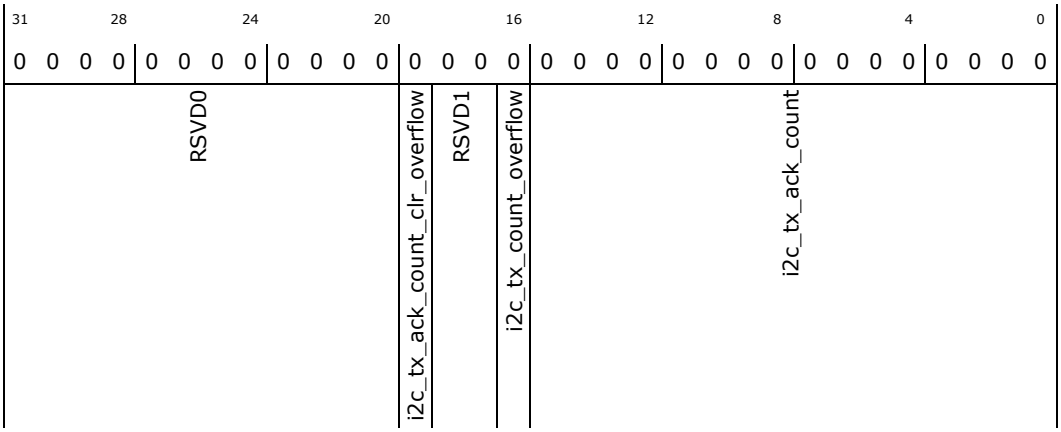
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_ACK_COUNT: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

3.35.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

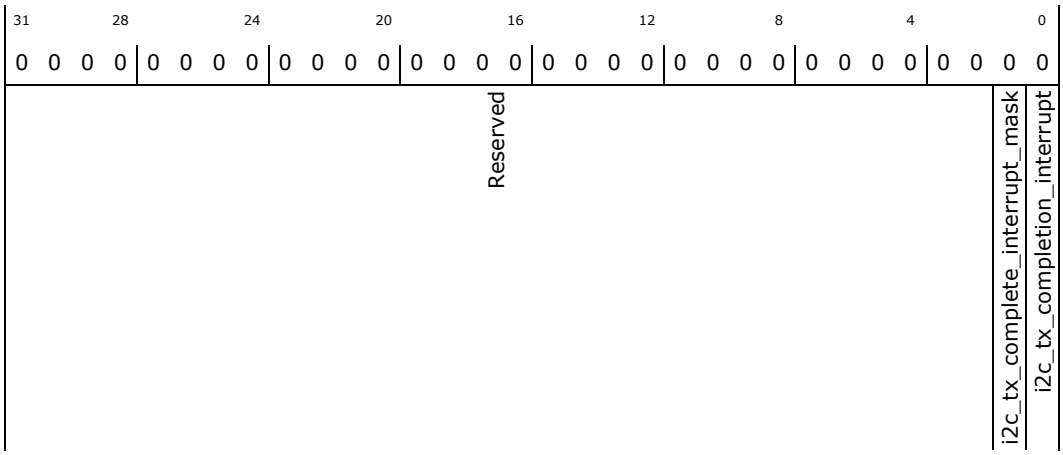
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_TX_COMPLETE_INTR_STAT: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

3.35.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

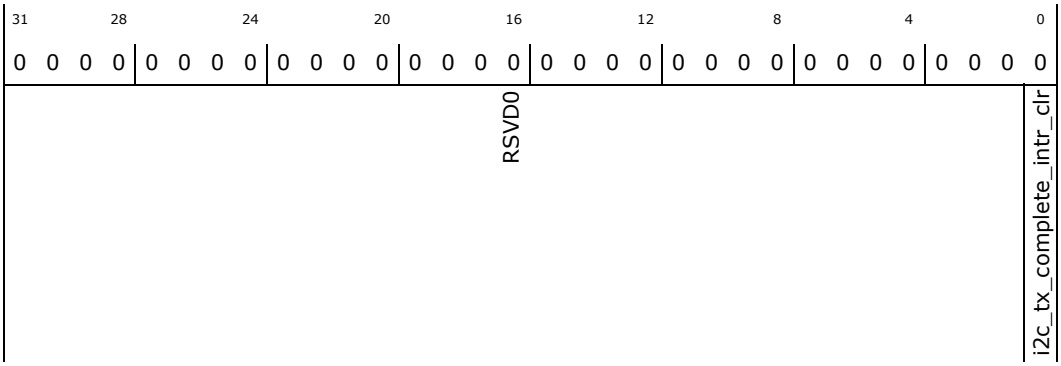
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

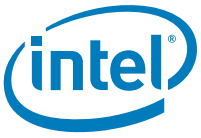
I2C_TX_COMPLETE_INTR_CLR: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt



3.36 SIO I2C2 PCI Configuration Registers

Table 44. Summary of SIO I2C2 PCI Configuration Registers—0/24/3

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2640	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2641	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2642	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2643	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2644	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2644	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2645	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2646	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2646	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2647	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2647	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2648	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2649	00000000h

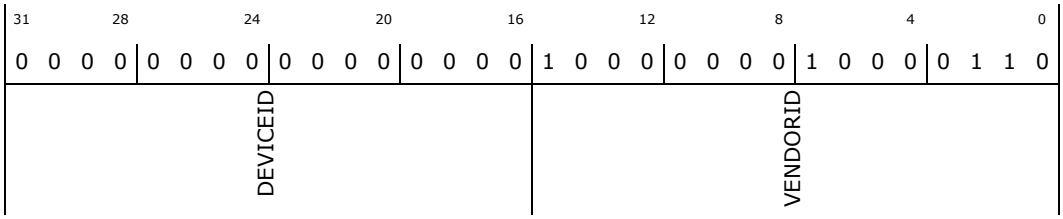
3.36.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:24, F:3] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

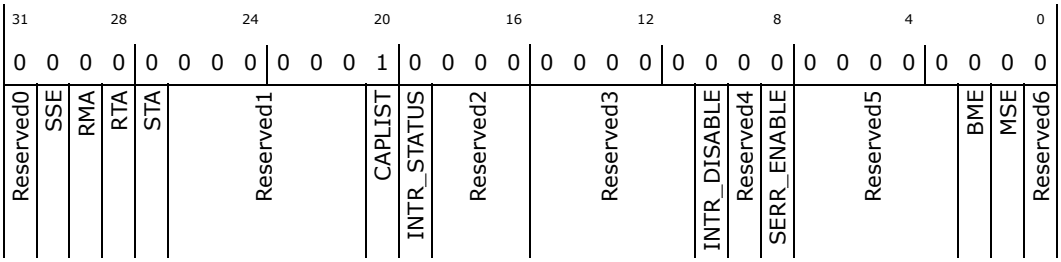
3.36.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:24, F:3] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

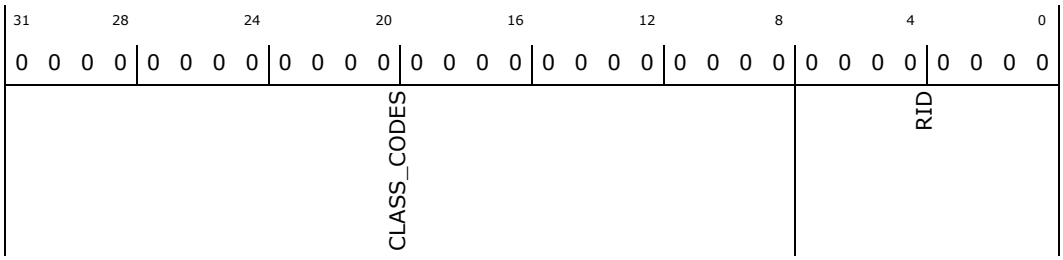
3.36.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:24, F:3] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

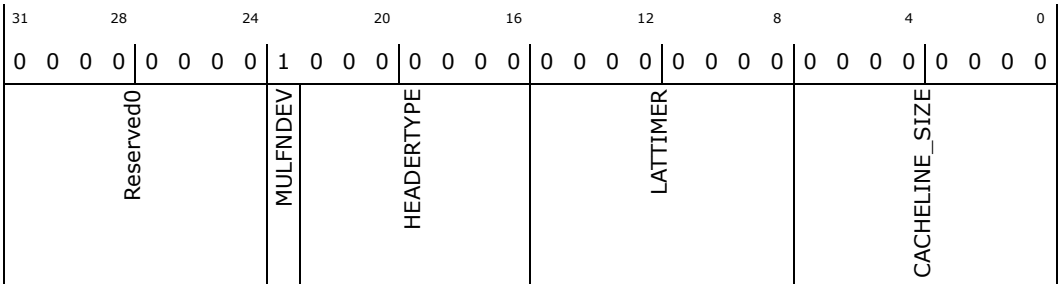
3.36.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:24, F:3] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

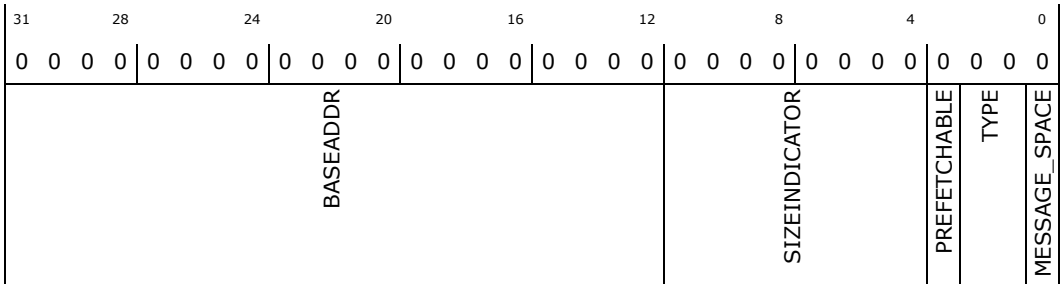
3.36.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

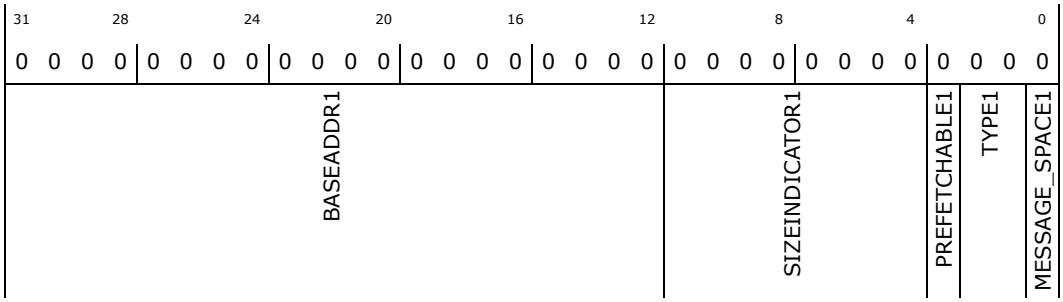
3.36.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:24, F:3] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

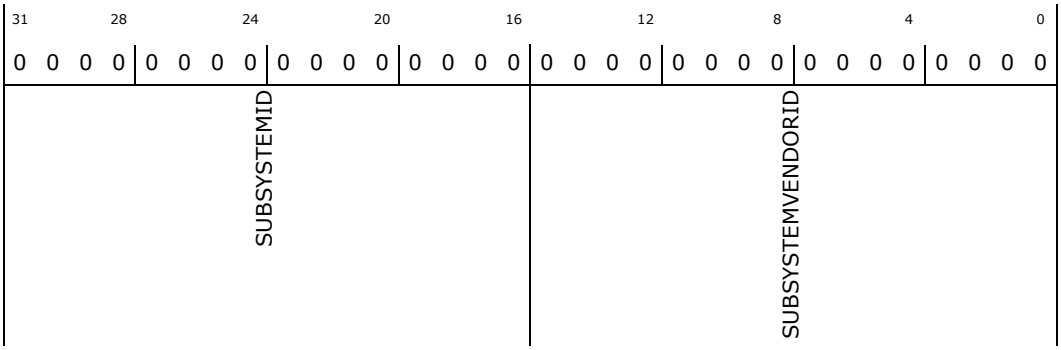
3.36.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:24, F:3] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

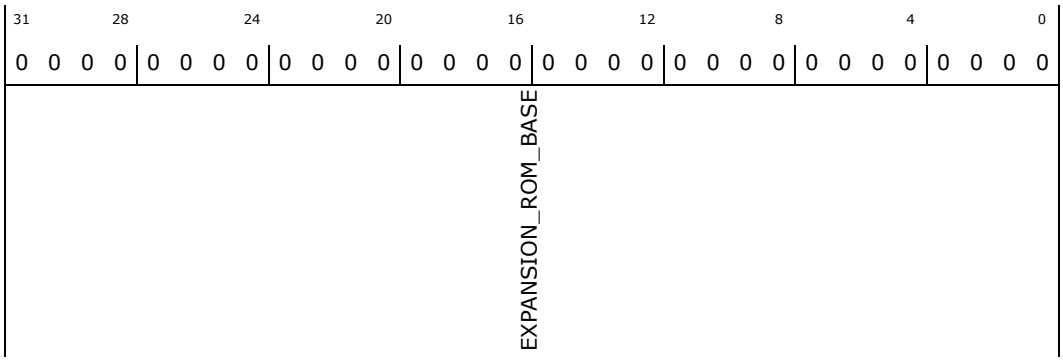
3.36.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:24, F:3] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

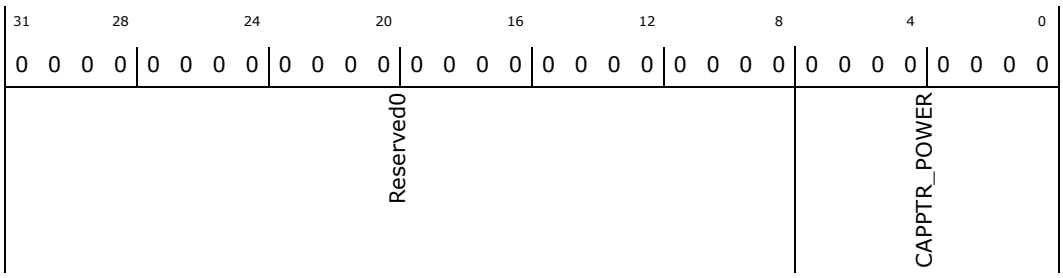
3.36.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:24, F:3] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

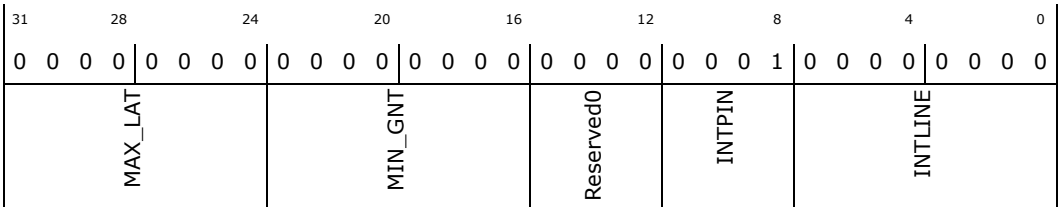
3.36.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

INTERRUPTREG: [B:0, D:24, F:3] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

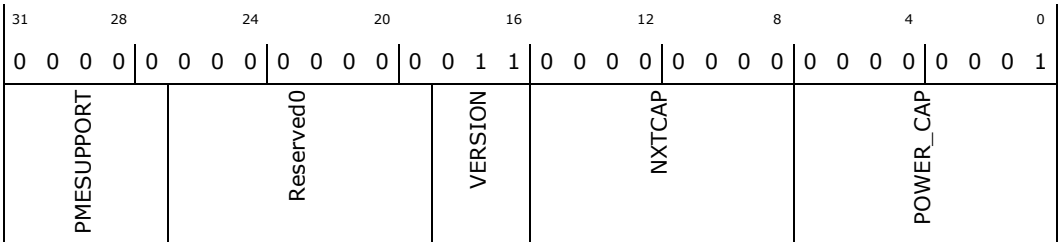
3.36.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

POWERCAPID: [B:0, D:24, F:3] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

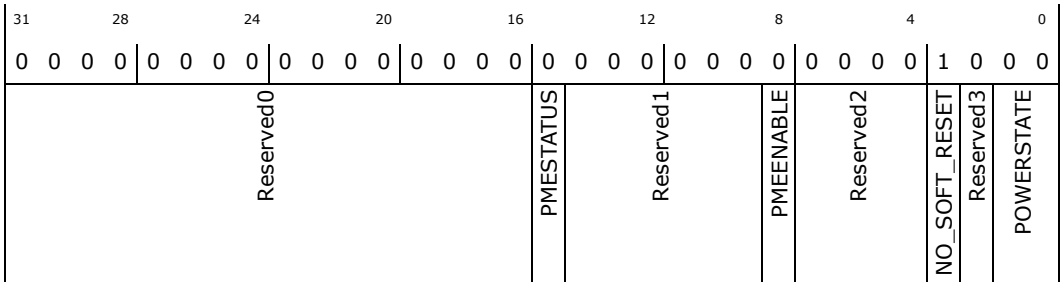
3.36.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:24, F:3] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

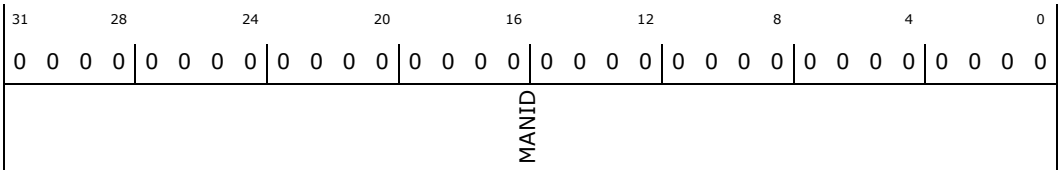
3.36.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:24, F:3] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

3.37 SIO I2C2 Memory Mapped IO Registers

Table 45. Summary of SIO I2C2 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 2652	0000007Fh
4h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 2653	00001055h
8h	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 2654	00000055h
Ch	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 2655	00000001h
10h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 2656	00000000h
14h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 2657	00000190h
18h	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 2658	000001D6h
1Ch	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 2658	0000003Ch
20h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 2659	00000082h
24h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 2660	0000000Ch
28h	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 2661	00000020h
2Ch	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 2662	00000000h
30h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 2663	000008FFh
34h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 2664	00000000h
38h	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 2666	00000010h
3Ch	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 2666	00000010h
40h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 2667	00000000h
44h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 2667	00000000h
48h	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 2668	00000000h
4Ch	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 2668	00000000h
50h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 2669	00000000h

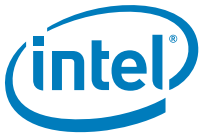


Table 45. Summary of SIO I²C2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
54h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 2670	00000000h
58h	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 2670	00000000h
5Ch	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 2671	00000000h
60h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 2671	00000000h
64h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 2672	00000000h
68h	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 2672	00000000h
6Ch	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 2673	00000000h
70h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 2674	00000006h
74h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 2675	00000000h
78h	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 2676	00000000h
7Ch	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 2676	00000001h
80h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 2677	00000000h
84h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 2679	00000000h
88h	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 2680	00000000h
8Ch	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 2681	00000000h
90h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 2681	00000000h
94h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 2682	00000064h
98h	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 2683	00000001h
9Ch	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 2684	00000000h
A0h	4	"IC_FS_SPKLEN—Offset A0h" on page 2685	00000005h
A4h	4	"IC_HS_SPKLEN—Offset A4h" on page 2685	00000002h
F4h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 2686	00FFFFEEh
F8h	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 2687	3131352Ah
FCh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 2688	44570140h
800h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 2688	00000000h

Table 45. Summary of SIO I²C2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
804h	4	"Software Reset (RESETS)—Offset 804h" on page 2689	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 2690	55000000h
818h	4	"I2C_ACK_COUNT—Offset 818h" on page 2691	00000000h
820h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 2692	00000000h
824h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 2692	00000000h

3.37.1 I2C Control Register (IC_CON)—Offset 0h

If configuration parameter I2C_DYNAMIC_TAR_UPDATE = 0, all bits are Read/Write.

If I2C_DYNAMIC_TAR_UPDATE = 1, bit 4 is Read-only.

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

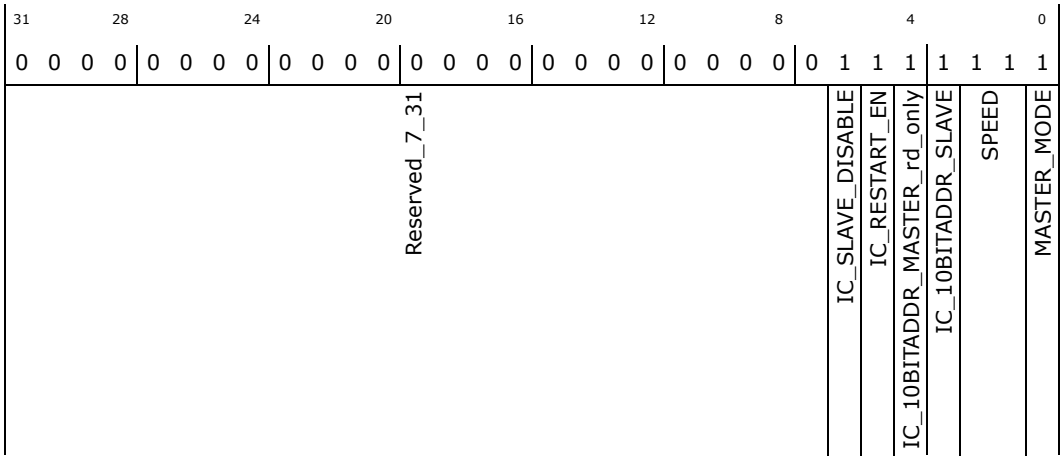
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CON: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

3.37.2 I2C Target Address Register (IC_TAR)—Offset 4h

If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to No (0), this register is 12 bits wide, and bits 15:12 are reserved. Writes to this register succeed only when IC_ENABLE is set to 0.

However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND

- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

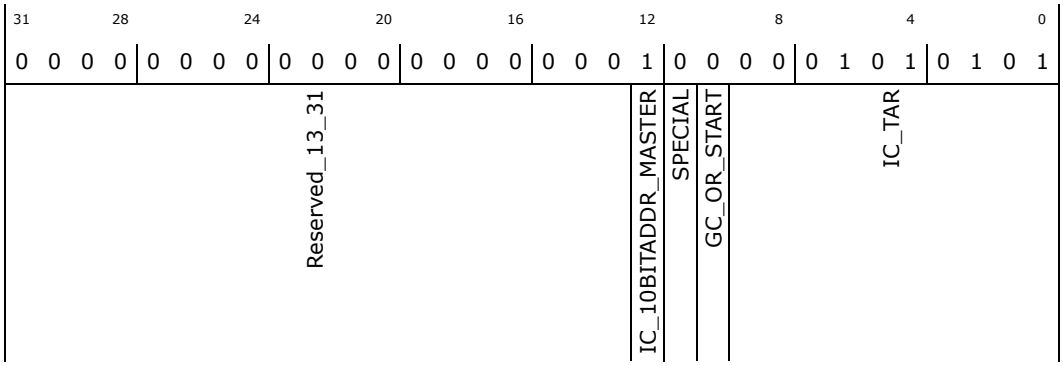
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TAR: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00001055h



Bit Range	Default & Access	Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

3.37.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

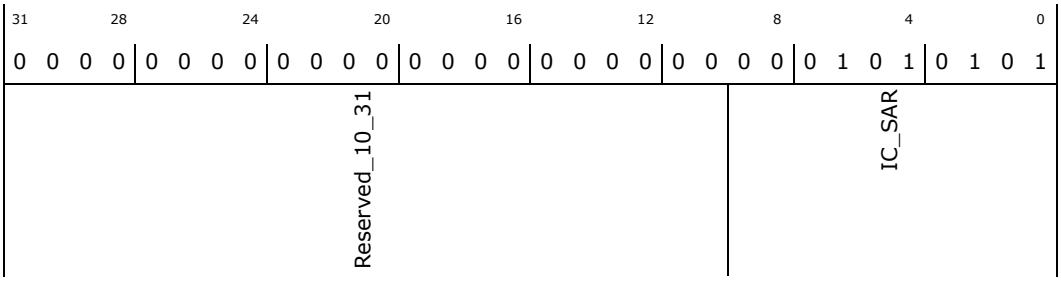
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SAR: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000055h



Bit Range	Default & Access	Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.37.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

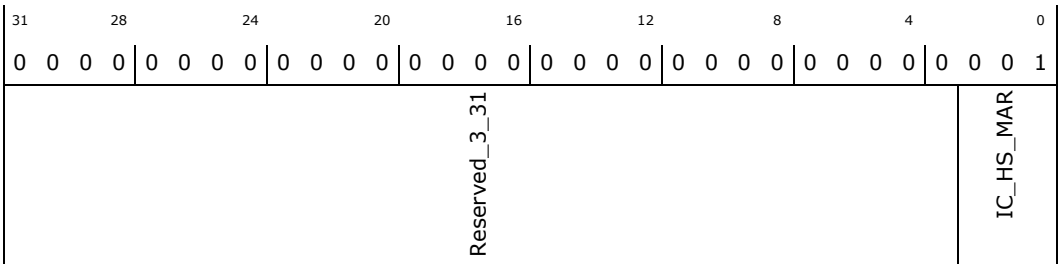
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_MADDR: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highs peed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.37.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

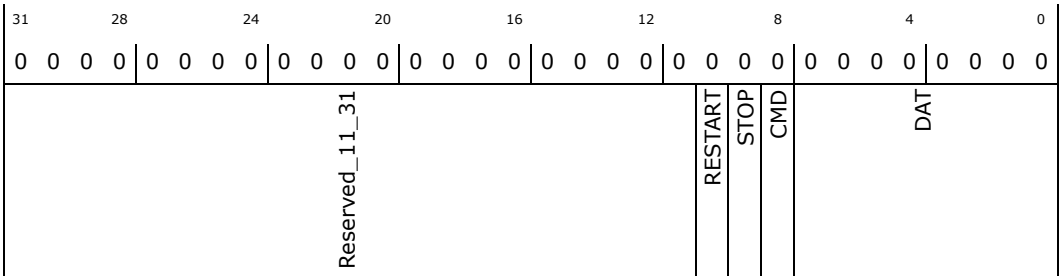
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DATA_CMD: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:11	0b RW	**Reserved_11_31:** Reserved.

Bit Range	Default & Access	Description
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/ received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

3.37.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

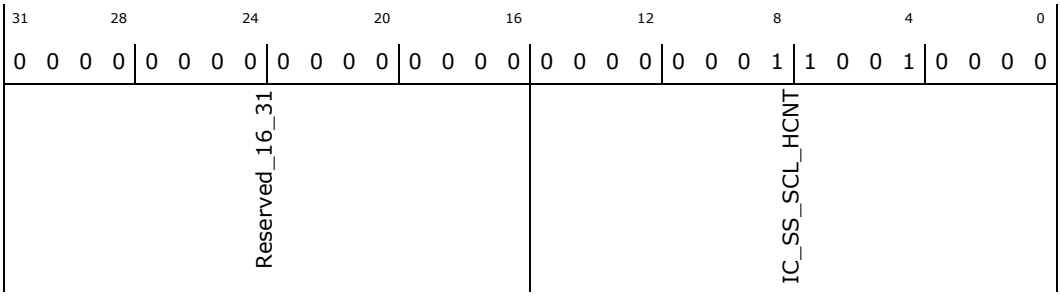
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_HCNT: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000190h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.37.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

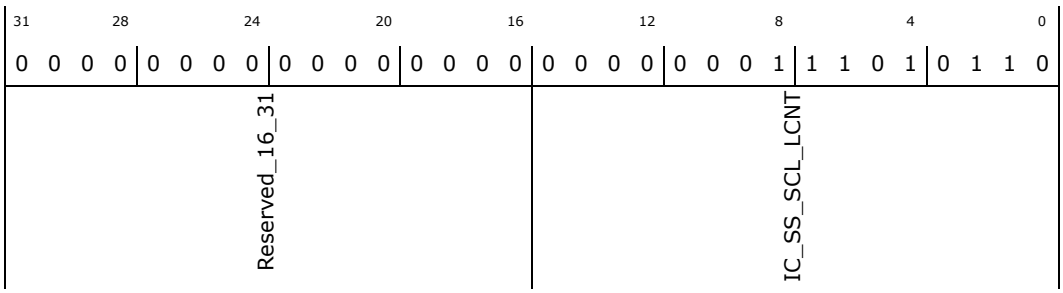
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_LCNT: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 000001D6h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.37.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

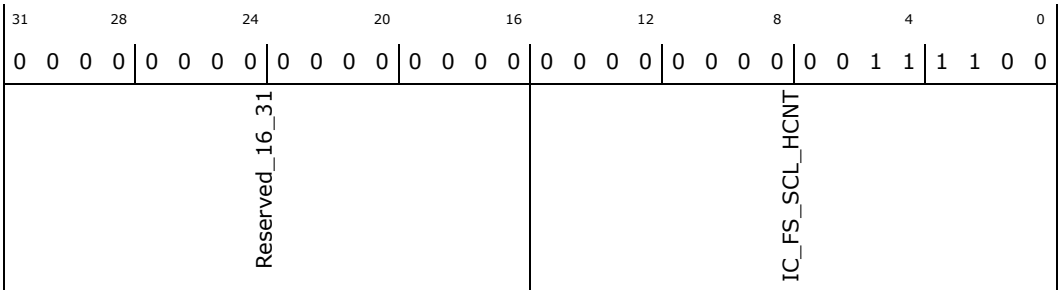
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_HCNT: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.37.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to 'IC_CLK Frequency Configuration' in the Synopsis DesignWare DW_apb_i2c Databook.

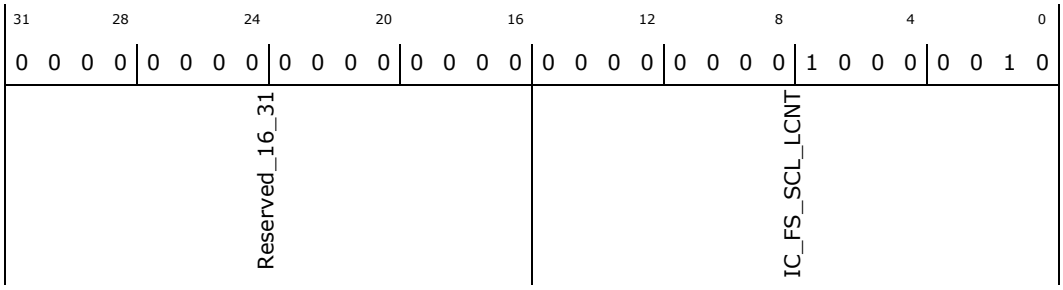
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_LCNT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000082h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.37.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* .

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

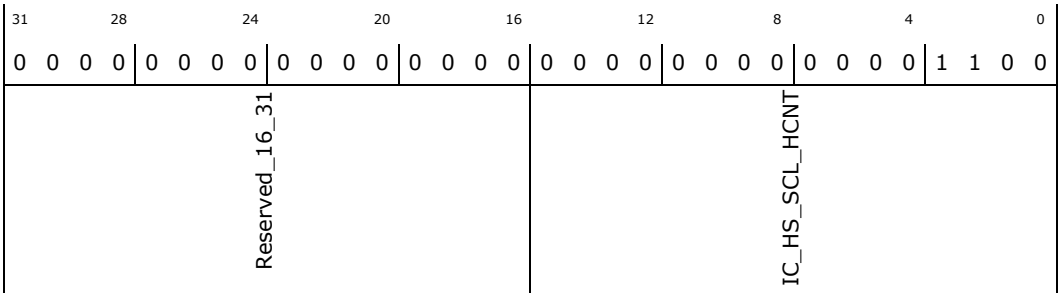
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_HCNT: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.37.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* in the Synopsis DesignWare DW_apb_i2c Databook.

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

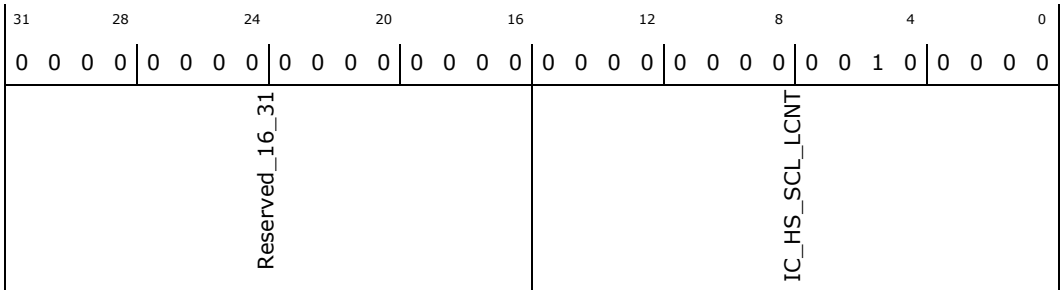
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_LCNT: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000020h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.37.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

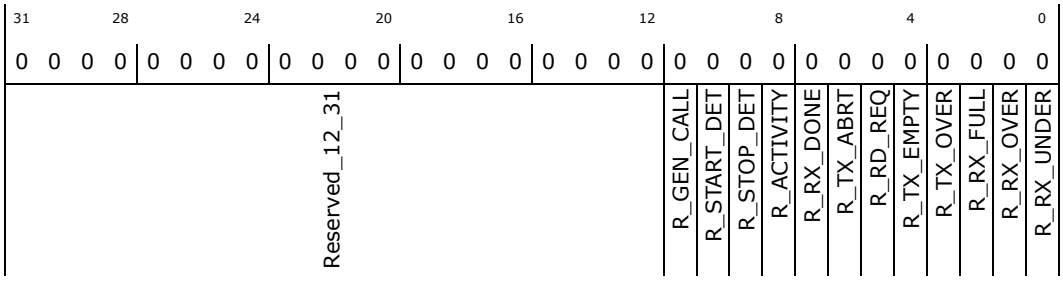
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_INTR_STAT: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.

Bit Range	Default & Access	Description
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

3.37.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

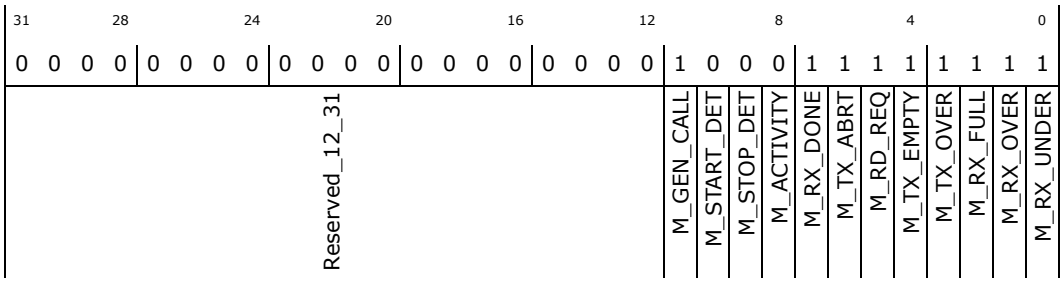
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_INTR_MASK: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 000008FFh



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

3.37.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

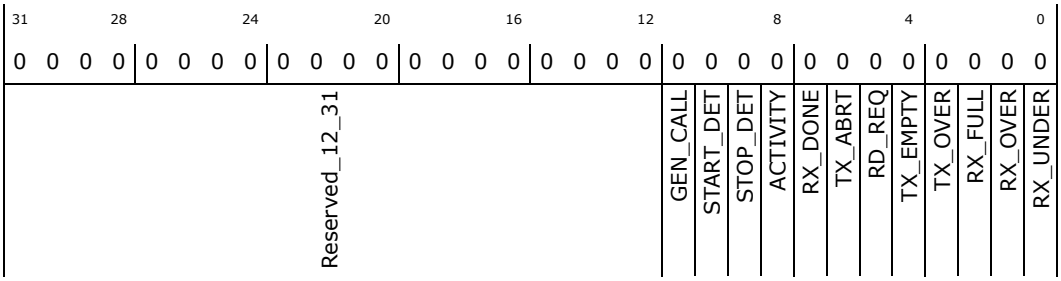
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RAW_INTR_STAT: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

3.37.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

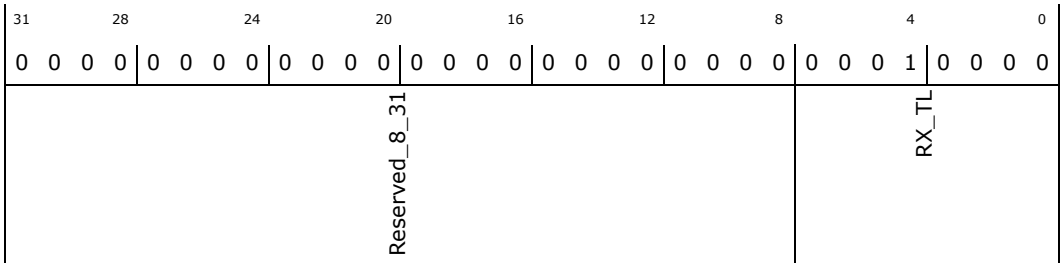
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RX_TL: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.37.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

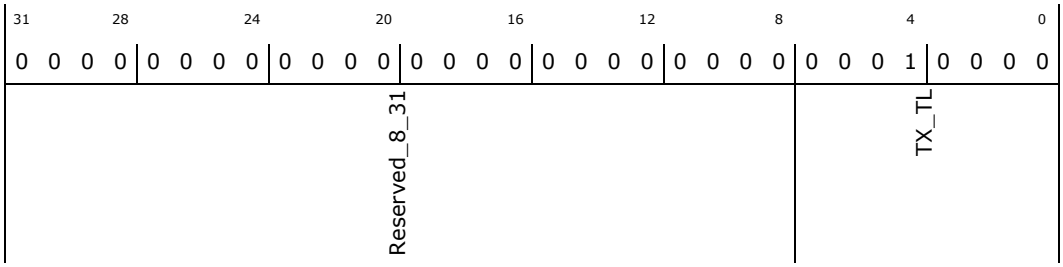
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_TL: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.37.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

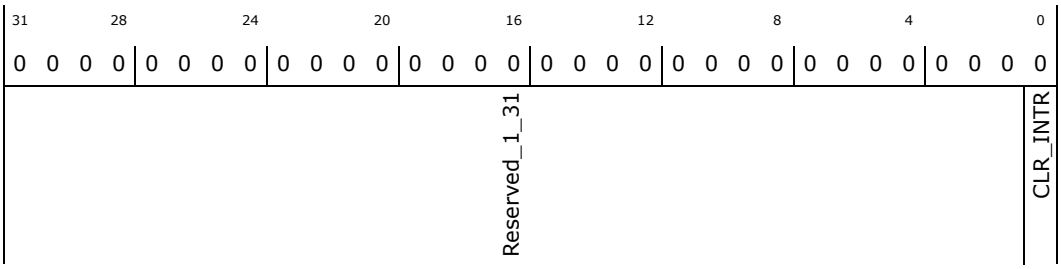
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_INTR: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

3.37.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

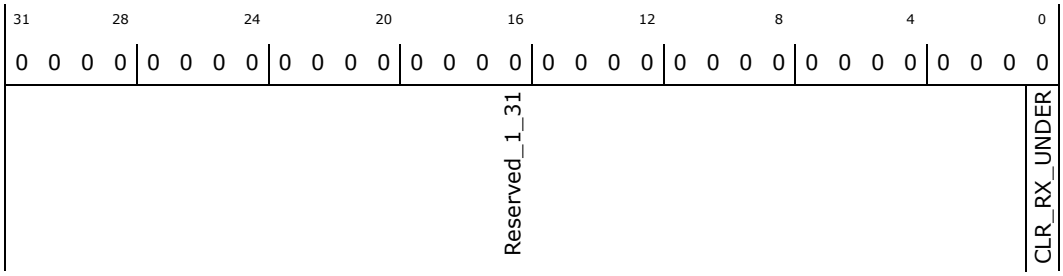
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_UNDER: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

3.37.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

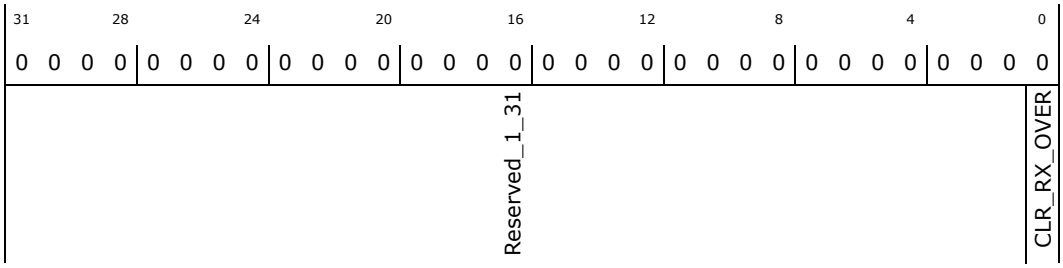
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_OVER: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

3.37.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

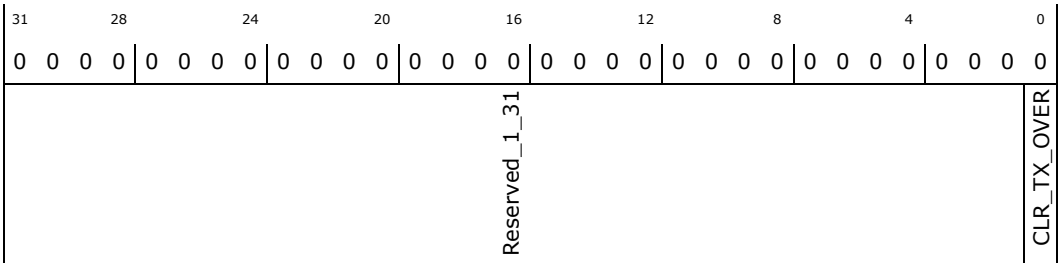
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_OVER: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

3.37.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

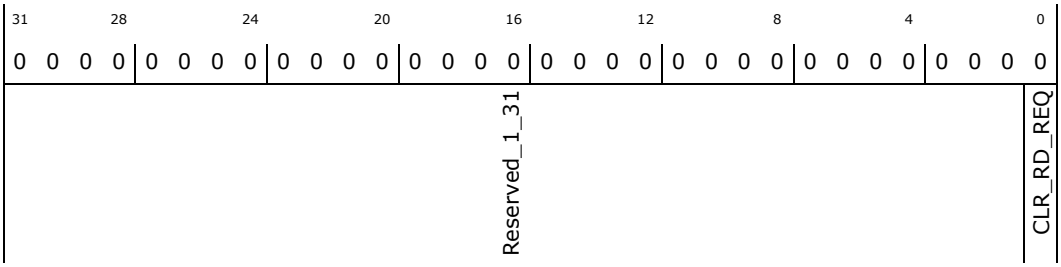
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RD_REQ: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

3.37.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

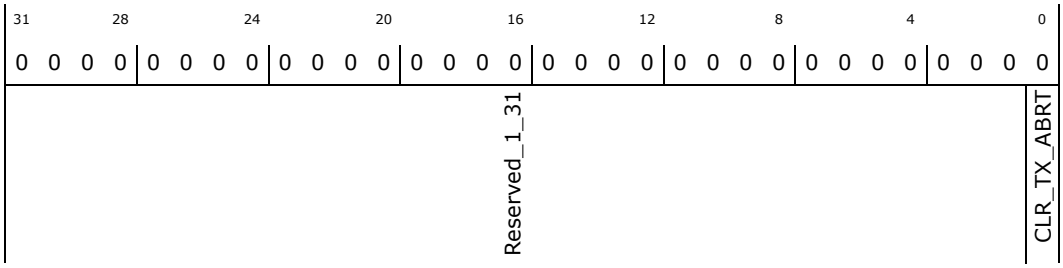
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_ABRT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

3.37.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

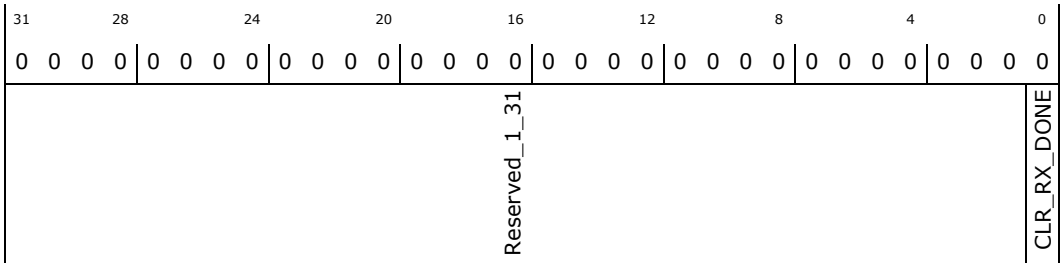
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_DONE: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

3.37.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

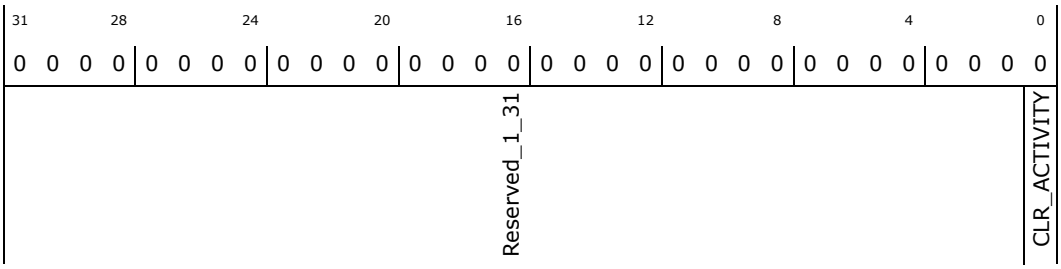
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_ACTIVITY: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

3.37.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

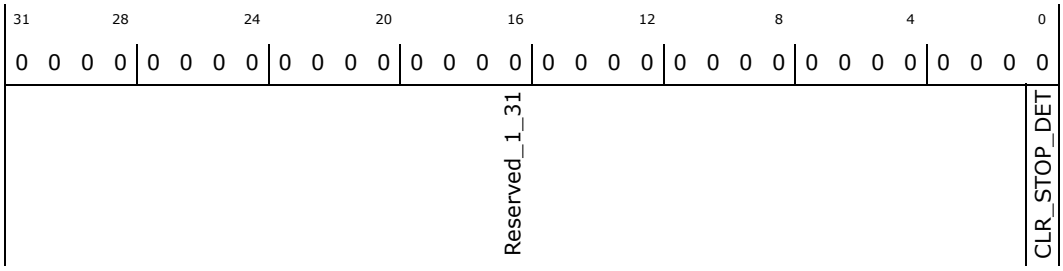
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_STOP_DET: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

3.37.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

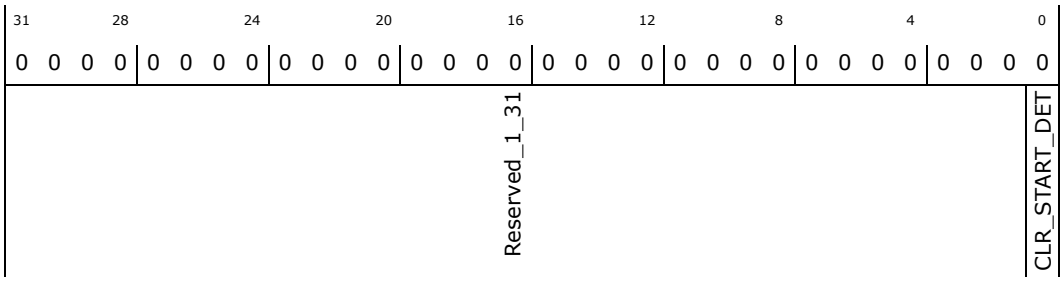
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_START_DET: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

3.37.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

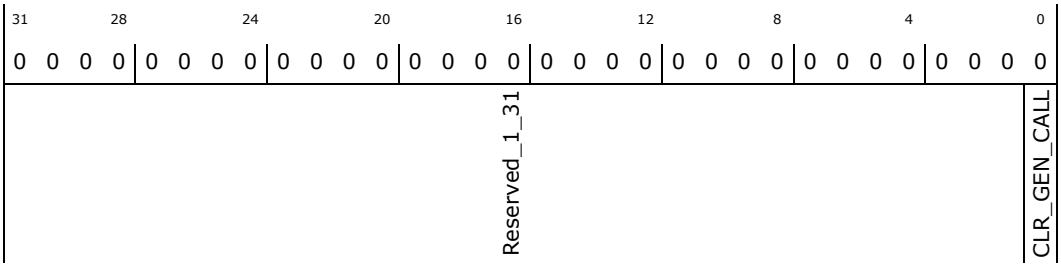
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_GEN_CALL: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

3.37.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

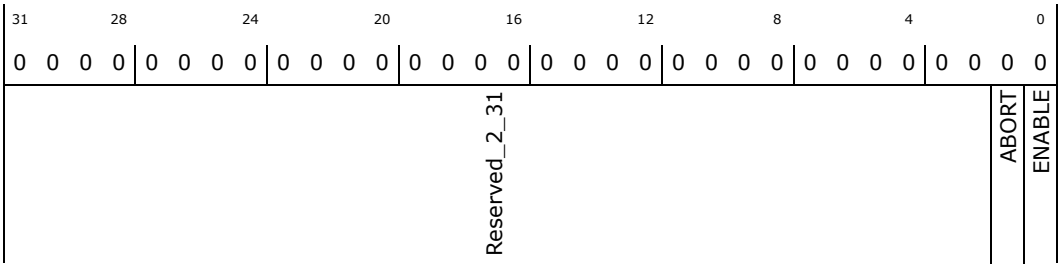
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.

Bit Range	Default & Access	Description
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

3.37.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

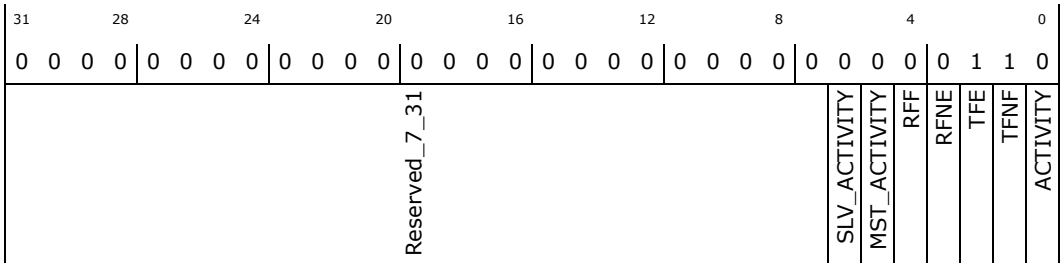
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_STATUS: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.

Bit Range	Default & Access	Description
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

3.37.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

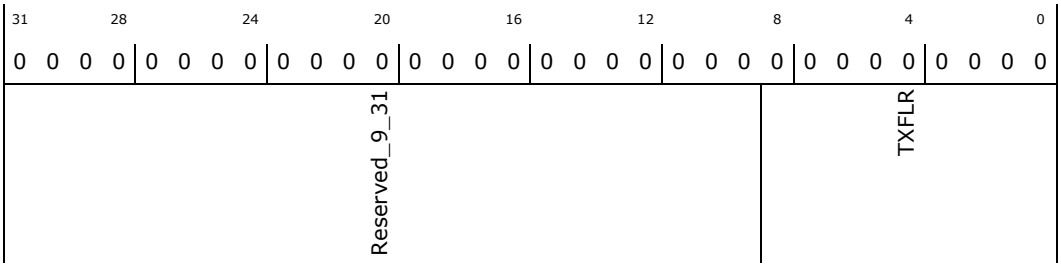
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TXFLR: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

3.37.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

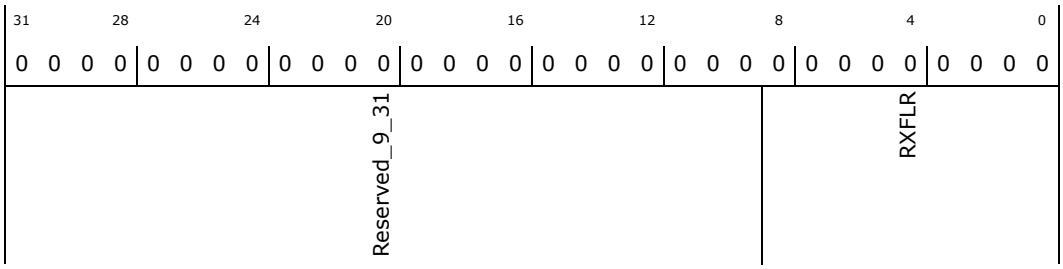
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RXFLR: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

3.37.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implemented one cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

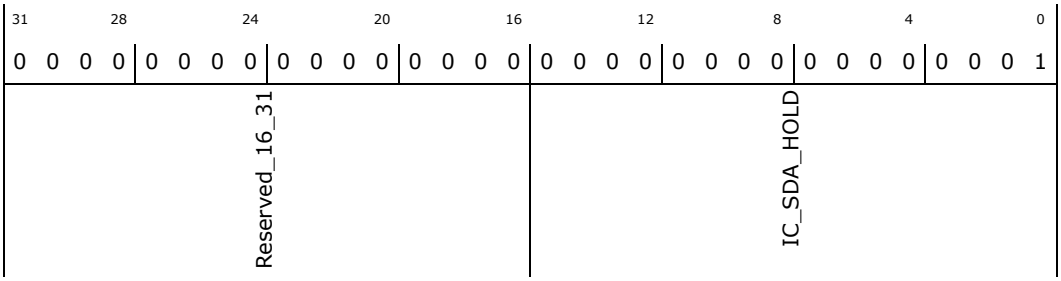
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_HOLD: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

3.37.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

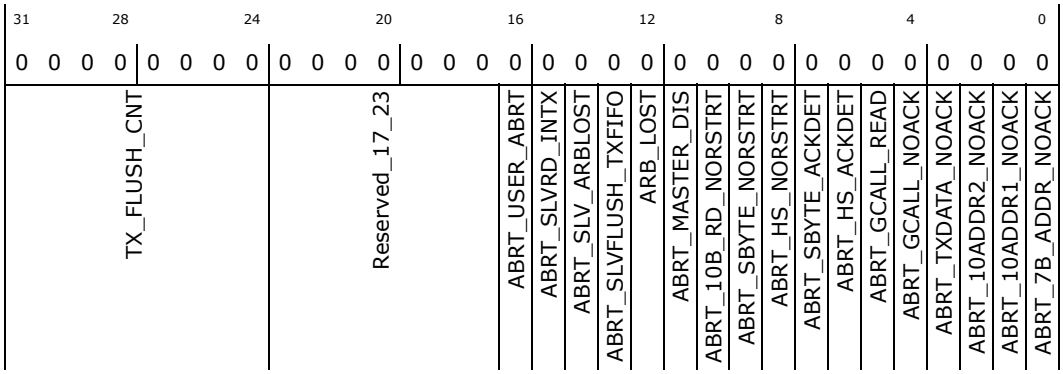
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_ABRT_SOURCE: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).

Bit Range	Default & Access	Description
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

3.37.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. This register only exists when the IC_SLV_DATA_NACK_ONLY parameter is set to 1. When this parameter disabled, this register does not exist and writing to the registers address has no effect. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

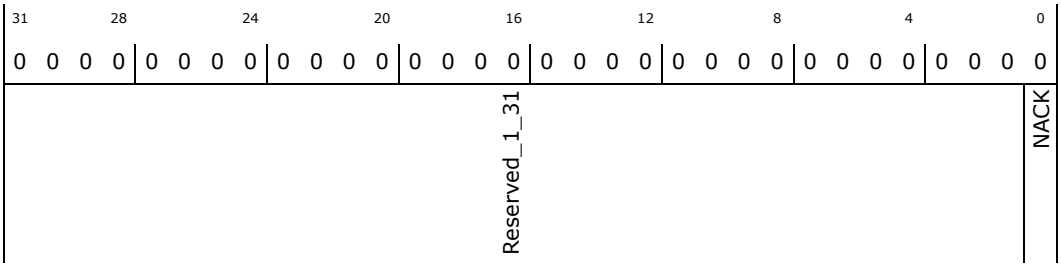
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SLV_DATA_NACK_ONLY: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slave receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

3.37.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

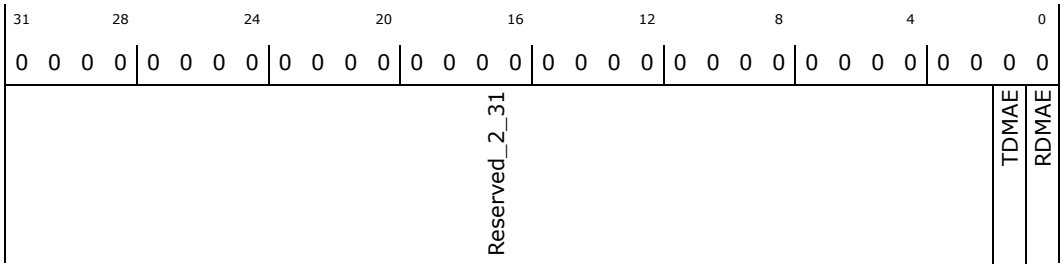
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_CR: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled

Bit Range	Default & Access	Description
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

3.37.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

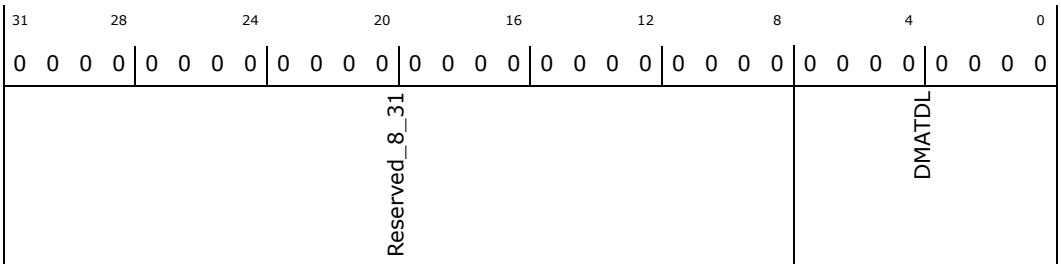
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_TDLR: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

3.37.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

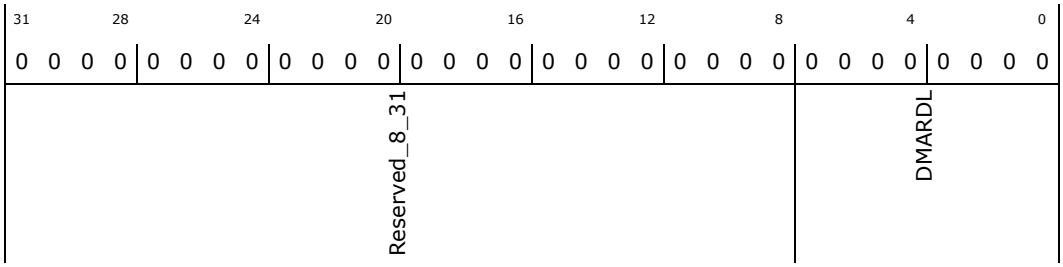
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_RDLR: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

3.37.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2.

NOTE: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

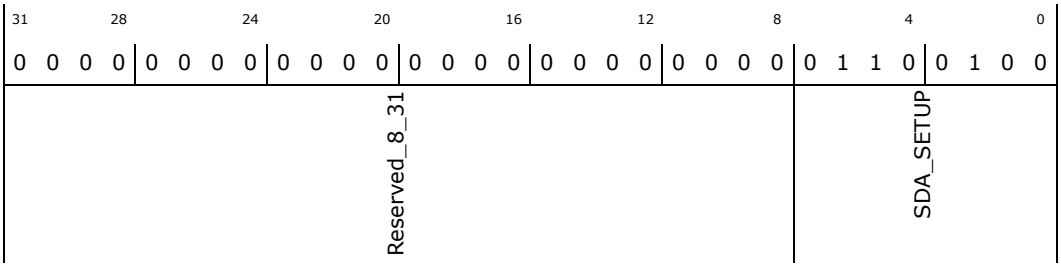
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_SETUP: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000064h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

3.37.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

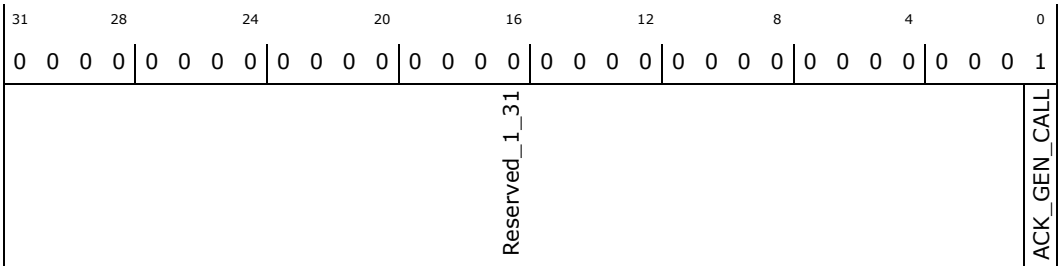
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ACK_GENERAL_CALL: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

3.37.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

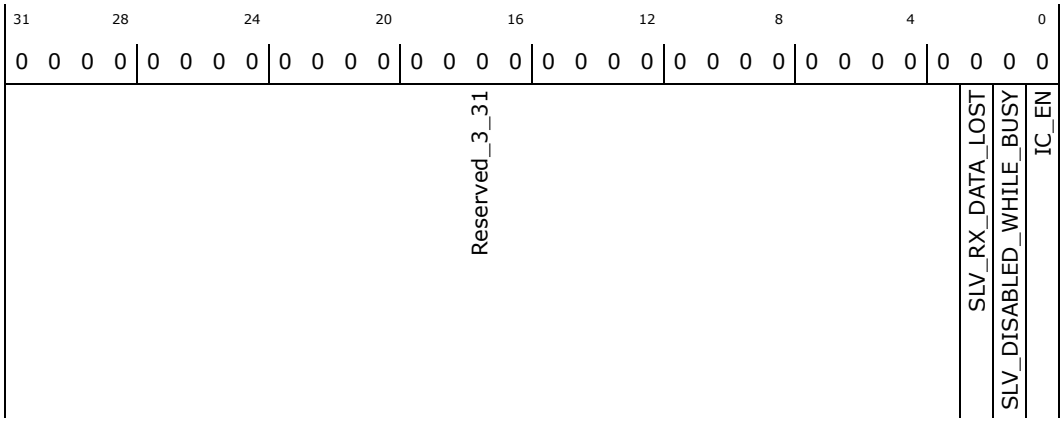
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE_STATUS: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

3.37.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

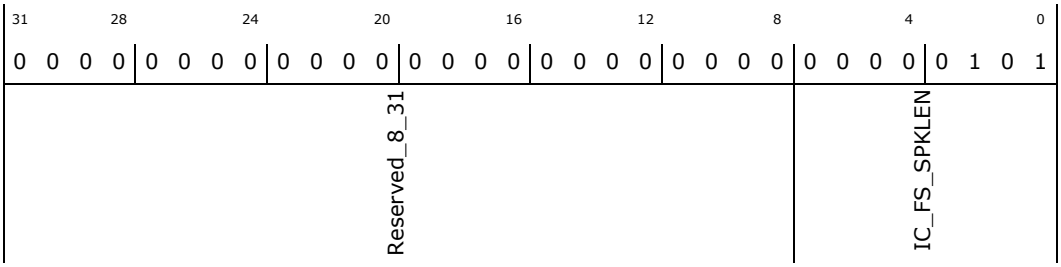
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SPKLEN: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000005h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. **Reset value:** IC_DEFAULT_FS_SPKLEN configuration parameter

3.37.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the

I2C Bus Specification. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

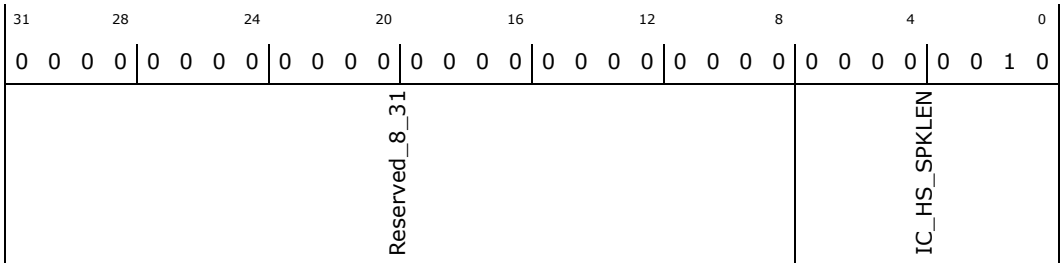
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SPKLEN: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. This register is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3. **Reset value:** IC_DEFAULT_HS_SPKLEN configuration parameter.

3.37.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

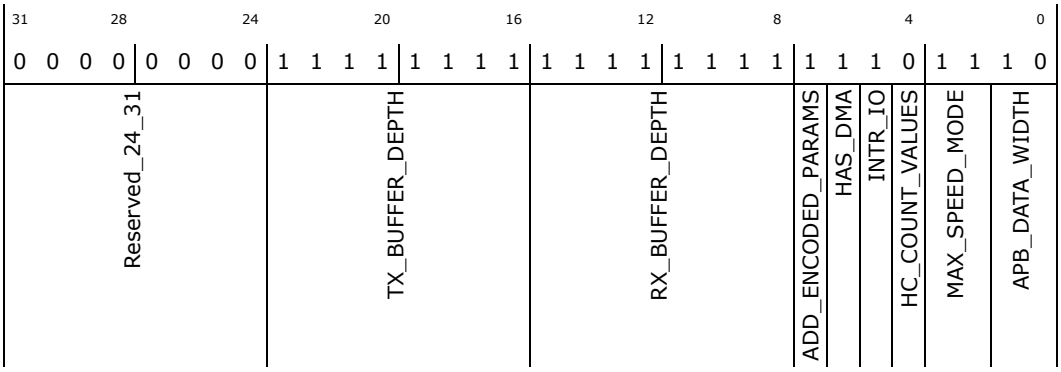
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_PARAM_1: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

3.37.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

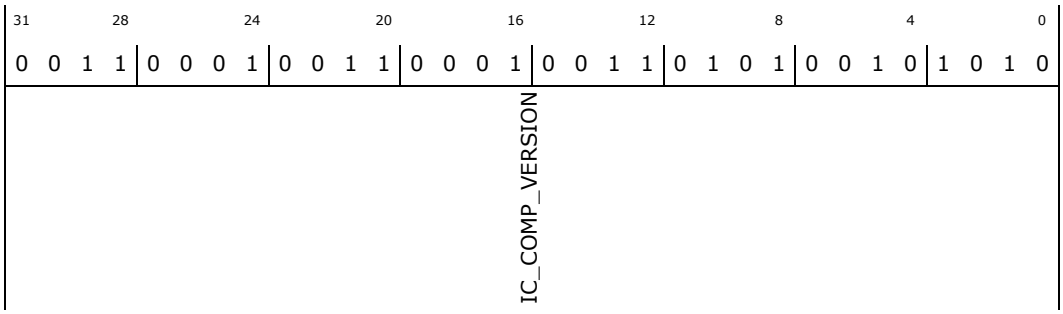
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_VERSION: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

3.37.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

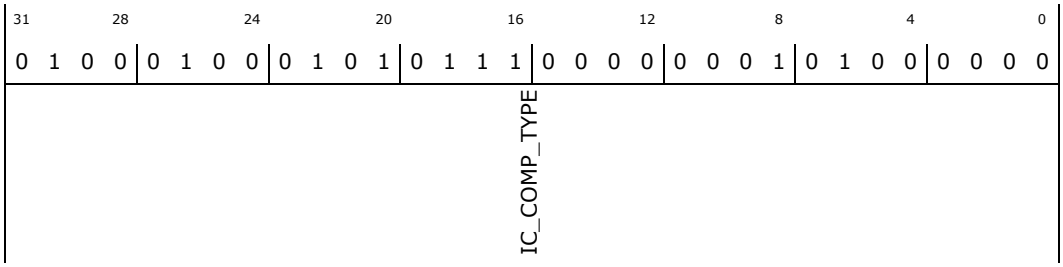
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_TYPE: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 44570140h



Bit Range	Default & Access	Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

3.37.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

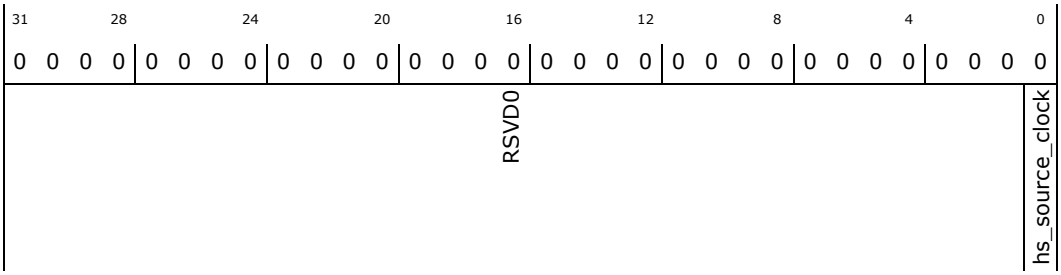
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CLOCK_PARAMS: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

3.37.47 Software Reset (RESETS)—Offset 804h

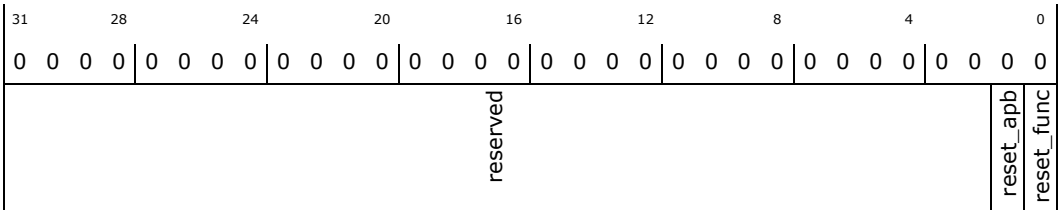
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.37.48 General Purpose Register (GENERAL)—Offset 808h

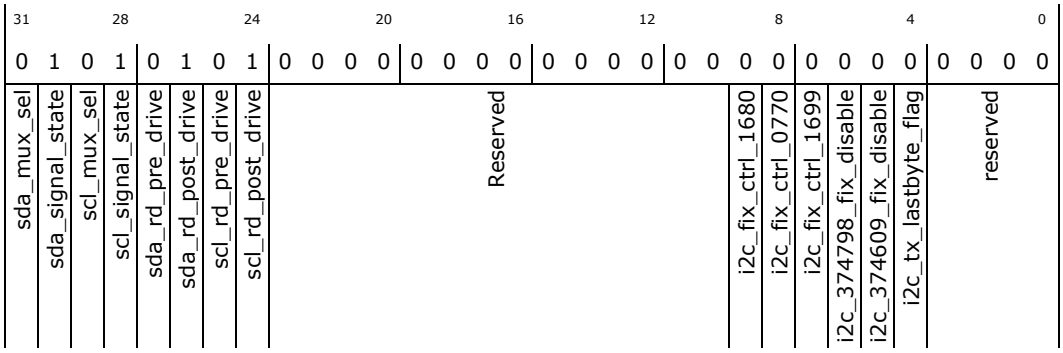
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 55000000h



Bit Range	Default & Access	Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)

Bit Range	Default & Access	Description
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

3.37.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

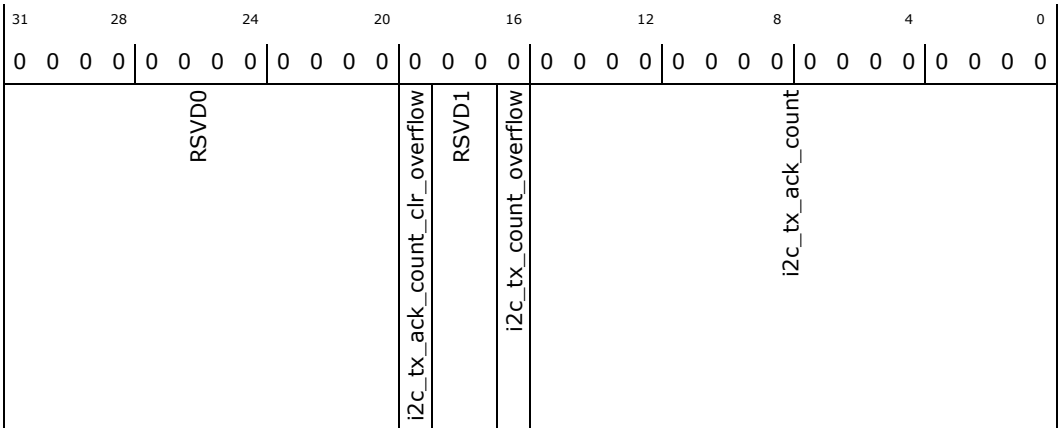
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_ACK_COUNT: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

3.37.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

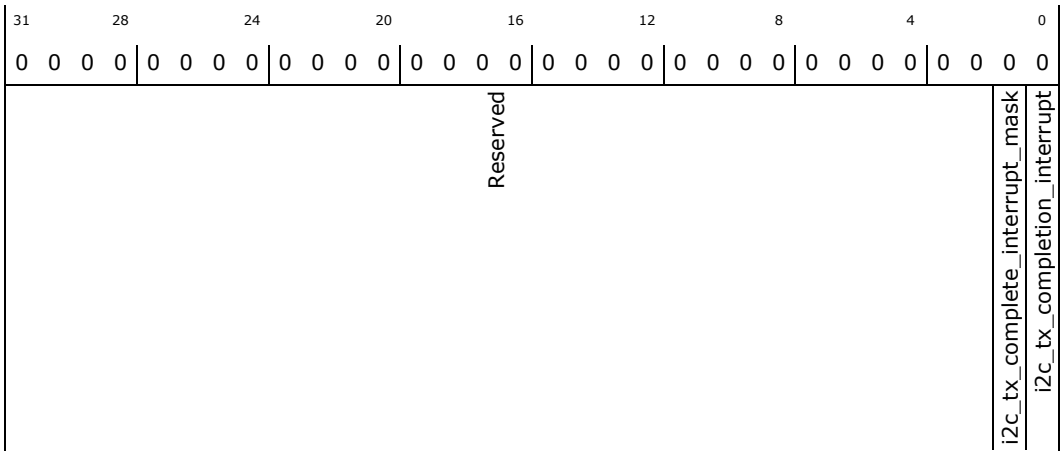
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_TX_COMPLETE_INTR_STAT: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

3.37.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

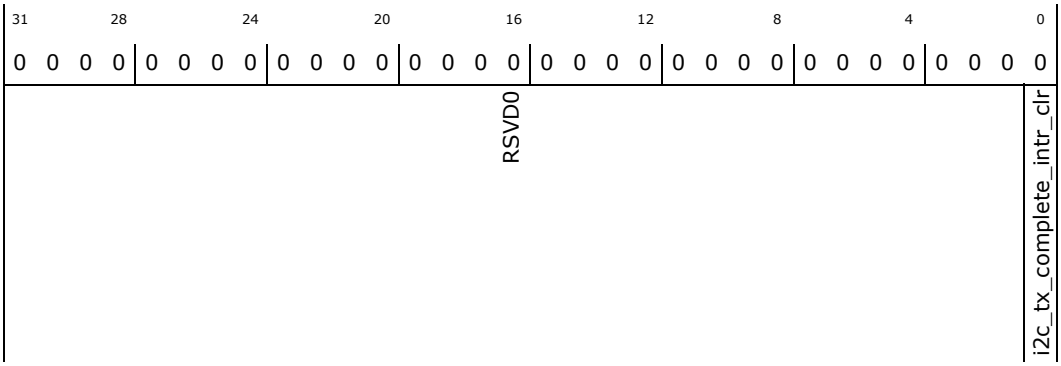
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

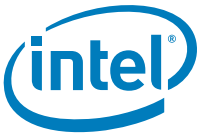
I2C_TX_COMPLETE_INTR_CLR: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt



3.38 SIO I2C3 PCI Configuration Registers

Table 46. Summary of SIO I2C3 PCI Configuration Registers—0/24/4

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2694	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2695	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2696	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2697	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2698	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2698	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2699	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2700	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2700	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2701	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2701	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2702	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2703	00000000h

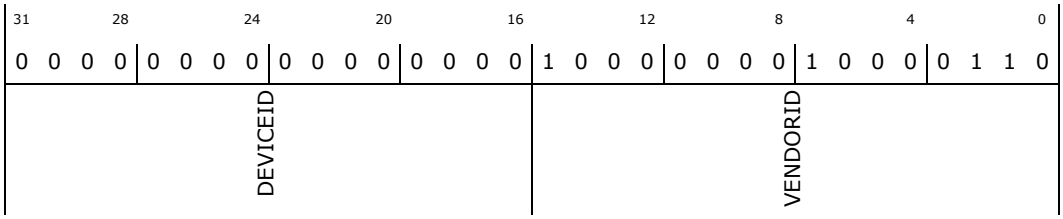
3.38.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:24, F:4] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

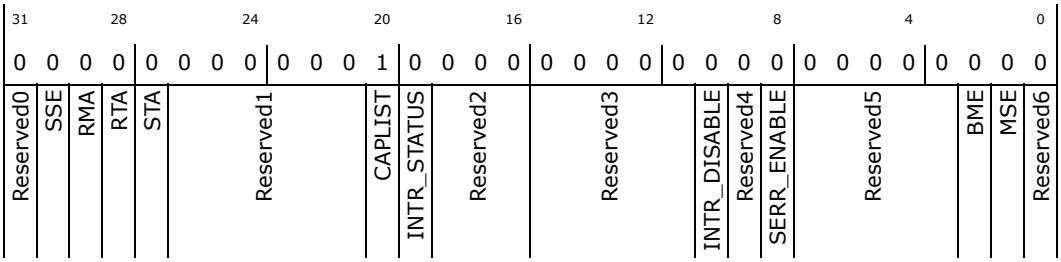
3.38.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:24, F:4] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

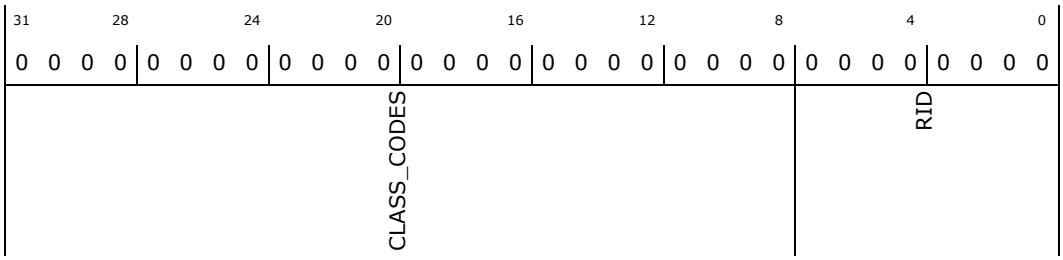
3.38.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:24, F:4] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

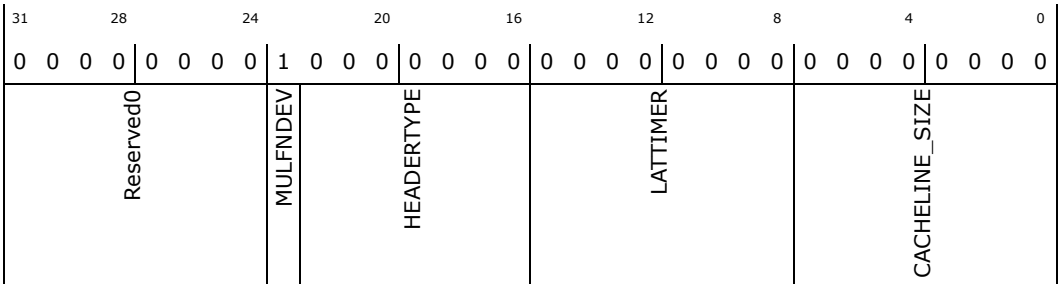
3.38.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:24, F:4] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

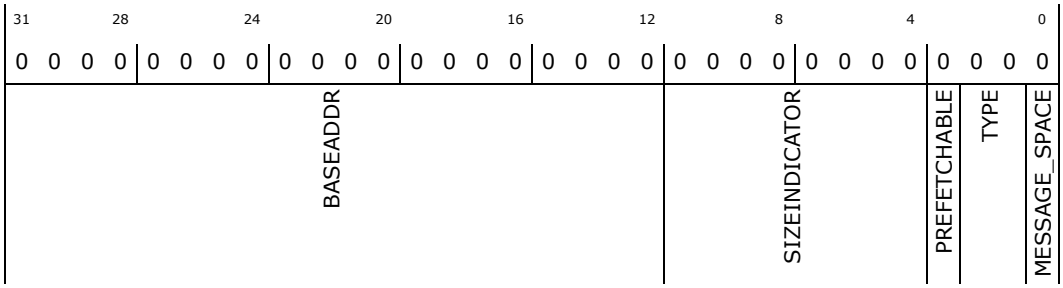
3.38.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

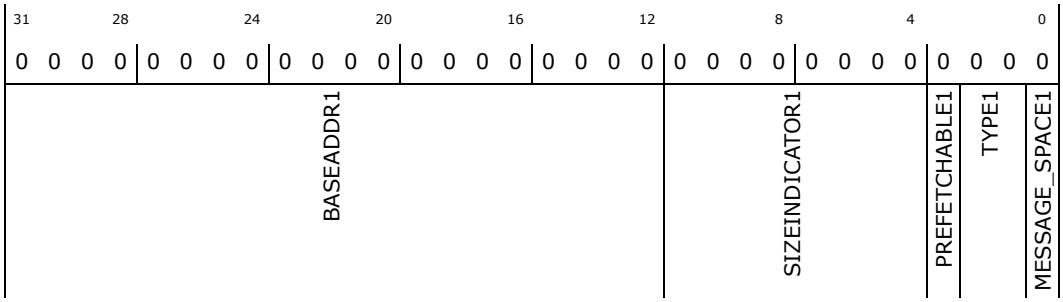
3.38.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:24, F:4] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

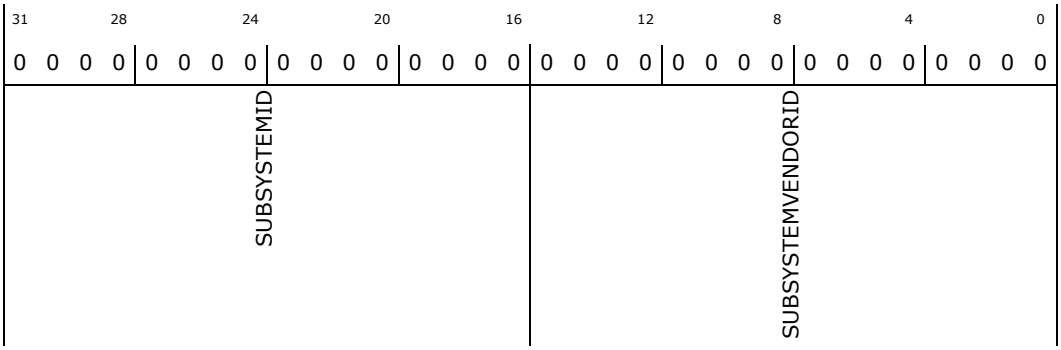
3.38.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:24, F:4] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

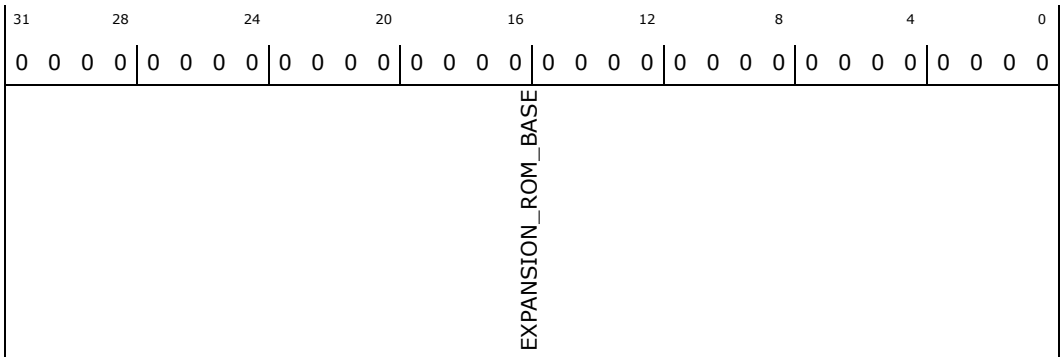
3.38.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:24, F:4] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

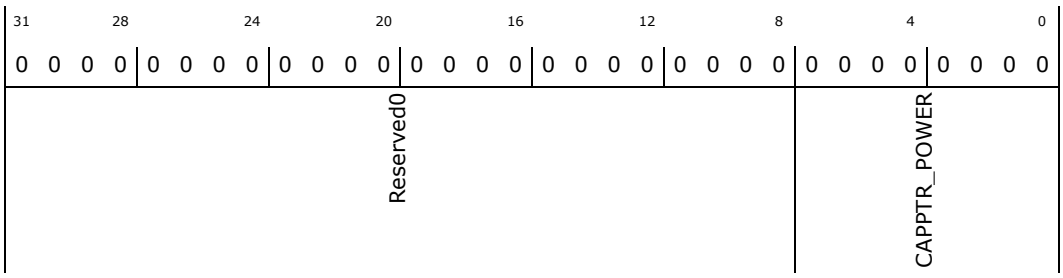
3.38.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:24, F:4] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

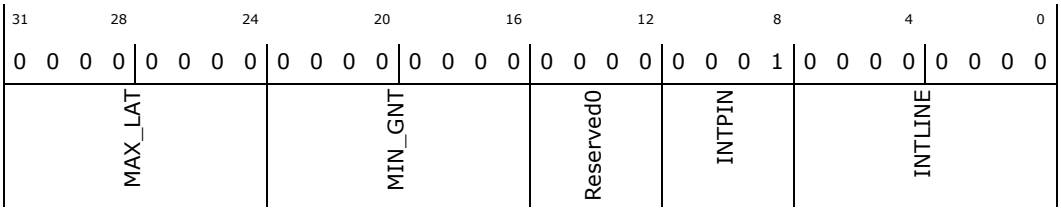
3.38.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

INTERRUPTREG: [B:0, D:24, F:4] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

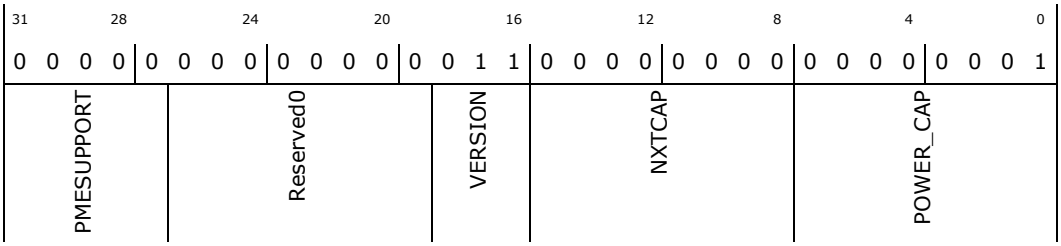
3.38.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

POWERCAPID: [B:0, D:24, F:4] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

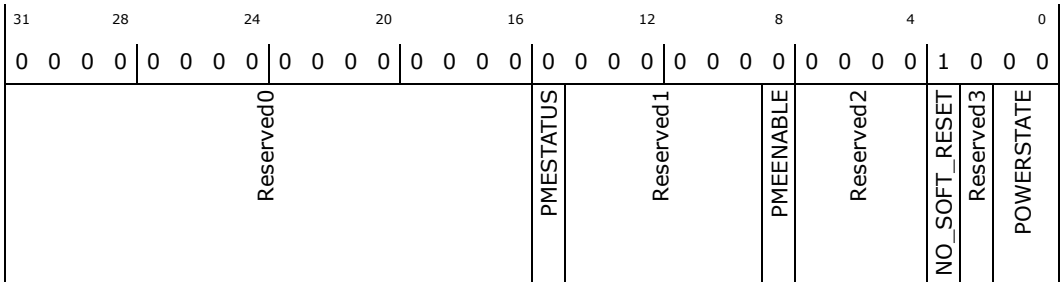
3.38.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:24, F:4] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

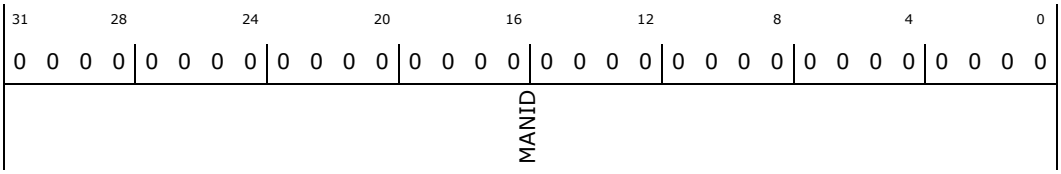
3.38.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:24, F:4] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

3.39 SIO I²C3 Memory Mapped IO Registers

Table 47. Summary of SIO I²C3 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 2706	0000007Fh
4h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 2707	00001055h
8h	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 2708	00000055h
Ch	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 2709	00000001h
10h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 2710	00000000h
14h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 2711	00000190h
18h	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 2712	000001D6h
1Ch	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 2712	0000003Ch
20h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 2713	00000082h
24h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 2714	0000000Ch
28h	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 2715	00000020h
2Ch	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 2716	00000000h
30h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 2717	000008FFh
34h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 2718	00000000h
38h	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 2720	00000010h
3Ch	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 2720	00000010h
40h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 2721	00000000h
44h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 2721	00000000h
48h	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 2722	00000000h
4Ch	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 2722	00000000h
50h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 2723	00000000h

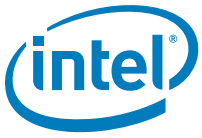


Table 47. Summary of SIO I²C3 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
54h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 2724	00000000h
58h	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 2724	00000000h
5Ch	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 2725	00000000h
60h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 2725	00000000h
64h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 2726	00000000h
68h	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 2726	00000000h
6Ch	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 2727	00000000h
70h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 2728	00000006h
74h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 2729	00000000h
78h	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 2730	00000000h
7Ch	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 2730	00000001h
80h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 2731	00000000h
84h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 2733	00000000h
88h	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 2734	00000000h
8Ch	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 2735	00000000h
90h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 2735	00000000h
94h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 2736	00000064h
98h	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 2737	00000001h
9Ch	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 2738	00000000h
A0h	4	"IC_FS_SPKLEN—Offset A0h" on page 2739	00000005h
A4h	4	"IC_HS_SPKLEN—Offset A4h" on page 2739	00000002h
F4h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 2740	00FFFFEEh
F8h	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 2741	3131352Ah
FCh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 2742	44570140h
800h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 2742	00000000h

Table 47. Summary of SIO I²C3 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
804h	4	"Software Reset (RESETS)—Offset 804h" on page 2743	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 2744	55000000h
818h	4	"I2C_ACK_COUNT—Offset 818h" on page 2745	00000000h
820h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 2746	00000000h
824h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 2746	00000000h

3.39.1 I2C Control Register (IC_CON)—Offset 0h

If configuration parameter I2C_DYNAMIC_TAR_UPDATE = 0, all bits are Read/Write.

If I2C_DYNAMIC_TAR_UPDATE = 1, bit 4 is Read-only.

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

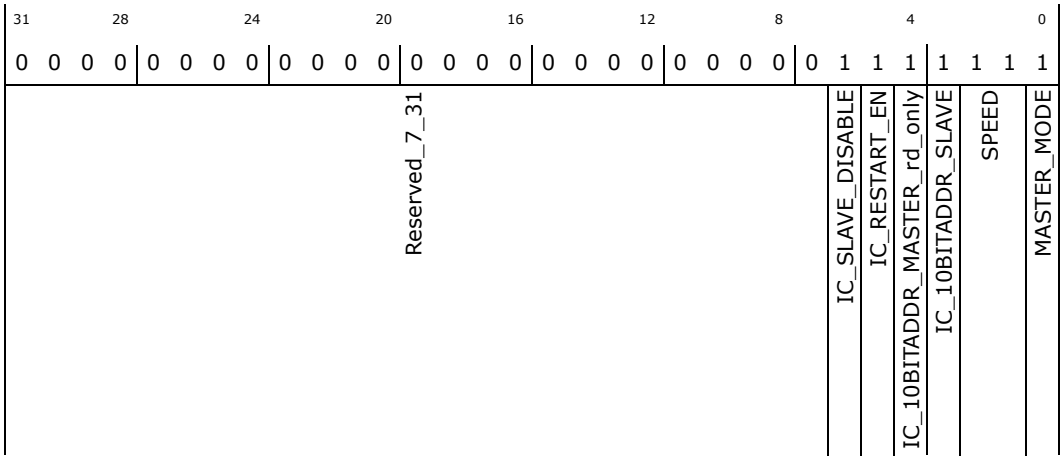
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CON: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

3.39.2 I2C Target Address Register (IC_TAR)—Offset 4h

If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to No (0), this register is 12 bits wide, and bits 15:12 are reserved. Writes to this register succeed only when IC_ENABLE is set to 0.

However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND

- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

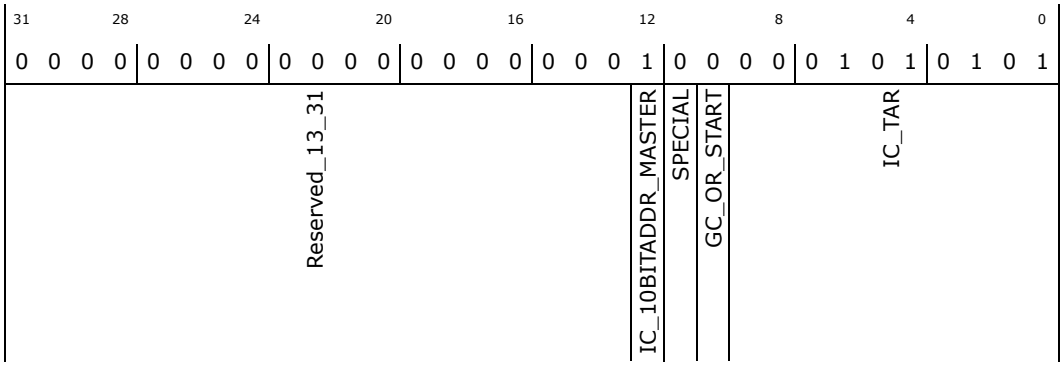
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TAR: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00001055h



Bit Range	Default & Access	Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

3.39.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

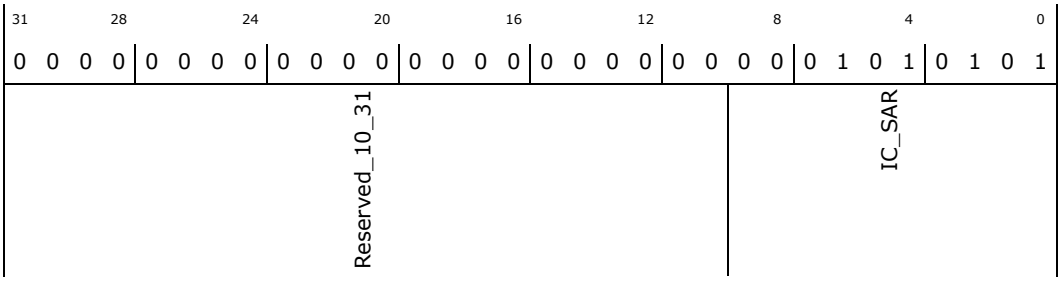
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SAR: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000055h



Bit Range	Default & Access	Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.39.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

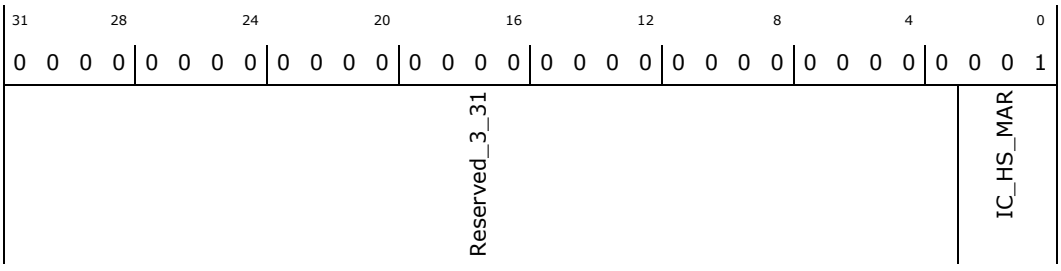
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_MADDR: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highs peed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.39.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

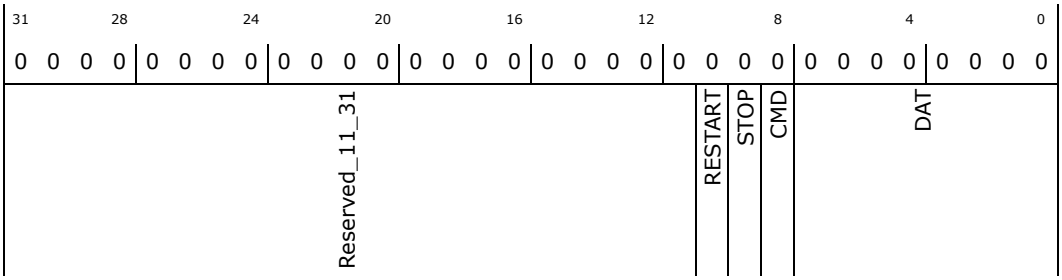
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DATA_CMD: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:11	0b RW	**Reserved_11_31:** Reserved.

Bit Range	Default & Access	Description
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/ received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

3.39.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

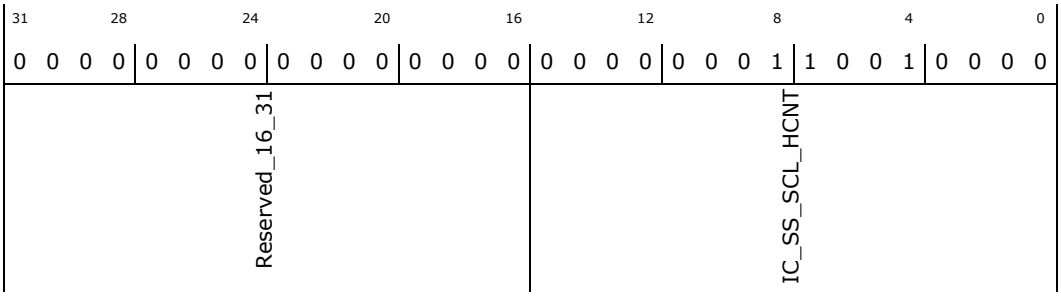
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_HCNT: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000190h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.39.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

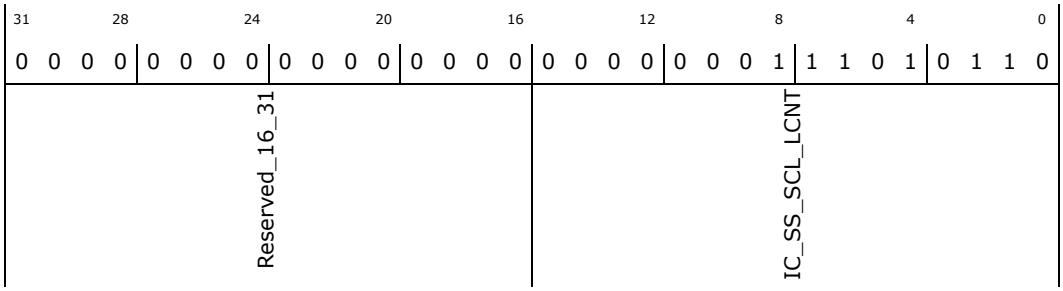
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_LCNT: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 000001D6h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.39.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

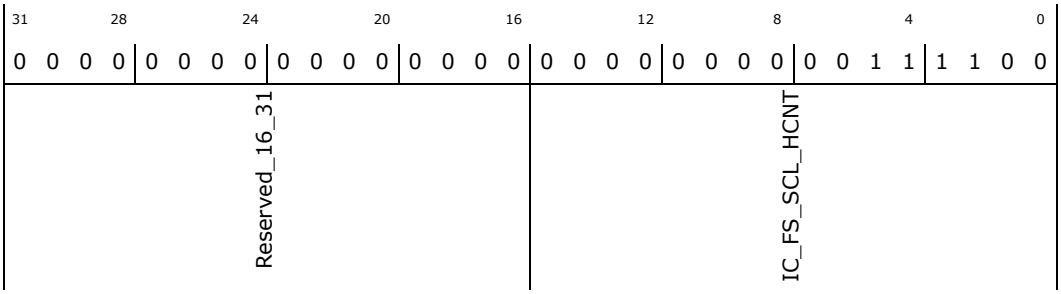
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_HCNT: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.39.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to 'IC_CLK Frequency Configuration' in the Synopsis DesignWare DW_apb_i2c Databook.

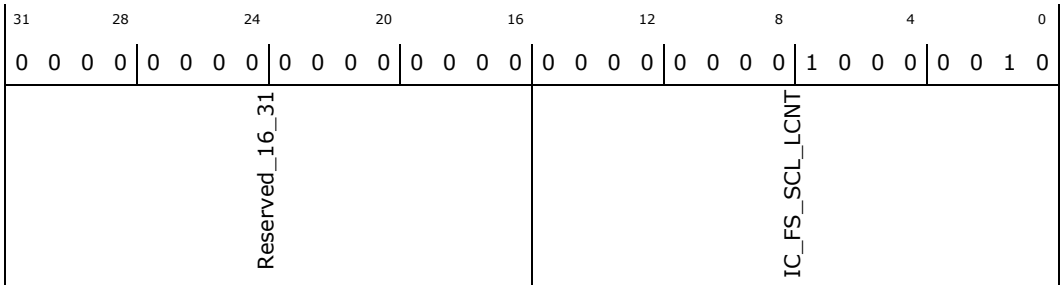
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_LCNT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000082h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.39.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* .

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

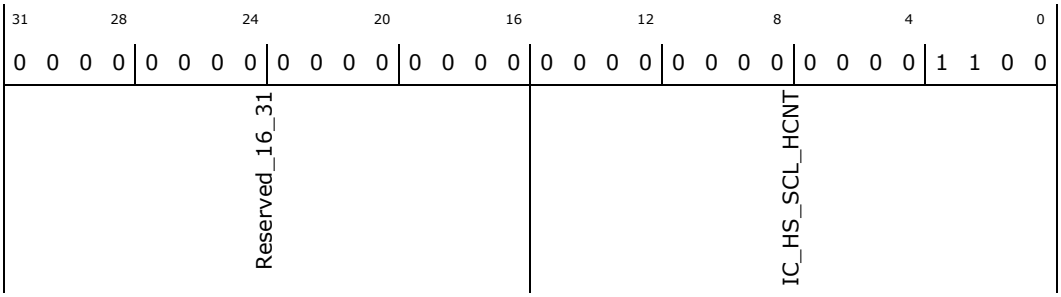
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_HCNT: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.39.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* in the Synopsis DesignWare DW_apb_i2c Databook.

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

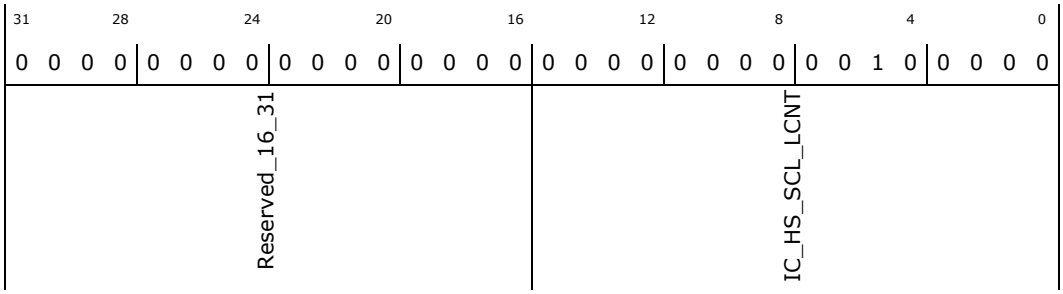
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_LCNT: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000020h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.39.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

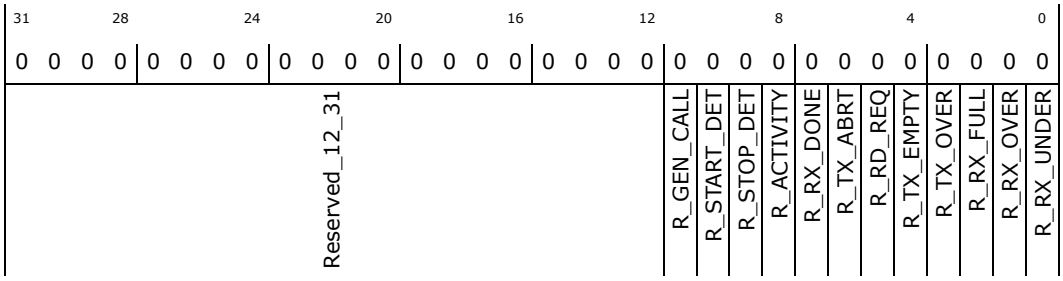
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

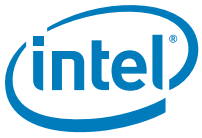
IC_INTR_STAT: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.



Bit Range	Default & Access	Description
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

3.39.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

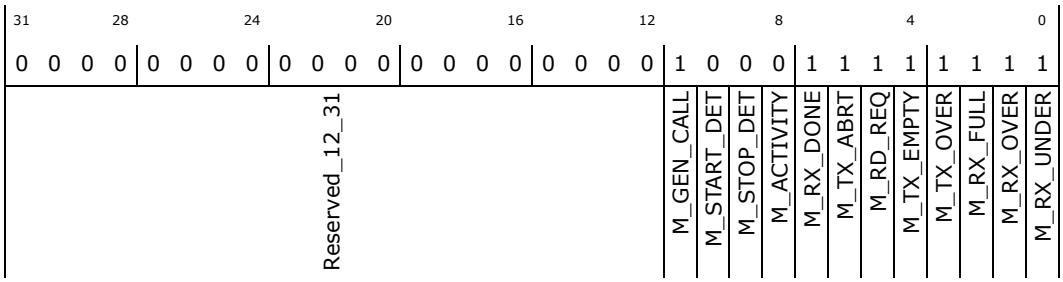
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_INTR_MASK: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 000008FFh



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

3.39.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

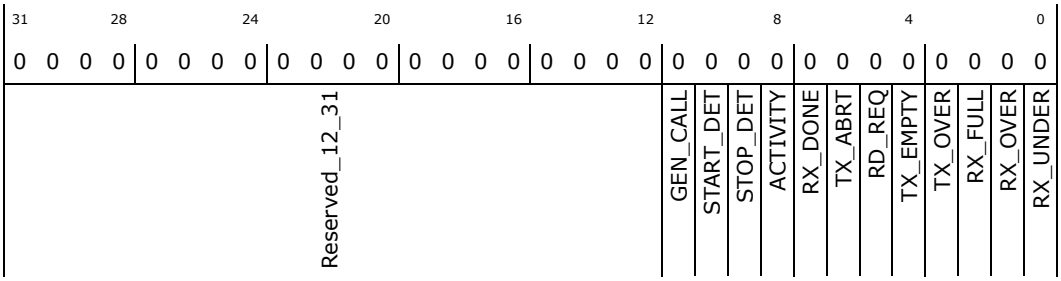
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RAW_INTR_STAT: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

3.39.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

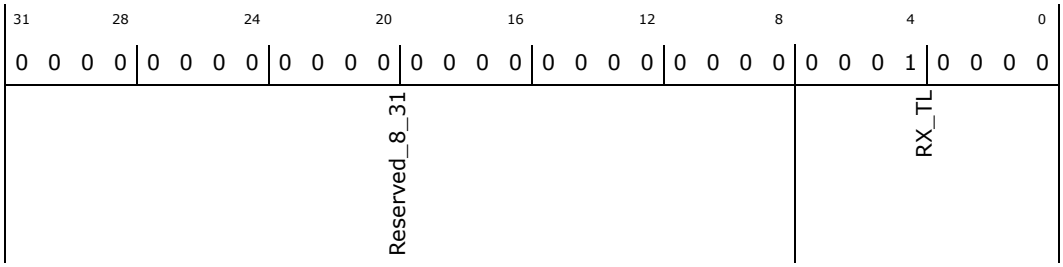
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RX_TL: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.39.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

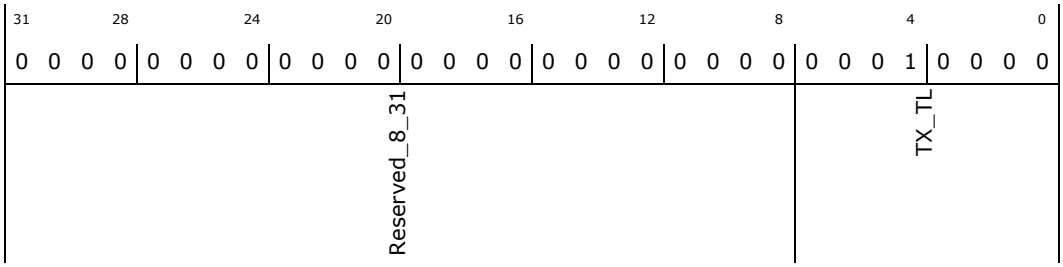
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_TL: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.39.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

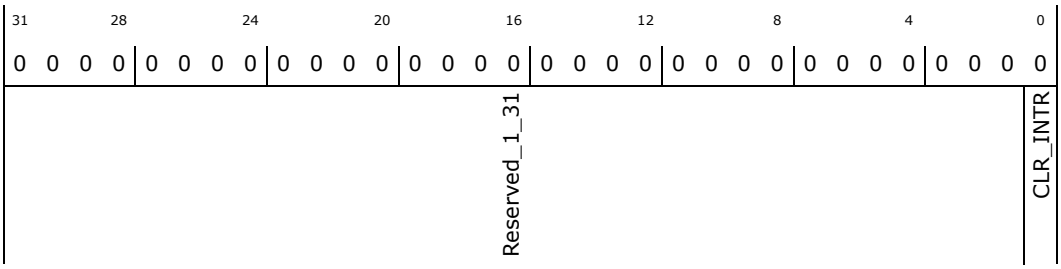
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_INTR: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

3.39.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

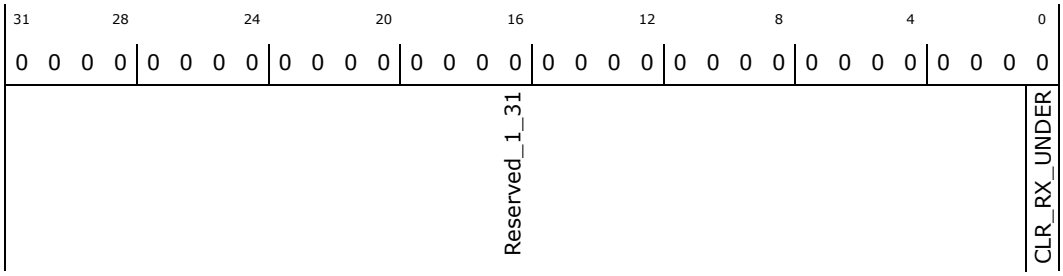
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_UNDER: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

3.39.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

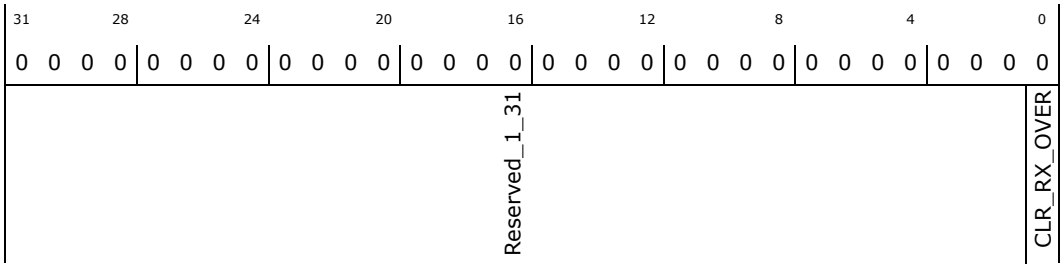
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_OVER: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

3.39.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

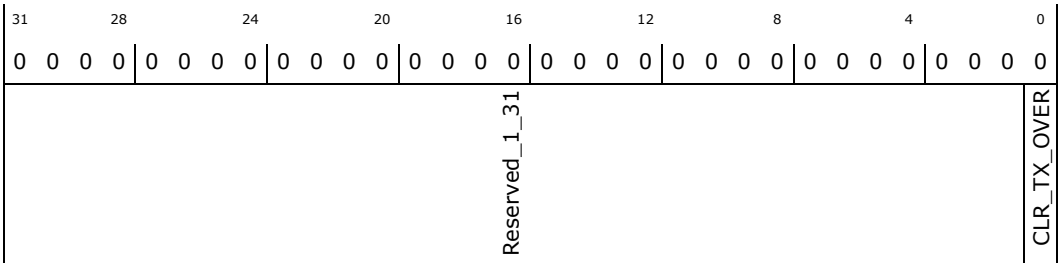
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_OVER: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

3.39.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

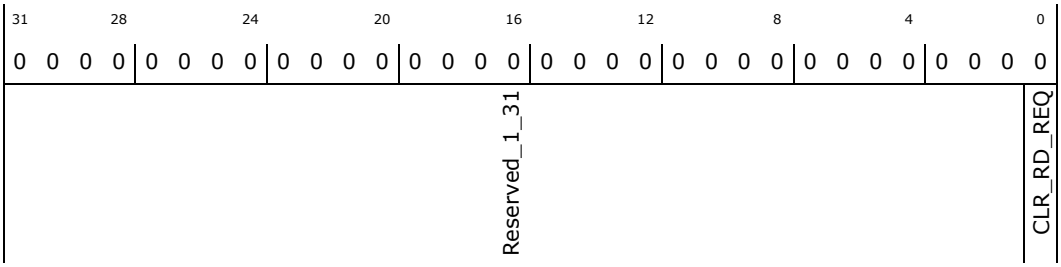
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RD_REQ: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

3.39.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

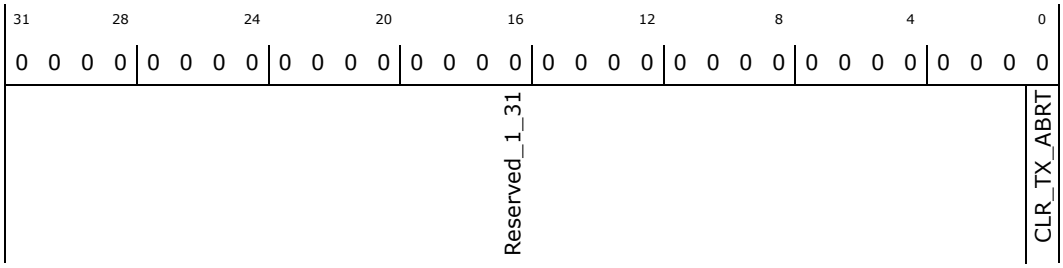
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_ABRT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

3.39.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

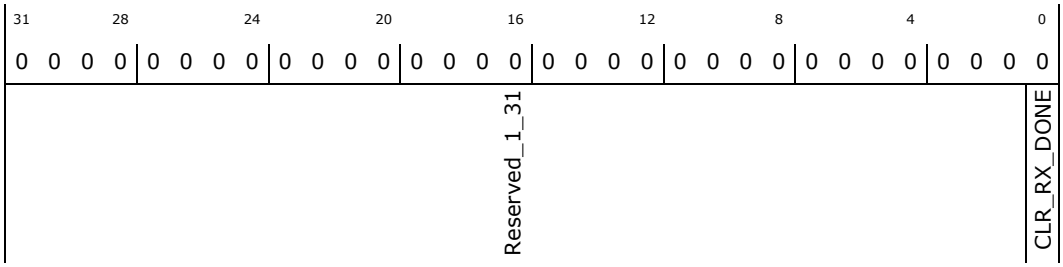
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_DONE: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

3.39.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

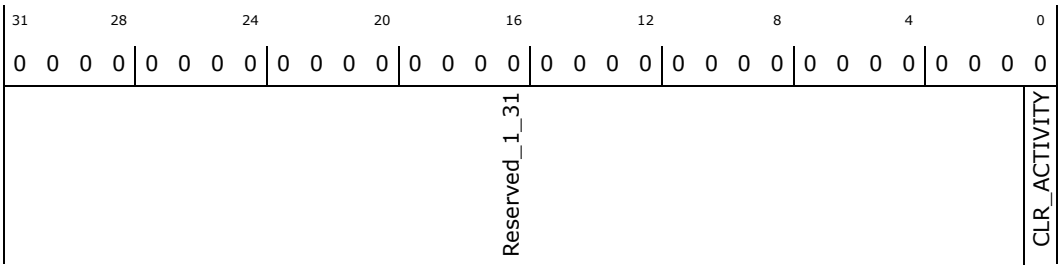
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_ACTIVITY: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

3.39.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

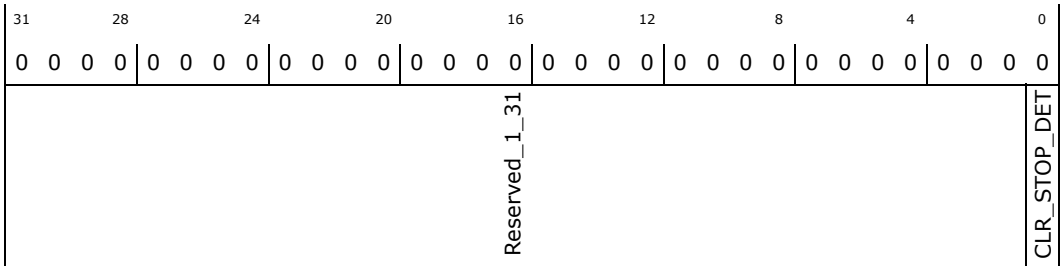
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_STOP_DET: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

3.39.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

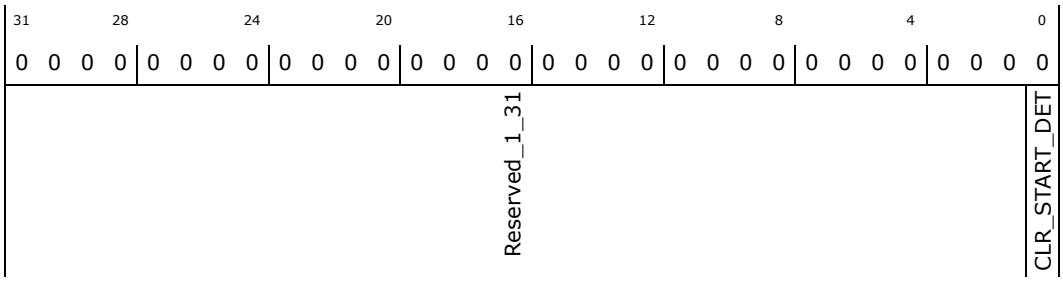
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_START_DET: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

3.39.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

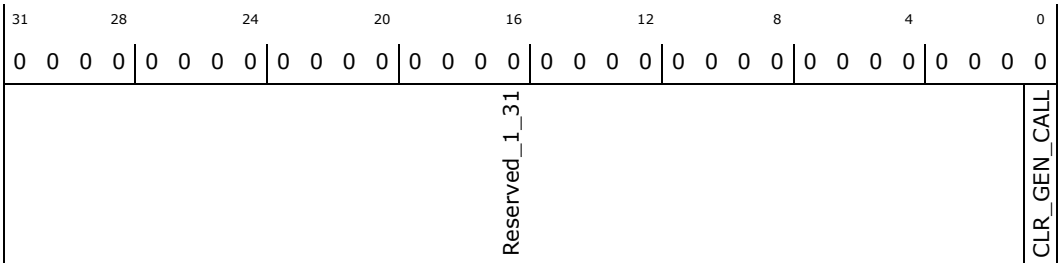
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_GEN_CALL: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

3.39.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

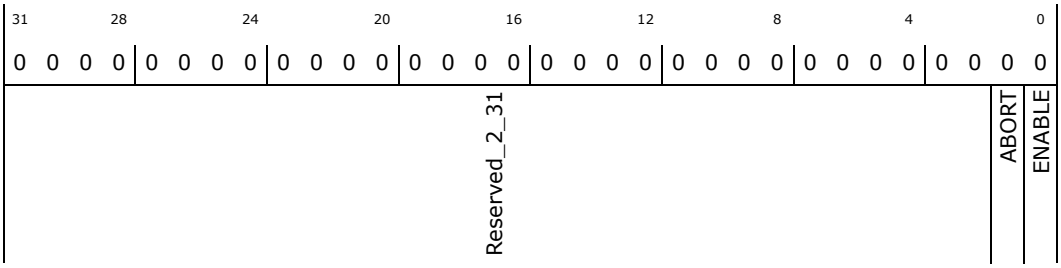
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.

Bit Range	Default & Access	Description
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

3.39.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

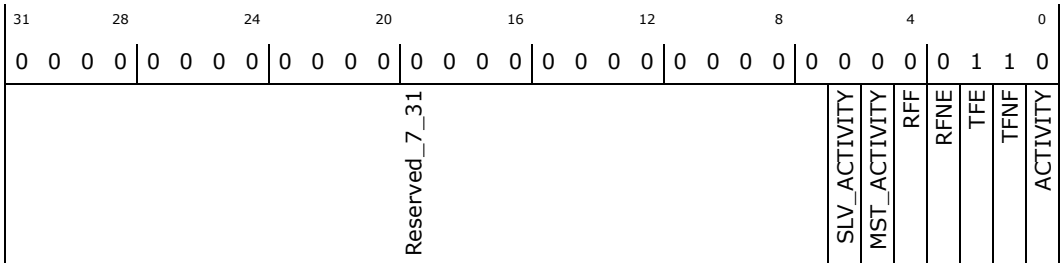
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_STATUS: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.

Bit Range	Default & Access	Description
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

3.39.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

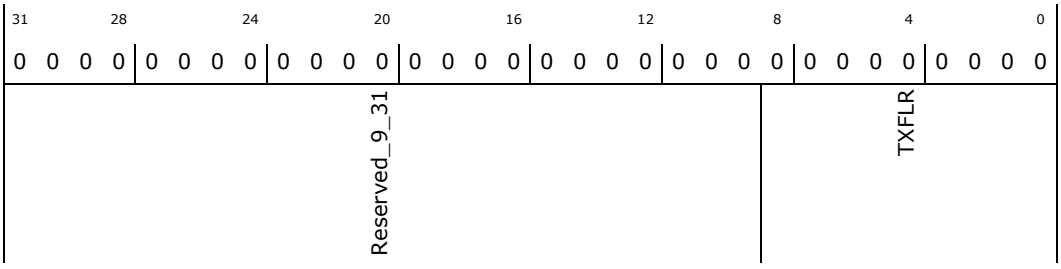
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TXFLR: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

3.39.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

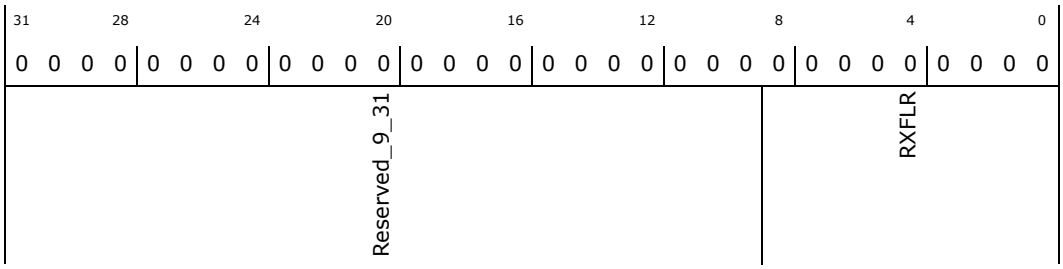
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RXFLR: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

3.39.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implemented one cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

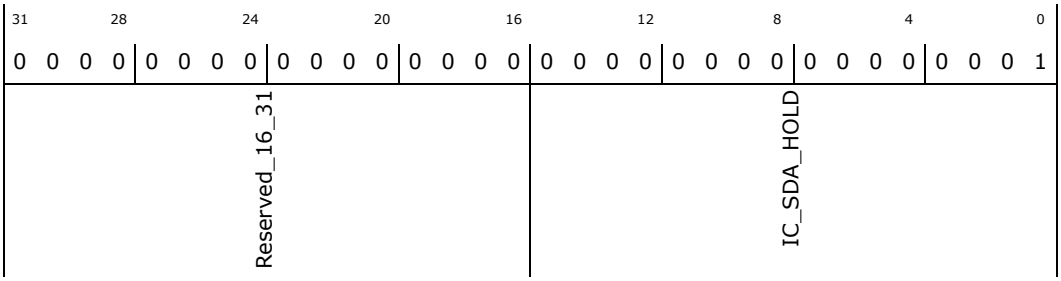
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_HOLD: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

3.39.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

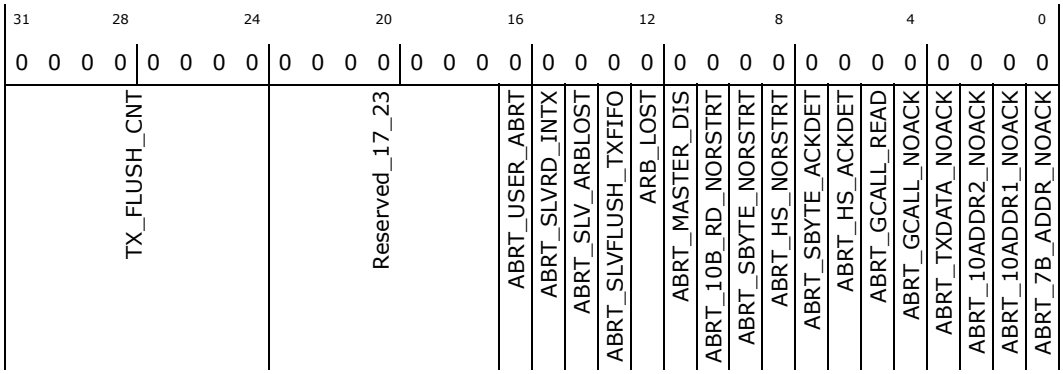
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_ABRT_SOURCE: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).

Bit Range	Default & Access	Description
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

3.39.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. This register only exists when the IC_SLV_DATA_NACK_ONLY parameter is set to 1. When this parameter disabled, this register does not exist and writing to the registers address has no effect. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

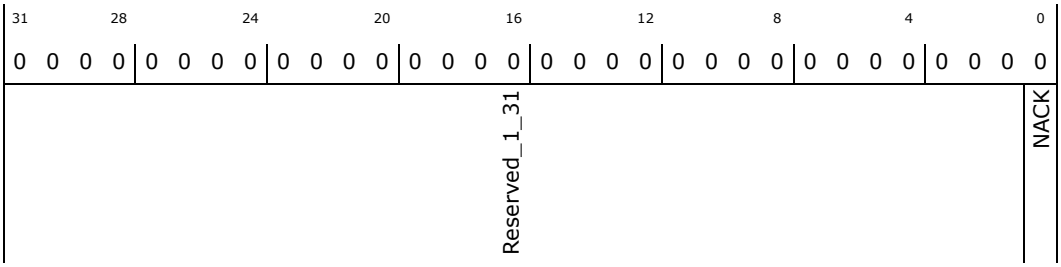
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SLV_DATA_NACK_ONLY: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slave receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

3.39.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

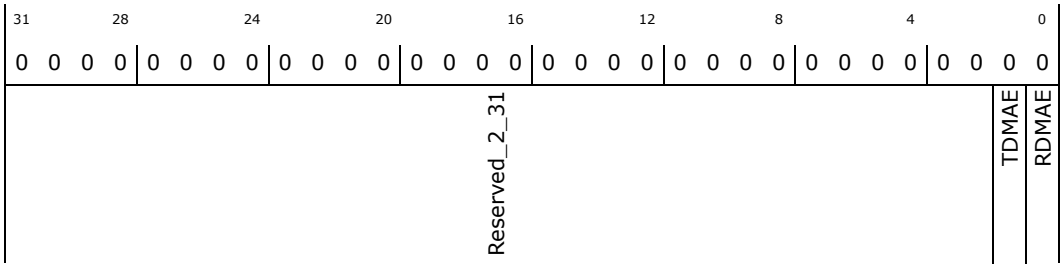
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_CR: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled

Bit Range	Default & Access	Description
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

3.39.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

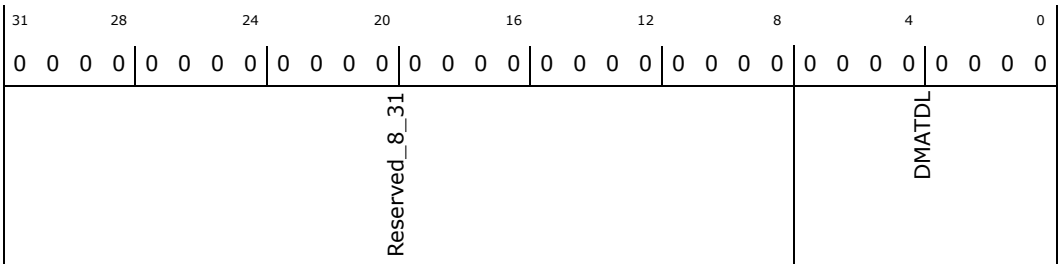
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_TDLR: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

3.39.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

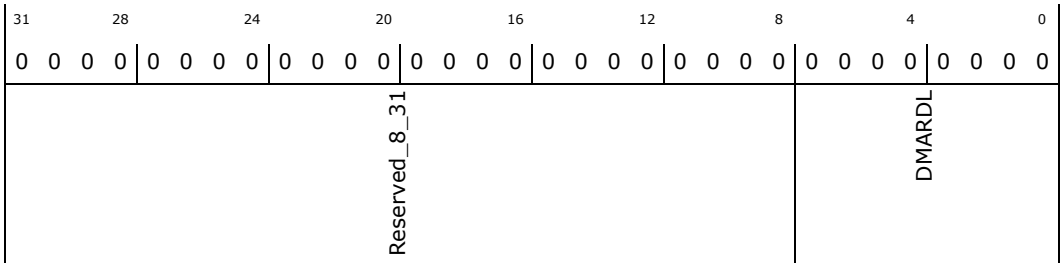
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_RDLR: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

3.39.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2.

NOTE: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

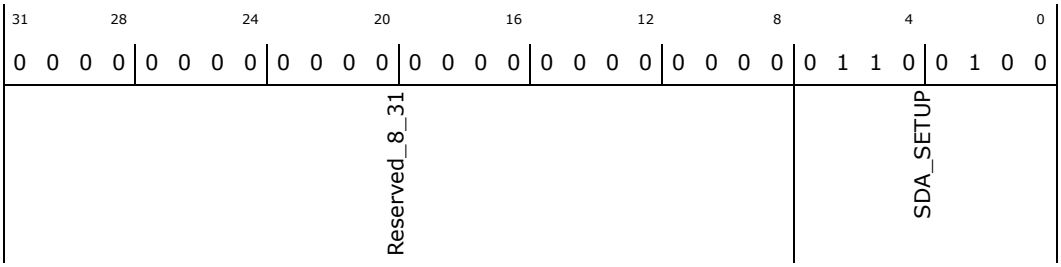
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_SETUP: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000064h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

3.39.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

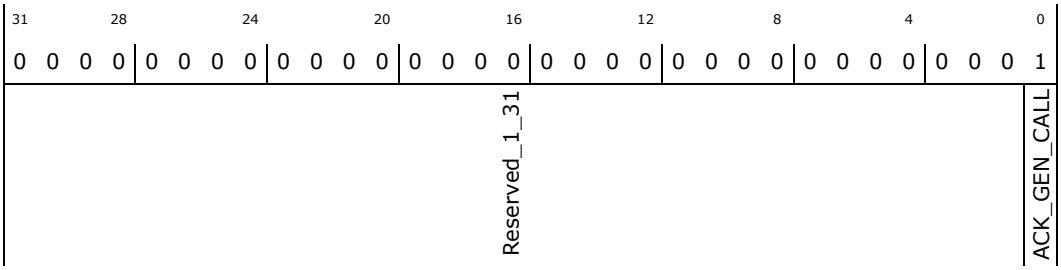
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ACK_GENERAL_CALL: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

3.39.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

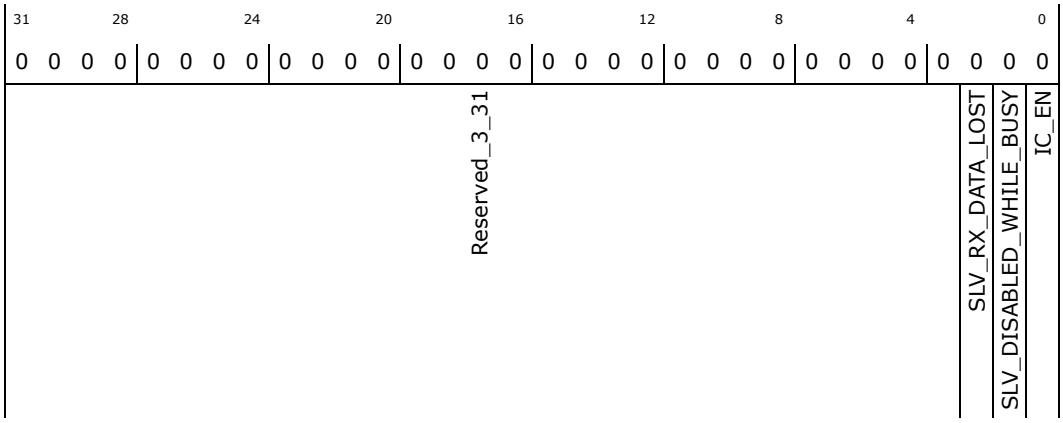
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE_STATUS: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

3.39.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

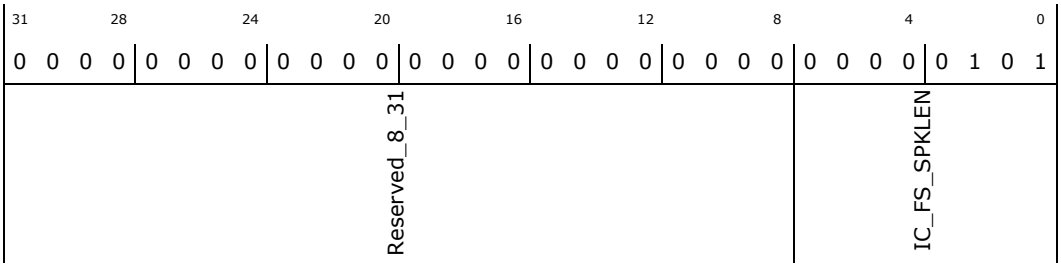
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SPKLEN: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000005h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. **Reset value:** IC_DEFAULT_FS_SPKLEN configuration parameter

3.39.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the

I2C Bus Specification. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

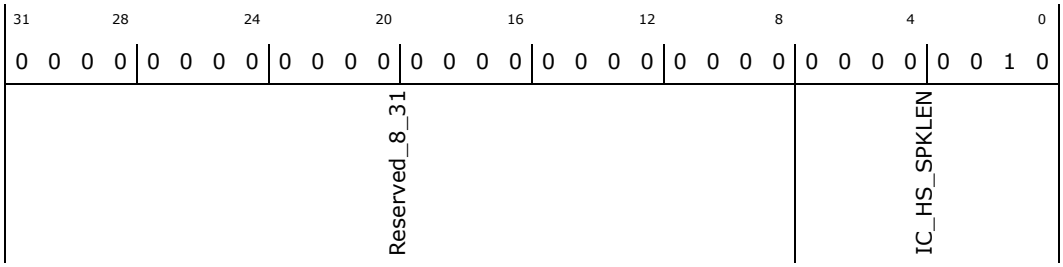
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SPKLEN: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. This register is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3. **Reset value:** IC_DEFAULT_HS_SPKLEN configuration parameter.

3.39.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

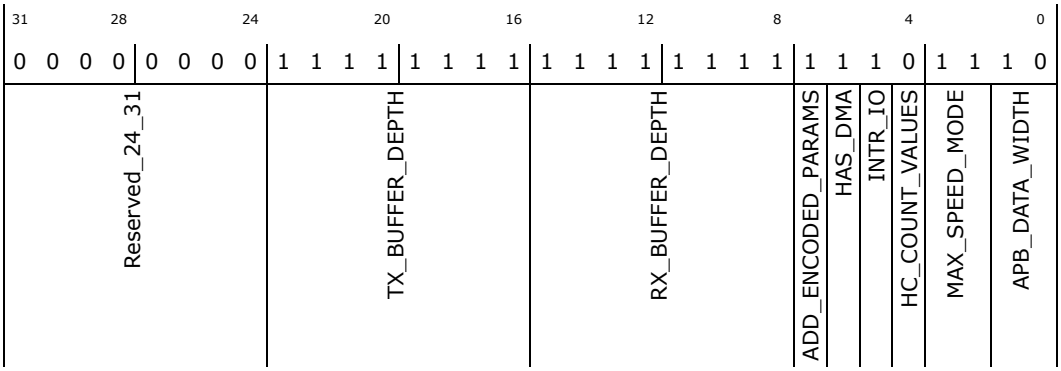
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_PARAM_1: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

3.39.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

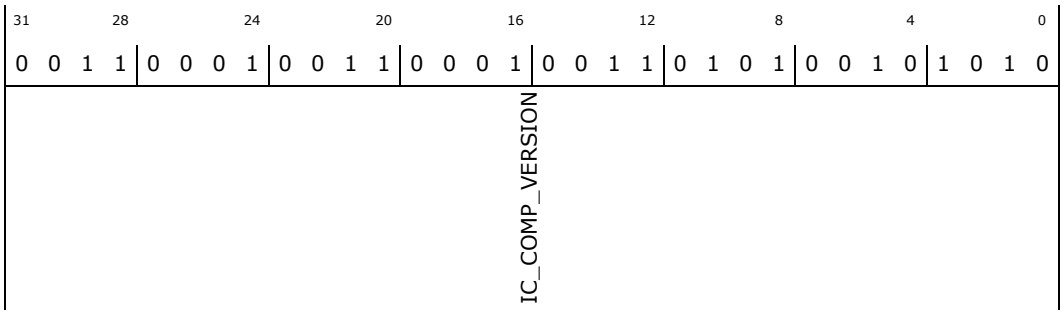
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_VERSION: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

3.39.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

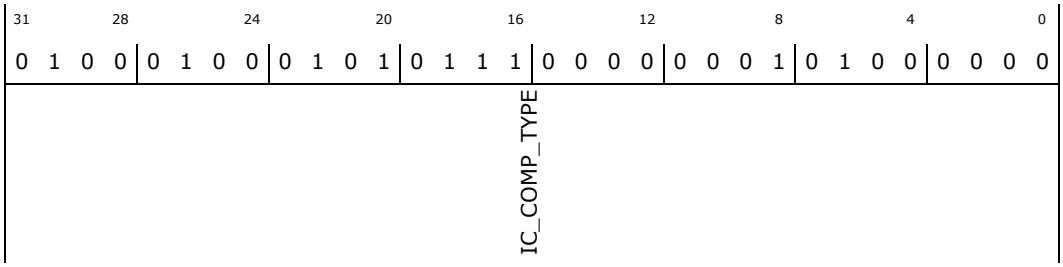
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_TYPE: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 44570140h



Bit Range	Default & Access	Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

3.39.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

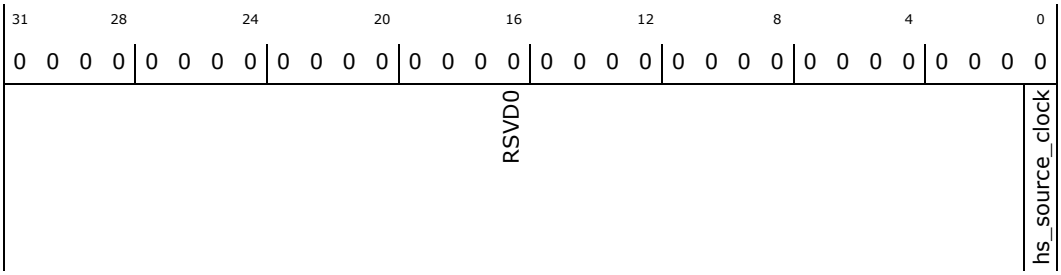
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CLOCK_PARAMS: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

3.39.47 Software Reset (RESETS)—Offset 804h

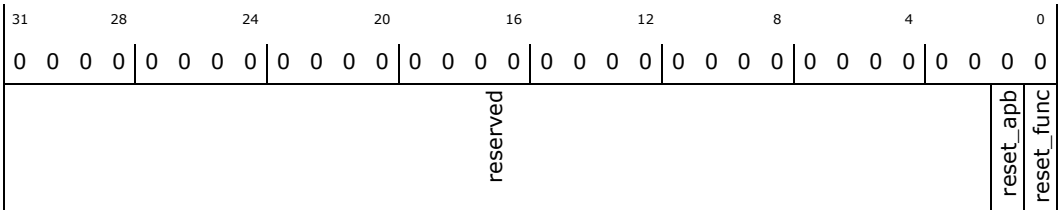
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.39.48 General Purpose Register (GENERAL)—Offset 808h

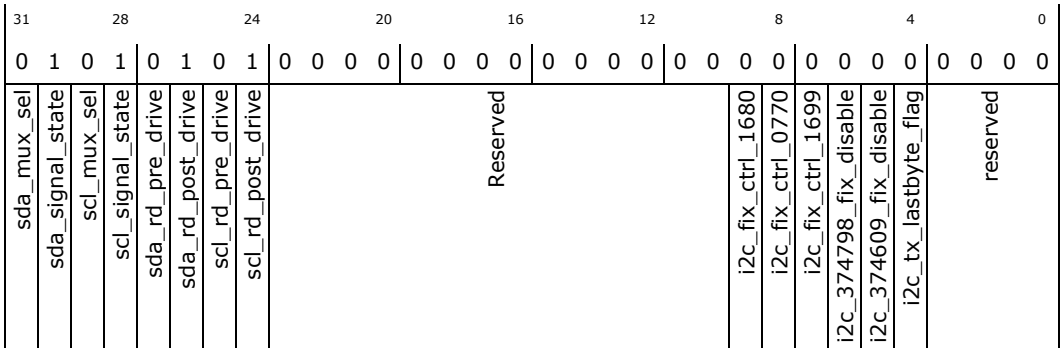
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 55000000h



Bit Range	Default & Access	Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)

Bit Range	Default & Access	Description
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

3.39.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

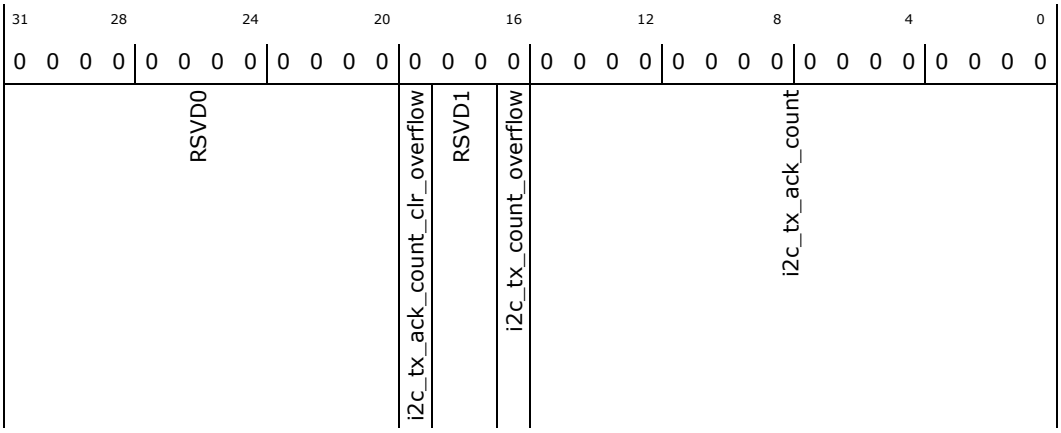
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_ACK_COUNT: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

3.39.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

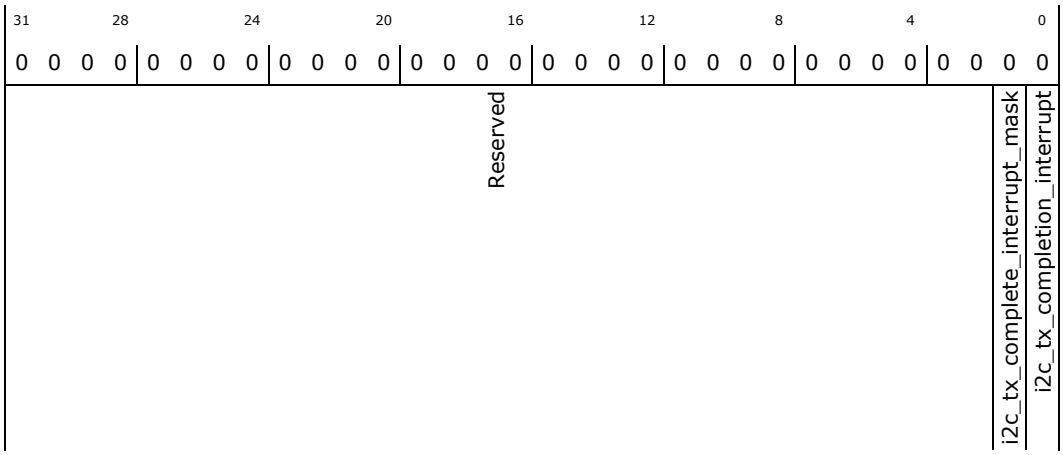
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_TX_COMPLETE_INTR_STAT: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

3.39.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

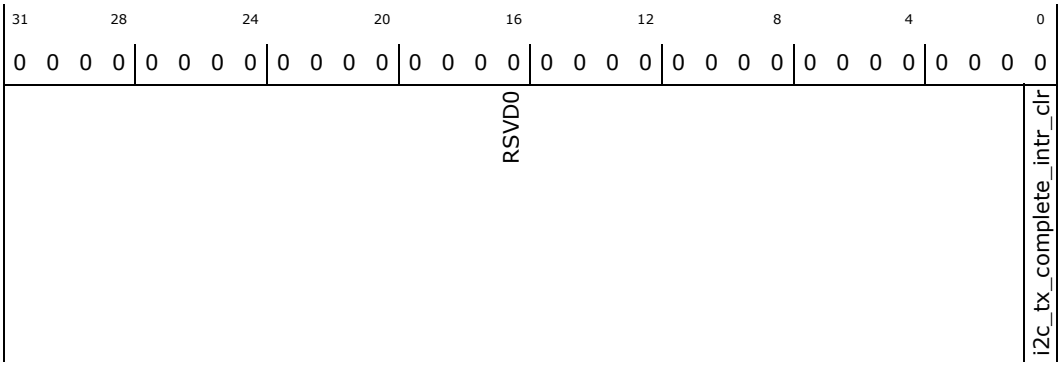
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_TX_COMPLETE_INTR_CLR: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

3.40 SIO I2C4 PCI Configuration Registers

Table 48. Summary of SIO I2C4 PCI Configuration Registers—0/24/5

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2748	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2749	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2750	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2751	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2752	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2752	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2753	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2754	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2754	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2755	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2755	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2756	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2757	00000000h

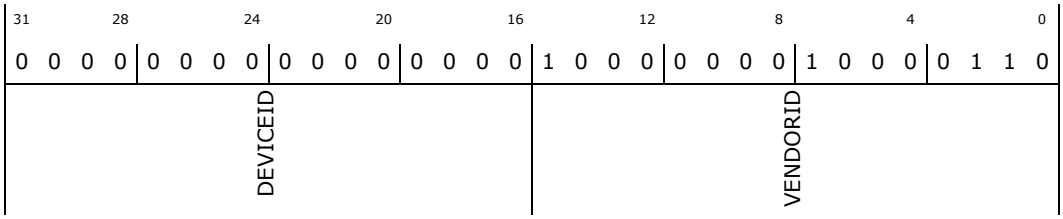
3.40.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:24, F:5] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

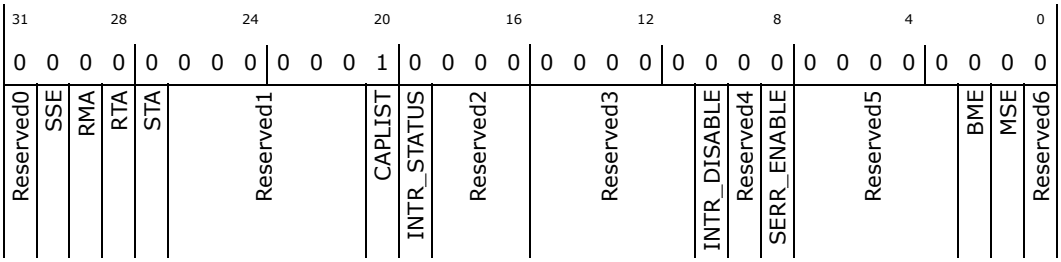
3.40.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:24, F:5] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

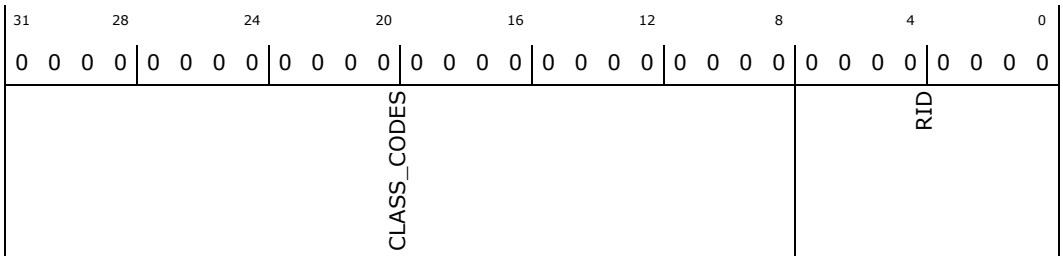
3.40.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:24, F:5] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

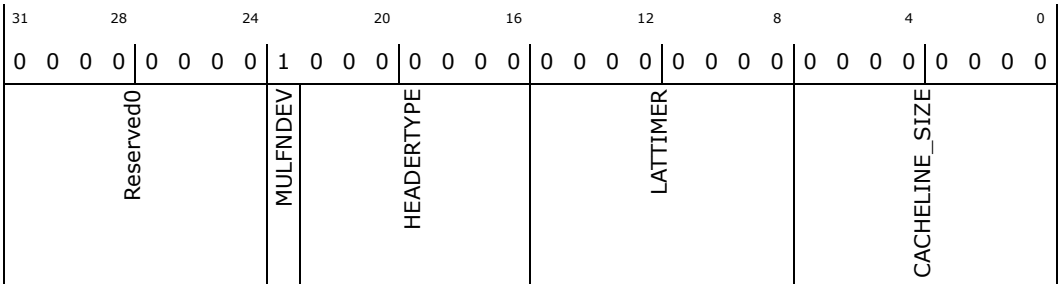
3.40.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:24, F:5] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

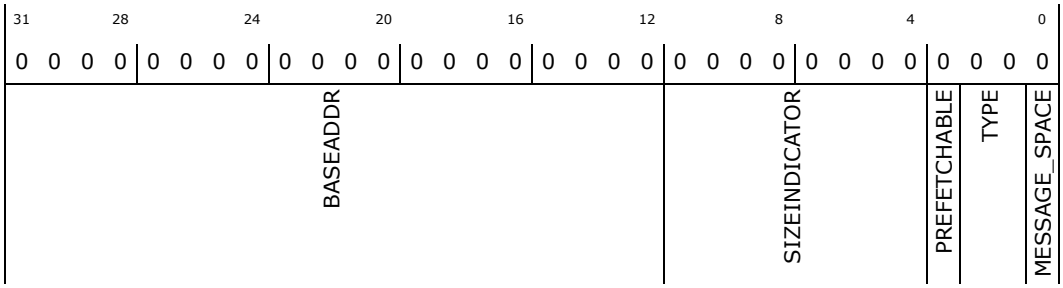
3.40.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

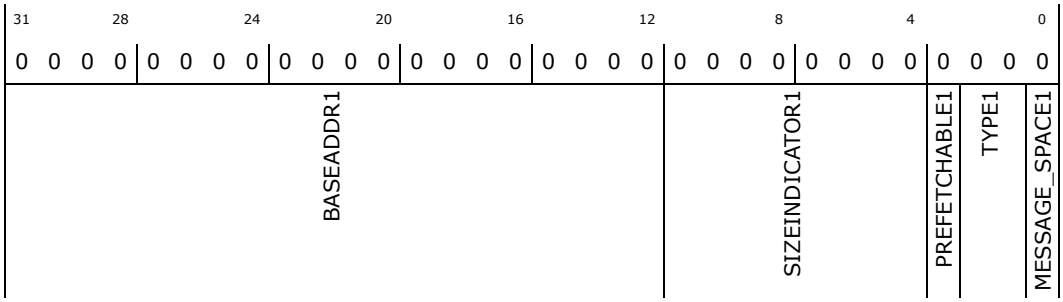
3.40.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:24, F:5] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

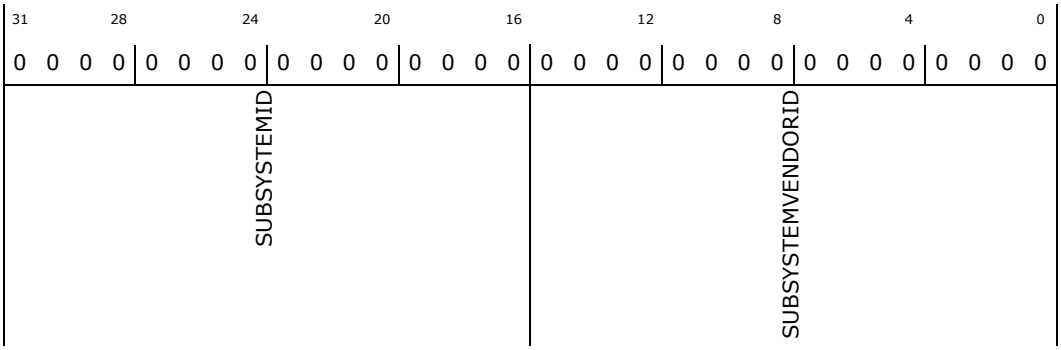
3.40.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:24, F:5] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

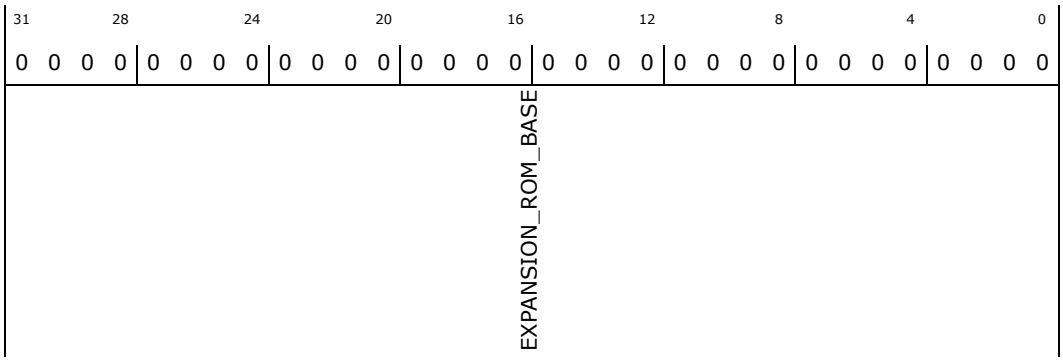
3.40.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:24, F:5] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

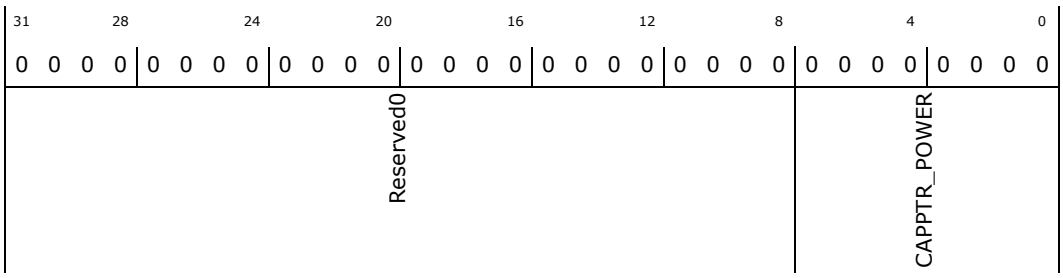
3.40.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:24, F:5] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

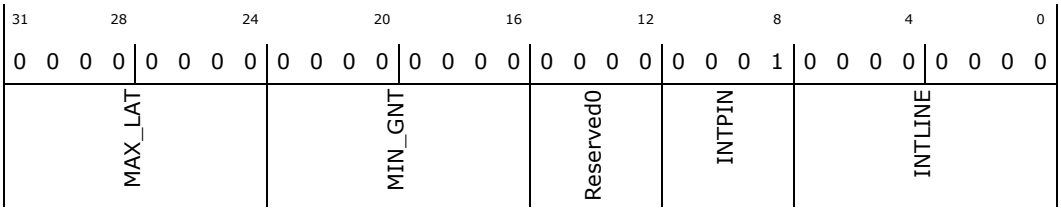
3.40.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

INTERRUPTREG: [B:0, D:24, F:5] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

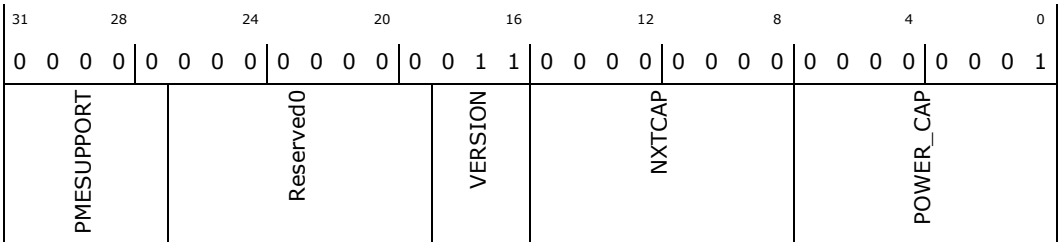
3.40.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

POWERCAPID: [B:0, D:24, F:5] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

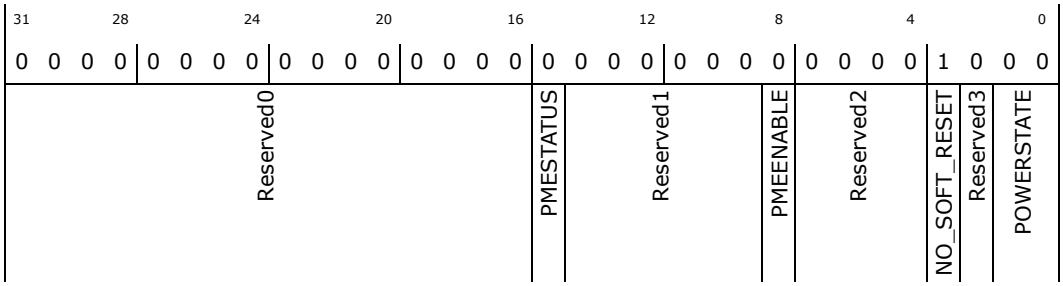
3.40.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:24, F:5] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

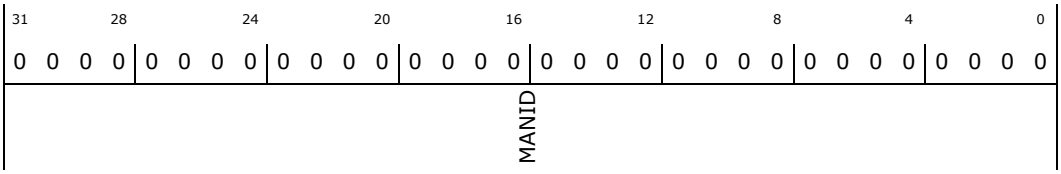
3.40.13 Manufacturer ID (MANID)—Offset F8h

Access Method

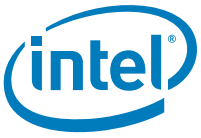
Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:24, F:5] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.



3.41 SIO I2C4 Memory Mapped IO Registers

Table 49. Summary of SIO I2C4 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 2760	0000007Fh
4h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 2761	00001055h
8h	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 2762	00000055h
Ch	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 2763	00000001h
10h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 2764	00000000h
14h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 2765	00000190h
18h	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 2766	000001D6h
1Ch	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 2766	0000003Ch
20h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 2767	00000082h
24h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 2768	0000000Ch
28h	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 2769	00000020h
2Ch	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 2770	00000000h
30h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 2771	000008FFh
34h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 2772	00000000h
38h	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 2774	00000010h
3Ch	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 2774	00000010h
40h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 2775	00000000h
44h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 2775	00000000h
48h	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 2776	00000000h
4Ch	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 2776	00000000h
50h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 2777	00000000h

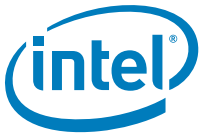


Table 49. Summary of SIO I²C4 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
54h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 2778	00000000h
58h	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 2778	00000000h
5Ch	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 2779	00000000h
60h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 2779	00000000h
64h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 2780	00000000h
68h	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 2780	00000000h
6Ch	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 2781	00000000h
70h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 2782	00000006h
74h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 2783	00000000h
78h	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 2784	00000000h
7Ch	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 2784	00000001h
80h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 2785	00000000h
84h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 2787	00000000h
88h	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 2788	00000000h
8Ch	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 2789	00000000h
90h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 2789	00000000h
94h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 2790	00000064h
98h	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 2791	00000001h
9Ch	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 2792	00000000h
A0h	4	"IC_FS_SPKLEN—Offset A0h" on page 2793	00000005h
A4h	4	"IC_HS_SPKLEN—Offset A4h" on page 2793	00000002h
F4h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 2794	00FFFFEEh
F8h	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 2795	3131352Ah
FCh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 2796	44570140h
800h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 2796	00000000h

Table 49. Summary of SIO I²C4 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
804h	4	"Software Reset (RESETS)—Offset 804h" on page 2797	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 2798	55000000h
818h	4	"I2C_ACK_COUNT—Offset 818h" on page 2799	00000000h
820h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 2800	00000000h
824h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 2800	00000000h

3.41.1 I2C Control Register (IC_CON)—Offset 0h

If configuration parameter I2C_DYNAMIC_TAR_UPDATE = 0, all bits are Read/Write.

If I2C_DYNAMIC_TAR_UPDATE = 1, bit 4 is Read-only.

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

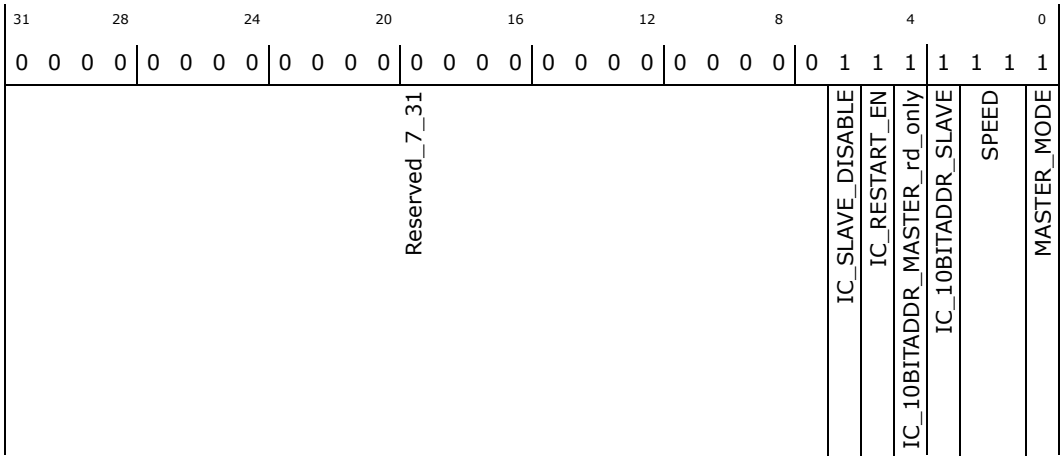
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CON: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

3.41.2 I2C Target Address Register (IC_TAR)—Offset 4h

If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to No (0), this register is 12 bits wide, and bits 15:12 are reserved. Writes to this register succeed only when IC_ENABLE is set to 0.

However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND

- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

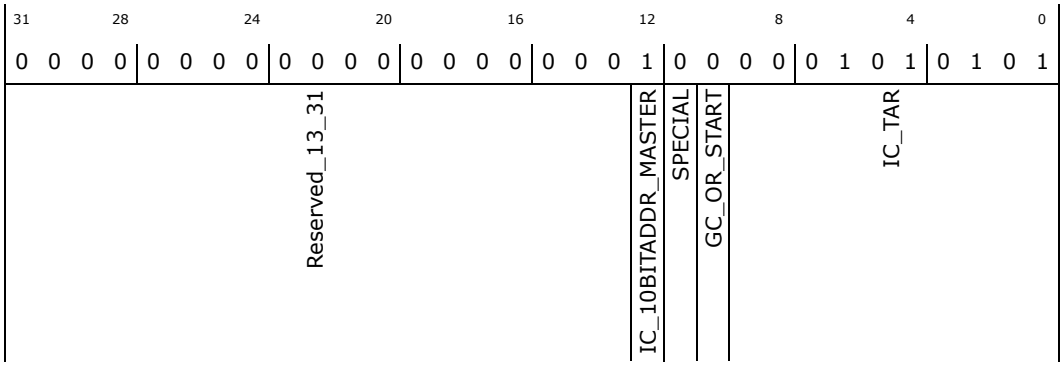
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TAR: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00001055h



Bit Range	Default & Access	Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

3.41.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

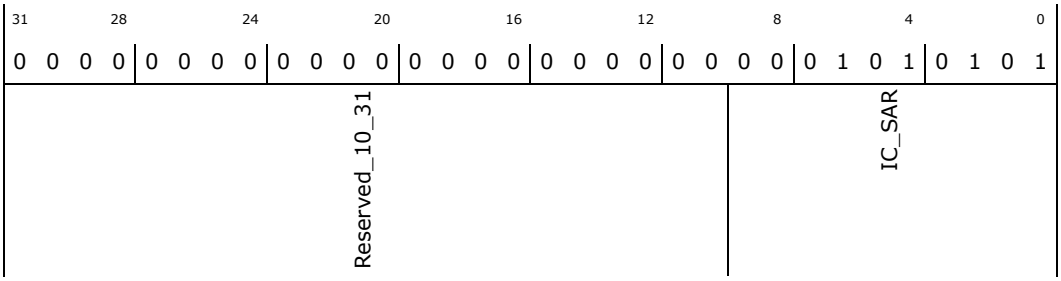
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SAR: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000055h



Bit Range	Default & Access	Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.41.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

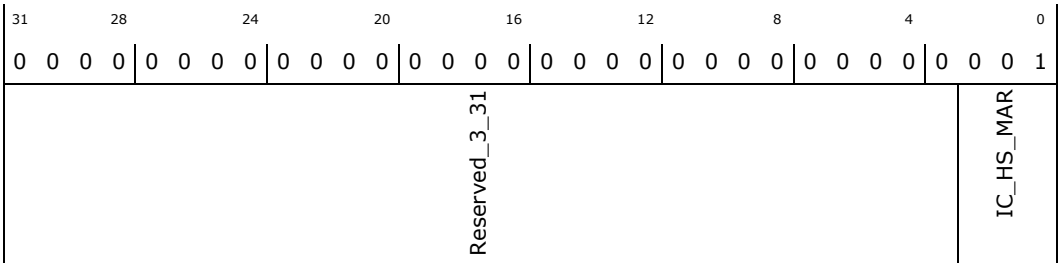
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_MADDR: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highs peed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.41.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

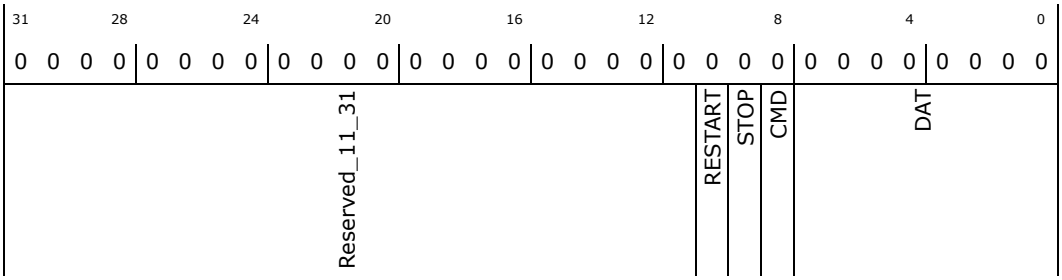
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DATA_CMD: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:11	0b RW	**Reserved_11_31:** Reserved.

Bit Range	Default & Access	Description
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/ received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

3.41.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

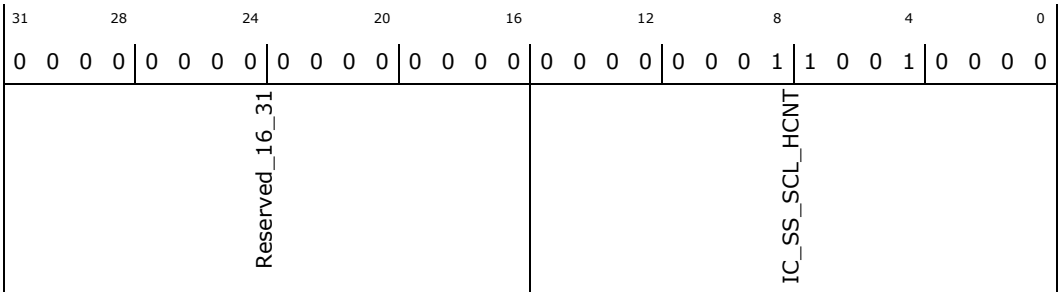
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_HCNT: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000190h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.41.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

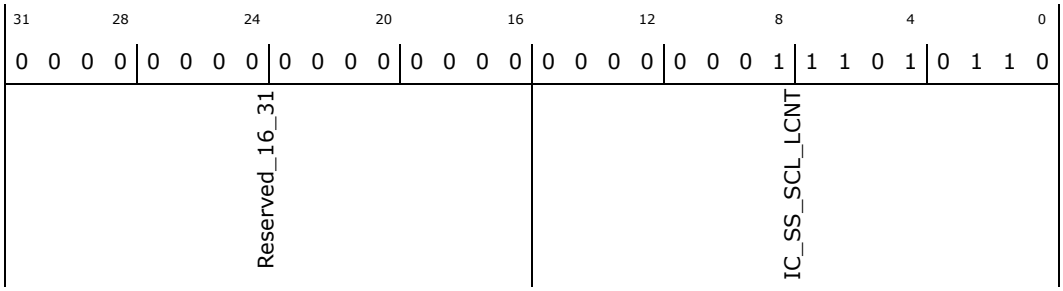
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_LCNT: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 000001D6h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.41.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

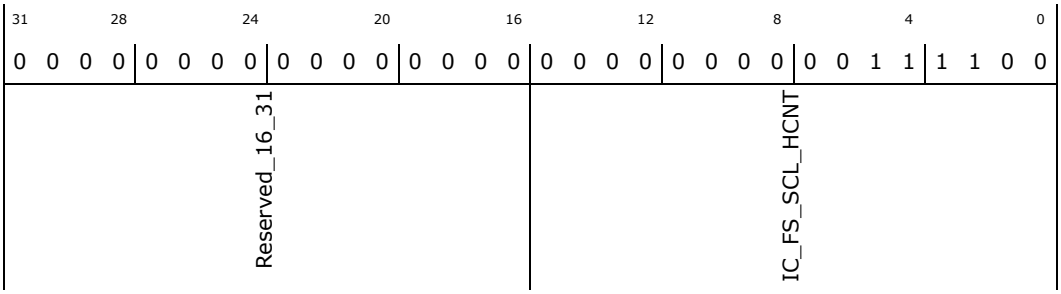
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_HCNT: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.41.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to 'IC_CLK Frequency Configuration' in the Synopsis DesignWare DW_apb_i2c Databook.

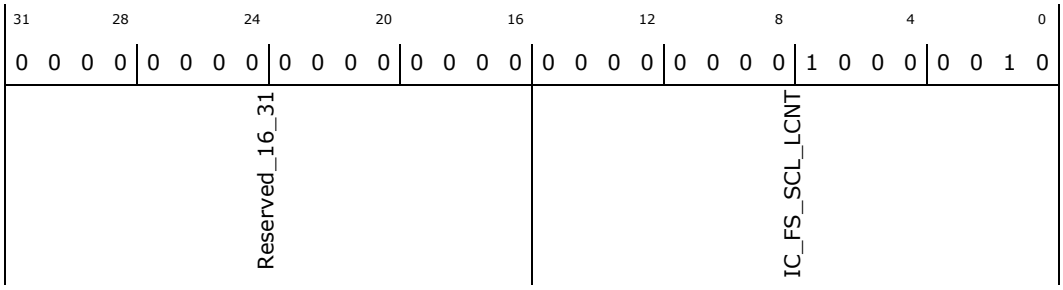
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_LCNT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000082h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.41.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* .

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

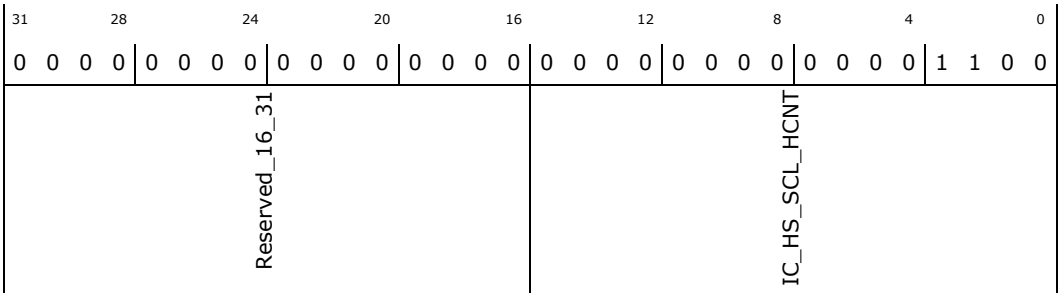
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_HCNT: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.41.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* in the Synopsis DesignWare DW_apb_i2c Databook.

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

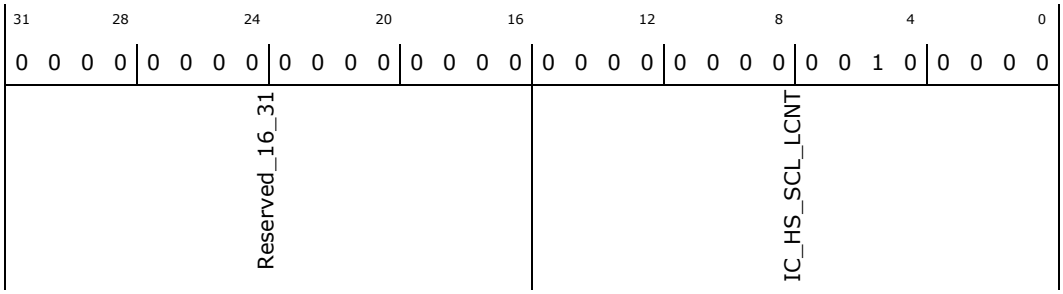
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_LCNT: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000020h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.41.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

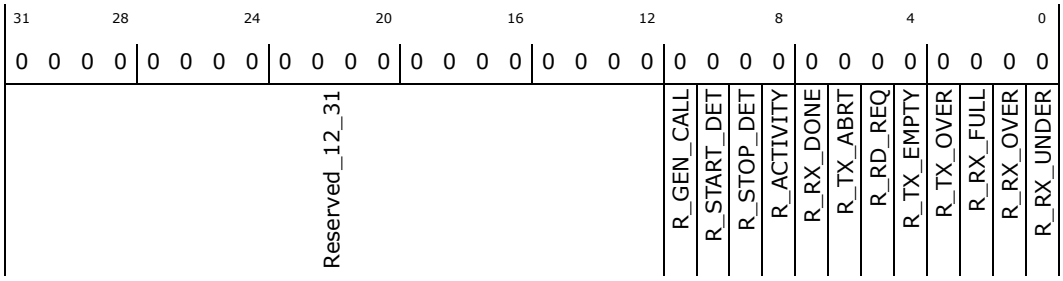
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

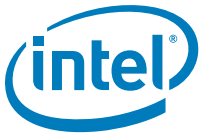
IC_INTR_STAT: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.



Bit Range	Default & Access	Description
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

3.41.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

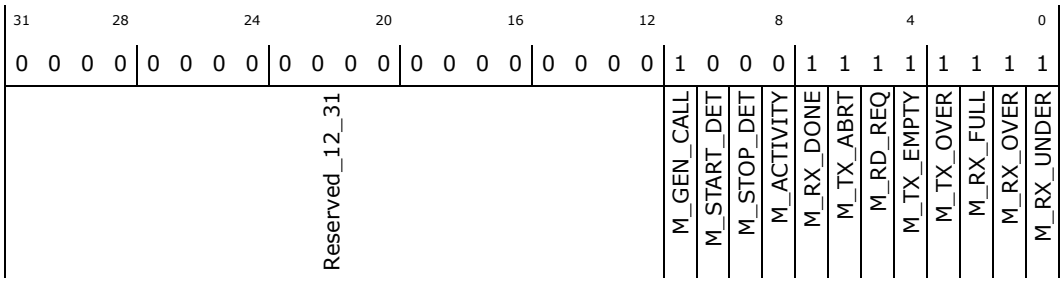
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_INTR_MASK: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 000008FFh



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

3.41.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

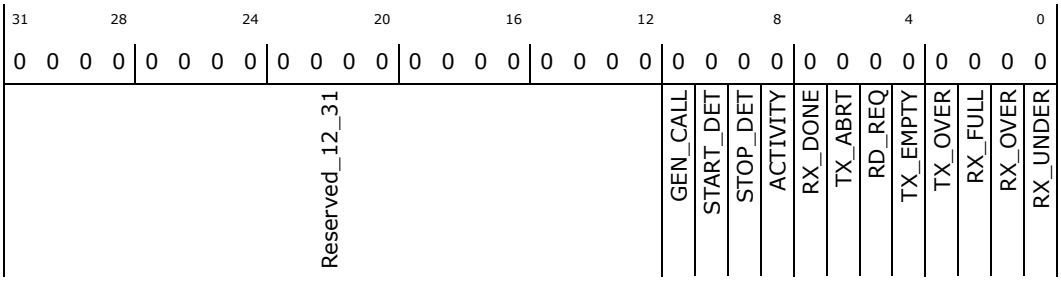
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RAW_INTR_STAT: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

3.41.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

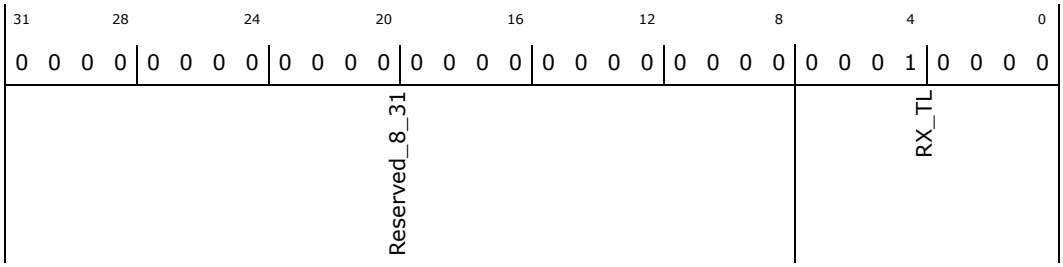
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RX_TL: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.41.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

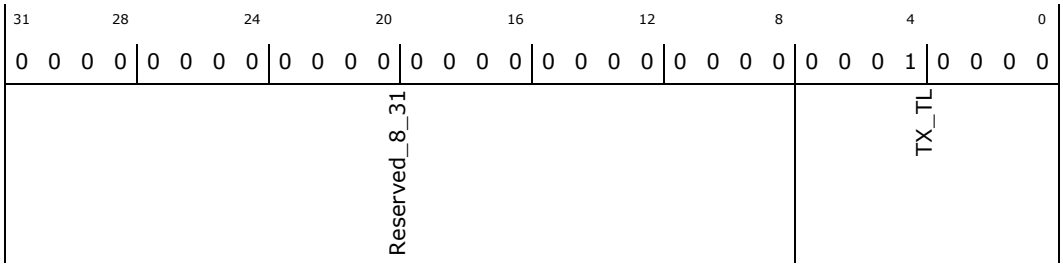
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_TL: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.41.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

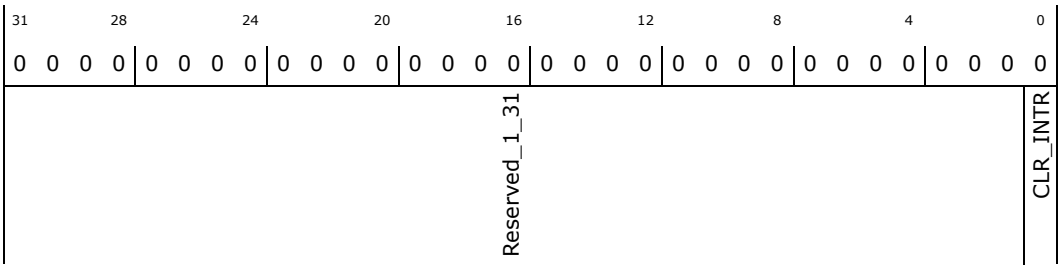
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_INTR: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

3.41.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

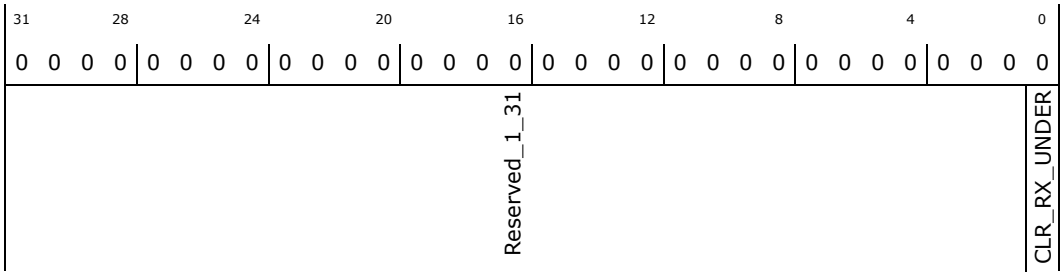
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_UNDER: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

3.41.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

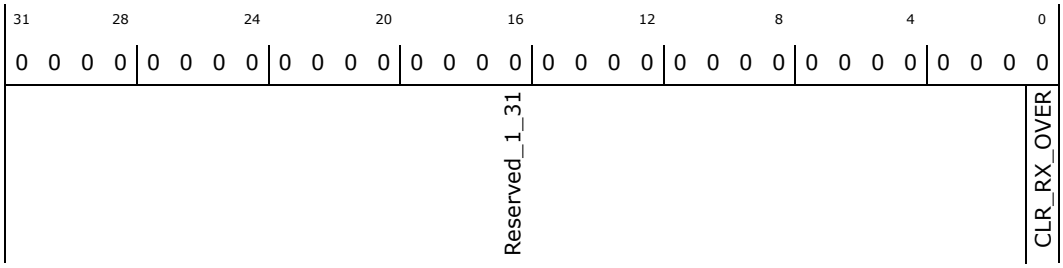
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_OVER: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

3.41.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

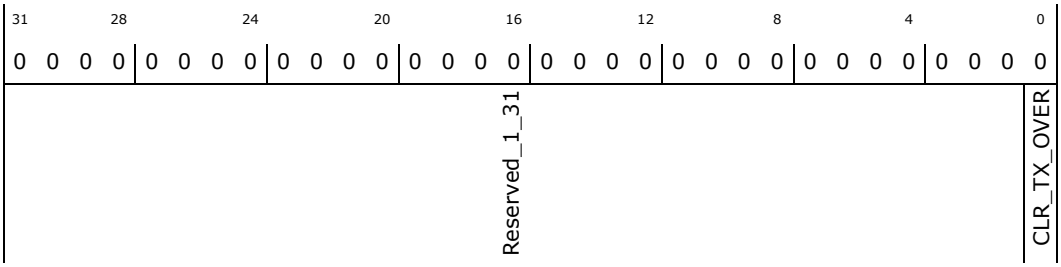
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_OVER: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

3.41.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

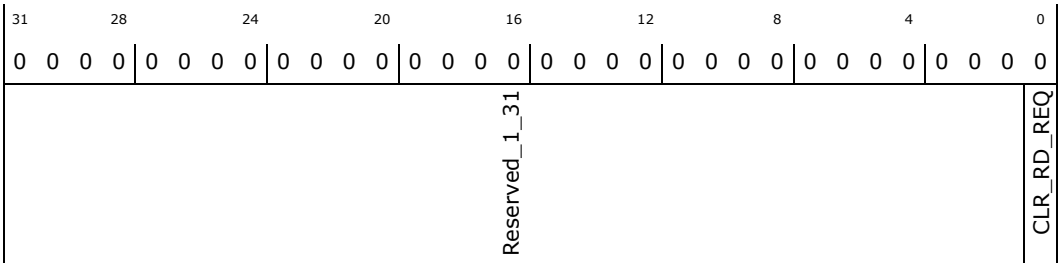
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RD_REQ: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

3.41.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

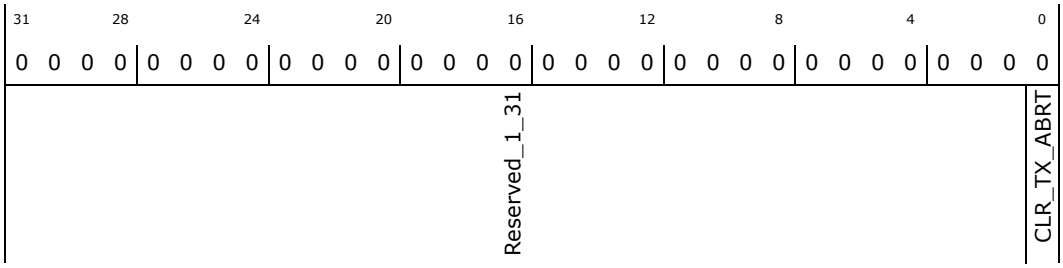
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_ABRT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

3.41.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

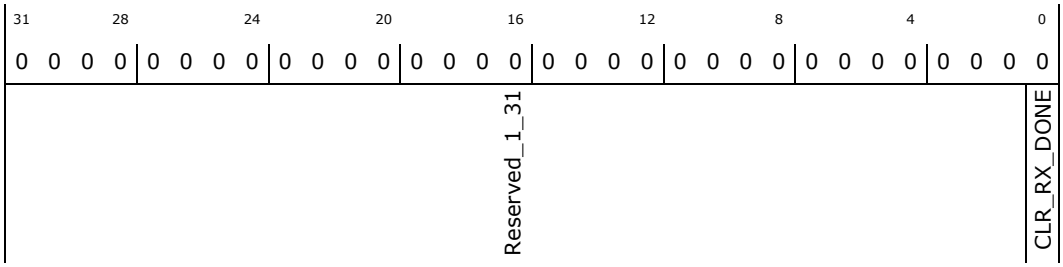
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_DONE: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

3.41.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

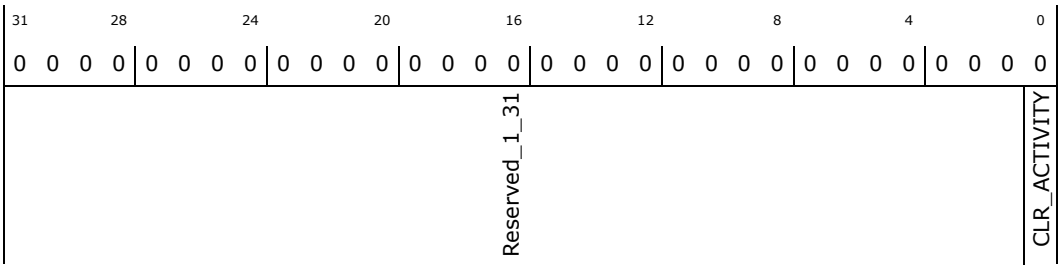
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_ACTIVITY: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

3.41.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

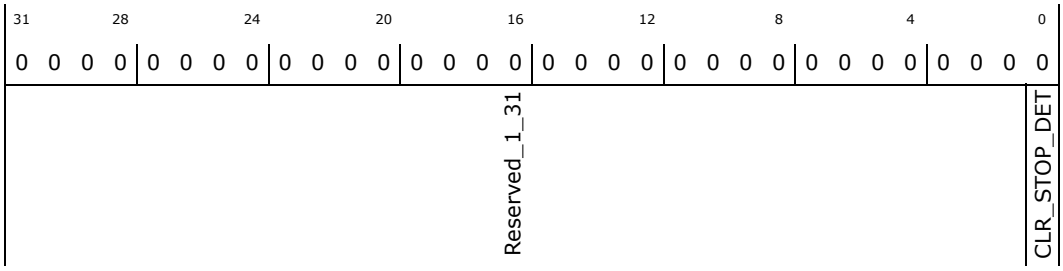
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_STOP_DET: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

3.41.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

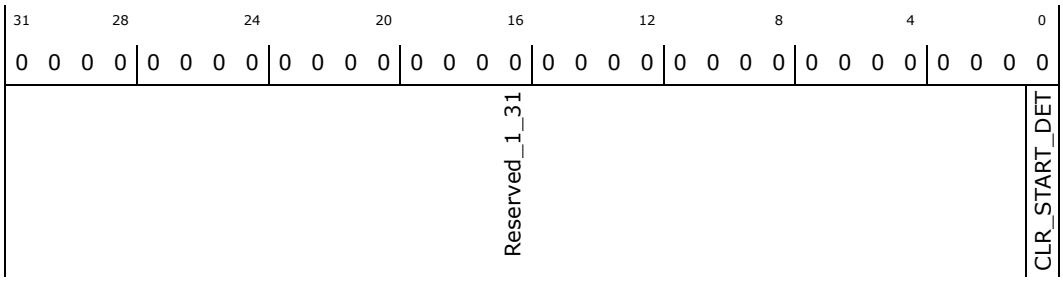
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_START_DET: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

3.41.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

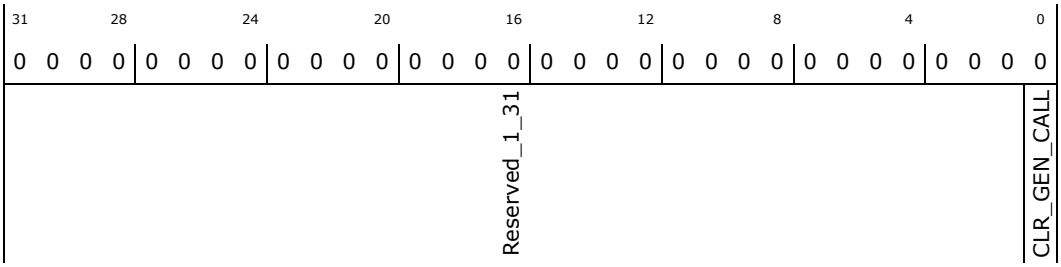
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_GEN_CALL: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

3.41.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

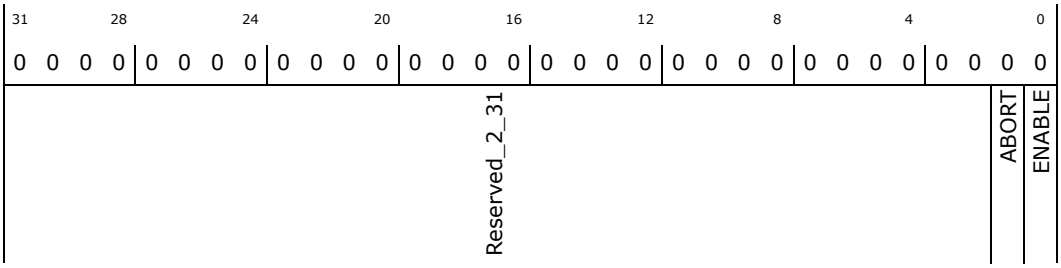
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.

Bit Range	Default & Access	Description
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

3.41.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

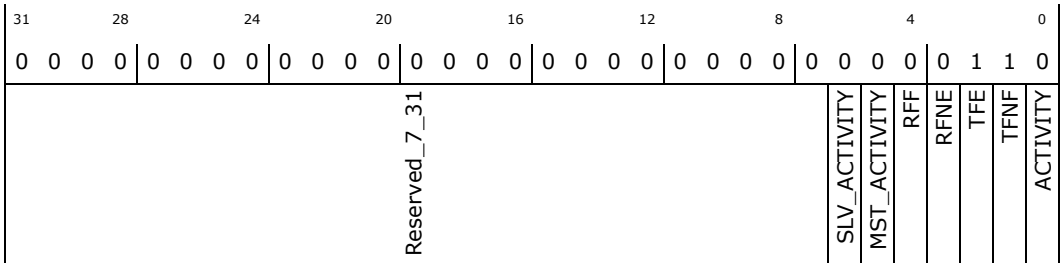
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_STATUS: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.

Bit Range	Default & Access	Description
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

3.41.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

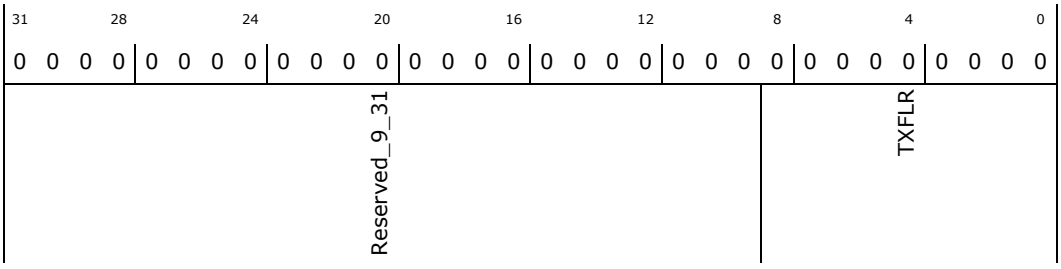
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TXFLR: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

3.41.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

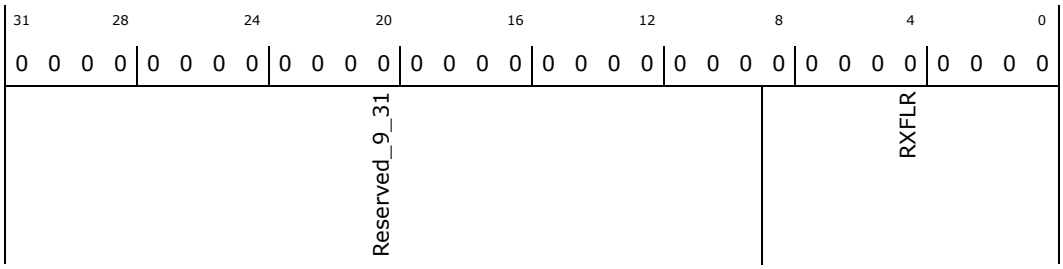
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RXFLR: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

3.41.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implemented one cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

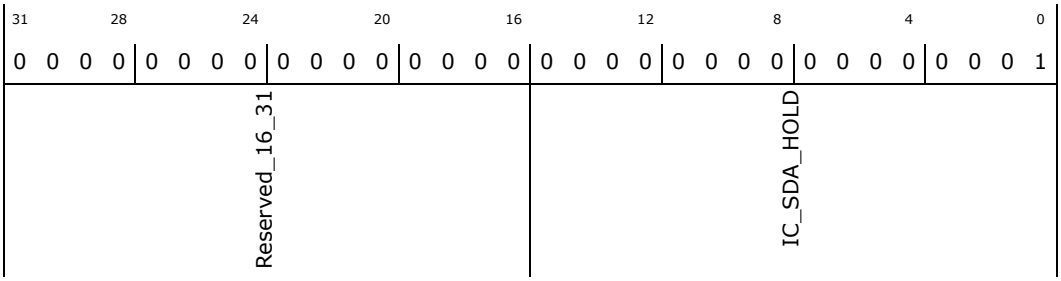
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_HOLD: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

3.41.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

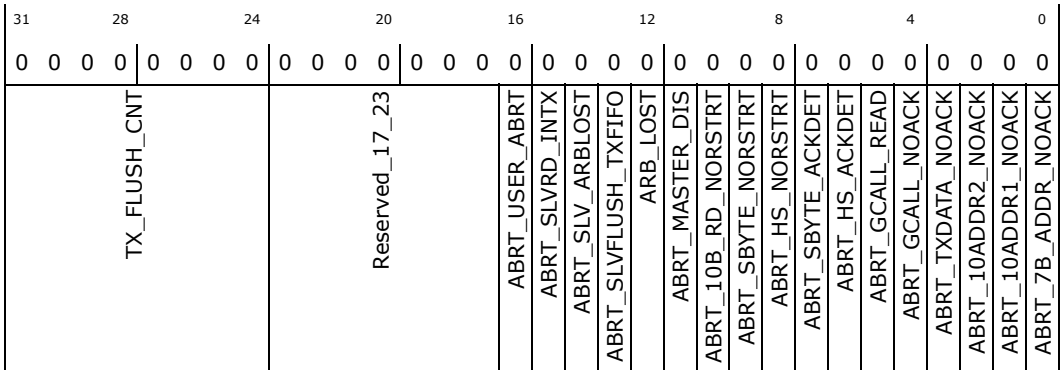
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_ABRT_SOURCE: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).

Bit Range	Default & Access	Description
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

3.41.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. This register only exists when the IC_SLV_DATA_NACK_ONLY parameter is set to 1. When this parameter disabled, this register does not exist and writing to the registers address has no effect. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

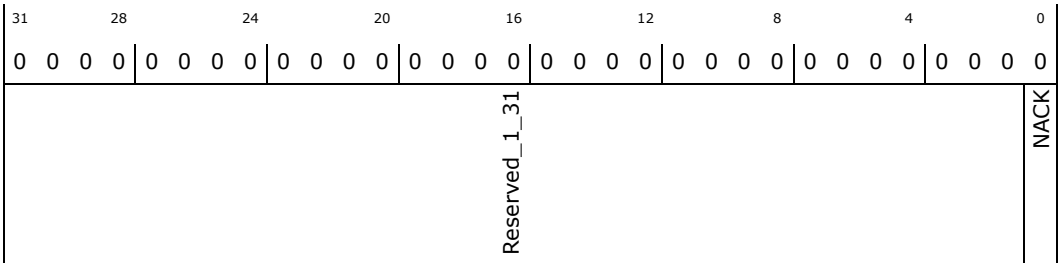
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SLV_DATA_NACK_ONLY: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slave receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

3.41.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

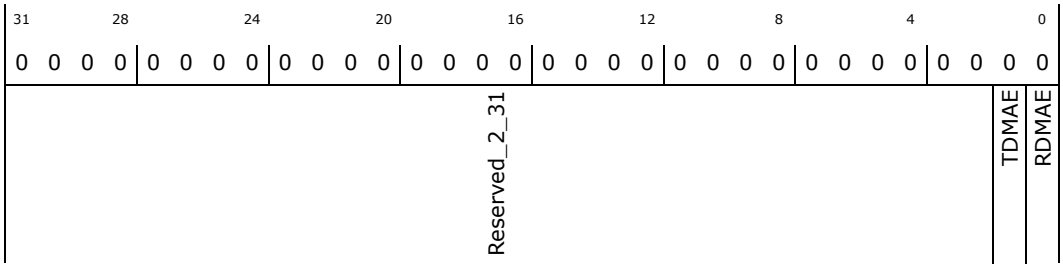
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_CR: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled

Bit Range	Default & Access	Description
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

3.41.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

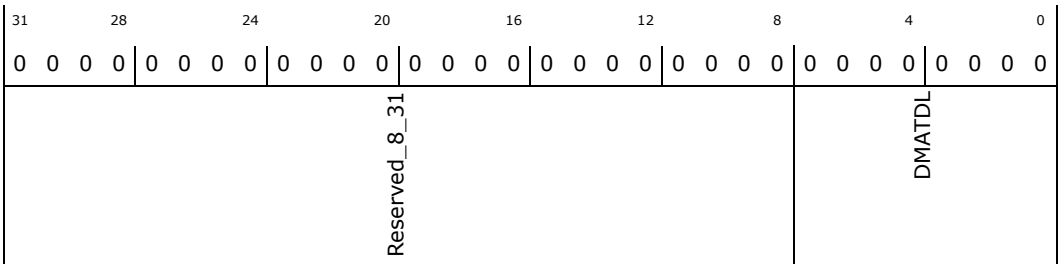
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_TDLR: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

3.41.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

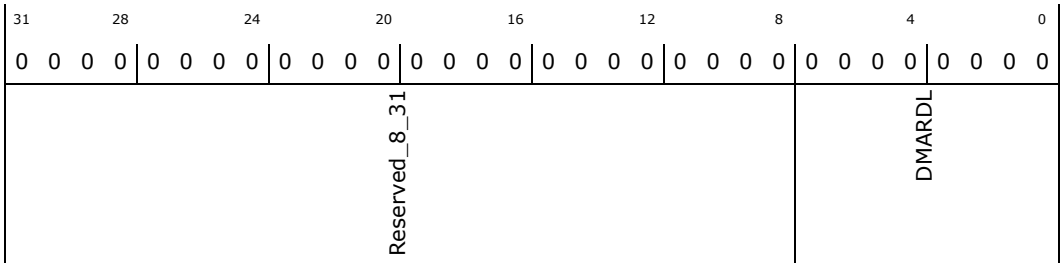
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_RDLR: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

3.41.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2.

NOTE: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

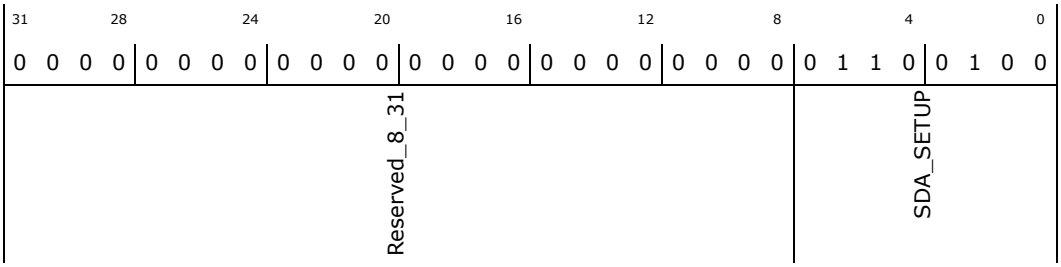
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_SETUP: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000064h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

3.41.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

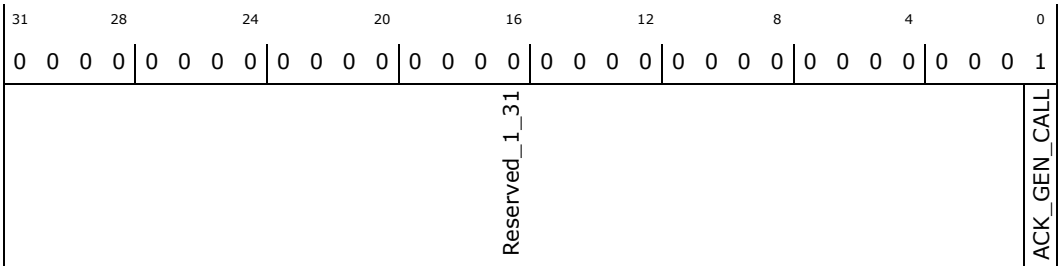
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ACK_GENERAL_CALL: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

3.41.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

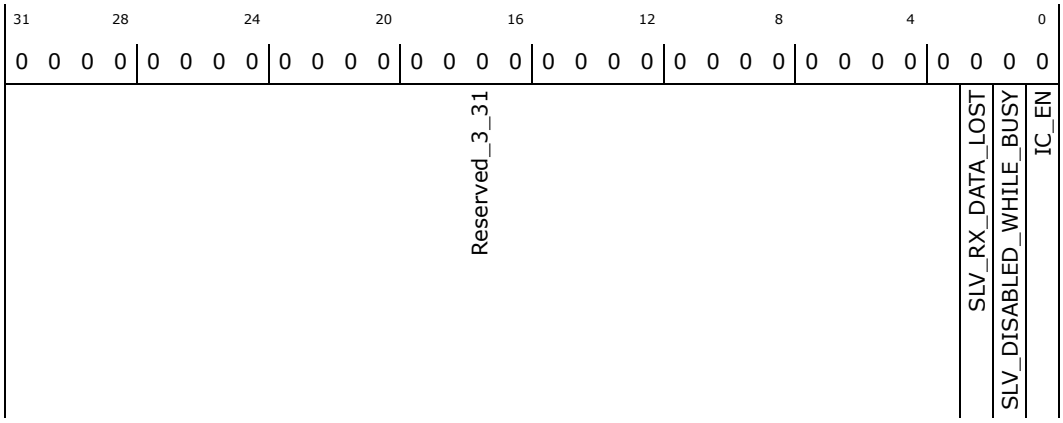
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE_STATUS: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

3.41.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

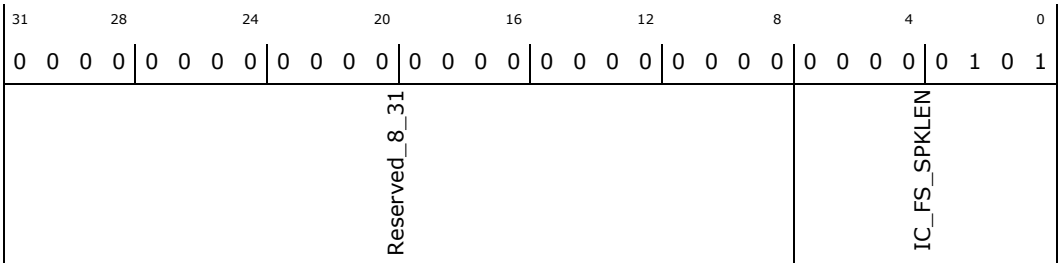
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SPKLEN: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000005h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. **Reset value:** IC_DEFAULT_FS_SPKLEN configuration parameter

3.41.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the

I2C Bus Specification. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

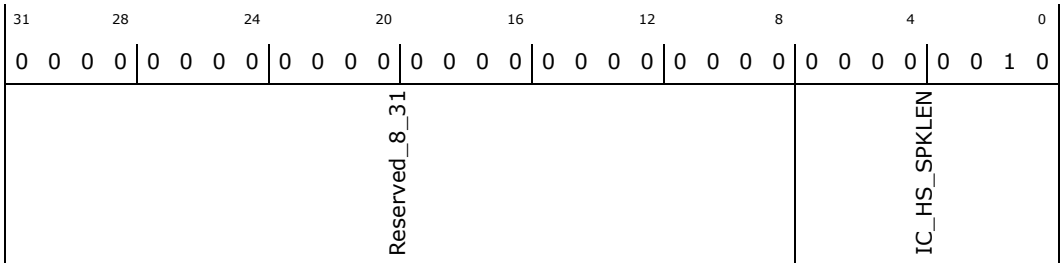
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SPKLEN: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. This register is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3. **Reset value:** IC_DEFAULT_HS_SPKLEN configuration parameter.

3.41.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

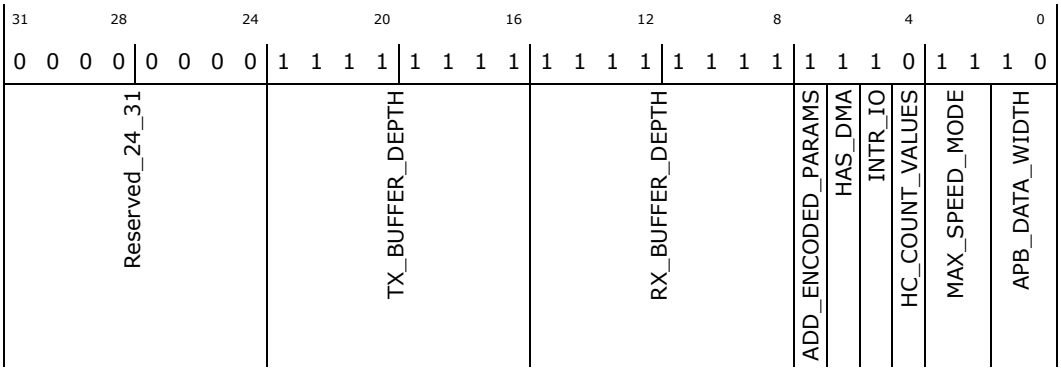
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_PARAM_1: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

3.41.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

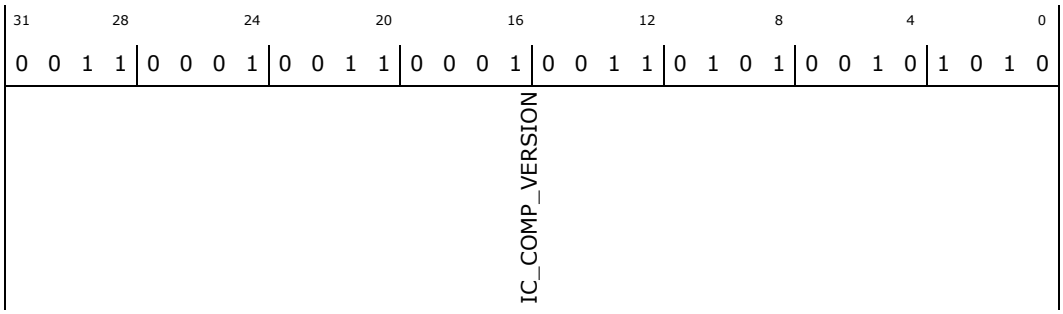
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_VERSION: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

3.41.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

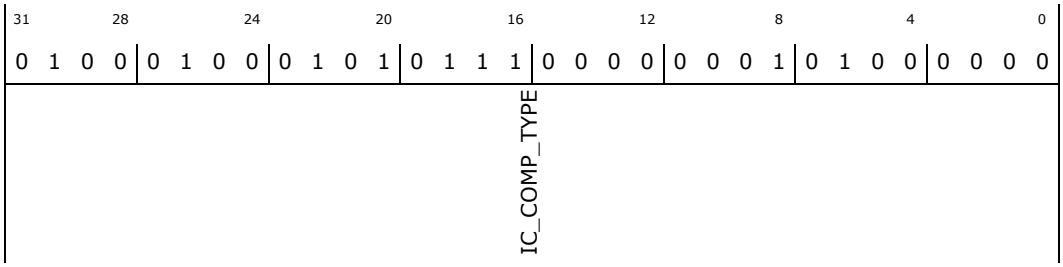
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_TYPE: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 44570140h



Bit Range	Default & Access	Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

3.41.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

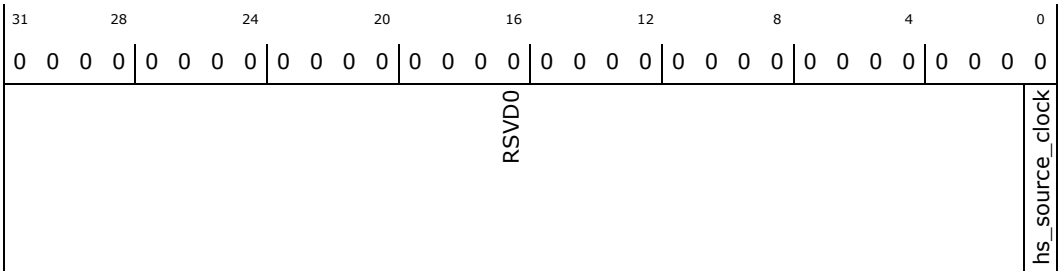
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CLOCK_PARAMS: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

3.41.47 Software Reset (RESETS)—Offset 804h

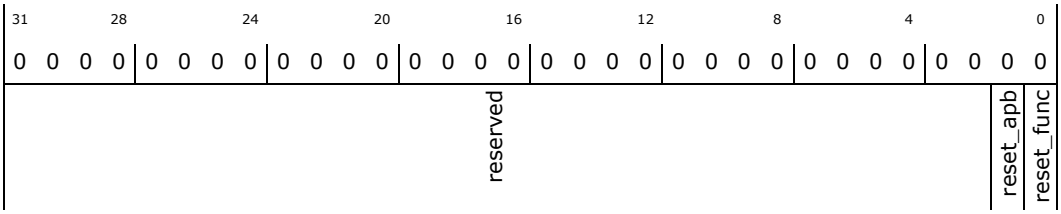
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.41.48 General Purpose Register (GENERAL)—Offset 808h

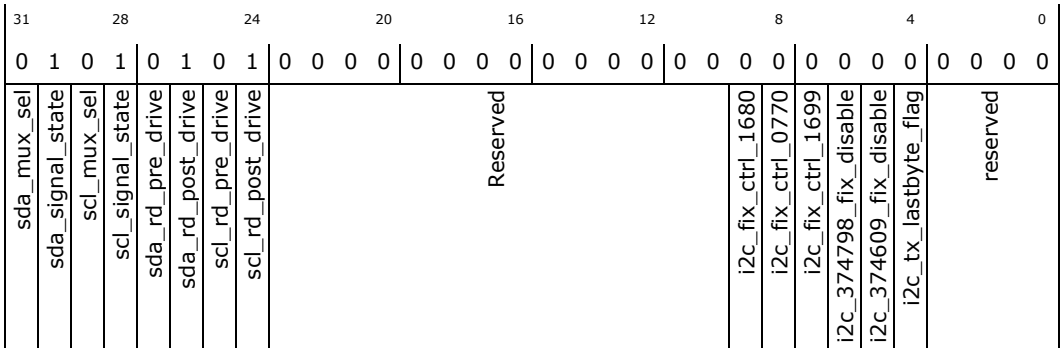
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 55000000h



Bit Range	Default & Access	Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)

Bit Range	Default & Access	Description
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

3.41.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

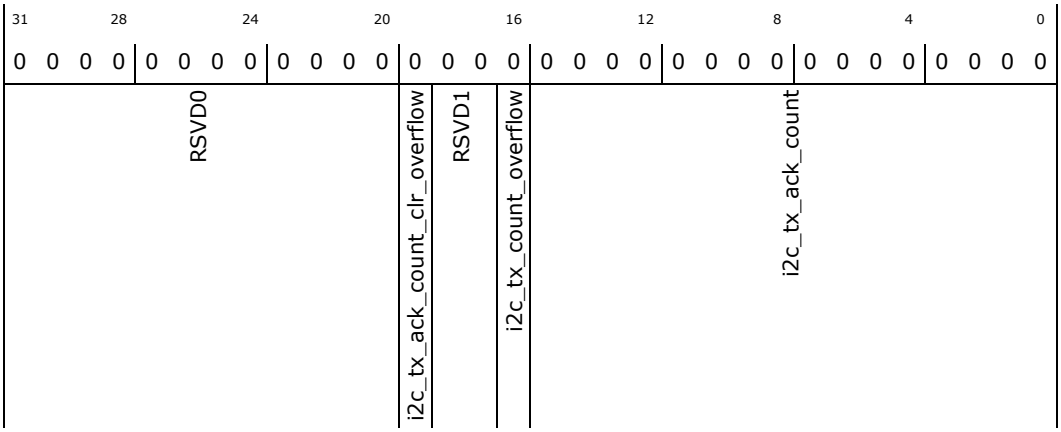
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_ACK_COUNT: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

3.41.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

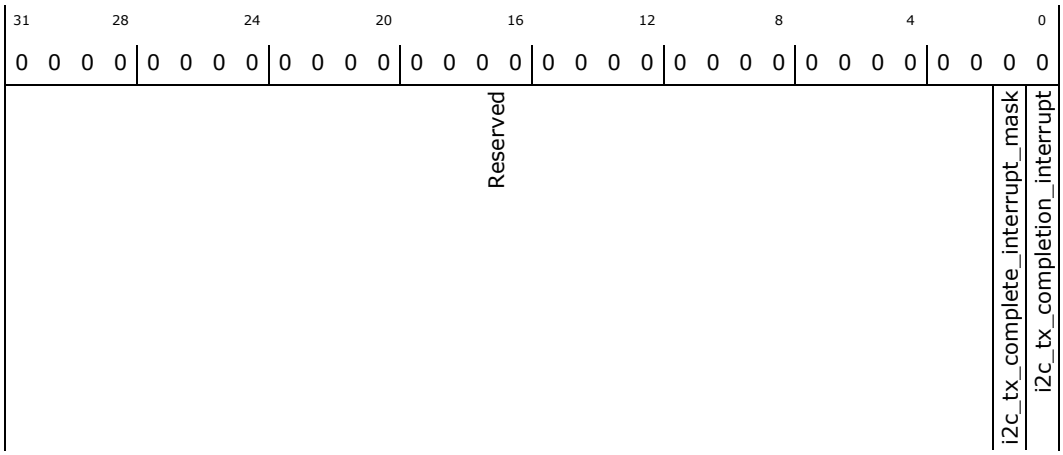
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_TX_COMPLETE_INTR_STAT: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

3.41.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

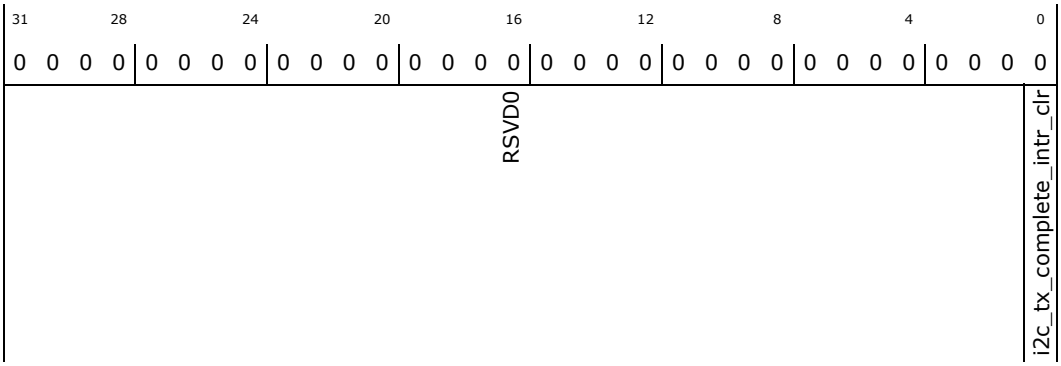
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_TX_COMPLETE_INTR_CLR: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

3.42 SIO I²C5 PCI Configuration Registers

Table 50. Summary of SIO I²C5 PCI Configuration Registers—0/24/6

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2802	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2803	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2804	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2805	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2806	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2806	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2807	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2808	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2808	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2809	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2809	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2810	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2811	00000000h

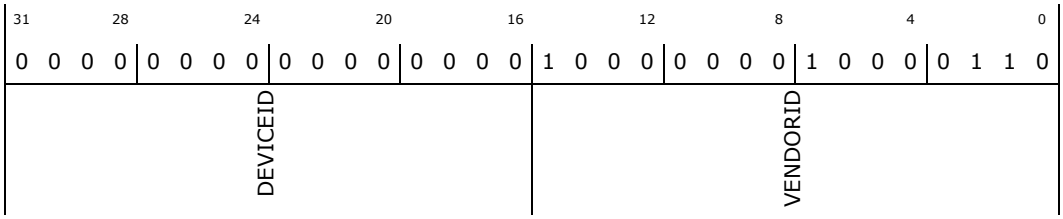
3.42.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:24, F:6] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

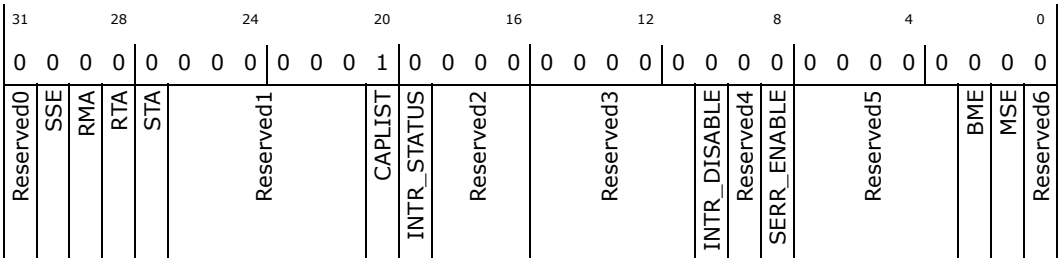
3.42.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:24, F:6] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

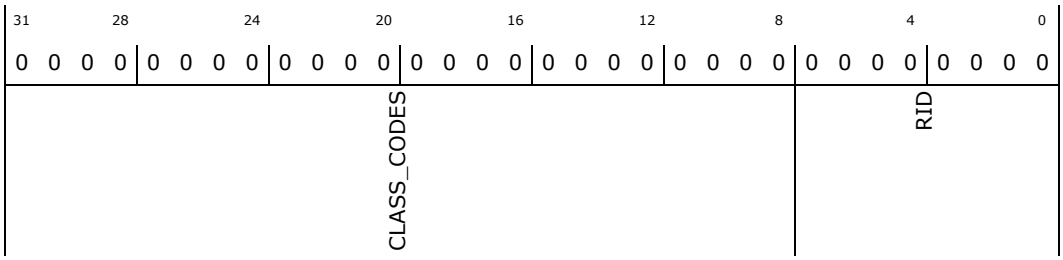
3.42.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:24, F:6] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

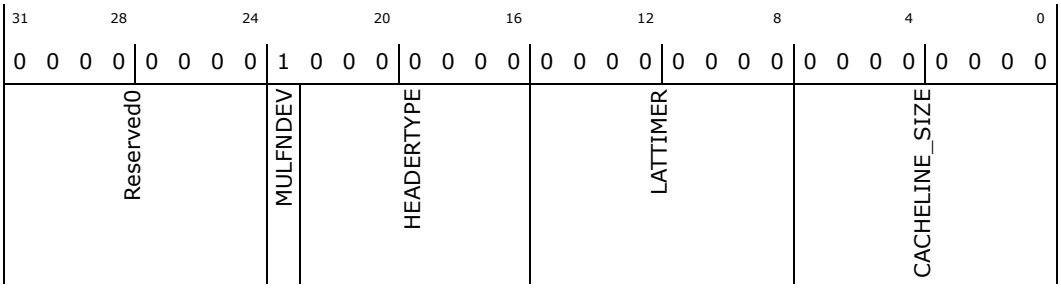
3.42.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:24, F:6] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

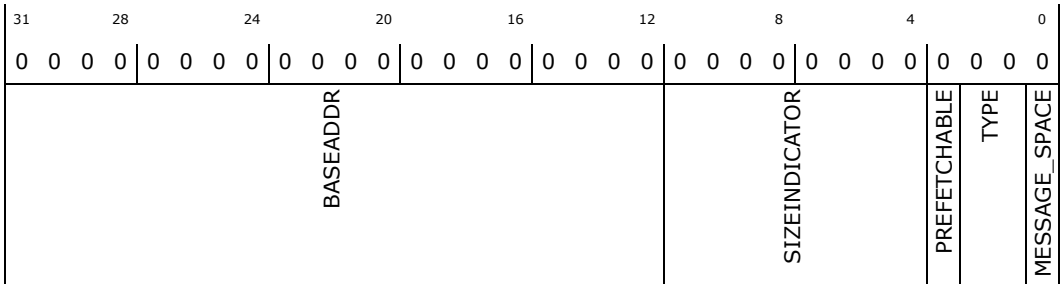
3.42.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

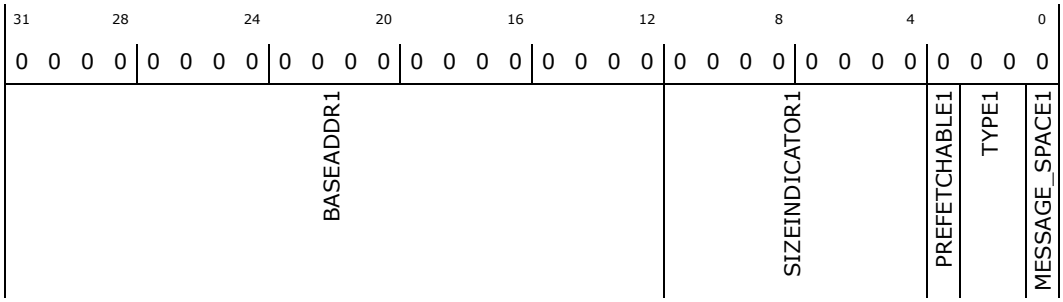
3.42.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:24, F:6] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

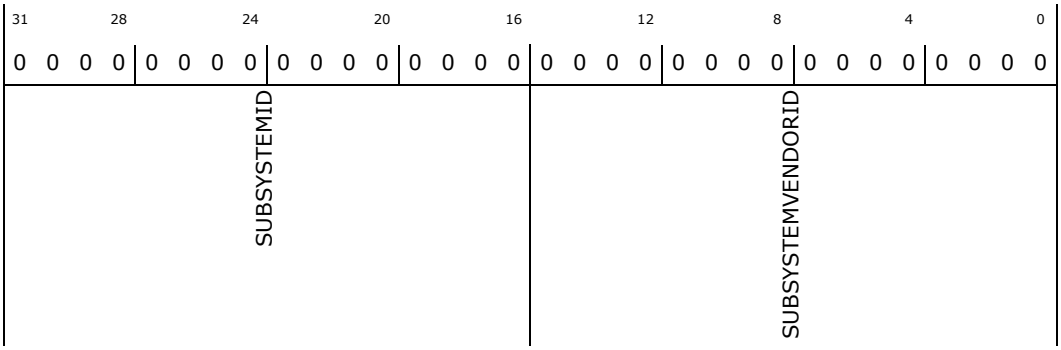
3.42.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:24, F:6] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

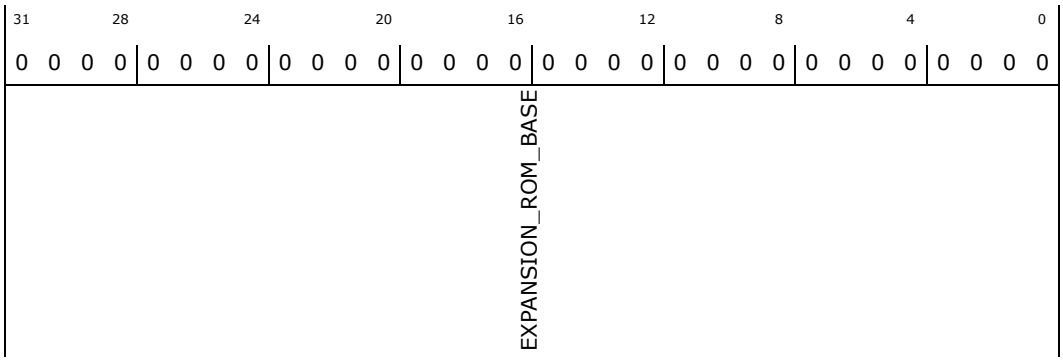
3.42.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:24, F:6] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

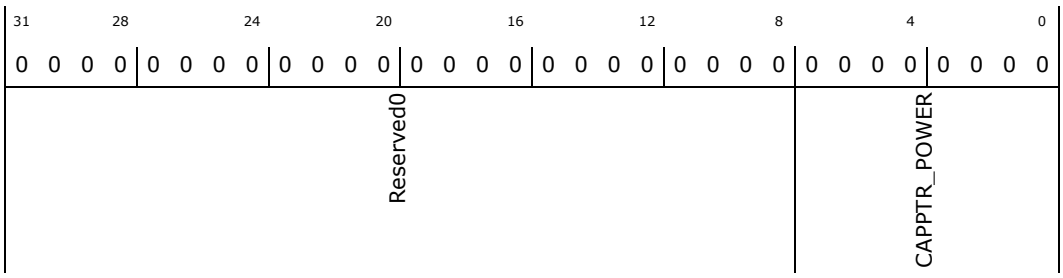
3.42.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:24, F:6] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

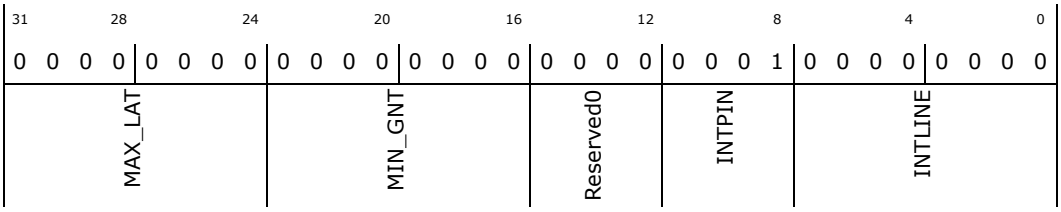
3.42.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

INTERRUPTREG: [B:0, D:24, F:6] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

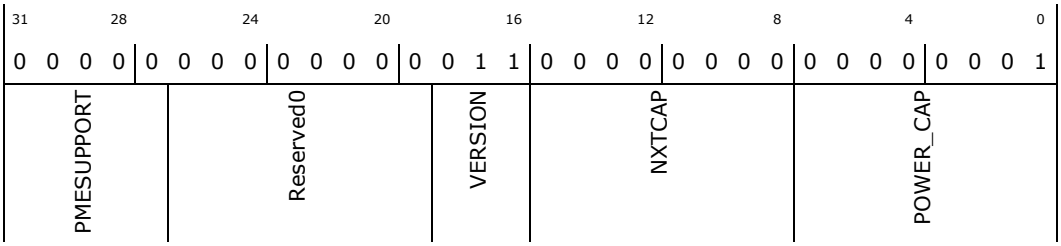
3.42.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

POWERCAPID: [B:0, D:24, F:6] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

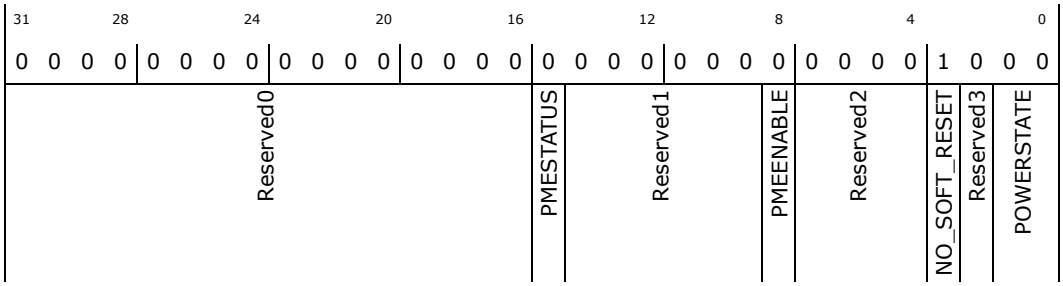
3.42.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:24, F:6] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

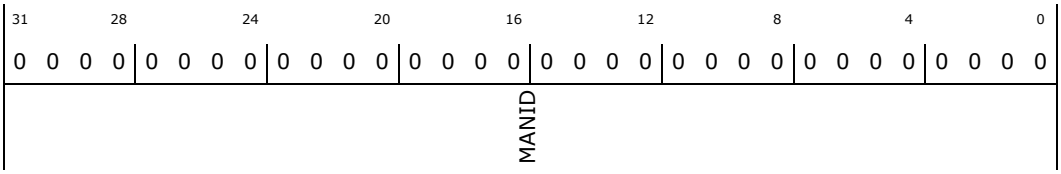
3.42.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:24, F:6] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

3.43 SIO I²C5 Memory Mapped IO Registers

Table 51. Summary of SIO I²C5 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 2814	0000007Fh
4h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 2815	00001055h
8h	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 2816	00000055h
Ch	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 2817	00000001h
10h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 2818	00000000h
14h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 2819	00000190h
18h	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 2820	000001D6h
1Ch	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 2820	0000003Ch
20h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 2821	00000082h
24h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 2822	0000000Ch
28h	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 2823	00000020h
2Ch	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 2824	00000000h
30h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 2825	000008FFh
34h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 2826	00000000h
38h	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 2828	00000010h
3Ch	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 2828	00000010h
40h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 2829	00000000h
44h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 2829	00000000h
48h	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 2830	00000000h
4Ch	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 2830	00000000h
50h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 2831	00000000h

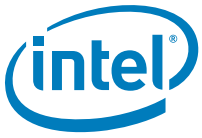


Table 51. Summary of SIO I²C5 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
54h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 2832	00000000h
58h	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 2832	00000000h
5Ch	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 2833	00000000h
60h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 2833	00000000h
64h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 2834	00000000h
68h	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 2834	00000000h
6Ch	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 2835	00000000h
70h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 2836	00000006h
74h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 2837	00000000h
78h	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 2838	00000000h
7Ch	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 2838	00000001h
80h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 2839	00000000h
84h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 2841	00000000h
88h	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 2842	00000000h
8Ch	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 2843	00000000h
90h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 2843	00000000h
94h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 2844	00000064h
98h	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 2845	00000001h
9Ch	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 2846	00000000h
A0h	4	"IC_FS_SPKLEN—Offset A0h" on page 2847	00000005h
A4h	4	"IC_HS_SPKLEN—Offset A4h" on page 2847	00000002h
F4h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 2848	00FFFFEEh
F8h	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 2849	3131352Ah
FCh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 2850	44570140h
800h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 2850	00000000h

Table 51. Summary of SIO I²C5 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
804h	4	"Software Reset (RESETS)—Offset 804h" on page 2851	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 2852	55000000h
818h	4	"I2C_ACK_COUNT—Offset 818h" on page 2853	00000000h
820h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 2854	00000000h
824h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 2854	00000000h

3.43.1 I2C Control Register (IC_CON)—Offset 0h

If configuration parameter I2C_DYNAMIC_TAR_UPDATE = 0, all bits are Read/Write.

If I2C_DYNAMIC_TAR_UPDATE = 1, bit 4 is Read-only.

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

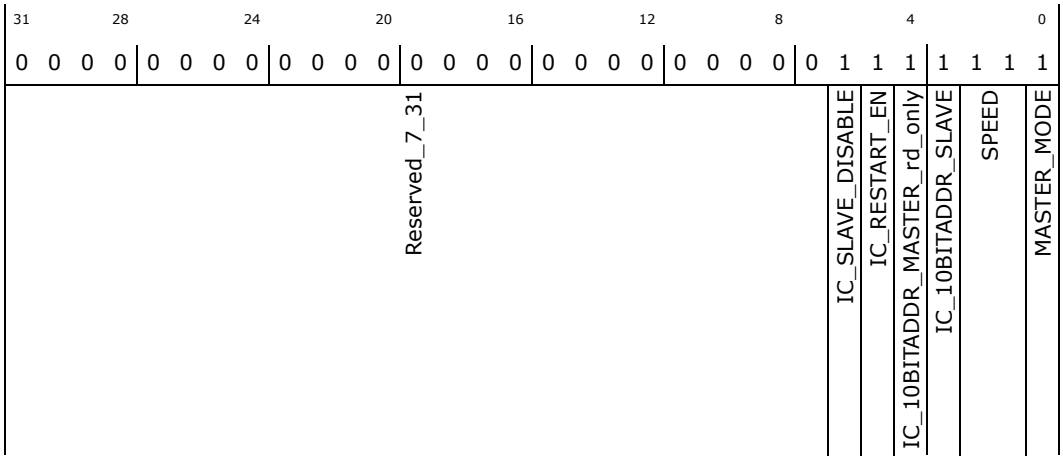
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CON: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

3.43.2 I2C Target Address Register (IC_TAR)—Offset 4h

If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to No (0), this register is 12 bits wide, and bits 15:12 are reserved. Writes to this register succeed only when IC_ENABLE is set to 0.

However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND

- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

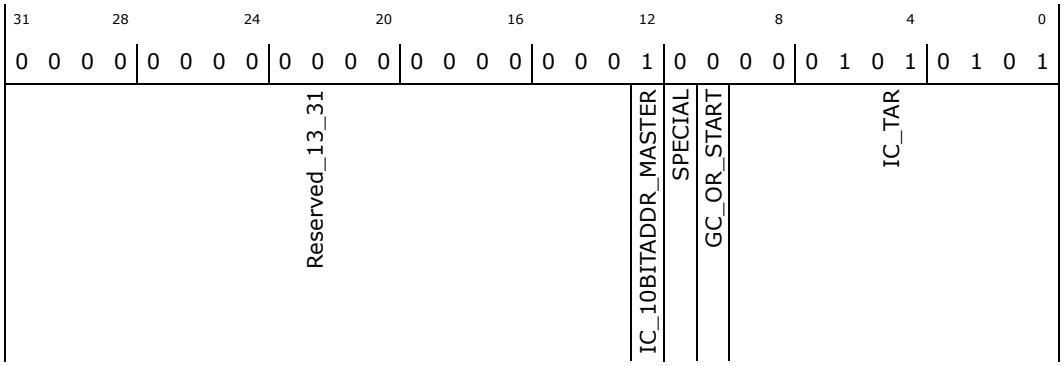
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TAR: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00001055h



Bit Range	Default & Access	Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

3.43.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

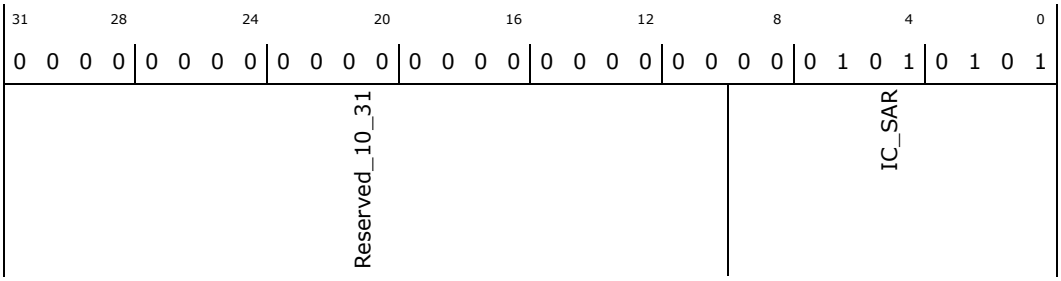
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SAR: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000055h



Bit Range	Default & Access	Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.43.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

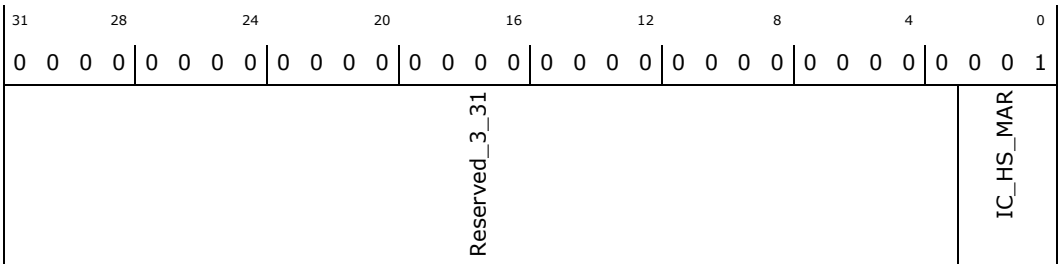
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_MADDR: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.43.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

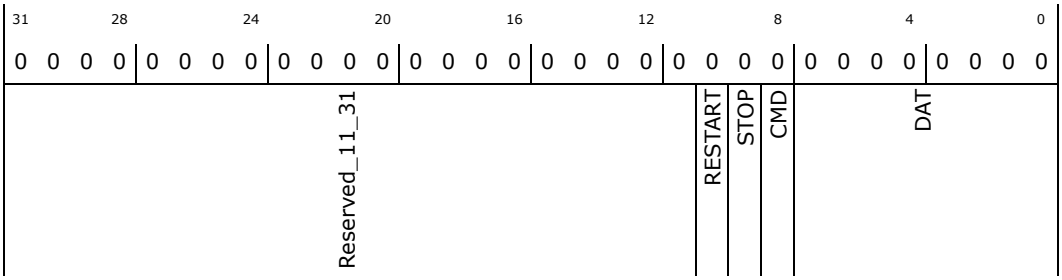
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DATA_CMD: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:11	0b RW	**Reserved_11_31:** Reserved.

Bit Range	Default & Access	Description
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/ received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

3.43.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

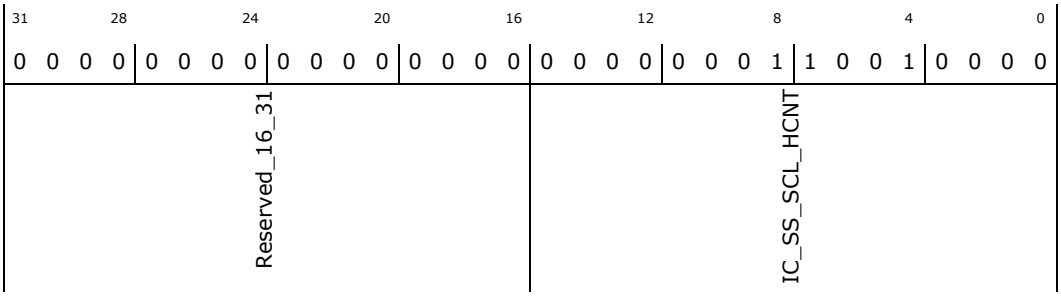
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_HCNT: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000190h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.43.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

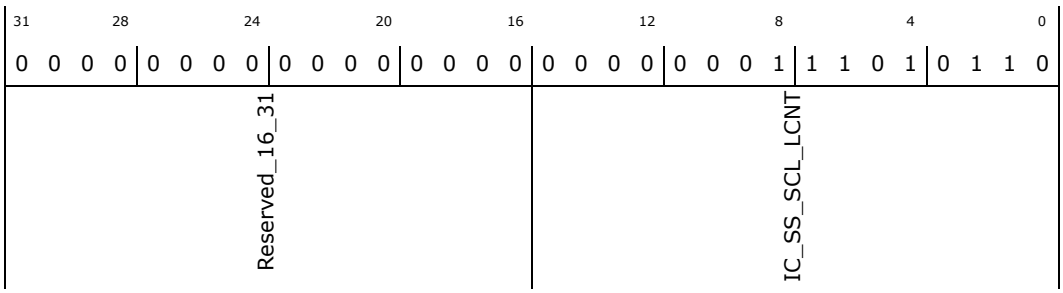
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_LCNT: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 000001D6h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.43.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

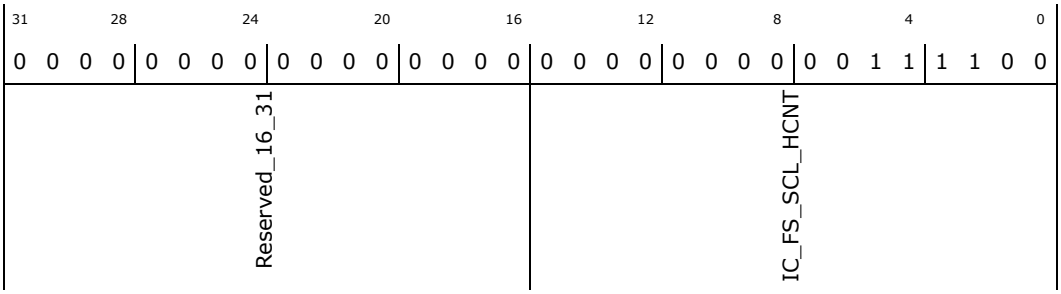
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_HCNT: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.43.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to 'IC_CLK Frequency Configuration' in the Synopsis DesignWare DW_apb_i2c Databook.

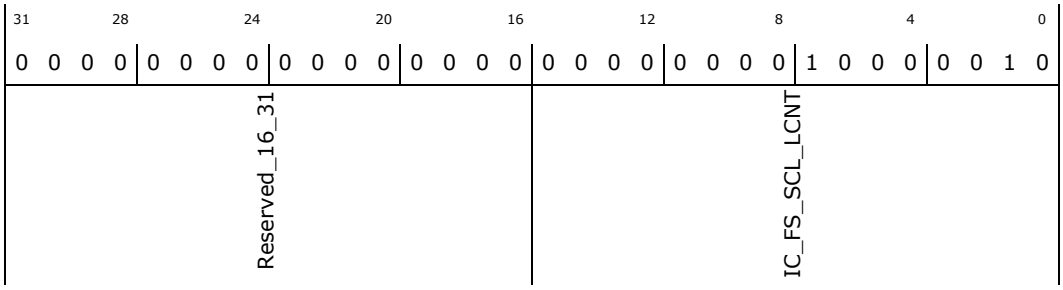
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_LCNT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000082h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.43.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* .

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

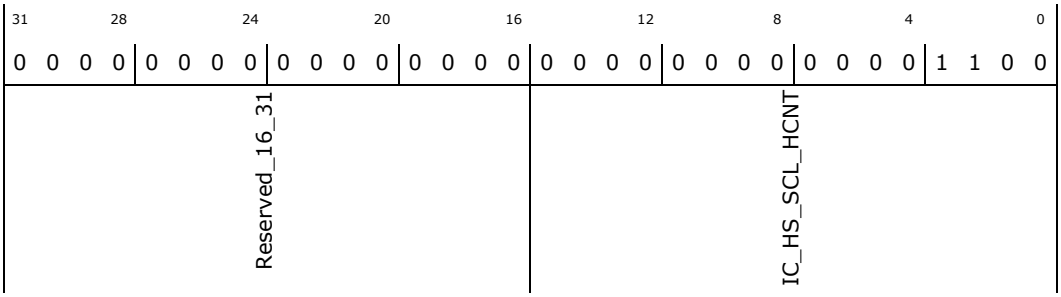
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_HCNT: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.43.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* in the Synopsis DesignWare DW_apb_i2c Databook.

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

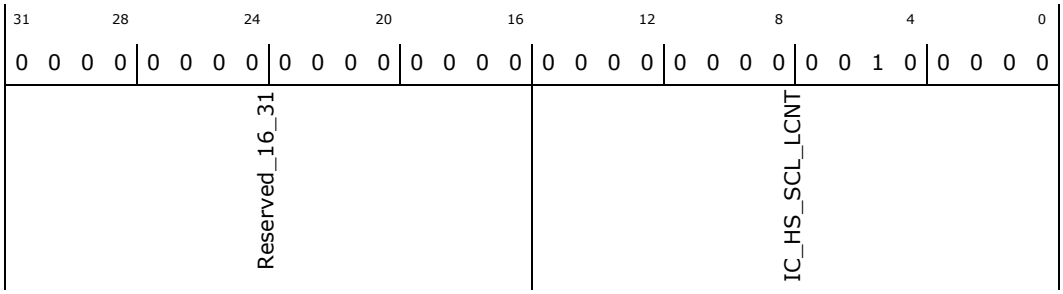
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_LCNT: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000020h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.43.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

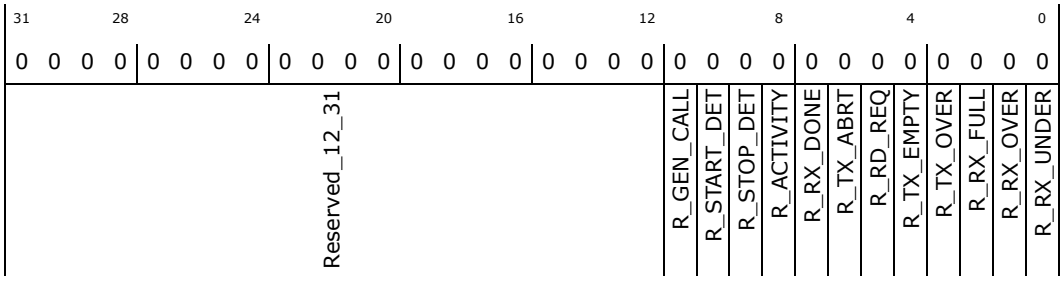
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

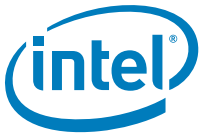
IC_INTR_STAT: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.



Bit Range	Default & Access	Description
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

3.43.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

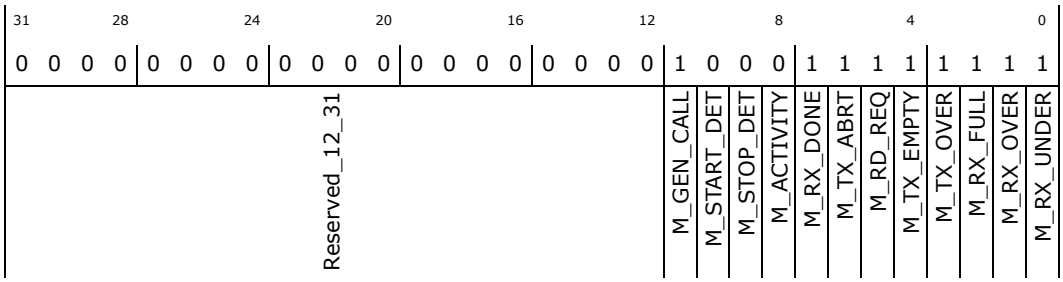
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_INTR_MASK: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 000008FFh



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

3.43.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

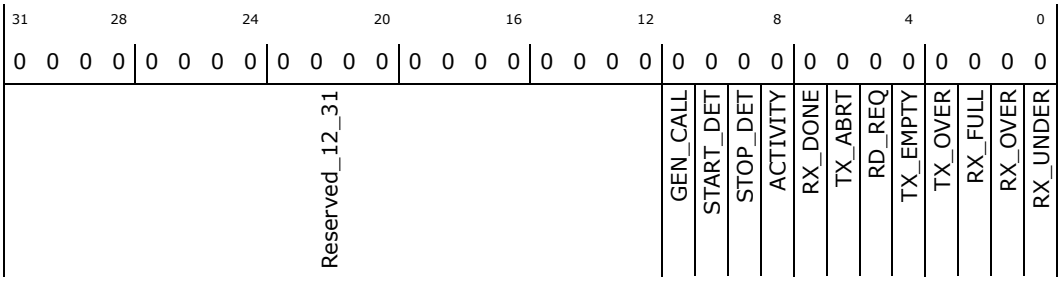
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RAW_INTR_STAT: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

3.43.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

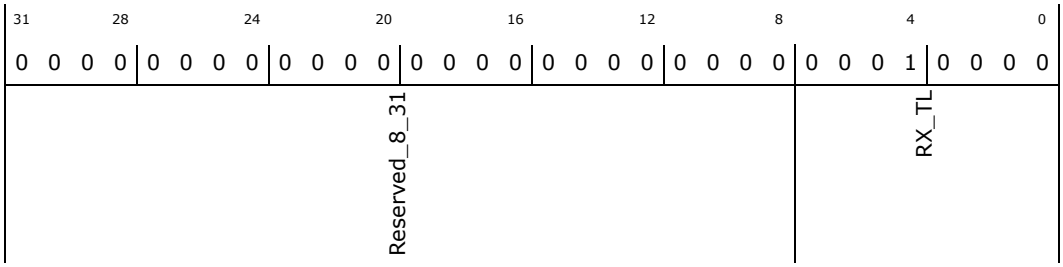
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RX_TL: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.43.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

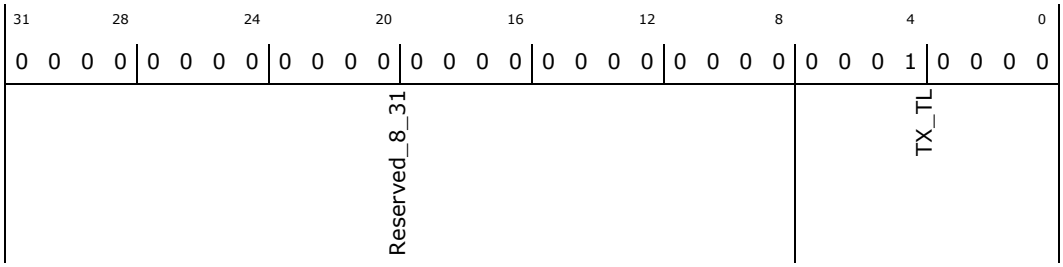
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_TL: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.43.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

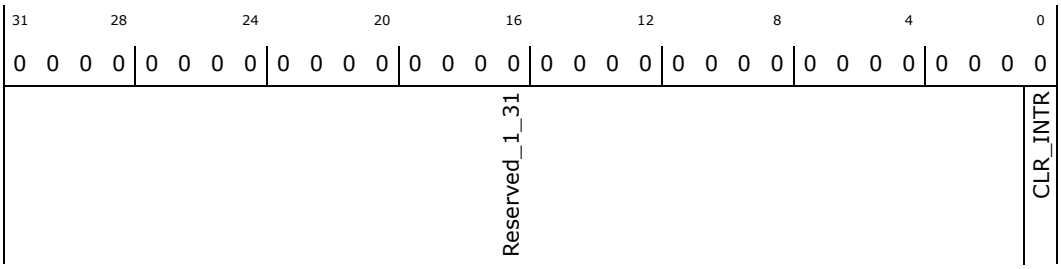
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_INTR: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

3.43.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

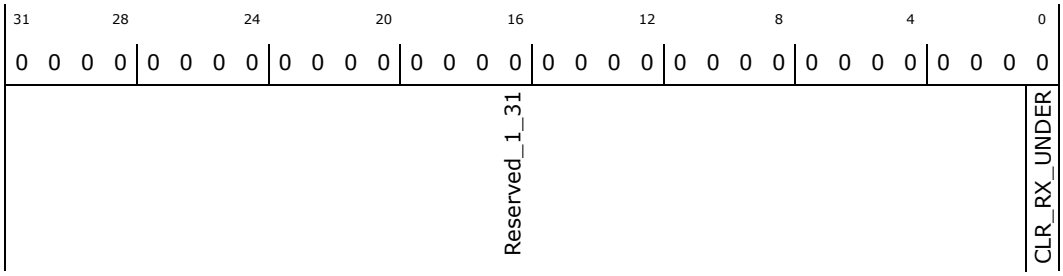
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_UNDER: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

3.43.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

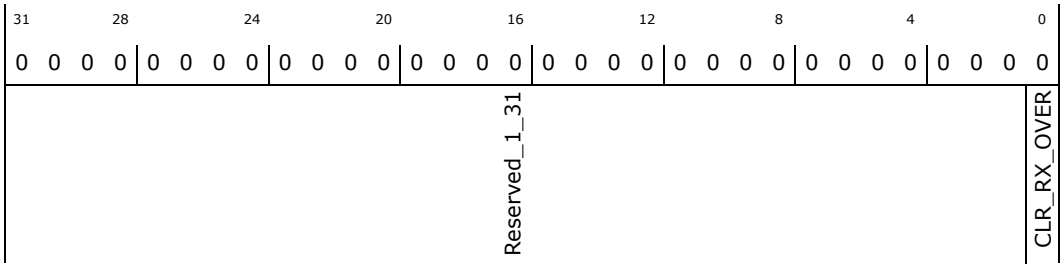
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_OVER: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

3.43.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

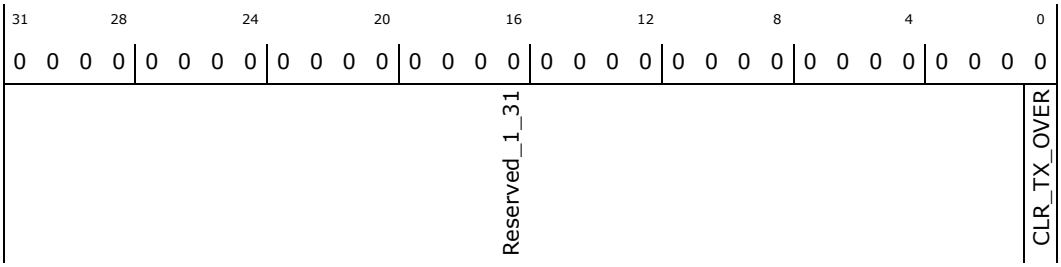
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_OVER: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

3.43.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

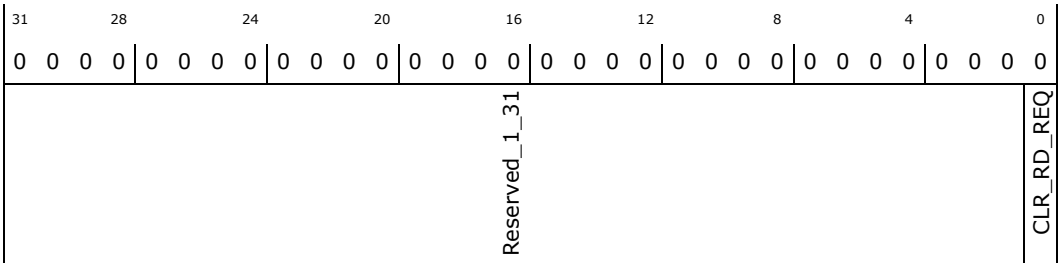
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RD_REQ: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

3.43.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

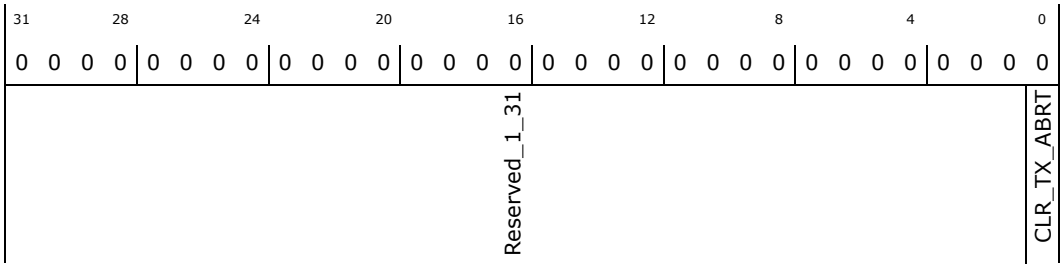
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_ABRT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

3.43.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

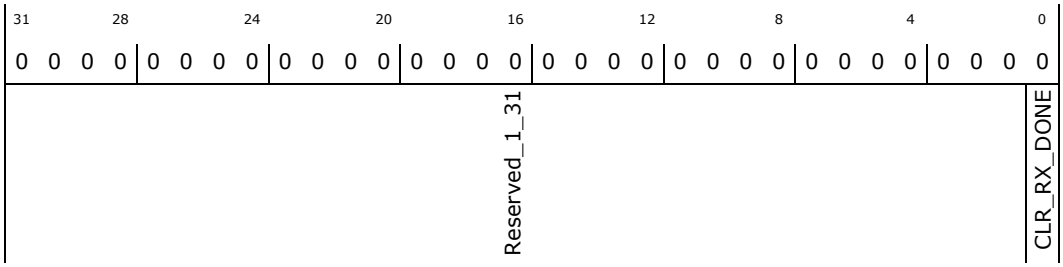
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_DONE: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

3.43.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

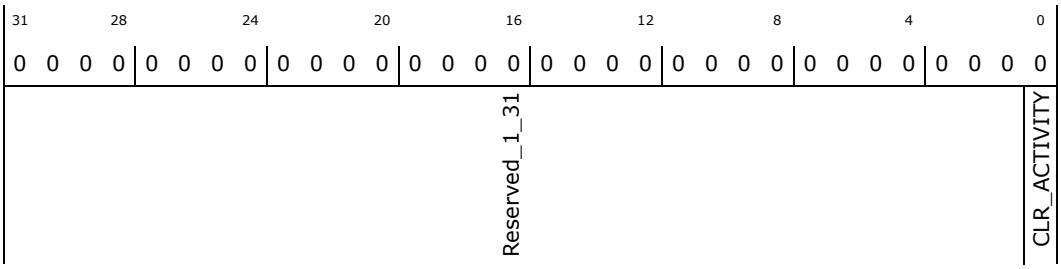
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_ACTIVITY: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

3.43.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

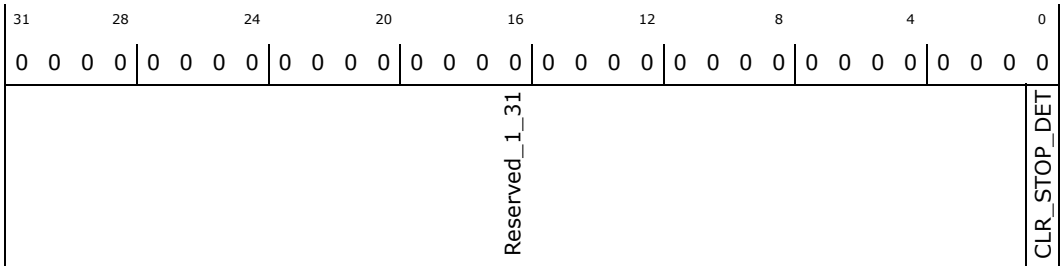
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_STOP_DET: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

3.43.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

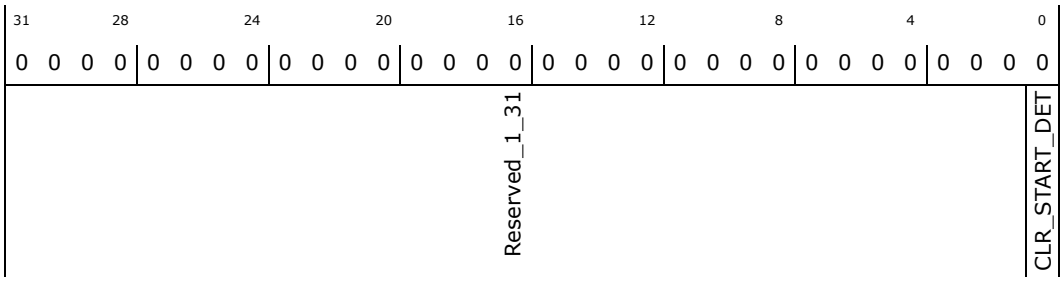
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_START_DET: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

3.43.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

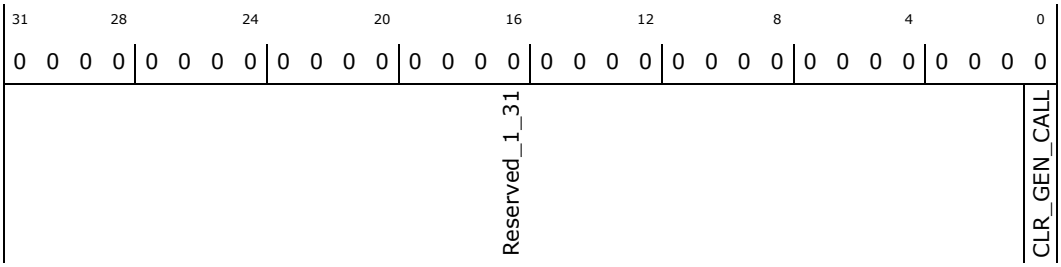
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_GEN_CALL: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

3.43.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

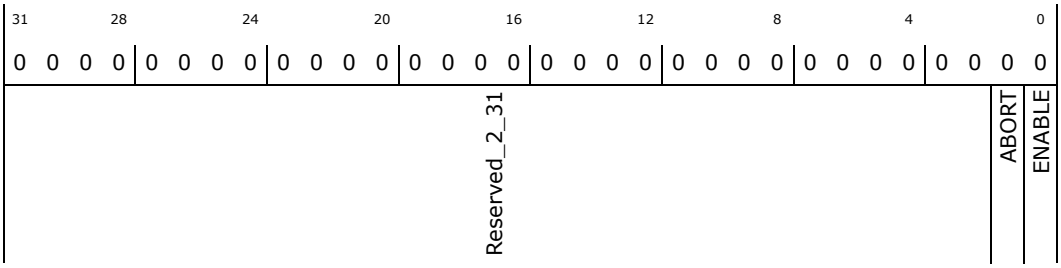
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.

Bit Range	Default & Access	Description
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

3.43.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

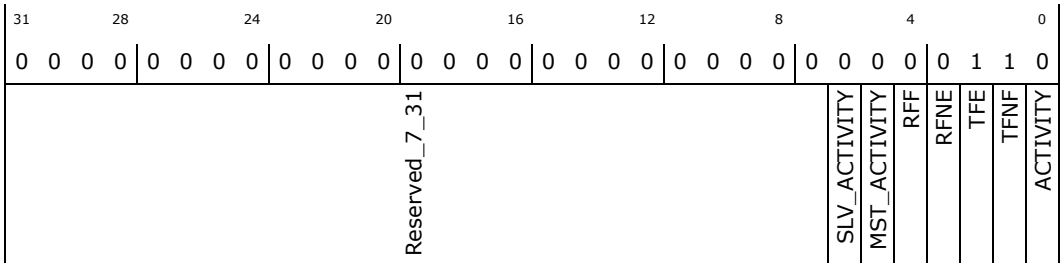
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_STATUS: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.

Bit Range	Default & Access	Description
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

3.43.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

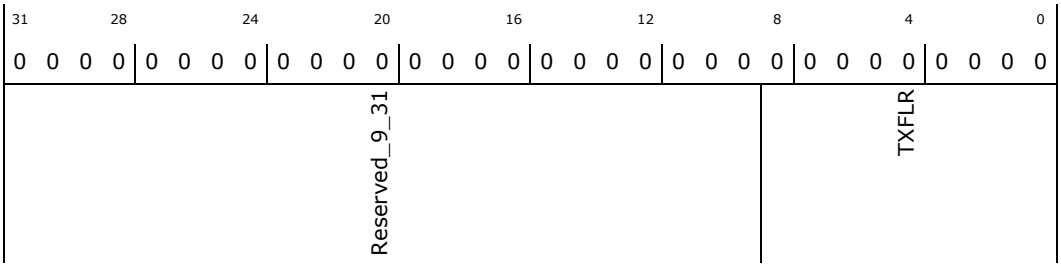
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TXFLR: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

3.43.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

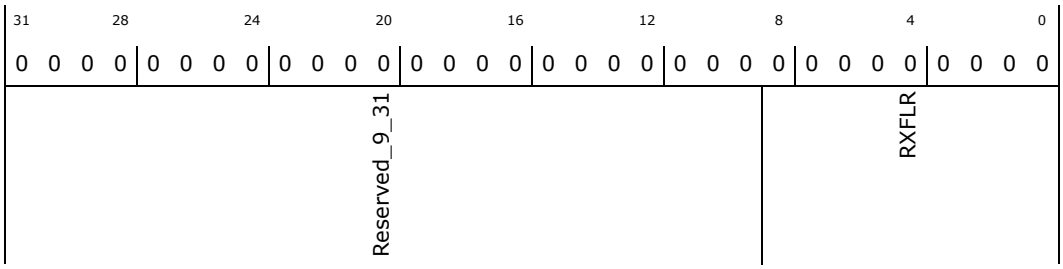
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RXFLR: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

3.43.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implemented one cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

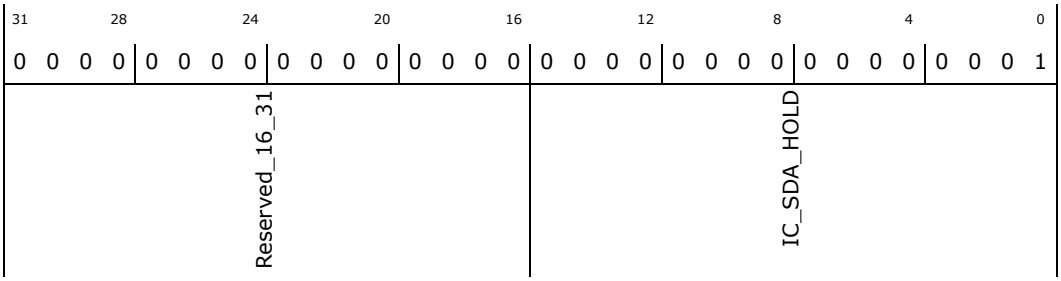
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_HOLD: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

3.43.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

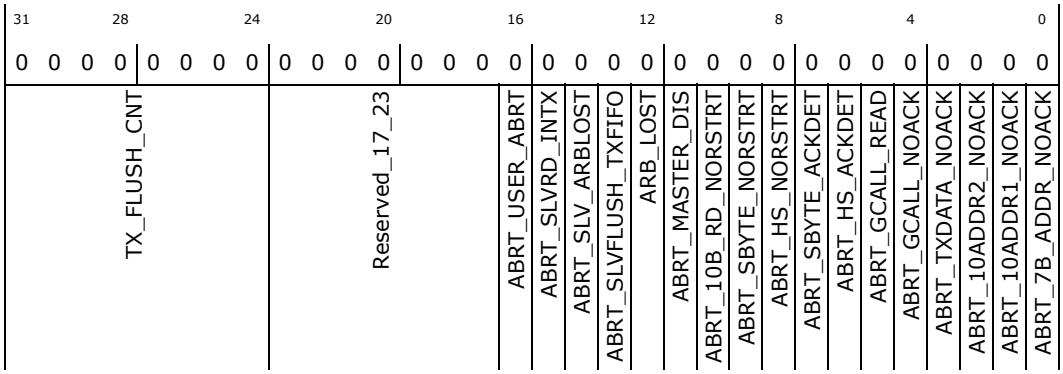
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_ABRT_SOURCE: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).

Bit Range	Default & Access	Description
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

3.43.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. This register only exists when the IC_SLV_DATA_NACK_ONLY parameter is set to 1. When this parameter disabled, this register does not exist and writing to the registers address has no effect. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

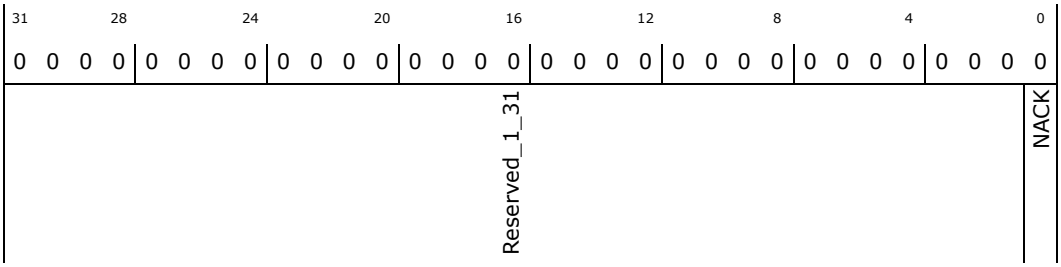
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SLV_DATA_NACK_ONLY: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

3.43.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

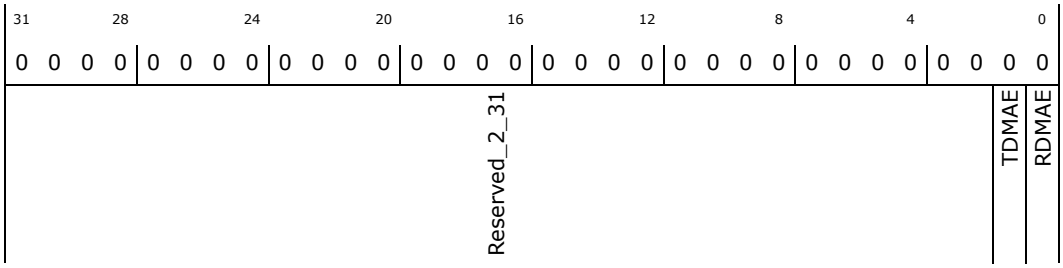
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_CR: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled

Bit Range	Default & Access	Description
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

3.43.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

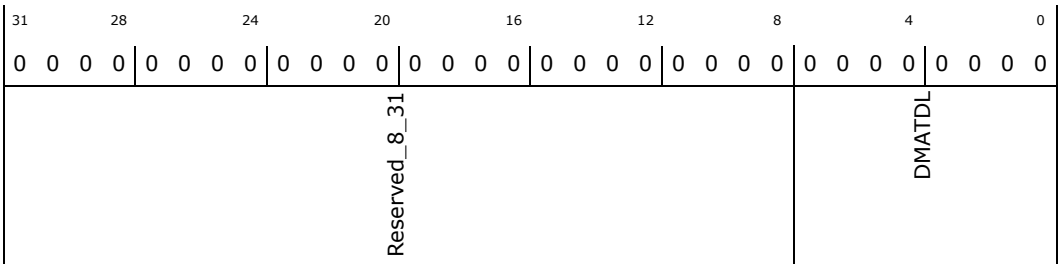
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_TDLR: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

3.43.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

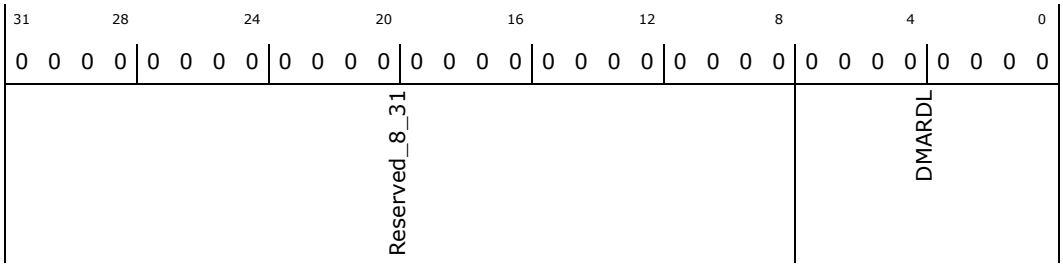
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_RDLR: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

3.43.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2.

NOTE: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

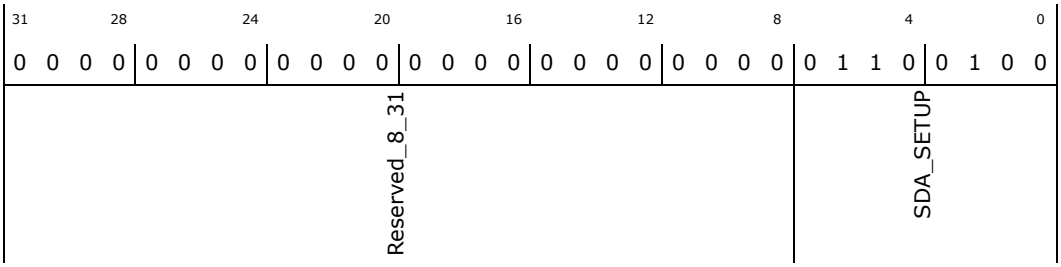
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_SETUP: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000064h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

3.43.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

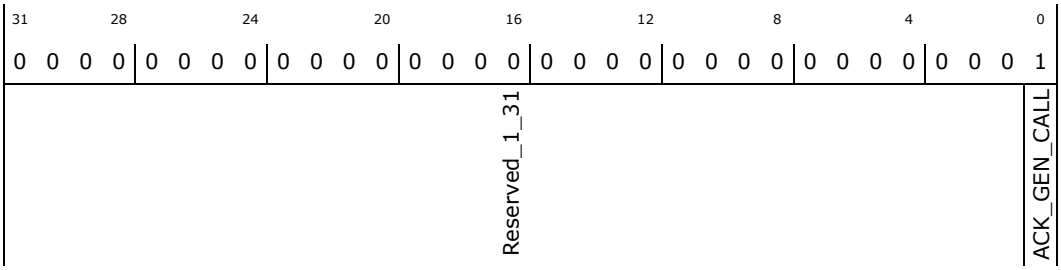
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ACK_GENERAL_CALL: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

3.43.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

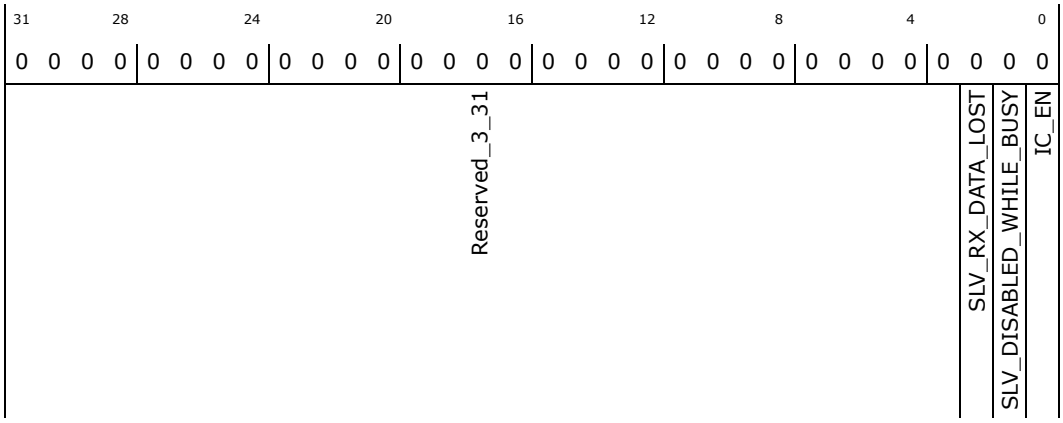
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE_STATUS: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

3.43.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

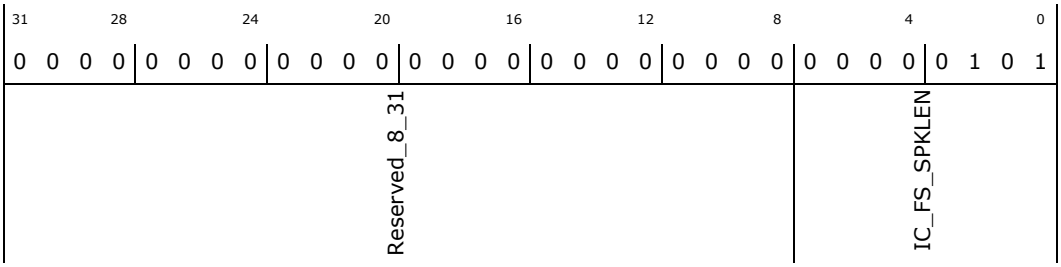
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SPKLEN: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000005h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. **Reset value:** IC_DEFAULT_FS_SPKLEN configuration parameter

3.43.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the

I2C Bus Specification. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

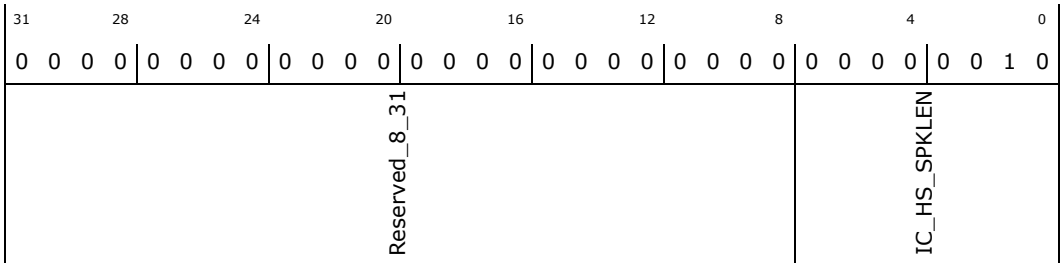
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SPKLEN: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. This register is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3. **Reset value:** IC_DEFAULT_HS_SPKLEN configuration parameter.

3.43.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

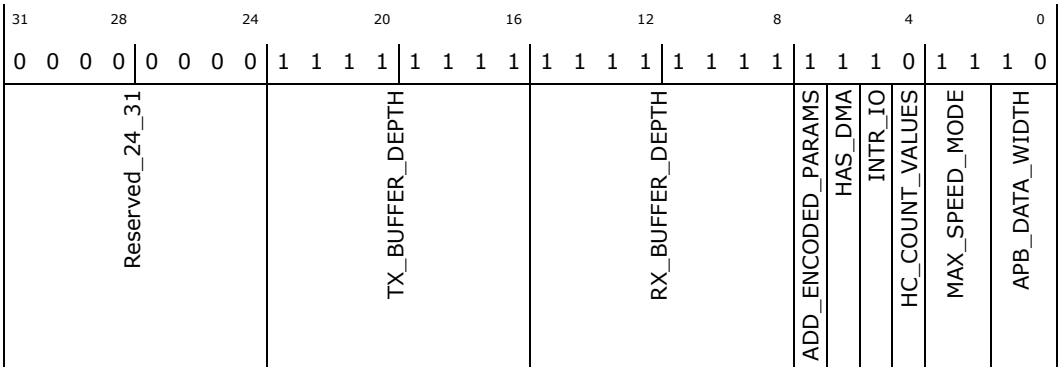
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_PARAM_1: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

3.43.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

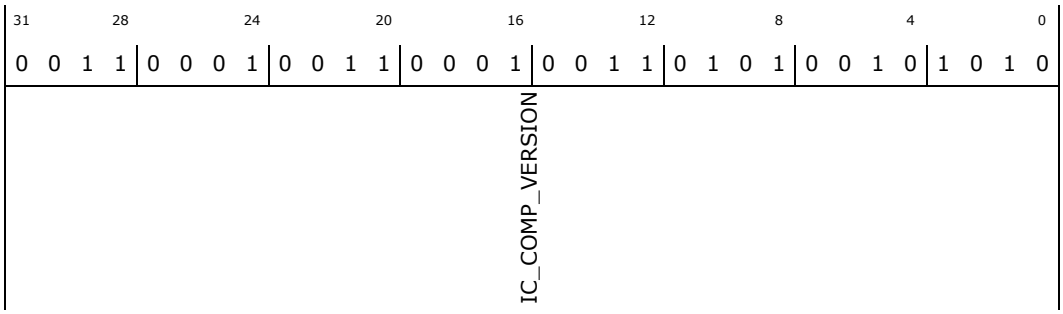
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_VERSION: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

3.43.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

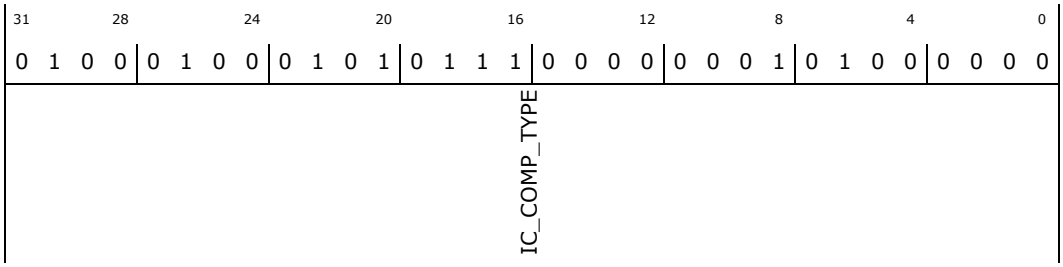
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_TYPE: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 44570140h



Bit Range	Default & Access	Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

3.43.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

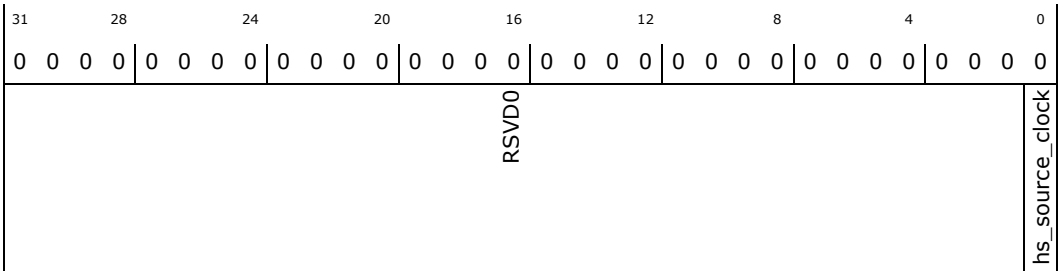
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CLOCK_PARAMS: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

3.43.47 Software Reset (RESETS)—Offset 804h

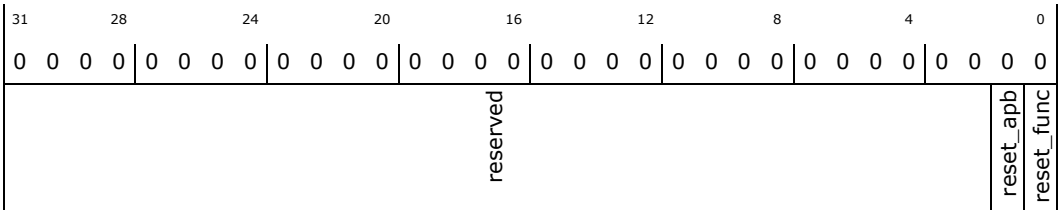
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.43.48 General Purpose Register (GENERAL)—Offset 808h

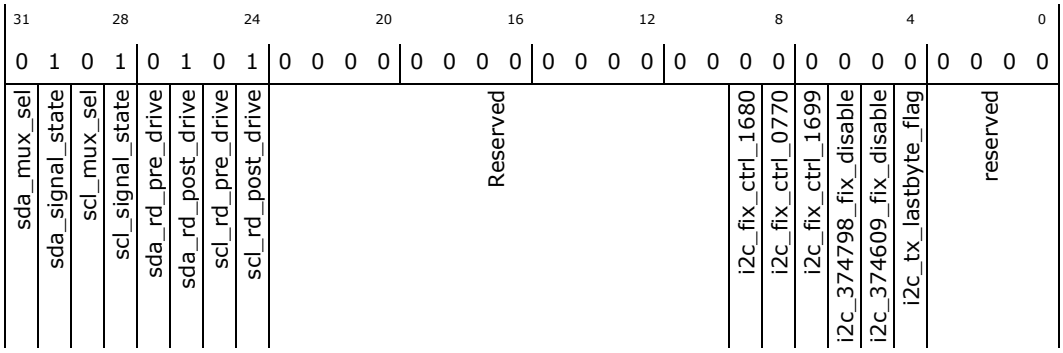
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 55000000h



Bit Range	Default & Access	Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)

Bit Range	Default & Access	Description
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

3.43.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

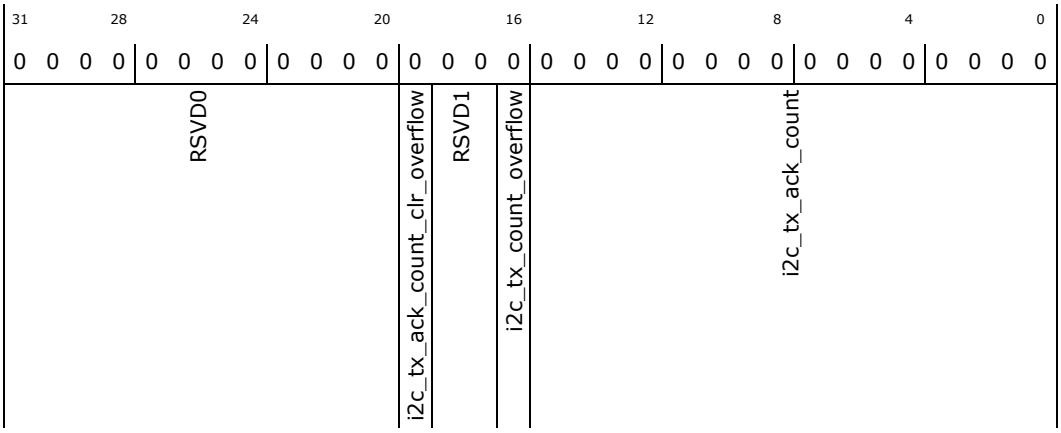
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_ACK_COUNT: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

3.43.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

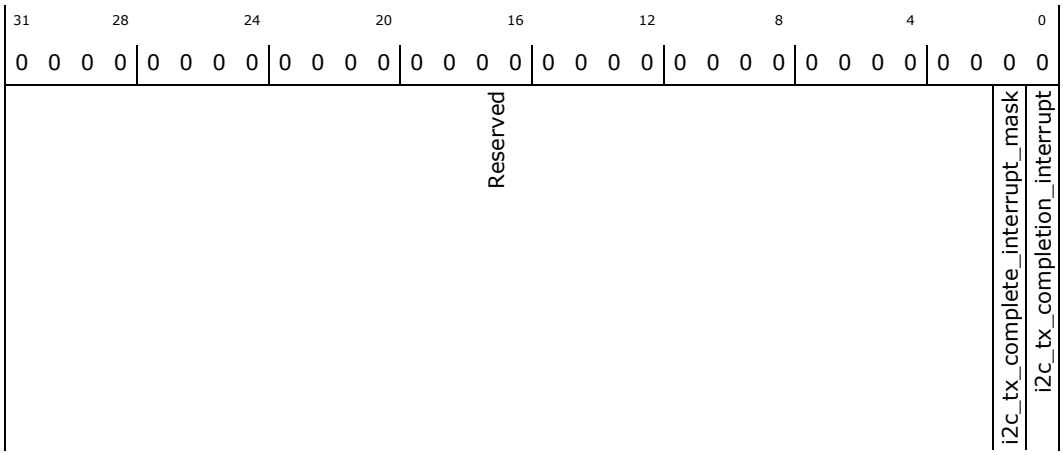
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_TX_COMPLETE_INTR_STAT: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

3.43.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

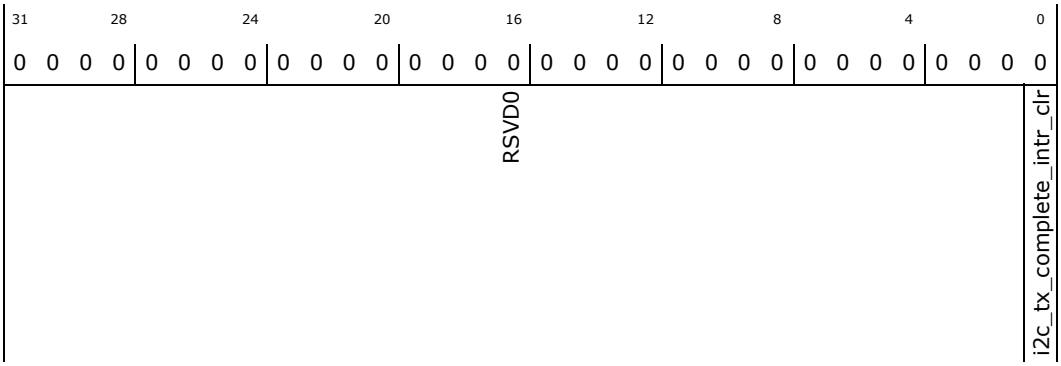
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

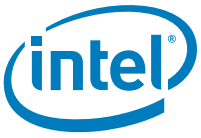
I2C_TX_COMPLETE_INTR_CLR: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt



3.44 SIO I²C6 PCI Configuration Registers

Table 52. Summary of SIO I²C6 PCI Configuration Registers—0/24/7

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2856	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2857	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2858	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2859	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2860	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2860	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2861	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2862	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2862	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2863	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2863	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2864	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2865	00000000h

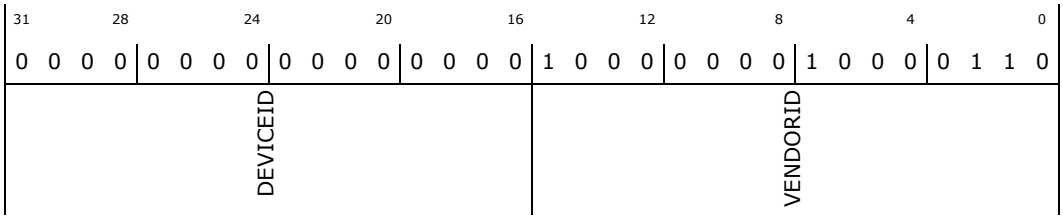
3.44.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:24, F:7] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

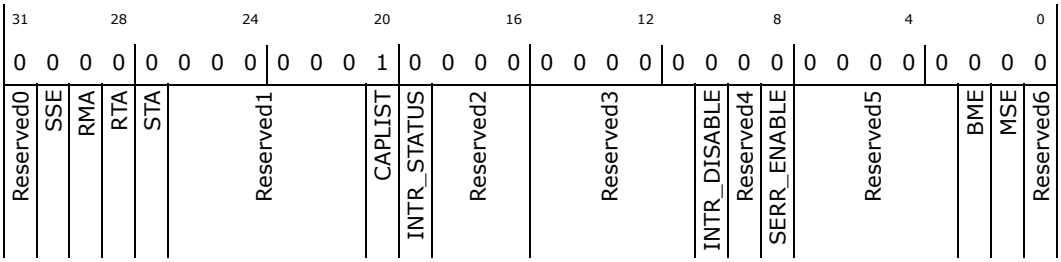
3.44.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:24, F:7] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

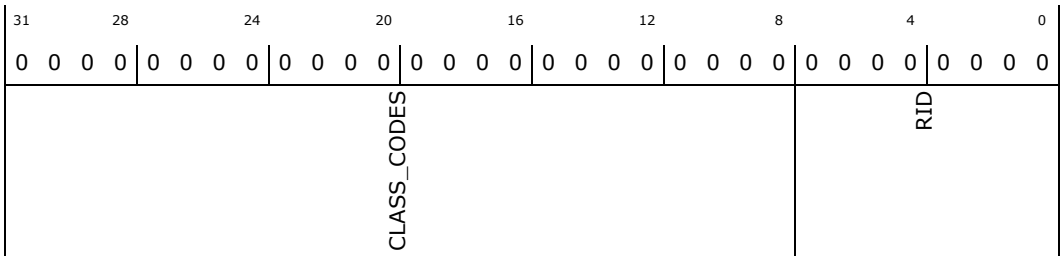
3.44.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:24, F:7] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

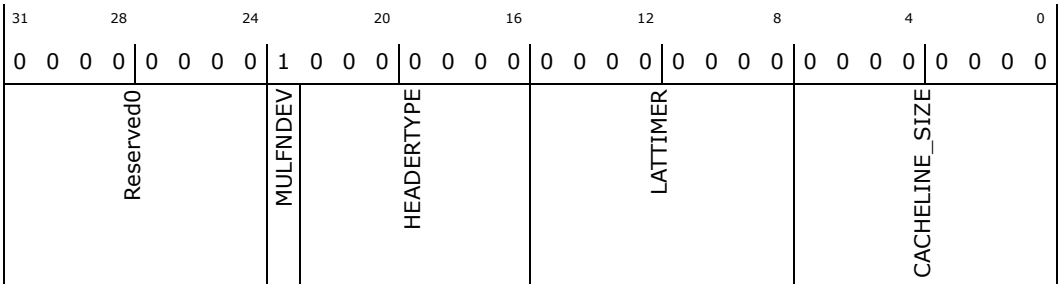
3.44.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:24, F:7] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

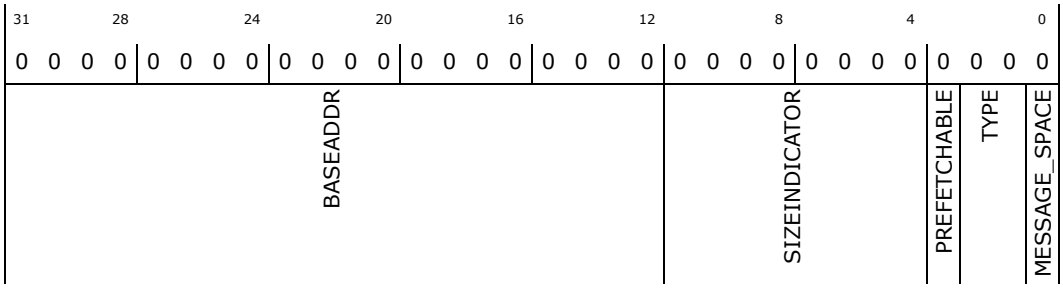
3.44.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

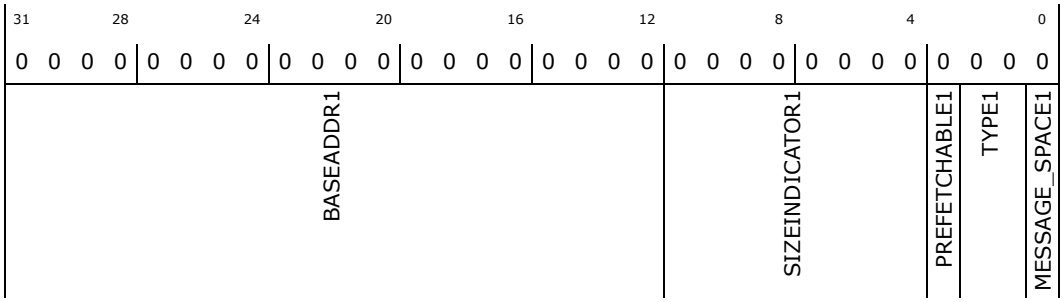
3.44.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:24, F:7] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

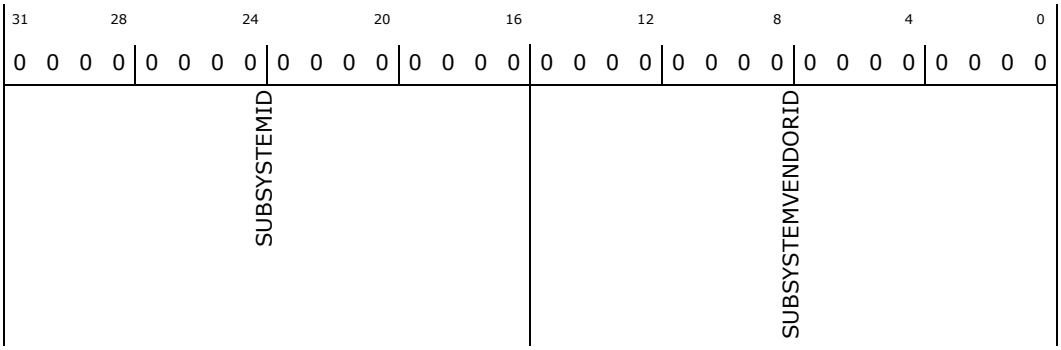
3.44.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:24, F:7] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

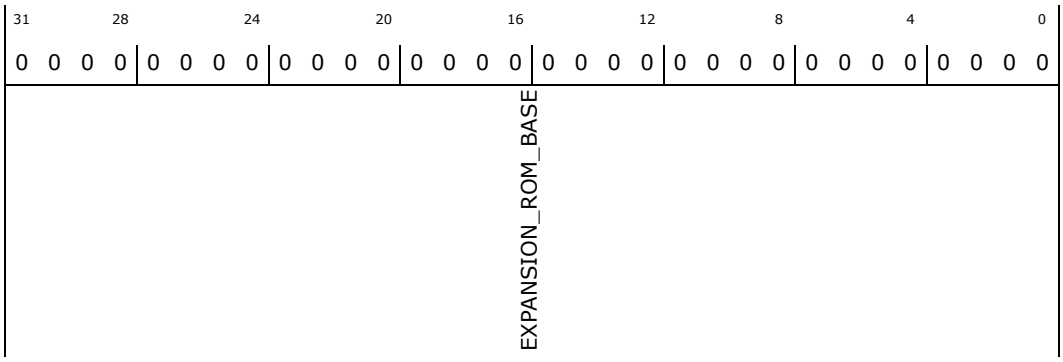
3.44.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:24, F:7] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

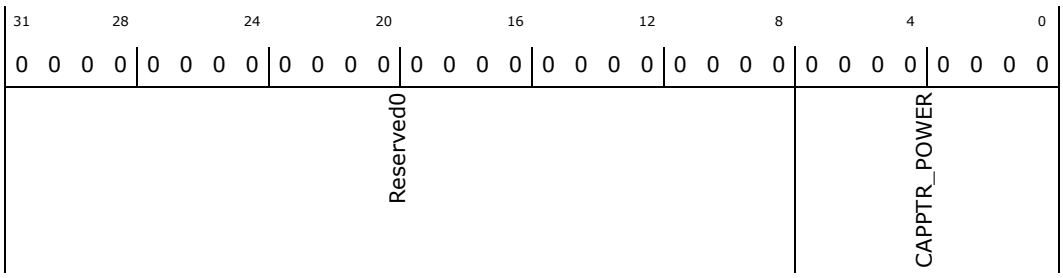
3.44.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:24, F:7] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

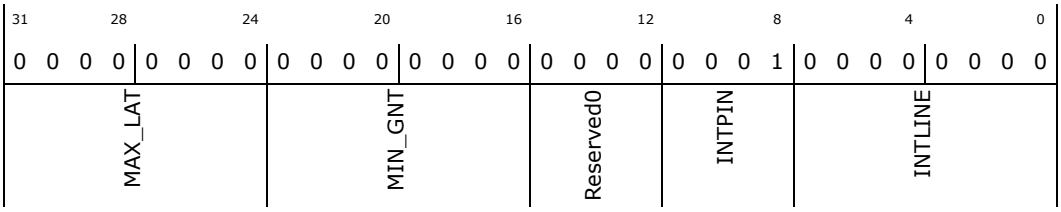
3.44.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:24, F:7] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

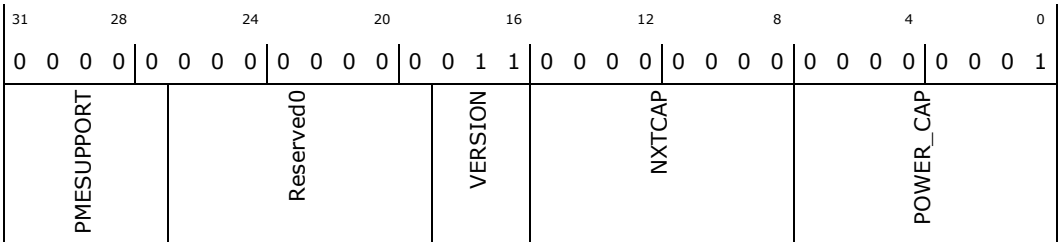
3.44.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:24, F:7] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

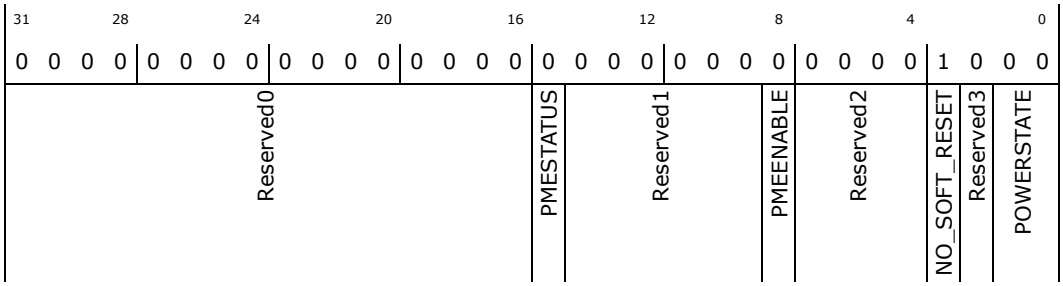
3.44.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:24, F:7] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

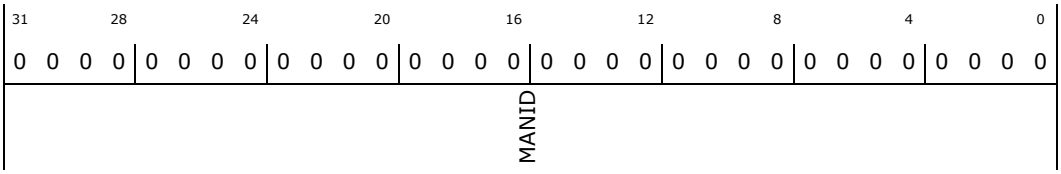
3.44.13 Manufacturer ID (MANID)—Offset F8h

Access Method

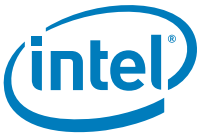
Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:24, F:7] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.



3.45 SIO I²C6 Memory Mapped IO Registers

Table 53. Summary of SIO I²C6 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 2868	0000007Fh
4h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 2869	00001055h
8h	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 2870	00000055h
Ch	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 2871	00000001h
10h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 2872	00000000h
14h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 2873	00000190h
18h	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 2874	000001D6h
1Ch	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 2874	0000003Ch
20h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 2875	00000082h
24h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 2876	0000000Ch
28h	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 2877	00000020h
2Ch	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 2878	00000000h
30h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 2879	000008FFh
34h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 2880	00000000h
38h	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 2882	00000010h
3Ch	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 2882	00000010h
40h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 2883	00000000h
44h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 2883	00000000h
48h	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 2884	00000000h
4Ch	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 2884	00000000h
50h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 2885	00000000h

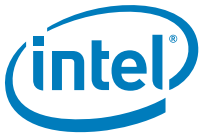


Table 53. Summary of SIO I²C6 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
54h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 2886	00000000h
58h	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 2886	00000000h
5Ch	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 2887	00000000h
60h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 2887	00000000h
64h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 2888	00000000h
68h	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 2888	00000000h
6Ch	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 2889	00000000h
70h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 2890	00000006h
74h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 2891	00000000h
78h	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 2892	00000000h
7Ch	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 2892	00000001h
80h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 2893	00000000h
84h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 2895	00000000h
88h	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 2896	00000000h
8Ch	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 2897	00000000h
90h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 2897	00000000h
94h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 2898	00000064h
98h	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 2899	00000001h
9Ch	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 2900	00000000h
A0h	4	"IC_FS_SPKLEN—Offset A0h" on page 2901	00000005h
A4h	4	"IC_HS_SPKLEN—Offset A4h" on page 2901	00000002h
F4h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 2902	00FFFFEEh
F8h	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 2903	3131352Ah
FCh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 2904	44570140h
800h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 2904	00000000h

Table 53. Summary of SIO I²C6 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
804h	4	"Software Reset (RESETS)—Offset 804h" on page 2905	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 2906	55000000h
818h	4	"I2C_ACK_COUNT—Offset 818h" on page 2907	00000000h
820h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 2908	00000000h
824h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 2908	00000000h

3.45.1 I2C Control Register (IC_CON)—Offset 0h

If configuration parameter I2C_DYNAMIC_TAR_UPDATE = 0, all bits are Read/Write.

If I2C_DYNAMIC_TAR_UPDATE = 1, bit 4 is Read-only.

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

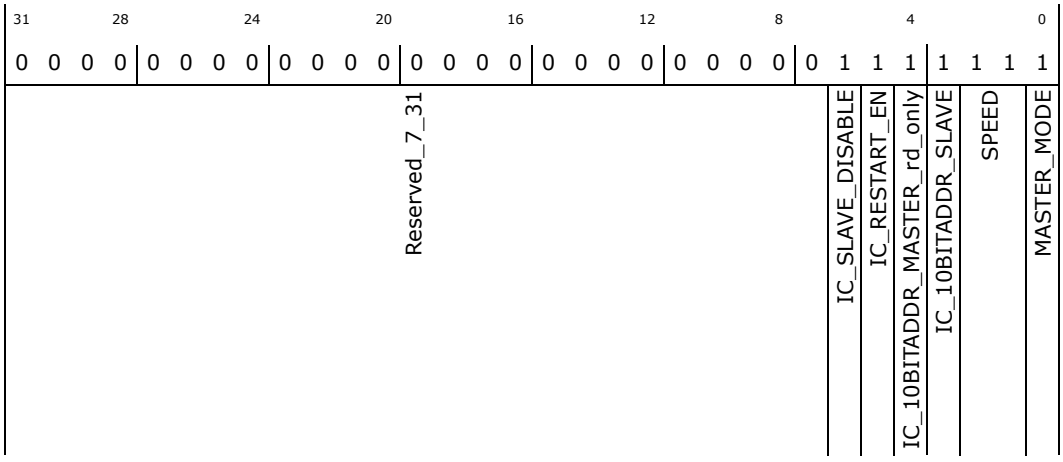
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CON: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

3.45.2 I2C Target Address Register (IC_TAR)—Offset 4h

If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to No (0), this register is 12 bits wide, and bits 15:12 are reserved. Writes to this register succeed only when IC_ENABLE is set to 0.

However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND

- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

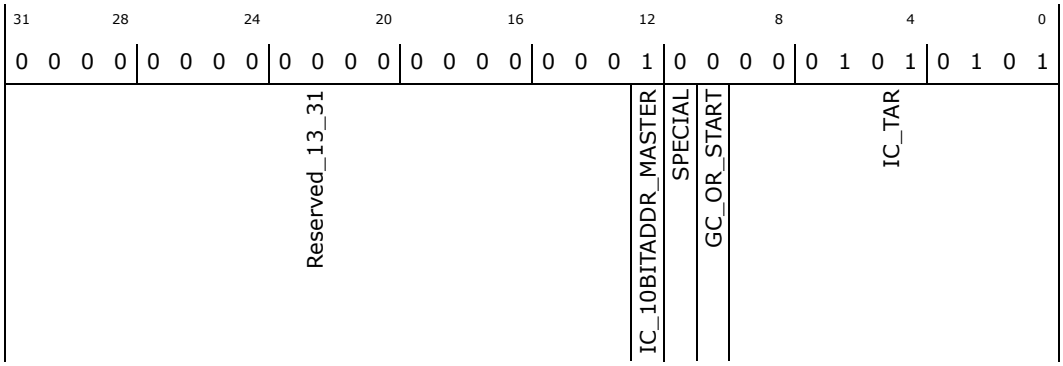
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TAR: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00001055h



Bit Range	Default & Access	Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

3.45.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

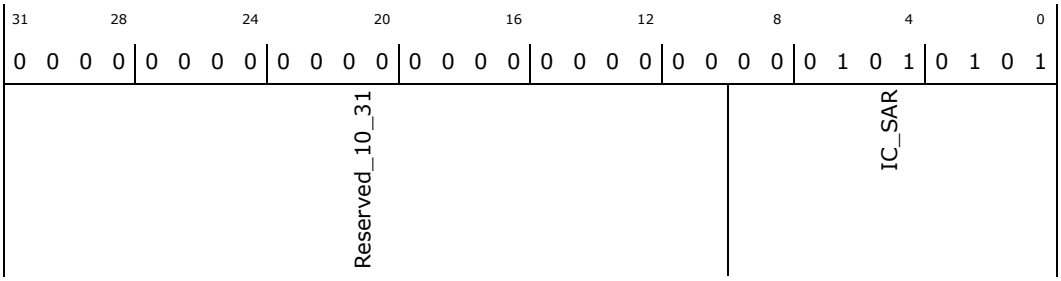
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SAR: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000055h



Bit Range	Default & Access	Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.45.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

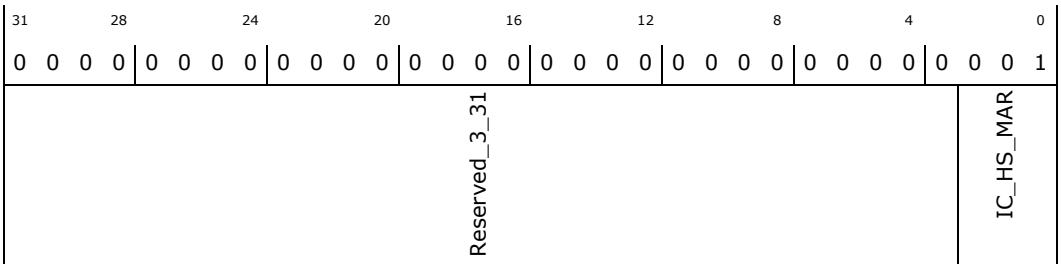
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_MADDR: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.45.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

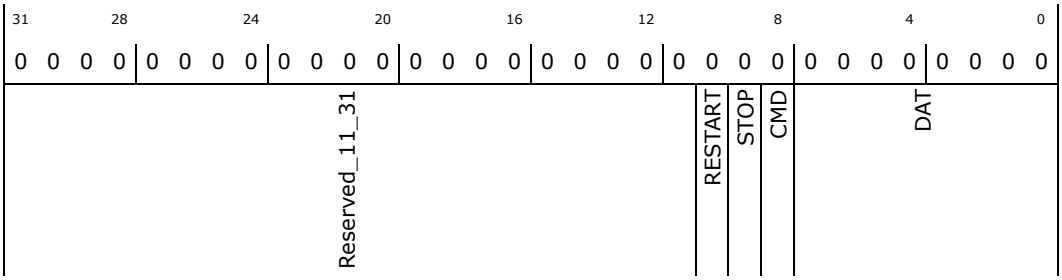
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DATA_CMD: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:11	0b RW	**Reserved_11_31:** Reserved.

Bit Range	Default & Access	Description
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/ received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

3.45.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

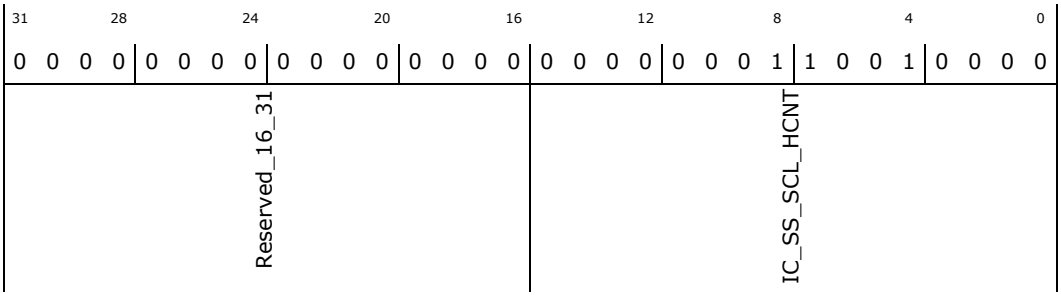
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_HCNT: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000190h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.45.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

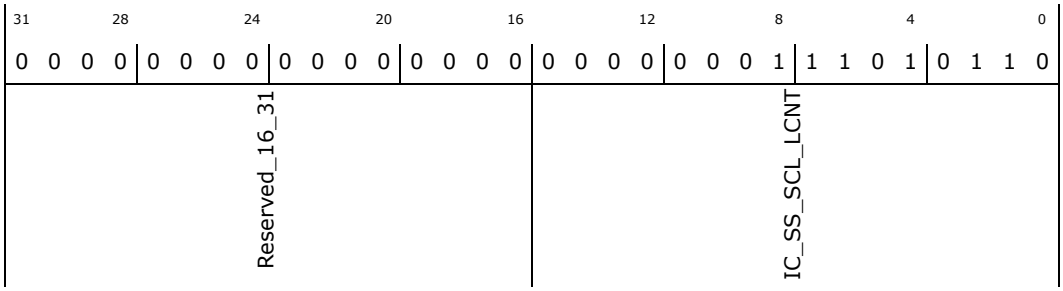
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SS_SCL_LCNT: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 000001D6h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.45.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to the Synopsis DesignWare DW_apb_i2c Databook.

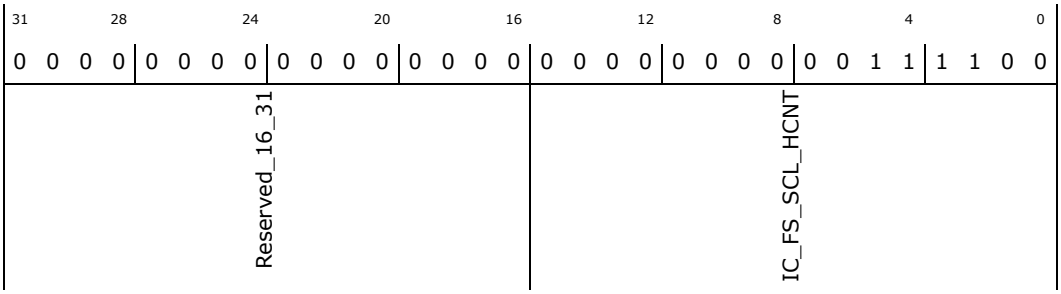
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_HCNT: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.45.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to 'IC_CLK Frequency Configuration' in the Synopsis DesignWare DW_apb_i2c Databook.

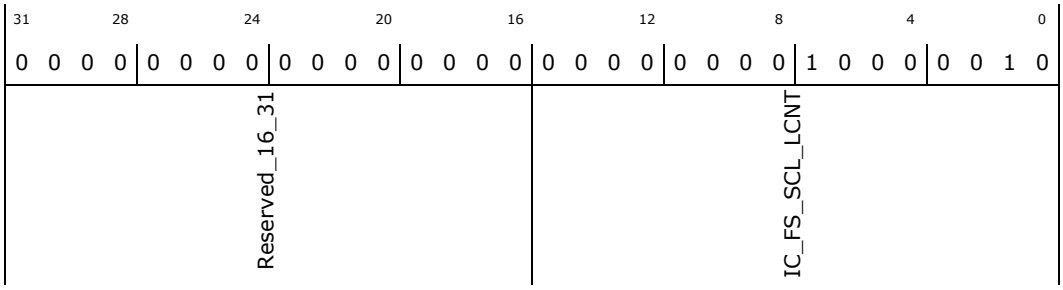
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SCL_LCNT: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000082h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.45.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* .

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

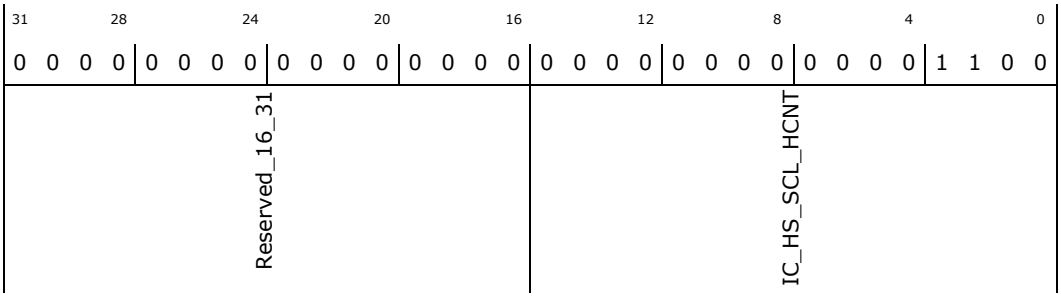
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_HCNT: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.45.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to *IC_CLK Frequency Configuration* in the Synopsis DesignWare DW_apb_i2c Databook.

The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.

This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

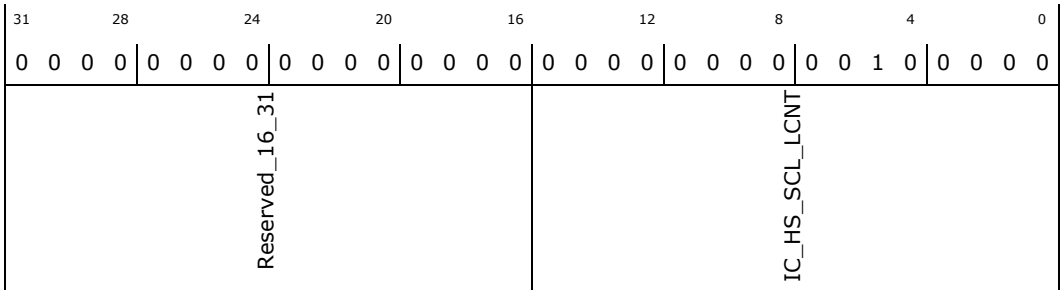
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SCL_LCNT: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000020h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

3.45.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

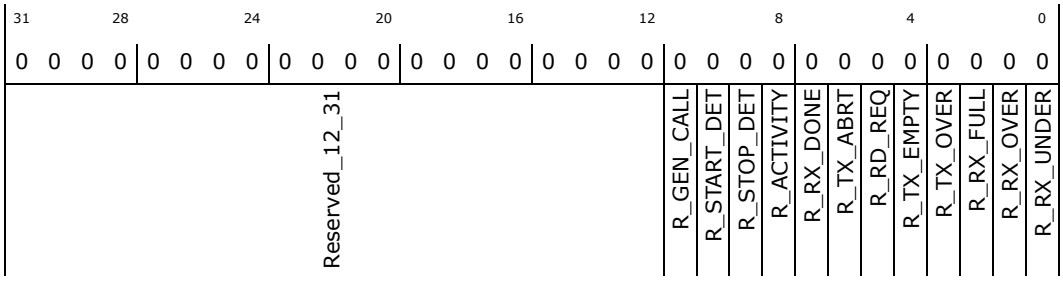
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

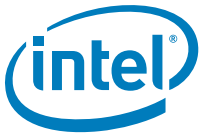
IC_INTR_STAT: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.



Bit Range	Default & Access	Description
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

3.45.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

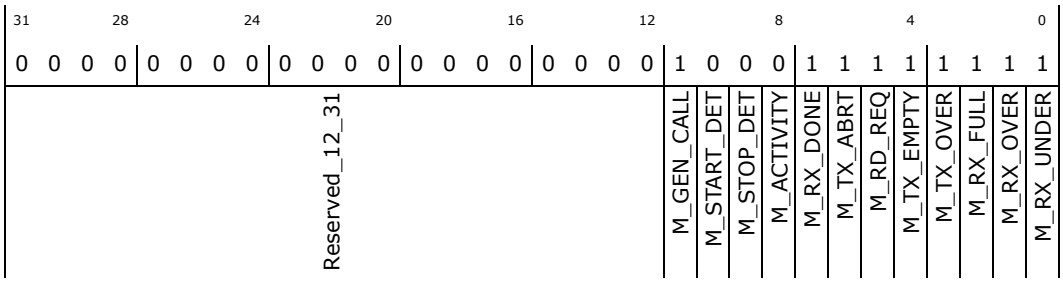
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_INTR_MASK: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 000008FFh



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

3.45.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

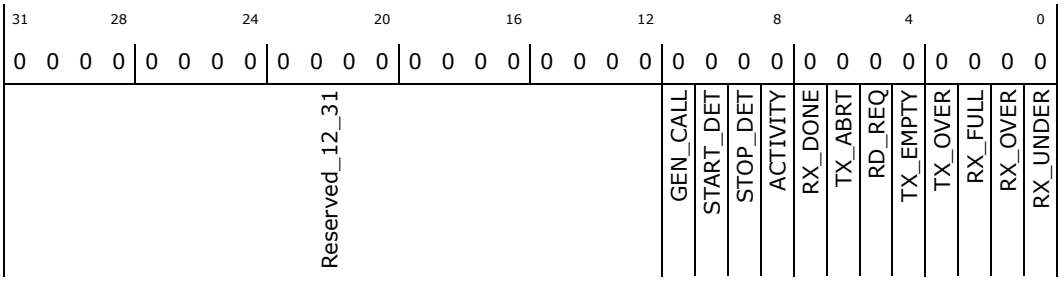
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RAW_INTR_STAT: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

3.45.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

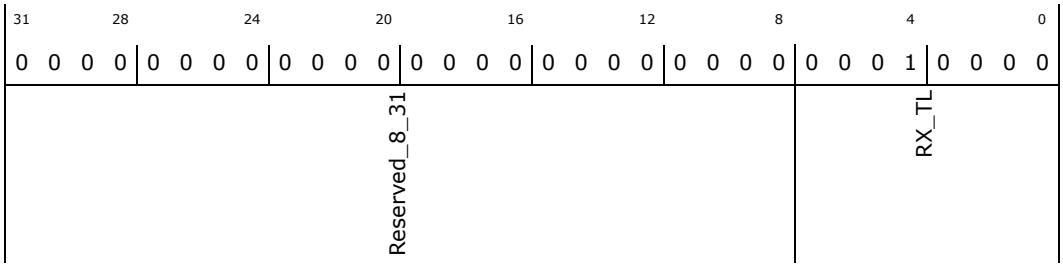
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RX_TL: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.45.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

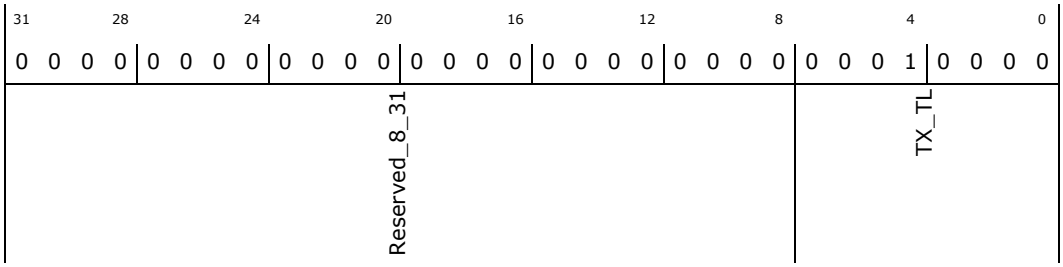
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_TL: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

3.45.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

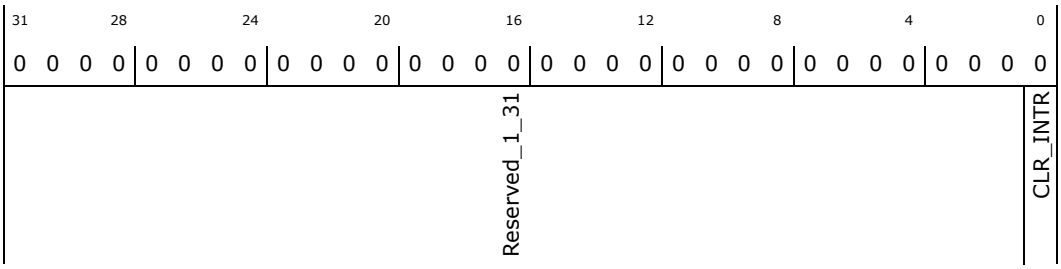
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_INTR: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

3.45.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

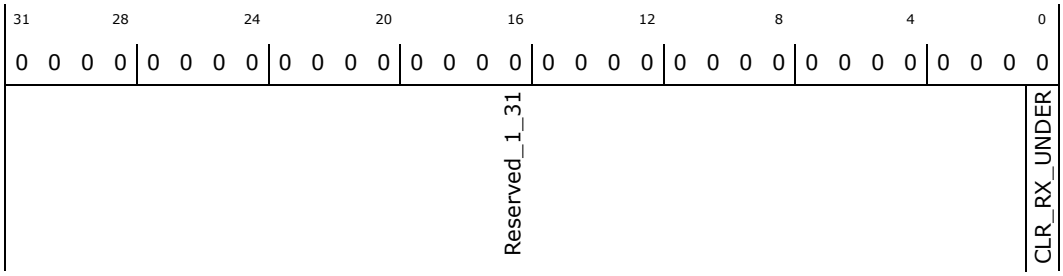
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_UNDER: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

3.45.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

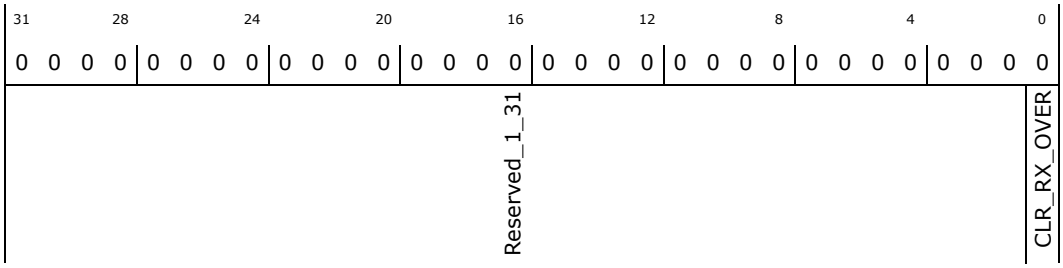
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_OVER: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

3.45.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

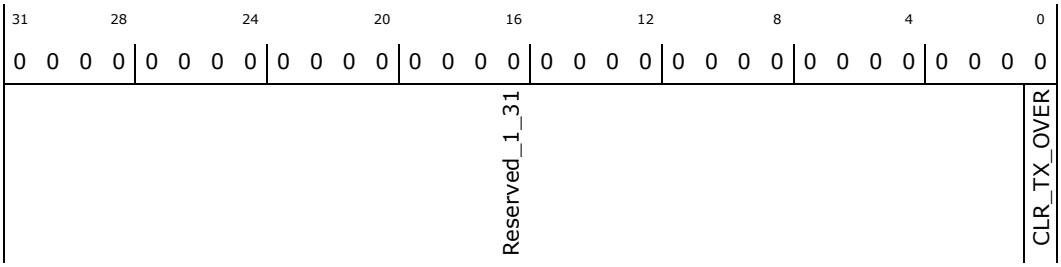
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_OVER: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

3.45.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

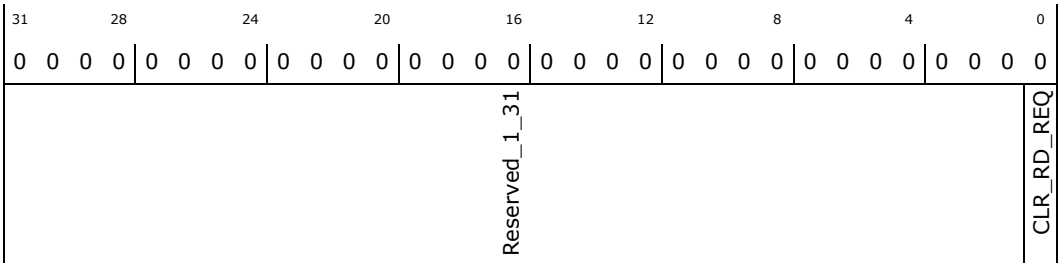
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RD_REQ: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

3.45.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

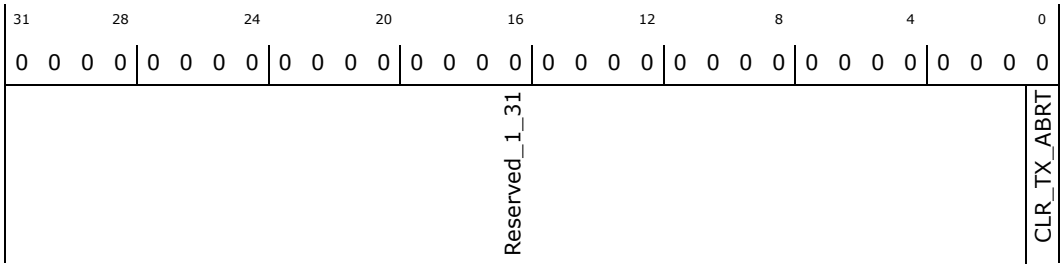
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_TX_ABRT: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

3.45.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

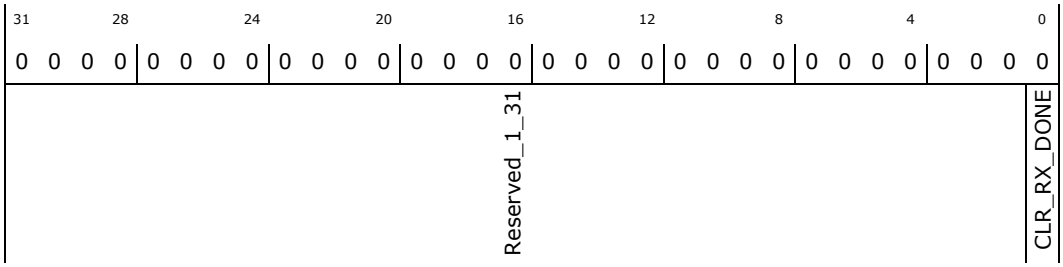
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_RX_DONE: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

3.45.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

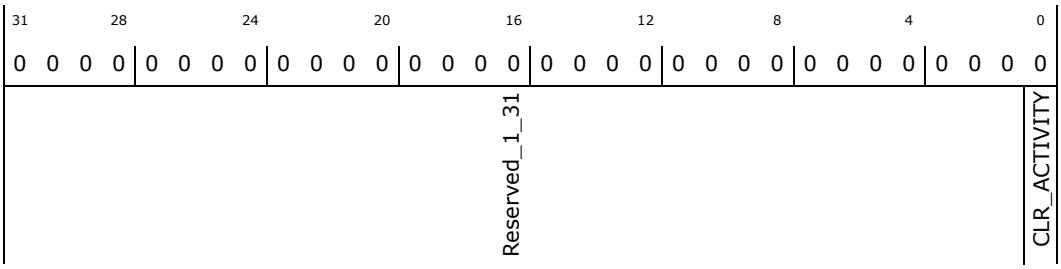
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_ACTIVITY: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

3.45.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

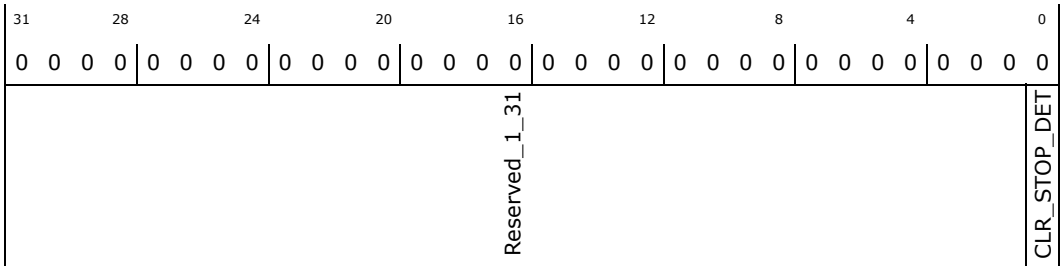
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_STOP_DET: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

3.45.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

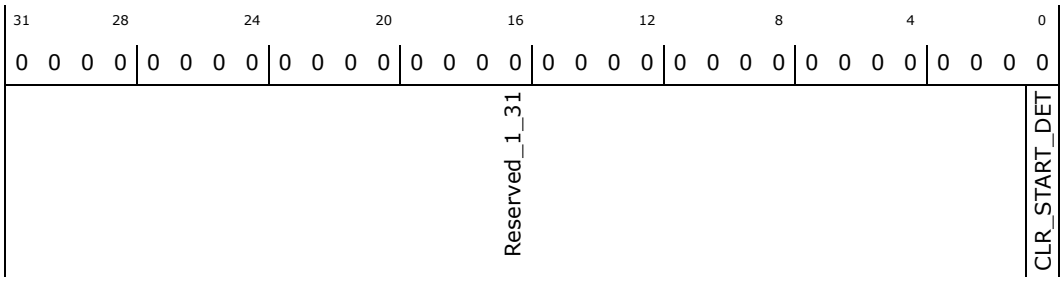
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_START_DET: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

3.45.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

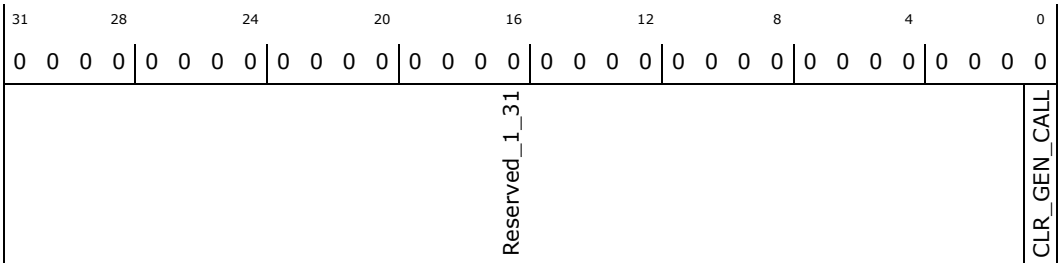
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_CLR_GEN_CALL: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

3.45.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

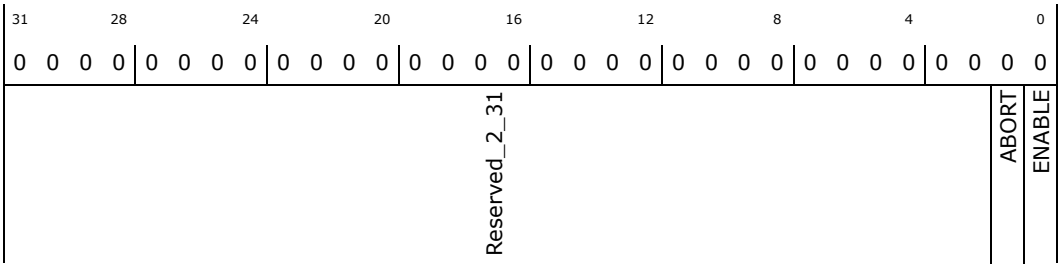
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.

Bit Range	Default & Access	Description
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

3.45.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

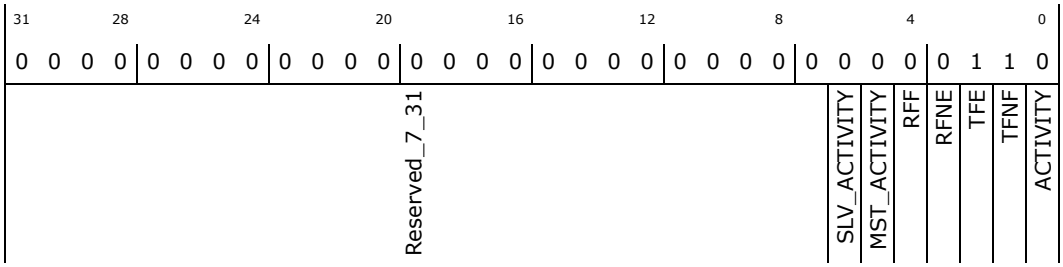
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_STATUS: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.

Bit Range	Default & Access	Description
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

3.45.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

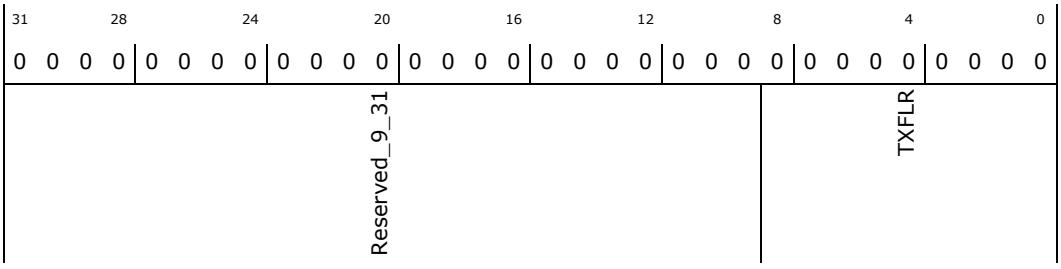
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TXFLR: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

3.45.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

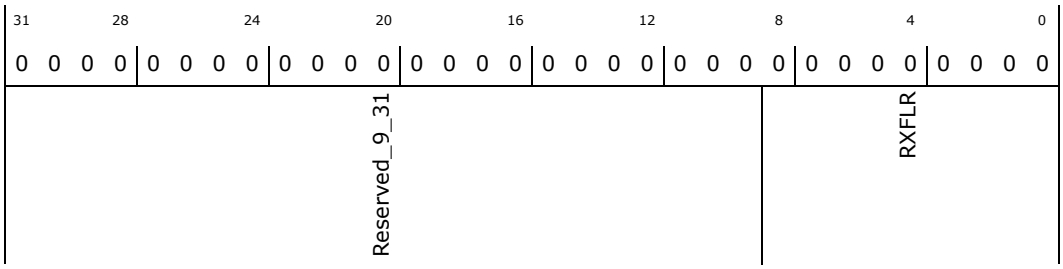
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_RXFLR: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

3.45.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implemented one cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

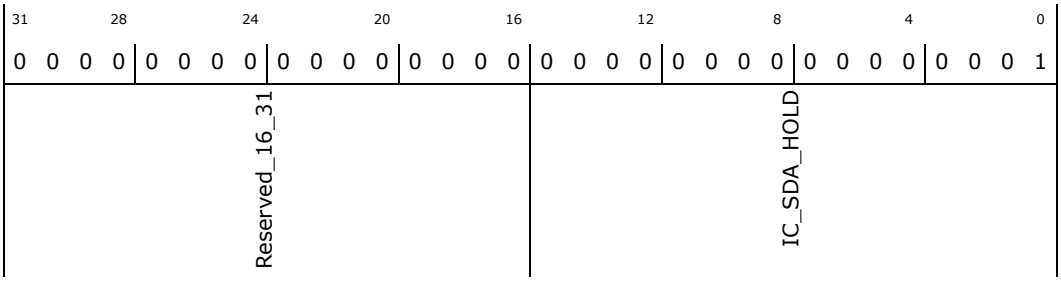
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_HOLD: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

3.45.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

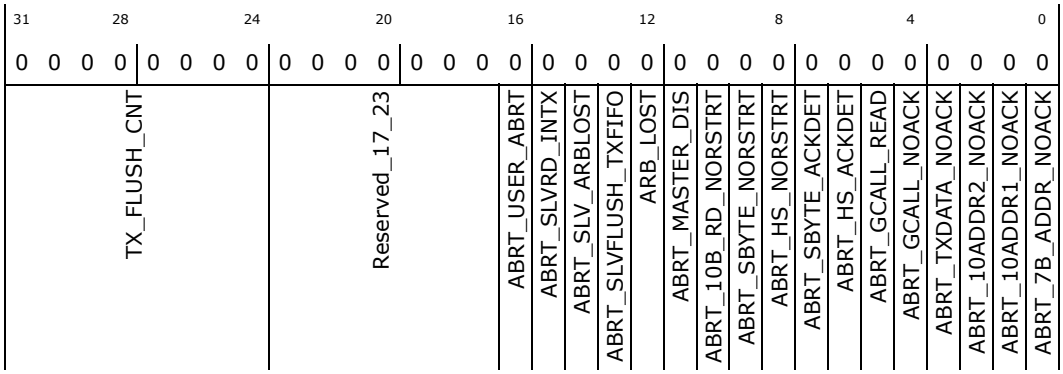
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_TX_ABRT_SOURCE: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).

Bit Range	Default & Access	Description
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

3.45.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. This register only exists when the IC_SLV_DATA_NACK_ONLY parameter is set to 1. When this parameter disabled, this register does not exist and writing to the registers address has no effect. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

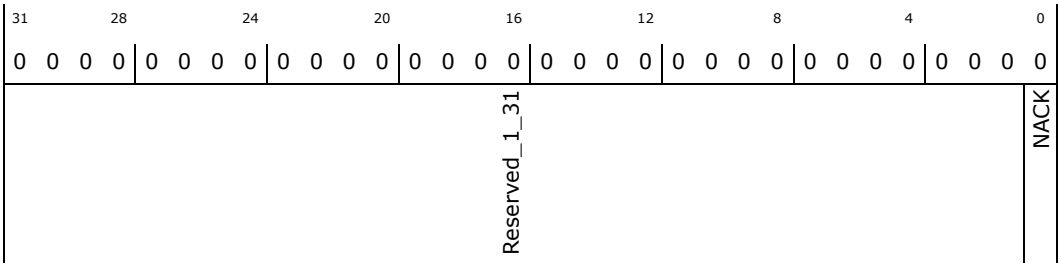
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SLV_DATA_NACK_ONLY: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slave receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

3.45.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

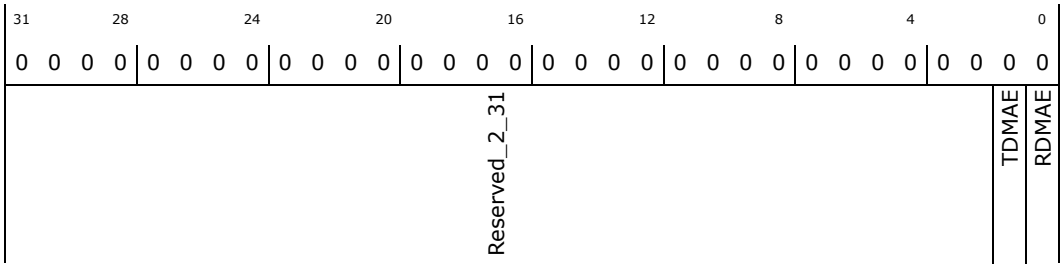
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_CR: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled

Bit Range	Default & Access	Description
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

3.45.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

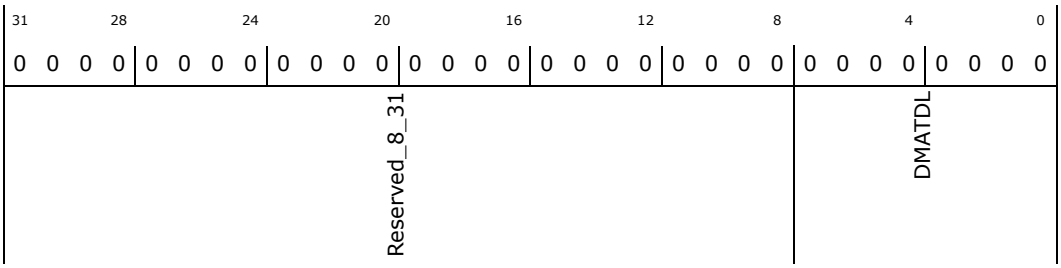
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_TDLR: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

3.45.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

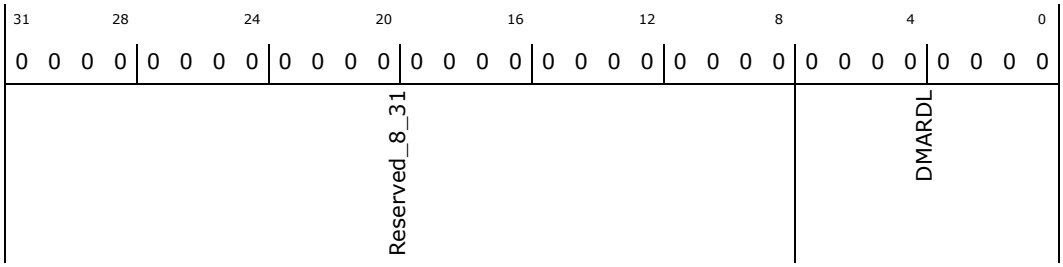
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_DMA_RDLR: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

3.45.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2.

NOTE: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

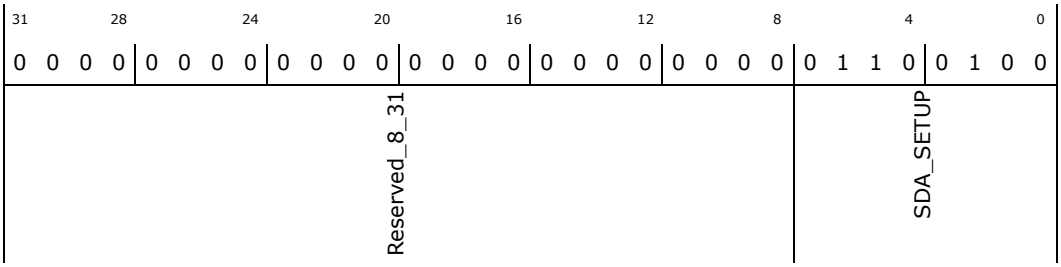
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_SDA_SETUP: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000064h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

3.45.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

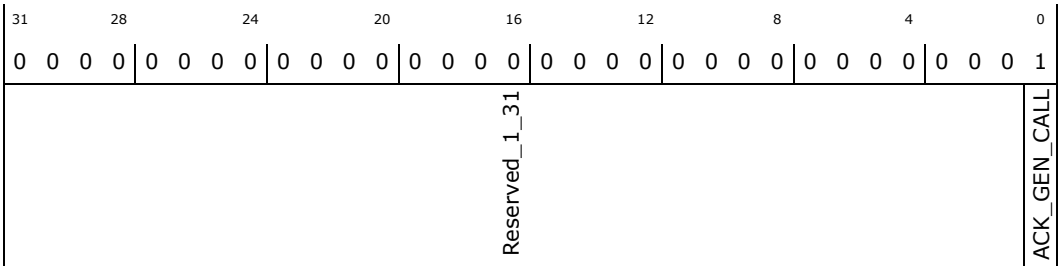
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ACK_GENERAL_CALL: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

3.45.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

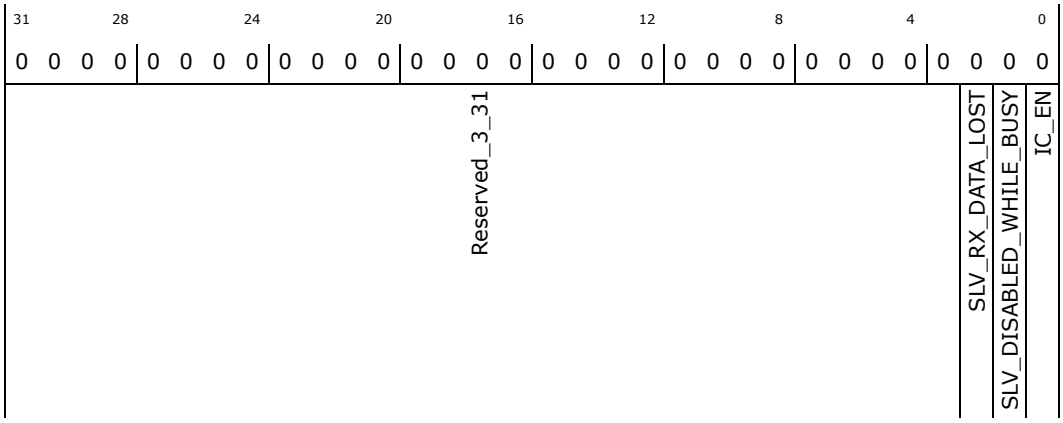
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_ENABLE_STATUS: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

3.45.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

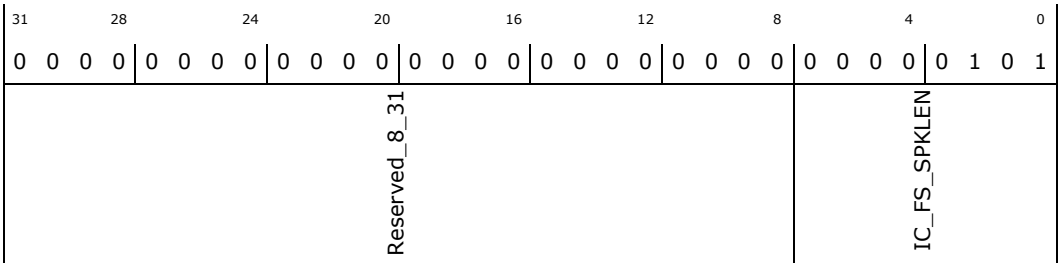
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_FS_SPKLEN: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000005h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. **Reset value:** IC_DEFAULT_FS_SPKLEN configuration parameter

3.45.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the

I2C Bus Specification. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

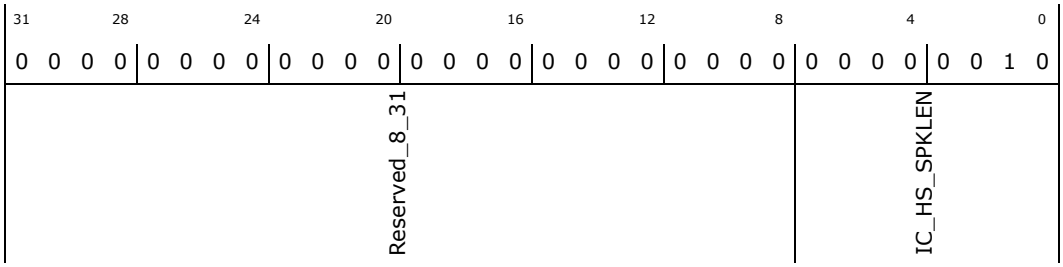
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_HS_SPKLEN: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000002h



Bit Range	Default & Access	Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set. This register is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3. **Reset value:** IC_DEFAULT_HS_SPKLEN configuration parameter.

3.45.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

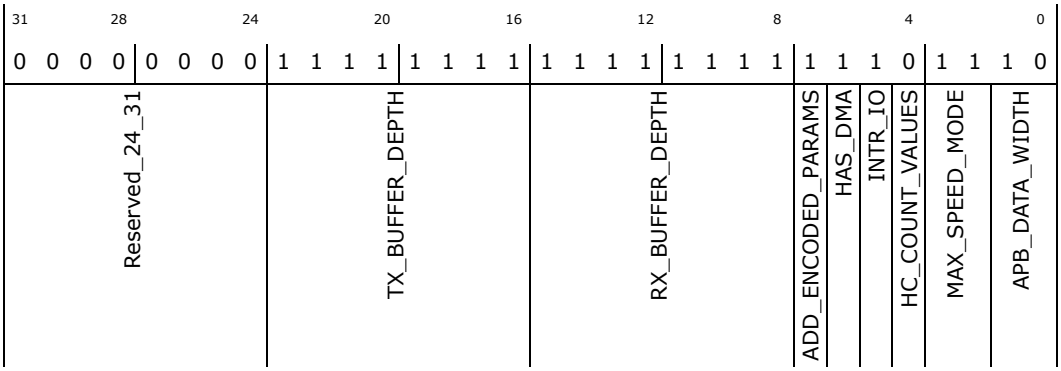
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_PARAM_1: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

3.45.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

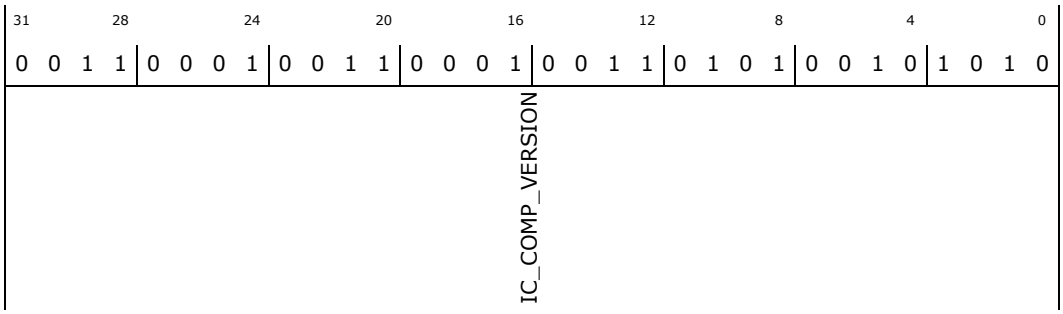
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_VERSION: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

3.45.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

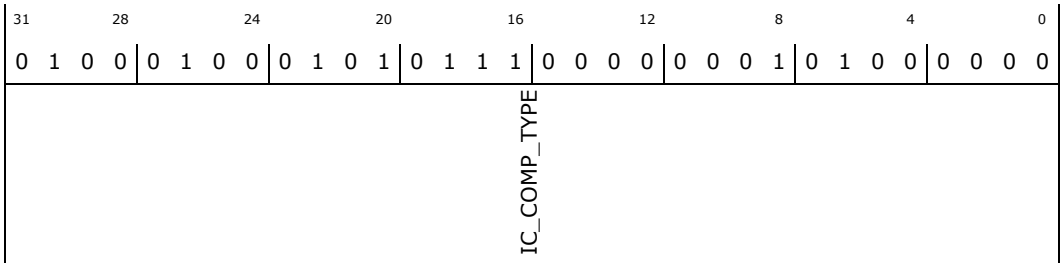
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC_COMP_TYPE: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 44570140h



Bit Range	Default & Access	Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

3.45.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

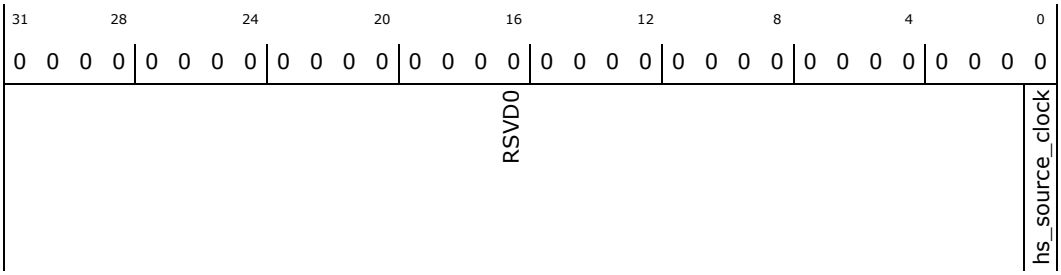
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CLOCK_PARAMS: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

3.45.47 Software Reset (RESETS)—Offset 804h

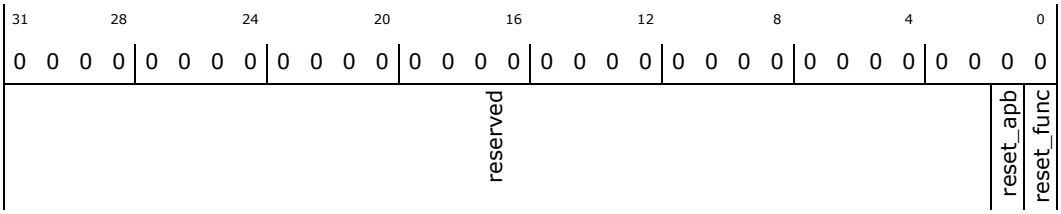
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.45.48 General Purpose Register (GENERAL)—Offset 808h

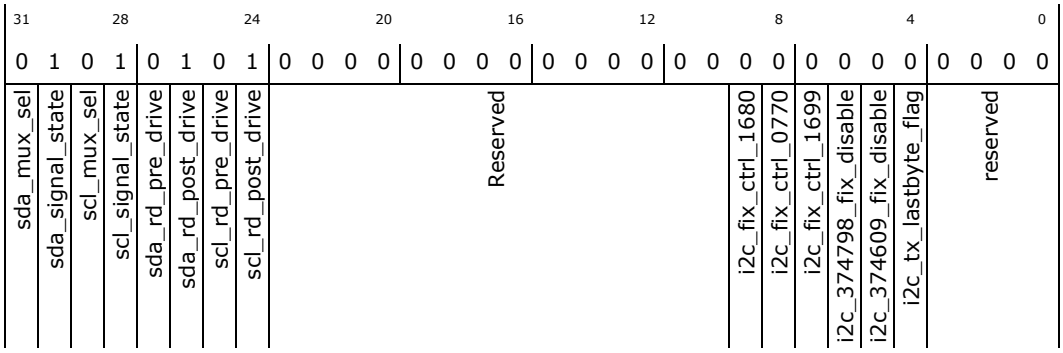
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 55000000h



Bit Range	Default & Access	Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)

Bit Range	Default & Access	Description
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

3.45.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

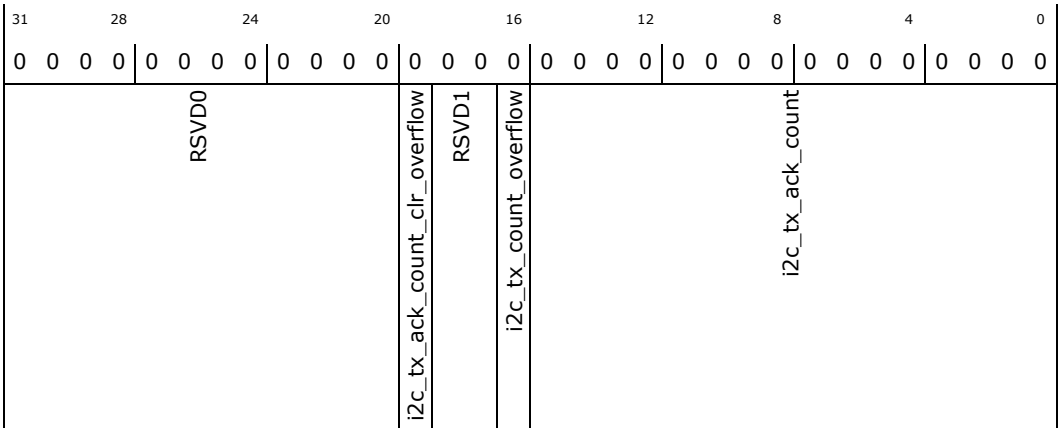
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_ACK_COUNT: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

3.45.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

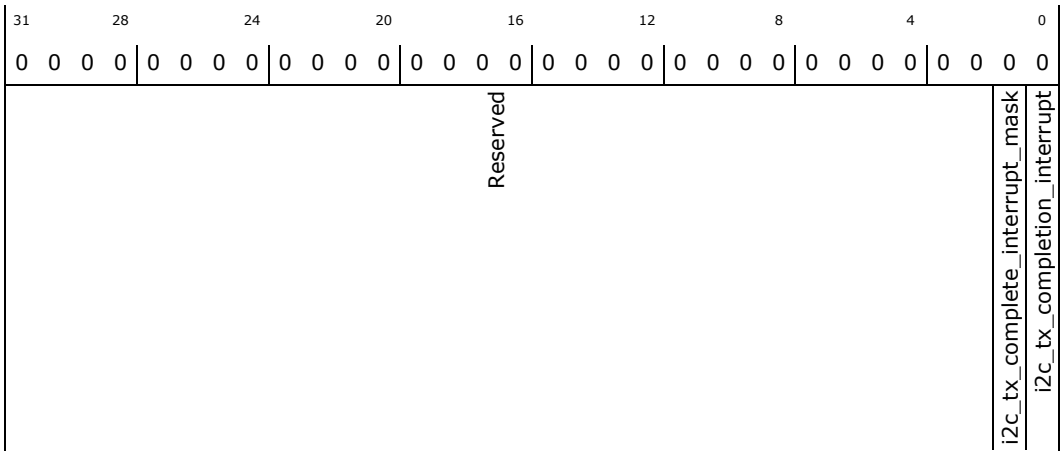
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

I2C_TX_COMPLETE_INTR_STAT: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

3.45.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

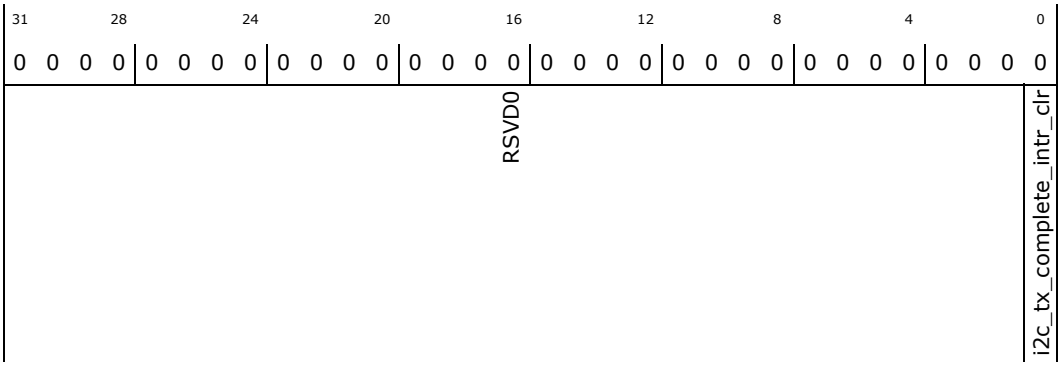
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

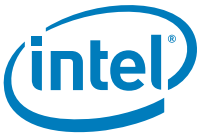
I2C_TX_COMPLETE_INTR_CLR: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt



3.46 SIO HSUART1 PCI Configuration Registers

Table 54. Summary of SIO HSUART1 PCI Configuration Registers—0/30/3

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2910	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2911	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2912	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2913	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2914	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2914	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2915	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2916	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2916	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2917	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2917	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2918	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2919	00000000h

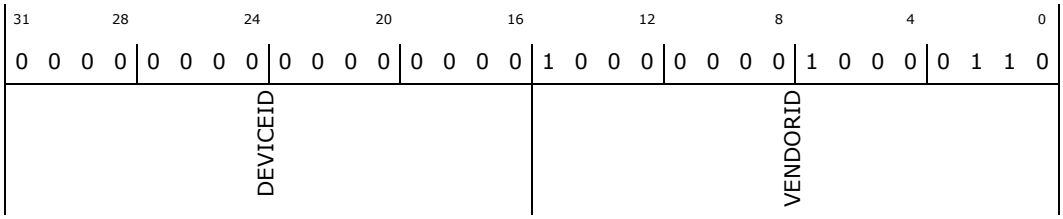
3.46.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:30, F:3] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

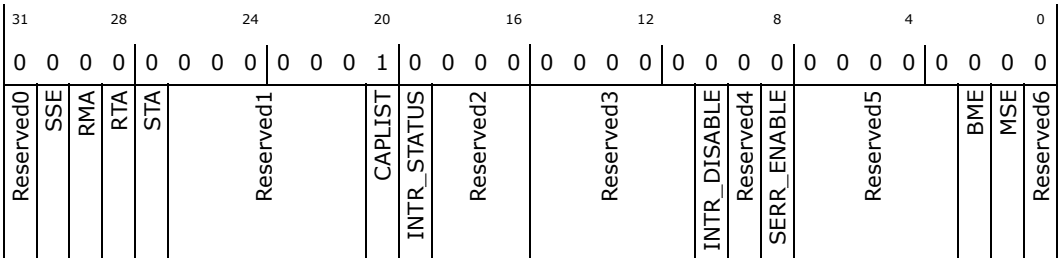
3.46.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:30, F:3] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

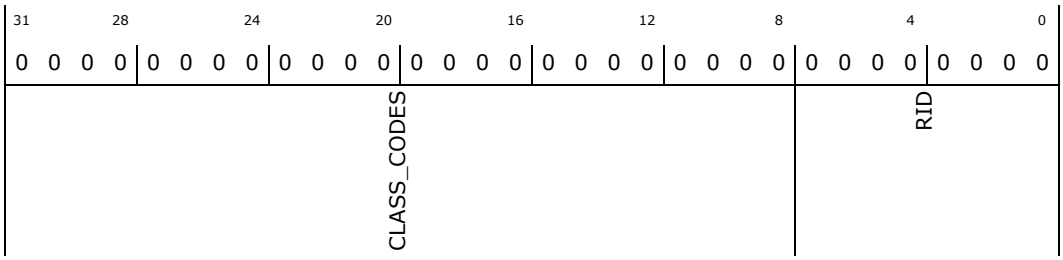
3.46.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:30, F:3] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

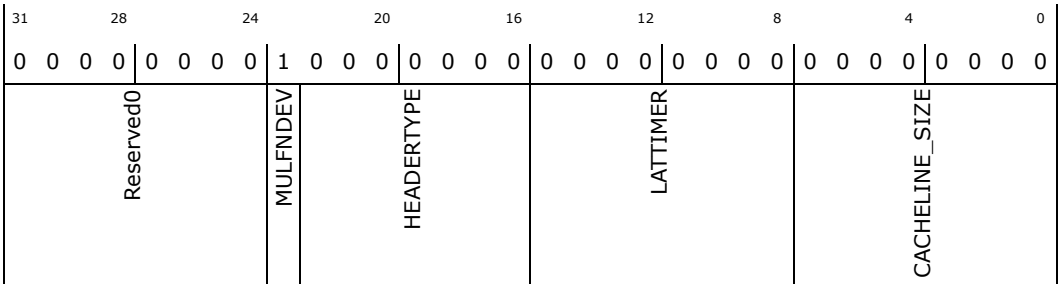
3.46.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:30, F:3] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

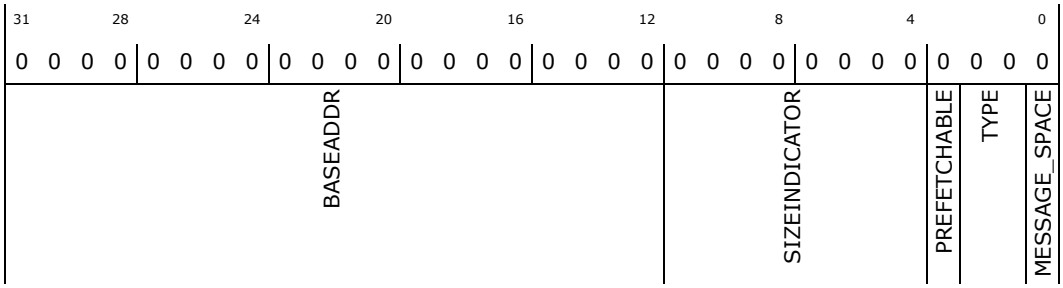
3.46.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

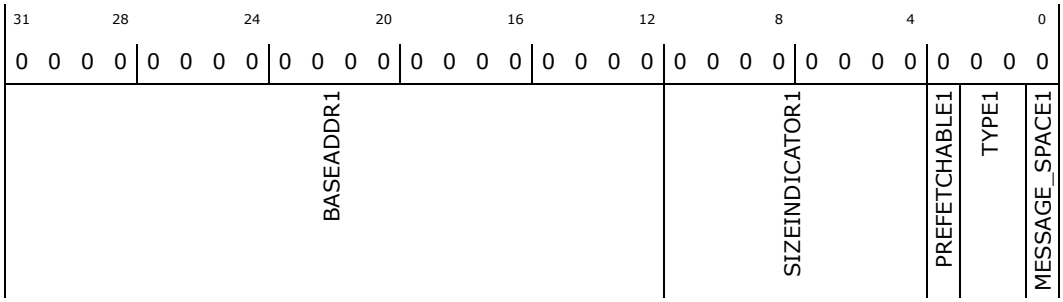
3.46.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:30, F:3] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

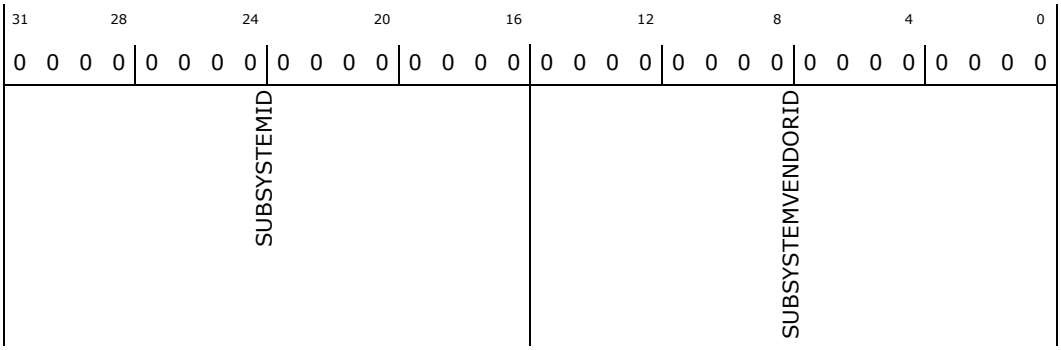
3.46.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:30, F:3] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

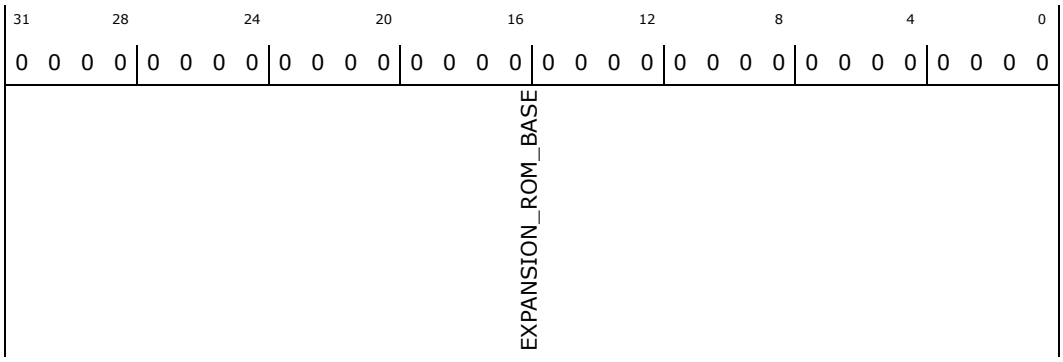
3.46.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:30, F:3] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

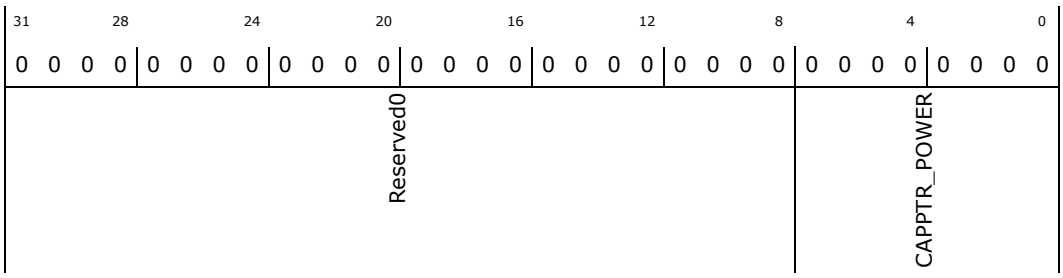
3.46.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:30, F:3] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

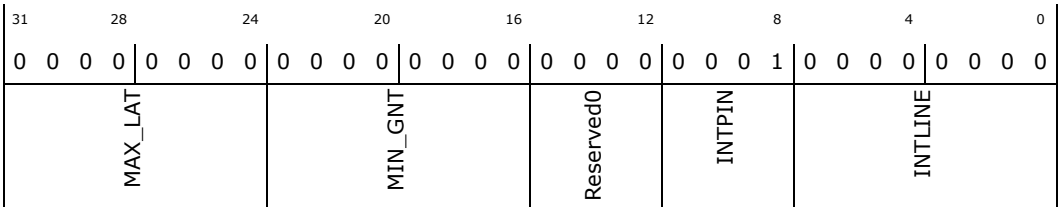
3.46.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:30, F:3] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

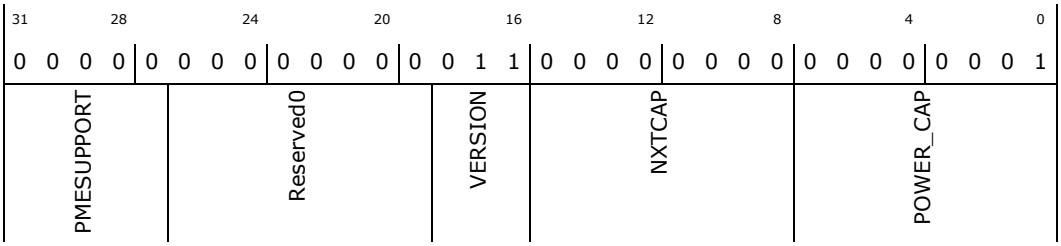
3.46.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:30, F:3] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

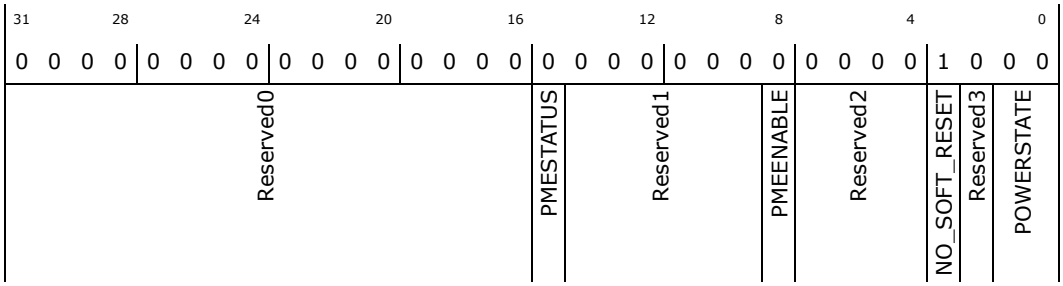
3.46.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:30, F:3] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

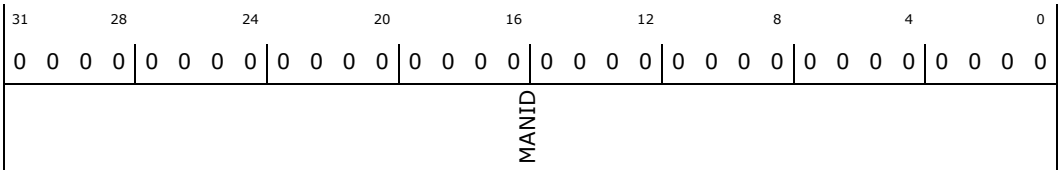
3.46.13 Manufacturer ID (MANID)—Offset F8h

Access Method

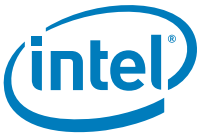
Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:30, F:3] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.



3.47 SIO HSUART1 Memory Mapped I/O Registers

Table 55. Summary of SIO HSUART1 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"Receive Buffer Register/Transmit Holding Register/Divisor Latch (Low) (RBR_THR_DLL)—Offset 0h" on page 2921	00000000h
4h	4	"Divisor Latch (High)/ Interrupt Enable Register (IER_DLH)—Offset 4h" on page 2922	00000000h
8h	4	"Interrupt Identification Register and FIFO Control Register (IIR_FCR)—Offset 8h" on page 2923	00000001h
Ch	4	"Line Control Register (LCR)—Offset Ch" on page 2924	00000000h
10h	4	"Modem Control Register (MCR)—Offset 10h" on page 2925	00000000h
14h	4	"Line Status Register (LSR)—Offset 14h" on page 2927	00000060h
18h	4	"Modem Status Register (MSR)—Offset 18h" on page 2930	00000000h
1Ch	4	"Scratchpad Register (SCR)—Offset 1Ch" on page 2931	00000000h
30h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h" on page 2932	00000000h
34h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h" on page 2933	00000000h
38h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h" on page 2933	00000000h
3Ch	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch" on page 2934	00000000h
40h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h" on page 2935	00000000h
44h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h" on page 2935	00000000h
48h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h" on page 2936	00000000h
4Ch	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch" on page 2936	00000000h
50h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h" on page 2937	00000000h
54h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h" on page 2937	00000000h
58h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h" on page 2938	00000000h
5Ch	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch" on page 2939	00000000h
60h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h" on page 2939	00000000h
64h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h" on page 2940	00000000h

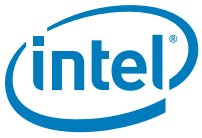


Table 55. Summary of SIO HSUART1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
68h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h" on page 2940	00000000h
6Ch	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch" on page 2941	00000000h
70h	4	"FIFO Access Register (FAR)—Offset 70h" on page 2941	00000000h
74h	4	"Transmit FIFO Read (TFR)—Offset 74h" on page 2942	00000000h
78h	4	"Receive FIFO Write (RFW)—Offset 78h" on page 2943	00000000h
7Ch	4	"UART Status Register (USR)—Offset 7Ch" on page 2943	00000006h
80h	4	"Transmit FIFO Level (TFL)—Offset 80h" on page 2944	00000000h
84h	4	"Receive FIFO Level (RFL)—Offset 84h" on page 2945	00000000h
88h	4	"Software Reset Register (SRR)—Offset 88h" on page 2945	00000000h
8Ch	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 2946	00000000h
90h	4	"Shadow Break Control Register (SBCR)—Offset 90h" on page 2947	00000000h
94h	4	"Shadow DMA Mode (SDMAM)—Offset 94h" on page 2948	00000000h
98h	4	"Shadow FIFO Enable (SFE)—Offset 98h" on page 2948	00000000h
9Ch	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 2946	00000000h
A0h	4	"Shadow TX Empty Trigger (STET)—Offset A0h" on page 2949	00000000h
A4h	4	"Halt TX (HTX)—Offset A4h" on page 2950	00000000h
A8h	4	"DMA Software Acknowledge (DMASA)—Offset A8h" on page 2951	00000000h
F4h	4	"Component Parameter Register (CPR)—Offset F4h" on page 2951	00043F32h
F8h	4	"UART Component Version (UCV)—Offset F8h" on page 2953	3330382Ah
FCh	4	"Component Type Register (CTR)—Offset FCh" on page 2953	44570110h
800h	4	"Private Clock Params (PRV_CLOCK_PARAMS)—Offset 800h" on page 2954	00000000h
804h	4	"Software Resets (RESETS)—Offset 804h" on page 2954	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 2955	00000050h
818h	4	"UART_BYTE_COUNT—Offset 818h" on page 2956	00000000h
820h	4	"UART_OVERFLOW_INTR_STAT—Offset 820h" on page 2957	00000000h

3.47.1 Receive Buffer Register/Transmit Holding Register/ Divisor Latch (Low) (RBR_THR_DLL)—Offset 0h

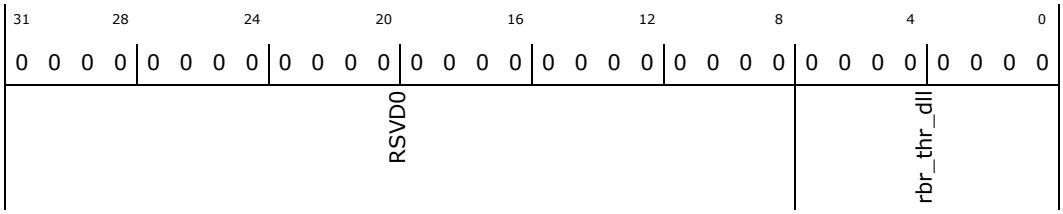
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RBR_THR_DLL: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**rbr_thr_dll:** Can be referred to 3 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more.

3.47.2 Divisor Latch (High)/ Interrupt Enable Register (IER_DLH)—Offset 4h

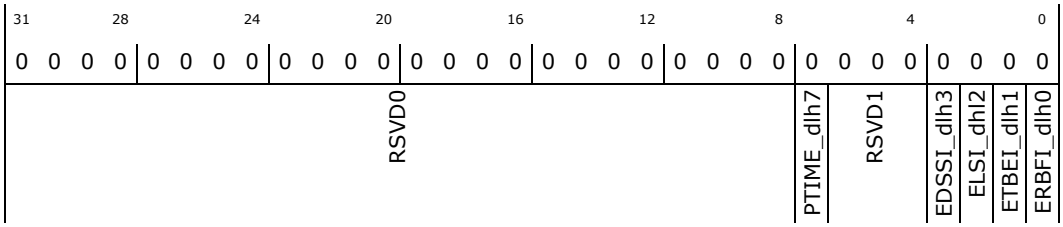
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IER_DLH: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**PTIME_dlh7:** Can be referred to 2 registers with different descriptions - go to Synopsys DesignWare DW_apb_uart Databook Spec to learn more.
6:4	0b RO	**RSVD1:** Reserved
3	0h RW	**EDSSI_dlh3:** Can be referred to 2 registers with different descriptions - go to Synopsys DesignWare DW_apb_uart Databook Spec to learn more.
2	0h RW	**ELSI_dhl2:** Can be referred to 2 registers with different descriptions - go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more.
1	0h RW	**ETBEI_dlh1:** Can be referred to 2 registers with different descriptions - go to Synopsys DesignWare DW_apb_uart Databook Spec to learn more.
0	0h RW	**ERBFI_dlh0:** Can be referred to 2 registers with different descriptions - go to Synopsys DesignWare DW_apb_uart Databook Spec to learn more.

3.47.3 Interrupt Identification Register and FIFO Control Register (IIR_FCR)—Offset 8h

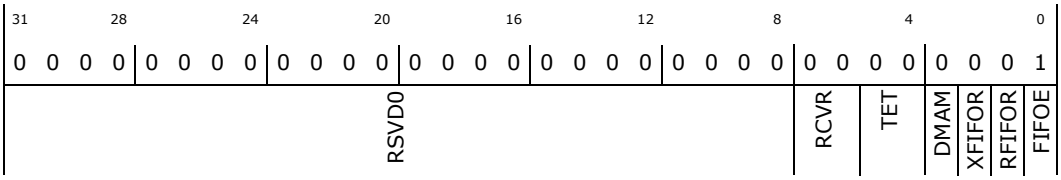
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IIR_FCR: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:6	0h RW	**FIFOSE_RCVR (RCVR):** RCVR Trigger. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. For details on DMA support, refer to DMA Support on page 43. The following trigger levels are supported: • 00 = 1 character in the FIFO • 01 = FIFO full • 10 = FIFO full • 11 = FIFO 2 less than full Reset Value: 0x0
5:4	0h RW	**Res_TET (TET):** TX Empty Trigger. Writes have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. For details on DMA support, refer to DMA Support on page 43. The following trigger levels are supported: • 00 = FIFO empty • 01 = 2 characters in the FIFO • 10 = FIFO full • 11 = FIFO full Reset Value: 0x0
3	0h RW	**IID3_DMAM (DMAM):** DMA Mode. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == No). For details on DMA support, refer to DMA Support on page 43. • 0 = mode 0 • 1 = mode 1 Reset Value: 0x0

Bit Range	Default & Access	Description
2	0h RW	**IID2_XFIFOR (XFIFOR):** XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
1	0h RW	**IID1_RFIFOR (RFIFOR):** RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
0	1h RW	**FIFO Enable (FIFOE):** This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset. Reset Value: 0x0

3.47.4 Line Control Register (LCR)—Offset Ch

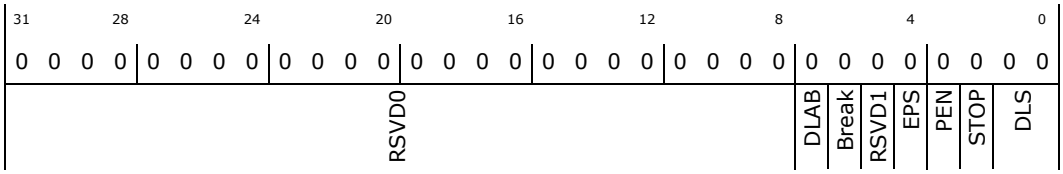
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LCR: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**Divisor Latch Access Bit (DLAB):** If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This bit is used to enable reading and writing of the Divisor Latch register(DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. Reset Value: 0x0
6	0h RW	**Break Control Bit (Break):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low. Reset Value: 0x0

Bit Range	Default & Access	Description
5	0b RO	**RSVD1:** Reserved
4	0h RW	**Even Parity Select (EPS):** If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked. Reset Value: 0x0
3	0h RW	**Parity Enable (PEN):** If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero) -- otherwise always writable, always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. • 0 = parity disabled • 1 = parity enabled Reset Value: 0x0
2	0h RW	**Number of Stop Bits (STOP):** If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. • 0 = 1 stop bit • 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit Reset Value: 0x0
1:0	0h RW	**Data Length Select (DLS):** If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero) -- otherwise always writable, always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected are as follows: • 00 = 5 bits • 01 = 6 bits • 10 = 7 bits • 11 = 8 bits Reset Value: 0x0

3.47.5 Modem Control Register (MCR)—Offset 10h

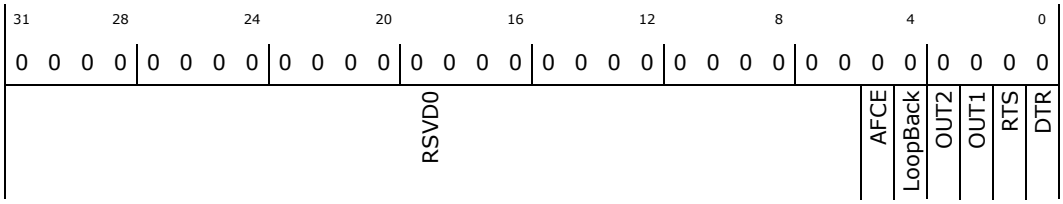
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MCR: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RO	**RSVD0:** Reserved
5	0h RW	**Auto Flow Control Enable (AFCE):** Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in Auto Flow Control on page 37. • 0 = Auto Flow Control Mode disabled • 1 = Auto Flow Control Mode enabled Reset Value: 0x0
4	0h RW	**LoopBack Bit (LoopBack):** This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line. Reset Value: 0x0
3	0h RW	**Output2 (OUT2):** This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: • 0 = out2_n de-asserted (logic 1) • 1 = out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
2	0h RW	**Output1 (OUT1):** This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: • 0 = out1_n de-asserted (logic 1) • 1 = out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0

Bit Range	Default & Access	Description
1	0h RW	**Request to Send (RTS):** This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
0	0h RW	**Data Terminal Ready (DTR):** This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: • 0 = dtr_n de-asserted (logic 1) • 1 = dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0

3.47.6 Line Status Register (LSR)—Offset 14h

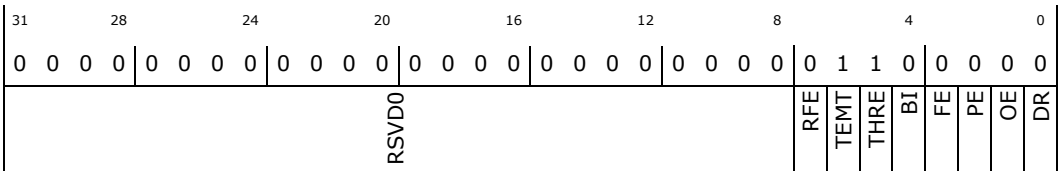
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LSR: [BAR] + 14h

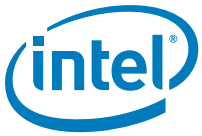
BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000060h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
7	0h RW	**Receiver FIFO Error Bit (RFE):** This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. • 0 = no error in RX FIFO • 1 = error in RX FIFO This bit is cleared when the LSR is read, the character with the error is at the top of the receiver FIFO, and there are no subsequent errors in the FIFO. Reset Value: 0x0
6	1h RW	**Transmitter Empty Bit (TEMT):** If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty. Reset Value: 0x1
5	1h RW	**Transmit Holding Register Empty Bit (THRE):** If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting. For more details, see Programmable THRE Interrupt on page 40. Reset Value: 0x1
4	0h RW	**Break Interrupt Bit (BI):** This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Reset Value: 0x0



Bit Range	Default & Access	Description
3	0h RW	**Framing Error Bit (FE):** This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to re synchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). • 0 = no framing error • 1 = framing error Reading the LSR clears the FE bit. Reset Value: 0x0
2	0h RW	**Parity Error Bit (PE):** This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). • 0 = no parity error • 1 = parity error Reading the LSR clears the PE bit. Reset Value: 0x0
1	0h RW	**Overrun Error Bit (OE):** This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. • 0 = no overrun error • 1 = overrun error Reading the LSR clears the OE bit. Reset Value: 0x0
0	0h RW	**Data Ready Bit (DR):** This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. • 0 = no data ready • 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode. Reset Value: 0x0

3.47.7 Modem Status Register (MSR)—Offset 18h

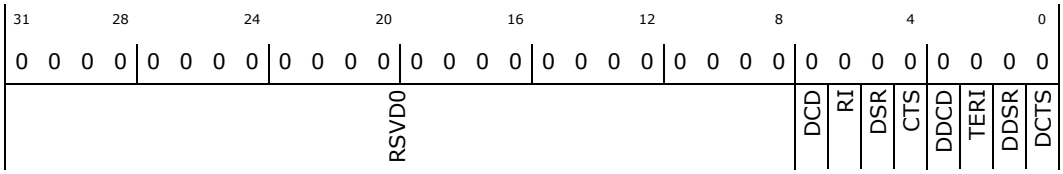
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MSR: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**Data Carrier Detect (DCD):** This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted, it is an indication that the carrier has been detected by the modem or data set. • 0 = dcd_n input is de-asserted (logic 1) • 1 = dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Reset Value: 0x0
6	0h RW	**Ring Indicator (RI):** This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. • 0 = ri_n input is de-asserted (logic 1) • 1 = ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Reset Value: 0x0
5	0h RW	**Data Set Ready (DSR):** This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. • 0 = dsr_n input is de-asserted (logic 1) • 1 = dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Reset Value: 0x0
4	0h RW	**Clear to Send (CTS):** This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted, it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. • 0 = cts_n input is de-asserted (logic 1) • 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). Reset Value: 0x0

Bit Range	Default & Access	Description
3	0h RW	**Delta Data Carrier Detect (DDCD):** This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. • 0 = no change on dcd_n since last read of MSR • 1 = change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. Reset Value: 0x0
2	0h RW	**Trailing Edge of Ring Indicator (TERI):** This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. • 0 = no change on ri_n since last read of MSR • 1 = change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Reset Value: 0x0
1	0h RW	**Delta Data Set Ready (DDSR):** This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. • 0 = no change on dsr_n since last read of MSR • 1 = change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. Reset Value: 0x0
0	0h RW	**Delta Clear to Send (DCTS):** This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. • 0 = no change on cts_n since last read of MSR • 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note that if the DCTS bit is not set, the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. Reset Value: 0x0

3.47.8 Scratchpad Register (SCR)—Offset 1Ch

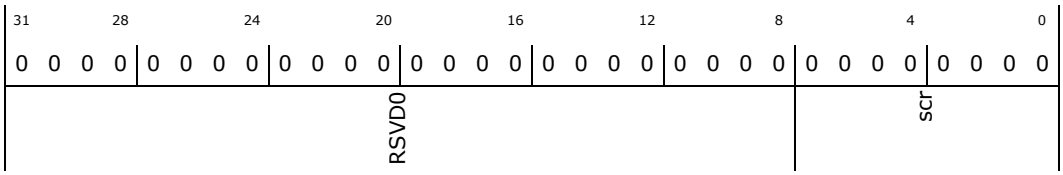
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SCR: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**scr:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart. Reset Value: 0x0

3.47.9 Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h

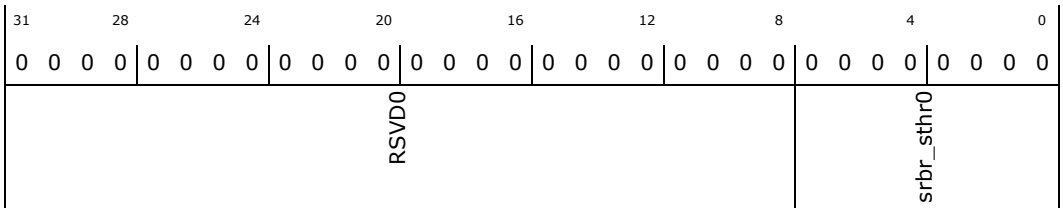
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR0: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
7:0	0h RW	**srbr_sthr0:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data are lost. An overrun error also occurs. Reset Value: 0x0

3.47.10 Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

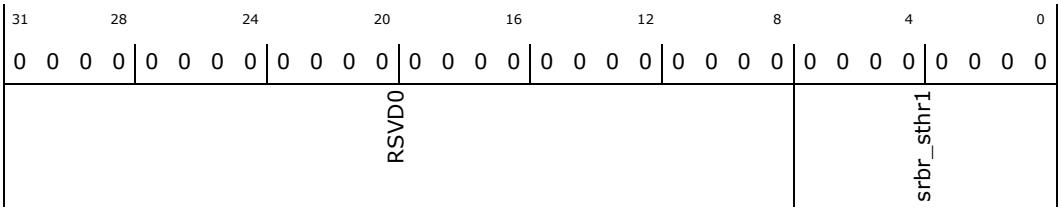
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR1: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr1:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.11 Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

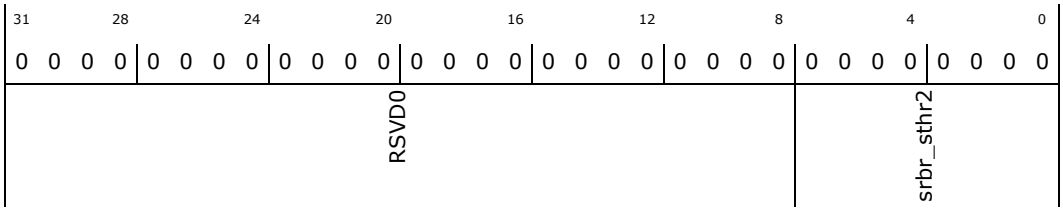
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR2: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr2:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.12 Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

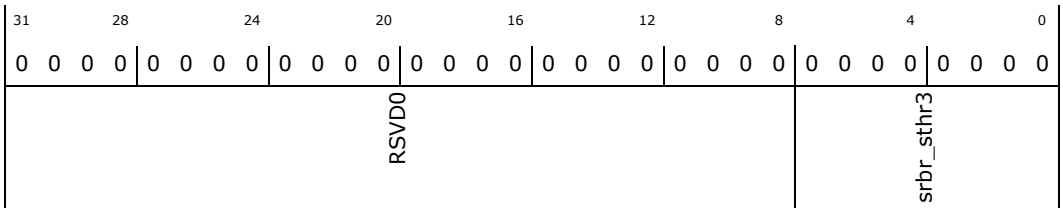
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR3: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr3:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.13 Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

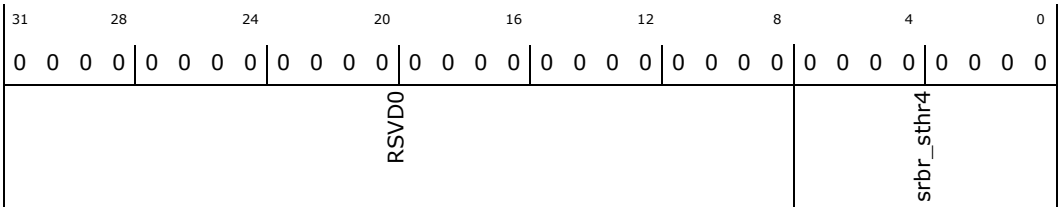
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR4: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr4:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.14 Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

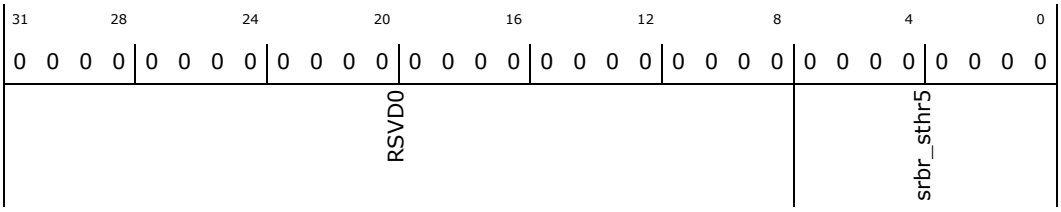
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR5: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
7:0	0h RW	**srbr_sthr5:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.15 Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

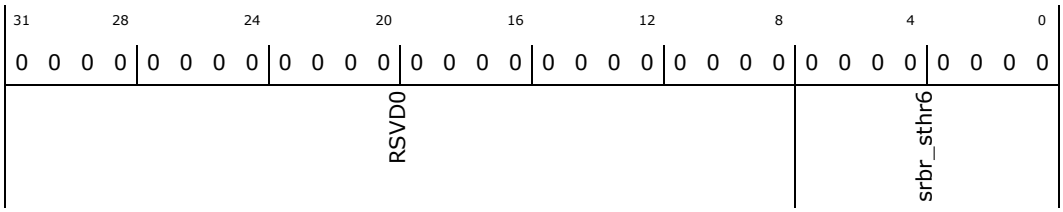
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR6: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr6:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.16 Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

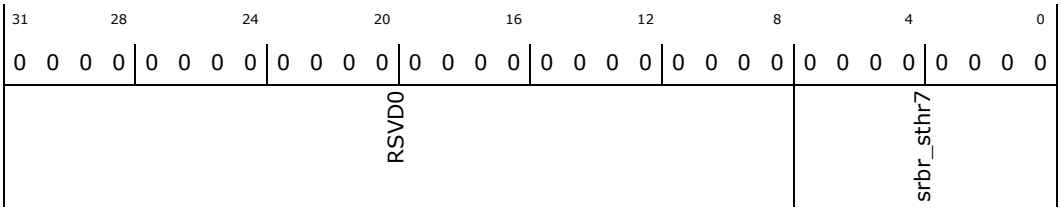
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR7: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr7:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.17 Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

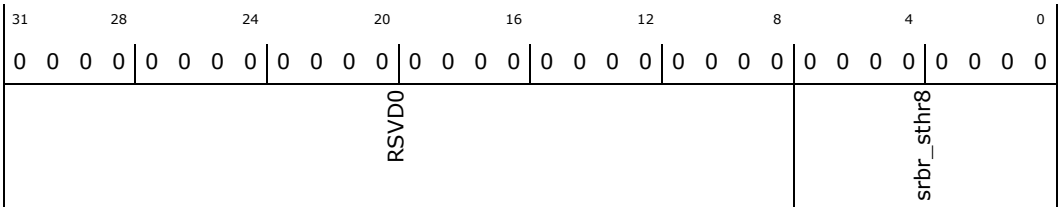
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR8: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr8:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.18 Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

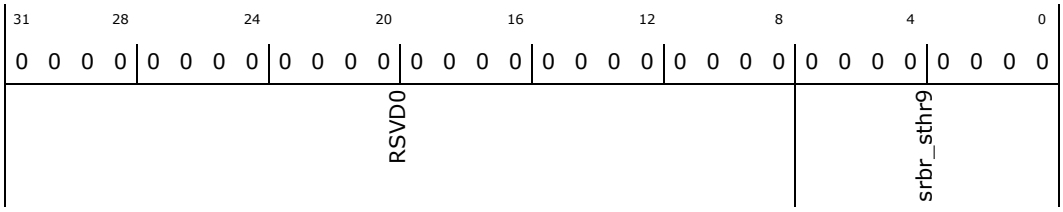
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR9: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr9:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.19 Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

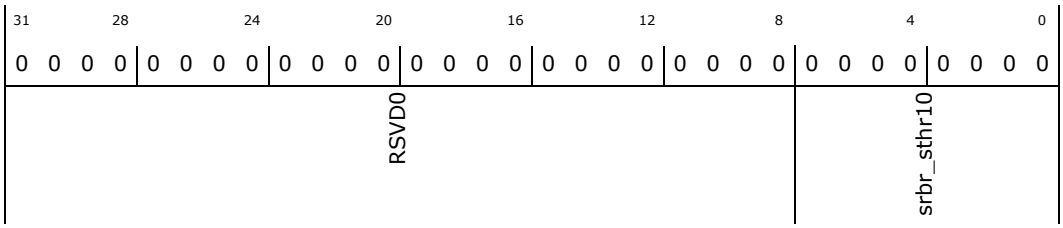
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR10: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr10:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.20 Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

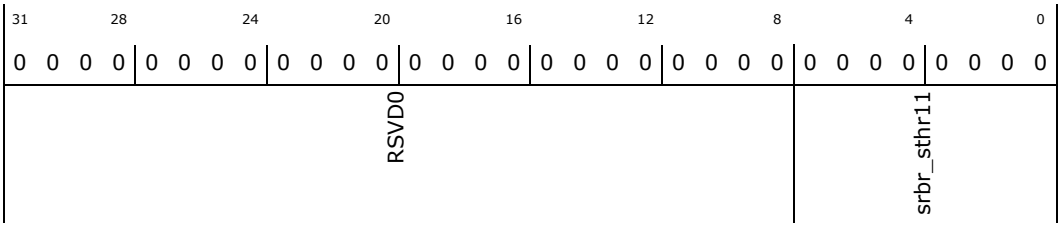
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR11: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr11:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.21 Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

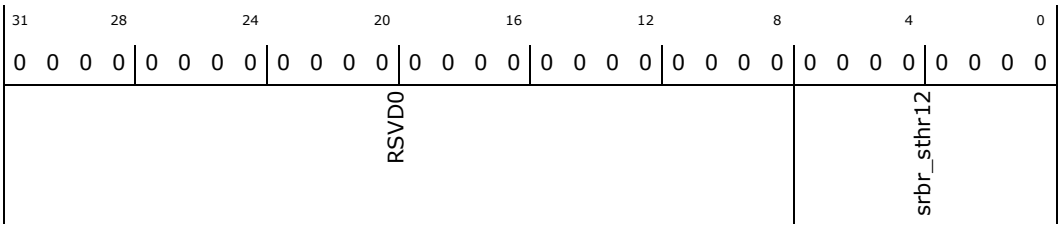
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR12: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr12:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.22 Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

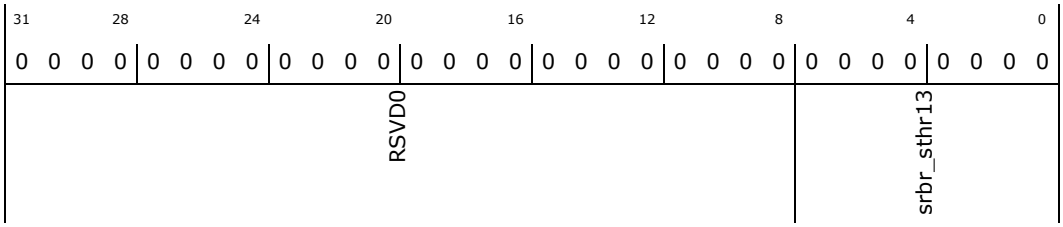
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR13: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr13:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.23 Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

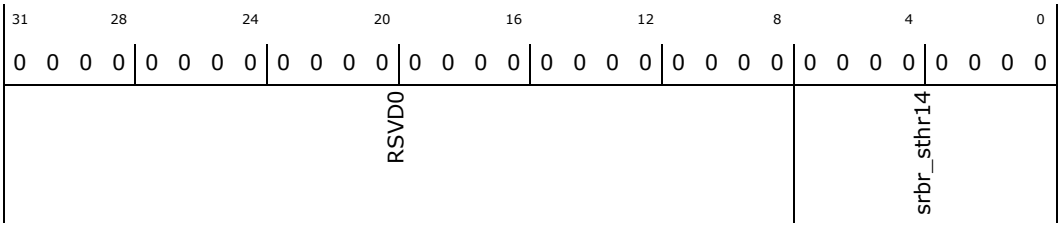
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR14: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr14:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.24 Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

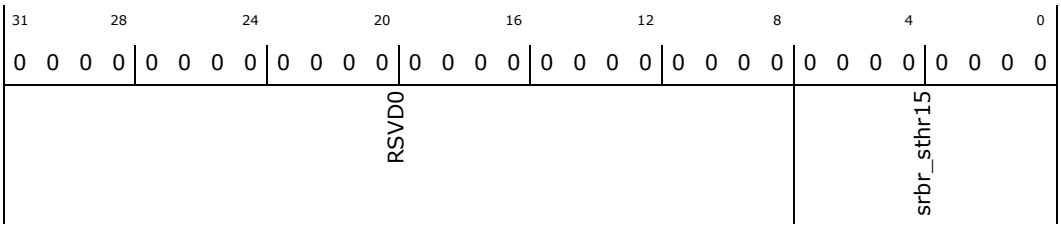
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR15: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr15:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.47.25 FIFO Access Register (FAR)—Offset 70h

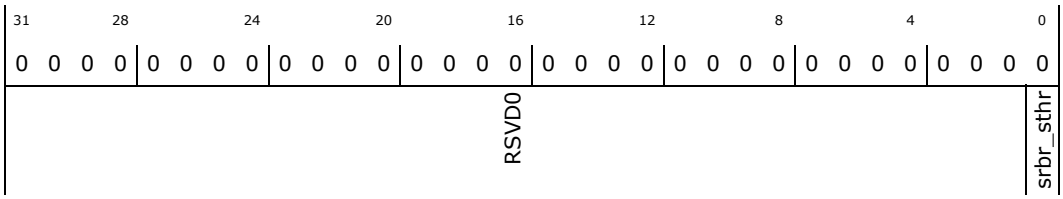
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FAR: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**srbr_sthr:** Writes have no effect when FIFO_ACCESS == No, always readable. This register is used to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. • 0 = FIFO access mode disabled • 1 = FIFO access mode enabled Note that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

3.47.26 Transmit FIFO Read (TFR)—Offset 74h

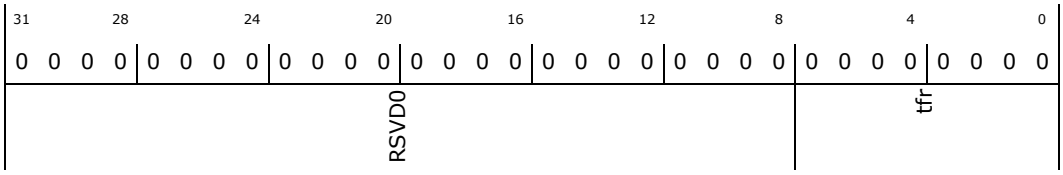
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TFR: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**Transmit FIFO Read (tfr):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

3.47.27 Receive FIFO Write (RFW)—Offset 78h

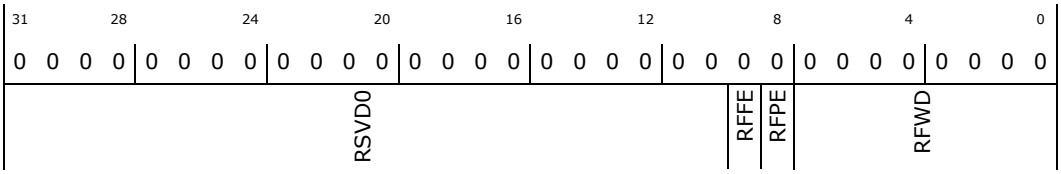
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RFW: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0b RO	**RSVD0:** Reserved
9	0h RW	**Receive FIFO Framing Error (RFFE):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR. Reset Value: 0x0
8	0h RW	**Receive FIFO Parity Error (RFPE):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR. Reset Value: 0x0
7:0	0h RW	**Receive FIFO Write Data (RFWD):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR. Reset Value: 0x0

3.47.28 UART Status Register (USR)—Offset 7Ch

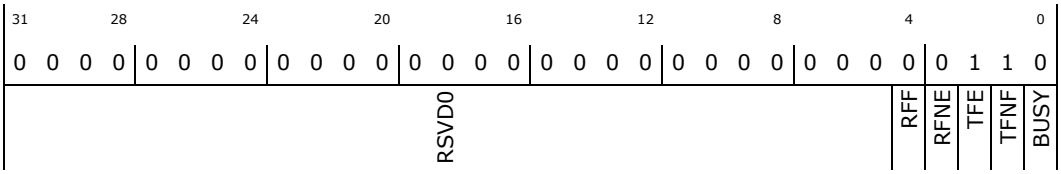
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

USR: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:5	0b RO	**RSVD0:** Reserved
4	0h RW	**Receive FIFO Full (RFF):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. • 0 = Receive FIFO not full • 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full. Reset Value: 0x0
3	0h RW	**Receive FIFO Not Empty (RFNE):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. • 0 = Receive FIFO is empty • 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty. Reset Value: 0x0
2	1h RW	**Transmit FIFO Empty (TFE):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. • 0 = Transmit FIFO is not empty • 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty. Reset Value: 0x1
1	1h RW	**Transmit FIFO Not Full (TFNF):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. • 0 = Transmit FIFO is full • 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full. Reset Value: 0x1
0	0h RW	**UART Busy (BUSY):** This bit is valid only when UART_16550_COMPATIBLE == NO and indicates that a serial transfer is in progress, ; when cleared, indicates that the DW_apb_uart is idle or inactive. • 0 = DW_apb_uart is idle or inactive • 1 = DW_apb_uart is busy (actively transferring data) NOTE: It is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the DW_apb_uart has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the DW_apb_uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock. Reset Value: 0x0

3.47.29 Transmit FIFO Level (TFL)—Offset 80h

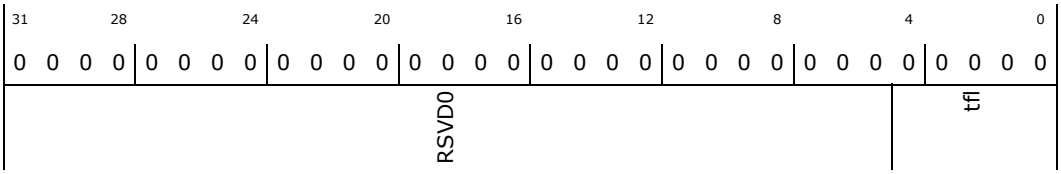
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TFL: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RO	**RSVD0:** Reserved
4:0	0h RW	**Transmit FIFO Level (tfl):** This indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

3.47.30 Receive FIFO Level (RFL)—Offset 84h

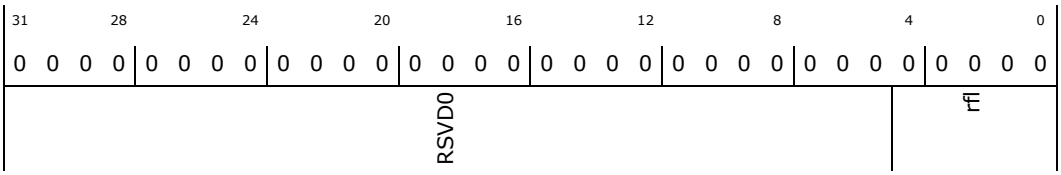
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RFL: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RO	**RSVD0:** Reserved
4:0	0h RW	**Receive FIFO Level (rfl):** This indicates the number of data entries in the receive FIFO. Reset Value: 0x0

3.47.31 Software Reset Register (SRR)—Offset 88h

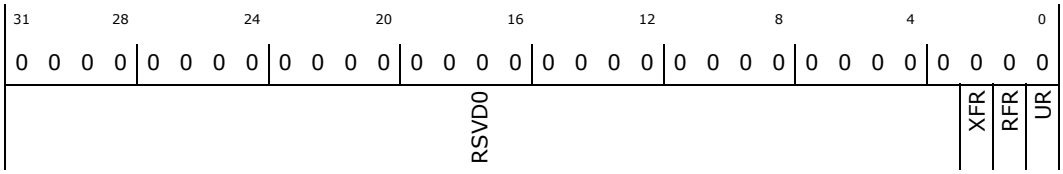
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRR: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RO	**RSVD0:** Reserved
2	0h RW	**XMIT FIFO Reset (XFR):** This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.
1	0h RW	**RCVR FIFO Reset (RFR):** This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.
0	0h RW	**UART Reset (UR):** This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset. Reset Value: 0x0

3.47.32 Shadow Request to Send (SRTS)—Offset 8Ch

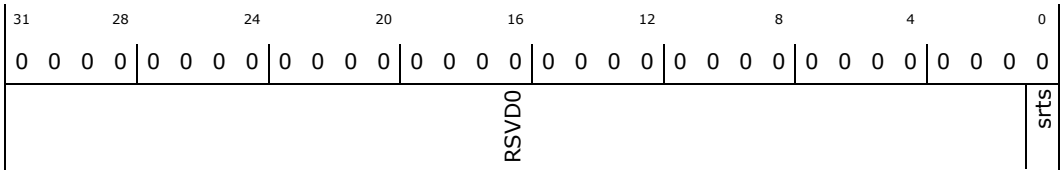
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRTS: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow Request to Send (srts):** This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

3.47.33 Shadow Break Control Register (SBCR)—Offset 90h

This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] = 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver. Reset Value: 0x0

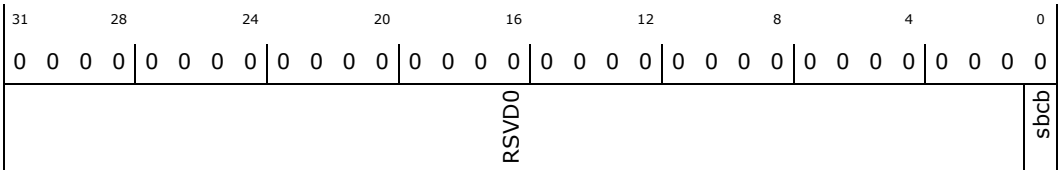
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SBCR: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow Break Control Bit (sbcb):** Reserved.

3.47.34 Shadow DMA Mode (SDMAM)—Offset 94h

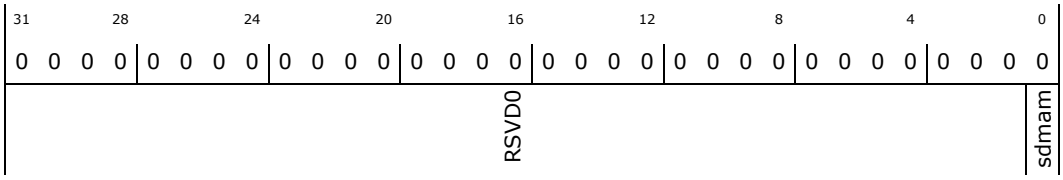
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SDMAM: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow DMA Mode (sdmam):** This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). • 0 = mode 0 • 1 = mode 1 Reset Value: 0x0

3.47.35 Shadow FIFO Enable (SFE)—Offset 98h

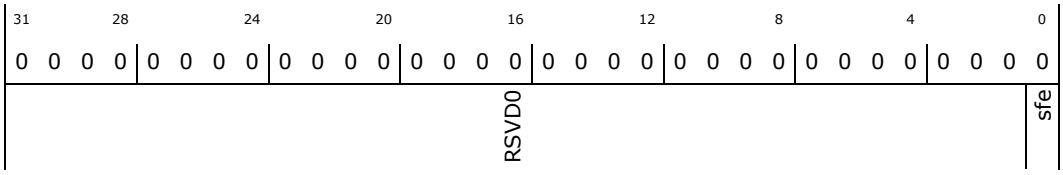
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFE: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
0	0h RW	**Shadow FIFO Enable (sfe):** This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

3.47.36 Shadow RCVR Trigger (SRT)—Offset 9Ch

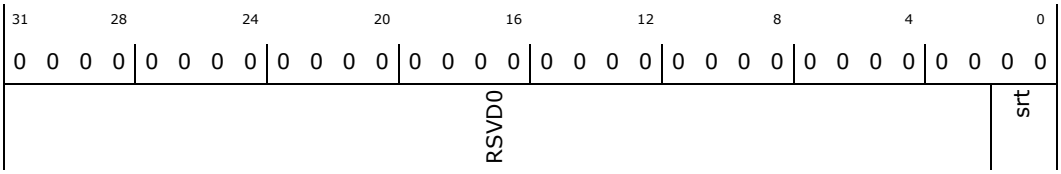
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRT: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1:0	0h RW	**Shadow RCVR Trigger (srt):** This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: • 00 = 1 character in the FIFO • 01 = FIFO full • 10 = FIFO full • 11 = FIFO 2 less than full Reset Value: 0x0

3.47.37 Shadow TX Empty Trigger (STET)—Offset A0h

This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated.

This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported:

- 00 = FIFO empty
- 01 = 2 characters in the FIFO
- 10 = FIFO full
- 11 = FIFO full

Reset Value: 0x0 Dependencies: Writes have no effect when THRE_MODE_USER == Disabled.

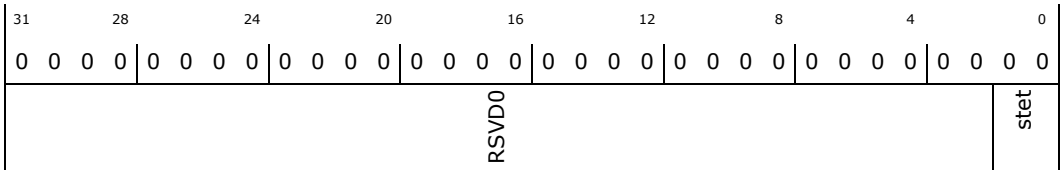
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STET: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1:0	0h RW	**stet:** Shadow TX Empty Trigger

3.47.38 Halt TX (HTX)—Offset A4h

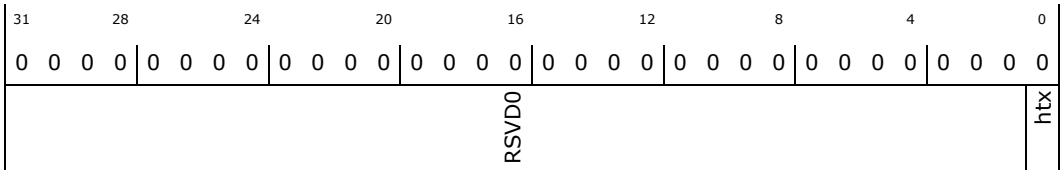
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HTX: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**htx:** This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. • 0 = Halt TX disabled • 1 = Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.

3.47.39 DMA Software Acknowledge (DMASA)—Offset A8h

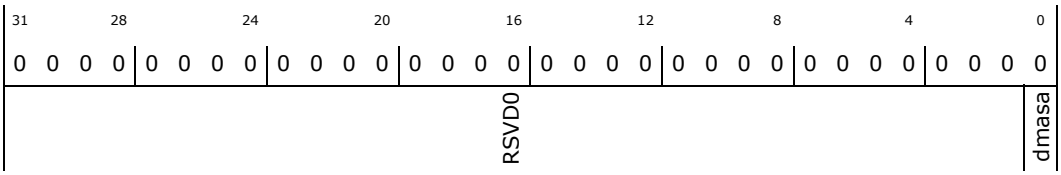
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMASA: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**dmasa:** This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when DMA_EXTRA == No.

3.47.40 Component Parameter Register (CPR)—Offset F4h

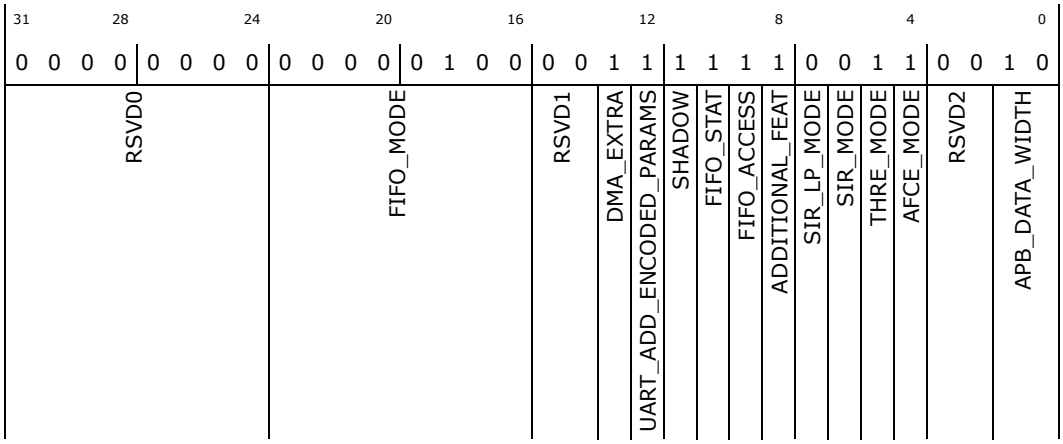
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CPR: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00043F32h



Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved
23:16	4h RO	**FIFO MODE (FIFO_MODE):** • 0x00 = 0 • 0x01 = 16 • 0x02 = 32 • to • 0x80 = 2048 • 0x81- 0xff = reserved
15:14	0b RO	**RSVD1:** Reserved
13	1h RO	**DMA EXTRA (DMA_EXTRA):** • 0 = FALSE • 1 = TRUE
12	1h RO	**UART ADD ENCODED PARAMS (UART_ADD_ENCODED_PARAMS):** • 0 = FALSE, • 1 = TRUE
11	1h RO	**SHADOW:** • 0 = FALSE, • 1 = TRUE
10	1h RO	**FIFO STAT (FIFO_STAT):** • 0 = FALSE, • 1 = TRUE
9	1h RO	**FIFO ACCESS (FIFO_ACCESS):** • 0 = FALSE, • 1 = TRUE
8	1h RO	**ADDITIONAL FEAT (ADDITIONAL_FEAT):** • 0 = FALSE, • 1 = TRUE
7	0h RO	**SIR LP MODE (SIR_LP_MODE):** • 0 = FALSE, • 1 = TRUE

Bit Range	Default & Access	Description
6	0h RO	**SIR MODE (SIR_MODE):** • 0 = FALSE, • 1 = TRUE
5	1h RO	**THRE MODE (THRE_MODE):** • 0 = FALSE, • 1 = TRUE
4	1h RO	**AFCE MODE (AFCE_MODE):** • 0 = FALSE, • 1 = TRUE
3:2	0b RO	**RSVD2:** Reserved
1:0	2h RO	**APB DATA WIDTH (APB_DATA_WIDTH):** • 00 = 8 bits • 01 = 16 bits • 10 = 32 bits • 11 = reserved

3.47.41 UART Component Version (UCV)—Offset F8h

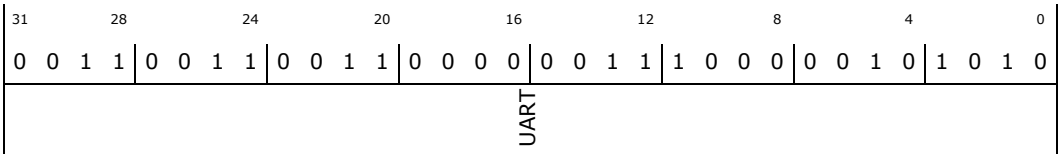
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

UCV: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 3330382Ah



Bit Range	Default & Access	Description
31:0	3330382ah RO	**UART:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*. Reset Value: See the releases table in the AMBA 2 release notes.

3.47.42 Component Type Register (CTR)—Offset FCh

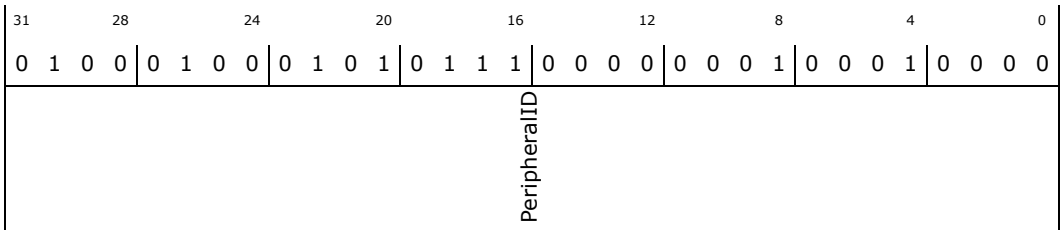
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTR: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 44570110h



Bit Range	Default & Access	Description
31:0	44570110h RO	**Peripheral ID (PeripheralID):** This register contains the peripherals identification code. Reset Value: 0x44570110

3.47.43 Private Clock Params (PRV_CLOCK_PARAMS)—Offset 800h

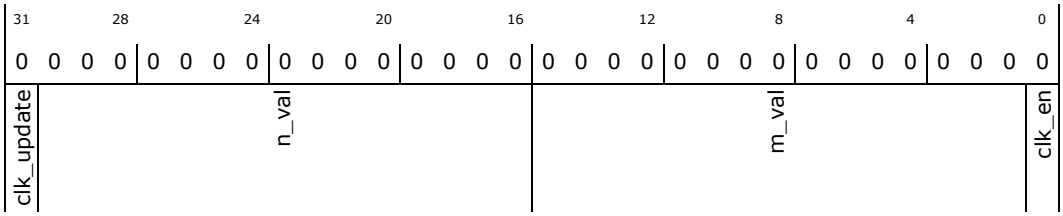
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRV_CLOCK_PARAMS: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**clk_update:** update the clock divider after setting new m and n values
30:16	0h RW	**N_VAL (n_val):** n value for the m over n divider
15:1	0h RW	**M_VAL (m_val):** m value for the m over n divider
0	0h RW	**clk_en:** clk en of the m over n divider

3.47.44 Software Resets (RESETS)—Offset 804h

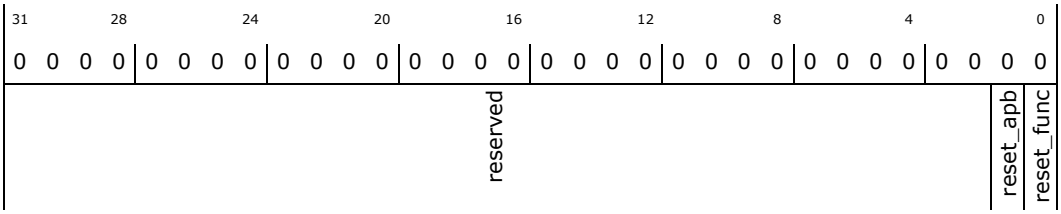
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.47.45 General Purpose Register (GENERAL)—Offset 808h

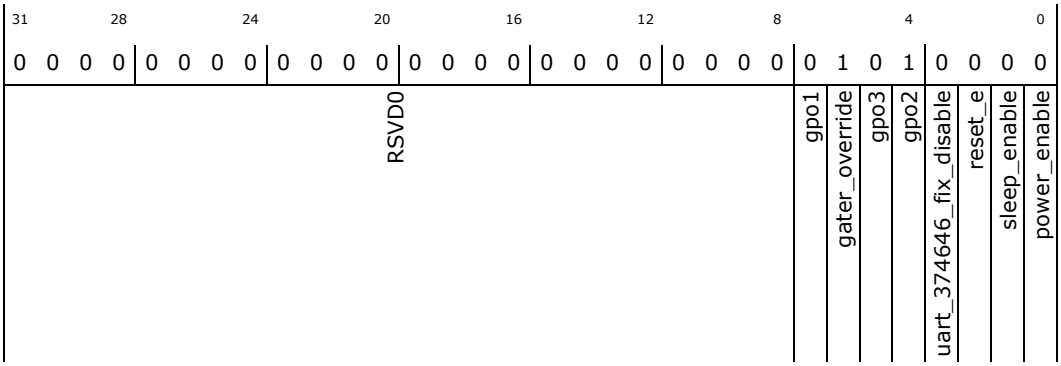
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000050h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
7	0h RW	**gpo1:** not applicable
6	1h RW	**gater_override:** not applicable
5	0h RW	**gpo3:** not applicable
4	1h RW	**gpo2:** This bit indicates whether the UART clock req will be dynamic or controlled by the UART clock en: • 1 = controlled by the clk en • 0 = dynamic Default value = 1
3	0h RW	**uart_374646_fix_disable:** Disable rts_n override
2	0h RW	**reset_e:** not applicable
1	0h RW	**sleep_enable:** not applicable
0	0h RW	**power_enable:** not applicable

3.47.46 UART_BYTE_COUNT—Offset 818h

Transaction counter

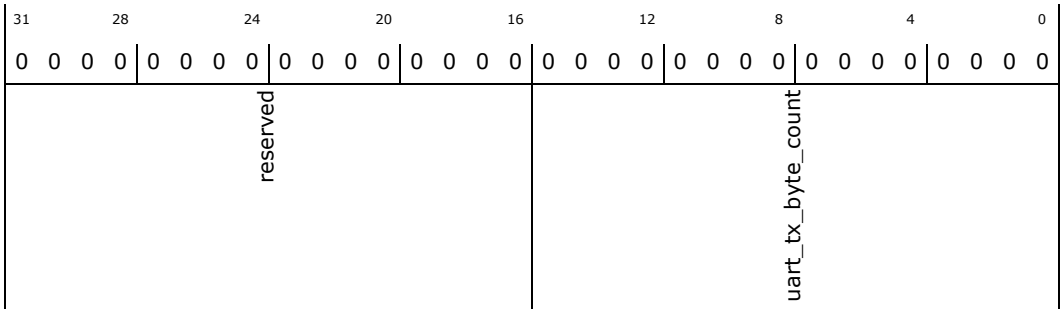
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

UART_BYTE_COUNT: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**reserved (reserved):** reserved

Bit Range	Default & Access	Description
15:0	0h RO	**uart_tx_byte_count:** UART transaction counter

3.47.47 UART_OVERFLOW_INTR_STAT—Offset 820h

Overflow interrupt

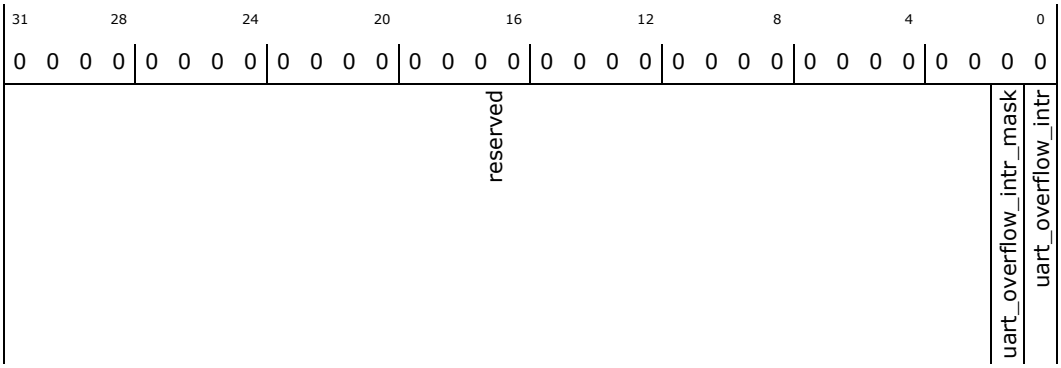
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

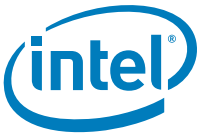
UART_OVERFLOW_INTR_STAT: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**reserved:** reserved
1	0h RW	**uart1_overflow_intr_mask (uart_overflow_intr_mask):** Mask the overflow into
0	0h RO	**uart_overflow_intr:** Indicate there was count overflow



3.48 SIO HSUART2 PCI Configuration Registers

Table 56. Summary of HSUART2 PCI Configuration Registers—0/30/4

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2958	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 2959	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 2960	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 2961	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 2962	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 2962	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 2963	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2964	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 2964	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2965	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 2965	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2966	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 2967	00000000h

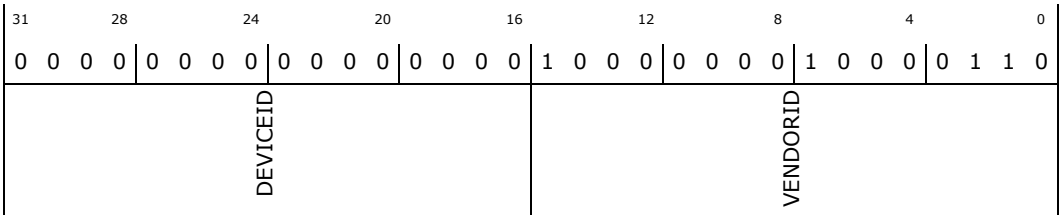
3.48.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:30, F:4] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

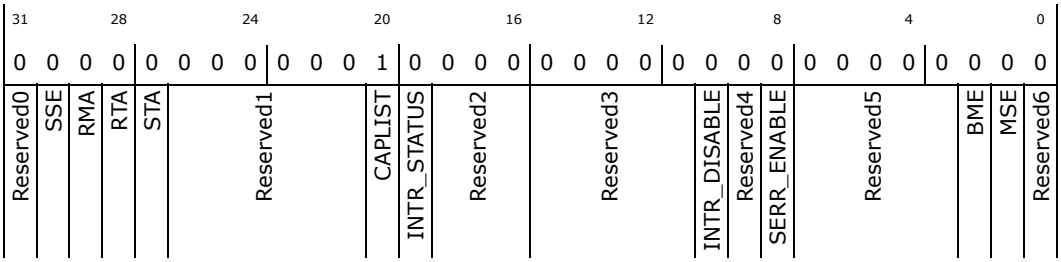
3.48.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:30, F:4] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

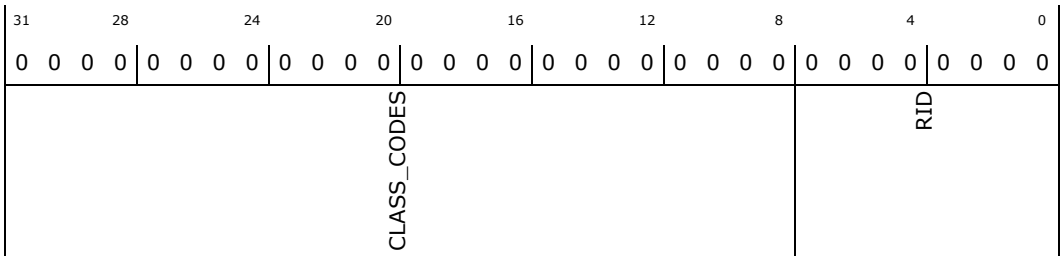
3.48.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:30, F:4] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

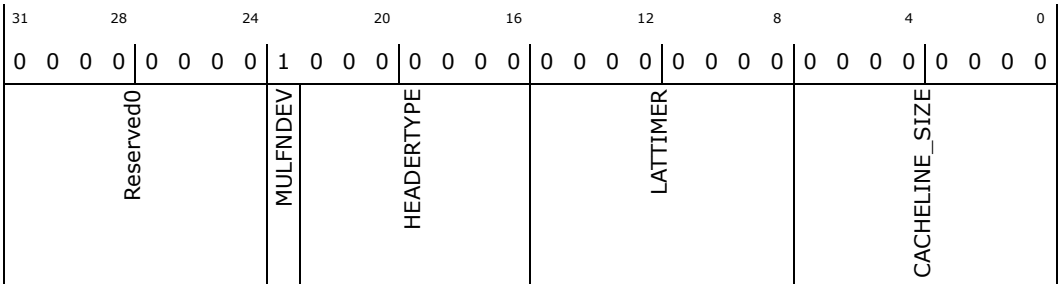
3.48.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:30, F:4] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

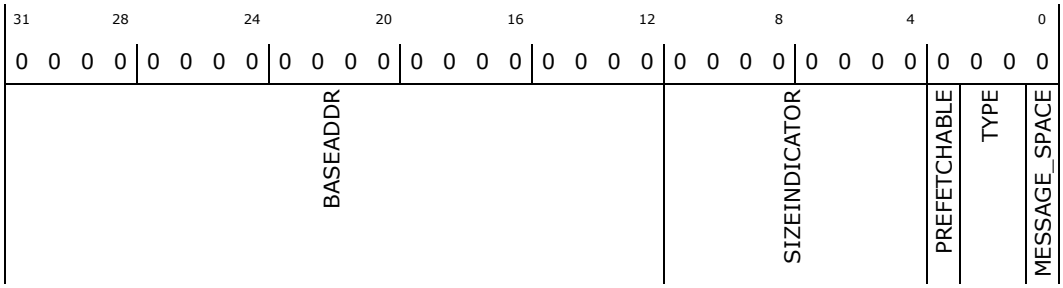
3.48.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

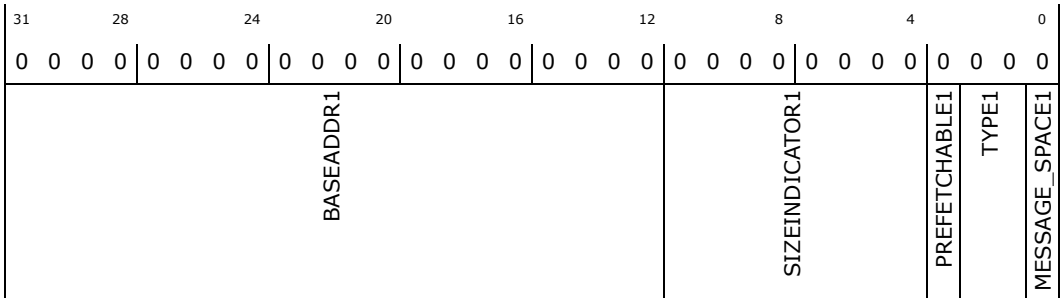
3.48.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:30, F:4] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

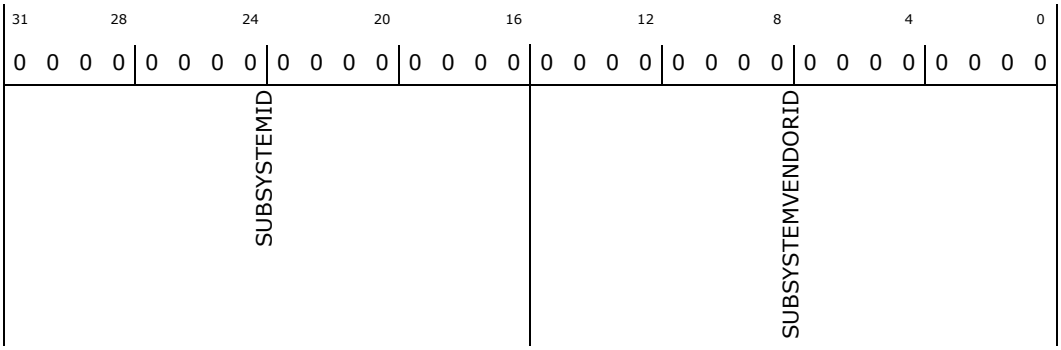
3.48.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:30, F:4] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

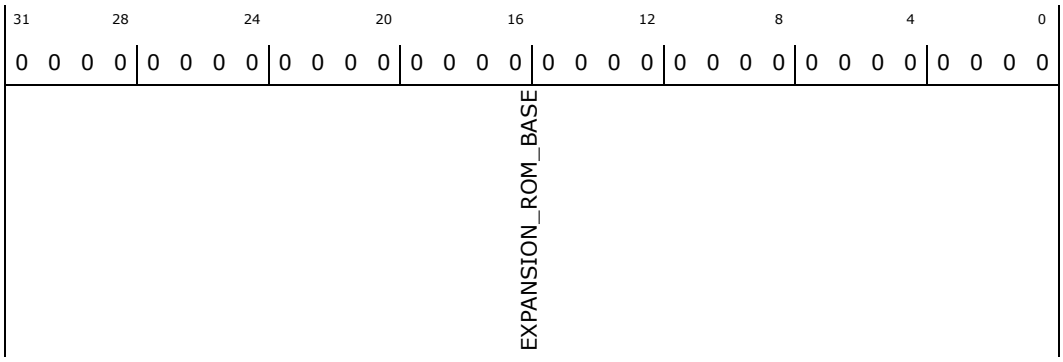
3.48.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:30, F:4] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

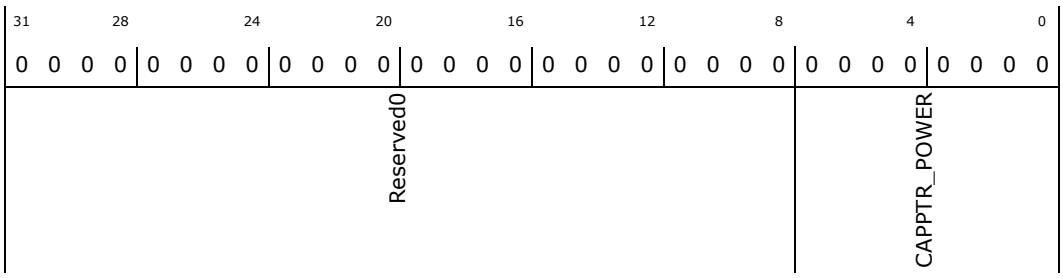
3.48.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:30, F:4] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

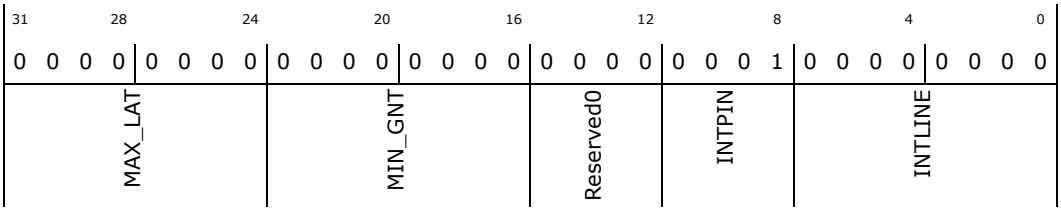
3.48.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:30, F:4] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

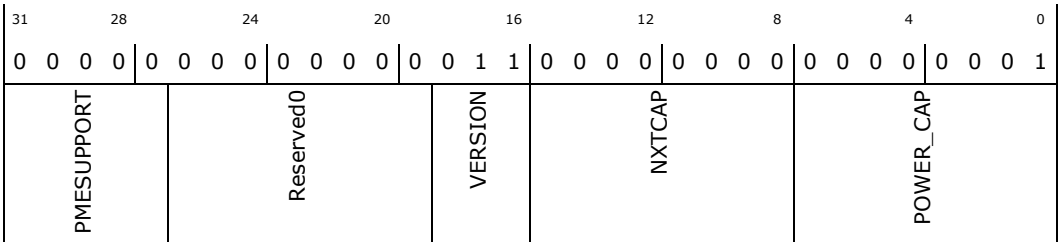
3.48.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:30, F:4] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

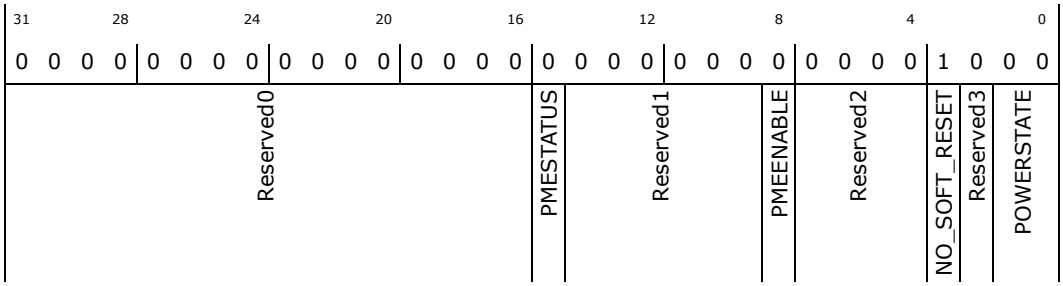
3.48.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:30, F:4] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

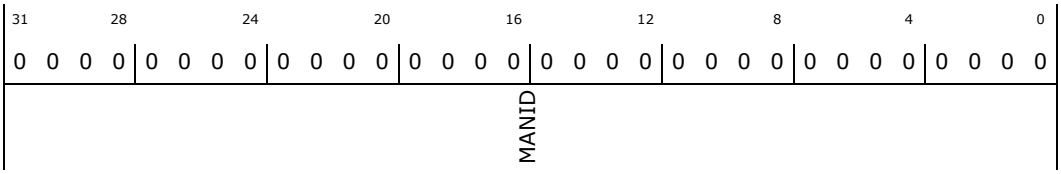
3.48.13 Manufacturer ID (MANID)—Offset F8h

Access Method

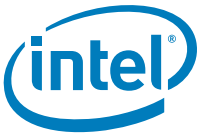
Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:30, F:4] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.



3.49 SIO HSUART2 Memory Mapped I/O Registers

Table 57. Summary of HSUART2 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"Receive Buffer Register/Transmit Holding Register/Divisor Latch (Low) (RBR_THR_DLL)—Offset 0h" on page 2969	00000000h
4h	4	"Divisor Latch (High)/ Interrupt Enable Register (IER_DLH)—Offset 4h" on page 2970	00000000h
8h	4	"Interrupt Identification Register and FIFO Control Register (IIR_FCR)—Offset 8h" on page 2971	00000001h
Ch	4	"Line Control Register (LCR)—Offset Ch" on page 2972	00000000h
10h	4	"Modem Control Register (MCR)—Offset 10h" on page 2973	00000000h
14h	4	"Line Status Register (LSR)—Offset 14h" on page 2975	00000060h
18h	4	"Modem Status Register (MSR)—Offset 18h" on page 2978	00000000h
1Ch	4	"Scratchpad Register (SCR)—Offset 1Ch" on page 2979	00000000h
30h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h" on page 2980	00000000h
34h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h" on page 2981	00000000h
38h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h" on page 2981	00000000h
3Ch	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch" on page 2982	00000000h
40h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h" on page 2983	00000000h
44h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h" on page 2983	00000000h
48h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h" on page 2984	00000000h
4Ch	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch" on page 2984	00000000h
50h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h" on page 2985	00000000h
54h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h" on page 2985	00000000h
58h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h" on page 2986	00000000h
5Ch	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch" on page 2987	00000000h
60h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h" on page 2987	00000000h
64h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h" on page 2988	00000000h

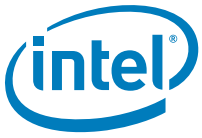


Table 57. Summary of HSUART2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
68h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h" on page 2988	00000000h
6Ch	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch" on page 2989	00000000h
70h	4	"FIFO Access Register (FAR)—Offset 70h" on page 2989	00000000h
74h	4	"Transmit FIFO Read (TFR)—Offset 74h" on page 2990	00000000h
78h	4	"Receive FIFO Write (RFW)—Offset 78h" on page 2991	00000000h
7Ch	4	"UART Status Register (USR)—Offset 7Ch" on page 2991	00000006h
80h	4	"Transmit FIFO Level (TFL)—Offset 80h" on page 2992	00000000h
84h	4	"Receive FIFO Level (RFL)—Offset 84h" on page 2993	00000000h
88h	4	"Software Reset Register (SRR)—Offset 88h" on page 2993	00000000h
8Ch	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 2994	00000000h
90h	4	"Shadow Break Control Register (SBCR)—Offset 90h" on page 2995	00000000h
94h	4	"Shadow DMA Mode (SDMAM)—Offset 94h" on page 2996	00000000h
98h	4	"Shadow FIFO Enable (SFE)—Offset 98h" on page 2996	00000000h
9Ch	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 2994	00000000h
A0h	4	"Shadow TX Empty Trigger (STET)—Offset A0h" on page 2997	00000000h
A4h	4	"Halt TX (HTX)—Offset A4h" on page 2998	00000000h
A8h	4	"DMA Software Acknowledge (DMASA)—Offset A8h" on page 2999	00000000h
F4h	4	"Component Parameter Register (CPR)—Offset F4h" on page 2999	00043F32h
F8h	4	"UART Component Version (UCV)—Offset F8h" on page 3001	3330382Ah
FCh	4	"Component Type Register (CTR)—Offset FCh" on page 3001	44570110h
800h	4	"Private Clock Params (PRV_CLOCK_PARAMS)—Offset 800h" on page 3002	00000000h
804h	4	"Software Resets (RESETS)—Offset 804h" on page 3002	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 3003	00000050h
818h	4	"UART_BYTE_COUNT—Offset 818h" on page 3004	00000000h
820h	4	"UART_OVERFLOW_INTR_STAT—Offset 820h" on page 3005	00000000h

3.49.1 Receive Buffer Register/Transmit Holding Register/ Divisor Latch (Low) (RBR_THR_DLL)—Offset 0h

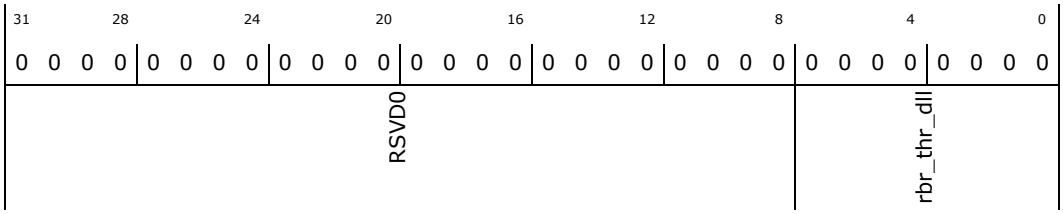
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RBR_THR_DLL: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**rbr_thr_dll:** Can be referred to 3 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more.

3.49.2 Divisor Latch (High)/ Interrupt Enable Register (IER_DLH)—Offset 4h

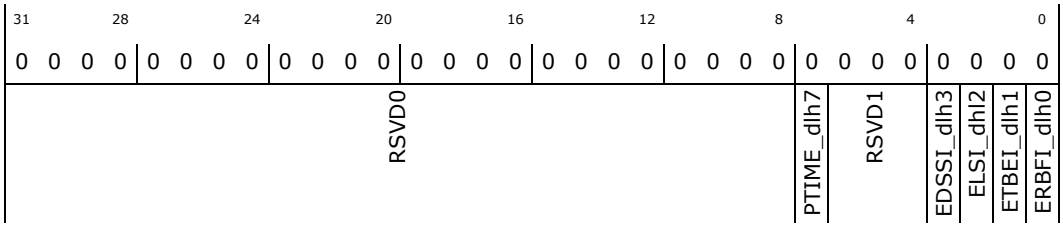
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IER_DLH: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**PTIME_dlh7:** Can be referred to 2 registers with different descriptions - go to Synopsys DesignWare DW_apb_uart Databook Spec to learn more.
6:4	0b RO	**RSVD1:** Reserved
3	0h RW	**EDSSI_dlh3:** Can be referred to 2 registers with different descriptions - go to Synopsys DesignWare DW_apb_uart Databook Spec to learn more.
2	0h RW	**ELSI_dhl2:** Can be referred to 2 registers with different descriptions - go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more.
1	0h RW	**ETBEI_dlh1:** Can be referred to 2 registers with different descriptions - go to Synopsys DesignWare DW_apb_uart Databook Spec to learn more.
0	0h RW	**ERBFI_dlh0:** Can be referred to 2 registers with different descriptions - go to Synopsys DesignWare DW_apb_uart Databook Spec to learn more.

3.49.3 Interrupt Identification Register and FIFO Control Register (IIR_FCR)—Offset 8h

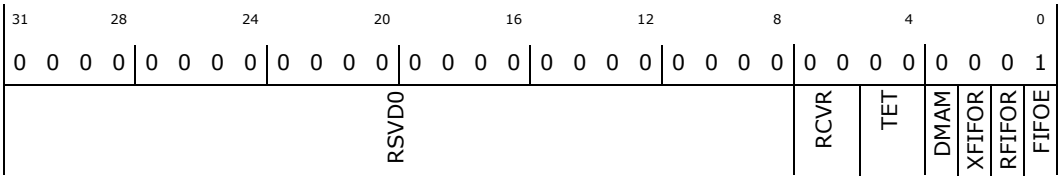
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IIR_FCR: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:6	0h RW	**FIFOSE_RCVR (RCVR):** RCVR Trigger. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. For details on DMA support, refer to DMA Support on page 43. The following trigger levels are supported: • 00 = 1 character in the FIFO • 01 = FIFO full • 10 = FIFO full • 11 = FIFO 2 less than full Reset Value: 0x0
5:4	0h RW	**Res_TET (TET):** TX Empty Trigger. Writes have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. For details on DMA support, refer to DMA Support on page 43. The following trigger levels are supported: • 00 = FIFO empty • 01 = 2 characters in the FIFO • 10 = FIFO full • 11 = FIFO full Reset Value: 0x0
3	0h RW	**IID3_DMAM (DMAM):** DMA Mode. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == No). For details on DMA support, refer to DMA Support on page 43. • 0 = mode 0 • 1 = mode 1 Reset Value: 0x0

Bit Range	Default & Access	Description
2	0h RW	**IID2_XFIFOR (XFIFOR):** XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
1	0h RW	**IID1_RFIFOR (RFIFOR):** RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
0	1h RW	**FIFO Enable (FIFOE):** This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset. Reset Value: 0x0

3.49.4 Line Control Register (LCR)—Offset Ch

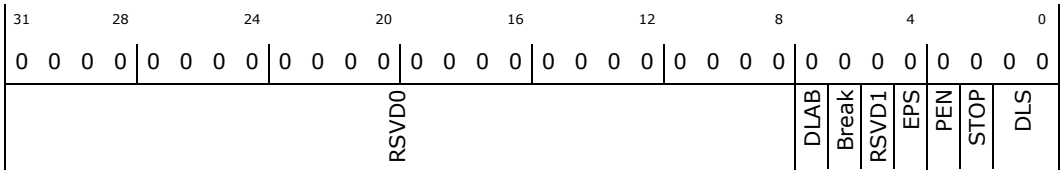
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LCR: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**Divisor Latch Access Bit (DLAB):** If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This bit is used to enable reading and writing of the Divisor Latch register(DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. Reset Value: 0x0
6	0h RW	**Break Control Bit (Break):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low. Reset Value: 0x0

Bit Range	Default & Access	Description
5	0b RO	**RSVD1:** Reserved
4	0h RW	**Even Parity Select (EPS):** If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked. Reset Value: 0x0
3	0h RW	**Parity Enable (PEN):** If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero) -- otherwise always writable, always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. • 0 = parity disabled • 1 = parity enabled Reset Value: 0x0
2	0h RW	**Number of Stop Bits (STOP):** If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. • 0 = 1 stop bit • 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit Reset Value: 0x0
1:0	0h RW	**Data Length Select (DLS):** If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero) -- otherwise always writable, always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected are as follows: • 00 = 5 bits • 01 = 6 bits • 10 = 7 bits • 11 = 8 bits Reset Value: 0x0

3.49.5 Modem Control Register (MCR)—Offset 10h

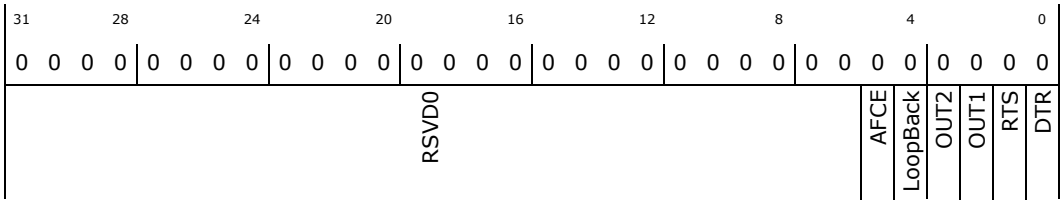
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MCR: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RO	**RSVD0:** Reserved
5	0h RW	**Auto Flow Control Enable (AFCE):** Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in Auto Flow Control on page 37. • 0 = Auto Flow Control Mode disabled • 1 = Auto Flow Control Mode enabled Reset Value: 0x0
4	0h RW	**LoopBack Bit (LoopBack):** This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line. Reset Value: 0x0
3	0h RW	**Output2 (OUT2):** This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: • 0 = out2_n de-asserted (logic 1) • 1 = out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
2	0h RW	**Output1 (OUT1):** This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: • 0 = out1_n de-asserted (logic 1) • 1 = out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0

Bit Range	Default & Access	Description
1	0h RW	**Request to Send (RTS):** This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
0	0h RW	**Data Terminal Ready (DTR):** This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: • 0 = dtr_n de-asserted (logic 1) • 1 = dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0

3.49.6 Line Status Register (LSR)—Offset 14h

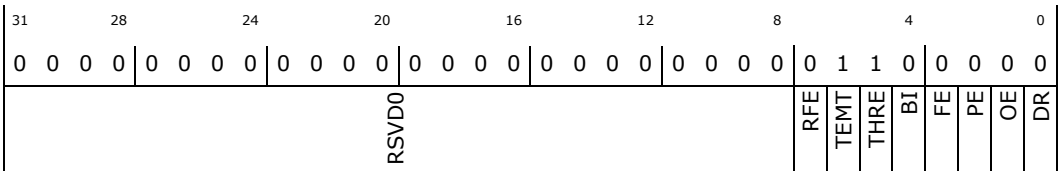
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LSR: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000060h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
7	0h RW	**Receiver FIFO Error Bit (RFE):** This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. • 0 = no error in RX FIFO • 1 = error in RX FIFO This bit is cleared when the LSR is read, the character with the error is at the top of the receiver FIFO, and there are no subsequent errors in the FIFO. Reset Value: 0x0
6	1h RW	**Transmitter Empty Bit (TEMT):** If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty. Reset Value: 0x1
5	1h RW	**Transmit Holding Register Empty Bit (THRE):** If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting. For more details, see Programmable THRE Interrupt on page 40. Reset Value: 0x1
4	0h RW	**Break Interrupt Bit (BI):** This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Reset Value: 0x0

Bit Range	Default & Access	Description
3	0h RW	**Framing Error Bit (FE):** This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). • 0 = no framing error • 1 = framing error Reading the LSR clears the FE bit. Reset Value: 0x0
2	0h RW	**Parity Error Bit (PE):** This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). • 0 = no parity error • 1 = parity error Reading the LSR clears the PE bit. Reset Value: 0x0
1	0h RW	**Overrun Error Bit (OE):** This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. • 0 = no overrun error • 1 = overrun error Reading the LSR clears the OE bit. Reset Value: 0x0
0	0h RW	**Data Ready Bit (DR):** This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. • 0 = no data ready • 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode. Reset Value: 0x0

3.49.7 Modem Status Register (MSR)—Offset 18h

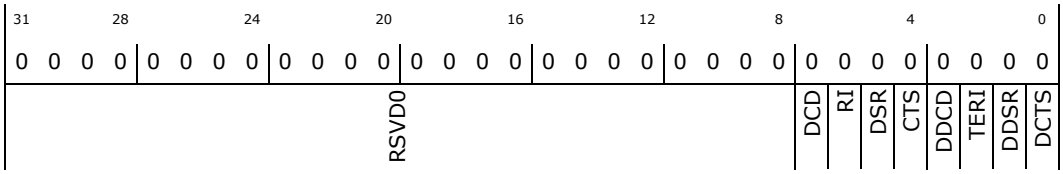
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MSR: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**Data Carrier Detect (DCD):** This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted, it is an indication that the carrier has been detected by the modem or data set. • 0 = dcd_n input is de-asserted (logic 1) • 1 = dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Reset Value: 0x0
6	0h RW	**Ring Indicator (RI):** This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. • 0 = ri_n input is de-asserted (logic 1) • 1 = ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Reset Value: 0x0
5	0h RW	**Data Set Ready (DSR):** This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. • 0 = dsr_n input is de-asserted (logic 1) • 1 = dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Reset Value: 0x0
4	0h RW	**Clear to Send (CTS):** This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted, it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. • 0 = cts_n input is de-asserted (logic 1) • 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). Reset Value: 0x0

Bit Range	Default & Access	Description
3	0h RW	**Delta Data Carrier Detect (DDCD):** This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. • 0 = no change on dcd_n since last read of MSR • 1 = change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. Reset Value: 0x0
2	0h RW	**Trailing Edge of Ring Indicator (TERI):** This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. • 0 = no change on ri_n since last read of MSR • 1 = change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Reset Value: 0x0
1	0h RW	**Delta Data Set Ready (DDSR):** This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. • 0 = no change on dsr_n since last read of MSR • 1 = change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. Reset Value: 0x0
0	0h RW	**Delta Clear to Send (DCTS):** This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. • 0 = no change on cts_n since last read of MSR • 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note that if the DCTS bit is not set, the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. Reset Value: 0x0

3.49.8 Scratchpad Register (SCR)—Offset 1Ch

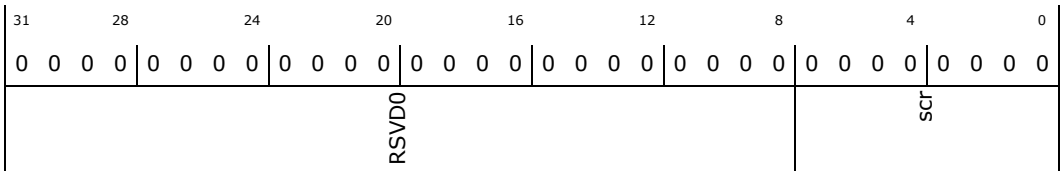
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SCR: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**scr:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart. Reset Value: 0x0

3.49.9 Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h

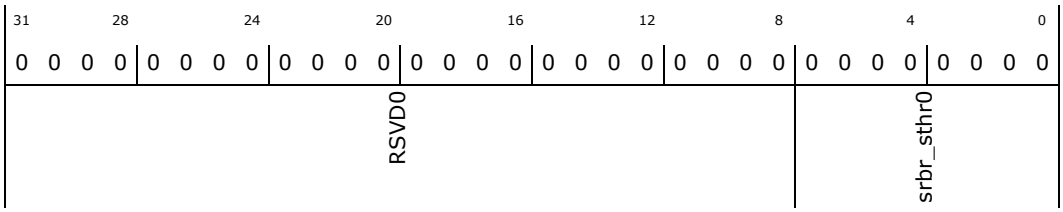
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR0: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
7:0	0h RW	**srbr_sthr0:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data are lost. An overrun error also occurs. Reset Value: 0x0

3.49.10 Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

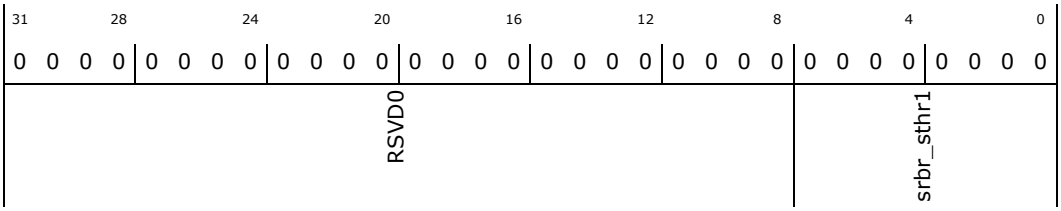
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR1: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr1:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.11 Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

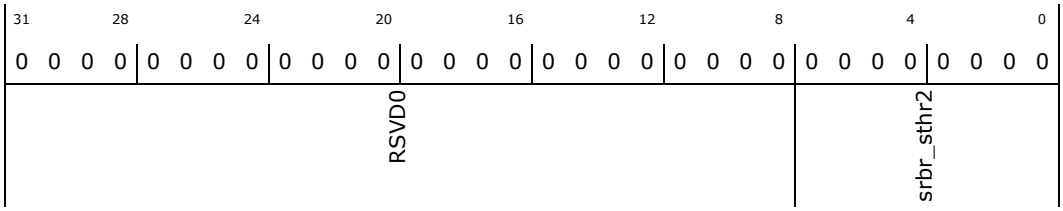
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR2: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr2:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.12 Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

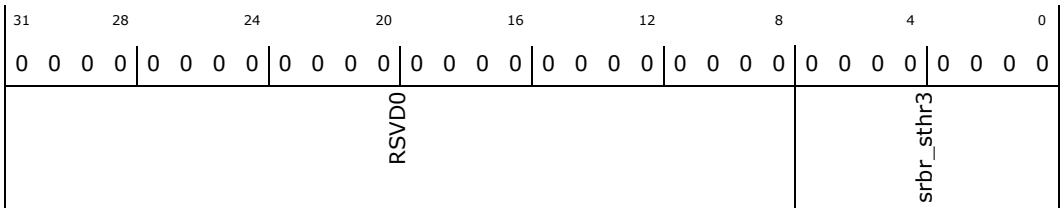
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR3: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr3:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.13 Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

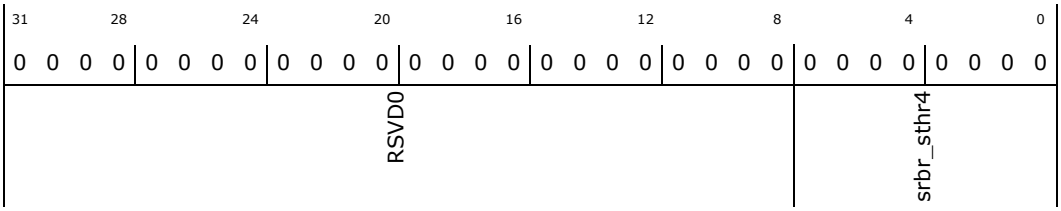
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR4: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr4:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.14 Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

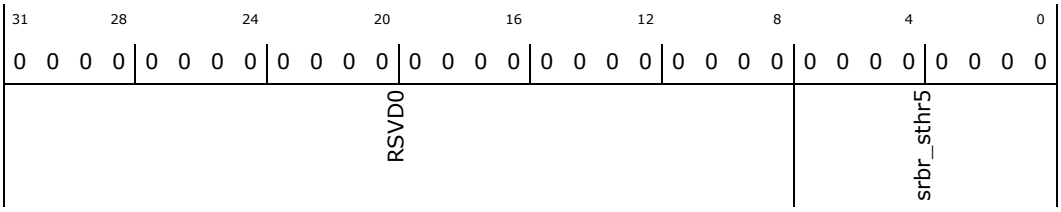
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR5: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
7:0	0h RW	**srbr_sthr5:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.15 Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

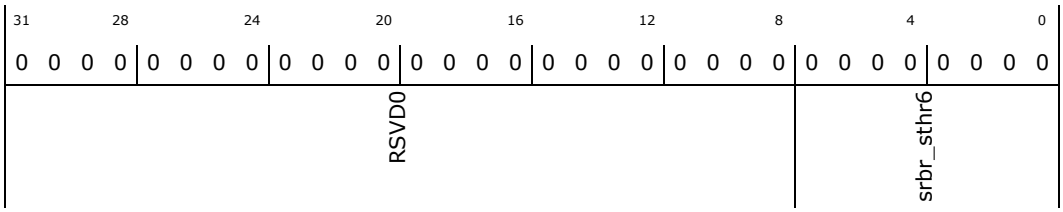
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR6: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr6:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.16 Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

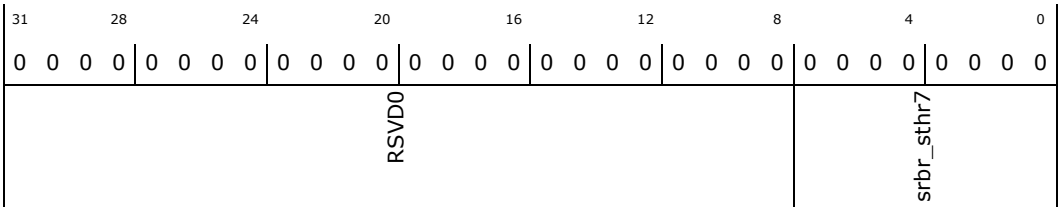
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR7: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr7:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.17 Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

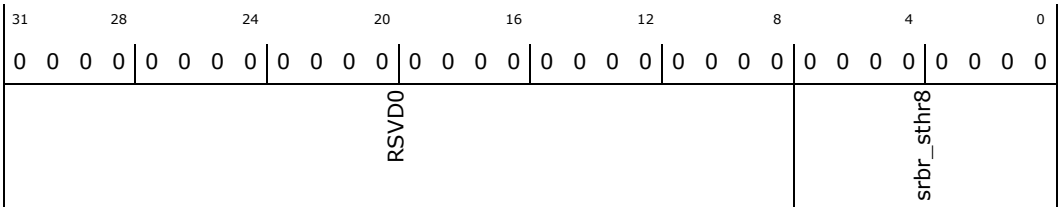
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR8: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr8:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.18 Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

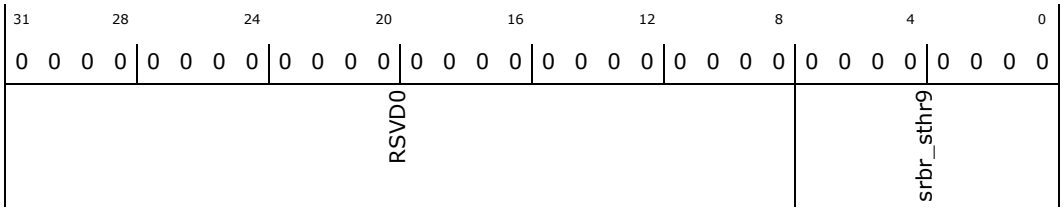
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR9: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr9:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.19 Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

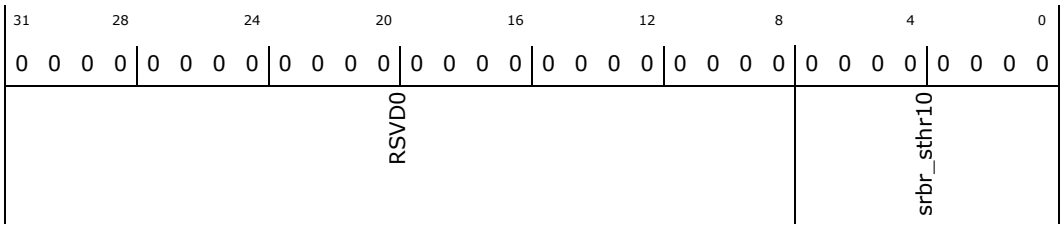
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR10: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr10:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.20 Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

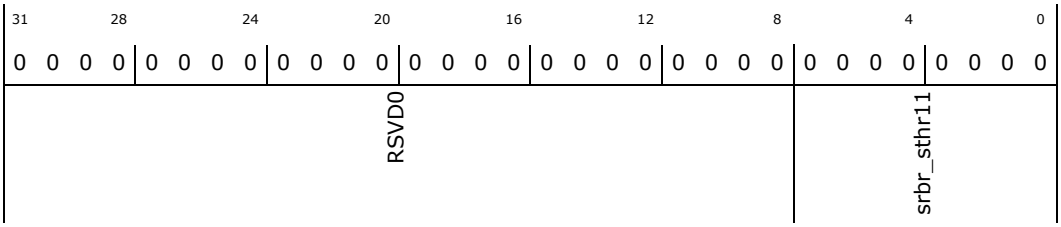
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR11: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr11:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.21 Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

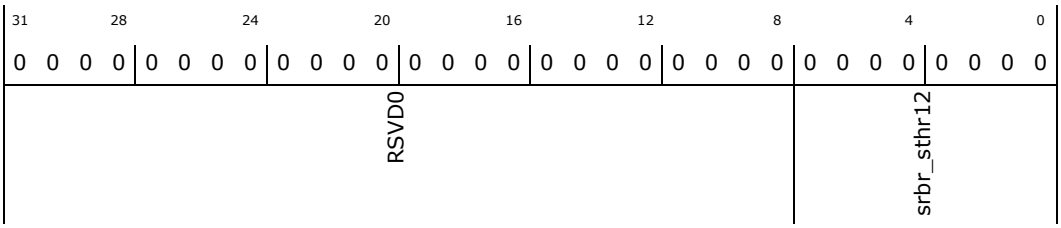
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR12: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr12:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.22 Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

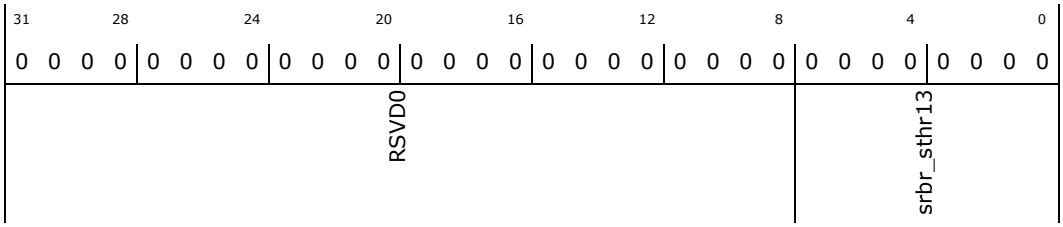
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR13: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr13:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.23 Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

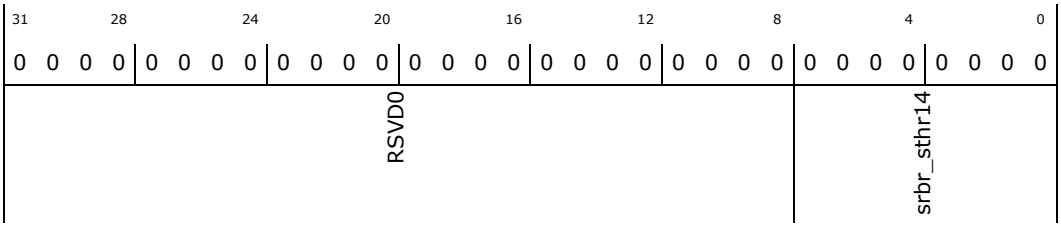
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR14: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr14:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.24 Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

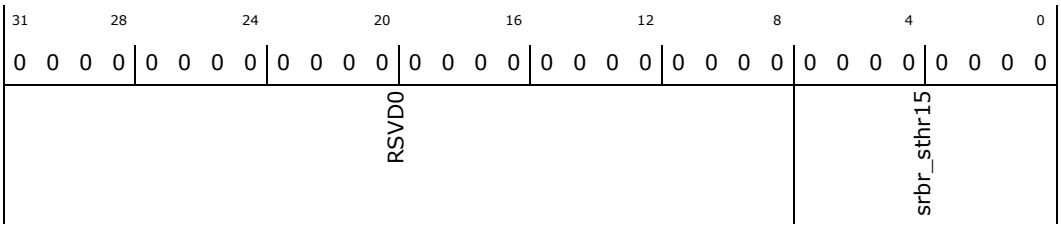
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRBR_STHR15: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr15:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

3.49.25 FIFO Access Register (FAR)—Offset 70h

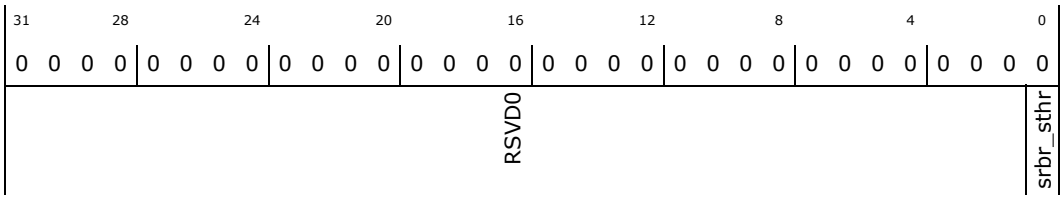
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FAR: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**srbr_sthr:** Writes have no effect when FIFO_ACCESS == No, always readable. This register is used to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. • 0 = FIFO access mode disabled • 1 = FIFO access mode enabled Note that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

3.49.26 Transmit FIFO Read (TFR)—Offset 74h

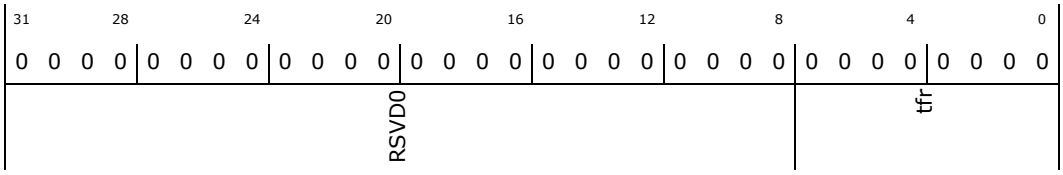
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TFR: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**Transmit FIFO Read (tfr):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

3.49.27 Receive FIFO Write (RFW)—Offset 78h

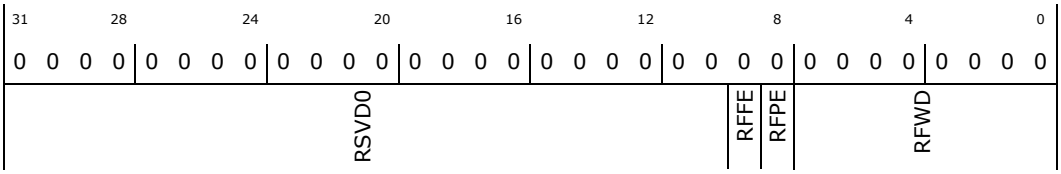
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RFW: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0b RO	**RSVD0:** Reserved
9	0h RW	**Receive FIFO Framing Error (RFFE):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR. Reset Value: 0x0
8	0h RW	**Receive FIFO Parity Error (RFPE):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR. Reset Value: 0x0
7:0	0h RW	**Receive FIFO Write Data (RFWD):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR. Reset Value: 0x0

3.49.28 UART Status Register (USR)—Offset 7Ch

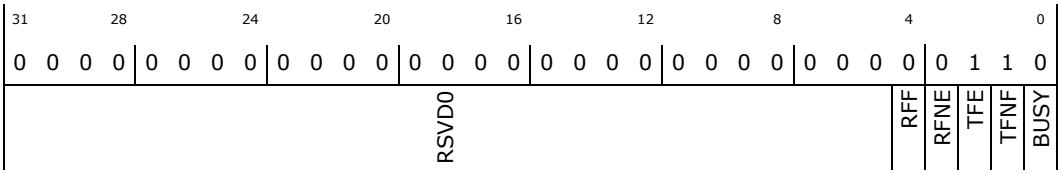
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

USR: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:5	0b RO	**RSVD0:** Reserved
4	0h RW	**Receive FIFO Full (RFF):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. • 0 = Receive FIFO not full • 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full. Reset Value: 0x0
3	0h RW	**Receive FIFO Not Empty (RFNE):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. • 0 = Receive FIFO is empty • 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty. Reset Value: 0x0
2	1h RW	**Transmit FIFO Empty (TFE):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. • 0 = Transmit FIFO is not empty • 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty. Reset Value: 0x1
1	1h RW	**Transmit FIFO Not Full (TFNF):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. • 0 = Transmit FIFO is full • 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full. Reset Value: 0x1
0	0h RW	**UART Busy (BUSY):** This bit is valid only when UART_16550_COMPATIBLE == NO and indicates that a serial transfer is in progress, ; when cleared, indicates that the DW_apb_uart is idle or inactive. • 0 = DW_apb_uart is idle or inactive • 1 = DW_apb_uart is busy (actively transferring data) NOTE: It is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the DW_apb_uart has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the DW_apb_uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock. Reset Value: 0x0

3.49.29 Transmit FIFO Level (TFL)—Offset 80h

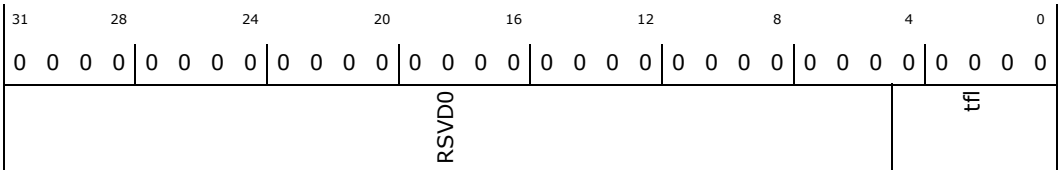
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

TFL: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RO	**RSVD0:** Reserved
4:0	0h RW	**Transmit FIFO Level (tfl):** This indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

3.49.30 Receive FIFO Level (RFL)—Offset 84h

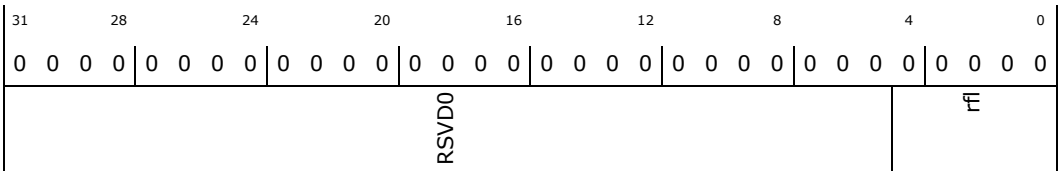
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RFL: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RO	**RSVD0:** Reserved
4:0	0h RW	**Receive FIFO Level (rfl):** This indicates the number of data entries in the receive FIFO. Reset Value: 0x0

3.49.31 Software Reset Register (SRR)—Offset 88h

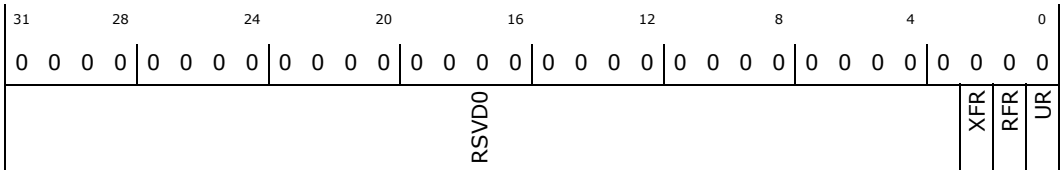
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRR: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RO	**RSVD0:** Reserved
2	0h RW	**XMIT FIFO Reset (XFR):** This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.
1	0h RW	**RCVR FIFO Reset (RFR):** This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.
0	0h RW	**UART Reset (UR):** This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset. Reset Value: 0x0

3.49.32 Shadow Request to Send (SRTS)—Offset 8Ch

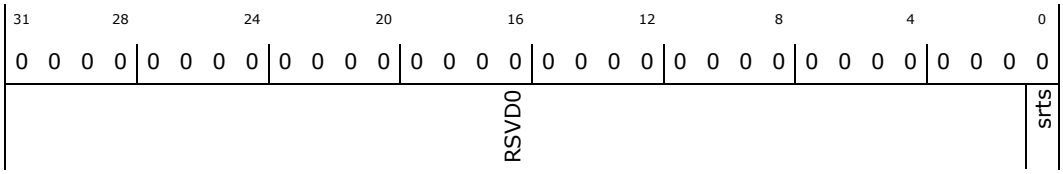
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRTS: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow Request to Send (srts):** This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

3.49.33 Shadow Break Control Register (SBCR)—Offset 90h

This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] = 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver. Reset Value: 0x0

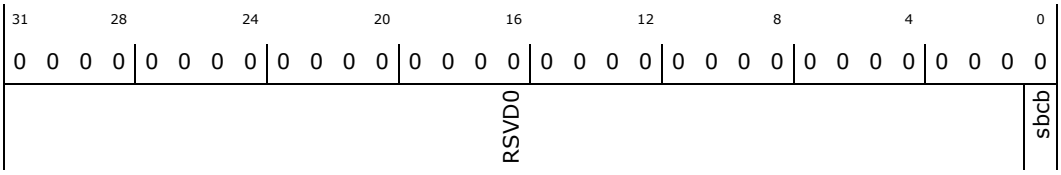
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SBCR: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow Break Control Bit (sbcb):** Reserved.

3.49.34 Shadow DMA Mode (SDMAM)—Offset 94h

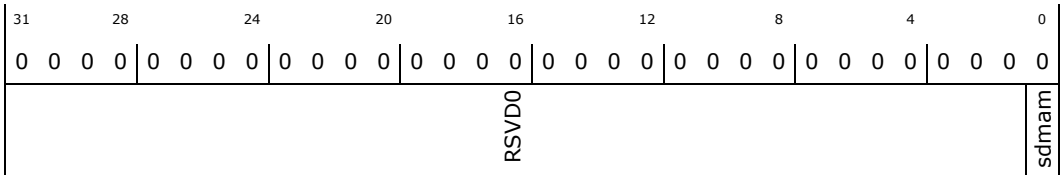
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SDMAM: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow DMA Mode (sdmam):** This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). • 0 = mode 0 • 1 = mode 1 Reset Value: 0x0

3.49.35 Shadow FIFO Enable (SFE)—Offset 98h

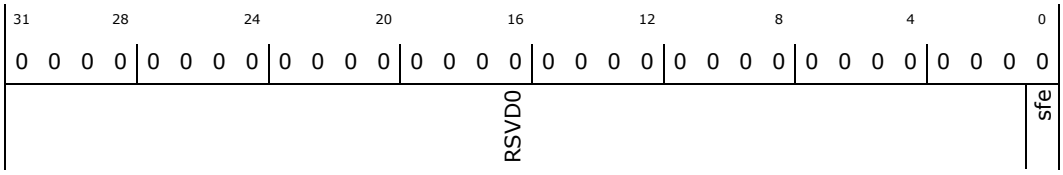
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFE: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
0	0h RW	**Shadow FIFO Enable (sfe):** This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

3.49.36 Shadow RCVR Trigger (SRT)—Offset 9Ch

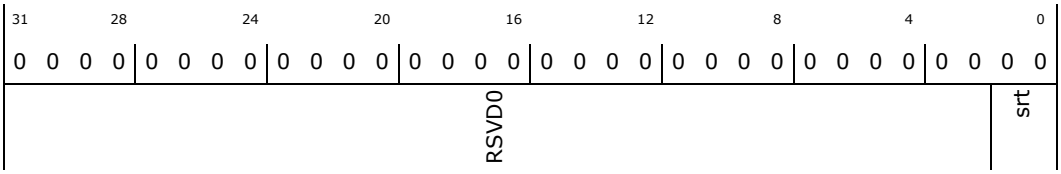
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SRT: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1:0	0h RW	**Shadow RCVR Trigger (srt):** This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: • 00 = 1 character in the FIFO • 01 = FIFO full • 10 = FIFO full • 11 = FIFO 2 less than full Reset Value: 0x0

3.49.37 Shadow TX Empty Trigger (STET)—Offset A0h

This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated.

This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported:

- 00 = FIFO empty
- 01 = 2 characters in the FIFO
- 10 = FIFO full
- 11 = FIFO full

Reset Value: 0x0 Dependencies: Writes have no effect when THRE_MODE_USER == Disabled.

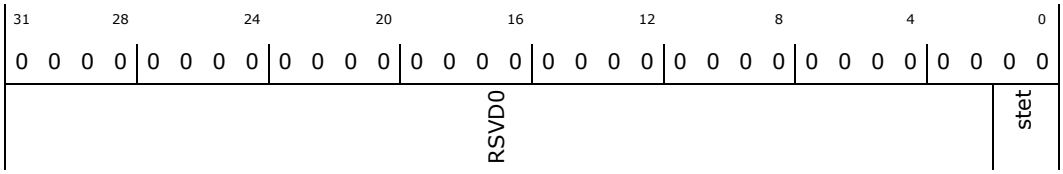
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

STET: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1:0	0h RW	**stet:** Shadow TX Empty Trigger

3.49.38 Halt TX (HTX)—Offset A4h

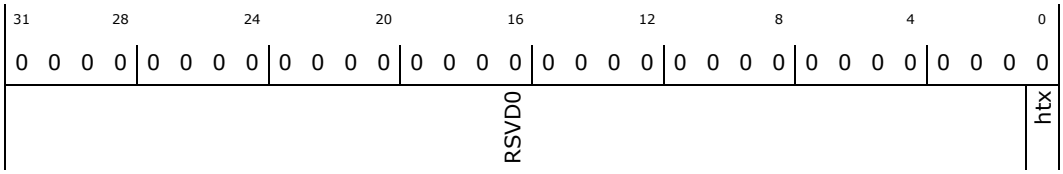
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HTX: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**htx:** This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. • 0 = Halt TX disabled • 1 = Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.

3.49.39 DMA Software Acknowledge (DMASA)—Offset A8h

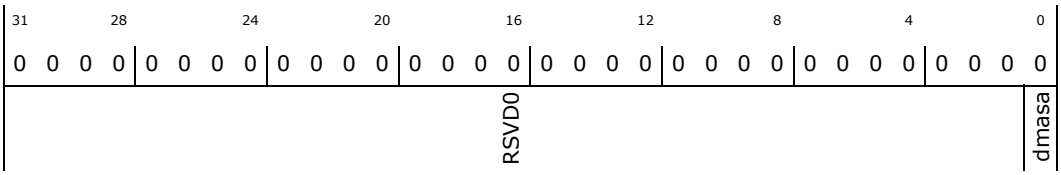
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DMASA: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**dmasa:** This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when DMA_EXTRA == No.

3.49.40 Component Parameter Register (CPR)—Offset F4h

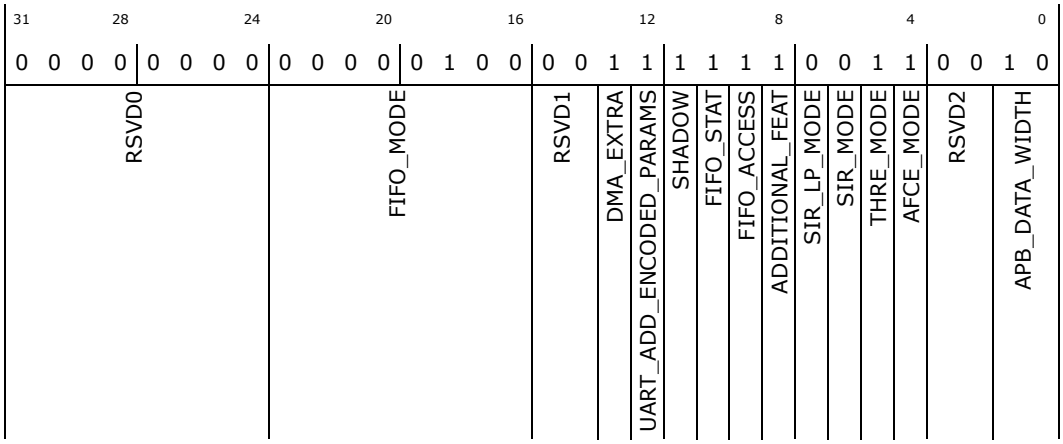
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CPR: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00043F32h



Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved
23:16	4h RO	**FIFO MODE (FIFO_MODE):** • 0x00 = 0 • 0x01 = 16 • 0x02 = 32 • to • 0x80 = 2048 • 0x81- 0xff = reserved
15:14	0b RO	**RSVD1:** Reserved
13	1h RO	**DMA EXTRA (DMA_EXTRA):** • 0 = FALSE • 1 = TRUE
12	1h RO	**UART ADD ENCODED PARAMS (UART_ADD_ENCODED_PARAMS):** • 0 = FALSE, • 1 = TRUE
11	1h RO	**SHADOW:** • 0 = FALSE, • 1 = TRUE
10	1h RO	**FIFO STAT (FIFO_STAT):** • 0 = FALSE, • 1 = TRUE
9	1h RO	**FIFO ACCESS (FIFO_ACCESS):** • 0 = FALSE, • 1 = TRUE
8	1h RO	**ADDITIONAL FEAT (ADDITIONAL_FEAT):** • 0 = FALSE, • 1 = TRUE
7	0h RO	**SIR LP MODE (SIR_LP_MODE):** • 0 = FALSE, • 1 = TRUE

Bit Range	Default & Access	Description
6	0h RO	**SIR MODE (SIR_MODE):** • 0 = FALSE, • 1 = TRUE
5	1h RO	**THRE MODE (THRE_MODE):** • 0 = FALSE, • 1 = TRUE
4	1h RO	**AFCE MODE (AFCE_MODE):** • 0 = FALSE, • 1 = TRUE
3:2	0b RO	**RSVD2:** Reserved
1:0	2h RO	**APB DATA WIDTH (APB_DATA_WIDTH):** • 00 = 8 bits • 01 = 16 bits • 10 = 32 bits • 11 = reserved

3.49.41 UART Component Version (UCV)—Offset F8h

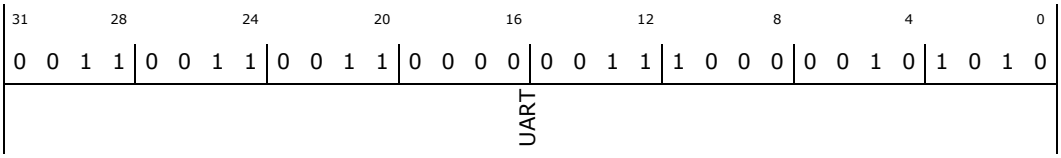
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

UCV: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 3330382Ah



Bit Range	Default & Access	Description
31:0	3330382ah RO	**UART:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*. Reset Value: See the releases table in the AMBA 2 release notes.

3.49.42 Component Type Register (CTR)—Offset FCh

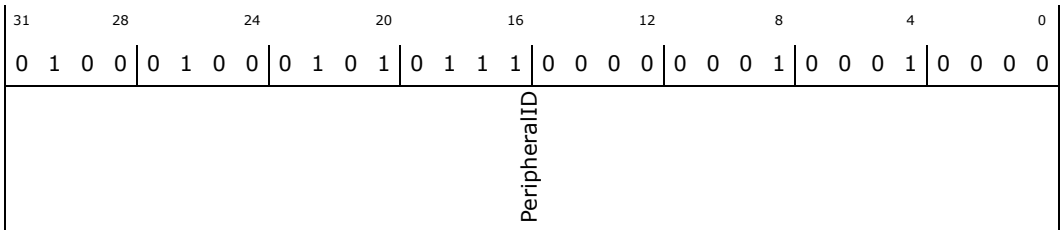
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTR: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 44570110h



Bit Range	Default & Access	Description
31:0	44570110h RO	**Peripheral ID (PeripheralID):** This register contains the peripherals identification code. Reset Value: 0x44570110

3.49.43 Private Clock Params (PRV_CLOCK_PARAMS)—Offset 800h

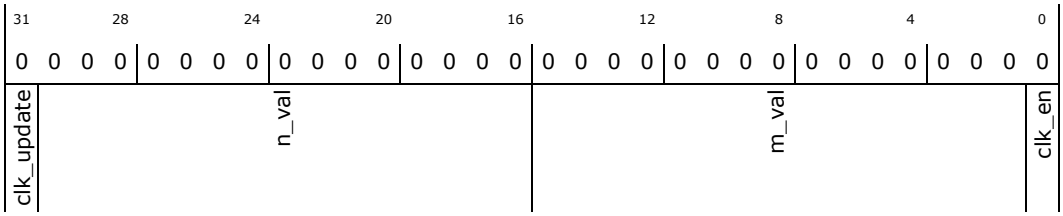
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRV_CLOCK_PARAMS: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**clk_update:** update the clock divider after setting new m and n values
30:16	0h RW	**N_VAL (n_val):** n value for the m over n divider
15:1	0h RW	**M_VAL (m_val):** m value for the m over n divider
0	0h RW	**clk_en:** clk en of the m over n divider

3.49.44 Software Resets (RESETS)—Offset 804h

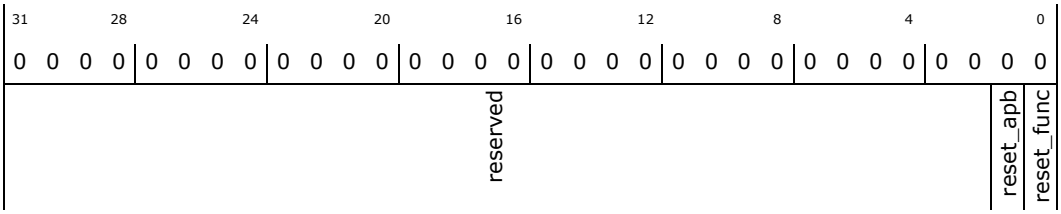
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.49.45 General Purpose Register (GENERAL)—Offset 808h

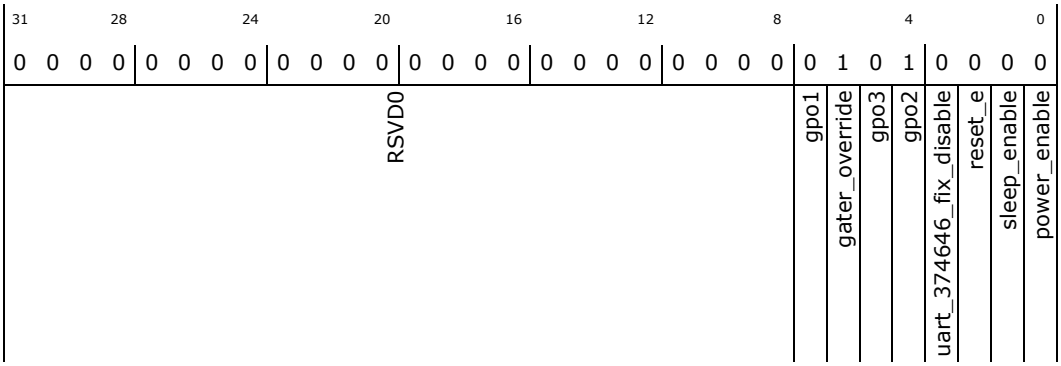
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000050h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
7	0h RW	**gpo1:** not applicable
6	1h RW	**gater_override:** not applicable
5	0h RW	**gpo3:** not applicable
4	1h RW	**gpo2:** This bit indicates whether the UART clock req will be dynamic or controlled by the UART clock en: • 1 = controlled by the clk en • 0 = dynamic Default value = 1
3	0h RW	**uart_374646_fix_disable:** Disable rts_n override
2	0h RW	**reset_e:** not applicable
1	0h RW	**sleep_enable:** not applicable
0	0h RW	**power_enable:** not applicable

3.49.46 UART_BYTE_COUNT—Offset 818h

Transaction counter

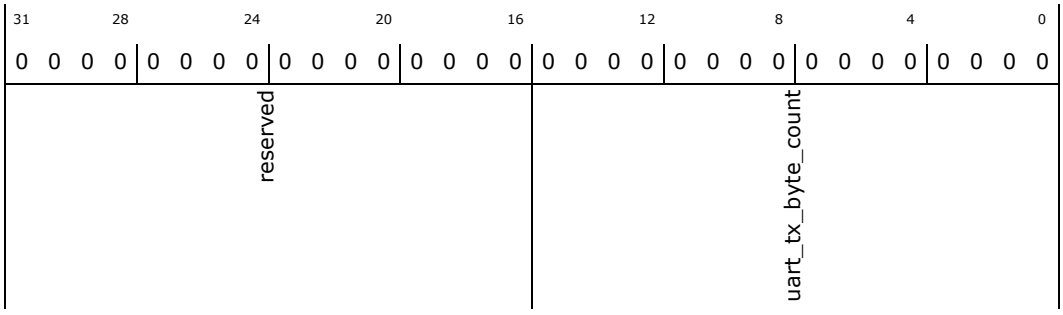
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

UART_BYTE_COUNT: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**reserved (reserved):** reserved

Bit Range	Default & Access	Description
15:0	0h RO	**uart_tx_byte_count:** UART transaction counter

3.49.47 UART_OVERFLOW_INTR_STAT—Offset 820h

Overflow interrupt

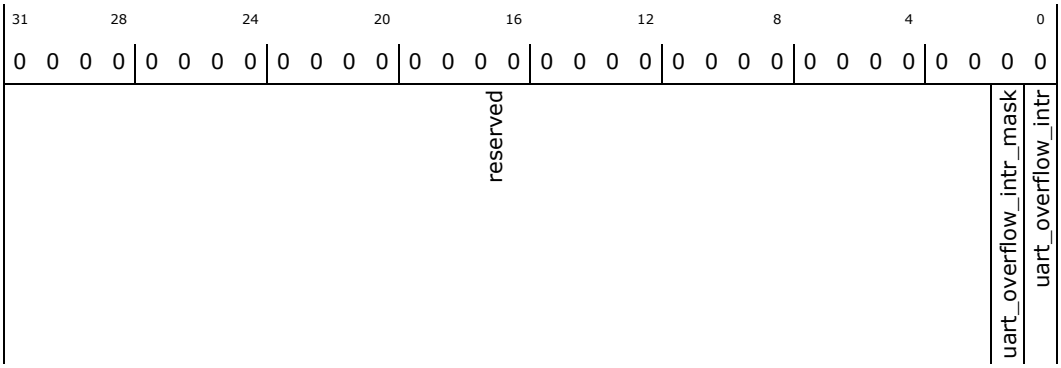
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

UART_OVERFLOW_INTR_STAT: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**reserved:** reserved
1	0h RW	**uart1_overflow_intr_mask (uart_overflow_intr_mask):** Mask the overflow into
0	0h RO	**uart_overflow_intr:** Indicate there was count overflow

3.50 SIO PWM0 PCI Configuration Registers

Table 58. Summary of SIO PWM0 PCI Configuration Registers—0/30/1

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 3006	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 3007	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3008	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 3009	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 3010	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 3010	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 3011	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3012	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 3012	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 3013	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 3013	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 3014	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 3015	00000000h

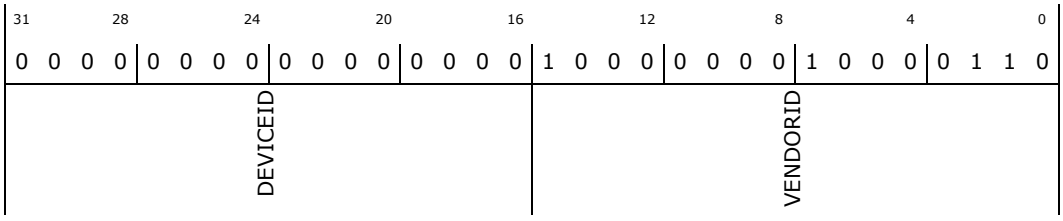
3.50.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:30, F:1] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

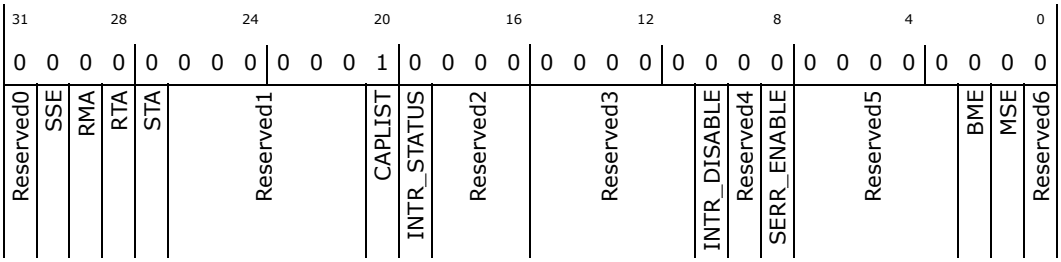
3.50.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:30, F:1] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

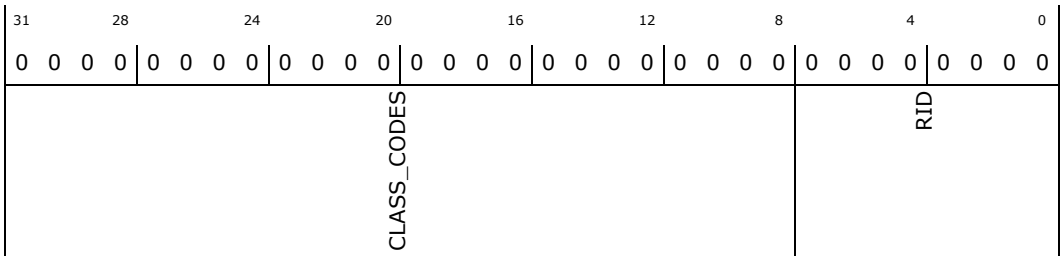
3.50.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:30, F:1] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

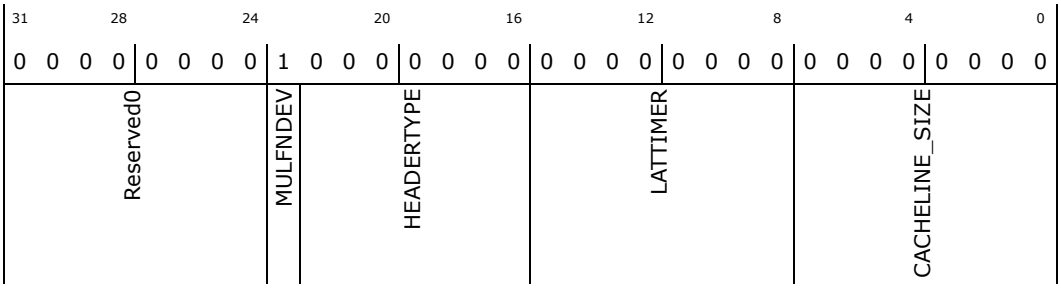
3.50.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:30, F:1] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

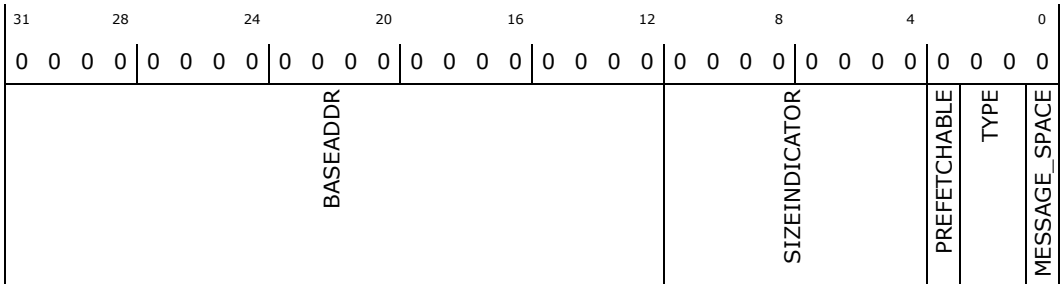
3.50.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:30, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

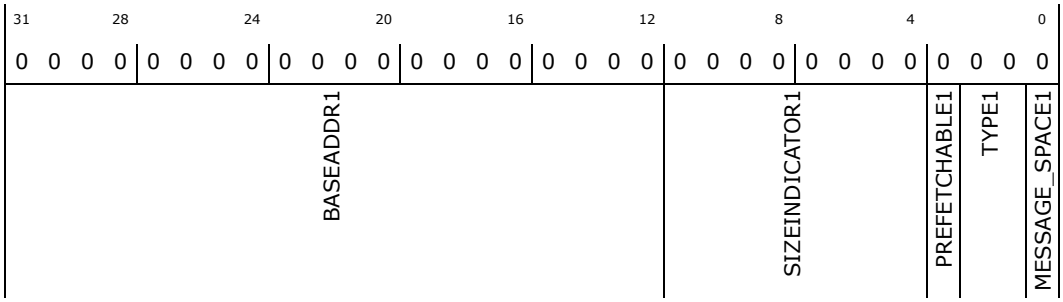
3.50.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:30, F:1] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

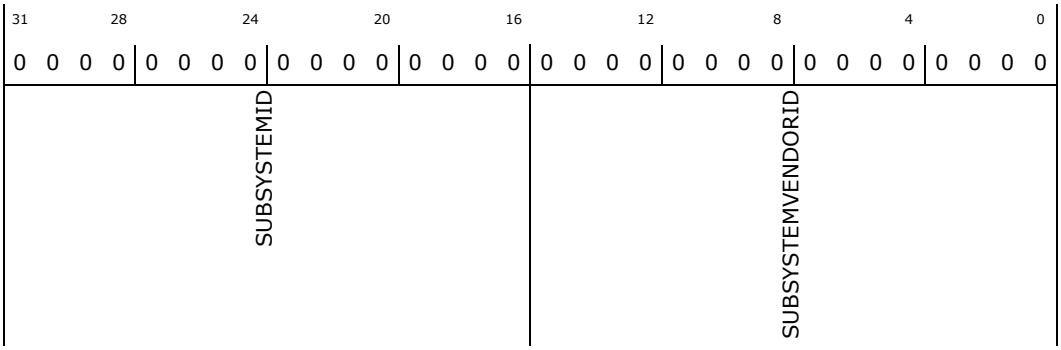
3.50.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:30, F:1] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

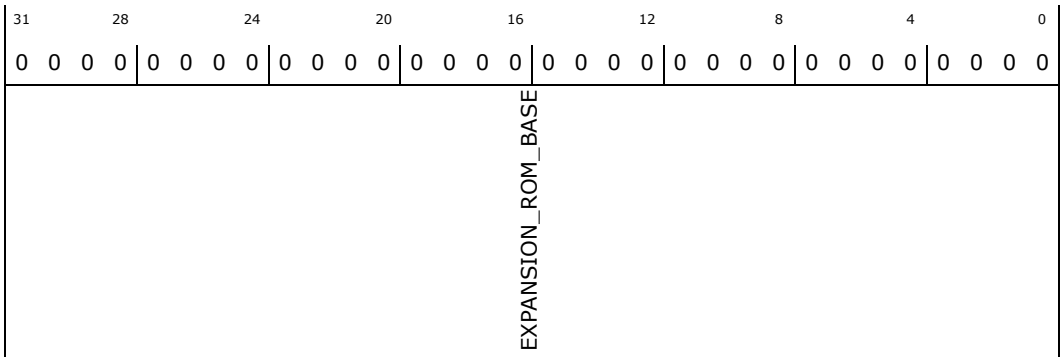
3.50.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:30, F:1] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

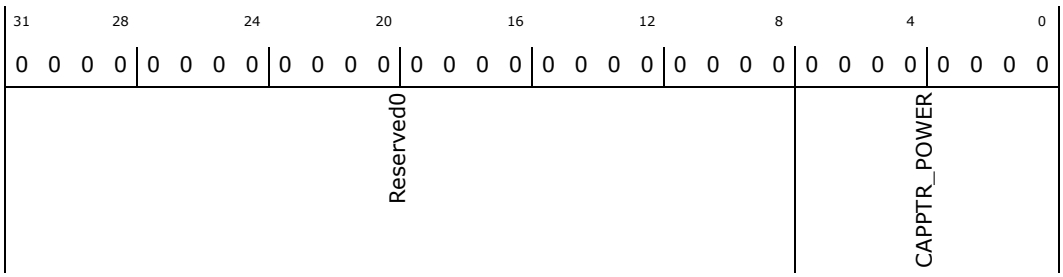
3.50.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:30, F:1] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

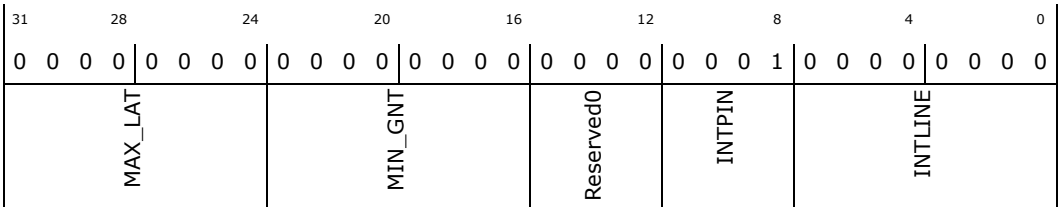
3.50.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:30, F:1] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

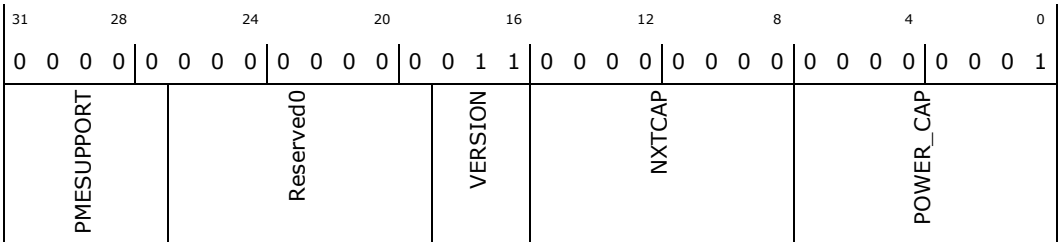
3.50.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:30, F:1] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

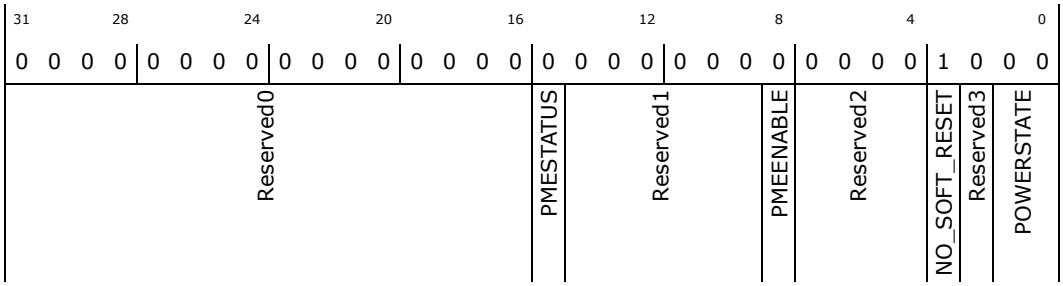
3.50.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:30, F:1] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

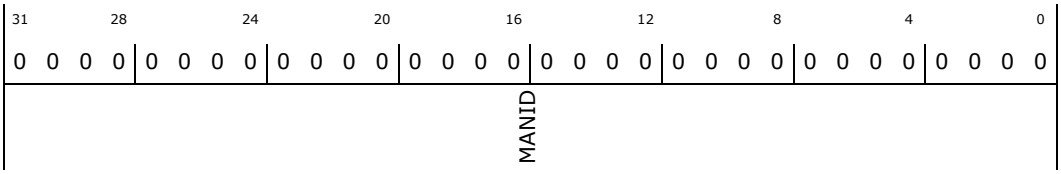
3.50.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:30, F:1] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

3.51 SIO PWM0 Memory Mapped IO Registers

Table 59. Summary of SIO PWM0 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"PWM Control Register (PWMCTRL)—Offset 0h" on page 3016	00010000h
804h	4	"Software Reset (RESETS)—Offset 804h" on page 3017	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 3017	00000010h

3.51.1 PWM Control Register (PWMCTRL)—Offset 0h

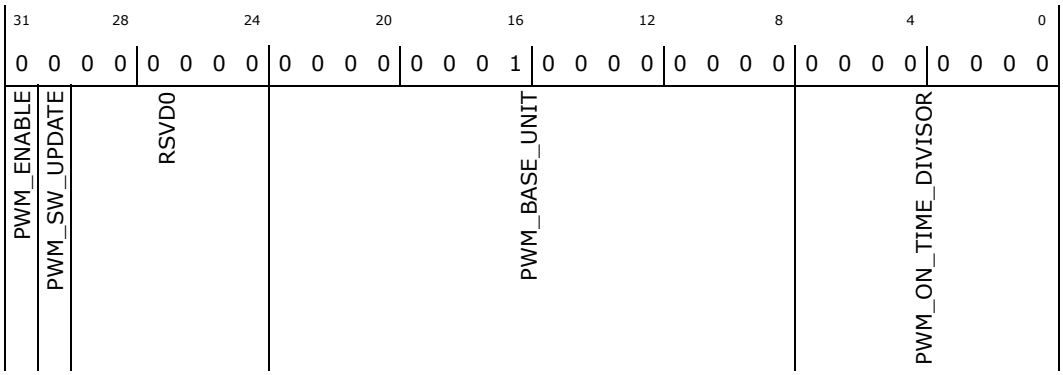
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PWMCTRL: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:1] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31	0b RW	**PWM Enable (PWM_ENABLE):** • 0 = Disable PWM Output • 1 = Enable PWM Output
30	0b RW	**PWM Software Update (PWM_SW_UPDATE):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. • 0 = No updates pending • 1 = Update pending
29:24	0b RO	**RSVD0:** Reserved
23:8	0100h RW	**PWM Base Unit (PWM_BASE_UNIT):** Base unit register. Unsigned 8 integer bits, 8 fraction bits. Used to determine PWM output frequency.

Bit Range	Default & Access	Description
7:0	00h RW	**PWM On Time Divisor (PWM_ON_TIME_DIVISOR):** PWM duty cycle = PWM_on-time_divisor/256.

3.51.2 Software Reset (RESETS)—Offset 804h

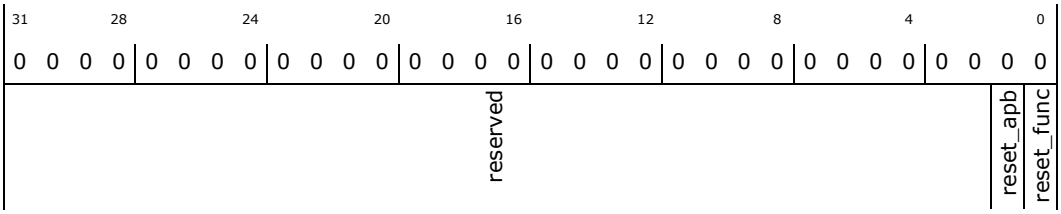
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.51.3 General Purpose Register (GENERAL)—Offset 808h

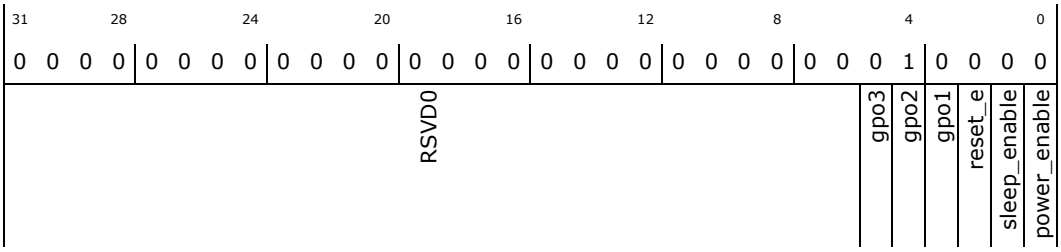
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:1] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:6	0b RO	**RSVD0:** Reserved
5	0h RW	**gpo3:** not applicable
4	1h RW	**gpo2:** not applicable
3	0h RW	**gpo1:** not applicable
2	0h RW	**reset_e:** not applicable
1	0h RW	**sleep_enable:** not applicable
0	0h RW	**power_enable:** not applicable

3.52 SIO PWM1 PCI Configuration Registers

Table 60. Summary of SIO PWM1 PCI Configuration Registers—0/30/2

Offset	Size	Register ID—Description	Default Value
0h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 3019	00008086h
4h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 3020	00100000h
8h	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3021	00000000h
Ch	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 3022	00800000h
10h	4	"Base Address Register (BAR)—Offset 10h" on page 3023	00000000h
14h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 3023	00000000h
2Ch	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 3024	00000000h
30h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3025	00000000h
34h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 3025	00000000h
3Ch	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 3026	00000100h
80h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 3026	00030001h
84h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 3027	00000008h
F8h	4	"Manufacturer ID (MANID)—Offset F8h" on page 3028	00000000h

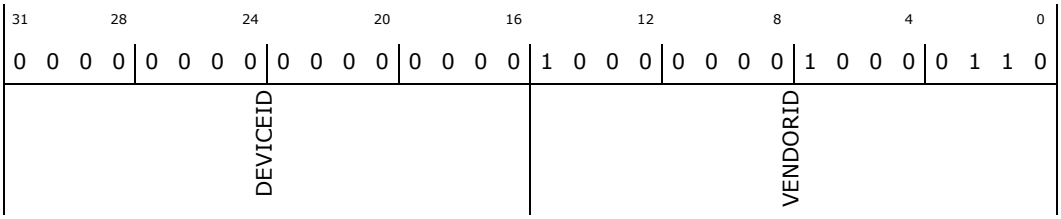
3.52.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:30, F:2] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.

Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

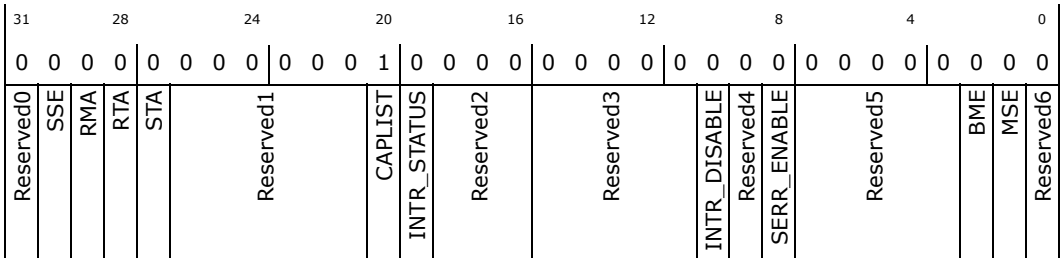
3.52.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:30, F:2] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Description
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

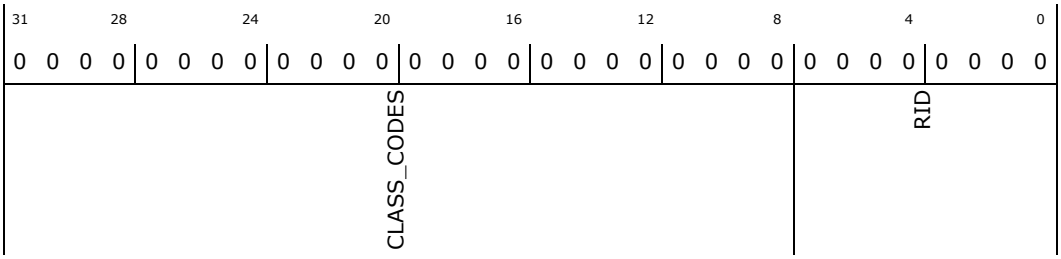
3.52.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:30, F:2] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

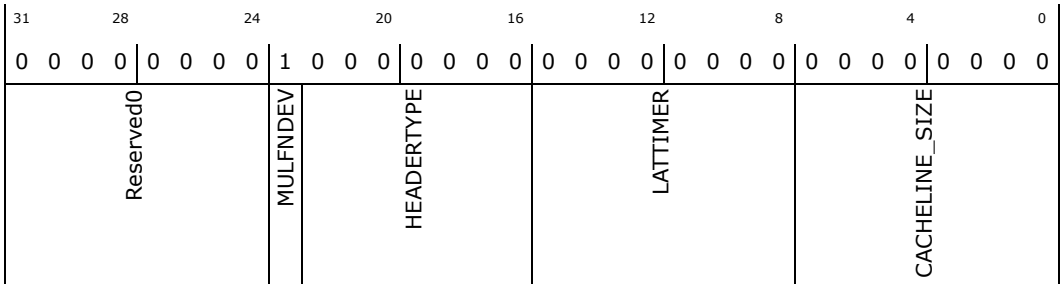
3.52.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:30, F:2] + Ch

Default: 00800000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

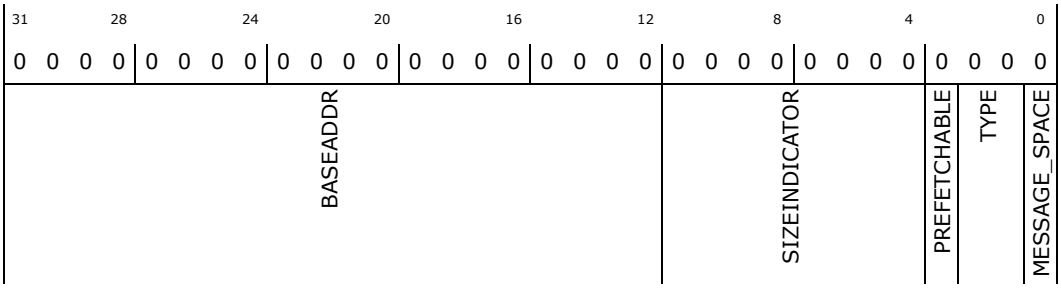
3.52.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:30, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

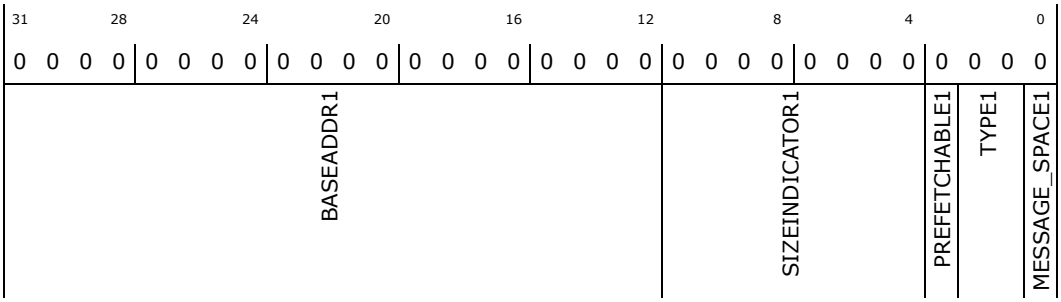
3.52.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:30, F:2] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

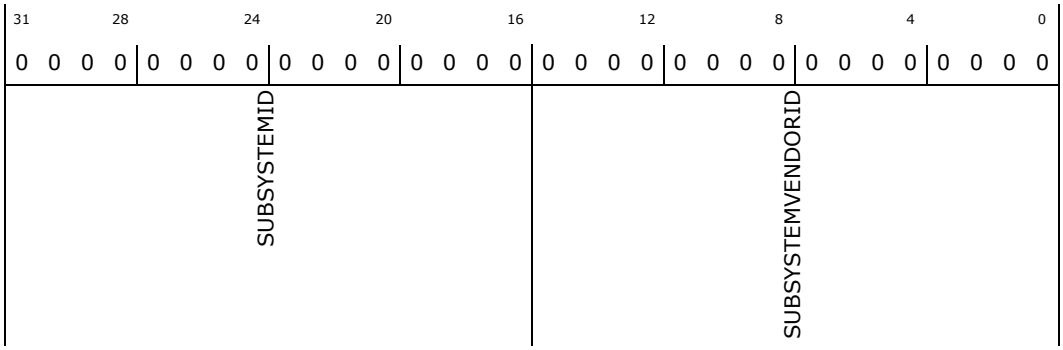
3.52.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:30, F:2] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

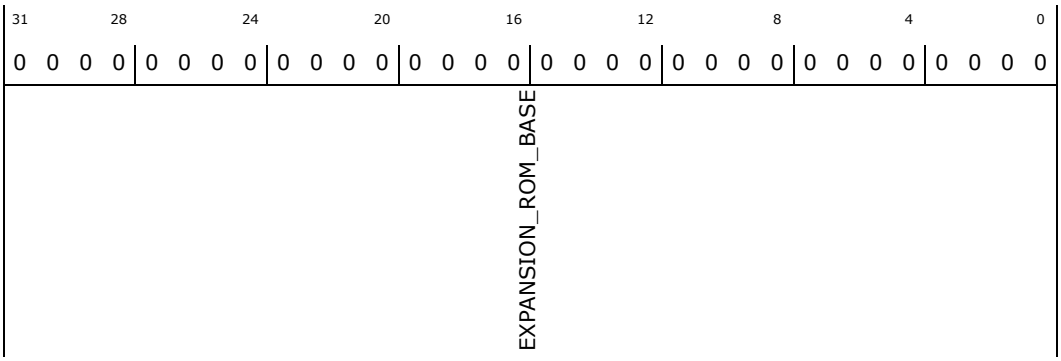
3.52.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:30, F:2] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

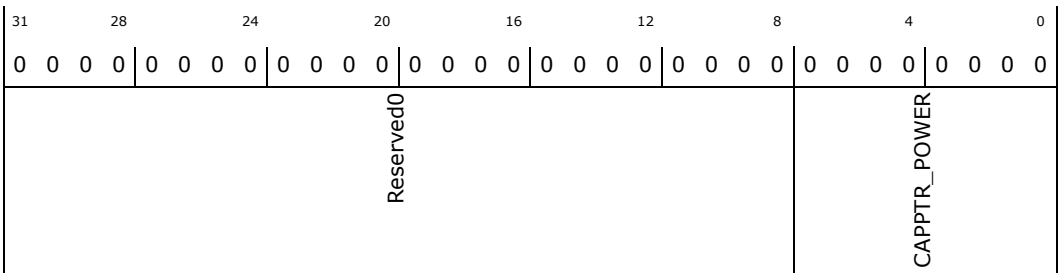
3.52.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:30, F:2] + 34h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

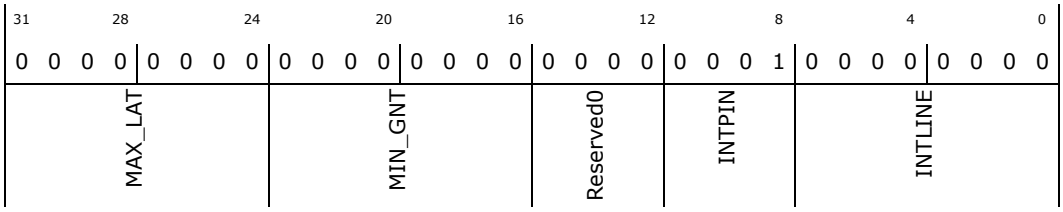
3.52.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:30, F:2] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

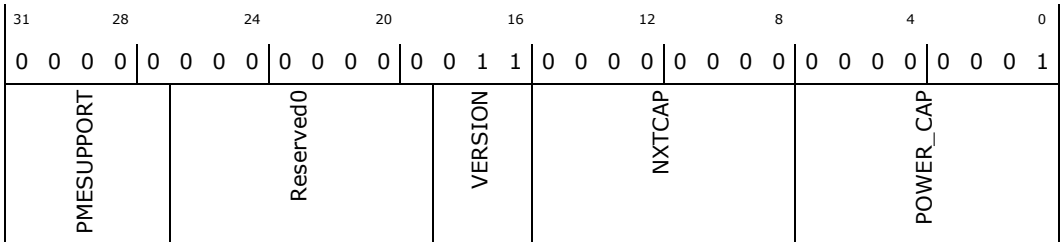
3.52.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:30, F:2] + 80h

Default: 00030001h



Bit Range	Default & Access	Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

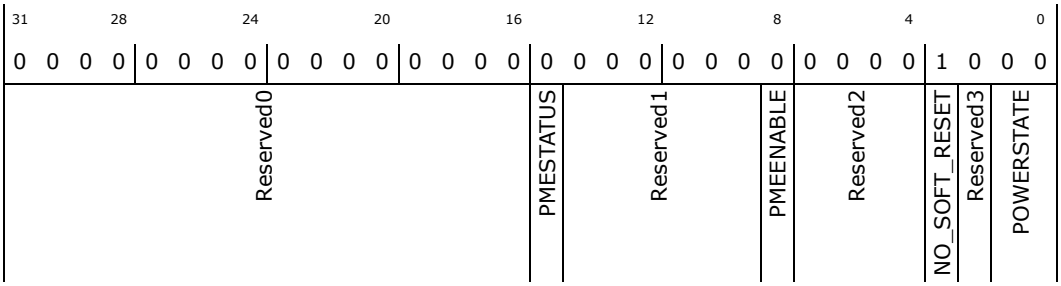
3.52.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:30, F:2] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).

Bit Range	Default & Access	Description
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

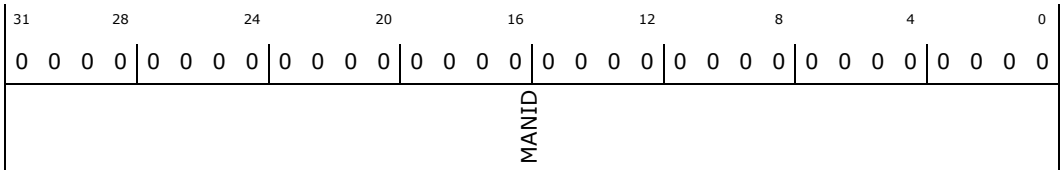
3.52.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:30, F:2] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

3.53 SIO PWM1 Memory Mapped IO Registers

Table 61. Summary of SIO PWM1 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"PWM Control Register (PWMCTRL)—Offset 0h" on page 3029	00010000h
804h	4	"Software Reset (RESETS)—Offset 804h" on page 3030	00000000h
808h	4	"General Purpose Register (GENERAL)—Offset 808h" on page 3030	00000010h

3.53.1 PWM Control Register (PWMCTRL)—Offset 0h

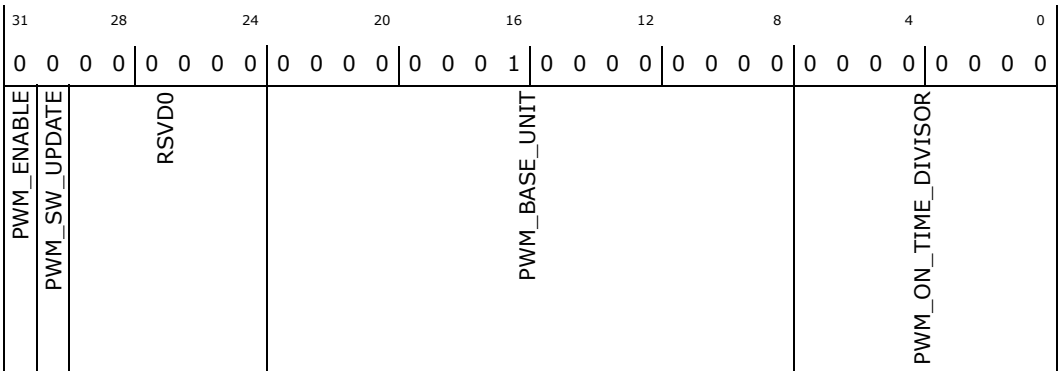
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PWMCTRL: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:2] + 10h

Default: 00010000h



Bit Range	Default & Access	Description
31	0b RW	**PWM Enable (PWM_ENABLE):** • 0 = Disable PWM Output • 1 = Enable PWM Output
30	0b RW	**PWM Software Update (PWM_SW_UPDATE):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. • 0 = No updates pending • 1 = Update pending
29:24	0b RO	**RSVD0:** Reserved
23:8	0100h RW	**PWM Base Unit (PWM_BASE_UNIT):** Base unit register. Unsigned 8 integer bits, 8 fraction bits. Used to determine PWM output frequency.

Bit Range	Default & Access	Description
7:0	00h RW	**PWM On Time Divisor (PWM_ON_TIME_DIVISOR):** PWM duty cycle = PWM_on-time_divisor/256.

3.53.2 Software Reset (RESETS)—Offset 804h

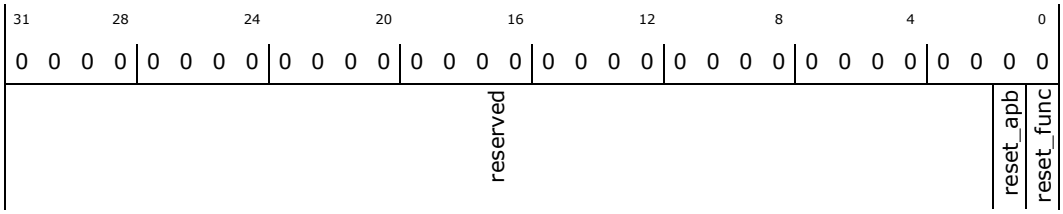
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RESETS: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

3.53.3 General Purpose Register (GENERAL)—Offset 808h

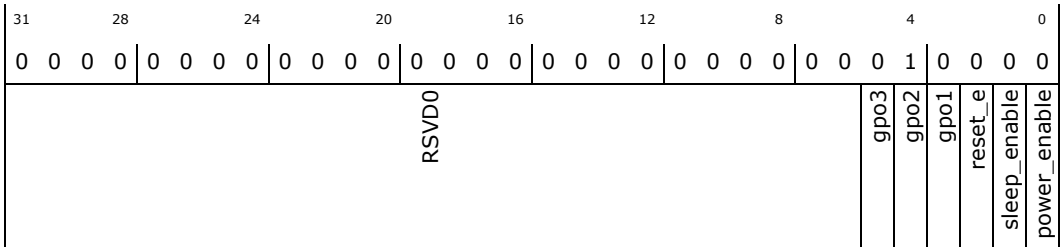
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

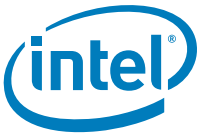
GENERAL: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:2] + 10h

Default: 00000010h



Bit Range	Default & Access	Description
31:6	0b RO	**RSVD0:** Reserved
5	0h RW	**gpo3:** not applicable
4	1h RW	**gpo2:** not applicable
3	0h RW	**gpo1:** not applicable
2	0h RW	**reset_e:** not applicable
1	0h RW	**sleep_enable:** not applicable
0	0h RW	**power_enable:** not applicable



3.54 PCU iLB LPC Port 80h I/O Registers

Table 62. Summary of PCU iLB LPC Port 80h I/O Registers—

Offset	Size	Register ID—Description	Default Value
80h	1	"PC80—Offset 80h" on page 3032	00h
81h	1	"PC81—Offset 81h" on page 3033	00h
82h	1	"PC82—Offset 82h" on page 3033	00h
83h	1	"PC83—Offset 83h" on page 3033	00h
84h	1	"PC84—Offset 84h" on page 3034	00h
85h	1	"PC85—Offset 85h" on page 3034	00h
86h	1	"PC86—Offset 86h" on page 3035	00h
87h	1	"PC87—Offset 87h" on page 3035	00h
88h	1	"PC88—Offset 88h" on page 3036	00h
89h	1	"PC89—Offset 89h" on page 3036	00h
8Ah	1	"PC8A—Offset 8Ah" on page 3036	00h
8Bh	1	"PC8B—Offset 8Bh" on page 3037	00h
8Ch	1	"PC8C—Offset 8Ch" on page 3037	00h
8Dh	1	"PC8D—Offset 8Dh" on page 3038	00h
8Eh	1	"PC8E—Offset 8Eh" on page 3038	00h
8Fh	1	"PC8F—Offset 8Fh" on page 3039	00h

3.54.1 PC80—Offset 80h

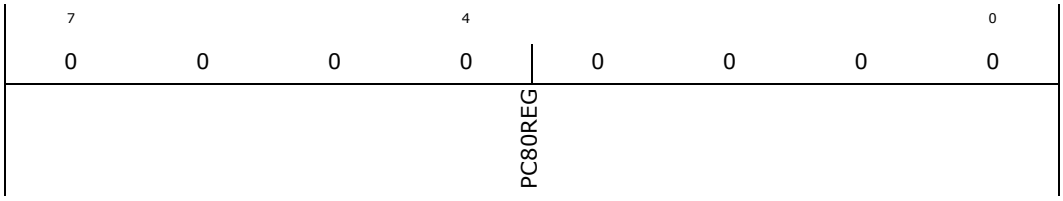
Post Code 80 register

Access Method

Type: I/O Register (Size: 8 bits)

PC80: 80h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RW	**PC80REG:** Post Code 80 register

3.54.2 PC81—Offset 81h

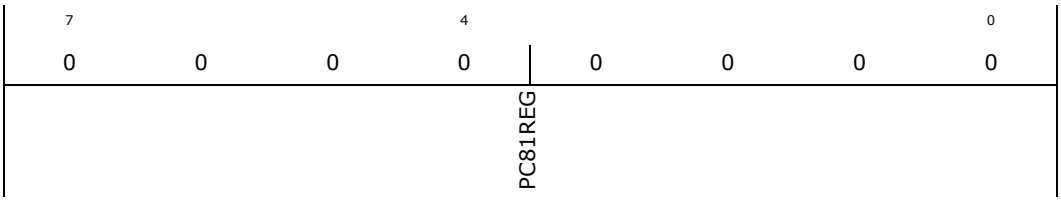
Post Code 81 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC81: 81h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**PC81REG:** Post Code 81 register

3.54.3 PC82—Offset 82h

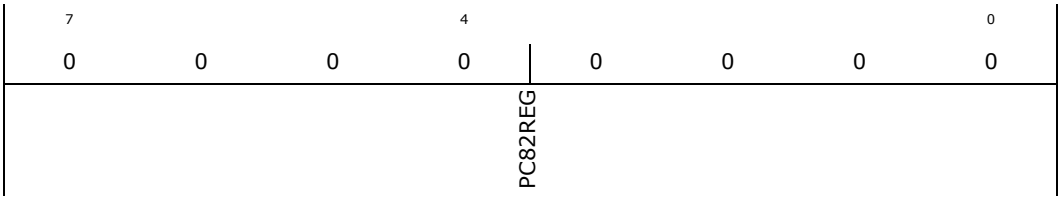
Post Code 82 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC82: 82h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**PC82REG:** Post Code 82 register

3.54.4 PC83—Offset 83h

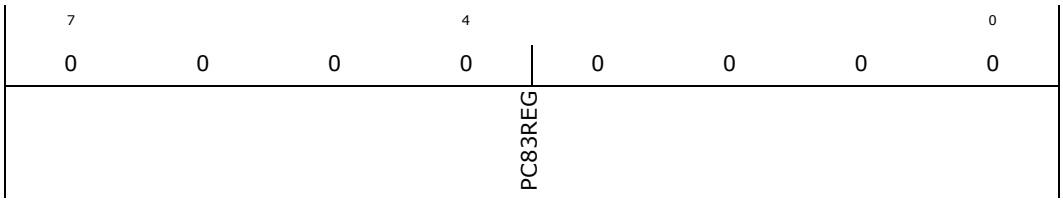
Post Code 83 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC83: 83h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**PC83REG:** Post Code 83 register

3.54.5 PC84—Offset 84h

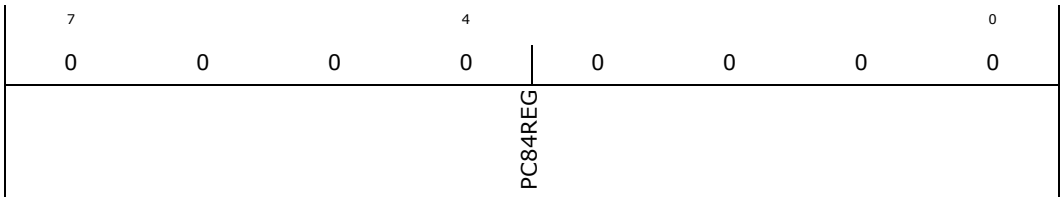
Post Code 84 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC84: 84h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**PC80REG (PC84REG):** Post Code 84 register

3.54.6 PC85—Offset 85h

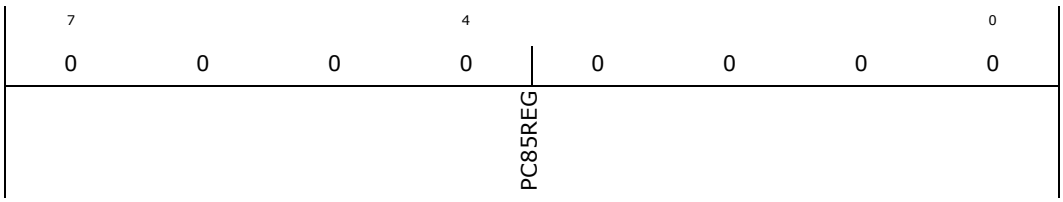
Post Code 85 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC85: 85h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**PC85REG:** Post Code 85 register

3.54.7 PC86—Offset 86h

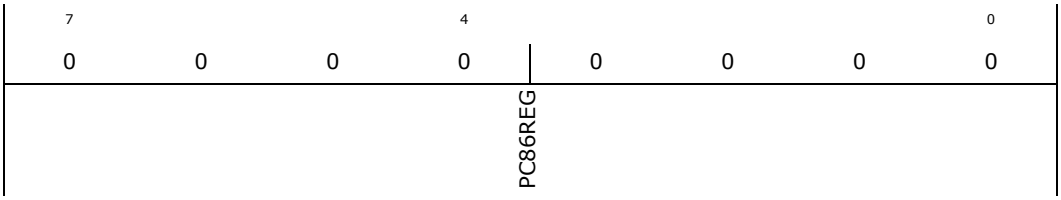
Post Code 86 register

Access Method

Type: I/O Register (Size: 8 bits)

PC86: 86h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**PC86REG:** Post Code 86 register

3.54.8 PC87—Offset 87h

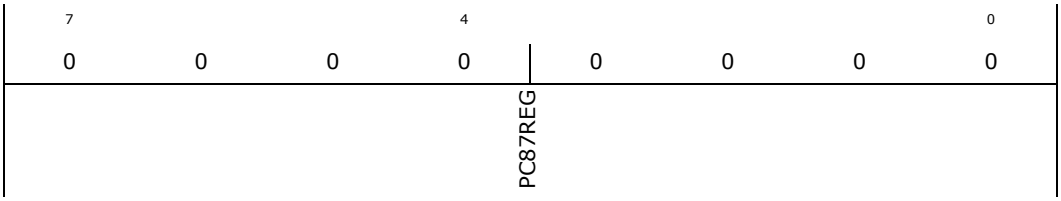
Post Code 87 register

Access Method

Type: I/O Register (Size: 8 bits)

PC87: 87h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**PC87REG:** Post Code 87 register

3.54.9 PC88—Offset 88h

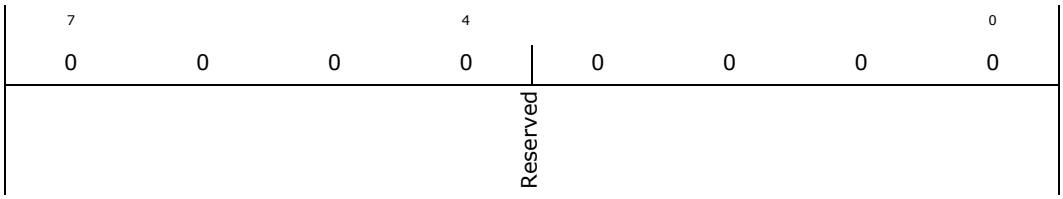
Post Code 88 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC88: 88h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

3.54.10 PC89—Offset 89h

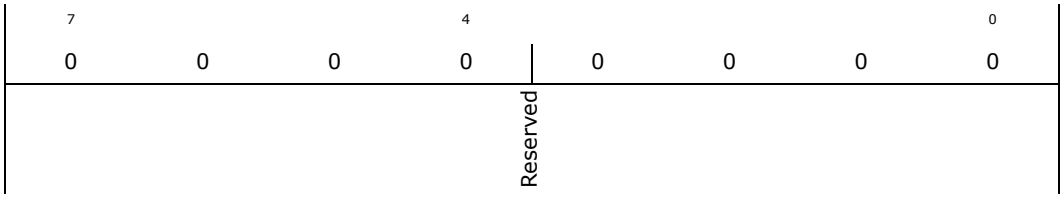
Post Code 89 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC89: 89h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

3.54.11 PC8A—Offset 8Ah

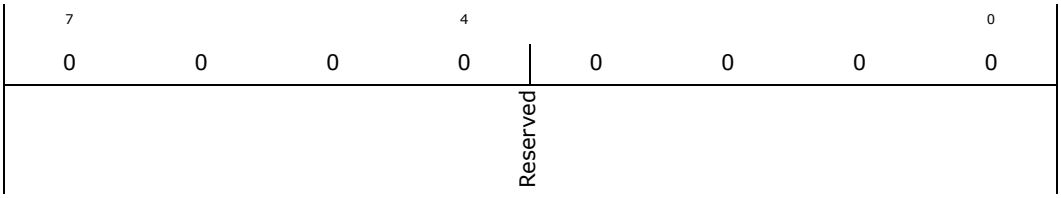
Post Code 8A register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8A: 8Ah

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

3.54.12 PC8B—Offset 8Bh

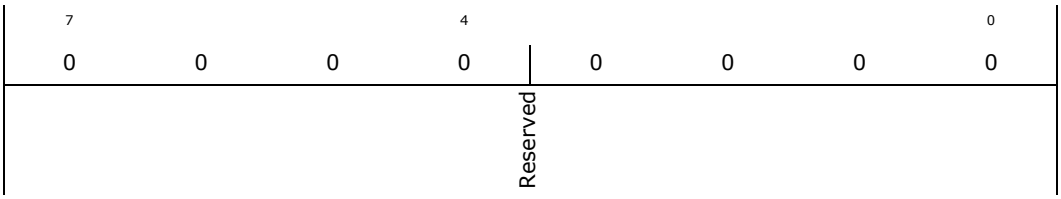
Post Code 8B register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8B: 8Bh

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

3.54.13 PC8C—Offset 8Ch

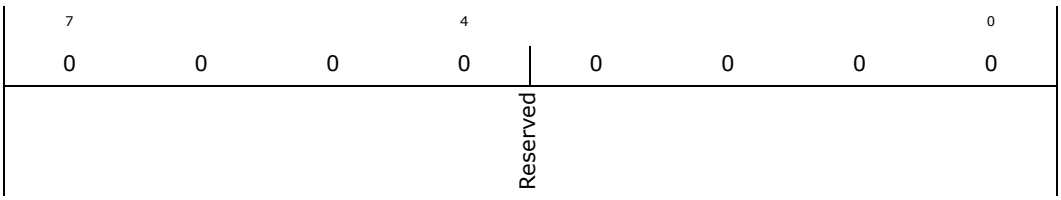
Post Code 8C register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8C: 8Ch

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

3.54.14 PC8D—Offset 8Dh

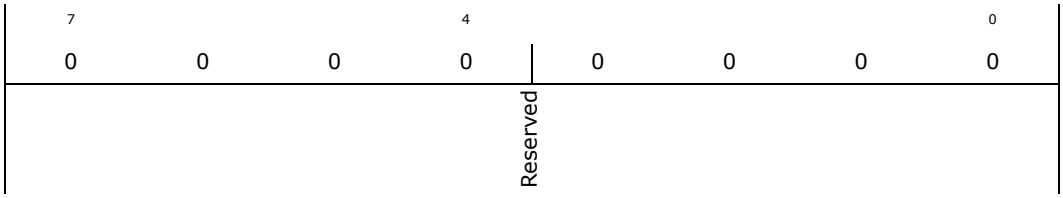
Post Code 8D register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8D: 8Dh

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

3.54.15 PC8E—Offset 8Eh

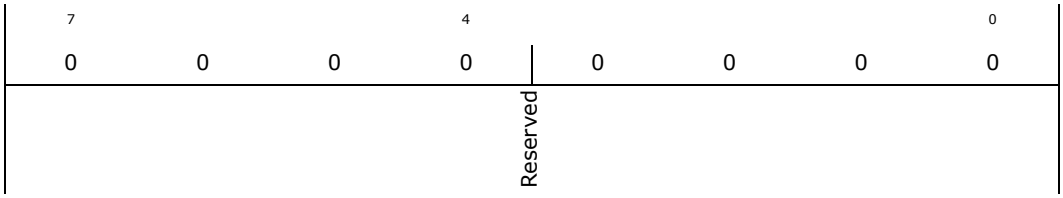
Post Code 8E register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8E: 8Eh

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

3.54.16 PC8F—Offset 8Fh

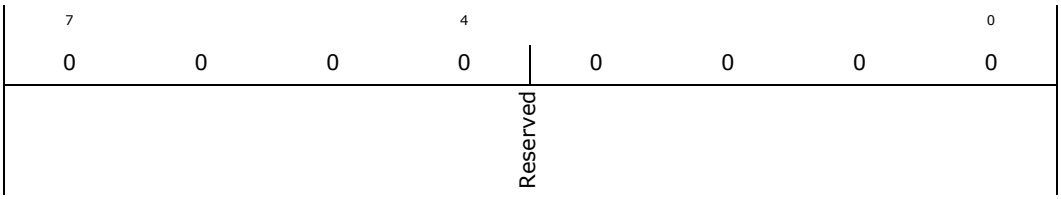
Post Code 8F register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8F: 8Fh

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

3.55 PCU PMC Memory Mapped I/O Registers

Table 63. Summary of PCU iLB PMC Memory Mapped I/O Registers—PMC_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"PRSTS - Power and Reset Status (PRSTS)—Offset 0h" on page 3041	00000000h
8h	4	"PM_CFG - Power Management Configuration (PMC_CFG)—Offset 8h" on page 3043	00000000h
Ch	4	"VLV_PM_STS - VLV Power Management Status (VLV_PM_STS)—Offset Ch" on page 3044	00000000h
10h	4	"MTPMC - Message to PMC (MTPMC)—Offset 10h" on page 3045	00000000h
20h	4	"General PM Configuration 1 (GEN_PMCON1)—Offset 20h" on page 3046	00004004h
24h	4	"General PM Configuration 2 (GEN_PMCON2)—Offset 24h" on page 3050	00000000h
28h	4	"MFPMC - Message from PMC (MFPMC)—Offset 28h" on page 3051	00000000h
2Ch	4	"SEC_STS - SEC Status (SEC_STS)—Offset 2Ch" on page 3052	00000000h
30h	4	"Configured Revision ID (CRID)—Offset 30h" on page 3053	00000000h
34h	4	"Function Disable (FUNC_DIS)—Offset 34h" on page 3053	00000000h
38h	4	"Function Disable 2 (FUNC_DIS_2)—Offset 38h" on page 3054	00000000h
3Ch	4	"S0ix wake enable (S0IX_WAKE_EN)—Offset 3Ch" on page 3055	00FFFFFFh
40h	4	"S0ix wake Status (S0IX_WAKE_STS)—Offset 40h" on page 3057	00000000h
44h	4	"S0ix control (S0IX_CTL)—Offset 44h" on page 3058	00000050h
48h	4	"ETR - Extended Test Mode Register (ETR)—Offset 48h" on page 3059	00230000h
50h	4	"VLT - Voltage Detect Register (VLT)—Offset 50h" on page 3060	00000000h
58h	4	"GPIO_ROUT - GPIO_ROUT register (GPIO_ROUT)—Offset 58h" on page 3060	00000000h
60h	4	"PLT_CLK_CTL_0 - Platform Clock Control 0 (PLT_CLK_CTL_0)—Offset 60h" on page 3061	00000003h
64h	4	"PLT_CLK_CTL_1 - Platform Clock Control 1 (PLT_CLK_CTL_1)—Offset 64h" on page 3062	00000003h
68h	4	"PLT_CLK_CTL_2 - Platform Clock Control 2 (PLT_CLK_CTL_2)—Offset 68h" on page 3062	00000003h
6Ch	4	"PLT_CLK_CTL_3 - Platform Clock Control 3 (PLT_CLK_CTL_3)—Offset 6Ch" on page 3063	00000003h
70h	4	"PLT_CLK_CTL_4 - Platform Clock Control 4 (PLT_CLK_CTL_4)—Offset 70h" on page 3064	00000003h
74h	4	"PLT_CLK_CTL_5 - Platform Clock Control 5 (PLT_CLK_CTL_5)—Offset 74h" on page 3064	00000003h
80h	4	"S0IR_TMR - S0I Ready Residency Timer (S0IR_TMR)—Offset 80h" on page 3065	00000000h
84h	4	"S0I1_TMR - S0I1 Residency Timer (S0I1_TMR)—Offset 84h" on page 3065	00000000h

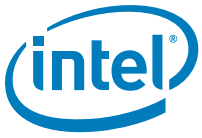


Table 63. Summary of PCU iLB PMC Memory Mapped I/O Registers—PMC_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
88h	4	"S0I2_TMR - S0I2 Residency Timer (S0I2_TMR)—Offset 88h" on page 3066	00000000h
8Ch	4	"S0I3_TMR - S0I3 Residency Timer (S0I3_TMR)—Offset 8Ch" on page 3066	00000000h
90h	4	"S0_TMR - S0 Residency Timer (S0_TMR)—Offset 90h" on page 3067	00000000h
98h	4	"PSS - Power island Power Status (PSS)—Offset 98h" on page 3067	00000000h
A0h	4	"D3_STS_0 - D3 Status register 0 (D3_STS_0)—Offset A0h" on page 3068	00000000h
A4h	4	"D3_STS_1 - D3 Status register 1 (D3_STS_1)—Offset A4h" on page 3069	00000000h
A8h	4	"D3_STDBY_STS_0 - D3 Standby Status register 0 (D3_STDBY_STS_0)—Offset A8h" on page 3069	00000000h
ACh	4	"D3_STDBY_STS_1 - D3 Standby Status register 1 (D3_STDBY_STS_1)—Offset ACh" on page 3070	00000000h
B0h	4	"MTPMC_1 - Message to PMC 1 (MTPMC_1)—Offset B0h" on page 3071	00000000h
B4h	4	"MTPMC_2 - Message to PMC 2 (MTPMC_2)—Offset B4h" on page 3072	00000000h
B8h	4	"MTPMC_3 - Message to PMC 3 (MTPMC_3)—Offset B8h" on page 3072	00000000h
BCh	4	"MTPMC_4 - Message to PMC 4 (MTPMC_4)—Offset BCh" on page 3073	00000000h
C0h	4	"PME Status 0 - Status bit for PME messages (PME_STS)—Offset C0h" on page 3073	00000000h
C4h	4	"GPE Level Edge mode (GPE_LEVEL_EDGE)—Offset C4h" on page 3074	00000000h
C8h	4	"GPE polarity mode (GPE_POLARITY)—Offset C8h" on page 3075	00000000h
CCh	4	"Lock Register (LOCK)—Offset CCh" on page 3075	00000000h
D0h	4	"Virtual UART register (VUART1)—Offset D0h" on page 3076	00000000h
D4h	4	"Virtual UART register (VUART2)—Offset D4h" on page 3077	00000000h
D8h	4	"Virtual UART register (VUART3)—Offset D8h" on page 3077	00000000h
DCh	4	"Virtual UART register (VUART4)—Offset DCh" on page 3077	00000000h

3.55.1 PRSTS - Power and Reset Status (PRSTS)—Offset 0h

Bits in this register only need to be valid for reading when the Main power well is up. However, since some of the events may initially be detected while the Main power well is down, they are marked as suspend well bits. All suspend well bits in this register are reset by global reset#.

Access Method

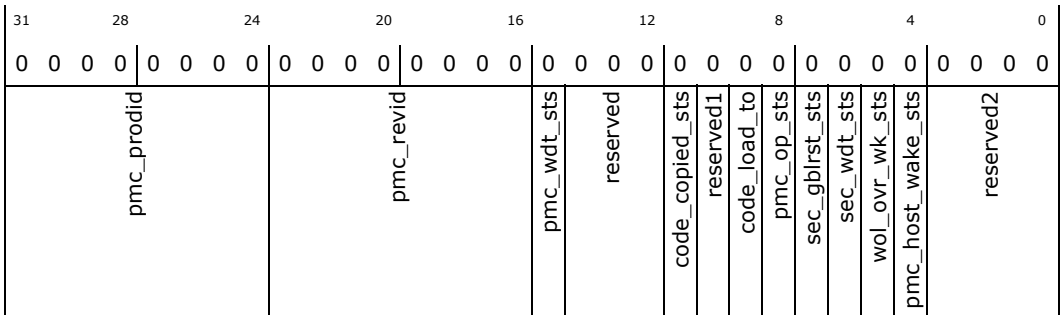
Type: Memory Mapped I/O Register (Size: 32 bits)

PRSTS: [PMC_BASE_ADDRESS] + 0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**Power Management Controller Product ID (PMC_PRODID) (pmc_prodid):** This field communicates the Product Family of the power management functionality
23:16	0b RO	**Power Management Controller Revision ID (PMC_REVID) (pmc_revid):** This field communicates the implementation revision of the power management functionality.
15	0b RW	**PMC Watchdog Timer Status (PMC_WDT_STS) (pmc_wdt_sts):** This bit will be set to '1' when the PMC Watch Dog Timer triggers a reset. It will be cleared by a write of '1' by software.
14:12	0b RO	**reserved:** Reserved.
11	0b RO	**Code Copied Over Status (CODE_COPIED_STS) (code_copied_sts):** The SOC sets this bit when PMC code is successfully authenticated and loaded from the flash
10	0b RO	**reserved (reserved1):** Reserved.
9	0b RO	**Code Load Timeout Status (CODE_LOAD_TO) (code_load_to):** The SOC sets this bit if the loading function fails to complete within a reasonable time limit. This bit remains valid after a PMC Code load is attempted until the next global reset
8	0b RO	**PMC Operational Status (PMC_OP_STS) (pmc_op_sts):** The SOC sets this bit when the PMC becomes operational after completing the Code Load. BIOS must wait for this bit to be set before performing resets or sleep events. This bit remains valid after a PMC Code load until the next global reset
7	0b RW	**SEC Watch Dog Timer Status (SEC_GBLRST_STS) (sec_gblrst_sts):** This bit will be set to '1' when the SEC FW triggers a reset. It will be cleared by a write of '1' by software.
6	0b RW	**SEC Watch Dog Timer Status (SEC_WDT_STS) (sec_wdt_sts):** This bit will be set to '1' when the SEC Watch Dog Timer triggers a reset. It will be cleared by a write of '1' by software.
5	0b RW	**Wake On LAN Override Wake Status (WOL_OVR_WK_STS) (wol_ovr_wk_sts):** This bit gets set when integrated LAN Signals a Power Management Event AND the system is in S5. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.

Bit Range	Default & Access	Description
4	0b RW	**PMC_HOST_WAKE_STS (PMC_HOST_WAKE_STS) (pmc_host_wake_sts):** The SOC Power Management Controller sets this bit if it wakes the host for reasons other than typical host-visible wake events. This status bit provides information to BIOS that the PMC caused the wake.
3:0	0b RO	**reserved2:** Reserved.

3.55.2 PM_CFG - Power Management Configuration (PMC_CFG)—Offset 8h

This register contains misc. fields used to configure the SOC's power management behavior.

Access Method

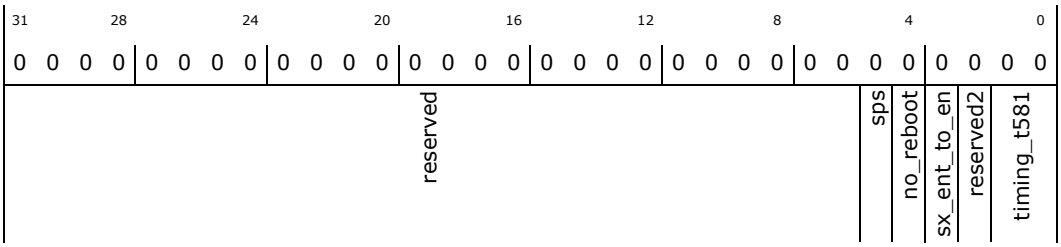
Type: Memory Mapped I/O Register (Size: 32 bits)

PMC_CFG: [PMC_BASE_ADDRESS] + 8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RO	**reserved:** Reserved.
5	0b RW	**Shutdown Policy Select (SPS) (sps):** When cleared (default) the SOC will drive INIT# in response to the shutdown Message. When set to 1, SOC will treat the shutdown message similar to receiving a CF9h I/O write, and will drive PMU_PLTRST active. . BIOS guide note: This register is reset any time PMU_PLTRST asserts.
4	0b RW	**No Reboot (NO_REBOOT) (no_reboot):** This bit is set when the No Reboot strap is sampled high on COREPWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates No Reboot. When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.

Bit Range	Default & Access	Description
3	0b RW	**S1/3/4/5 Entry Timeout Enable (SX_ENT_TO_EN) (sx_ent_to_en):** This policy bit determines whether the SOC will apply a timeout to the S1/S3/S4/S5 entry flow. If this timeout is enabled and the entry flow appears to be hung, the SOC will trigger a straight-to-S5 global reset. Encodings: 0: Timeout disabled (default) 1: Timeout enabled reset_type=RSMRST_B
2	0b RO	**reserved (reserved2):** Reserved.
1:0	0b RW	**Timing t581 (TIMING_T581) (timing_t581):** This field configures the t581 timing involved in the power down flow (CPU Power Good indication inactive to PLL Enable inactive). Encodings (all min timings): 00: 10 us (default) 01: 100 us 10: 1 ms 11: 10 ms reset_type=Resume Well Reset#

3.55.3 VLV_PM_STS - VLV Power Management Status (VLV_PM_STS)—Offset Ch

This register contains misc. fields used to record events pertaining to SOC power management. Unless otherwise indicated, all RWC bits are cleared with a write of 1 by software.

Access Method

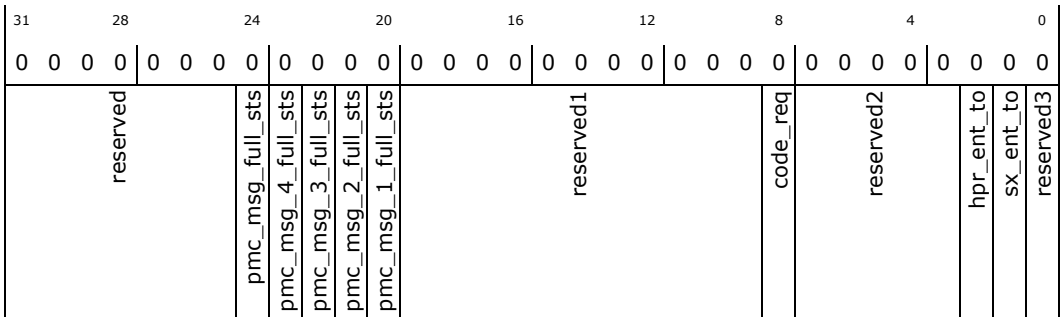
Type: Memory Mapped I/O Register (Size: 32 bits)

VLV_PM_STS: [PMC_BASE_ADDRESS] + Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RO	**reserved:** Reserved.
24	0b RO	**PMC Message Full Status (PMC_MSG_FULL_STS) (pmc_msg_full_sts):** 'This bit gets set to 1b automatically when the MTPMC register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.

Bit Range	Default & Access	Description
23	0b RO	**PMC Message 4 Full Status (PMC_MSG_4_FULL_STS) (pmc_msg_4_full_sts):** This bit gets set to 1b automatically when the Message to PMC 4 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
22	0b RO	**PMC Message 3 Full Status (PMC_MSG_3_FULL_STS) (pmc_msg_3_full_sts):** This bit gets set to 1b automatically when the Message to PMC 3 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
21	0b RO	**PMC Message 2 Full Status (PMC_MSG_2_FULL_STS) (pmc_msg_2_full_sts):** This bit gets set to 1b automatically when the Message to PMC 2 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
20	0b RO	**PMC Message 1 Full Status (PMC_MSG_1_FULL_STS) (pmc_msg_1_full_sts):** This bit gets set to 1b automatically when the Message to PMC 1 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
19:9	0b RO	**reserved1:** Reserved.
8	0b RO	**Code Requested (CODE_REQ) (code_req):** PMC will set this bit when SEC unit requests exclusion from power flows
7:3	0b RO	**reserved2:** Reserved.
2	0b RW	**Host Partition Reset Entry Timeout (HPR_ENT_TO) (hpr_ent_to):** This bit is set to '1' to record that a global reset was triggered by a timeout during Host partition reset entry sequence.
1	0b RW	**S3/4/5 Entry Timeout (SX_ENT_TO) (sx_ent_to):** This bit is set to '1' to record that a global reset was triggered by a timeout during an S3, S4, or S5 entry sequence.
0	0b RO	**reserved3:** Reserved.

3.55.4 MTPMC - Message to PMC (MTPMC)—Offset 10h

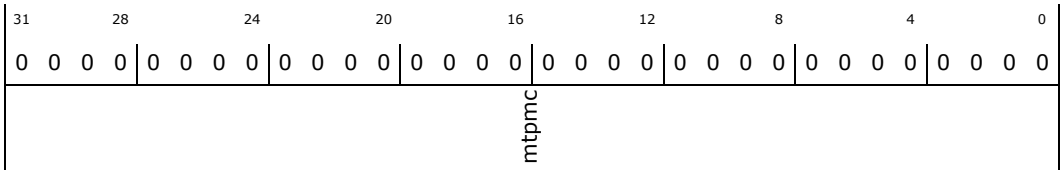
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MTPMC: [PMC_BASE_ADDRESS] + 10h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to any of the bytes in this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. In the case of a message that involves a response from the PMC (such as a PMC XRAM read), the host must also consume any data returned by the PMC in the Message from PMC register (MFPMC) before initiating another message

3.55.5 General PM Configuration 1 (GEN_PMCON1)—Offset 20h

Access Method

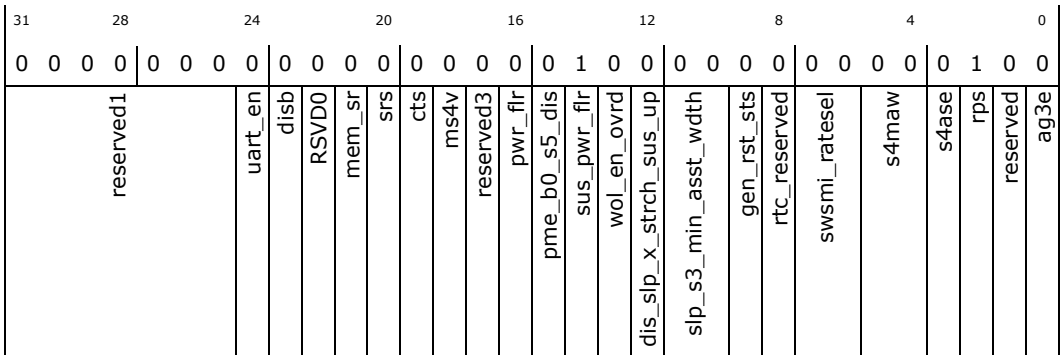
Type: Memory Mapped I/O Register (Size: 32 bits)

GEN_PMCON1: [PMC_BASE_ADDRESS] + 20h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00004004h



Bit Range	Default & Access	Description
31:25	0b RO	**reserved1:** Reserved.
24	0b RW	**UART Enable (UART_EN) (uart_en):** When set, PMC enables UART debug port

Bit Range	Default & Access	Description
23	0b RW	**DRAM Initialization Scratchpad Bit (DISB) (disb):** This bit does not effect hardware functionality in any way. It is provided as a scratchpad bit that is maintained through main power well resets and CF9h-initiated resets. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. If the bit is 1, then the DRAM initialization was interrupted. This bit is reset by the assertion of the RSMRST_B pin.
22	0b RO	**RSVD0:** Reserved
21	0b RO	**Memory Placed in Self-Refresh (MEM_SR) (mem_sr):** This bit will be set to 1 if DRAM should have remained powered and held in Self-Refresh through the last power state transition (i.e. the last time the system left S0). The scenarios where this should be the case are: - successful S3 entry and exit - successful Host partition reset without power cycle This bit will be cleared whenever the SOC begins a transition out of S0. Note: This bit should not be consulted upon wake from S1, as that state does not involve the same type of handshake or placing memory into Self-Refresh. It is assumed that software is already aware that memory context is not impacted by S1 and therefore does not need to check this bit. reset_type=global reset
20	0b RW	**System Reset Status (SRS) (srs):** SOC sets this bit when the PMU_RESETBUTTON_B# button is pressed. BIOS is expected to read this bit and clear it if it is set. This bit is also reset by RSMRST_B and CF9h resets. reset_type=Resume Well Reset#
19	0b RW	**CPU Thermal Trip Status (CTS) (cts):** This bit is set when the SOC thermal trip active while the system is in a valid state to honor the pin. This bit is also reset by RSMRST_B and CF9h resets. It is not reset by the shutdown and reboot associated with the thermal trip event. reset_type=Resume Well Reset#
18	0b RW	**Minimum PMU_SLP_S4_B Assertion Width Violation Status (MS4V) (ms4v):** Hardware sets this bit when the PMU_SLP_S4_B assertion width is less than the time programmed in the PMU_SLP_S4_B Minimum Assertion Width field. The SOC begins the timer when PMU_SLP_S4_B pin is asserted during S4/S5 entry, or when the RSMRST_B input is deasserted during SUS well power-up. The status bit is cleared by software writing a 1 to the bit. Note that this bit is functional regardless of the value in the PMU_SLP_S4_B Assertion Stretch Enable and the Disable-SLP_X-Stretching-After-SUS-Power-Failure bits. This bit is reset by the assertion of the RSMRST_B pin, but can be set in some cases before the default value is readable. reset_type=RSMRST_B
17	0b RO	**reserved3:** Reserved.
16	0b RW	**COREPWROK Failure (PWR_FLR) (pwr_flr):** Intel SOC sets this bit any time COREPWROK goes low if the system was in an S0 or S1 state. The bit will be cleared only by software writing a 1 back to the bit or by SUS well power loss. reset_type=global reset

Bit Range	Default & Access	Description
15	0b RW	**PME B0 S5 Disable (PME_B0_S5_DIS) (pme_b0_s5_dis):** When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'. Wakes from power states other than S5 are not affected by this policy bit. The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below: Y = Wake N = Don't wake B0 = PME_B0_EN OV = WOL Enable Override B0/OV | S1/S3/S4 | S5 00 | N | N 01 | N | Y (LAN only) 11 | Y (all PME B0 sources) | Y (LAN only) 10 | Y (all PME B0 sources) | N This bit is cleared by the SRTCRST_B pin. reset_type=SRTCRST_B
14	1b RW	**SUS Well Power Failure (SUS_PWR_FLR) (sus_pwr_flr):** This bit is set to '1' whenever SUS well power is lost, as indicated by RSMRST_B assertion. Software writes a 1 to this bit to clear it. This bit is in the SUS well, and defaults to '1' based on RSMRST_B assertion (not cleared by any type of reset). Implementation Note: RSMRST_B is an asynchronous set term to this bit. reset_type=RSMRST_B
13	0b RW	**WOL Enable Override (WOL_EN_OVRD) (wol_en_ovrd):** When this bit is set to 1, the integrated LAN is enabled to wake the system from S5 regardless of the value in the PME_B0_EN bit in the GPE0a_EN register. This allows the system BIOS to enable Wake-On-LAN regardless of the policies selected through the operating system. This bit is maintained in the RTC power well, therefore permitting WOL following a surprise power failure even in cases in which the system may have been running in S0 without the PME Enables set. (Note that the LAN NVRAM configuration must support WOL after SUS power loss.) When this bit is cleared to 0, the wake-on-LAN policies are determined by OS-visible bits. This bit has no effect on wakes from S1, S3, or S4. This bit is cleared by the SRTCRST_B pin reset_type=SRTCRST_B
12	0b RW	**Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP) (dis_slp_x_strch_sus_up):** When this bit is set to 1, all SLP_* pin stretching is disabled when powering up after a SUS well power loss. When this bit is left at 0, SLP_* stretching will be performed after SUS power failure as enabled in various other fields. Note that if this bit is a 0, SLP_* stretch timers start on SUS well power up (the SOC has no ability to count stretch time while the SUS well is powered down). Setting this bit can therefore prevent long delays after SUS power loss which may be common in mobile platforms and in manufacturing flow testing, while still allowing for the full power cycling during S3, S4 and S5 states. If the platform guarantees minimum SUS power down residence in other ways, an additional SOC-induced delay is not needed or wanted. This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by the SRTCRST_B pin.
11:10	0b RW	**PMU_SLP_S3_B Minimum Assertion Width (SLP_S3_MIN_ASST_WDTH) (slp_s3_min_asst_wdth):** This 2-bit value indicates the minimum assertion width of the PMU_SLP_S3_B signal to guarantee that the Main power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00: 60 usec 01: 1 ms 10: 50 ms 11: 2 sec This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This bit is cleared by the RSMRST_B pin. reset_type=RSMRST_B

Bit Range	Default & Access	Description
9	0b RW	**General Reset Status (GEN_RST_STS) (gen_rst_sts):** This bit is set by hardware whenever PMU_PLTRST asserts for any reason other than going into a software-entered sleep state (via PM1_CNT.SLP_EN write). This bit is an optional tool to help BIOS determine when a reset might have collided with a wake from a valid sleep state. A possible usage model would be to consult and then write a '1' to clear this bit during the boot flow before determine what action to take based on reading PM1_STS.WAK_STS = '1'. If GEN_RST_STS = '1', the cold reset boot path could be followed rather than the resume path, regardless of the setting of WAK_STS. This bit does not affect SOC operation in any way, and can therefore be left set if BIOS chooses not to use it. This bit is set by global reset. reset_type=global reset
8	0b RW	**RTC_reserved (rtc_reserved):** reset_type=SRTCRST_B
7:6	0b RW	**SWSMI Rate Select (SWSMI_RATESEL) (swsmi_ratesel):** This 2-bit value indicates when the SWSMI timer will time out. Valid values are: 00 1.5ms +/- 0.6ms 01 16ms +/- 4ms 10 32ms +/- 4ms 11 64ms +/- 4ms These bits are not cleared by any type of reset except SRTCRST_B. Implementation Note: SWSMI is generated based on the internal free-running 1ms tick (to be accurate, it is 0.983ms/tick generated from 30ns * 2^15). Since the tick is free-running, the accuracy is within the following range. # of 0.983ms tick count SWSMI range 64ms SWSMI 62 -to- 63 60.946ms -to- 61.929ms 32ms SWSMI 31 -to- 32 30.473ms -to- 31.456ms 16ms SWSMI 15 -to- 16 14.745ms -to- 15.728ms 1.5ms SWSMI 1 -to- 2 0.983ms -to- 1.966ms reset_type=SRTCRST_B
5:4	0b RW	**PMU_SLP_S4_B Minimum Assertion Width (S4MAW) (s4maw):** This 2-bit value indicates the minimum assertion width of the PMU_SLP_S4_B signal to guarantee that the DRAMs have been safely power-cycled. This value may be modified per platform depending on DRAM types, power supply capacitance, etc. Valid values are: - 11: 1 second - 10: 2 seconds - 01: 3 seconds - 00: 4 seconds This value is used in two ways: 1. If the PMU_SLP_S4_B assertion width is ever shorter than this time, a status bit is set for BIOS to read when S0 is entered 2. If enabled by bit 3 in this register, the hardware will prevent the PMU_SLP_S4_B signal from deasserting within this minimum time period after asserting. Note that the logic that measures this time is in the suspend power well. Therefore, when leaving a G3 state, the minimum time is measured from the deassertion of the internal suspend well reset (unless the Disable SLP_X Stretching After SUS Power Failure bit is set). This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. SRTCRST_B forces this field to the conservative default state (00b). reset_type=SRTCRST_B

Bit Range	Default & Access	Description
3	0b RW	**PMU_SLP_S4_B Assertion Stretch Enable (S4ASE) (s4ase):** When set to 1, the PMU_SLP_S4_B pin will minimally assert for the time specified in bits 5:4 of this register. This bit is provided so that all DIMMs in the system can deterministically detect a power-cycle event for proper initialization. Note that there are behavioral changes that may be noticeable to the end-user when this bit is set. Resume times from S4 and S5 and power-up times from G3 may be delayed by several seconds. Cases in which this feature may not be desirable and therefore keeping the bit cleared are: - A customer decides the user confusion due to the hardware delay is a bigger issue than the potential DRAM issue - A customer decides the software status bit solution is adequate - A different DRAM type is used or the platform provides an external solution to solve the power-cycling issue - Validation regressions are impacted by the delay (especially after RSMRST_B deassertion) - Avoid potential resume time WHQL violations This bit is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by SRTCRST_B. reset_type=SRTCRST_B
2	1b RW	**RTC_PWR_STS (RPS) (rps):** Intel SOC will set this bit to 1 when RTEST_B indicates a weak or missing battery. The bit will remain set until the software clears it by writing a 0 back to this bit position. This bit is not cleared by any type of reset. reset_type=RTEST_B
1	0b RO	**reserved:** Reserved.
0	0b RW	**AFTERG3_EN (AG3E) (ag3e):** Determines what state to go to when power is reapplied after a power failure (G3 state). 0 = System will return to an S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4-like state). In the S5 state, the only enabled wake-up event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well and is only cleared by SRTCRST_B assertion. reset_type=SRTCRST_B

3.55.6 General PM Configuration 2 (GEN_PMCON2)—Offset 24h

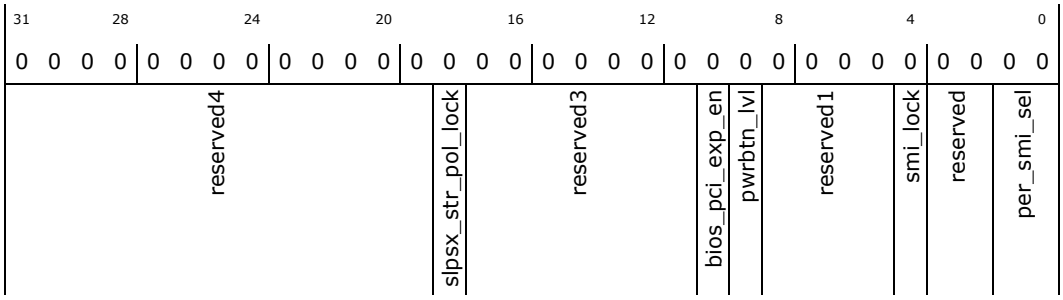
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GEN_PMCON2: [PMC_BASE_ADDRESS] + 24h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0b RO	**reserved (reserved4):** Reserved.
18	0b RW	**SLP_Sx# Stretching Policy Lock-Down (SLPSX_STR_POL_LOCK) (slpsx_str_pol_lock):** When set to 1, this bit locks down the following fields: - GEN_PMCON_1.DIS_SLP_X_STRCH_SUSPF - GEN_PMCON_1.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_1.S4MAW - GEN_PMCON_1.S4ASE Those bits become read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.
17:11	0b RO	**reserved (reserved3):** Reserved.
10	0b RW	**BIOS PCI Express Enable (BIOS_PCI_EXP_EN) (bios_pci_exp_en):** This bit acts as a global enable for the SCI associated with the PCI express ports. If this bit is not set, then the various PCI Express ports cannot cause the PCI_EXP_STS bit to go active.
9	0b RO	**Power Button Level (PWRBTN_LVL) (pwrbtn_lvl):** This read-only bit indicates the current state of the PMU_PWRBTN_B signal. 1= High, 0 = Low. The value reflected in this bit is the debounced PMU_PWRBTN_B pin value that is seen at the output of a 16ms debouncer.
8:5	0b RO	**reserved (reserved1):** Reserved.
4	0b RW	**SMI Lock (SMI_LOCK) (smi_lock):** When this bit is set, writes to the GBL_SMI_EN bit will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by PMU_PLTRST).
3:2	0b RO	**reserved:** Reserved.
1:0	0b RW	**Period SMI Select (PER_SMI_SEL) (per_smi_sel):** Software sets these bits to control the rate at which the periodic SMI# is generated: 00 = 64 seconds (default), 01 = 32 seconds, 10 = 16 seconds, 11 = 8 seconds Tolerance for the timer is +/- 1 second.

3.55.7 MFPMC - Message from PMC (MFPMC)—Offset 28h

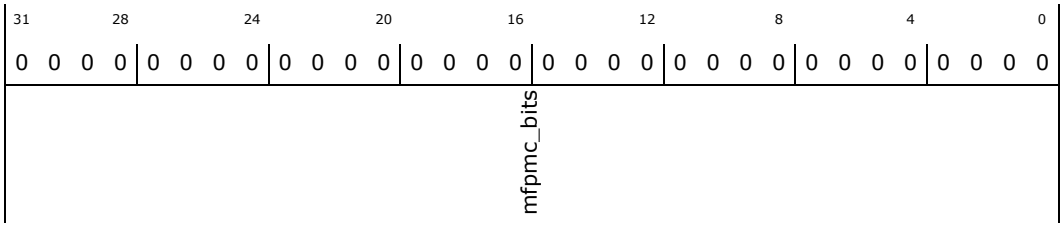
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MFPMC: [PMC_BASE_ADDRESS] + 28h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Message from PMC (MFPMC) (mfpmc_bits):** The data in this register is typically updated in response to a host write to the MTPMC register.

3.55.8 SEC_STS - SEC Status (SEC_STS)—Offset 2Ch

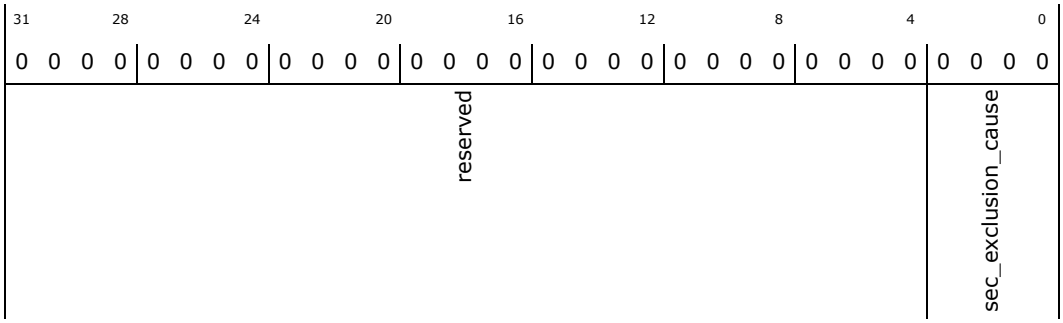
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SEC_STS: [PMC_BASE_ADDRESS] + 2Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0b RO	**reserved:** Reserved.
3:0	0b RW	**SEC_EXCLUSION_CAUSE (sec_exclusion_cause):** The cause associated with SeC setting requesting exclusion from power flows in SEC_EXCLUSION_REQ field. 0000b: SeC FW Fault Tolerant Initialization failed. 0001b: SeC FLASH Descriptor Override invoked. 0010b: SeC disabled using SW means (such as OEM setting). 0011b: Post-boot SeC applications not supported. 0100b: ROM BIST failure. 0101b: Fuse unit completed with unsupported request for group 1. 0110b: Invalid fuses bit at line 3 of group 1 fuses wasn't written with value 0. 0111b: DRAM Initialization by BIOS failed. Other values reserved.

3.55.9 Configured Revision ID (CRID)—Offset 30h

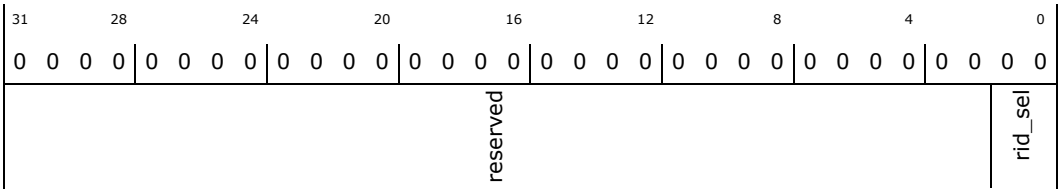
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRID: [PMC_BASE_ADDRESS] + 30h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**reserved:** Reserved.
1:0	0b RW	**RID Select(RID_SEL) (rid_sel):** Software writes this field to select the Revision ID reflected in PCI config space. The decoding is: 00 - Revision ID 01 - CRID 0 10 - CRID 1 11 - CRID 2 Once written, this field can only be cleared by a platform reset. reset_type=PMU_PLTRST

3.55.10 Function Disable (FUNC_DIS)—Offset 34h

BIOS uses this register to disable specific function. Upon writing this register PMC will set the corresponding Function Disable bit in the PSF

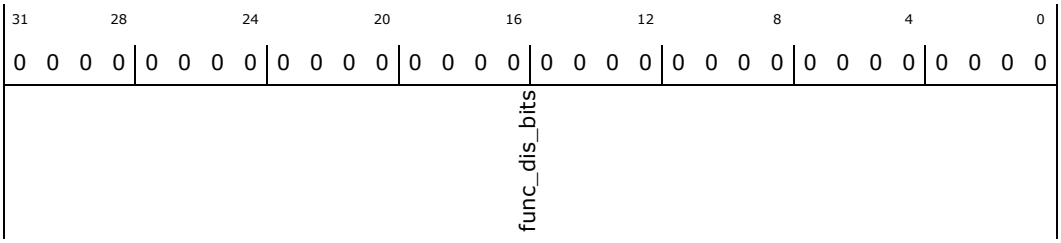
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FUNC_DIS: [PMC_BASE_ADDRESS] + 34h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**FUNC_DIS_BITS (func_dis_bits):** When a bit is set, the corresponding function should be disabled. 31 LPSS2_F7_Disable LPSS2 Function7 (I2C#7) Disable. 1'b1: Disable 1'b0: Enable 30 LPSS2_F6_Disable LPSS2 Function6 (I2C#6) Disable. 1'b1: Disable 1'b0: Enable 29 LPSS2_F5_Disable LPSS2 Function5 (I2C#5) Disable. 1'b1: Disable 1'b0: Enable 28 LPSS2_F4_Disable LPSS2 Function4 (I2C#4) Disable. 1'b1: Disable 1'b0: Enable 27 LPSS2_F3_Disable LPSS2 Function3 (I2C#3) Disable. 1'b1: Disable 1'b0: Enable 26 LPSS2_F2_Disable LPSS2 Function2 (I2C#2) Disable. 1'b1: Disable 1'b0: Enable 25 LPSS2_F1_Disable LPSS2 Function1 (I2C#1) Disable. 1'b1: Disable 1'b0: Enable 24 LPSS2_F0_Disable LPSS2 Function0 (DMA) Disable. 1'b1: Disable 1'b0: Enable 23 PCIe_P3_Disable PCIe Port3 Disable. 1'b1: Disable 1'b0: Enable 22 PCIe_P2_Disable PCIe Port2 Disable. 1'b1: Disable 1'b0: Enable 21 PCIe_P1_Disable PCIe Port1 Disable. 1'b1: Disable 1'b0: Enable 20 PCIe_P0_Disable PCIe Port0 Disable. 1'b1: Disable 1'b0: Enable 19 Reserved2 reserved 18 USB_Disable USB2 (EHCI) Disable. 1'b1: Disable 1'b0: Enable 17 SATA_Disable SATA Disable. 1'b1: Disable 1'b0: Enable 16 LAN_Disable LAN Disable. 1'b1: Disable 1'b0: Enable 15 USH_Disable USH Disable. 1'b1: Disable 1'b0: Enable 14 OTG_Disable OTG Disable. 1'b1: Disable 1'b0: Enable 13 LPE_Disable LPE Disable. 1'b1: Disable 1'b0: Enable 12 HDA_Disable HDA Disable. 1'b1: Disable 1'b0: Enable 11 SCC_MIPI_Disable MIPI-HSI Disable. 1'b1: Disable 1'b0: Enable 10 SCC_SDCARD_Disable SDCARD Disable. 1'b1: Disable 1'b0: Enable 9 SCC_SDIO_Disable SDIO Disable. 1'b1: Disable 1'b0: Enable 8 SCC_eMMC_Disable eMMC Disable. 1'b1: Disable 1'b0: Enable 7 LPSS1_F7_Disable Reserved for LPSS1 function 7 6 LPSS1_F6_Disable Reserved for LPSS1 function 6 5 LPSS1_F5_Disable PSS1 Function5 (SPI) Disable. 1'b1: Disable 1'b0: Enable 4 LPSS1_F4_Disable LPSS1 Function4 (HSUART#2) Disable. 1'b1: Disable 1'b0: Enable 3 LPSS1_F3_Disable LPSS1 Function3 (HSUART#1) Disable. 1'b1: Disable 1'b0: Enable 2 LPSS1_F2_Disable LPSS1 Function2 (PWM#2) Disable. 1'b1: Disable 1'b0: Enable 1 LPSS1_F1_Disable LPSS1 Function1 (PWM#1) Disable. 1'b1: Disable 1'b0: Enable 0 LPSS1_F0_Disable LPSS1 Function0 (DMA) Disable. 1'b1: Disable 1'b0: Enable

3.55.11 Function Disable 2 (FUNC_DIS_2)—Offset 38h

BIOS uses this register to disable specific function. Upon writing this register PMC will set the corresponding Function Disable bit in the PSF

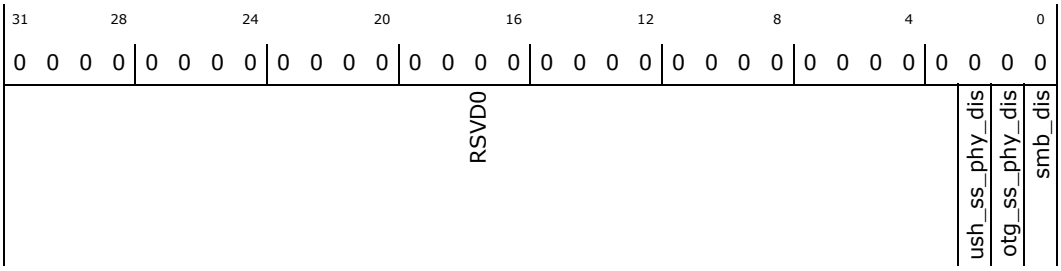
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FUNC_DIS_2: [PMC_BASE_ADDRESS] + 38h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RO	**RSVD0:** Reserved
2	0b RW	**USH_SS_PHY_DIS (ush_ss_phy_dis):** When this bit is set, USH Super Speed PHY should be disabled.
1	0b RW	**OTG_SS_PHY_DIS (otg_ss_phy_dis):** When this bit is set, OTG Super Speed PHY should be disabled.
0	0b RW	**SMB_DIS (smb_dis):** When this bit is set, SMB function should be disabled.

3.55.12 S0ix wake enable (S0IX_WAKE_EN)—Offset 3Ch

This register contains wake enable bit per S0ix wake event. Note: Common wake events with sleep sates have their wake enables in the ACPI space.

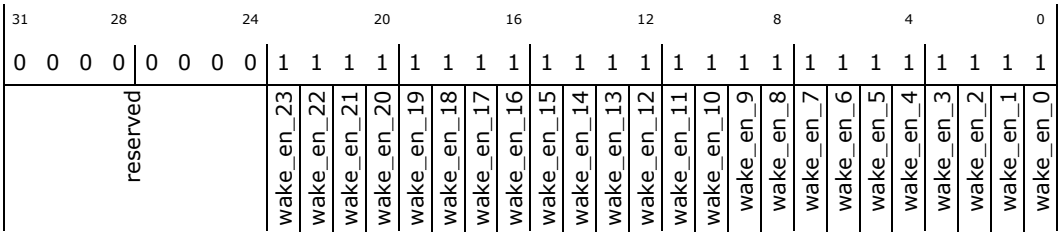
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

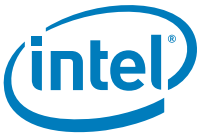
S0IX_WAKE_EN: [PMC_BASE_ADDRESS] + 3Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00FFFFFFh



Bit Range	Default & Access	Description
31:24	0b RO	**Reserved (reserved):** Reserved.
23	1b RW	**WAKE_EN_23 (wake_en_23):** wake enable bit 23 - Spare bit
22	1b RW	**WAKE_EN_22 (wake_en_22):** wake enable bit 22 - Spare bit



Bit Range	Default & Access	Description
21	1b RW	**WAKE_EN_21 (wake_en_21):** wake enable bit 21 - Spare bit
20	1b RW	**WAKE_EN_20 (wake_en_20):** wake enable bit 20 - Shared IRQ from GPSS
19	1b RW	**WAKE_EN_19 (wake_en_19):** wake enable bit 19 - Ored dedicated IRQs from GPSC
18	1b RW	**WAKE_EN_18 (wake_en_18):** wake enable bit 18 - Ored dedicated IRQs from GPSS
17	1b RW	**WAKE_EN_17 (wake_en_17):** wake enable bit 17 - Wake LAN
16	1b RW	**WAKE_EN_16 (wake_en_16):** wake enable bit 16 - Pending NMI
15	1b RW	**WAKE_EN_15 (wake_en_15):** wake enable bit 15 - SCI
14	1b RW	**WAKE_EN_14 (wake_en_14):** wake enable bit 14 - SMI
13	1b RW	**WAKE_EN_13 (wake_en_13):** wake enable bit 13 - OTG wake
12	1b RW	**WAKE_EN_12 (wake_en_12):** wake enable bit 12 - AONT Si03 wake
11	1b RW	**WAKE_EN_11 (wake_en_11):** wake enable bit 11 - AONT Si02 wake
10	1b RW	**WAKE_EN_10 (wake_en_10):** wake enable bit 10 - AONT Si01 wake
9	1b RW	**WAKE_EN_9 (wake_en_9):** wake enable bit 9 - IOAPIC delivery status
8	1b RW	**WAKE_EN_8 (wake_en_8):** wake enable bit 8 - Shared IRQ from GPNC
7	1b RW	**WAKE_EN_7 (wake_en_7):** wake enable bit 7 - GPE from GPSS
6	1b RW	**WAKE_EN_6 (wake_en_6):** wake enable bit 6 - GPE from GPSC
5	1b RW	**WAKE_EN_5 (wake_en_5):** wake enable bit 5 - Shared IRQ from GPSC
4	1b RW	**WAKE_EN_4 (wake_en_4):** wake enable bit 4 - LPC Clock run
3	1b RW	**WAKE_EN_3 (wake_en_3):** wake enable bit 3 - SEC Timers
2	1b RW	**WAKE_EN_2 (wake_en_2):** wake enable bit 2 - LPE IPC
1	1b RW	**WAKE_EN_1 (wake_en_1):** wake enable bit 1 - LPE wake
0	1b RW	**WAKE_EN_0 (wake_en_0):** wake enable bit 0 - NFC wake

3.55.13 S0ix wake Status (S0IX_WAKE_STS)—Offset 40h

This register contains wake status bits per S0ix wake event. Note: Common wake events with sleep sates have their wake enables in the ACPI space.

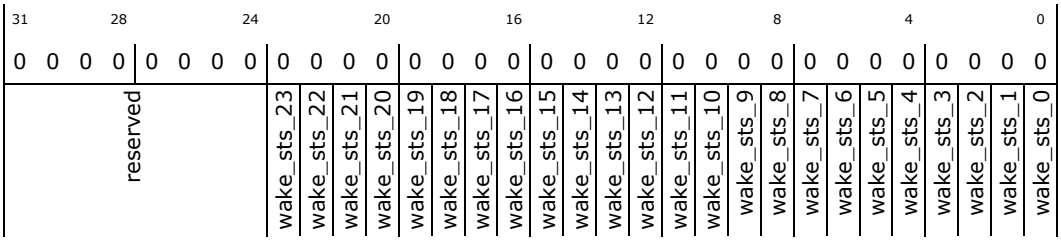
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0IX_WAKE_STS: [PMC_BASE_ADDRESS] + 40h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**Reserved (reserved):** Reserved.
23	0b RW	**WAKE_STS_23 (wake_sts_23):** wake status bit 23 - Spare bit
22	0b RW	**WAKE_STS_22 (wake_sts_22):** wake status bit 22 - Spare bit
21	0b RW	**WAKE_STS_21 (wake_sts_21):** wake status bit 21 - Spare bit
20	0b RW	**WAKE_STS_20 (wake_sts_20):** wake status bit 20- Shared IRQ from GPSS
19	0b RW	**WAKE_STS_19 (wake_sts_19):** wake status bit 19 - Ored dedicated IRQs from GPSC
18	0b RW	**WAKE_STS_18 (wake_sts_18):** wake status bit 18 - Ored dedicated IRQs from GPSS
17	0b RW	**WAKE_STS_17 (wake_sts_17):** wake status bit 17 - Wake LAN
16	0b RW	**WAKE_STS_16 (wake_sts_16):** wake status bit 16 - Pending NMI
15	0b RW	**WAKE_STS_15 (wake_sts_15):** wake status bit 15 - SCI
14	0b RW	**WAKE_STS_14 (wake_sts_14):** wake status bit 14 - SMI
13	0b RW	**WAKE_STS_13 (wake_sts_13):** wake status bit 13 - OTG wake
12	0b RW	**WAKE_STS_12 (wake_sts_12):** wake status bit 12 - AONT Si03 wake

Bit Range	Default & Access	Description
11	0b RW	**WAKE_STS_11 (wake_sts_11):** wake status bit 11 - AONT Si02 wake
10	0b RW	**WAKE_STS_10 (wake_sts_10):** wake status bit 10 - AONT Si01 wake
9	0b RW	**WAKE_STS_9 (wake_sts_9):** wake status bit 9 - IOAPIC delivery status
8	0b RW	**WAKE_STS_8 (wake_sts_8):** wake status bit 8 - Shared IRQ from GPNC
7	0b RW	**WAKE_STS_7 (wake_sts_7):** wake status bit 7 - GPE from GPSS
6	0b RW	**WAKE_STS_6 (wake_sts_6):** wake status bit 6- GPE from GPSC
5	0b RW	**WAKE_STS_5 (wake_sts_5):** wake status bit 5 - Shared IRQ from GPSC
4	0b RW	**WAKE_STS_4 (wake_sts_4):** wake status bit 4 - LPC Clock run
3	0b RW	**WAKE_STS_3 (wake_sts_3):** wake status bit 3 - SEC Timers
2	0b RW	**WAKE_STS_2 (wake_sts_2):** wake status bit 2 - LPE IPC
1	0b RW	**WAKE_STS_1 (wake_sts_1):** wake status bit 1 - LPE wake
0	0b RW	**WAKE_STS_0 (wake_sts_0):** wake status bit 0 - NFC wake

3.55.14 S0ix control (S0IX_CTL)—Offset 44h

This register contains S0ix miscellaneous controls

Access Method

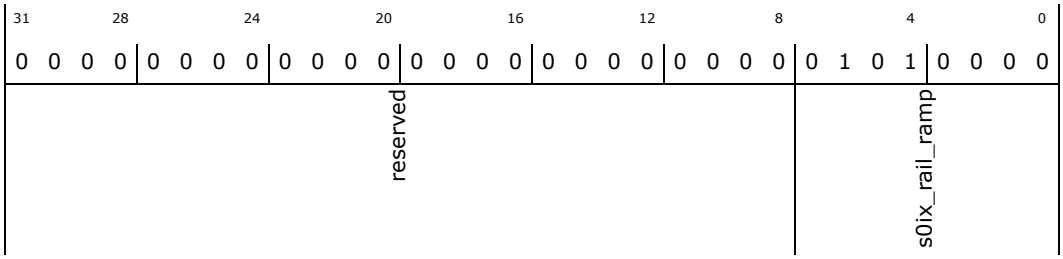
Type: Memory Mapped I/O Register (Size: 32 bits)

S0IX_CTL: [PMC_BASE_ADDRESS] + 44h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000050h



Bit Range	Default & Access	Description
31:8	0b RO	**Reserved (reserved):** Reserved.
7:0	50h RW	**S0IX_RAIL_RAMP (s0ix_rail_ramp):** specifies S0IX rail ramp time

3.55.15 ETR - Extended Test Mode Register (ETR)—Offset 48h

This register resides in the resume well. All bits except bit[23:16] are reset by internal Resume Well Reset. Bit[23:16] are reset by RSMRST_B only.

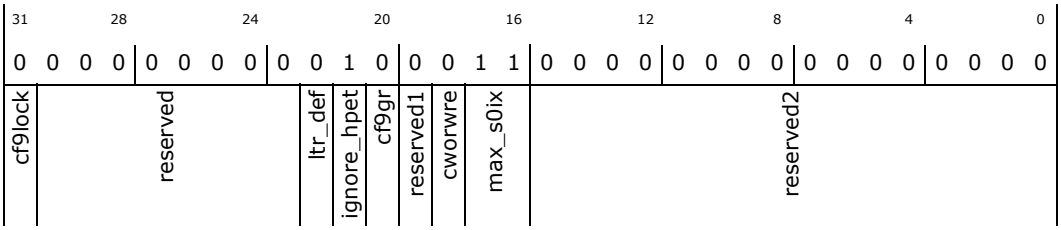
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ETR: [PMC_BASE_ADDRESS] + 48h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00230000h



Bit Range	Default & Access	Description
31	0b RW	**CF9h Lockdown (CF9LOCK) (cf9lock):** When set, this will lock the CF9h-Global-Reset bit. When set, this register locks itself. This register is reset by a CF9h reset.
30:23	0b RO	**reserved:** Reserved.
22	0b RW	**LTR default (LTR_DEF) (ltr_def):** When this bit is cleared, PMC will assume low LTR by default. When set, PMC will assume high LTR by default
21	1b RW	**Ignore HPET When going to S0i2 (IGNORE_HPET) (ignore_hpet):** When this bit is set, PMC will not check for HPET disabled before going to S0i2
20	0b RW	**CF9h Global Reset (CF9GR) (cf9gr):** When this bit is set, a CF9h write of 6h or Eh will cause a Global Reset of the Host partition. If this bit is cleared, a CF9h write of 6h or Eh will only reset the Host partition. It is recommended that BIOS should set this bit early on in the boot sequence, and then clear it and set the CF9LOCK bit prior to loading the OS. When this bit is set, the hardware assumes that bit 18 (CF9h Without Resume Well Reset Enable) is cleared. This register is locked by the CF9 Lockdown (CF9LOCK) bit. This register is not reset by a CF9h reset. reset_type=RSMRST_B
19	0b RO	**reserved (reserved1):** Reserved.

Bit Range	Default & Access	Description
18	0b RW	**CF9h Without Resume Well Reset Enable (CWORWRE) (cworwre):** When this bit is set, a CF9h write of 6h or Eh will not cause internal Resume Well Reset (WrsmrstB) to be asserted and thus resume well logic will maintain its state. When this bit is cleared, CF9h write of 6h or Eh will also reset resume well logic. This bit is to be used when a second reset through CF9 write is desired upon power up or after resume from low power states. This bit has to be set prior to the write to CF9 register and has to be cleared upon completing the reset. Failing to do so prevents resume well registers from being reset in the future CF9 writes. reset_type=RSMRST_B
17:16	11b RW	**MAX_S0IX (MAX_S0IX (max_s0ix):** Indicated the maximum S0i state SOC can go
15:0	0b RO	**reserved (reserved2):** Reserved.

3.55.16 VLT - Voltage Detect Register (VLT)—Offset 50h

This register reflects the Voltage detect fuses.

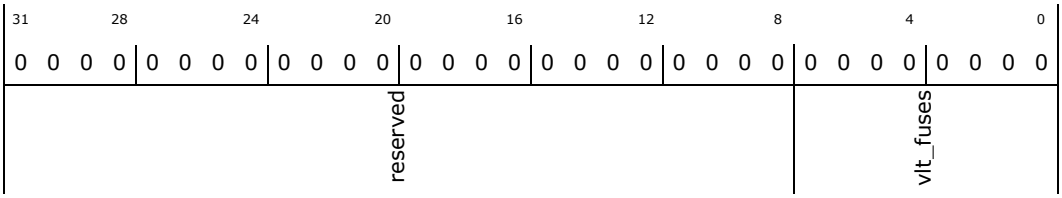
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VLT: [PMC_BASE_ADDRESS] + 50h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RO	**VLT Fuses (VLT_FUSES) (vlt_fuses):** These bits reflects the Voltage detect fuses

3.55.17 GPIO_ROUT - GPIO_ROUT register (GPIO_ROUT)—Offset 58h

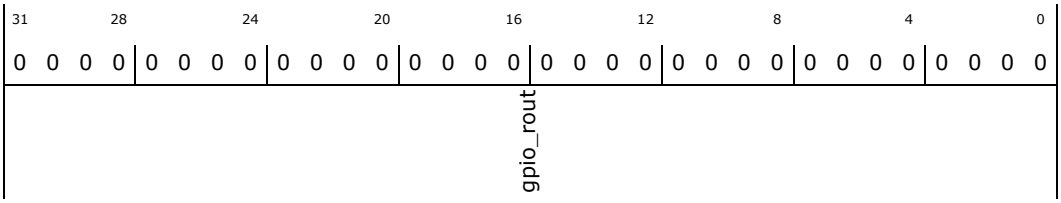
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPIO_ROUT: [PMC_BASE_ADDRESS] + 58h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**GPIO Rout (GPIO_ROUT) (gpio_rout):** Bits [15:0] determines GPIO SUS events rout. Bits [31:16] determines GPIO CORE events rout. Bits [1:0] determines GPIO SUS event 0. Bits [3:2] determines GPIO SUS event 1 and so on. Bits [17:16] determines GPIO CORE event 0. Bits [19:18] determines GPIO CORE event 1 and so on. If the corresponding GPIO is implemented and is set to an input, a '1' in the GP_LVL bit can be routed to cause an interrupt. If the GPIO is not set to an input, this field has no effect. * 00 No effect (or GPIO unimplemented), * 01 SMI# (if corresponding ALT_GPIO_SMI bit also set), * 10 SCI (if corresponding GPE0a_EN bit also set), * 11 Reserved If the system is in an S0-S5 state and if the GPE0a_EN bit is also set, then the GPIO can cause a Wake event, even if the GPIO is NOT routed to cause an interrupt. Exception: If the system is in S5 state due to a powerbutton override, then the GPIO's will not cause wake events. Note: Core well GPIO's are not capable of waking the system from sleep states where the core well is not powered.

3.55.18 PLT_CLK_CTL_0 - Platform Clock Control 0 (PLT_CLK_CTL_0)—Offset 60h

This register controls Platform clocks.

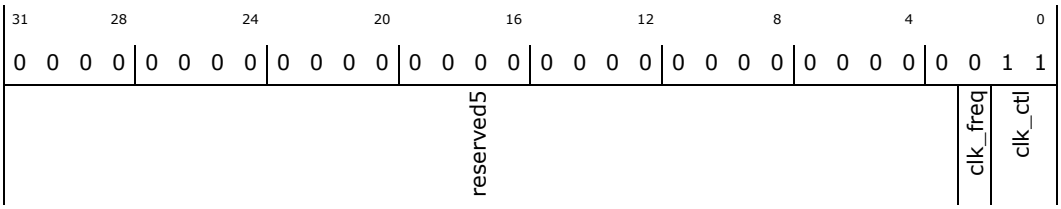
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_0: [PMC_BASE_ADDRESS] + 60h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

3.55.19 PLT_CLK_CTL_1 - Platform Clock Control 1 (PLT_CLK_CTL_1)—Offset 64h

This register controls Platform clocks.

Access Method

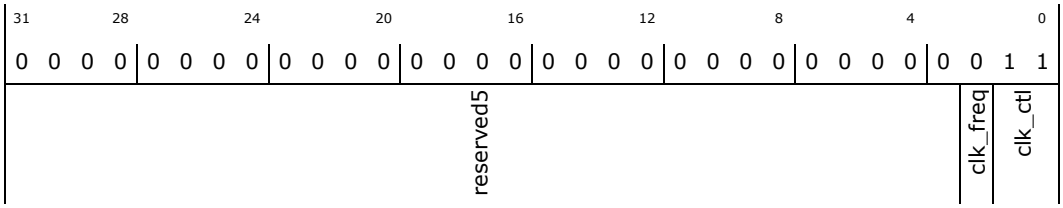
Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_1: [PMC_BASE_ADDRESS] + 64h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

3.55.20 PLT_CLK_CTL_2 - Platform Clock Control 2 (PLT_CLK_CTL_2)—Offset 68h

This register controls Platform clocks.

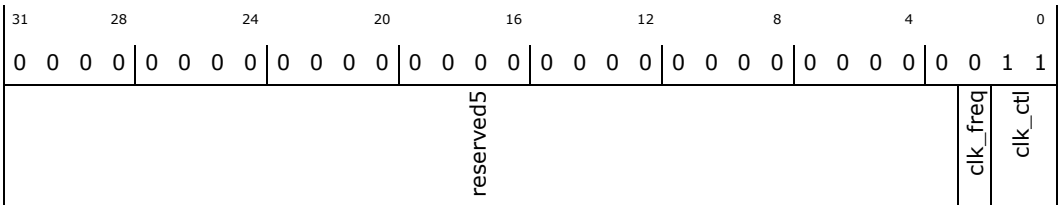
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_2: [PMC_BASE_ADDRESS] + 68h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

3.55.21 PLT_CLK_CTL_3 - Platform Clock Control 3 (PLT_CLK_CTL_3)—Offset 6Ch

This register controls Platform clocks.

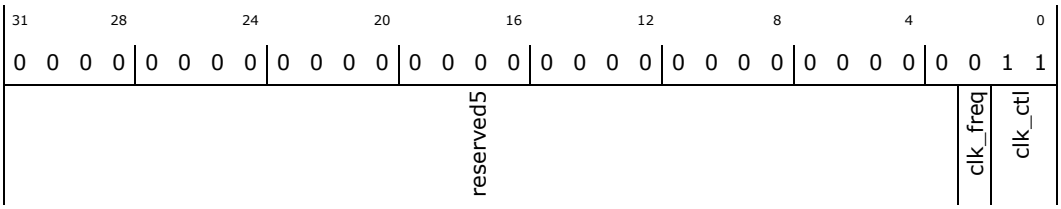
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_3: [PMC_BASE_ADDRESS] + 6Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)

Bit Range	Default & Access	Description
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

3.55.22 PLT_CLK_CTL_4 - Platform Clock Control 4 (PLT_CLK_CTL_4)—Offset 70h

This register controls Platform clocks.

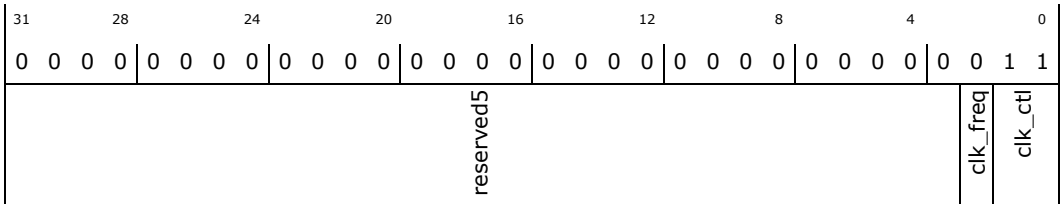
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_4: [PMC_BASE_ADDRESS] + 70h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

3.55.23 PLT_CLK_CTL_5 - Platform Clock Control 5 (PLT_CLK_CTL_5)—Offset 74h

This register controls Platform clocks.

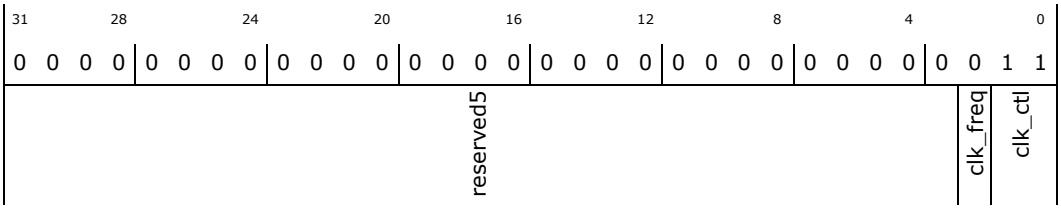
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_5: [PMC_BASE_ADDRESS] + 74h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

3.55.24 S0IR_TMR - S0I Ready Residency Timer (S0IR_TMR)—Offset 80h

This timer accumulates time spent in S0I Ready state

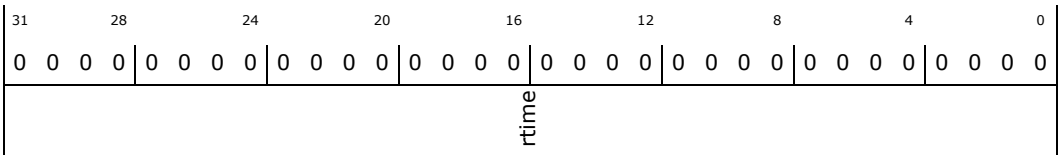
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0IR_TMR: [PMC_BASE_ADDRESS] + 80h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0I Ready state, in units of 32 uS

3.55.25 S0I1_TMR - S0I1 Residency Timer (S0I1_TMR)—Offset 84h

This timer accumulates time spent in S0I1 state

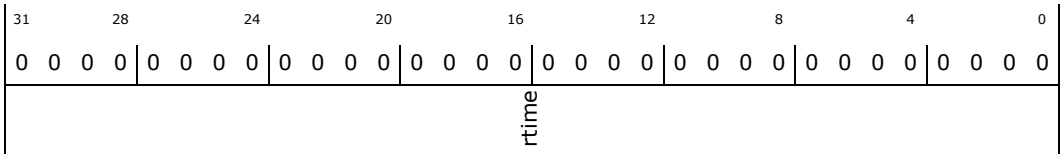
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0I1_TMR: [PMC_BASE_ADDRESS] + 84h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0I1 state, in units of 32 uS

3.55.26 S0I2_TMR - S0I2 Residency Timer (S0I2_TMR)—Offset 88h

This timer accumulates time spent in S0I2 state

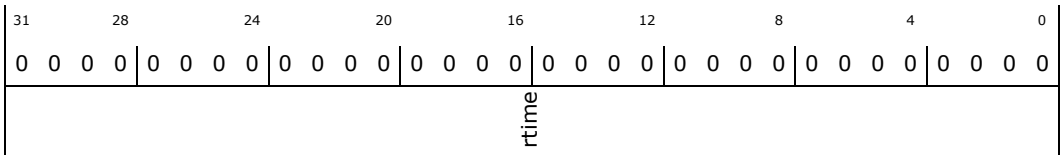
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0I2_TMR: [PMC_BASE_ADDRESS] + 88h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0I2 state, in units of 32 uS

3.55.27 S0I3_TMR - S0I3 Residency Timer (S0I3_TMR)—Offset 8Ch

This timer accumulates time spent in S0I3 state

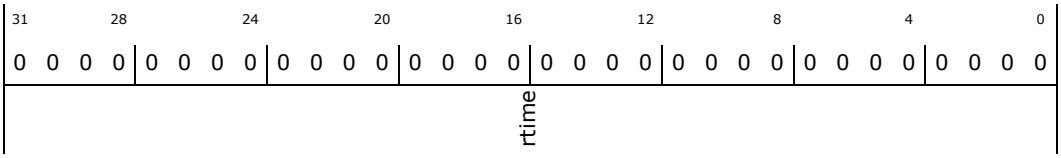
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0I3_TMR: [PMC_BASE_ADDRESS] + 8Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0I3 state, in units of 32 uS

3.55.28 S0_TMR - S0 Residency Timer (S0_TMR)—Offset 90h

This timer accumulates time spent in S0 state

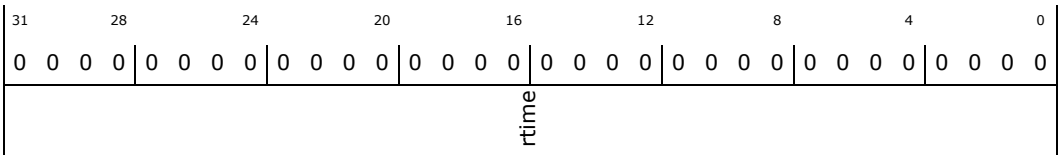
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0_TMR: [PMC_BASE_ADDRESS] + 90h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0 state, in units of 32 uS

3.55.29 PSS - Power island Power Status (PSS)—Offset 98h

This register reflects the power status for each physical power island controlled by PMC. note it does not reflect the tap override values

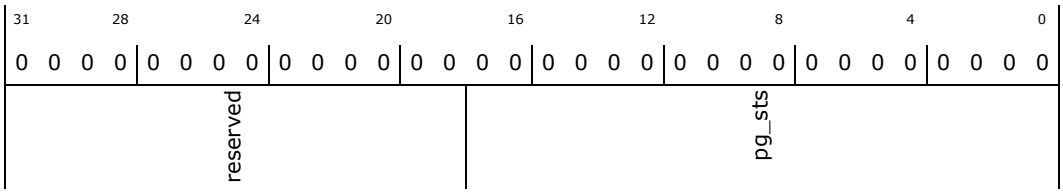
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PSS: [PMC_BASE_ADDRESS] + 98h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:18	0b RO	**reserved:** Reserved.
17:0	0b RO	**PG_STS (POWER GATE status) (pg_sts):** reflects the power gate status of all power islands 0 - power island is powered on. 1 - power island is powered off bits mapping: 0 - GBE 1 - SATA 2 - HDA 3 - SEC 4 - PCIE 5 - LPSS 6 - LPE 7 - DFX 8 - USH control 9 - USH SUS 10 - USH VCCS 11 - USH VCCA 12 - OTG control 13 - OTG VCCS 14 - OTG VCCACLK 15 - OTG VCCA 16 - USB 17 - USB SUS

3.55.30 D3_STS_0 - D3 Status register 0 (D3_STS_0)—Offset A0h

This register reflects D3 status of functions

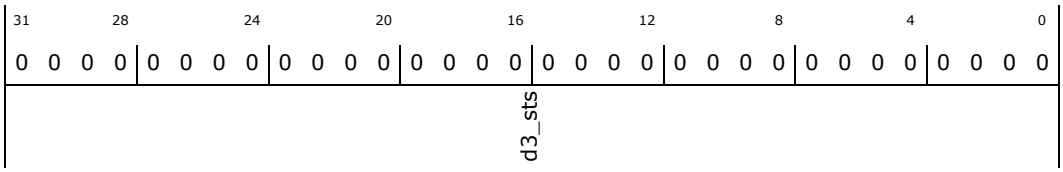
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STS_0: [PMC_BASE_ADDRESS] + A0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - LPSS 0 function 0 1 - LPSS 0 function 1 2 - LPSS 0 function 2 3 - LPSS 0 function 3 4 - LPSS 0 function 4 5 - LPSS 0 function 5 6 - LPSS 0 function 6 7 - LPSS 0 function 7 8 - SCC function 0 9 - SCC function 1 10 - SCC function 2 11 - MIPI 12 - HDA 13 - LPE 14 - OTG 15 - USH 16 - GBE 17 - SATA 18 - USB 19 - SEC 20 - PCIE function 0 21 - PCIE function 1 22 - PCIE function 2 23 - PCIE function 3 24 - LPSS 1 function 0 25 - LPSS 1 function 1 26 - LPSS 1 function 2 27 - LPSS 1 function 3 28 - LPSS 1 function 4 29 - LPSS 1 function 5 30 - LPSS 1 function 6 31 - LPSS 1 function 7

3.55.31 D3_STS_1 - D3 Status register 1 (D3_STS_1)—Offset A4h

This register reflects D3 status of functions

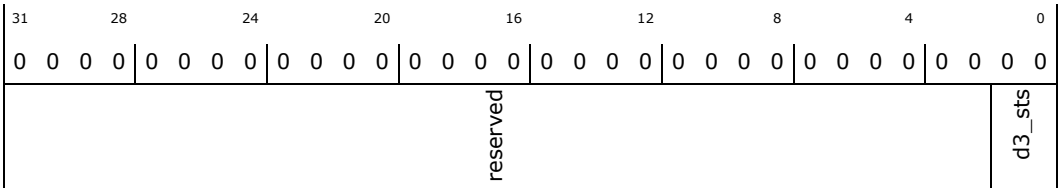
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STS_1: [PMC_BASE_ADDRESS] + A4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**reserved:** Reserved.
1:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - SMB 1 - USH Super speed PHY 2 - OTG Super speed PHY 3 - DFX

3.55.32 D3_STDBY_STS_0 - D3 Standby Status register 0 (D3_STDBY_STS_0)—Offset A8h

This register reflects D3 status of functions at the moment standby ready message received

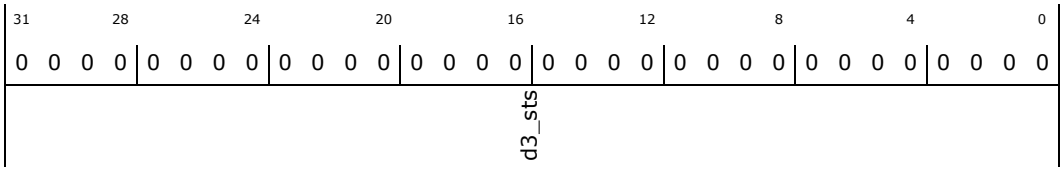
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STDBY_STS_0: [PMC_BASE_ADDRESS] + A8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - LPSS 0 function 0 1 - LPSS 0 function 1 2 - LPSS 0 function 2 3 - LPSS 0 function 3 4 - LPSS 0 function 4 5 - LPSS 0 function 5 6 - LPSS 0 function 6 7 - LPSS 0 function 7 8 - SCC function 0 9 - SCC function 1 10 - SCC function 2 11 - MIPI 12 - HDA 13 - LPE 14 - OTG 15 - USH 16 - GBE 17 - SATA 18 - HDA 19 - SEC 20 - PCIE function 0 21 - PCIE function 1 22 - PCIE function 2 23 - PCIE function 3 24 - LPSS 1 function 0 25 - LPSS 1 function 1 26 - LPSS 1 function 2 27 - LPSS 1 function 3 28 - LPSS 1 function 4 29 - LPSS 1 function 5 30 - LPSS 1 function 6 31 - LPSS 1 function 7

3.55.33 D3_STDBY_STS_1 - D3 Standby Status register 1 (D3_STDBY_STS_1)—Offset ACh

This register reflects D3 status of functions at the moment Standby Ready Message was received

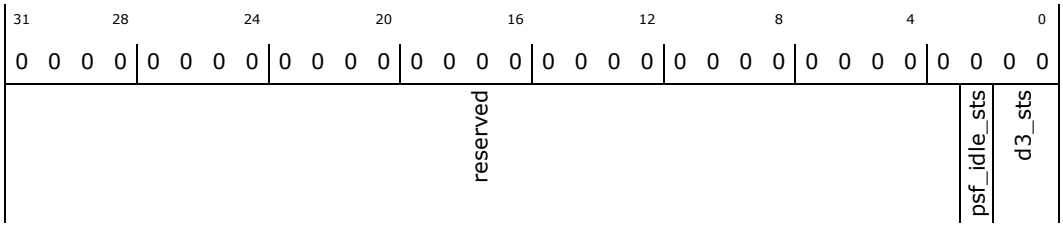
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STDBY_STS_1: [PMC_BASE_ADDRESS] + ACh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved:** Reserved.
2	0b RO	**PSF IDLE (status) (psf_idle_sts):** Reflect if S0IX flow was stopped because PSF isn't IDLE
1:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - SMB 1 - USH Super speed PHY 2 - OTG Super speed PHY 3 - DFX

3.55.34 MTPMC_1 - Message to PMC 1 (MTPMC_1)—Offset B0h

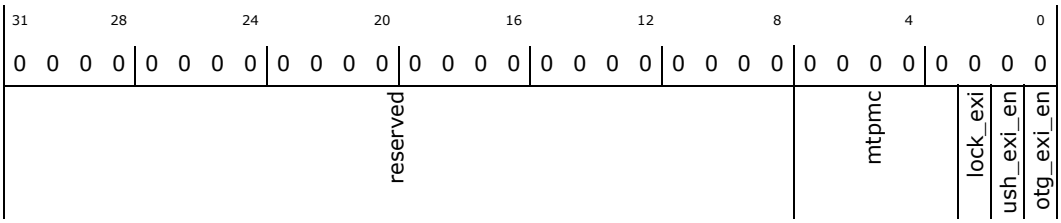
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MTPMC_1: [PMC_BASE_ADDRESS] + B0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:3	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS
2	0b RW	**LOCK EXI (lock_exi):** This field locks the ush_exi_en and otg_exi_en fields. The lock is soft lock, meaning register value will be changed but FW will keep the value on internal register GP1[2] until warm reset
1	0b RW	**USH_EXI_Enable (ush_exi_en):** A write to this field causes an interrupt to the PMC. The PMC FW will read the contents of this register and will set pcu_ush_exi_enable_xttnfwh signal. This will prevent USH PIMA power down upon S0IX entry. The host must wait until the PMC has taken action, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS. This field will be copied to FW internal register and it will hold the value until global reset.

Bit Range	Default & Access	Description
0	0b RW	**OTG_EXI_Enable (otg_exi_en):** A write to this field causes an interrupt to the PMC. The PMC FW will read the contents of this register and will set pcu_otg_exi_enable_xttnfwh signal. This will prevent OTG PIMA power down upon S0IX entry. The host must wait until the PMC has taken action, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS. This field will be copied to FW internal register and it will hold the value until global reset

3.55.35 MTPMC_2 - Message to PMC 2 (MTPMC_2)—Offset B4h

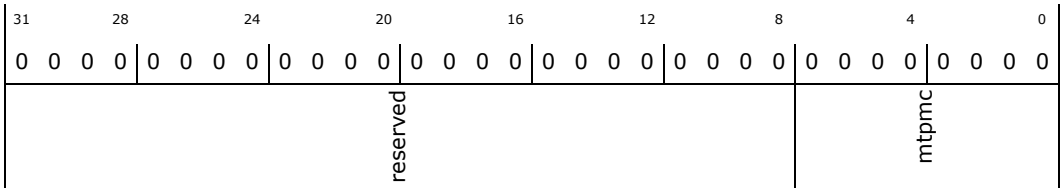
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MTPMC_2: [PMC_BASE_ADDRESS] + B4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_2_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

3.55.36 MTPMC_3 - Message to PMC 3 (MTPMC_3)—Offset B8h

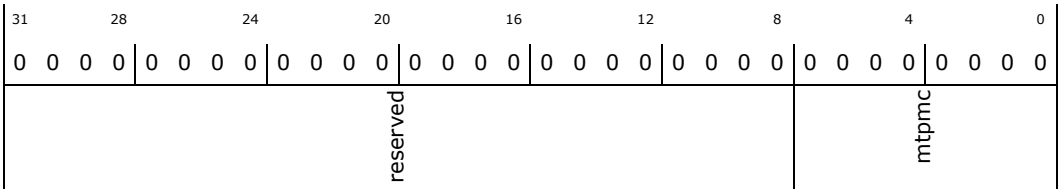
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MTPMC_3: [PMC_BASE_ADDRESS] + B8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_3_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

3.55.37 MTPMC_4 - Message to PMC 4 (MTPMC_4)—Offset BCh

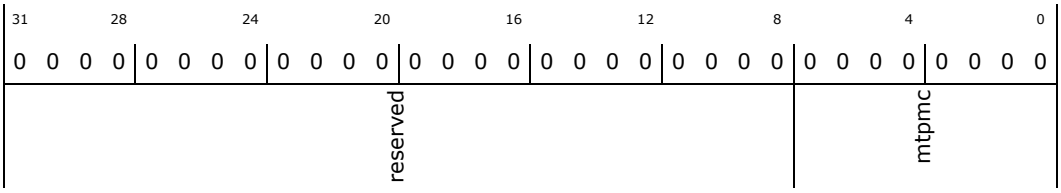
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MTPMC_4: [PMC_BASE_ADDRESS] + BCh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_4_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

3.55.38 PME Status 0 - Status bit for PME messages (PME_STS)—Offset C0h

Access Method

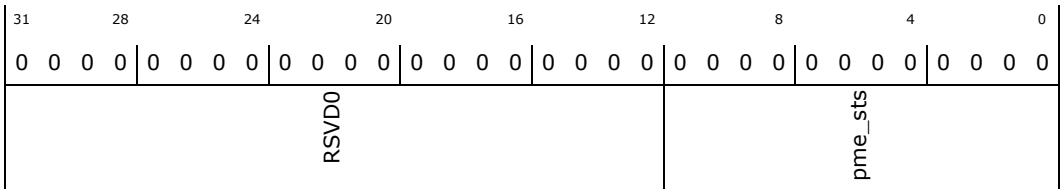
Type: Memory Mapped I/O Register (Size: 32 bits)

PME_STS: [PMC_BASE_ADDRESS] + C0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11:0	0b RO	**PME Status (pme_sts):** when set PME was received from the following agents 0 = GBE 1 = HDA 2 = SATA 3 = SCCSDIO 4 = SCCSDCARD 5 = LPSDIO1; 6 = SECEP 7 = LPE 8 = LPSDIO2 9 = OTG 10 = SCCEMMC 11 = SCCMIPIHSI

3.55.39 GPE Level Edge mode (GPE_LEVEL_EDGE)—Offset C4h

Access Method

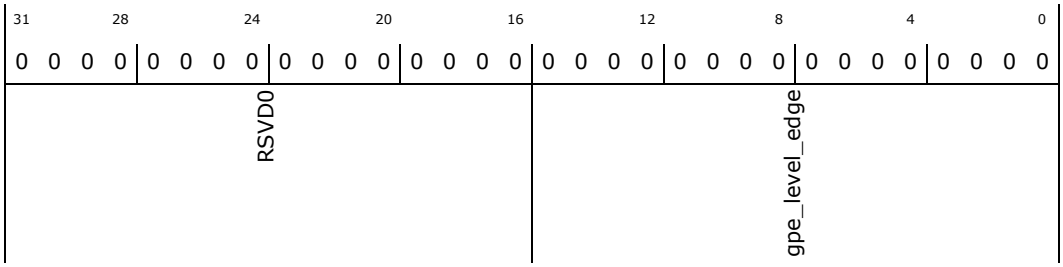
Type: Memory Mapped I/O Register (Size: 32 bits)

GPE_LEVEL_EDGE: [PMC_BASE_ADDRESS] + C4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0b RW	**Edge Level mode (gpe_level_edge):** When set GPE is in level mode when clear GPE is in edge mode gpe_level_edge[15:8] used for GPIO Core gpe_level_edge[7:0] used for GPIO SUS

3.55.40 GPE polarity mode (GPE_POLARITY)—Offset C8h

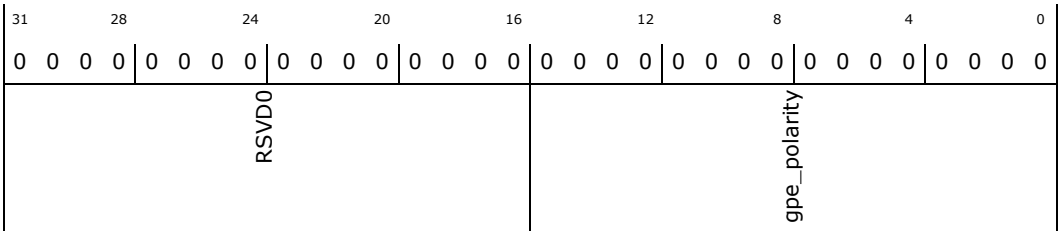
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPE_POLARITY: [PMC_BASE_ADDRESS] + C8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0b RW	**Polarity (gpe_polarity):** When set GPE is active high when clear GPE is active low gpe_polarity[15:8] used for GPIO Core gpe_polarity[7:0] used for GPIO SUS

3.55.41 Lock Register (LOCK)—Offset CCh

Register Field Lock bit ---------- GEN_PMCON1 PME_B0_S5_DIS LOCK.Sx_WAKE GEN_PMCON1 WOL_EN_OVRD LOCK.Sx_WAKE GEN_PMCON1 AG3E LOCK.Sx_WAKE GEN_PMCON2 BIOS_PCI_EXP_EN LOCK.PCIE GEN_PMCON2 PER_SMI_SEL LOCK.PER_SMI FUNC_DIS all LOCK.FUNC_DIS FUNC_DIS_2 all LOCK.FUNC_DIS S0IX_WAKE_EN all LOCK.SOIX S0IX_CTL S0IX_RAIL_RAMP LOCK.SOIX ETR IGNORE_HPET LOCK.SOIX ETR MAX_S0IX LOCK.SOIX GPIO_ROUT all LOCK.GPIO_ROUT PLT_CLK_CTL_0 all LOCK.PLT_CLK PLT_CLK_CTL_1 all LOCK.PLT_CLK PLT_CLK_CTL_2 all LOCK.PLT_CLK PLT_CLK_CTL_3 all LOCK.PLT_CLK PLT_CLK_CTL_4 all LOCK.PLT_CLK PLT_CLK_CTL_5 all LOCK.PLT_CLK

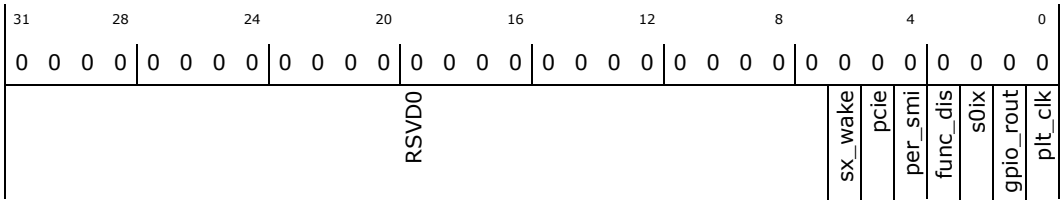
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LOCK: [PMC_BASE_ADDRESS] + CCh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0b RO	**RSVD0:** Reserved
6	0b RW	**SX_WAKE lock (sx_wake):** Reserved.
5	0b RW	**PCIE lock (pcie):** Reserved.
4	0b RW	**PER_SMI lock (per_smi):** Reserved.
3	0b RW	**FUNC_DIS (func_dis):** Reserved.
2	0b RW	**S0IX lock (s0ix):** Reserved.
1	0b RW	**GPIO_ROUT lock (gpio_rout):** Reserved.
0	0b RW	**PLT_CLK lock (plt_clk):** Reserved.

3.55.42 Virtual UART register (VUART1)—Offset D0h

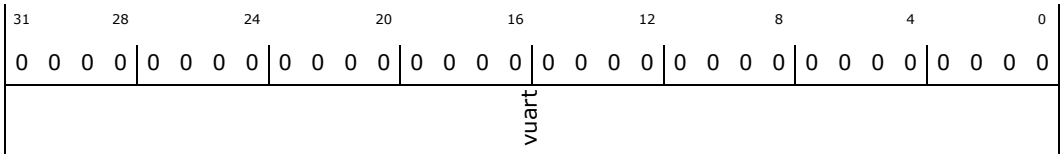
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VUART1: [PMC_BASE_ADDRESS] + D0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

3.55.43 Virtual UART register (VUART2)—Offset D4h

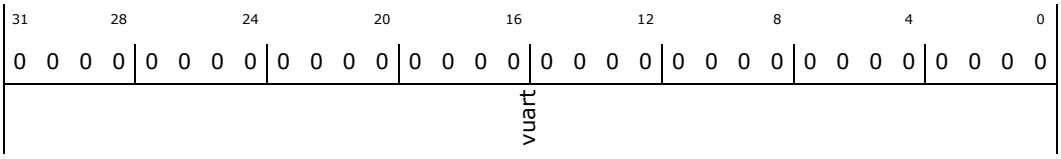
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VUART2: [PMC_BASE_ADDRESS] + D4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

3.55.44 Virtual UART register (VUART3)—Offset D8h

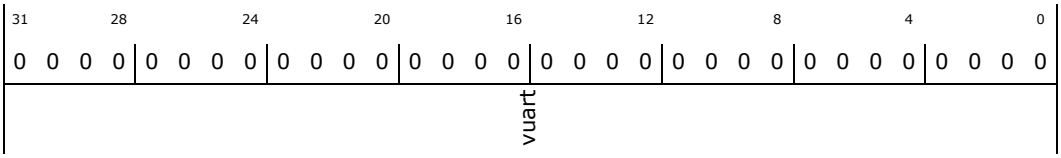
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VUART3: [PMC_BASE_ADDRESS] + D8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

3.55.45 Virtual UART register (VUART4)—Offset DCh

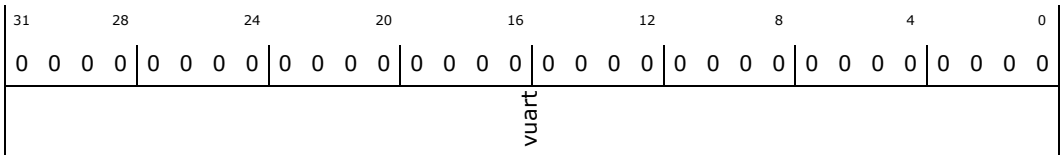
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VUART4: [PMC_BASE_ADDRESS] + DCh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

3.56 PCU PMC IO Registers

Table 64. Summary of PCI iLB PMC I/O Registers

Offset	Size	Register ID—Description	Default Value
92h	1	"PORT92: Init Register (PORT92)—Offset 92h" on page 3079	00h
B2h	1	"APM Register (APM)—Offset B2h" on page 3079	00h
B3h	1	"APM_STS Register (APM_STS)—Offset B3h" on page 3080	00h
CF9h	1	"RST_CNT: Reset Control Register (RST_CNT)—Offset CF9h" on page 3080	00h

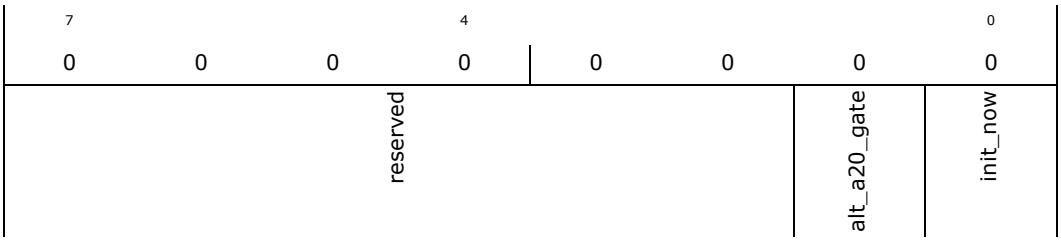
3.56.1 PORT92: Init Register (PORT92)—Offset 92h

Access Method

Type: I/O Register
(Size: 8 bits)

PORT92: 92h

Default: 00h



Bit Range	Default & Access	Description
7:2	0b RO	**reserved:** Reserved.
1	0b RW	**ALT_A20_GATE - Alternate A20 Gate (alt_a20_gate):** Legacy bit - kept just in case DOS expects it to be read/write
0	0b RW	**INIT_NOW (init_now):** When this bit transitions from a 0 to a 1, PMC will sent an INIT# VLW to T-Unit

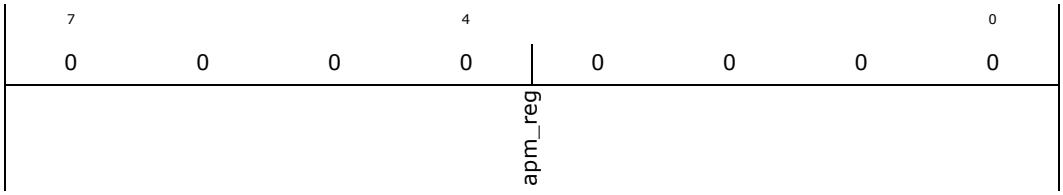
3.56.2 APM Register (APM)—Offset B2h

Access Method

Type: I/O Register
(Size: 8 bits)

APM: B2h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**APM_Register (apm_reg):** TBD

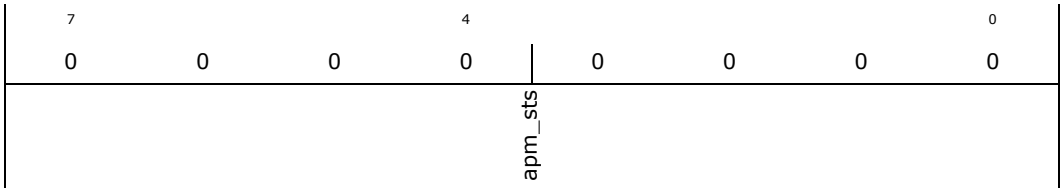
3.56.3 APM_STS Register (APM_STS)—Offset B3h

Access Method

Type: I/O Register
(Size: 8 bits)

APM_STS: B3h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**APM_STS (apm_sts):** Advanced Power Management Status Port. used to pass data between the OS and the SMI handler. Basically, this is scratchpad register and is not effected by any other register or function (other than a PCI reset)

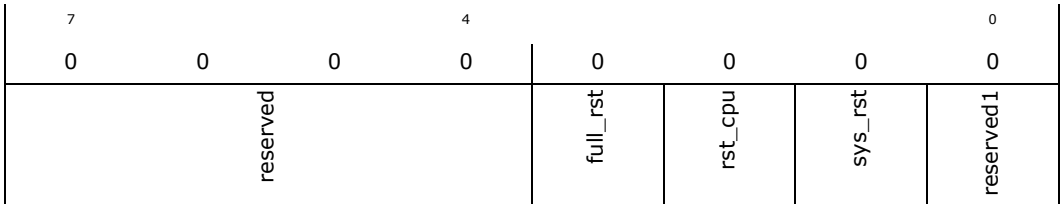
3.56.4 RST_CNT: Reset Control Register (RST_CNT)—Offset CF9h

Access Method

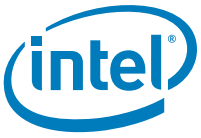
Type: I/O Register
(Size: 8 bits)

RST_CNT: CF9h

Default: 00h



Bit Range	Default & Access	Description
7:4	0b RO	**reserved:** Reserved.
3	0b RW	**Full Reset (FULL_RST) (full_rst):** When this bit is set to 1 and bit 1 is set to 1 (indicating Hard Reset, not Soft Reset), and the RST_CPU bit (bit 2) is written from 0 to 1, the PMC will do a full reset, including driving PMU_SLP_S3_B and PMU_SLP_S4_B active (low) for at least 3 (and no more than 5) seconds. When this bit is set, it also causes the full power cycle (PMU_SLP_S3/4_B assertion) in response to PMU_RESETBUTTON_B, COREPWROK, and Watchdog timer reset sources.
2	0b RW	**Reset CPU (RST_CPU) (rst_cpu):** This bit will cause either a hard or soft reset to the CPU depending on the state of the SYS_RST bit (bit 1 in this same register). The software will cause the reset by setting bit 2 from a 0 to a 1.
1	0b RW	**System Reset (SYS_RST) (sys_rst):** This bit determines the type of reset caused via RST_CPU (bit 2 of this register). If SYS_RST is 0 when RST_CPU goes from 0 to 1, then the PMC will force INIT# active for 16 PCI clocks. If SYS_RST is 1 when RST_CPU goes from 0 to 1, then the PMC will force PCI reset active for about 1 ms, however the PMU_SLP_S3_B and PMU_SLP_S4_B signals assertion is dependent on the value of the FULL_RST (bit3 of this register).
0	0b RO	**reserved1:** Reserved.



3.57 PCU iLB PMC I/O Registers

Table 65. Summary of PCU iLB PMC I/O Registers—ACPI_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"PM1_STS_EN - Power Management 1 Status and enable (PM1_STS_EN)—Offset 0h" on page 3082	00000000h
4h	4	"PM1_CNT - Power Management 1 Control (PM1_CNT)—Offset 4h" on page 3085	00000000h
8h	4	"PM1_TMR - Power Management 1 Timer (PM1_TMR)—Offset 8h" on page 3086	00000000h
20h	4	"GPE0a_STS - General Purpose Event 0 Status (GPE0a_STS)—Offset 20h" on page 3087	00000000h
28h	4	"GPE0a_EN - General Purpose Event 0 Enables (GPE0a_EN)—Offset 28h" on page 3090	00000000h
30h	4	"SMI_EN - SMI Control and Enable (SMI_EN)—Offset 30h" on page 3091	00000002h
34h	4	"SMI_STS - SMI Status Register (SMI_STS)—Offset 34h" on page 3093	00000000h
38h	4	"ALT_GPIO_SMI - Alternate GPIO SMI Status and Enable Register. (ALT_GPIO_SMI)—Offset 38h" on page 3095	00000000h
3Ch	4	"UPRWC - USB Per-Port Registers Write Control (UPRWC)—Offset 3Ch" on page 3096	00000000h
40h	4	"GPE_CTRL - General Purpose Event Control (GPE_CTRL)—Offset 40h" on page 3097	00000000h
50h	4	"PM2A_CNT_BLK - PM2a Control Block (PM2A_CNT_BLK)—Offset 50h" on page 3098	00000000h
60h	4	"TCO_RLD: TCO Reload Register (TCO_RLD)—Offset 60h" on page 3098	00000000h
64h	4	"TCO_STS: TCO Timer Status (TCO_STS)—Offset 64h" on page 3099	00000000h
68h	4	"TCO1_CNT: TCO Timer Control (TCO1_CNT)—Offset 68h" on page 3100	00000000h
70h	4	"TCO_TMR: TCO Timer Register (TCO_TMR)—Offset 70h" on page 3101	00040000h

3.57.1 PM1_STS_EN - Power Management 1 Status and enable (PM1_STS_EN)—Offset 0h

Access Method

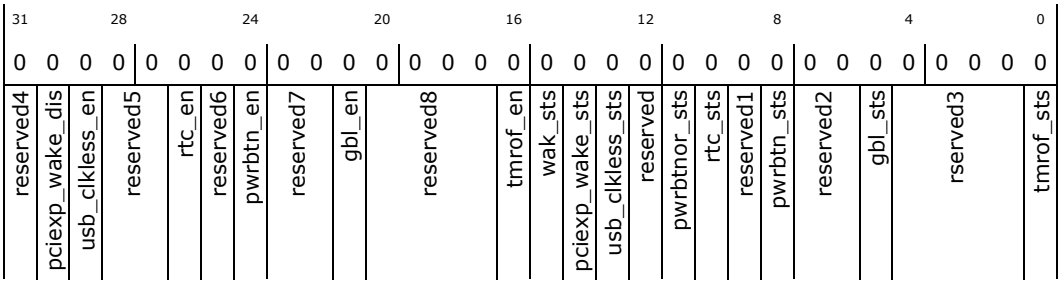
Type: I/O Register (Size: 32 bits)

PM1_STS_EN: [ACPI_BASE_ADDRESS] + 0h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**reserved4:** Reserved.
30	0b RW	**PCI Express Wake Disable (PCIEXP_WAKE_DIS) (pciexp_wake_dis):** This bit disables the inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register from waking the system. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit. reset_type=Resume Well Reset#
29	0b RW	**USB clockless Wake Enable (USB_CLKLESS_EN) (usb_clkless_en):** This bit enables the inputs to the USB_CLKLESS_STS bit in the PM1 Status register to wake the system. Modification of this bit has no impact on the value of the USB_CLKLESS_STS bit. reset_type=Resume Well Reset#
28:27	0b RO	**reserved5:** Reserved.
26	0b RW	**RTC Alarm Enable (RTC_EN) (rtc_en):** This is the RTC alarm enable bit. It works in conjunction with the SCI_EN bit: RTC_EN SCI_EN Effect when RTC_STS is set 0 x No SMI# or SCI. If system was in S1-S5, no wake even occurs. 1 0 SMI#. If system was in S1-S5, then a wake event occurs before the SMI#. 1 1 SCI. If system was in S1-S5, then a wake event occurs before the SCI. Note: This bit needs to be backed by the RTC well to allow an RTC event to wake after a power failure. In addition to being reset by SRTCRST_B assertion, PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
25	0b RO	**reserved6:** Reserved.
24	0b RW	**Power Button Enable (PWRBTN_EN) (pwrbtn_en):** This bit is the power button enable. It works in conjunction with the SCI_EN bit: PWRBTN_EN SCI_EN Effect when PWRBTN_STS is set 0 x No SMI# or SCI. 1 0 SMI#. 1 1 SCI. NOTE: PWRBTN_EN has no effect on the PWRBTN_STS bit being set by the assertion of the power button. The Power Button is always enabled as a Wake event. reset_type=Resume Well Reset#
23:22	0b RO	**reserved7:** Reserved.
21	0b RW	**Global Enable (GBL_EN) (gbl_en):** The global enable bit. When both the GBL_EN and the GBL_STS are set, PMC generates an SCI. reset_type=PMU_PLTRST_B
20:17	0b RO	**reserved8:** Reserved.

Bit Range	Default & Access	Description
16	0b RW	**Timer Overflow Interrupt Enable (TMROF_EN) (tmrof_en):** This is the timer overflow interrupt enable bit. It works in conjunction with the SCI_EN bit: TMROF_EN SCI_EN Effect when TMROF_STS is set 0 x No SMI# or SCI. . 1 0 SMI#. 1 1 SCI. reset_type=PMU_PLTRST_B
15	0b RW	**Wake Status (WAK_STS) (wak_sts):** This bit is set when the system is in one of the Sleep states (via the SLP_EN bit) and an enabled Wake event occurs. Upon setting this bit, the PMC will transition the system to the ON state. This bit can only be set by hardware and can only be cleared by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. If a power failure occurs (such as removed batteries) without the SLP_EN bit set, the WAK_STS bit will not be set when the power returns if the AFTER_G3 bit is 0. If the AFTER_G3 bit is 1, then the WAK_STS bit will be set after waking from a power failure. If necessary, the BIOS can clear the WAK_STS bit in this case This is based on discussions with Microsoft. That behavior is not in the ACPI spec. reset_type=RSMRST_B
14	0b RW	**PCI Express Wake Status (PCIEXP_WAKE_STS) (pciexp_wake_sts):** This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This event can be caused by the PCI Express WAKE# pins (PMU_WAKE_B, PCI_WAKE1_B, PCI_WAKE2_B, PCI_WAKE3_B) being active, or one or more of the PCI Express ports being in beacon state, or receipt of a PCI Express PME message at root port. This bit should only be set when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independent of the PCIEXP_WAKE_DIS bit. Software writes a 1 to clear this bit. If one of the WAKE# pins is still active during the write or one or more PCI Express ports is in the beacon state or PME message received indication is not cleared in the root port, then the bit will remain Power Management active (i.e. all inputs to this bit are level sensitive) Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake. reset_type=pmc_global_rst_b
13	0b RW	**USB clockless Wake Status (USB_CLKLESS_STS) (usb_clkless_sts):** This bit is set by hardware to indicate that the system woke due to change in USB serial lines. This bit is set independent of the USB_CLKLESS_EN bit. Software writes a 1 to clear this bit. reset_type=pmc_global_rst_b
12	0b RO	**reserved:** Reserved.
11	0b RW	**Power Button Override (PWRBTNOR_STS) (pwrbtnor_sts):** This bit is set any time a Power Button Override Event occurs (i.e. the power button is pressed for at least 4 consecutive seconds), or due to an internal thermal sensor catastrophic condition. These events cause an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST_B. Thus, this bit is preserved through power failures. Note that this bit is still asserted when the global SCI_EN is set to '1' then an SCI will be generated. reset_type=SRTCRST_B

Bit Range	Default & Access	Description
10	0b RW	**RTC Status (RTC_STS) (rtc_sts):** This bit is set when the RTC generates an alarm (assertion of the IRQ8# signal), and is not affected by any other enable bit. See RTC_EN for the effect when RTC_STS goes active. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. reset_type=RSMRST_B
9	0b RO	**reserved1:** Reserved.
8	0b RW	**Power Button Status (PWRBTN_STS) (pwrbtn_sts):** This bit is set when the PMU_PWRBTN_B signal is asserted (low), independent of any other enable bit. See PWRBTN_EN for the effect when PWRBTN_STS goes active. PWRBTN_STS is always a wake event. This bit is only set by hardware and can be cleared by software writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. If the PMU_PWRBTN_B signal is held low for more than 4 seconds, the PMC clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, the system transitions to the S5 state, and only PMU_PWRBTN_B is enabled as a wake event. If PWRBTN_STS bit is cleared by software while the PMU_PWRBTN_B pin is still held low, this will not cause the PWRBTN_STS bit to be set. The PMU_PWRBTN_B signal must go inactive and active again to set the PWRBTN_STS bit. Note that the CPU Thermal Trip and the Internal Thermal Sensors' Catastrophic Condition result in behavior matching the Powerbutton Override, which includes clearing this bit. reset_type=RSMRST_B
7:6	0b RO	**reserved2:** Reserved.
5	0b RW	**GBL Status (GBL_STS) (gbl_sts):** This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit. The SCI handler should then clear this bit by writing a 1 to it. This bit will not cause wake events or SMI#. This bit is not effected by SCI_EN. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. reset_type=PMU_PLTRST_B
4:1	0b RO	**reserved3 (rserved3):** reserved
0	0b RW	**Timer Overflow Status (TMROF_STS) (tmrof_sts):** This is the timer overflow status bit. This bit gets set anytime bit 22 of the 24 bit timer goes low (bits are counted from 0 to 23). This will occur every 2.3435 seconds. See TMROF_EN for the effect when TMROF_STS goes active. Software clears this bit by writing a 1 to it. reset_type=PMU_PLTRST_B

3.57.2 PM1_CNT - Power Management 1 Control (PM1_CNT)—Offset 4h

Access Method

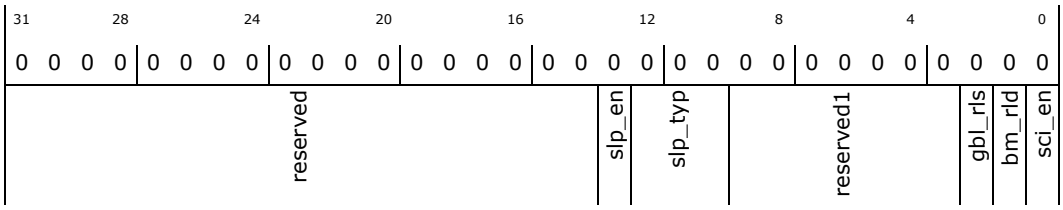
Type: I/O Register (Size: 32 bits)

PM1_CNT: [ACPI_BASE_ADDRESS] + 4h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0b RO	**reserved:** Reserved.
13	0b WO	**Sleep Enable (SLP_EN) (slp_en):** This is a write-only bit and reads to it always return a zero. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.
12:10	0b RW	**Sleep Type (SLP_TYP) (slp_typ):** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. These bits are reset by SRTCRST_B only. Bits Mode Typical Mapping 000 ON S0 001 Puts CPU in S1 state. S1 010 Reserved 011 Reserved 100 Reserved 101 Suspend-To-RAM S3 110 Suspend-To-Disk S4 111 Soft Off S5
9:3	0b RO	**reserved1:** Reserved.
2	0b RW	**GBL_RLS (GBL_RLS) (gbl_rls):** This bit is used by the ACPI software to raise an event to the BIOS software. BIOS software has a corresponding enable and status bits to control its ability to receive ACPI events. This bit always reads as 0.
1	0b RW	**BM_RLD (BM_RLD) (bm_rld):** This bit is treated as a scratchpad bit
0	0b RW	**SCI Enable (SCI_EN) (sci_en):** SCI Enable (SCI_EN): Selects the SCI interrupt or the SMI# for various events. When this bit is 1, then the events will generate an SCI interrupt. When this bit is 0, these events will generate an SMI#.

3.57.3 PM1_TMR - Power Management 1 Timer (PM1_TMR)—Offset 8h

Access Method

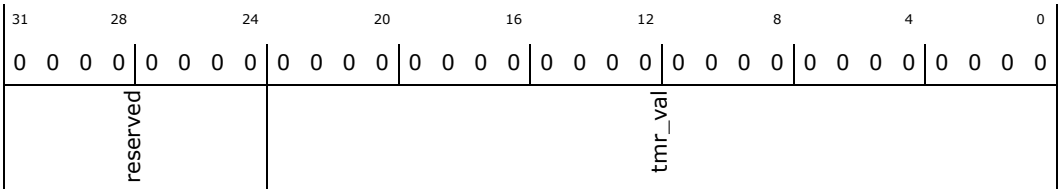
Type: I/O Register (Size: 32 bits)

PM1_TMR: [ACPI_BASE_ADDRESS] + 8h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**reserved:** Reserved.
23:0	0b RO	**Timer Value (TMR_VAL) (tmr_val):** This read-only field returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (derived from 14.31818 MHz divided by 4). It is reset (to 0) during a Platform reset, and then continues counting as long as the system is in the S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit is set. The High-to-Low transition will occur every 2.3435 seconds. Writes to this register have no effect.

3.57.4 GPE0a_STS - General Purpose Event 0 Status (GPE0a_STS)—Offset 20h

Note: This register is symmetrical to the General Purpose Event 0a Enable Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the STS bit get set, the PMC will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the PMC will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set. CLARIFICATION: Bits 15:0 should not be reset by CF9 write. Bits 31:16 are reset by CF9h full resets. reset_type=RSMRST_B

Access Method

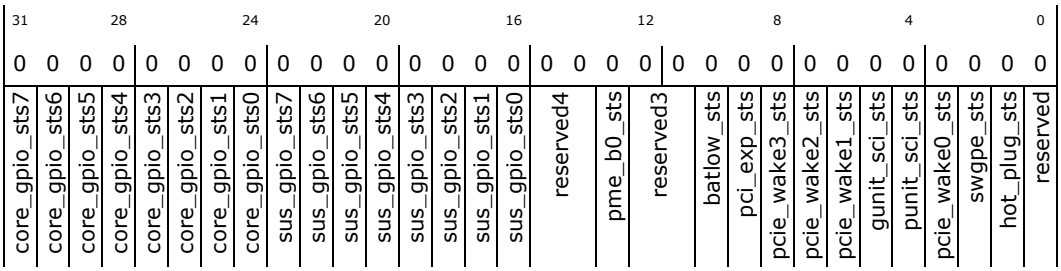
Type: I/O Register (Size: 32 bits)

GPE0a_STS: [ACPI_BASE_ADDRESS] + 20h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts7):** These bits are set any time the corresponding Core GPIO is set up as an input and the corresponding GPIO signal is asserted. Core GPIO pins are: SATA_GP0 (GPIO core 0) SATA_GP1 (GPIO core 1) SATA_LEDN (GPIO core 2) PCIE_CLKREQ0B (GPIO core 3) PCIE_CLKREQ1B (GPIO core 4) PCIE_CLKREQ2B (GPIO core 5) PCIE_CLKREQ3B (GPIO core 6) PCIE_CLKREQ4B (GPIO core 7) If the corresponding enable bit is set in the GPE0a_EN register, then when the CORE_GPIO_STS[n] bit is set, an SCI will be caused, depending on the GPIO_ROUT bits for the corresponding GPIO. These bits are sticky bits and are cleared by writing a 1 back to this bit position. reset_type=Resume Well Reset#
30	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts6):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
29	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts5):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
28	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts4):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
27	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts3):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
26	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts2):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
25	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts1):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
24	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts0):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
23	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts7):** These bits are set any time the corresponding Sus GPIO is set up as an input and the corresponding GPIO signal is asserted. Sus GPIO pins are GPIO_SUS0-7. If the corresponding enable bit is set in the GPE0a_EN register, then when the SUS_GPIO_STS[n] bit is set: * If the system is in an S3-S5 state, the event will also wake the system. * If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIO_ROUT bits for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. reset_type=Resume Well Reset#
22	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts6):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
21	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts5):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
20	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts4):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
19	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts3):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
18	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts2):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
17	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts1):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)

Bit Range	Default & Access	Description
16	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts0):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
15:14	0b RO	**reserved (reserved4):** Reserved.
13	0b RW	**Power Management Event Bus 0 Status (PME_B0_STS) (pme_b0_sts):** This bit will be set to 1 by the PMC when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). This bit is cleared by a software write of '1'. Internal devices which can set this bit: - Integrated LAN - HD Audio - SATA - USB
12:11	0b RO	**reserved (reserved3):** Reserved.
10	0b RW	**Battery Low Status (BATLOW_STS) (batlow_sts):** This bit will be set to 1 by hardware when the PMU_BATLOW_B signal goes low. Software clears the bit by writing a 1 to the bit position. In Desktop Mode, this bit will be treated as Reserved.
9	0b RW	**PCI Express Status (PCI_EXP_STS) (pci_exp_sts):** This bit will be set to 1 by hardware to indicate that: - The PME event message was received on one or more of the PCI-Express Ports Note: The PCI PMU_WAKE_B pin and the PCI-Express Beacons have no impact on this bit. Software attempts to clear this bit by writing a 1 to this bit position. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the leveltriggered SCI will remain active. Note that a race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds.
8	0b RW	**PCI Express Wake3 Status (PCIE_WAKE3_STS) (pcie_wake3_sts):** This bit is set by hardware to indicate that the PCI_WAKE3_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE3_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
7	0b RW	**PCI Express Wake2 Status (PCIE_WAKE2_STS) (pcie_wake2_sts):** This bit is set by hardware to indicate that the PCI_WAKE2_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE2_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
6	0b RW	**PCI Express Wake1 Status (PCIE_WAKE1_STS) (pcie_wake1_sts):** This bit is set by hardware to indicate that the PCI_WAKE1_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE1_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
5	0b RW	**GUNIT SCI status (GUNIT_SCI_STS) (gunit_sci_sts):** This bit will be set if the Graphics Unit requests SCI
4	0b RW	**PUNIT SCI status (PUNIT_SCI_STS) (punit_sci_sts):** This bit will be set if the Power Management Unit requests SCI

Bit Range	Default & Access	Description
3	0b RW	**PCI Express Wake0 Status (PCIE_WAKE0_STS) (pcie_wake0_sts):** This bit is set by hardware to indicate that the PMU_WAKE_B pin was asserted. Software writes a 1 to clear this bit. If PMU_WAKE_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
2	0b RW	**Software GPE Status (SWGPE_STS) (swgpe_sts):** The SWGPE_CTRL bit (bit 1 of GPE_CTRL reg) acts as a level input to this bit.
1	0b RO	**Hot Plug Status (HOT_PLUG_STS) (hot_plug_sts):** This bit is set to 1 by hardware when a PCI-Express hot plug event occurs. This will cause an SCI if the HOT_PLUG_EN and SCI_EN bits are set. This bit is cleared by writing a 1 to this bit position. The following events cause this bit to set - Assert_GPE message received from any of the PCI_E ports in the SOC - Assert_HPGPE message received from any of the PCI_E ports in the SOC
0	0b RO	**reserved:** Reserved.

3.57.5 GPE0a_EN - General Purpose Event 0 Enables (GPE0a_EN)—Offset 28h

Note: This register is symmetrical to the General Purpose Event 0a Status Register. reset_type=Resume Well Reset#

Access Method

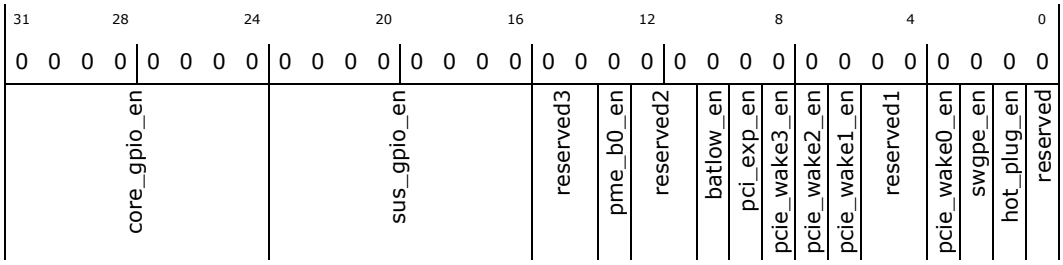
Type: I/O Register (Size: 32 bits)

GPE0a_EN: [ACPI_BASE_ADDRESS] + 28h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**CORE GPIO Enable (CORE_GPIO_EN) (core_gpio_en):** These bits enable the corresponding CORE_GPIO_STS[n] bits being set to cause an SCI and/or wake event.
23:16	0b RW	**SUS GPIO Enable (SUS_GPIO_EN) (sus_gpio_en):** These bits enable the corresponding SUS_GPIO_STS[n] bits being set to cause an SCI and/or wake event.

Bit Range	Default & Access	Description
15:14	0b RO	**reserved (reserved3):** Reserved.
13	0b RW	**PME_B0 Enable (PME_B0_EN) (pme_b0_en):** Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. In addition to being reset by SRTCRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
12:11	0b RO	**reserved (reserved2):** Reserved.
10	0b RW	**Low Battery Enable (BATLOW_EN) (batlow_en):** This bit enables the PMU_BATLOW_B signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low.This bit does not prevent the PMU_BATLOW_B signal from inhibiting the wake event. In Desktop Mode this bit will be treated as Reserved. In addition to being reset by SRTCRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
9	0b RW	**PCI Express Enable (PCI_EXP_EN) (pci_exp_en):** Enables the PMC to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express ports, to cause an SCI due to wake/PME events
8	0b RW	**PCI Express Wake3 Enable (PCIE_WAKE3_EN) (pcie_wake3_en):** This bit, when set to 1, enables the PCIE_WAKE3_STS to to cause an SCI
7	0b RW	**PCI Express Wake2 Enable (PCIE_WAKE2_EN) (pcie_wake2_en):** This bit, when set to 1, enables the PCIE_WAKE2_STS to to cause an SCI
6	0b RW	**PCI Express Wake1 Enable (PCIE_WAKE1_EN) (pcie_wake1_en):** This bit, when set to 1, enables the PCIE_WAKE1_STS to to cause an SCI
5:4	0b RO	**reserved (reserved1):** Reserved.
3	0b RW	**PCI Express Wake0 Enable (PCIE_WAKE0_EN) (pcie_wake0_en):** This bit, when set to 1, enables the PCIE_WAKE0_STS to to cause an SCI
2	0b RW	**Software GPE Enable (SWGPE_EN) (swgpe_en):** This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated
1	0b RW	**Hot Plug Enable (HOT_PLUG_EN) (hot_plug_en):** Enables the PMC to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events.
0	0b RO	**reserved:** Reserved.

3.57.6 SMI_EN - SMI Control and Enable (SMI_EN)—Offset 30h

Access Method

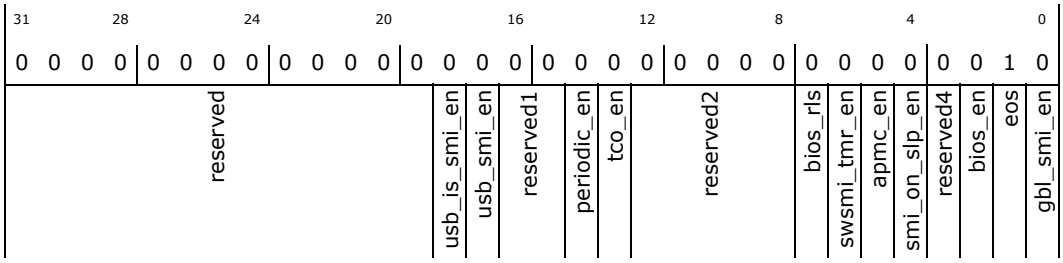
Type: I/O Register (Size: 32 bits)

SMI_EN: [ACPI_BASE_ADDRESS] + 30h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000002h



Bit Range	Default & Access	Description
31:19	0b RO	**reserved:** Reserved.
18	0b RW	**Intel USB 2 Enable (USB_IS_SMI_EN): (usb_is_smi_en):** Enables Intel-Specific USB2 SMI logic to cause SMI#.
17	0b RW	**USB SMI Enable (USB_SMI_EN): (usb_smi_en):** Enables SMI from USB
16:15	0b RO	**reserved1:** Reserved.
14	0b RW	**Periodic Enable (PERIODIC_EN) (periodic_en):** Setting this bit will cause the PMC to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register.
13	0b RW	**TCO Enable (TCO_EN): (tco_en):** when set Enables the TCO logic to generate SMI#. when cleared disables TCO logic generating an SMI#. NOTE: This bit can not be written once the TCO_LOCK bit is set. This prevents unauthorized software from disabling the generation of TCO-based SMI's
12:8	0b RO	**reserved2:** Reserved.
7	0b RW	**BIOS_RLS (BIOS_RLS): (bios_rls):** Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software. This bit always reads a zero. NOTE: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.
6	0b RW	**Software SMI Timer Enable (SWSMI_TMR_EN): (swsmi_tmr_en):** Software sets this bit to a 1 to start the Software SMI# Timer. When the timer expires (depending on the SWSMI_RATE_SEL bits), it will generate an SMI# and set the SWSMI_TMR_STS bit. The SWSMI_TMR_EN bit will remain at 1 until software sets it back to 0. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. The default for this bit is 0.
5	0b RW	**APMC_EN (apmc_en):** APMC Enable - If set, this enables writes to the APM register to cause an SMI#

Bit Range	Default & Access	Description
4	0b RW	**SMI On Sleep Enable (SMI_ON_SLP_EN): (smi_on_slp_en):** If this bit is set, the PMC will generate an SMI# when a write access attempts to set the SLP_EN bit (in the PM1_CNT register). Furthermore, the PMC will not put the system to a sleep state. This allows the SMI# handler work around chip-level bugs. It is expected that the SMI# handler will turn off the SMI_ON_SLP_EN bit before actually setting the SLP_EN bit.
3	0b RO	**reserved4:** Reserved.
2	0b RW	**BIOS Enable (BIOS_EN): (bios_en):** Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes a 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set.
1	1b RW	**End of SMI (EOS): (eos):** SMI handler sets this bit when it finishes handling the SMI. Setting this bit will force the PMC internal SMI request to zero for 1 clock.Thus if the internal SMI request is still asserted due to new SMI trigger a new rising edge will happen, setting the interrupt to the PMC controller.
0	0b RW	**Global SMI Enable (GBL_SMI_EN): (gbl_smi_en):** When set, this bit enables the generation of SMIs in the system upon any enabled SMI event. This bit is reset by a PMU_PLTRST_B reset event. If this bit is not set, no SMI# will be generated. NOTE: When the SMI_LOCK bit is set, this bit cannot be changed.

3.57.7 SMI_STS - SMI Status Register (SMI_STS)—Offset 34h

Access Method

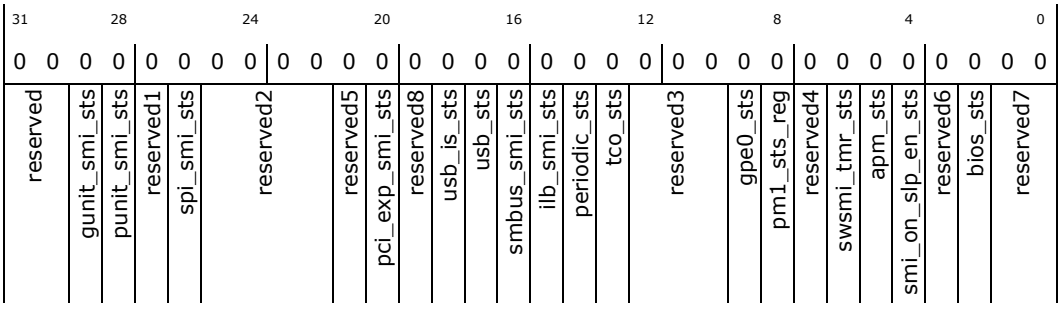
Type: I/O Register (Size: 32 bits)

SMI_STS: [ACPI_BASE_ADDRESS] + 34h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RO	**reserved:** Reserved.

Bit Range	Default & Access	Description
29	0b RW	**GUNIT SMI Status (GUNIT_SMI_STS): (gunit_smi_sts):** This bit will be set if Graphics unit is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'
28	0b RW	**PUNIT SMI Status (PUNIT_SMI_STS): (punit_smi_sts):** This bit will be set if Power Management is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'
27	0b RO	**reserved (reserved1):** Reserved.
26	0b RO	**SPI_SMI Status (SPI_SMI_STS): (spi_smi_sts):** This bit will be set when the SPI logic is requesting an SMI#
25:22	0b RO	**reserved (reserved2):** Reserved.
21	0b RW	**reserved (reserved5):** This bit is reserved for future use
20	0b RO	**PCI_EXP_SMI Status (PCI_EXP_SMI_STS): (pci_exp_smi_sts):** 1-PCI Express SMI event occurred. This could be due to a PCI Express PME event.
19	0b RO	**reserved (reserved8):** Reserved.
18	0b RO	**Intel USB2 Status (USB_IS_STS): (usb_is_sts):** This non-sticky read-only bit is a logical OR of each of the SMI status bits in the Intel-Specific USB2 SMI Status Register ANDed with the corresponding enable bits. Additionally, the Port Disable Write Enable SMI is reported in this bit; the specific status bit for this event is contained in the USB Per-Port Registers Write Control Register in this I/O space. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated USB2 Host Controllers are represented with this bit.
17	0b RO	**USB Status (USB_STS): (usb_sts):** This bit will be set when the USB logic is requesting an SMI#
16	0b RO	**SMBUS_SMI Status (SMBUS_SMI_STS): (smbus_smi_sts):** This bit will be set when the SMBUS logic is requesting an SMI#
15	0b RO	**ILB_SMI Status (ILB_SMI_STS): (ilb_smi_sts):** This bit will be set when the ILB logic is requesting an SMI#
14	0b RW	**Periodic Status (PERIODIC_STS): (periodic_sts):** This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the PMC will generate an SMI#. This bit is cleared by writing a 1 to this bit position.
13	0b RW	**TCO Status (TCO_STS): (tco_sts):** Indicates SMI was caused by the TCO logic. This bit is cleared by writing a 1 to this bit position.
12:10	0b RO	**reserved (reserved3):** Reserved.
9	0b RO	**GPE0a Status (GPE0a_STS): (gpe0_sts):** There are several status/ enable bit pairs in GPE0a_STS/EN that are capable of triggering SMI. This bit is a logical OR of all of those pairs (i.e. this bit is asserted whenever at least one of those pairs has both the status and enable bit asserted). This bit is NOT sticky. Writes to this bit will have no effect. Note: The setting of this bit does not cause the SMI#.

Bit Range	Default & Access	Description
8	0b RO	**PM1 Status Register (PM1_STS_REG): (pm1_sts_reg):** This is an OR of the bits (except for bits 5 and 4) in the ACPI PM1_STS_EN Status Reg. Not sticky. Writes to this bit have no effect. Note: The setting of this bit does not cause the SMI#.
7	0b RO	**reserved (reserved4):** Reserved.
6	0b RW	**Software SMI Timer Status (SWSMI_TMR_STS): (swsmi_tmr_sts):** This bit will be set to 1 by the hardware when the Software SMI# Timer expires. This bit will remain 1 until the software writes a 1 to this bit.
5	0b RW	**APM_STS (apm_sts):** APM Status - SMI# was generated by a write access to the APM control register and if the APMC_EN bit is set. This bit is cleared by writing a one to its bit position.
4	0b RW	**SMI_ON_SLP_EN Status (SMI_ON_SLP_EN_STS): (smi_on_slp_en_sts):** This bit will be set by the PMC when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position
3	0b RO	**reserved (reserved6):** Reserved.
2	0b RW	**BIOS Status (BIOS_STS): (bios_sts):** This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit. When both BIOS_EN and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to this bit position.
1:0	0b RO	**reserved (reserved7):** Reserved.

3.57.8 ALT_GPIO_SMI - Alternate GPIO SMI Status and Enable Register. (ALT_GPIO_SMI)—Offset 38h

reset_type=Resume Well Reset#

Access Method

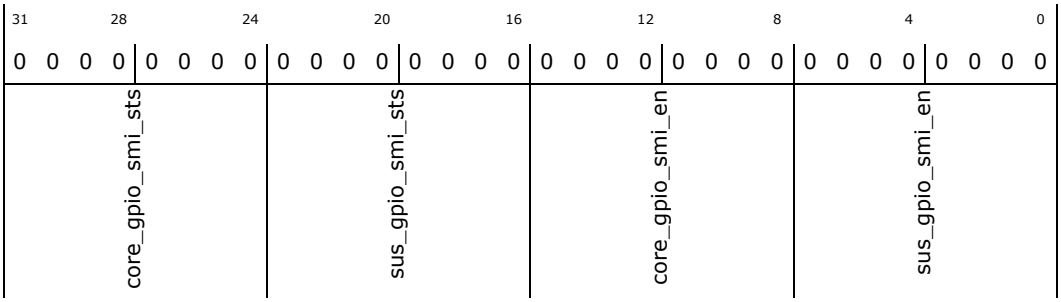
Type: I/O Register (Size: 32 bits)

ALT_GPIO_SMI: [ACPI_BASE_ADDRESS] + 38h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**CORE GPIO SMI Status Setting (CORE_GPIO_SMI_STS): (core_gpio_smi_sts):** These bits report the status of the corresponding GPIO's. 1 = active, -0 = inactive. These bits are sticky. If the following conditions are true, then an SMI# will be generated: 1. The corresponding enable bit in this register is set 2. The corresponding GPIO must be routed in the GPIO_ROUT register to cause an SMI. 3. The corresponding GPIO must be implemented. Core GPIO pins are: SATA_GP0 (GPIO core 0) SATA_GP1 (GPIO core 1) SATA_LEDN (GPIO core 2) PCIE_CLKREQ0B (GPIO core 3) PCIE_CLKREQ1B (GPIO core 4) PCIE_CLKREQ2B (GPIO core 5) PCIE_CLKREQ3B (GPIO core 6) PCIE_CLKREQ4B (GPIO core 7) All bits are in the resume well. Default for these bits are dependent on the state of the GPIO pins.
23:16	0b RW	**SUS GPIO SMI Status Setting (SUS_GPIO_SMI_STS): (sus_gpio_smi_sts):** These bits report the status of the corresponding GPIO's. 1 = active, -0 = inactive. These bits are sticky. If the following conditions are true, then an SMI# will be generated: 1. The corresponding enable bit in this register is set 2. The corresponding GPIO must be routed in the GPIO_ROUT register to cause an SMI. 3. The corresponding GPIO must be implemented. Sus GPIO pins are GPIO_SUS0-7. All bits are in the resume well. Default for these bits are dependent on the state of the GPIO pins.
15:8	0b RW	**CORE GPIO SMI Enable Setting (CORE_GPIO_SMI_EN): (core_gpio_smi_en):** These bits are used to enable the corresponding GPIO to cause an SMI#.
7:0	0b RW	**SUS GPIO SMI Enable Setting (SUS_GPIO_SMI_EN): (sus_gpio_smi_en):** These bits are used to enable the corresponding GPIO to cause an SMI#.

3.57.9 UPRWC - USB Per-Port Registers Write Control (UPRWC)—Offset 3Ch

Access Method

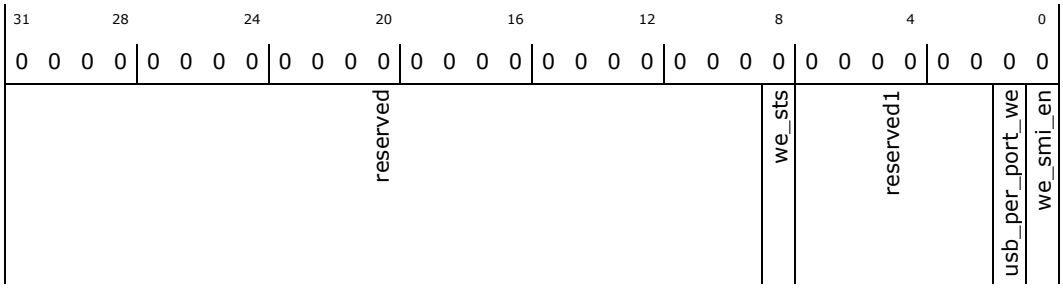
Type: I/O Register (Size: 32 bits)

UPRWC: [ACPI_BASE_ADDRESS] + 3Ch

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RO	**reserved:** Reserved.
8	0b RW	**Write Enable Status (WE_STS) (we_sts):** This bit gets set by hardware when the Per-Port Registers Write Enable bit is written from 0 to 1. This bit is cleared by software writing a 1b to this bit location. The setting condition takes precedence over the clearing condition in the event that both occur at once. When this bit is 1b and bit 0 is 1b, the INTEL_USB2_STS bit is set in the SMI_STS register.
7:2	0b RO	**reserved (reserved1):** Reserved.
1	0b RW	**USB Per-Port Registers Write Enable (USB_PER_PORT_WE) (usb_per_port_we):** This bit controls whether writes are enabled to the USB Port Power Off and Port Disable Override registers
0	0b RW	**Write Enable SMI Enable (WE_SMI_EN) (we_smi_en):** This bit enables the generation of SMI when the Per-Port Registers Write Enable (bit 1) is written from 0 to 1. Once written to 1b, this bit can not be cleared by software.

3.57.10 GPE_CTRL - General Purpose Event Control (GPE_CTRL)—Offset 40h

Access Method

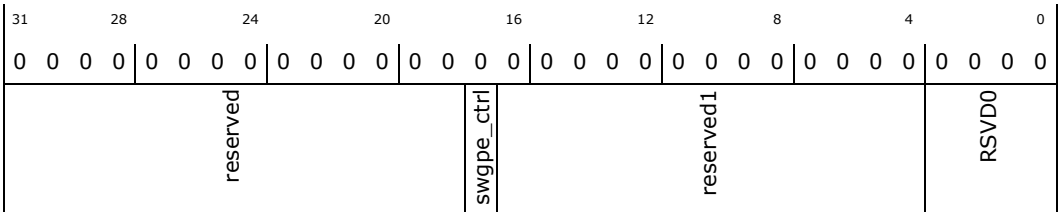
Type: I/O Register (Size: 32 bits)

GPE_CTRL: [ACPI_BASE_ADDRESS] + 40h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:18	0b RO	**reserved:** Reserved.

Bit Range	Default & Access	Description
17	0b RW	**Software GPE Control (SWGPE_CTRL) (swgpe_ctrl):** This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0a_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. In addition to being reset by RSMRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip
16:4	0b RO	**reserved1:** Reserved.
3:0	0b RO	**RSVD0:** Reserved

3.57.11 PM2A_CNT_BLK - PM2a Control Block (PM2A_CNT_BLK)—Offset 50h

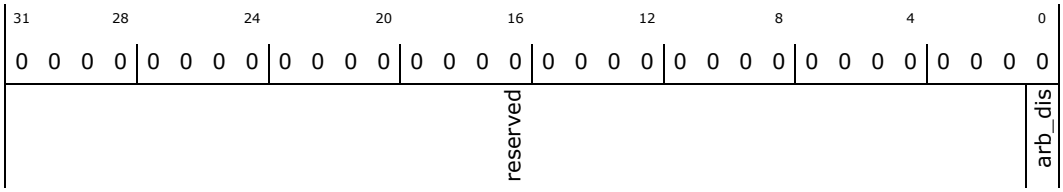
Access Method

Type: I/O Register (Size: 32 bits)

PM2A_CNT_BLK: [ACPI_BASE_ADDRESS] + 50h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**reserved:** Reserved.
0	0b RW	**ARB_DIS (ARB_DIS) (arb_dis):** This bit is essentially just a scratchpad bit for legacy software compatibility.

3.57.12 TCO_RLD: TCO Reload Register (TCO_RLD)—Offset 60h

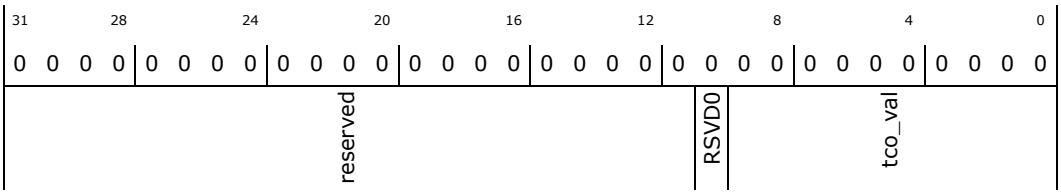
Access Method

Type: I/O Register (Size: 32 bits)

TCO_RLD: [ACPI_BASE_ADDRESS] + 60h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:11	0b RO	**reserved:** Reserved.
10	0b RO	**RSVD0:** Reserved
9:0	0b RO	**TCO Timer Value (TCO_TVAL) (tco_val):** Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

3.57.13 TCO_STS: TCO Timer Status (TCO_STS)—Offset 64h

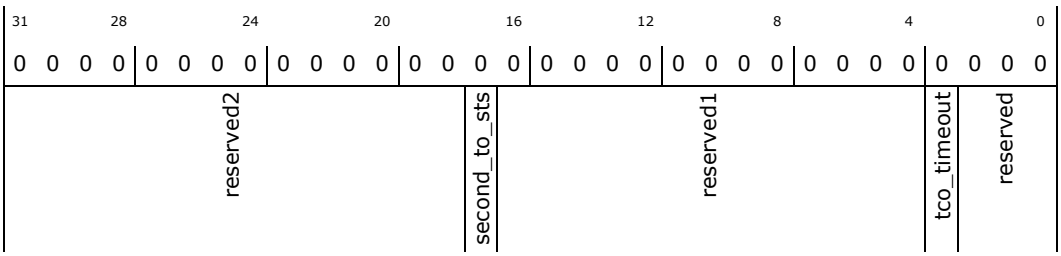
Access Method

Type: I/O Register (Size: 32 bits)

TCO_STS: [ACPI_BASE_ADDRESS] + 64h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:18	0b RO	**reserved (reserved2):** Reserved.
17	0b RW	**Second Timeout Status(SECOND_TO_STS) (second_to_sts):** PMC sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the PMC will reboot the system after the second timeout. The reboot is done by asserting PMU_PLTRST_B. This bit is only cleared by writing a 1 to this bit or by a RSMRST_B.
16:4	0b RO	**reserved (reserved1):** Reserved.

Bit Range	Default & Access	Description
3	0b RW	**TCO Timeout (TCO_TIMEOUT) (tco_timeout):** Bit set to 1 by PMC to indicate that the SMI was caused by TCO timer reaching 0.
2:0	0b RO	**reserved:** Reserved.

3.57.14 TCO1_CNT: TCO Timer Control (TCO1_CNT)—Offset 68h

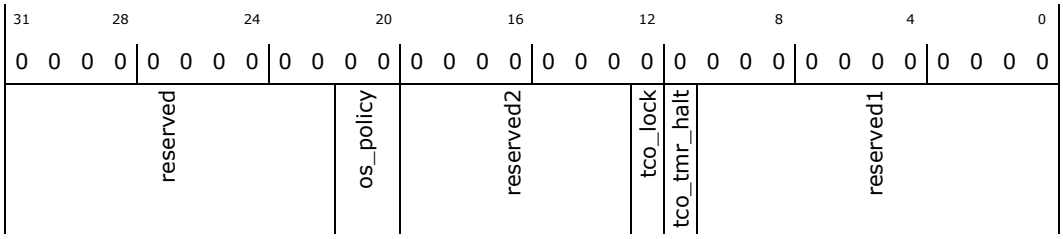
Access Method

Type: I/O Register (Size: 32 bits)

TCO1_CNT: [ACPI_BASE_ADDRESS] + 68h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0b RO	**reserved:** Reserved.
21:20	0b RW	**OS_POLICY (os_policy):** OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00 Boot normally 01 Shut down 10 Do not load OS. Hold in pre-boot state and use LAN to determine next step 11 Reserved
19:13	0b RO	**reserved (reserved2):** Reserved.
12	0b RW	**TCO Lock (TCO_LOCK) (tco_lock):** When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	0b RW	**TCO Timer Halt (TCO_TMR_HALT) (tco_tmr_halt):** 1 = The TCO timer will halt. It will not count, and thus cannot reach a value that would cause an SMI# or to cause the SECOND_TO_STS bit to be set. This will also prevent rebooting. 0 = The TCO timer is enabled to count. This is the default.
10:0	0b RO	**reserved1:** Reserved.

3.57.15 TCO_TMR: TCO Timer Register (TCO_TMR)—Offset 70h

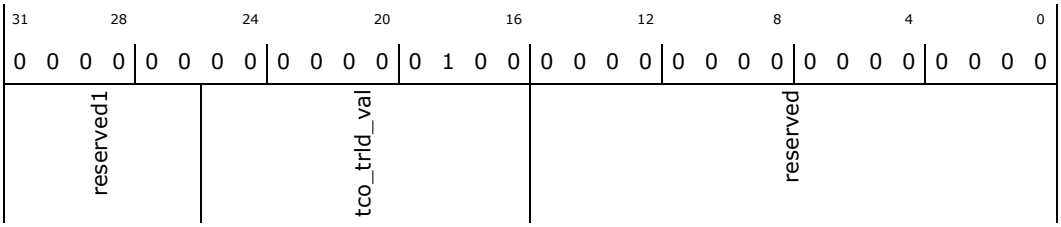
Access Method

Type: I/O Register (Size: 32 bits)

TCO_TMR: [ACPI_BASE_ADDRESS] + 70h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00040000h



Bit Range	Default & Access	Description
31:26	0b RO	**reserved (reserved1):** Reserved.
25:16	004h RW	**TCO Timer reload value (TCO_TRLD_VAL) (tco_trld_val):** Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. Note: The timer has an error of +/- 1 tick (0.6s). The TCO Timer will only count down in the S0 state.
15:0	0b RO	**reserved:** Reserved.

3.58 PCU SPI for Firmware Memory Mapped I/O Registers

Table 66. Summary of PCU SPI for Firmware Memory Mapped I/O Registers—SPI_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"BFPREG (BIOS_Flash_Primary_Region_bios)—Offset 0h" on page 3103	00001FFFh
4h	2	"HSFSTS (Hardware_Sequencing_Flash_Status_bios)—Offset 4h" on page 3104	0000h
6h	2	"HSFCTL (Hardware_Sequencing_Flash_Control_bios)—Offset 6h" on page 3105	0000h
8h	4	"FADDR (Flash_Address_bios)—Offset 8h" on page 3106	00000000h
10h	4	"FDATA0 (Flash_Data_0_bios)—Offset 10h" on page 3107	00000000h
14h	4	"FDATA1 (Flash_Data_1_bios)—Offset 14h" on page 3107	00000000h
18h	4	"FDATA2 (Flash_Data_2_bios)—Offset 18h" on page 3108	00000000h
1Ch	4	"FDATA3 (Flash_Data_3_bios)—Offset 1Ch" on page 3108	00000000h
20h	4	"FDATA4 (Flash_Data_4_bios)—Offset 20h" on page 3109	00000000h
24h	4	"FDATA5 (Flash_Data_5_bios)—Offset 24h" on page 3109	00000000h
28h	4	"FDATA6 (Flash_Data_6_bios)—Offset 28h" on page 3110	00000000h
2Ch	4	"FDATA7 (Flash_Data_7_bios)—Offset 2Ch" on page 3110	00000000h
30h	4	"FDATA8 (Flash_Data_8_bios)—Offset 30h" on page 3111	00000000h
34h	4	"FDATA9 (Flash_Data_9_bios)—Offset 34h" on page 3111	00000000h
38h	4	"FDATA10 (Flash_Data_10_bios)—Offset 38h" on page 3112	00000000h
3Ch	4	"FDATA11 (Flash_Data_11_bios)—Offset 3Ch" on page 3112	00000000h
40h	4	"FDATA12 (Flash_Data_12_bios)—Offset 40h" on page 3113	00000000h
44h	4	"FDATA13 (Flash_Data_13_bios)—Offset 44h" on page 3113	00000000h
48h	4	"FDATA14 (Flash_Data_14_bios)—Offset 48h" on page 3114	00000000h
4Ch	4	"FDATA15 (Flash_Data_15_bios)—Offset 4Ch" on page 3114	00000000h
50h	4	"FRACC (Flash_Region_Access_Permissions_bios)—Offset 50h" on page 3115	00000202h
54h	4	"FREG0 (Flash_Region_0_bios)—Offset 54h" on page 3116	00001FFFh
58h	4	"FREG1 (Flash_Region_1_bios)—Offset 58h" on page 3117	00001FFFh
5Ch	4	"FREG2 (Flash_Region_2_bios)—Offset 5Ch" on page 3117	00001FFFh
60h	4	"FREG3 (Flash_Region_3_bios)—Offset 60h" on page 3118	00001FFFh
64h	4	"FREG4 (Flash_Region_4_bios)—Offset 64h" on page 3119	00001FFFh
74h	4	"PR0 (Protected_Range_0_bios)—Offset 74h" on page 3119	00000000h
78h	4	"PR1 (Protected_Range_1_bios)—Offset 78h" on page 3120	00000000h
7Ch	4	"PR2 (Protected_Range_2_bios)—Offset 7Ch" on page 3121	00000000h
80h	4	"PR3 (Protected_Range_3_bios)—Offset 80h" on page 3122	00000000h

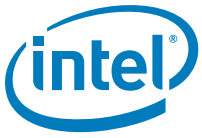


Table 66. Summary of PCU SPI for Firmware Memory Mapped I/O Registers—SPI_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
84h	4	"PR4 (Protected_Range_4_bios)—Offset 84h" on page 3123	00000000h
90h	4	"SSFCTLSTS (Software_Sequencing_Flash_Control_Status_bios)—Offset 90h" on page 3124	F8000000h
94h	2	"PREOP (Prefix_Opcode_Configuration_bios)—Offset 94h" on page 3126	0000h
96h	2	"OPTYPE (Opcode_Type_Configuration_bios)—Offset 96h" on page 3127	0000h
98h	4	"OPMENU0 (Opcode_Menu_Configuration_0_bios)—Offset 98h" on page 3128	00000000h
9Ch	4	"OPMENU1 (Opcode_Menu_Configuration_1_bios)—Offset 9Ch" on page 3129	00000000h
A4h	4	"LOCK (Individual_Lock_Register)—Offset A4h" on page 3130	00000000h
B0h	4	"FDOC (Flash_Descriptor_Observability_Control_bios)—Offset B0h" on page 3131	00000000h
B4h	4	"FDOD (Flash_Descriptor_Observability_Data_bios)—Offset B4h" on page 3131	00000000h
C0h	4	"AFC (Additional_Flash_Control_bios)—Offset C0h" on page 3132	00000000h
C4h	4	"LVSCC (Lower_Vendor_Specific_Component_Capabilities_bios)—Offset C4h" on page 3133	00000000h
C8h	4	"UVSCC (Upper_Vendor_Specific_Component_Capabilities_bios)—Offset C8h" on page 3134	00000000h
D0h	4	"FPB (Flash_Partition_Boundary_bios)—Offset D0h" on page 3135	00000000h
F8h	4	"SCS (SMI_Control_Status_Register_bios)—Offset F8h" on page 3136	00000080h
FCh	4	"BCR (BIOS_Control_Register_bios)—Offset FCh" on page 3136	00000020h
100h	4	"TCGC (Trunk_Clock_Gating_Control_bios)—Offset 100h" on page 3138	00000510h

3.58.1 BFPREG (BIOS_Flash_Primary_Region_bios)—Offset 0h

BIOS flash primary region addresses

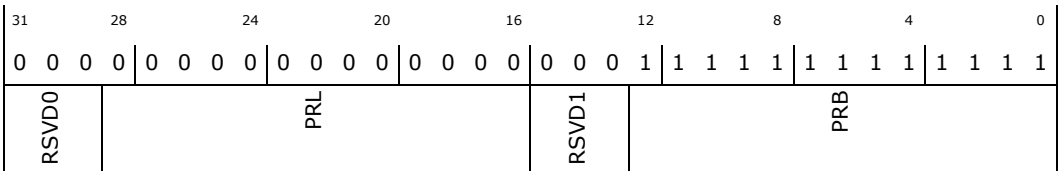
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BIOS_Flash_Primary_Region_bios: [SPI_BASE_ADDRESS] + 0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**BIOS Flash Primary Region Limit (PRL):** This specifies address bits 24:12 for the Primary Region Limit. The value in this register loaded from the contents in the Flash Descriptor.FLREG1.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**BIOS Flash Primary Region Base (PRB):** This specifies address bits 24:12 for the Primary Region Base The value in this register iloaded from the contents in the Flash Descriptor.FLREG1.Region Base

3.58.2 HSFSTS (Hardware_Sequencing_Flash_Status_bios)—Offset 4h

Hardware sequencing flash status Note: If operating in Non-Descriptor mode, the Software Sequencing Flash Status register must be used.

Access Method

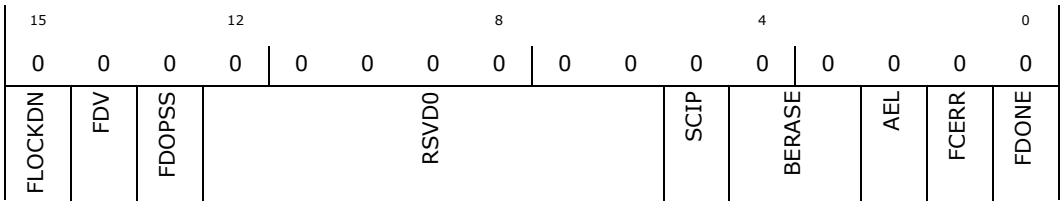
Type: Memory Mapped I/O Register (Size: 16 bits)

Hardware_Sequencing_Flash_Status_bios: [SPI_BASE_ADDRESS] + 4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW/L	**Flash Configuration Lock-Down (FLOCKDN):** When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
14	0b RO	**Flash Descriptor Valid (FDV):** This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1 , software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set.
13	0b RO	**Flash Descriptor Override Pin-Strap Status (FDOPSS):** This register reflects the value the Flash Descriptor Override Pin-Strap. '1': No override '0': The Flash Descriptor Override strap is set
12:6	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
5	0b RO	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4:3	00b RO	**Block/Sector Erase Size (BERASE):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: 00 : 256 Byte 01 : 4K Byte 10 : 8K Byte 11 : 64K Byte If the FLA (FPBA then this field reflects the value in the LVSCC.LBES register. If the FLA)= FPBA then this field reflects the value in the UVSCC.UBES register.
2	0b RW/1C	**Access Error Log (AEL):** Hardware sets this bit to a 1 when a direct read was made by BIOS that violated the security restrictions. Or , when a SB transaction to read/write one of the BIOS registers was accepted with bad SAI - see security table. This bit has no affect on indirect accesses. This bit is cleared by software writing a 1.
1	0b RW/1C	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1 when an program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occurs. Software must clear this bit before setting the FLASH Cycle GO bit in this register.
0	0b RW/1C	**Flash Cycle Done (FDONE):** The SPI controller sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.

3.58.3 HSFCTL (Hardware_Sequencing_Flash_Control_bios)—Offset 6h

Hardware sequencing flash control.

Access Method

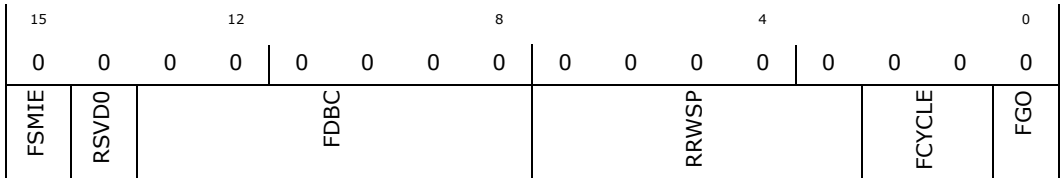
Type: Memory Mapped I/O Register (Size: 16 bits)

Hardware_Sequencing_Flash_Control_bios: [SPI_BASE_ADDRESS] + 6h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**Flash SPI SMI# Enable (FSMIE):** When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
14	0b RO	**RSVD0:** Reserved
13:8	00h RW	**Flash Data Byte Count (FDBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b representing 1 byte and 111111b representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
7:3	00h RW	**Reserved RW Scratch Pad (RRWSP):** Reserved: Scratch Pad bits that are R/W to be used during ECO
2:1	00b RW	**FLASH Cycle (FCYCLE):** This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 Read (1 up to 64 bytes by setting FDBC) 01 Reserved 10 Write (1 up to 64 bytes by setting FDBC) 11 Block Erase Implementation Note: if reserved 2'b01 is programmed to this field, flash controller will handle it as if it is 00 (Read)
0	0b RW/SE	**Flash Cycle Go (FGO):** A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.

3.58.4 FADDR (Flash_Address_bios)—Offset 8h

Flash address

Access Method

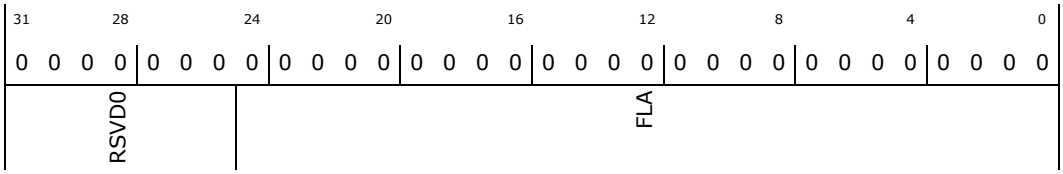
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Address_bios: [SPI_BASE_ADDRESS] + 8h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
24:0	00000000h RW	**Flash Linear Address (FLA):** The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus. When operating in Tekoa mode bit 24 is ignored and the FLA[lb]13:0[rb] is the FPA.

3.58.5 FDATA0 (Flash_Data_0_bios)—Offset 10h

Flash data #0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

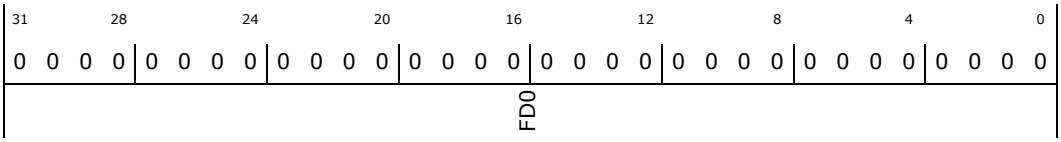
Flash_Data_0_bios: [SPI_BASE_ADDRESS] + 10h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 0 (FD0):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- 8-23-22- 16-31 24 Bit 24 is the last bit shifted out/in. There are no alignment assumptions, byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

3.58.6 FDATA1 (Flash_Data_1_bios)—Offset 14h

Flash data #1

Access Method

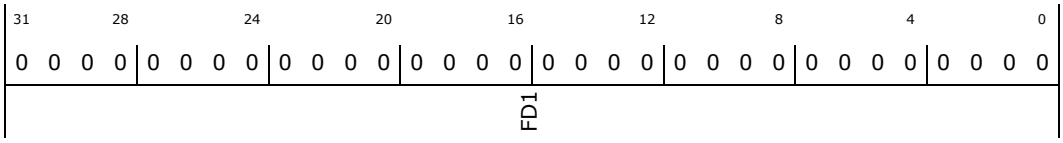
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_1_bios: [SPI_BASE_ADDRESS] + 14h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 1 (FD1):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD0 has completely shifted in/out.

3.58.7 FDATA2 (Flash_Data_2_bios)—Offset 18h

Flash data #2

Access Method

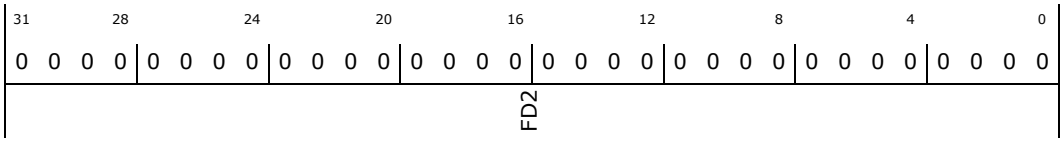
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_2_bios: [SPI_BASE_ADDRESS] + 18h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 2 (FD2):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD1 has completely shifted in/out.

3.58.8 FDATA3 (Flash_Data_3_bios)—Offset 1Ch

Flash data #3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

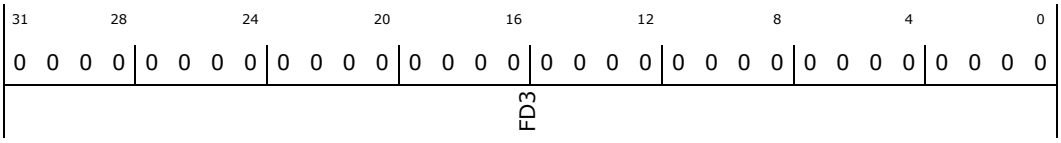
Flash_Data_3_bios: [SPI_BASE_ADDRESS] + 1Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 3 (FD3):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD2 has completely shifted in/out.

3.58.9 FDATA4 (Flash_Data_4_bios)—Offset 20h

Flash data #4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

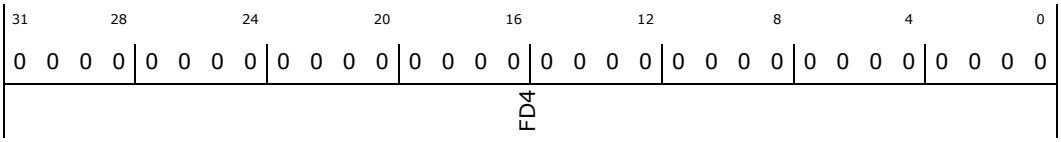
Flash_Data_4_bios: [SPI_BASE_ADDRESS] + 20h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 4 (FD4):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD3 has completely shifted in/out.

3.58.10 FDATA5 (Flash_Data_5_bios)—Offset 24h

Flash data #5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

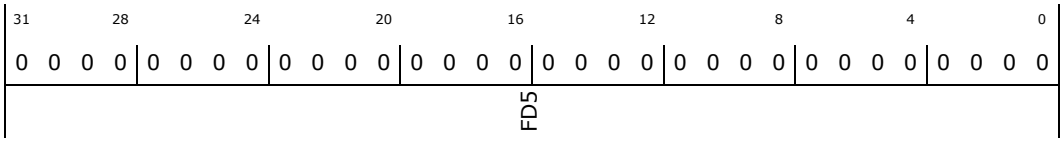
Flash_Data_5_bios: [SPI_BASE_ADDRESS] + 24h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 5 (FD5):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD4 has completely shifted in/out.

3.58.11 FDATA6 (Flash_Data_6_bios)—Offset 28h

Flash data #6

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

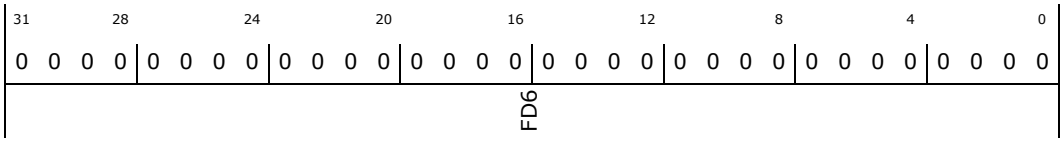
Flash_Data_6_bios: [SPI_BASE_ADDRESS] + 28h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 6 (FD6):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD5 has completely shifted in/out.

3.58.12 FDATA7 (Flash_Data_7_bios)—Offset 2Ch

Flash data #7

Access Method

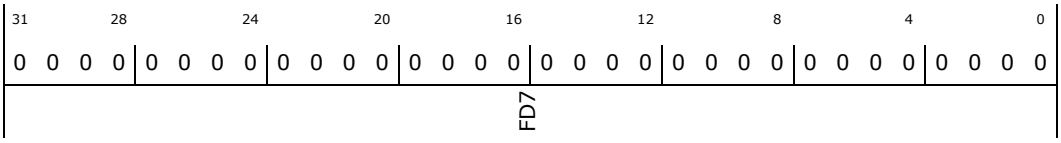
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_7_bios: [SPI_BASE_ADDRESS] + 2Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 7 (FD7):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD6 has completely shifted in/out.

3.58.13 FDATA8 (Flash_Data_8_bios)—Offset 30h

Flash data #8

Access Method

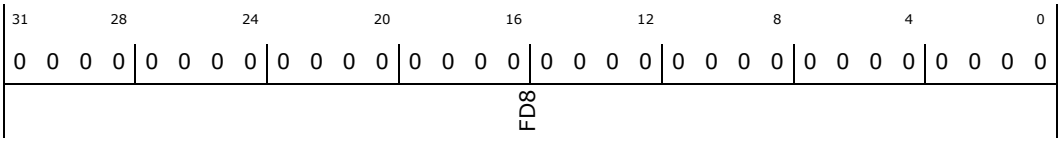
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_8_bios: [SPI_BASE_ADDRESS] + 30h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 8 (FD8):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD7 has completely shifted in/out.

3.58.14 FDATA9 (Flash_Data_9_bios)—Offset 34h

Flash data #9

Access Method

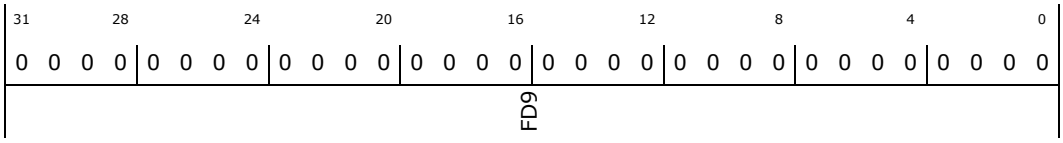
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_9_bios: [SPI_BASE_ADDRESS] + 34h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 9 (FD9):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD8 has completely shifted in/out.

3.58.15 FDATA10 (Flash_Data_10_bios)—Offset 38h

Flash data #10

Access Method

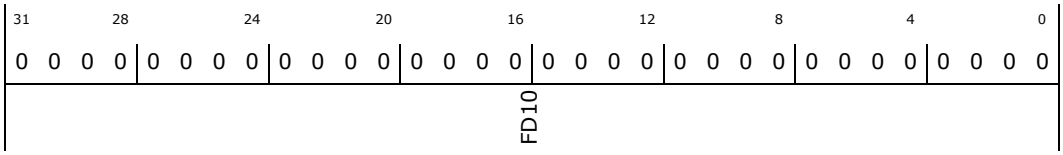
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_10_bios: [SPI_BASE_ADDRESS] + 38h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 10 (FD10):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD9 has completely shifted in/out.

3.58.16 FDATA11 (Flash_Data_11_bios)—Offset 3Ch

Flash data #11

Access Method

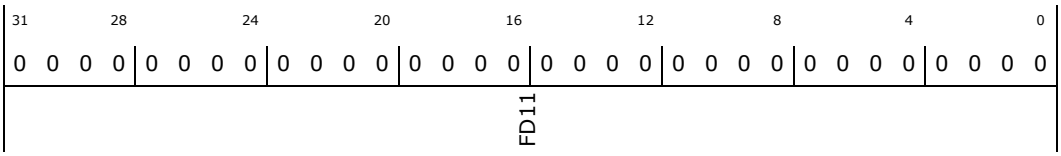
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_11_bios: [SPI_BASE_ADDRESS] + 3Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 11 (FD11):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD10 has completely shifted in/out.

3.58.17 FDATA12 (Flash_Data_12_bios)—Offset 40h

Flash data #12

Access Method

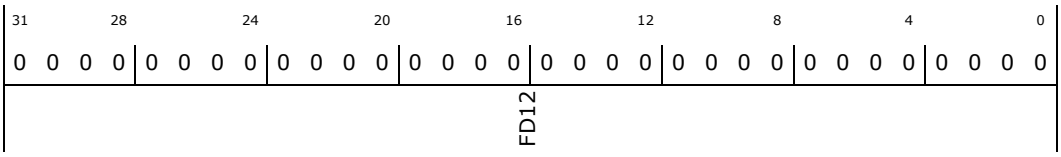
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_12_bios: [SPI_BASE_ADDRESS] + 40h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 12 (FD12):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD11 has completely shifted in/out.

3.58.18 FDATA13 (Flash_Data_13_bios)—Offset 44h

Flash data #13

Access Method

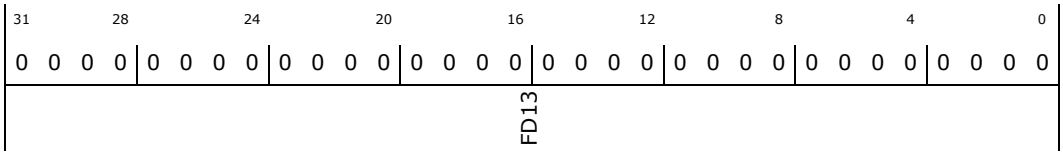
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_13_bios: [SPI_BASE_ADDRESS] + 44h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 13 (FD13):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD12 has completely shifted in/out.

3.58.19 FDATA14 (Flash_Data_14_bios)—Offset 48h

Flash data #14

Access Method

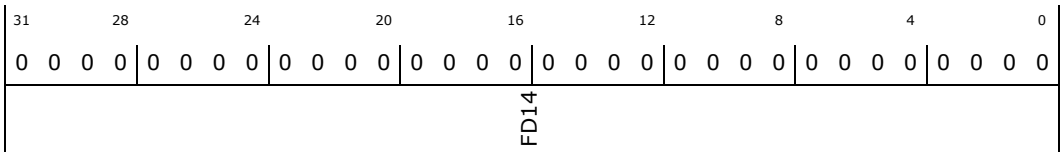
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_14_bios: [SPI_BASE_ADDRESS] + 48h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 14 (FD14):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD13 has completely shifted in/out.

3.58.20 FDATA15 (Flash_Data_15_bios)—Offset 4Ch

Flash data #15

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

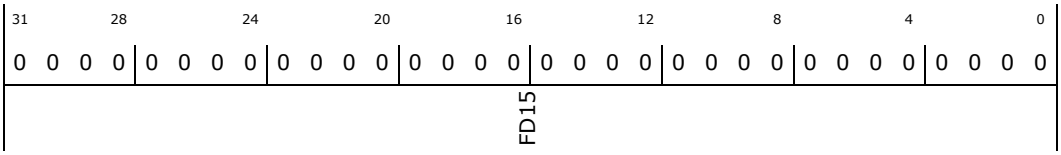
Flash_Data_15_bios: [SPI_BASE_ADDRESS] + 4Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 15 (FD15):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD14 has completely shifted in/out.

3.58.21 FRACC (Flash_Region_Access_Permissions_bios)—Offset 50h

Flash region access permissions

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

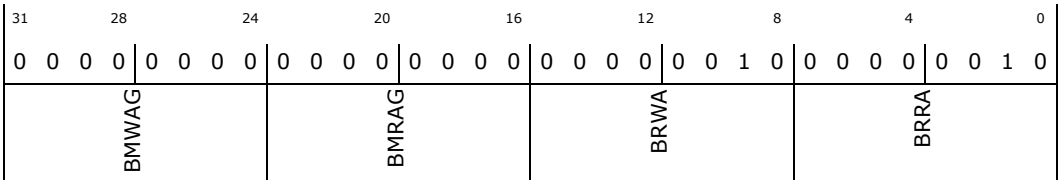
Flash_Region_Access_Permissions_bios: [SPI_BASE_ADDRESS] + 50h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000202h



Bit Range	Default & Access	Description
31:24	00h RW/L	**BIOS Master Write Access Grant (BMWAG):** Each bit [lb]31:24[rb] corresponds to Master[lb]7:0[rb]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. Master[lb]1[rb] is Host CPU/BIOS, Master[lb]2[rb] is SEC, Master[lb]3[rb] is GBE. Master[lb]0[rb] and Master[lb]7:4[rb] are reserved. The contents of this register are locked by the FLOCKDN or BMWAGLOCKDN bits.

Bit Range	Default & Access	Description
23:16	00h RW/L	**BIOS Master Read Access Grant (BMRAG):** Each bit [lb]23:16[rb] corresponds to Master[lb]7:0[rb]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. Master[lb]1[rb] is Host CPU/BIOS, Master[lb]2[rb] is SEC, Master[lb]3[rb] is GBE. Master[lb]0[rb] and Master[lb]7:4[rb] are reserved. The contents of this register are locked by the FLOCKDN or BMRAGLOCKDN bit.
15:8	02h RO	**BIOS Region Write Access (BRWA):** Each bit [lb]15:8[rb] corresponds to Regions [lb]7:0[rb]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the write access to its own Region 1 by default. Thus, the reset default of this field will be read as 8'h02 regardless of descriptor or non-descriptor mode.
7:0	02h RO	**BIOS Region Read Access (BRRA):** Each bit [lb]7:0[rb] corresponds to Regions [lb]7:0[rb]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the read access to its own Region 1 by default. Thus, the reset default of this field will be read as 8'h02 regardless of descriptor or non-descriptor mode.

3.58.22 FREG0 (Flash_Region_0_bios)—Offset 54h

Flash region 0 (flash descriptor)

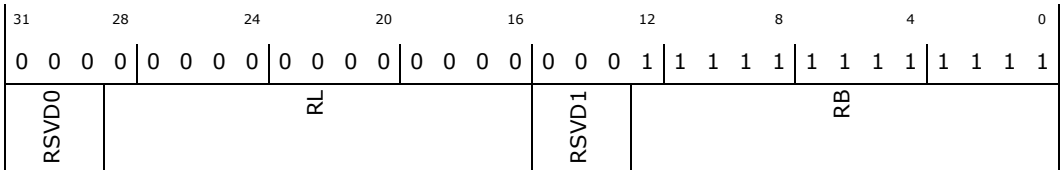
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_0_bios: [SPI_BASE_ADDRESS] + 54h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base

3.58.23 FREG1 (Flash_Region_1_bios)—Offset 58h

Flash region 1 (BIOS)

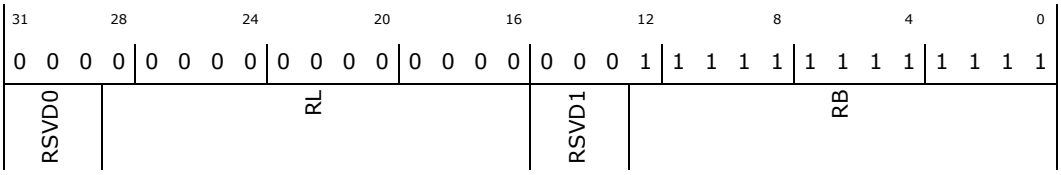
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_1_bios: [SPI_BASE_ADDRESS] + 58h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 1 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base

3.58.24 FREG2 (Flash_Region_2_bios)—Offset 5Ch

Flash region 2 (SEC)

Access Method

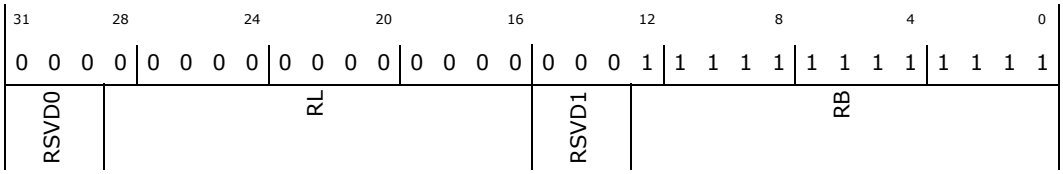
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_2_bios: [SPI_BASE_ADDRESS] + 5Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base

3.58.25 FREG3 (Flash_Region_3_bios)—Offset 60h

Flash region 3 (GBE)

Access Method

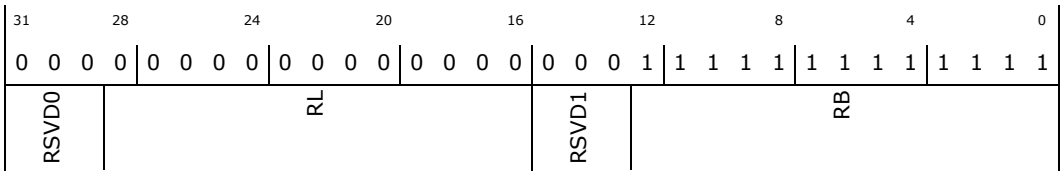
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_3_bios: [SPI_BASE_ADDRESS] + 60h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base

3.58.26 FREG4 (Flash_Region_4_bios)—Offset 64h

Flash region 4 (platform data)

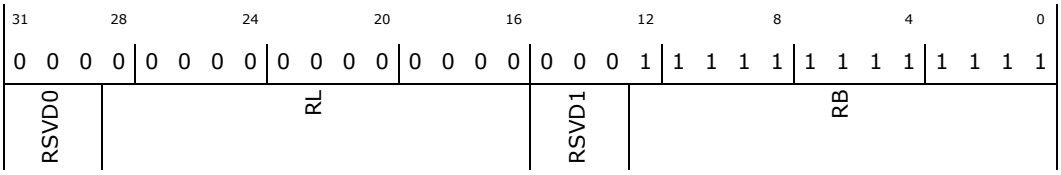
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_4_bios: [SPI_BASE_ADDRESS] + 64h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 4 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base

3.58.27 PR0 (Protected_Range_0_bios)—Offset 74h

Protected range #0. This register can not be written when the FLOCKDN or PR0LOCKDN bits are set to 1.

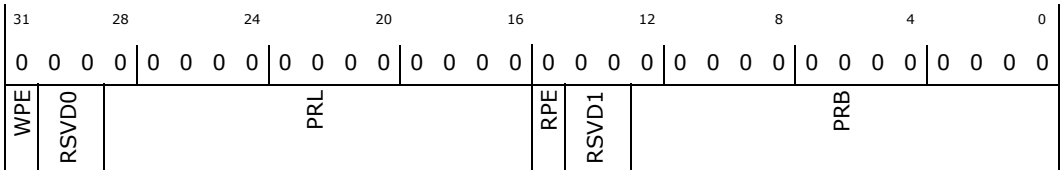
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_0_bios: [SPI_BASE_ADDRESS] + 74h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

3.58.28 PR1 (Protected_Range_1_bios)—Offset 78h

Protected range #1. This register can not be written when the FLOCKDN or PR1LOCKDN bits are set to 1.

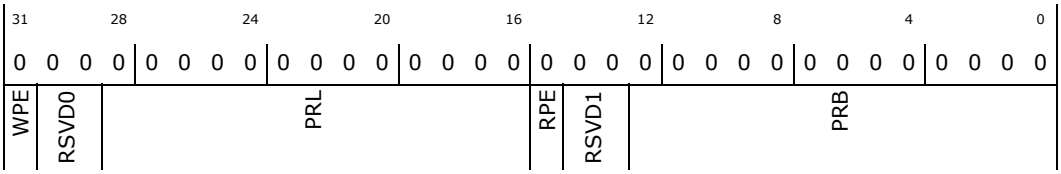
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_1_bios: [SPI_BASE_ADDRESS] + 78h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

3.58.29 PR2 (Protected_Range_2_bios)—Offset 7Ch

Protected range #2. This register can not be written when the FLOCKDN or PR2LOCKDN bits are set to 1.

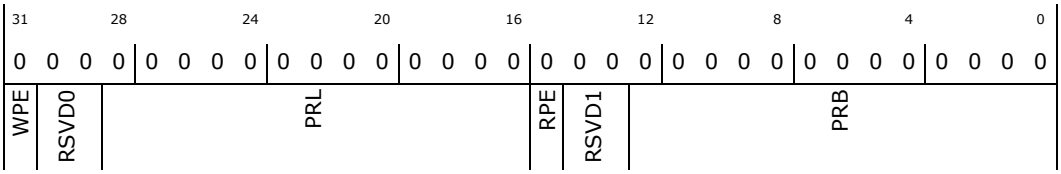
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_2_bios: [SPI_BASE_ADDRESS] + 7Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

3.58.30 PR3 (Protected_Range_3_bios)—Offset 80h

Protected range #3. This register can not be written when the FLOCKDN or PR3LOCKDN bits are set to 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_3_bios: [SPI_BASE_ADDRESS] + 80h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.

Bit Range	Default & Access	Description
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

3.58.31 PR4 (Protected_Range_4_bios)—Offset 84h

Protected range #4. This register use for H/W range protection. All register values are coming from soft-straps, and the Write Protection Enable is controlled also by the Flash Security Override Pin Strap

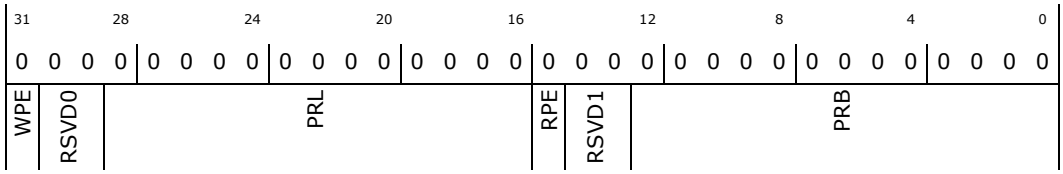
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_4_bios: [SPI_BASE_ADDRESS] + 84h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31	X RO	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. This field value should be an or between soft-strap and the ~Flash Security Override Pin Strap. Such, H/W range protection is active only if write protection is enabled by soft-strap and Flash Security Override Pin Strap is deasserted.

Bit Range	Default & Access	Description
30:29	0b RO	**RSVD0:** Reserved
28:16	X RO	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. This field value should be taken from soft-straps.
15	0b RO	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. This field should be always 1'b0
14:13	0b RO	**RSVD1:** Reserved
12:0	X RO	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. This field value should be taken from soft-straps.

3.58.32 SSFCTLSTS (Software_Sequencing_Flash_Control_Status_bios)—Offset 90h

The software sequencing flash control and Status register is a combination of two registers the software sequencing flash status register (bits 7:0) and the software sequencing flash control register (bits 31:8). This register is intended to be used only as a back-up mode to the hardware sequencing control and status registers.

Access Method

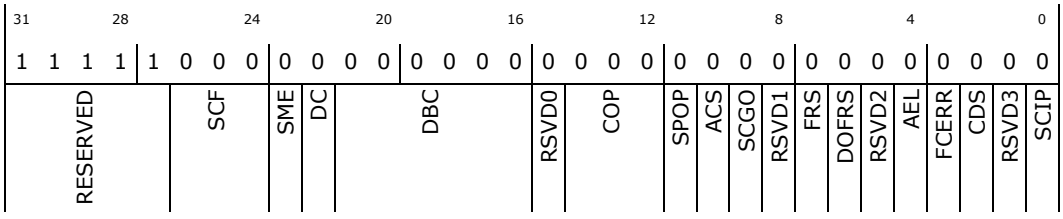
Type: Memory Mapped I/O Register (Size: 32 bits)

Software_Sequencing_Flash_Control_Status_bios: [SPI_BASE_ADDRESS] + 90h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: F8000000h



Bit Range	Default & Access	Description
31:27	11111b RO	**RESERVED:** reserved, should be with default 1

Bit Range	Default & Access	Description
26:24	000b RW/L	**SPI Cycle Frequency (SCF):** 000 : 20MHz 001 : 33MHz 010 : 66MHz (reserved - not supported on VLV) 011 : 25MHz (reserved - not supported on VLV) 100 : 50MHz (reserved - not supported on VLV-DC) All Others: Reserved This register sets frequency to use for all SPI Software Sequencing cycles (write, erase, fast read, read status, .etc) except for the Read cycle which always run at 20MHz. This register is locked when the SPI Configuration Lock-Down bit is set or when FREQLOCKDN bit is set.
23	0b RW	**SPI SMI# Enable (SME):** When set to 1, the SPI asserts an SMI# request whenever the Cycle Done Status bit is 1.
22	0b RW	**Data Cycle (DC):** When set to 1, there is data that corresponds to this transaction. When 0, no data is delivered for this cycle, and the DBC and data fields themselves are don t cares.
21:16	000000b RW	**Data Byte Count (DBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 63. The number of bytes transferred is the value of this field plus 1. Note that when this field is 00_0000b, then there is 1 byte to transfer and that 11_1111b means there are 64 bytes to transfer.
15	0b RO	**RSVD0:** Reserved
14:12	000b RW	**Cycle Opcode Pointer (COP):** This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
11	0b RW	**Sequence Prefix Opcode Pointer (SPOP):** This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the SPI controller supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
10	0b RW	**Atomic Cycle Sequence (ACS):** When set to 1 along with the SCGO assertion, the SPI controller will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of:) Atomic Sequence Prefix Command (8-bit opcode only)) Primary Command specified below by software (can include address and data)) Polling the Flash Status Register (opcode 8'h05) until bit 0 becomes 1'b0. The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0.
9	0b RW/SE	**SPI Cycle Go (SCGO):** This bit always returns 1'b0 on reads. However, a write to this register with a 1'b1 in this bit starts the SPI cycle defined by the other bits of this register. The SPI Cycle in Progress (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1'b1. This saves an additional memory write.
8	0b RO	**RSVD1:** Reserved
7	0b RO/U	**Fast Read Supported (FRS):** This bit reflects the value of the Fast Read Support bit in the Flash Descriptor Component Section.

Bit Range	Default & Access	Description
6	0b RO/U	**Dual Output Fast Read Supported (DOFRS):** This bit reflects the value of the Dual Output Fast Read Support bit in the Flash Descriptor Component Section.
5	0b RO	**RSVD2:** Reserved
4	0b RO	**Access Error Log (AEL):** This bit reflects the value of the Hardware Sequencing Status.AEL register.
3	0b RW/1C	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1'b1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset.
2	0b RW/1C	**Cycle Done Status (CDS):** The SPI controller sets this bit to 1'b1 when the SPI Cycle completes i.e., SCIP bit is 1'b0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.
1	0b RO	**RSVD3:** Reserved
0	0b RO	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 1'b0.

3.58.33 PREOP (Prefix_Opcode_Configuration_bios)—Offset 94h

Prefix opcode configuration. This register is not writable when the SPI Configuration Lock-Down bit is set or when the PREOPLOCKDN bit is set.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

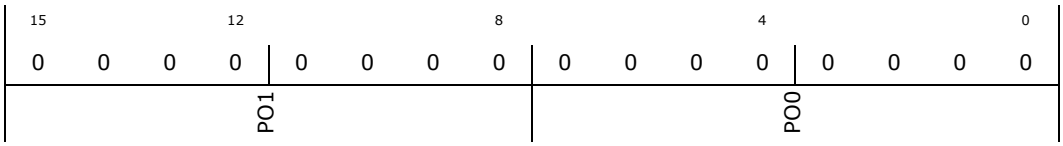
Prefix_Opcode_Configuration_bios: [SPI_BASE_ADDRESS] + 94h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RW/L	**Prefix Opcode 1 (PO1):** Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	00h RW/L	**Prefix Opcode 0 (PO0):** Prefix Opcode 0: Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

3.58.34 OPTYPE (Opcode_Type_Configuration_bios)—Offset 96h

Opcode type configuration. This register is not writable when the Flash Configuration Lock-Down bit is set or when the OPTYPELOCKDN bit is set. Entries in this register correspond to the entries in the Opcode Menu Configuration register. Note that the definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, Chip Erase and Auto-Address Increment Byte Program).

Access Method

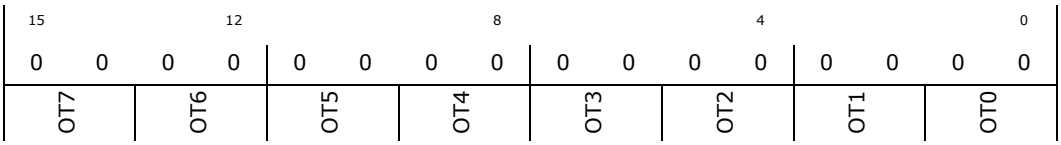
Type: Memory Mapped I/O Register (Size: 16 bits)

Opcode_Type_Configuration_bios: [SPI_BASE_ADDRESS] + 96h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 0000h



Bit Range	Default & Access	Description
15:14	00b RW/L	**Opcode Type 7 (OT7):** See the description for bits 1:0
13:12	00b RW/L	**Opcode Type 6 (OT6):** See the description for bits 1:0
11:10	00b RW/L	**Opcode Type 5 (OT5):** See the description for bits 1:0
9:8	00b RW/L	**Opcode Type 4 (OT4):** See the description for bits 1:0
7:6	00b RW/L	**Opcode Type 3 (OT3):** See the description for bits 1:0
5:4	00b RW/L	**Opcode Type 2 (OT2):** See the description for bits 1:0
3:2	00b RW/L	**Opcode Type 1 (OT1):** See the description for bits 1:0

Bit Range	Default & Access	Description
1:0	00b RW/L	**Opcode Type 0 (OT0):** This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The hardware implementation also uses the read vs. write information for modifying the behavior of the SPI interface logic. The encoding of the two bits is: 00 = No Address associated with this Opcode and Read Cycle type 01 = No Address associated with this Opcode and Write Cycle type 10 = Address required, Read cycle type 11 = Address required, Write cycle type

3.58.35 OPMENU0 (Opcode_Menu_Configuration_0_bios)—Offset 98h

Opcode (0-3) Menu Configuration. This register is not writable when the SPI Configuration Lock-Down bit is set or when OPMENULOCKDN bit is set. Four entries are available in this register and four are available in OPMENU1 register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices. It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Access Method

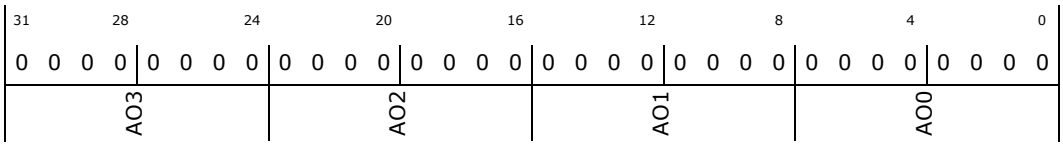
Type: Memory Mapped I/O Register (Size: 32 bits)

Opcode_Menu_Configuration_0_bios: [SPI_BASE_ADDRESS] + 98h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RW/L	**Allowable Opcode 3 (AO3):** See the description for bits 7:0
23:16	00h RW/L	**Allowable Opcode 2 (AO2):** See the description for bits 7:0
15:8	00h RW/L	**Allowable Opcode 1 (AO1):** See the description for bits 7:0

Bit Range	Default & Access	Description
7:0	00h RW/L	**Allowable Opcode 0 (AO0):** Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

3.58.36 OPMENU1 (Opcode_Menu_Configuration_1_bios)—Offset 9Ch

Opcode (7-4) Menu Configuration. This register is not writable when the SPI Configuration Lock-Down bit is set or when OPMENULOCKDN bit is set. Four entries are available in this register and four are available in OPMENU0 register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices. It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

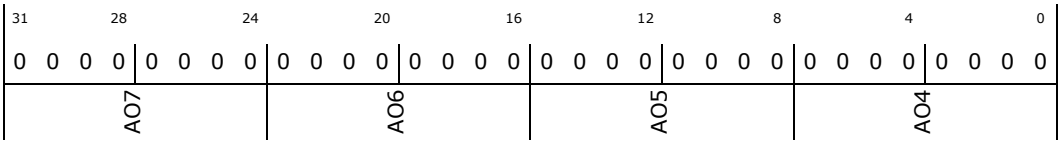
Opcode_Menu_Configuration_1_bios: [SPI_BASE_ADDRESS] + 9Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RW/L	**Allowable Opcode 7 (AO7):** See the description for bits 7:0 in OPMENU0
23:16	00h RW/L	**Allowable Opcode 6 (AO6):** See the description for bits 7:0 in OPMENU0
15:8	00h RW/L	**Allowable Opcode 5 (AO5):** See the description for bits 7:0 in OPMENU0
7:0	00h RW/L	**Allowable Opcode 4 (AO4):** See the description for bits 7:0 in OPMENU0

3.58.37 LOCK (Individual_Lock_Register)—Offset A4h

Used to individually lock each one of the registers formally locked only by FLOCKDN bit. This register doesn't exclude FLOCKDN. It adds an individual option to lock each register in above to FLOCKDN.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

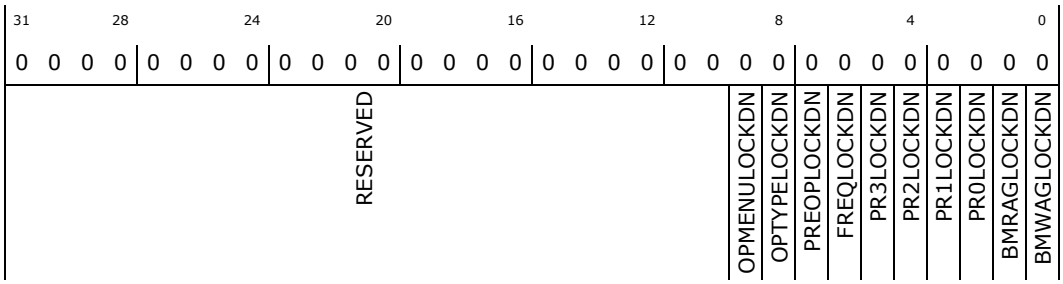
Individual_Lock_Register: [SPI_BASE_ADDRESS] + A4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0000000000000000000000b RO	**RESERVED:** reserved, should be with default 0
9	0b RW/L	**OPMENU Lock-Down (OPMENULOCKDN):** When set to 1, OPMENU0 and OPMENU1 registers cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
8	0b RW/L	**OPTYPE Lock-Down (OPTYPELOCKDN):** When set to 1, OPTYPE register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
7	0b RW/L	**PREOP Lock-Down (PREOPLOCKDN):** When set to 1, PREOP register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
6	0b RW/L	**SCF Lock-Down (FREQLOCKDN):** When set to 1, SCF field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
5	0b RW/L	**PR3 Lock-Down (PR3LOCKDN):** When set to 1, PR3 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
4	0b RW/L	**PR2 Lock-Down (PR2LOCKDN):** When set to 1, PR2 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
3	0b RW/L	**PR1 Lock-Down (PR1LOCKDN):** When set to 1, PR1 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
2	0b RW/L	**PR0 Lock-Down (PR0LOCKDN):** When set to 1, PR0 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.

Bit Range	Default & Access	Description
1	0b RW/L	**BMRAG Lock-Down (BMRAGLOCKDN):** When set to 1, BMRAG field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
0	0b RW/L	**BMWAG Lock-Down (BMWAGLOCKDN):** When set to 1, BMWAG field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.

3.58.38 FDOC (Flash_Descriptor_Observability_Control_bios)—Offset B0h

Flash Descriptor Observability Control. This is a test mode only register that can be used to observe the contents of the Flash Descriptor that is stored internally in the SPI Controller.

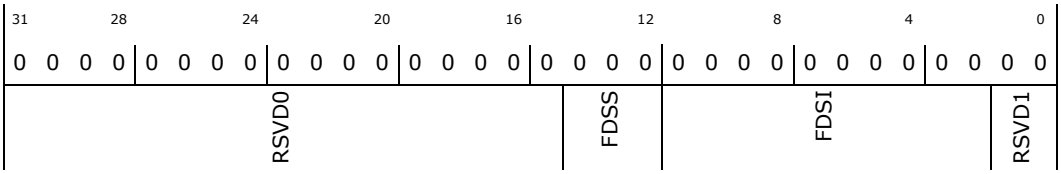
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Descriptor_Observability_Control_bios: [SPI_BASE_ADDRESS] + B0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0b RO	**RSVD0:** Reserved
14:12	000b RW	**Flash Descriptor Section Select (FDSS):** Selects which section within the loaded Flash Descriptor to observe. 000 : Flash Signature and Descriptor Map 001 : Component 010 : Region 011 : Master 100 : Soft Straps 111 : Reserved
11:2	000h RW	**Flash Descriptor Section Index (FDSI):** Selects the DW offset within the Flash Descriptor Section to observe.
1:0	0b RO	**RSVD1:** Reserved

3.58.39 FDOD (Flash_Descriptor_Observability_Data_bios)—Offset B4h

Flash descriptor observability data

Access Method

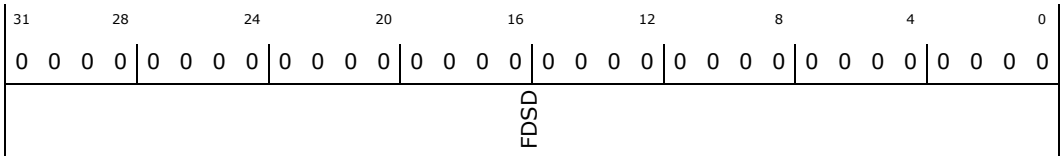
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Descriptor_Observability_Data_bios: [SPI_BASE_ADDRESS] + B4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Flash Descriptor Section Data (FDSD):** Contains the DW of data to observe as selected in the Flash Descriptor Observability Control. at default the FDSS==3'b000 hence this register contains the data of Flash Signature and Descriptor Map.

3.58.40 AFC (Additional_Flash_Control_bios)—Offset C0h

Additional flash control

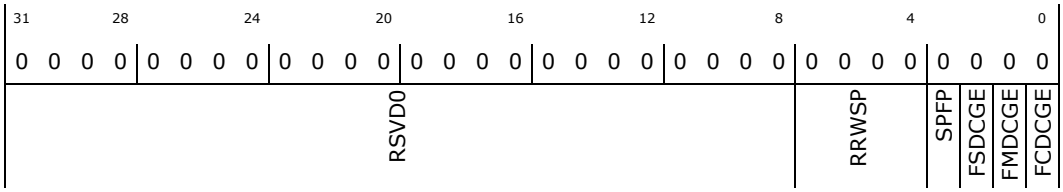
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Additional_Flash_Control_bios: [SPI_BASE_ADDRESS] + C0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:4	0000b RW	**Reserved RW Scratch Pad (RRWSP):** Scratch Pad bits that are R/W to be used during ECO
3	0b RW	**Stop Prefetch on Flush Pending (SPFP):** When set to 1'b1, the in progress of a prefetch will be ended if subsequence access from the same master is detected to be a cache-miss and read cache will be flushed. When set to 1'b0, the prefetch will be allowed to complete prior to flushing.

Bit Range	Default & Access	Description
2	0b RW	**Flash IOSF PRI Dynamic Clock Gating Enable (FSDCGE):** When set to 1'b1, the SPI controller IOSF-PRI interface logic can be dynamically clock gated. This register is only clear on a reset.
1	0b RW	**Flash IOSF SB Dynamic Clock Gating Enable (FMDCGE):** When set to 1'b1, the SPI controller IOSF-SB interface logic can be dynamically clock gated. This register is only clear on a reset.
0	0b RW	**Flash Core Dynamic Clock Gating Enable (FCDCGE):** When set to 1'b1, the SPI controller core logic can be dynamically clock gated. This register is only clear on a reset.

3.58.41 LVSCC (Lower_Vendor_Specific_Component_Capabilities_bios)—Offset C4h

Lower vendor specific component capabilities

Access Method

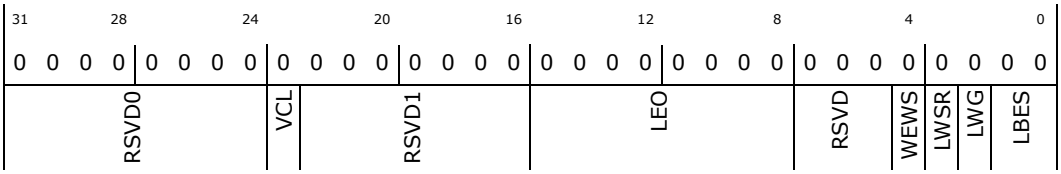
Type: Memory Mapped I/O Register (Size: 32 bits)

Lower_Vendor_Specific_Component_Capabilities_bios: [SPI_BASE_ADDRESS] + C4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved
23	0b RW/L	**Vendor Component Lock (VCL):** '0': The lock bit is not set '1': The Vendor Component Lock bit is set. This register locks itself when set. If this register is not set and the Flash is operating in Flash Mode (as opposed to EEPROM mode), then software cannot use hardware sequencing. This requirement is not enforced by hardware, but is a requirement of the the power-on usage model.
22:16	0b RO	**RSVD1:** Reserved
15:8	00h RW/L	**Lower Erase Opcode (LEO):** This register is programed with the Flash erase instruction opcode required by this vendors Flash component. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address.

Bit Range	Default & Access	Description
7:5	000b RW/L	**Reserved RW/L Scratch Pad (RSVD):** Keep RW/L for future Flash Component Specific capabilities. This register is locked by the Vendor Component Lock (VCL) bit.
4	0b RW/L	**Write Enable on Write Status (WEWS):** '0' : No Write Enable command is required to write to the Write Status register '1' : Write Enable command is required to write to the Write Status register Must be set to 1'b1 for Intel's Blanshard Flash Component and for Atmel
3	0b RW/L	**Lower Write Status Required (LWSR):** '0' : No requirement to to write to the Write Status Register prior to a write '1' : A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address.
2	0b RW/L	**Lower Write Granularity (LWG):** '0' : 1 Byte '1' : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address.
1:0	00b RW/L	**Lower Block/Sector Erase Size (LBES):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte This register is locked by the Vendor Component Lock (VCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers. This field is used for cycles targeting addresses below the Flash Partition Address.

3.58.42 UVSCC (Upper_Vendor_Specific_Component_Capabilities_bios)—Offset C8h

Upper vendor specific component capabilities

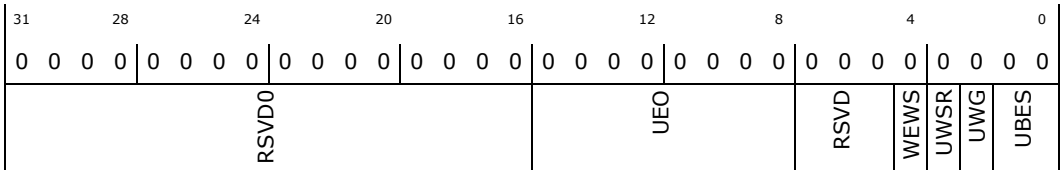
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Upper_Vendor_Specific_Component_Capabilities_bios: [SPI_BASE_ADDRESS] + C8h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RW/L	**Upper Erase Opcode (UEO):** This register is programed with the Flash erase instruction opcode required by this vendors Flash component. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address.
7:5	0h RW/L	**Reserved RW/L Scratch Pad (RSVD):** Keep RW/L for future Flash Component Specific capabilities. This register is locked by the Vendor Component Lock (VCL) bit.
4	0b RW/L	**Write Enable on Write Status (WEWS):** '0' : No Write Enable command is required to write to the Write Status register '1' : Write Enable command is required to write to the Write Status register Must be set to 1'b1 for Intel's Blanshard Flash Component and for Atmel
3	0b RW/L	**Upper Write Status Required (UWSR):** '0': No requirement to to write to the Write Status Register prior to a write '1': A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address.
2	0b RW/L	**Upper Write Granularity (UWG):** '0' : 1 Byte '1' : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address.
1:0	00b RW/L	**Upper Block/Sector Erase Size (UBES):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte Note: If supporting more than one Flash component, all flash components must have identical Block/ Sector erase sizes. This register is locked by the Vendor Component Lock (VCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GBE program registers. This field is used for cycles targeting addresses above the Flash Partition Address.

3.58.43 FPB (Flash_Partition_Boundary_bios)—Offset D0h

Flash partition boundary

Access Method

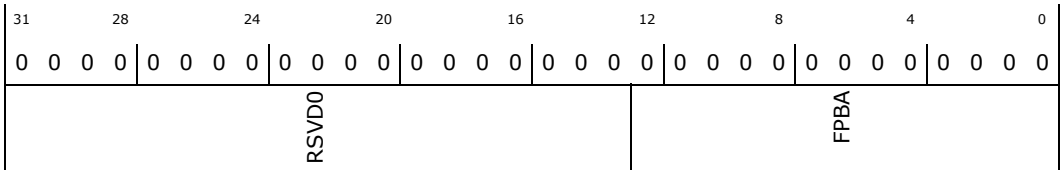
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Partition_Boundary_bios: [SPI_BASE_ADDRESS] + D0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:13	0b RO	**RSVD0:** Reserved
12:0	0000h RO/U	**Flash Partition Boundary Address (FPBA):** This register reflects the value of the Flash Descriptor Component FPBA field

3.58.44 SCS (SMI_Control_Status_Register_bios)—Offset F8h

SMI Control and Status

Access Method

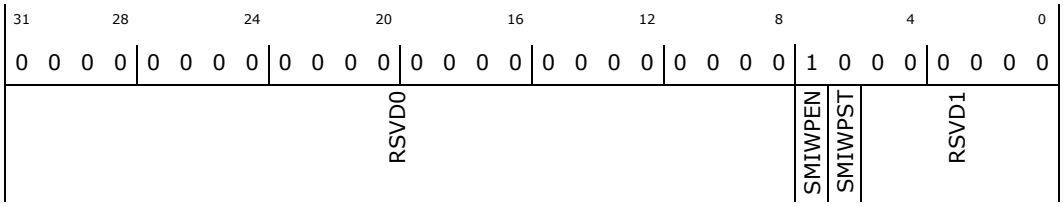
Type: Memory Mapped I/O Register (Size: 32 bits)

SMI_Control_Status_Register_bios: [SPI_BASE_ADDRESS] + F8h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000080h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	1b RW	**SMI WPD Enable (SMIWPEN):** When this bit is set to a 1'b1, it enables the SPI controller to generate SMI upon not SMM code is trying to set WPD from a 1'b0 to a 1'b1 while LE is set.
6	0b RW/1C	**SMI WPD Status (SMIWPST):** Set when SMI is generated upon trying to set WPD from a 1'b0 to a 1'b1 by not SMM code (while LE and SMIWPEN are set). Write a 1'b1 to this bit should clear it and clear the SMI (send DEASSERT_SMI)
5:0	0b RO	**RSVD1:** Reserved

3.58.45 BCR (BIOS_Control_Register_bios)—Offset FCh

BIOS control register. This register formerly was in the 0:31:0 config space

Access Method

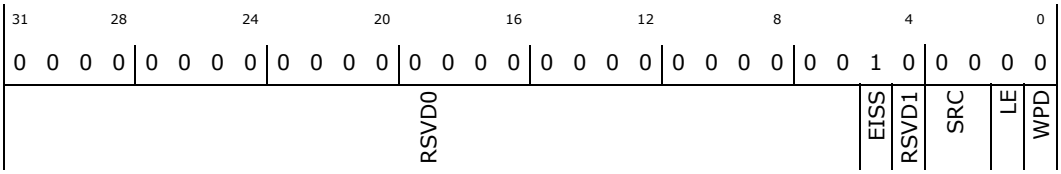
Type: Memory Mapped I/O Register (Size: 32 bits)

BIOS_Control_Register_bios: [SPI_BASE_ADDRESS] + FCh

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000020h



Bit Range	Default & Access	Description
31:6	0b RO	**RSVD0:** Reserved
5	1b RW/L	**Enable InSMM_STS (EISS):** When this bit is set, the BIOS region is writable only to SMM code. Today BIOS Flash is writable if WPD is a '1'. If this bit [lb]5[rb] is set, then WPD must be a 1'b1 and iosfep_xxx_hprot[lb]1[rb] signal be 1'b1 also. If this bit [lb]5[rb] is clear, then BIOS is writable based only on WPD = 1'b1 and the iosfep_xxx_hprot[lb]1[rb] signal is a don't care.
4	0b RO	**RSVD1:** Reserved
3:2	00b RW	**SPI Read Configuration (SRC):** This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3 - Prefetch Enable, Bit 2 - Cache Disable. Settings are summarized below: '00' : No prefetching, but caching enabled. Direct Memory reads load the read buffer cache with 'valid' data, allowing repeated reads to the same range to complete quickly. '01' : No prefetching and no caching. One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. '10' : Prefetching and Caching enabled. This mode is used for long sequences of short reads to consecutive addresses (i.e. shadowing) '11' : Illegal. Caching must be enabled when Prefetching is enabled. This eliminates the need for a complex prefetch-flushing mechanism. Note that if BIOS direct read caching is disabled while data has already been cached internally, subsequent BIOS direct reads will continue to return data from the cache until the cache is invalidated.
1	0b RW/L	**Lock Enable (LE):** When set, WPD bit could be set from a 1'b0 to a 1'b1 only by SMM code. When cleared, setting the WP bit is allowed in all modes and SMI is not generated. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [lb]5[rb] of this register is locked down.
0	0b RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles. When cleared, only read cycles are permitted to the flash. When LE bit is set this bit could be written from a 1'b0 to a 1'b1 only by SMM code. When not SMM code tries to writes this bit from a 1'b0 to a 1'b1, bit remain in its 1'b0 value. An Async-SMI is generated (Send ASSERT_SMI) if SMIWPEN is set. This ensures that only SMM code can update BIOS.

3.58.46 TCGC (Trunk_Clock_Gating_Control_bios)—Offset 100h

Trunk_Clock_Gating_Control

Access Method

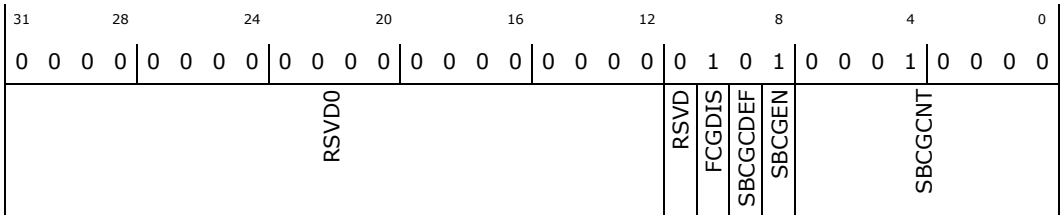
Type: Memory Mapped I/O Register (Size: 32 bits)

Trunk_Clock_Gating_Control_bios: [SPI_BASE_ADDRESS] + 100h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000510h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RO	**Reserved (RSVD):** Reserved.
10	1b RW	**FCGDIS:** Functional clock gating disable, chicken bit for the func_clk_gating FSM
9	0b RW	**SBCGCDEF:** SideBanb Control Gating Clock Defeature .Clock gate defeature bit which allows the ISM to transition to idle, but prevents the final clock masking from occurring. The value of this bit goes to the 'cgctrl_clkgatedef' port of the SideBand EndPoint
8	1b RW	**SBCGEN:** SideBanb Control Gating Clock Enable. Clock gate enable which prevents ISM from leaving ACTIVE. Also prevents the clocks from being gated. The value of this bit goes to the 'cgctrl_clkgaten' port of the SideBand EndPoint
7:0	10h RW	**SBCGCNT:** SideBanb Control Gating Clock Counter. Idle count limit for ISM which is used to determine the block is idle.Recommended value 8'd16 . The value of those bits goes to the 'cgctrl_idlecnt' ports of the SideBand EndPoint

3.59 PCU iLB UART IO Registers

Table 67. Summary of PCU iLB UART I/O Registers—

Offset	Size	Register ID—Description	Default Value
3F8h	1	"Receiver Buffer / Transmitter Holding Register (COM1_Rx_Tx_Buffer)—Offset 3F8h" on page 3139	00h
3F9h	1	"Interrupt Enable Register (COM1_IER)—Offset 3F9h" on page 3140	00h
3FAh	1	"Interrupt Identification / FIFO Control Register (COM1_IIR)—Offset 3FAh" on page 3141	01h
3FBh	1	"Line Control Register (COM1_LCR)—Offset 3FBh" on page 3142	00h
3FCh	1	"Modem Control Register (COM1_MCR)—Offset 3FCh" on page 3143	00h
3FDh	1	"Line Status Register (COM1_LSR)—Offset 3FDh" on page 3145	60h
3FEh	1	"Modem Status Register (COM1_MSR)—Offset 3FEh" on page 3147	00h
3FFh	1	"Scratchpad Register (COM1_SCR)—Offset 3FFh" on page 3149	00h

3.59.1 Receiver Buffer / Transmitter Holding Register (COM1_Rx_Tx_Buffer)—Offset 3F8h

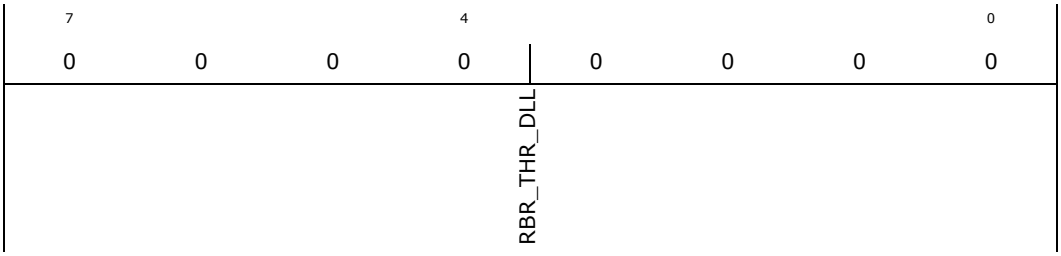
This register is a combination of three registers: the receiver buffer register (RBR) that is a read-only register when DLAB=0, the transmitter holding register (THR) that is a write-only register when DLAB=0 and the divisor latch LSB (DLL) register when DLAB=1.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_Rx_Tx_Buffer: 3F8h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Receiver buffer / transmitter holding (RBR_THR_DLL): When reading from this register and DLAB=1'b0**, it contains the byte received if no FIFO is used, or the oldest unread byte with FIFO's. If FIFO buffering is used, each new read action of the register will return the next byte, until no more bytes are present. Bit 0 in the LSR line status register can be used to check if all received bytes have been read. This bit will change to zero if no more bytes are present. **When writing to this register and DLAB=1'b0**, it is used to buffer outgoing characters. If no FIFO buffering is used, only one character can be stored. Otherwise the amount of characters depends on the type of UART. Bit 5 in the LSR, line status register can be used to check if new information must be written to this register. The value 1'b1 indicates that the register is empty. If FIFO buffering is used, more than one character can be written to the transmitter holding register when the bit signals an empty state. There is no indication of the amount of bytes currently present in the transmitter FIFO. This register is not used to transfer the data directly. The byte is first transferred to a shift register where the information is broken in single bits which are sent one by one. **If DLAB=1'b1**, this register is used as DLL (Divisor Latch LSB). For generating its timing information, each UART uses an oscillator generating a frequency of about 1.8432 MHz. This frequency is divided by 16 to generate the time base for communication. Because of this division, the maximum allowed communication speed is 115200 bps. Modern UARTS like the 16550 are capable of handling higher input frequencies up to 24 MHz which makes it possible to communicate with a maximum speed of 1.5 Mbps. On PC's higher frequencies than the 1.8432 MHz are rarely seen because this would be software incompatible with the original XT configuration. This 115200 bps communication speed is not suitable for all applications. To change the communication speed, the frequency can be further decreased by dividing it by a programmable value. For very slow communications, this value can go beyond 255. Therefore, the divisor is stored in two separate bytes, the divisor latch registers DLL and DLM which contain the least, and most significant byte. For error free communication, it is necessary that both the transmitting and receiving UART use the same time base. Default values have been defined which are commonly used. The table shows the most common values with the appropriate settings of the divisor latch bytes. Note that these values only hold for a PC compatible system where a clock frequency of 1.8432 MHz is used. Speed(bps) Divisor DLL DLM 50 2,304 0x00 0x09 300 384 0x80 0x01 1,200 96 0x60 0x00 2,400 48 0x30 0x00 4,800 24 0x18 0x00 9,600 12 0x0C 0x00 19,200 6 0x06 0x00 38,400 3 0x03 0x00 57,600 2 0x02 0x00 115,200 1 0x01 0x00

3.59.2 Interrupt Enable Register (COM1_IER)—Offset 3F9h

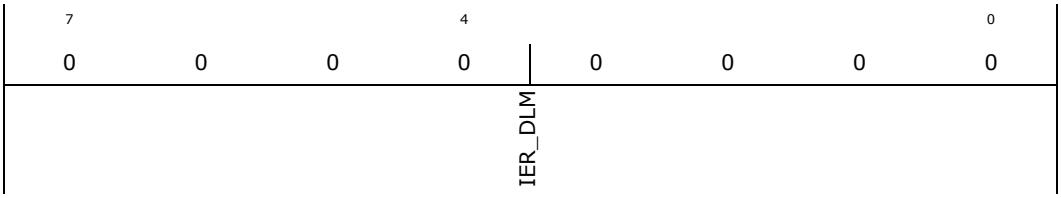
This register is a combination of two registers: the interrupt enable register (IER) when DLAB=0 and the divisor latch MSB (DLM) register when DLAB=1.

Access Method

Type: I/O Register (Size: 8 bits)

COM1_IER: 3F9h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Interrupt Enable (IER_DLM): If DLAB=1'b0**, This field is used as interrupt enable register. The smartest way to perform serial communications on a PC is using interrupt driven routines. In that configuration, it is not necessary to poll the registers of the UART periodically for state changes. The UART will signal each change by generating a processor interrupt. A software routine must be present to handle the interrupt and to check what state change was responsible for it. Interrupts are not generated, unless the UART is told to do so. This is done by setting bits in the IER, interrupt enable register. A bit value 1 indicates, that an interrupt may take place. Bit Description 0 ERBFI - Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 1 ETBEI - Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 2 ELSI - Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 3 EDSSI - Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 4 Reserved and read as zero 5 Reserved and read as zero 6 Reserved and read as zero 7 PTIME - Programmable THRE Interrupt Mode Enable that can be written to only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. **If DLAB=1'b1**, this register is used as DLM (Divisor Latch MSB). See DLL field description in the Rx_Tx_Buffer register.

3.59.3 Interrupt Identification / FIFO Control Register (COM1_IIR)—Offset 3FAh

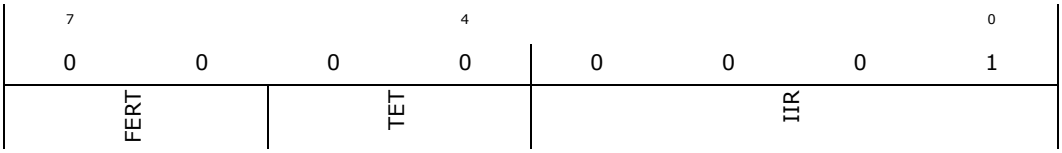
This register is a combination of two registers: the interrupt identification register (IIR) that is a read-only register and the FIFO control register (FCR) that is a write-only register. If FIFOs are not implemented, the FIFO control register does not exist and writing to this register address has no effect.

Access Method

Type: I/O Register (Size: 8 bits)

COM1_IIR: 3FAh

Default: 01h



Bit Range	Default & Access	Description
7:6	00b RO	**FIFOs Enabled / RCVR Trigger (FERT): Read** from this field is used to indicate whether the FIFOs are enabled or disabled. '00' - disabled '11' - enabled **Write** to this field is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. The following trigger levels are supported: '00' - 1 character in the FIFO '01' - FIFO 1/4 full '10' - FIFO 1/2 full '11' - FIFO 2 less than full
5:4	00b RO	**TX Empty Trigger (TET): Read** from this field is reserved and should return zero **Write** to this field is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: '00' - FIFO empty '01' - 2 characters in the FIFO '10' - FIFO 1/4 full '11' - FIFO 1/2 full
3:0	0001b RO	**Interrupt ID (IIR): Read** from this field indicates the highest priority pending interrupt which can be one of the following types: '0000' - modem status '0001' - no interrupt pending '0010' - THR empty '0100' - received data available '0110' - receiver line status '0111' - busy detect '1100' - character timeout **Write** to this field is split to four bits: Bit Description 3 DMA Mode, determines the DMA signalling mode used: '0'- mode 0, '1' - mode 1 2 XMIT FIFO Reset, resets the control portion of the transmit FIFO and treats the FIFO as empty. 1 RCVR FIFO Reset, resets the control portion of the receive FIFO and treats the FIFO as empty. 0 FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

3.59.4 Line Control Register (COM1_LCR)—Offset 3FBh

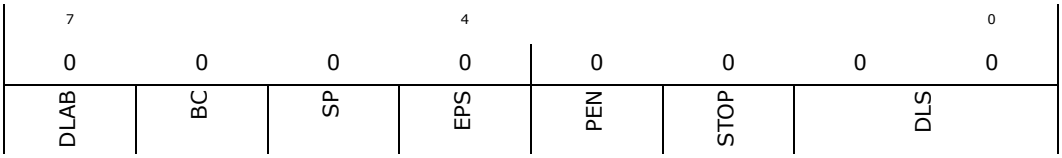
The LCR, line control register is used at initialization to set the communication parameters. Parity and number of data bits can be changed for example. The register also controls the accessibility of the DLL and DLM registers. These registers are mapped to the same I/O port as the RBR, THR and IER registers. Because they are only accessed at initialization when no communication occurs this register swapping has no influence on performance.

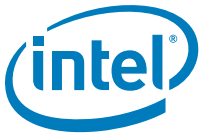
Access Method

Type: I/O Register
(Size: 8 bits)

COM1_LCR: 3FBh

Default: 00h





Bit Range	Default & Access	Description
7	0b RW	**Divisor Latch Access Bit (DLAB):** This field is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. '0' - RBR, THR and IER accessible '1' - DLL and DLM accessible See Rx_Tx_Buffer and IER registers description for more details.
6	0b RW	**Break Control (BC):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0b RO	**Stick Parity (SP):** Reserved and read as zero
4	0b RW	**Even Parity Select (EPS):** This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.
3	0b RW	**Parity Enable (PEN):** This is used to enable and disable parity generation and detection in transmitted and received serial character respectively. '0' - parity disabled '1' - parity enabled
2	0b RW	**Number ofStop bits (STOP):** This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. '0' - 1 stop bit '1' - 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	00b RW	**Data Length Select (DLS):** This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: '00' - 5 bits '01' - 6 bits '10' - 7 bits '11' - 8 bits

3.59.5 Modem Control Register (COM1_MCR)—Offset 3FCh

The MCR, modem control register is used to perform handshaking actions with the attached device. In the original UART series including the 16550, setting and resetting of the control signals must be done by software. The new 16750 is capable of handling flow control automatically, thereby reducing the load on the processor.

Access Method

Type: I/O Register (Size: 8 bits)

COM1_MCR: 3FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD0	SIRE	AFCE	LB	OUT2	OUT1	RTS	DTR

Bit Range	Default & Access	Description
7	0b RO	**RSVD0:** Reserved
6	0b RW	**SIR Mode Enable (SIRE):** Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/disable the IrDA SIR Mode features as described in 'IrDA 1.0 SIR Protocol' on Synopsys UART specification. '0' - IrDA SIR Mode disabled '1' - IrDA SIR Mode enabled
5	0b RW	**Auto Flow Control Enable (AFCE):** Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in 'Auto Flow Control' on Synopsys UART specification. '0' - Auto Flow Control Mode disabled '1' - Auto Flow Control Mode enabled
4	0b RW	**LoopBack (LB):** This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0b RW	**Auxiliary output 2 (OUT2):** This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: '0' - out2_n de-asserted (logic 1) '1' - out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	0b RW	**Auxiliary output 1 (OUT1):** This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: '0' - out1_n de-asserted (logic 1) '1' - out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.

Bit Range	Default & Access	Description
1	0b RW	**Request to Send (RTS):** This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Note that PCU-UART does not implement the Request to Send (rts_n) output.
0	0b RW	**Data Terminal Ready (DTR):** This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: '0' - dtr_n de-asserted (logic 1) '1' - dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Note that PCU-UART does not implement the Data Terminal Ready (dtr_n) output.

3.59.6 Line Status Register (COM1_LSR)—Offset 3FDh

The LSR, line status register shows the current state of communication. Errors are reflected in this register. The state of the receive and transmit buffers is also available.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_LSR: 3FDh

Default: 60h

7			4				0
0	1	1	0	0	0	0	0
RFE	TEMT	THRE	BI	FE	PE	OE	DR

Bit Range	Default & Access	Description
7	0b RO	**Receiver FIFO Error (RFE):** This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. '0' - no error in RX FIFO '1' - error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.

Bit Range	Default & Access	Description
6	1b RO	**Transmitter Empty (TEMT):** If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1b RO	**Transmit Holding Register Empty (THRE):** If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0b RO	**Break Interrupt (BI):** This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	0b RO	**Framing Error (FE):** This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). '0' - no framing error '1' - framing error Reading the LSR clears the FE bit.
2	0b RO	**Parity Error (PE):** This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). '0' - no parity error '1' - parity error Reading the LSR clears the PE bit.

Bit Range	Default & Access	Description
1	0b RO	**Overrun Error (OE):** This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. '0' - no overrun error '1' - overrun error Reading the LSR clears the OE bit.
0	0b RO	**Data Ready (DR):** This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. '0' - no data ready '1' - data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

3.59.7 Modem Status Register (COM1_MSR)—Offset 3FEh

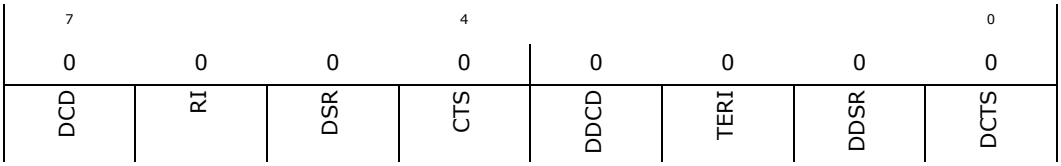
The MSR, modem status register contains information about the four incoming modem control lines on the device. The information is split in two nibbles. The four most significant bits contain information about the current state of the inputs where the least significant bits are used to indicate state changes. The four LSB's are reset, each time the register is read. Whenever bits 0, 1, 2 or 3 are set to logic one, to indicate a change on the modem control inputs, a modem status interrupt is generated if enabled through the IER, regardless of when the change occurred. Since the delta bits (bits 0, 1, 3) can get set after a reset if their respective modem signals are active (see individual bits for details), a read of the MSR after reset can be performed to prevent unwanted interrupts.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_MSR: 3FEh

Default: 00h



Bit Range	Default & Access	Description
7	0b RO	**Data Carrier Detect (DCD):** This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. '0' - dcd_n input is de-asserted (logic 1) '1' - dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Note that PCU-UART does not implement the Data Carrier Detect (dcd_n) input.

Bit Range	Default & Access	Description
6	0b RO	**Ring Indicator (RI):** This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. '0' - ri_n input is de-asserted (logic 1) '1' - ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Note that PCU-UART does not implement the Ring Indicator (ri_n) input.
5	0b RO	**Data Set Ready (DSR):** This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. '0' - dsr_n input is de-asserted (logic 1) '1' - dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Note that PCU-UART does not implement the Data Set Ready (dsr_n) input.
4	0b RO	**Clear to Send (CTS):** This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. '0' - cts_n input is de-asserted (logic 1) '1' - cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). Note that PCU-UART does not implement the Clear to Send (cts_n) input.
3	0b RO	**Delta Data Carrier Detect (DDCD):** This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. '0' - no change on dcd_n since last read of MSR '1' - change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. Note that PCU-UART does not implement the Data Carrier Detect (dcd_n) input.
2	0b RO	**Trailing Edge of Ring Indicator (TERI):** This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. '0' - no change on ri_n since last read of MSR '1' - change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Note that PCU-UART does not implement the Ring Indicator (ri_n) input.
1	0b RO	**Delta Data Set Ready (DDSR):** This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. '0' - no change on dsr_n since last read of MSR '1' - change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. Note that PCU-UART does not implement the Data Set Ready (dsr_n) input.

Bit Range	Default & Access	Description
0	0b RO	**Delta Clear to Send (DCTS):** This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. '0' - no change on cts_n since last read of MSR '1' - change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. Note that PCU-UART does not implement the Clear to Send (cts_n) input.

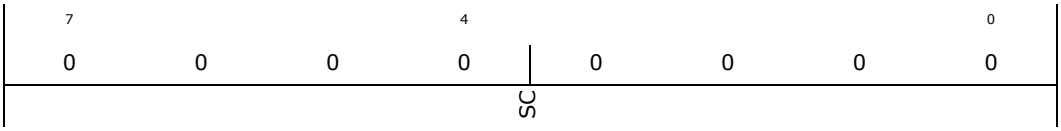
3.59.8 Scratchpad Register (COM1_SCR)—Offset 3FFh

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_SCR: 3FFh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Scratchpad (SC):** This register is for programmers to use as a temporary storage space.

3.60 PCU iLB Interrupt Decode and Route

Table 68. Summary of PCU iLB Interrupt Decode and Route Memory Mapped I/O Registers—ILB_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"ACTL—Offset 0h" on page 3151	00000003h
4h	4	"MC—Offset 4h" on page 3152	00000000h
8h	1	"PIRQA—Offset 8h" on page 3153	80h
9h	1	"PIRQB—Offset 9h" on page 3153	80h
Ah	1	"PIRQC—Offset Ah" on page 3154	80h
Bh	1	"PIRQD—Offset Bh" on page 3155	80h
Ch	1	"PIRQE—Offset Ch" on page 3155	80h
Dh	1	"PIRQF—Offset Dh" on page 3156	80h
Eh	1	"PIRQG—Offset Eh" on page 3156	80h
Fh	1	"PIRQH—Offset Fh" on page 3157	80h
10h	4	"SCNT—Offset 10h" on page 3158	00000000h
14h	4	"KMC—Offset 14h" on page 3158	00000000h
18h	4	"FS—Offset 18h" on page 3159	00112233h
1Ch	4	"BC—Offset 1Ch" on page 3160	00000100h
20h	2	"IR0—Offset 20h" on page 3161	0000h
22h	2	"IR1—Offset 22h" on page 3162	0000h
24h	2	"IR2—Offset 24h" on page 3162	0000h
26h	2	"IR3—Offset 26h" on page 3163	0000h
28h	2	"IR4—Offset 28h" on page 3163	0000h
2Ah	2	"IR5—Offset 2Ah" on page 3164	0000h
2Ch	2	"IR6—Offset 2Ch" on page 3165	0000h
2Eh	2	"IR7—Offset 2Eh" on page 3165	0000h
30h	2	"IR8—Offset 30h" on page 3166	0000h
32h	2	"IR9—Offset 32h" on page 3166	0000h
34h	2	"IR10—Offset 34h" on page 3167	0000h
36h	2	"IR11—Offset 36h" on page 3167	0000h
38h	2	"IR12—Offset 38h" on page 3168	0000h
3Ah	2	"IR13—Offset 3Ah" on page 3169	0000h
3Ch	2	"IR14—Offset 3Ch" on page 3169	0000h
3Eh	2	"IR15—Offset 3Eh" on page 3170	0000h
40h	2	"IR16—Offset 40h" on page 3170	0000h
42h	2	"IR17—Offset 42h" on page 3171	0000h
44h	2	"IR18—Offset 44h" on page 3171	0000h

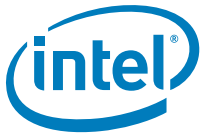


Table 68. Summary of PCU iLB Interrupt Decode and Route Memory Mapped I/O Registers—ILB_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
46h	2	"IR19—Offset 46h" on page 3172	0000h
48h	2	"IR20—Offset 48h" on page 3173	0000h
4Ah	2	"IR21—Offset 4Ah" on page 3173	0000h
4Ch	2	"IR22—Offset 4Ch" on page 3174	0000h
4Eh	2	"IR23—Offset 4Eh" on page 3174	0000h
50h	2	"IR24—Offset 50h" on page 3175	0000h
52h	2	"IR25—Offset 52h" on page 3175	0000h
54h	2	"IR26—Offset 54h" on page 3176	0000h
56h	2	"IR27—Offset 56h" on page 3177	0000h
58h	2	"IR28—Offset 58h" on page 3177	0000h
5Ah	2	"IR29—Offset 5Ah" on page 3178	0000h
5Ch	2	"IR30—Offset 5Ch" on page 3178	0000h
5Eh	2	"IR31—Offset 5Eh" on page 3179	0000h
60h	4	"OIC—Offset 60h" on page 3179	00001100h
64h	4	"RC—Offset 64h" on page 3180	00000000h
6Ch	4	"BCS - BIOS Control Status (BCS)—Offset 6Ch" on page 3181	00000002h
70h	4	"LE—Offset 70h" on page 3181	00000003h
80h	4	"NMI (GNMI)—Offset 80h" on page 3182	00000004h
84h	4	"LPCC—Offset 84h" on page 3183	00000001h
88h	4	"IRQEN (IRQE)—Offset 88h" on page 3184	00000000h

3.60.1 ACTL—Offset 0h

ACPI Control

Access Method

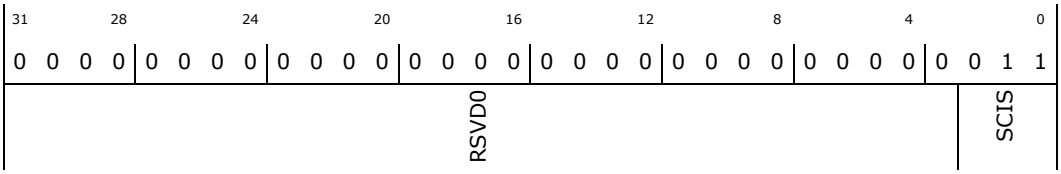
Type: Memory Mapped I/O Register (Size: 32 bits)

ACTL: [ILB_BASE_ADDRESS] + 0h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**RSVD0:** Reserved
2:0	011b RW	**SCIS:** SCI IRQ Select (SCIS): Specifies on which IRQ SCI will rout to. If not using APIC, SCI must be routed to IRQ9-11 , and that interrupt is not sharable with SERIRQ, but is shareable with other interrupts. If using APIC, SCI can be mapped to IRQ20-23, and can be shared with other interrupts. When the interrupt is mapped to APIC interrupts 9, 10 or 11, APIC must be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, APIC must be programmed for active-low reception.

3.60.2 MC—Offset 4h

Miscellaneous Control

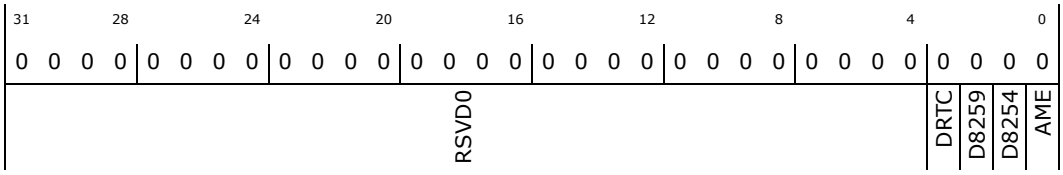
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MC: [ILB_BASE_ADDRESS] + 4h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0b RO	**RSVD0:** Reserved
3	0b RW	**DRTC:** Disable RTC (DRTC): When set, decodes to the RTC will be disabled, and the accesses instead will be sent to LPC. This allows testing to determine whether these functions are needed for XP and Vista 'EDS Note: Do not include this field in the EDS.
2	0b RW	**D8259:** Disable 8259 (D8259): When set, decodes to the 8259 will be disabled, and the accesses instead will be sent to LPC. This allows testing to determine whether these functions are needed for XP and Vista 'EDS Note: Do not include this field in the EDS.
1	0b RW	**D8254:** Disable 8254 (D8254): When set, decodes to the 8254 will be disabled, and the accesses instead will be sent to LPC. This allows testing to determine whether these functions are needed for XP and Vista 'EDS Note: Do not include this field in the EDS.

Bit Range	Default & Access	Description
0	0b RW	**AME:** Alt Access Mode is a mode that enables host reading some WO registers . 1. Read 8254 (legacy timers) indirect WO registers 2. Read 8259 (legacy interrupt controller) indirect WO registers 3. Read port 0x70 - port 0x70 includes the RTC memory address [6:0] and the NMI enable bit [7]

3.60.3 PIRQA—Offset 8h

PIRQA Routing Control

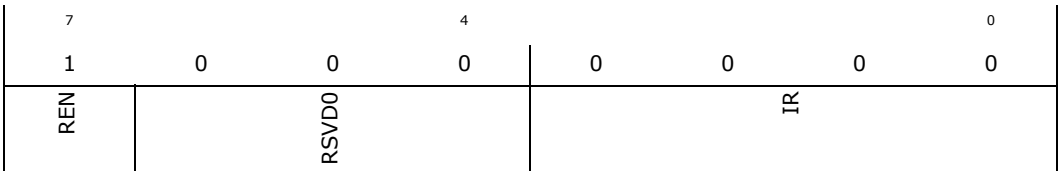
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQA: [ILB_BASE_ADDRESS] + 8h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h



Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

3.60.4 PIRQB—Offset 9h

PIRQB Routing Control

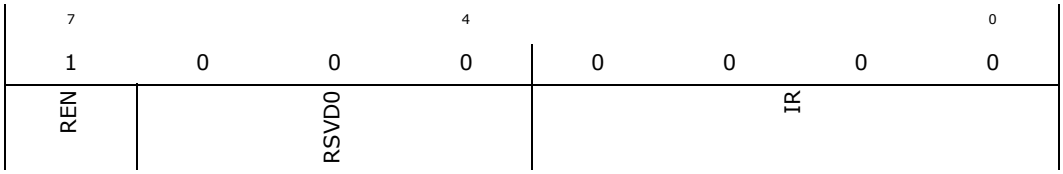
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQB: [ILB_BASE_ADDRESS] + 9h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h



Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

3.60.5 PIRQC—Offset Ah

PIRQC Routing Control

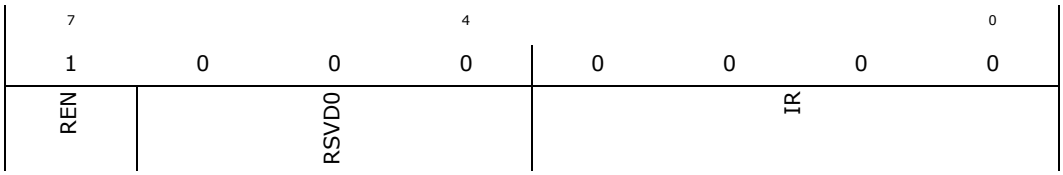
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQC: [ILB_BASE_ADDRESS] + Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h



Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

3.60.6 PIRQD—Offset Bh

PIRQD Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQD: [ILB_BASE_ADDRESS] + Bh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7				4				0
1	0	0	0	0	0	0	0	
REN	RSVD0			IR				

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

3.60.7 PIRQE—Offset Ch

PIRQE Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQE: [ILB_BASE_ADDRESS] + Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7				4				0
1	0	0	0	0	0	0	0	
REN	RSVD0			IR				

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

3.60.8 PIRQF—Offset Dh

PIRQF Routing Control

Access Method

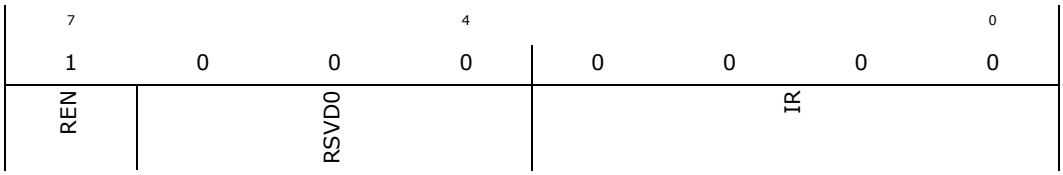
Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQF: [ILB_BASE_ADDRESS] + Dh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h



Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

3.60.9 PIRQG—Offset Eh

PIRQG Routing Control

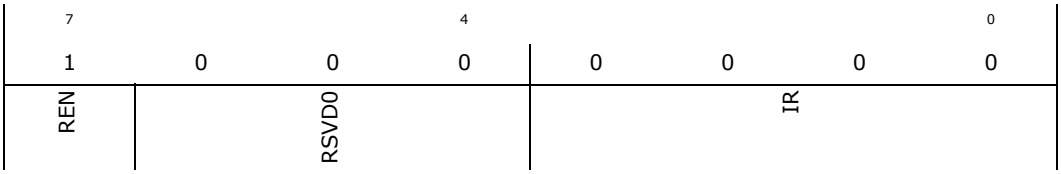
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQG: [ILB_BASE_ADDRESS] + Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h



Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

3.60.10 PIRQH—Offset Fh

PIRQH Routing Control

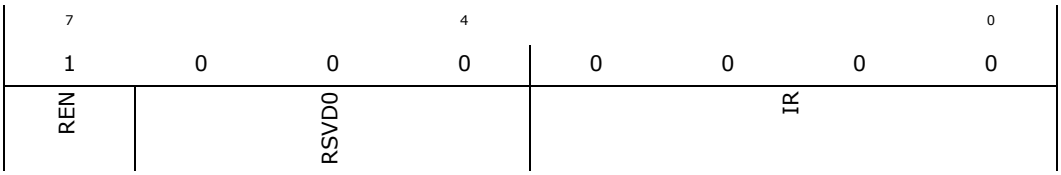
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQH: [ILB_BASE_ADDRESS] + Fh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h



Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

3.60.11 SCNT—Offset 10h

SCNT - Serial IRQ Control

Access Method

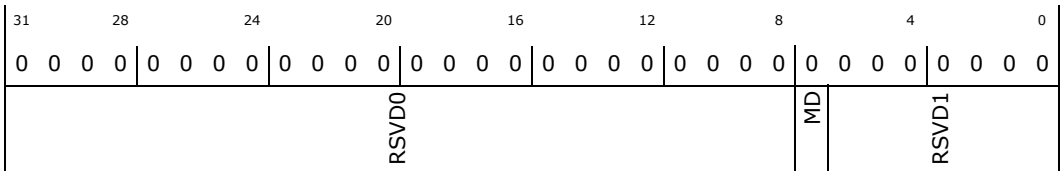
Type: Memory Mapped I/O Register (Size: 32 bits)

SCNT: [ILB_BASE_ADDRESS] + 10h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	0b RW	**MD:** Mode (MD): When set, the SERIRQ is in continuous mode. When cleared, SERIRQ is in quiet mode. This bit must be set to guarantee that the first action of SERIRQ is a start frame.
6:0	0b RO	**RSVD1:** Reserved

3.60.12 KMC—Offset 14h

USB Legacy Keyboard/Mouse Control

Access Method

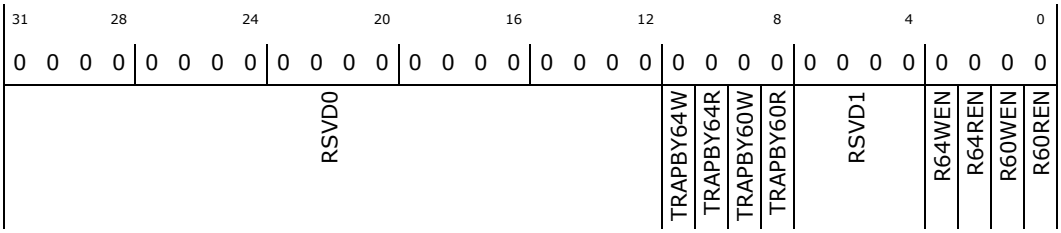
Type: Memory Mapped I/O Register (Size: 32 bits)

KMC: [ILB_BASE_ADDRESS] + 14h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RW/1C	**TRAPBY64W:** TRAPBY64W - SMI Caused by Port 64 Write: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
10	0b RW/1C	**TRAPBY64R:** TRAPBY64R - SMI Caused by Port 64 Read: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
9	0b RW/1C	**TRAPBY60W:** TRAPBY60W - SMI Caused by Port 60 Write: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
8	0b RW/1C	**TRAPBY60R:** TRAPBY60R - SMI Caused by Port 60 Read: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7:4	0b RO	**RSVD1:** Reserved
3	0b RW	**R64WEN:** R64WEN - SMI on Port 64 Writes Enable: When set, a 1 in bit 11 will cause an SMI event.
2	0b RW	**R64REN:** R64REN - SMI on Port 64 Reads Enable: When set, a 1 in bit 10 will cause an SMI event.
1	0b RW	**R60WEN:** R60WEN - SMI on Port 60 Writes Enable: When set, a 1 in bit 9 will cause an SMI event.
0	0b RW	**R60REN:** R60REN - SMI on Port 60 Reads Enable: When set, a 1 in bit 8 will cause an SMI event.

3.60.13 FS—Offset 18h

FS - FWH ID Select

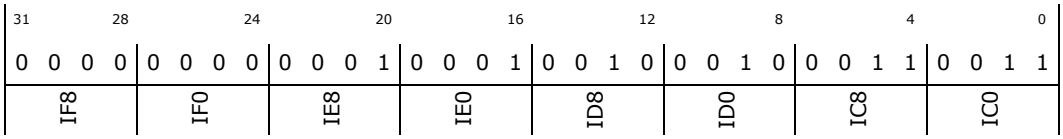
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FS: [ILB_BASE_ADDRESS] + 18h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00112233h



Bit Range	Default & Access	Description
31:28	0h RO	**IF8:** F8-FF IDSEL (IF8): IDSEL to use in FWH cycle for range enabled by BDE.EF8. The Address ranges are: FFF80000h - FFFFFFFFh, FFB80000h - FFBFFFFFh and 000E0000h - 000FFFFFh
27:24	0h RW	**IF0:** F0-F7 IDSEL (IF0): IDSEL to use in FWH cycle for range enabled by BDE.EF0. The Address ranges are: FFF00000h - FFF7FFFFh, FFB00000h - FFB7FFFFh
23:20	1h RW	**IE8:** E8-EF IDSEL (IE8): IDSEL to use in FWH cycle for range enabled by BDE.EE8. The Address ranges are: FFE80000h - FFEFFFFFh, FFA80000h - FFAFFFFFh
19:16	1h RW	**IE0:** E0-E7 IDSEL (IE0): IDSEL to use in FWH cycle for range enabled by BDE.EE0. The Address ranges are: FFE00000h - FFE7FFFFh, FFA00000h - FFA7FFFFh
15:12	2h RW	**ID8:** D8-DF IDSEL (ID8): IDSEL to use in FWH cycle for range enabled by BDE.ED8. The Address ranges are: FFD80000h - FFDFFFFFh, FF980000h - FF9FFFFFh
11:8	2h RW	**ID0:** D0-D7 IDSEL (ID0): IDSEL to use in FWH cycle for range enabled by BDE.ED0. The Address ranges are: FFD00000h - FFD7FFFFh, FF900000h - FF97FFFFh
7:4	3h RW	**IC8:** C8-CF IDSEL (IC8): IDSEL to use in FWH cycle for range enabled by BDE.EC8. The Address ranges are: FFC80000h - FFCFFFFFh, FF880000h - FF8FFFFFh
3:0	3h RW	**IC0:** C0-C7 IDSEL (IC0): IDSEL to use in FWH cycle for range enabled by BDE.EC0. The Address ranges are: FFC00000h - FFC7FFFFh, FF800000h - FF87FFFFh

3.60.14 BC—Offset 1Ch

BC - BIOS Control

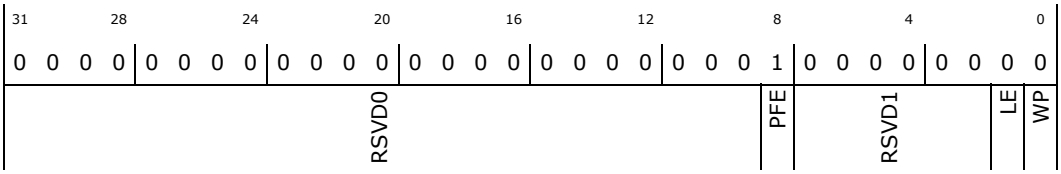
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BC: [ILB_BASE_ADDRESS] + 1Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000100h



Bit Range	Default & Access	Description
31:9	0b RO	**RSVD0:** Reserved
8	1b RW	**PFE:** Prefetch Enable (PFE): When set, BIOS prefetching is enabled. An access to BIOS causes a 64-byte fetch of the line starting at that region. Subsequent accesses within that region result in data being returned from the prefetch buffer. The prefetch buffer is invalidated when this bit is cleared, or a BIOS access occurs to a different line than what is currently in the buffer.
7:2	0b RO	**RSVD1:** Reserved
1	0b RW	**LE:** Lock Enable (LE): When set, setting the WP bit will cause SMIs. When cleared, setting the WP bit will not cause SMIs. Once set, this bit can only be cleared by a PMU_PLTRST_B#.
0	0b RW	**WP:** Write Protect (WP): When set, access to BIOS is enabled for both read and write cycles. When cleared, only read cycles are permitted to BIOS. When written from a 0 to a 1 and LE is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

3.60.15 IR0—Offset 20h

IR0 - Interrupt Routing Device 0

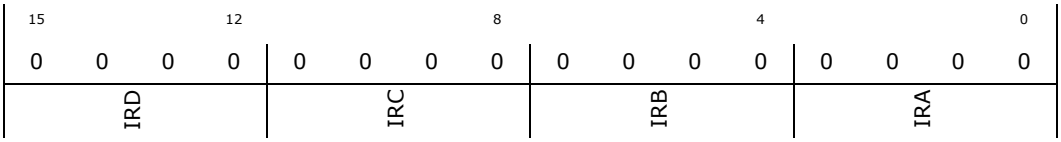
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR0: [ILB_BASE_ADDRESS] + 20h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.16 IR1—Offset 22h

IR1 - Interrupt Routing Device 1

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR1: [ILB_BASE_ADDRESS] + 22h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.17 IR2—Offset 24h

IR2 - Interrupt Routing Device 2

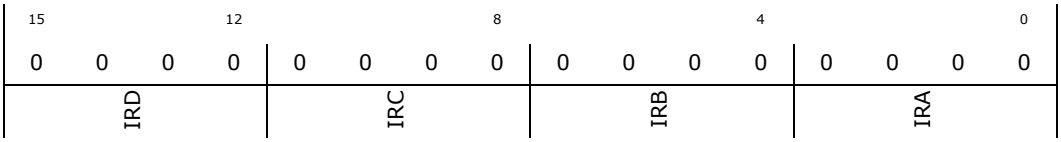
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR2: [ILB_BASE_ADDRESS] + 24h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.18 IR3—Offset 26h

IR3 - Interrupt Routing Device 3

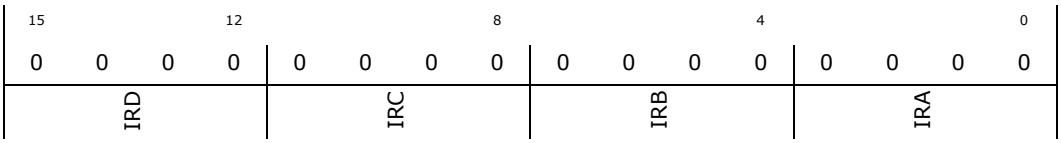
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR3: [ILB_BASE_ADDRESS] + 26h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.19 IR4—Offset 28h

IR4 - Interrupt Routing Device 4

Access Method

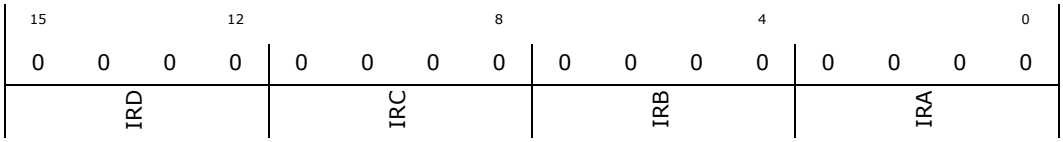
Type: Memory Mapped I/O Register (Size: 16 bits)

IR4: [ILB_BASE_ADDRESS] + 28h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.20 IR5—Offset 2Ah

IR5 - Interrupt Routing Device 5

Access Method

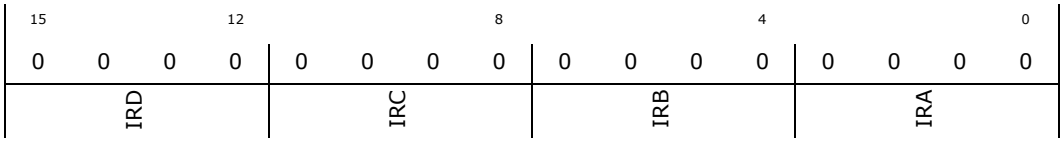
Type: Memory Mapped I/O Register (Size: 16 bits)

IR5: [ILB_BASE_ADDRESS] + 2Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.21 IR6—Offset 2Ch

IR6 - Interrupt Routing Device 6

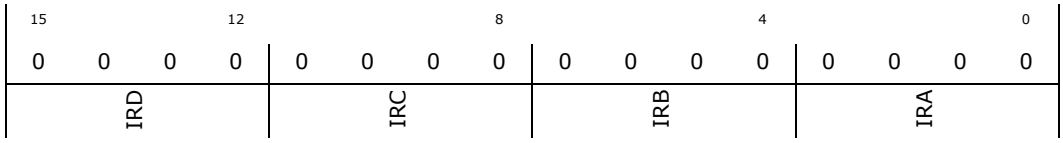
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR6: [ILB_BASE_ADDRESS] + 2Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.22 IR7—Offset 2Eh

IR7 - Interrupt Routing Device 7

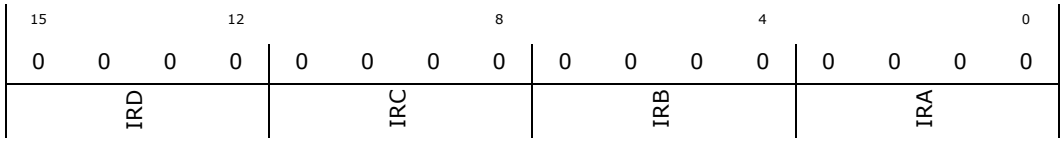
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR7: [ILB_BASE_ADDRESS] + 2Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H

Bit Range	Default & Access	Description
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.23 IR8—Offset 30h

IR8 - Interrupt Routing Device 8

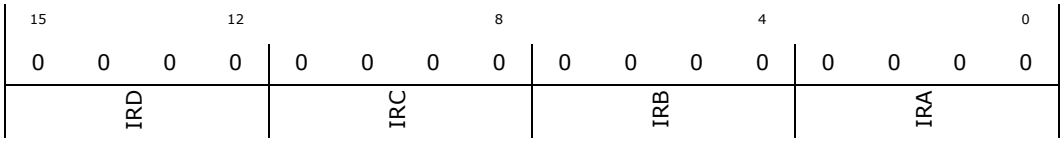
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR8: [ILB_BASE_ADDRESS] + 30h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.24 IR9—Offset 32h

IR9 - Interrupt Routing Device 9

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR9: [ILB_BASE_ADDRESS] + 32h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.25 IR10—Offset 34h

IR10 - Interrupt Routing Device 10

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR10: [ILB_BASE_ADDRESS] + 34h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.26 IR11—Offset 36h

IR11 - Interrupt Routing Device 11

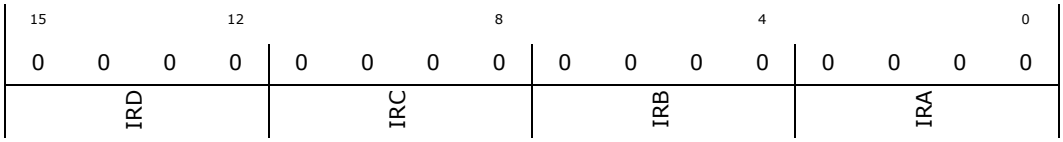
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR11: [ILB_BASE_ADDRESS] + 36h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.27 IR12—Offset 38h

IR12 - Interrupt Routing Device 12

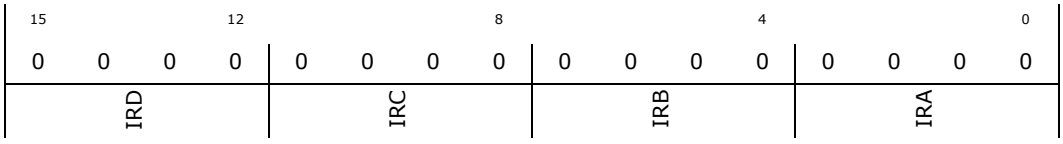
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR12: [ILB_BASE_ADDRESS] + 38h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.28 IR13—Offset 3Ah

IR13 - Interrupt Routing Device 13

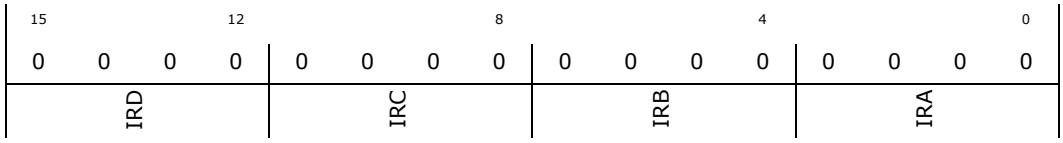
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR13: [ILB_BASE_ADDRESS] + 3Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.29 IR14—Offset 3Ch

IR14 - Interrupt Routing Device 14

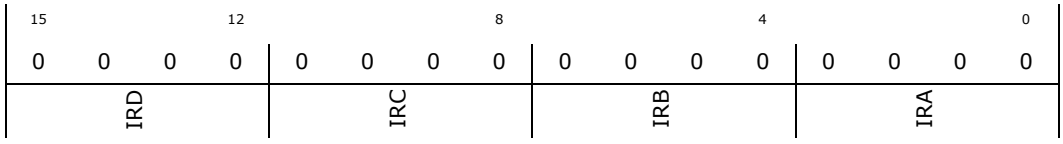
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR14: [ILB_BASE_ADDRESS] + 3Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H

Bit Range	Default & Access	Description
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.30 IR15—Offset 3Eh

IR15 - Interrupt Routing Device 15

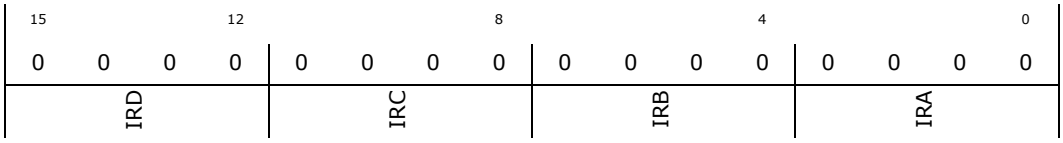
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR15: [ILB_BASE_ADDRESS] + 3Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.31 IR16—Offset 40h

IR16 - Interrupt Routing Device 16

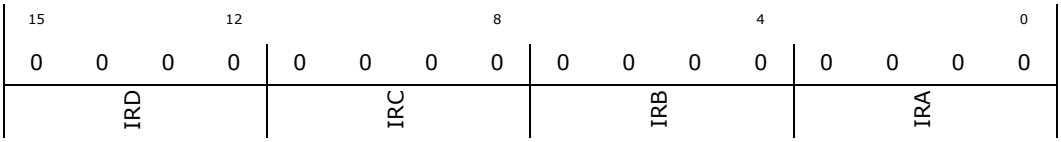
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR16: [ILB_BASE_ADDRESS] + 40h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.32 IR17—Offset 42h

IR17 - Interrupt Routing Device 17

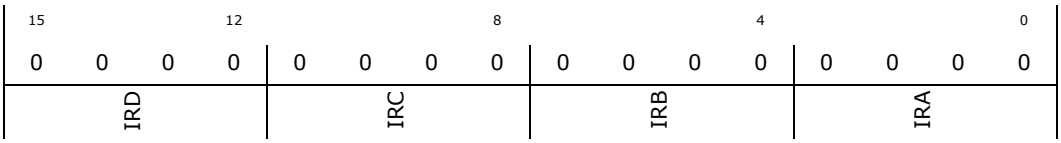
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR17: [ILB_BASE_ADDRESS] + 42h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.33 IR18—Offset 44h

IR18 - Interrupt Routing Device 18

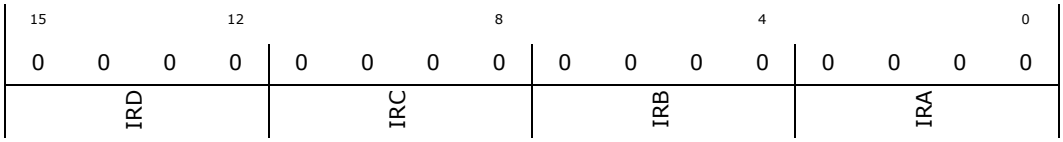
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR18: [ILB_BASE_ADDRESS] + 44h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.34 IR19—Offset 46h

IR19 - Interrupt Routing Device 19

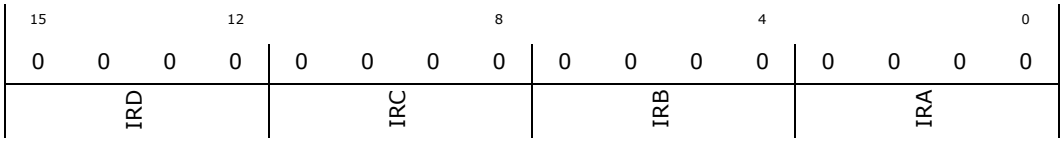
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR19: [ILB_BASE_ADDRESS] + 46h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.35 IR20—Offset 48h

IR20 - Interrupt Routing Device 20

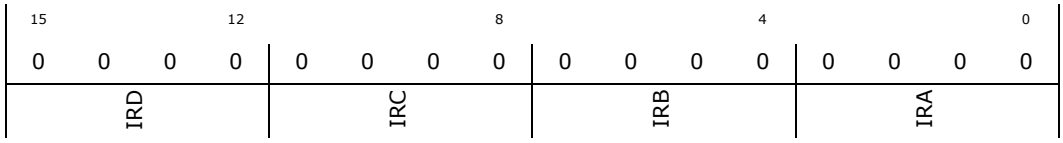
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR20: [ILB_BASE_ADDRESS] + 48h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.36 IR21—Offset 4Ah

IR21 - Interrupt Routing Device 21

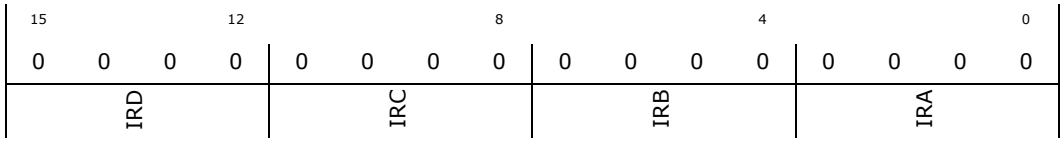
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR21: [ILB_BASE_ADDRESS] + 4Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H

Bit Range	Default & Access	Description
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.37 IR22—Offset 4Ch

IR22 - Interrupt Routing Device 22

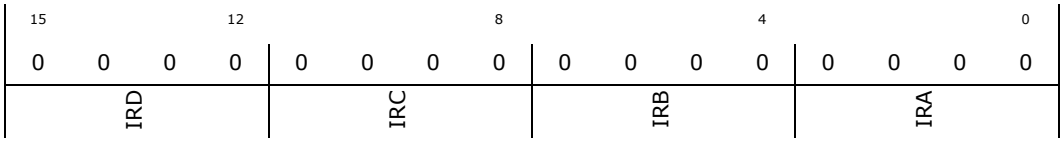
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR22: [ILB_BASE_ADDRESS] + 4Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.38 IR23—Offset 4Eh

IR23 - Interrupt Routing Device 23

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR23: [ILB_BASE_ADDRESS] + 4Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.39 IR24—Offset 50h

IR24 - Interrupt Routing Device 24

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR24: [ILB_BASE_ADDRESS] + 50h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.40 IR25—Offset 52h

IR25 - Interrupt Routing Device 25

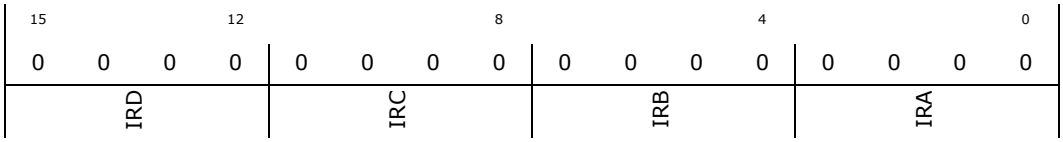
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR25: [ILB_BASE_ADDRESS] + 52h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.41 IR26—Offset 54h

IR26 - Interrupt Routing Device 26

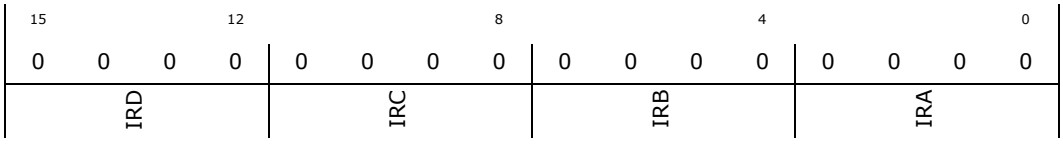
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR26: [ILB_BASE_ADDRESS] + 54h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.42 IR27—Offset 56h

IR27 - Interrupt Routing Device 27

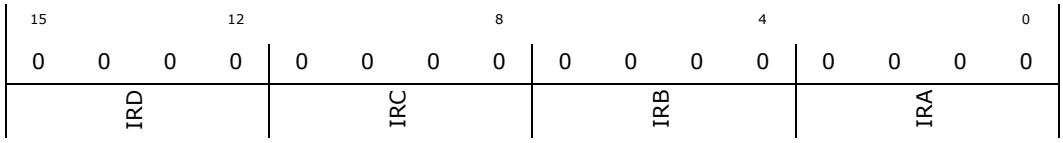
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR27: [ILB_BASE_ADDRESS] + 56h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.43 IR28—Offset 58h

IR28 - Interrupt Routing Device 28

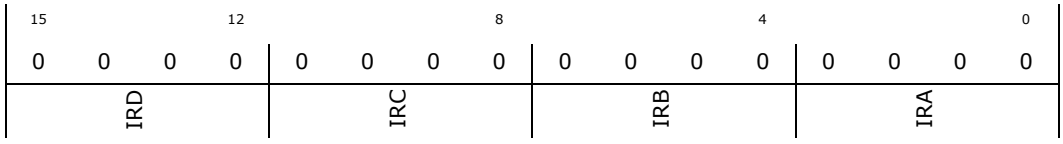
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR28: [ILB_BASE_ADDRESS] + 58h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H

Bit Range	Default & Access	Description
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.44 IR29—Offset 5Ah

IR29 - Interrupt Routing Device 29

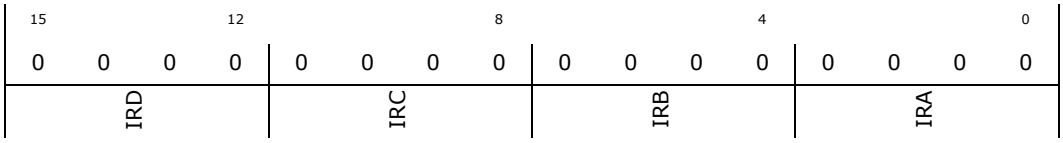
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR29: [ILB_BASE_ADDRESS] + 5Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.45 IR30—Offset 5Ch

IR30 - Interrupt Routing Device 30

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR30: [ILB_BASE_ADDRESS] + 5Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.46 IR31—Offset 5Eh

IR31 - Interrupt Routing Device 31

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR31: [ILB_BASE_ADDRESS] + 5Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

3.60.47 OIC—Offset 60h

Other Interrupt Control

Access Method

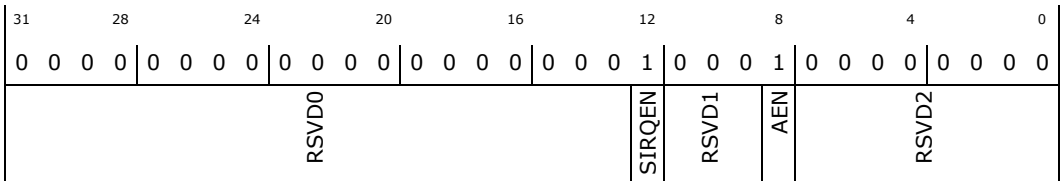
Type: Memory Mapped I/O Register (Size: 32 bits)

OIC: [ILB_BASE_ADDRESS] + 60h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00001100h



Bit Range	Default & Access	Description
31:13	0b RO	**RSVD0:** Reserved
12	1b RW	**SIRQEN:** When set, enables the internal SIRQ . when cleared the internal sIRQ is disabled
11:9	0b RO	**RSVD1:** Reserved
8	1b RW	**AEN:** When set, enables the internal IOAPIC and its address decode, when cleared the internal IOxAPIC is disabled. software should read this register after modifying the APIC enable prior to access to IOxAPIC address range. comment: en Couger Point the default value is 0.
7:0	0b RO	**RSVD2:** Reserved

3.60.48 RC—Offset 64h

RC - RTC Configuration

Access Method

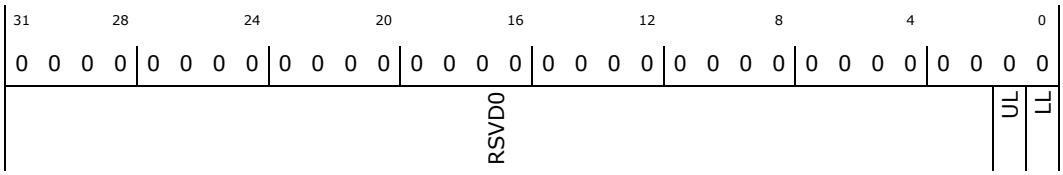
Type: Memory Mapped I/O Register (Size: 32 bits)

RC: [ILB_BASE_ADDRESS] + 64h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	0b RW/L	**UL:** Upper 128 Byte Lock (UL): When set, bytes 38h-3Fh in the upper 128 byte bank of RTC RAM are locked. Writes will be dropped and reads will not return any guaranteed data.
0	0b RW/L	**LL:** Lower 128 Byte Lock (LL): When set, bytes 38h-3Fh in the lower 128 byte bank of RTC RAM are locked. Writes will be dropped and reads will not return any guaranteed data.

3.60.49 BCS - BIOS Control Status (BCS)—Offset 6Ch

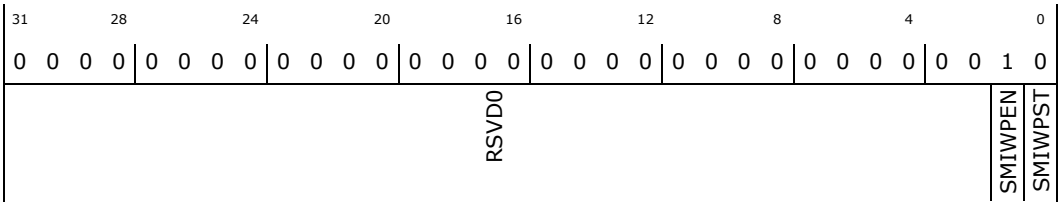
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BCS: [ILB_BASE_ADDRESS] + 6Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000002h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	1b RW	**SMIWPEN:** SMI WP Enable (SMIWPEN): When this bit is set to a 1, it enables the LPC to generate SMI upon not SMM code is trying to set BC.WP from a 0 to a 1 while BC.LE is set.
0	0b RW/1C	**SMIWPST:** SMI WP Status (SMIWPST): Set when SMI is generated upon trying to set BC.WP from a 0 to a 1 by not SMM code (while BC.LE and SMIWPEN are set). Write a 1 to this bit should clear it and clear the SMI (send DEASSERT_SMI)

3.60.50 LE—Offset 70h

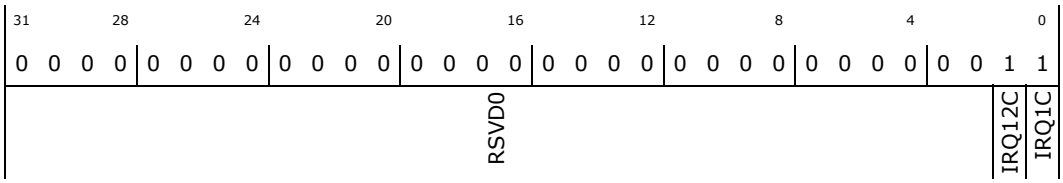
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LE: [ILB_BASE_ADDRESS] + 70h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000003h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	1b RW	**IRQ12_CAUSE (IRQ12C):** When software sets the bit to 1, IRQ12 will be high (asserted), When software set bit to 0,IRQ12 will be low (deasserted). default for this bit is 1
0	1b RW	**IRQ1_CAUSE (IRQ1C):** When software sets the bit to 1, IRQ11 will be high (asserted), When software set bit to 0,IRQ1 will be low (deasserted). default for this bit is 1

3.60.51 NMI (GNMI)—Offset 80h

NMI register

Access Method

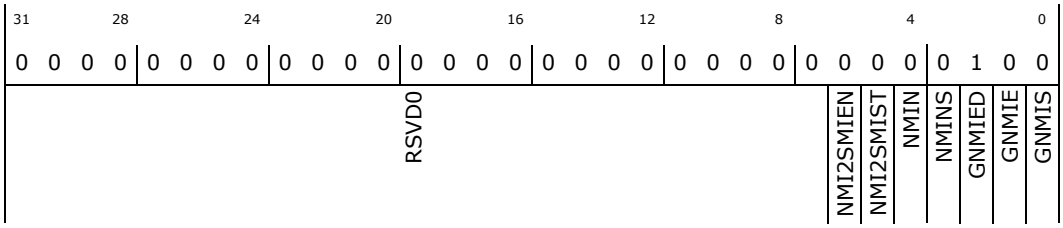
Type: Memory Mapped I/O Register (Size: 32 bits)

GNMI: [ILB_BASE_ADDRESS] + 80h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000004h



Bit Range	Default & Access	Description
31:7	0b RO	**RSVD0:** Reserved
6	0b RW	**NMI2SMIEN:** NMI to SMI Enable (NMI2SMIEN): When set, instead of NMI message SMI message will be sent.
5	0b RO	**NMI2SMIST:** NMI to SMI bit Status (NMI2SMIST)
4	0b RW/1C	**NMIN:** NMI NOW (NMIN): When set, NMI message will be sent. Writing 1'b1 to NMI_NOW inverts NMI_MOW and NMI_NOW_STS value

Bit Range	Default & Access	Description
3	0b RO	**NMINS:** NMI_NOW_STS is a result of the NMI_NOW configuration bit. Writing 1'b1 to NMI_NOW inverts NMI_NOW_STS value. Resulting that the first time NMI_NOW is written sets the NMI_NOW_STS and initiates NMI. Next writing clears the NMI_NOW_STS and allows initiating NMI by the next writing to NMI_NOW
2	1b RW	**GNMIED:** GPIO NMI Edge Detection (GNMIED): When set, NMI message will be sent on NMI GPIO posedge. when cleared the NMI message will be sent on negedge
1	0b RW	**GNMIE:** GPIO NMI Enable (GNMIE): When set, NMI message will be sent when NMI GPIO occurred. when cleared the message will not be sent
0	0b RW/1C	**GNMS (GNMIS):** GPIO NMI Status (GNMIS), when NMI is received from GPIO this bit is set. write '1' to this register to clear the status bit

3.60.52 LPCC—Offset 84h

LPC Control register

Access Method

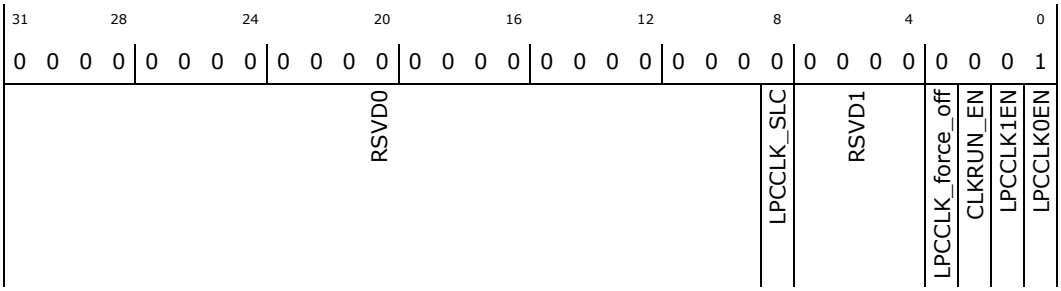
Type: Memory Mapped I/O Register (Size: 32 bits)

LPCC: [ILB_BASE_ADDRESS] + 84h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000001h



Bit Range	Default & Access	Description
31:9	0b RO	**RSVD0:** Reserved
8	0b RO	**LPCCLK_SLC:** iLPCCLK mux select (0 - ilpcclk0, 1 ilpcclk1)This bit get value from soft strap.
7:4	0b RO	**RSVD1:** Reserved
3	0b RW	**LPCCLK_force_off:** when asserted,oLPCCLK shut off similarly to CLKRUN protocol while ignoring iCLKRUN (LPC device reactions)
2	0b RW	**CLKRUN_EN:** LPC CLKRUN protocol enable (when not asserted, oLPCCLK toggles)

Bit Range	Default & Access	Description
1	0b RO	**LPCCLK1EN:** Clock 1 Enable (EN): This bit get value from soft strap. When set, LPC clock 1 is enabled. When cleared, it is disabled.
0	1b RO	**LPCCLK0EN:** Clock 0 Enable (EN): When set, LPC clock 0 is enabled. When cleared, it is disabled.

3.60.53 IRQEN (IRQE)—Offset 88h

IRQ Enable Control

Access Method

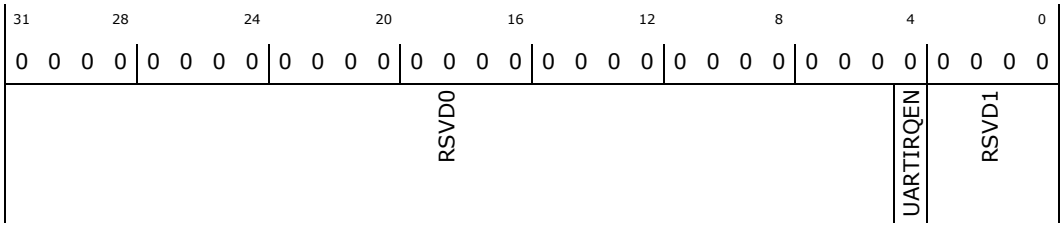
Type: Memory Mapped I/O Register (Size: 32 bits)

IRQE: [ILB_BASE_ADDRESS] + 88h

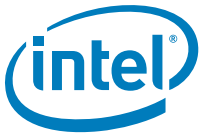
ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0b RO	**RSVD0:** Reserved
4	0b RO	**UARTIRQEN:** UART IRQ4 Enable
3:0	0b RO	**RSVD1:** Reserved



3.61 PCU iLB Low Pin Count (LPC) Bridge PCI Configuration Registers

Table 69. Summary of PCU iLB Low Pin Count (LPC) Bridge PCI Configuration Registers—0/31/0

Offset	Size	Register ID—Description	Default Value
0h	4	"Identifiers Register (PCIE_REG_Identifiers)—Offset 0h" on page 3186	00008086h
4h	2	"Command (PCIE_REG_COMMAND)—Offset 4h" on page 3186	0007h
6h	2	"Status (PCIE_REG_STATUS)—Offset 6h" on page 3188	0210h
8h	4	"Revision ID and Class Code (PCIE_REG_REVISION_ID_CLASS_CODE)—Offset 8h" on page 3189	06010000h
Dh	1	"Master Latency Timer (PCIE_REG_MASTER_LAT_TIMER)—Offset Dh" on page 3190	00h
Eh	1	"Header Type (PCIE_REG_HEADER_TYPE)—Offset Eh" on page 3191	80h
2Ch	4	"Subsystem ID and Vendor ID (PCIE_REG_SUBSYS_VENDOR_ID)—Offset 2Ch" on page 3191	00000000h
34h	4	"Capability List Pointer (PCIE_REG_CAP_POINTER)—Offset 34h" on page 3192	000000E0h
40h	4	"ABASE (ACPI_BASE_ADDRESS)—Offset 40h" on page 3193	00000001h
44h	4	"PBASE (PMC_BASE_ADDRESS)—Offset 44h" on page 3193	00000000h
48h	4	"GBASE (GPIO_BASE_ADDRESS)—Offset 48h" on page 3194	00000001h
4Ch	4	"IOBASE (IO_CONTROLLER_BASE_ADDRESS)—Offset 4Ch" on page 3195	00000000h
50h	4	"IBASE (ILB_BASE_ADDRESS)—Offset 50h" on page 3196	00000000h
54h	4	"SBASE (SPI_BASE_ADDRESS)—Offset 54h" on page 3196	00000000h
58h	4	"MPBASE (MPHY_BASE_ADDRESS)—Offset 58h" on page 3197	00000000h
5Ch	4	"PUBASE (PUNIT_BASE_ADDRESS)—Offset 5Ch" on page 3198	00000000h
80h	4	"UART Control (UART_CONT)—Offset 80h" on page 3199	00000000h
D8h	2	"BIOS Decode Enable (PCIE_REG_BIOS_DECODE_EN)—Offset D8h" on page 3199	FFCFh
E0h	2	"FDCAP (Feature_Detection_Capability_ID)—Offset E0h" on page 3201	0009h
E2h	1	"FDLEN (Feature_Detection_Capability_Length)—Offset E2h" on page 3201	0Ch
E3h	1	"FDVER (Feature_Detection_Version_Register)—Offset E3h" on page 3202	10h
E4h	4	"FVECTIDX (Feature_Vector_Index)—Offset E4h" on page 3202	00000000h
E8h	4	"FVECTD (Feature_Vector_Data)—Offset E8h" on page 3202	00000000h
F0h	4	"RCBA (RCRB_BASE_ADDRESS)—Offset F0h" on page 3203	00000000h

Table 69. Summary of PCU iLB Low Pin Count (LPC) Bridge PCI Configuration Registers—0/31/0 (Continued)

Offset	Size	Register ID—Description	Default Value
F4h	4	"ULT Observability (PCIE_REG_ULT_OBSERVABILITY)—Offset F4h" on page 3203	00000000h
F8h	4	"Manufacturer ID (PCIE_REG_MANUFACTURER_ID)—Offset F8h" on page 3204	00000F00h
FCh	4	"Clock Gating Control (CLOCK_GATING_CONTROL)—Offset FCh" on page 3205	00000303h

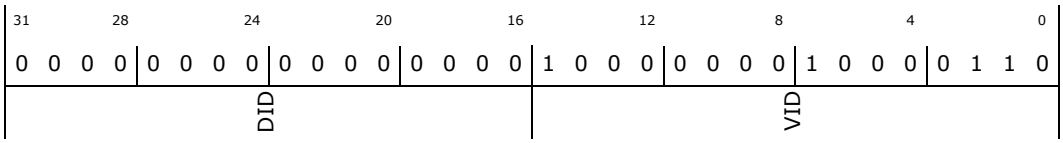
3.61.1 Identifiers Register (PCIE_REG_Identifiers)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_Identifiers: [B:0, D:31, F:0] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	X RO	**Device Identification (DID):** This field identifies the particular device. This identifier is allocated by the vendor. This field is controlled by the LPC DID fuses Bits [31:23] are coming from the SETIDVALUE message Device ID[15:7] bits. Bits [22:21] are set constantly to 2'b00. Bits [20:16] are set constantly by pcu_did fuses.
15:0	8086h RO	**Vendor Identification (VID):** This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. 0 FFFFh is an invalid value for Vendor ID.

3.61.2 Command (PCIE_REG_COMMAND)—Offset 4h

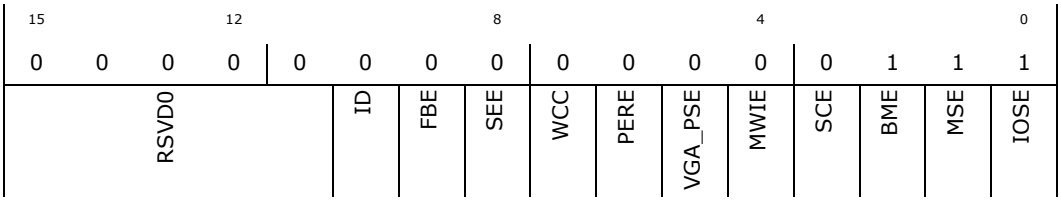
The Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command register may or may not be implemented depending on a device's functionality

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCIE_REG_COMMAND: [B:0, D:31, F:0] + 4h

Default: 0007h



Bit Range	Default & Access	Description
15:11	0b RO	**RSVD0:** Reserved
10	0b RO	**Interrupt Disable (ID):** This bit disables the device/function from asserting INTx#. A value of 0 enables the assertion of its INTx# signal. A value of 1 disables the assertion of its INTx# signal. The LPC bridge has no interrupts to disable
9	0b RO	**Fast Back to Back Enable (FBE):** This optional read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. A value of 0 means fast back-to-back transactions are only allowed to the same agent
8	0b RW	**SERR# Enable (SEE):** This bit is an enable bit for the SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver.
7	0b RO	**Wait Cycle Control (WCC):** Reserved as '0' per PCI-Express spec
6	0b RW	**Parity Error Response Enable (PERE):** This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error status bit (bit 15 in the Status register) when an error is detected, but does not assert PERR# and continues normal operation.
5	0b RO	**VGA Palette Snoop (VGA_PSE):** This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. When this bit is 1, palette snooping is enabled (i.e., the device does not respond to palette register writes and snoops the data). When the bit is 0, the device should treat palette write accesses like all other accesses. Reserved as '0' per PCI-Express spec
4	0b RO	**Memory Write and Invalidate Enable (MWIE):** This is an enable bit for using the Memory Write and Invalidate command. When this bit is 1, masters may generate the command. When it is 0, Memory Write must be used instead. Reserved as '0' per PCI-Express spec
3	0b RO	**Special Cycle Enable (SCE):** Controls a device's action on Special Cycle operations. A value of 0 causes the device to ignore all Special Cycle operations. A value of 1 allows the device to monitor Special Cycle operations. Reserved as '0' per PCI-Express spec
2	1b RO	**Bus Master Enable (BME):** Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. Bus master cannot be disabled on LPC
1	1b RO	**Memory Space Enable (MSE):** Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. Memory space cannot be disable on LPC

Bit Range	Default & Access	Description
0	1b RO	**I/O Space Enable (IOSE):** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. I/O space cannot be disable on LPC

3.61.3 Status (PCIE_REG_STATUS)—Offset 6h

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A one bit is reset (if it is not read-only) whenever the register is written, and the write data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCIE_REG_STATUS: [B:0, D:31, F:0] + 6h

Default: 0210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DTS		DPD	FBC	RSVD0		C66	CLIST	IS	RSVD1	

Bit Range	Default & Access	Description
15	0b RW	**Detected Parity Error (DPE):** This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register).
14	0b RW	**Signaled System Error (SSE):** This bit must be set whenever the device asserts SERR#. Set when the LPC bridge signals a system error to the internal SERR# logic.
13	0b RW	**Received Master Abort (RMA):** This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort. All master devices must implement this bit.
12	0b RW	**Received Target Abort: (RTA):** This bit must be set by a master device whenever its transaction is terminated with Target-Abort. All master devices must implement this bit.
11	0b RW	**Signaled Target Abort (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target- Abort do not need to implement this bit.
10:9	01b RO	**DEVSEL# Timing Status (DTS):** These bits encode the timing of DEVSEL#. These are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). These bits Indicate medium timing, although this has no meaning on the backbone

Bit Range	Default & Access	Description
8	0b RW	**Data Parity Error Detected (DPD):** This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3) the Parity Error Response bit (Command register) is set.
7	0b RO	**Fast Back to Back Capable (FBC):** This optional read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise. This bit has no meaning on internal backbone.
6	0b RO	**RSVD0:** Reserved
5	0b RO	**66 MHz Capable (C66):** This optional read-only bit indicates whether or not this device is capable of running at 66 MHz. A value of zero indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable. This bit has no meaning on internal backbone
4	1b RO	**Capabilities List (CLIST):** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities. There is a capabilities list in the LPC bridge.
3	0b RO	**Interrupt Status (IS):** This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. The LPC bridge does not generate interrupts
2:0	0b RO	**RSVD1:** Reserved

3.61.4 Revision ID and Class Code (PCIE_REG_REVISION_ID_CLASS_CODE)—Offset 8h

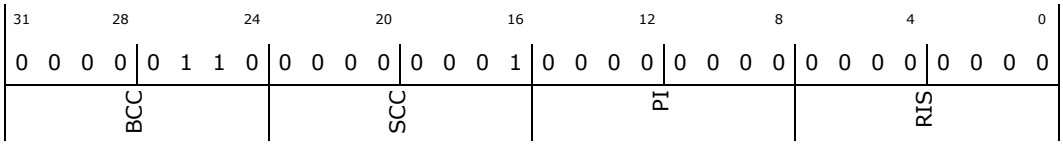
This register is a combination of two registers the Revision ID register and the Class Code register. The revision ID register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. The Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_REVISION_ID_CLASS_CODE: [B:0, D:31, F:0] + 8h

Default: 06010000h



Bit Range	Default & Access	Description
31:24	06h RO	**Base Class Code (BCC):** This field is a base class code which broadly classifies the type of function the device performs. Indicates the device is a bridge device.
23:16	01h RO	**Sub-Class Code (SCC):** This field is a sub-class code which identifies more specifically the function of the device. Indicates the device a PCI to ISA bridge
15:8	00h RO	**Programming Interface (PI):** This field identifies a specific register-level programming interface if any) so that device independent software can interact with the device. The LPC bridge has no programming interface.
7:0	X RO	**Revision ID (RIS):** This register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. This field should be viewed as a vendor defined extension to the Device ID. This field is controlled by the LPC RID fuses. Coming from the SETIDVALUE message Revision ID field

3.61.5 Master Latency Timer (PCIE_REG_MASTER_LAT_TIMER)—Offset Dh

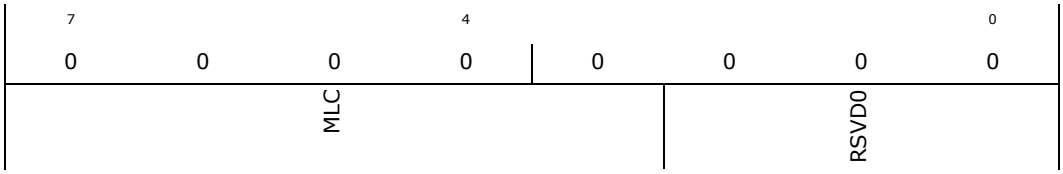
This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. This register is implemented as read-only, the register must be initialized to 0.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

PCIE_REG_MASTER_LAT_TIMER: [B:0, D:31, F:0] + Dh

Default: 00h



Bit Range	Default & Access	Description
7:3	00h RO	**Master Latency Count (MLC):** Reserved per PCIe spec.
2:0	0b RO	**RSVD0:** Reserved

3.61.6 Header Type (PCIE_REG_HEADER_TYPE)—Offset Eh

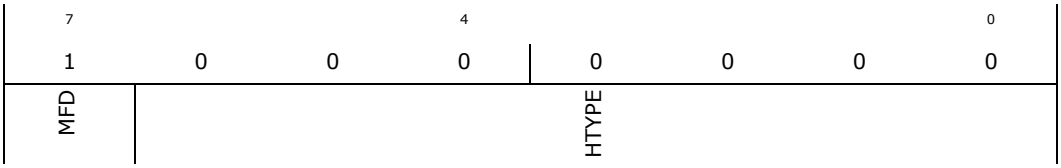
This byte identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space) and also whether or not the device contains multiple functions.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

PCIE_REG_HEADER_TYPE: [B:0, D:31, F:0] + Eh

Default: 80h



Bit Range	Default & Access	Description
7	1b RO	**Multi-function Device (MFD):** This field is used to identify a multi-function device. If the bit is 0, then the device is single function. If the bit is 1, then the device has multiple functions.
6:0	00h RO	**Header Type (HTYPE):** This field identifies the layout of the second part of the predefined header. The encoding 00h specifies the standard layout.

3.61.7 Subsystem ID and Vendor ID (PCIE_REG_SUBSYS_VENDOR_ID)—Offset 2Ch

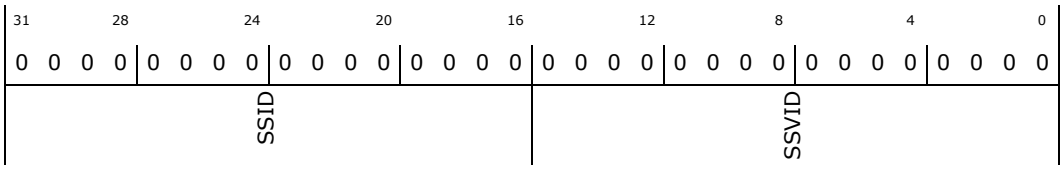
This register is used to uniquely identify the add-in card or subsystem where the PCI device resides. It provides a mechanism for add-in card vendors to distinguish their add- in cards from one another even though the add-in cards may have the same PCI controller on them (and, therefore, the same Vendor ID and Device ID). Implementation of this register is required for all PCI devices except those that have a base class 6 with sub class 0-4 (0, 1, 2, 3, 4), or a base class 8 with sub class 0-3 (0, 1, 2, 3). Subsystem Vendor IDs can be obtained from the PCI SIG and are used to identify the vendor of the add-in card or subsystem. Values for the Subsystem ID are vendor specific. Values in these registers must be loaded and valid prior to the system firmware or any system software accessing the PCI Configuration Space. How these values are loaded is not specified but could be done during the manufacturing process or loaded from external logic (e.g., strapping options, serial ROMs, etc.). These values must not be loaded using expansion ROM software because expansion ROM software is not guaranteed to be run during POST in all systems. Devices are responsible for guaranteeing the data is valid before allowing reads to these registers to complete. This can be done by responding to any accesses with Retry until the data is valid. If a device is designed to be used exclusively on the system board, the system vendor may use system specific software to initialize these registers after each power-on. This register can be written only once after PMU_PLTRST_B de-assertion.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_SUBSYS_VENDOR_ID: [B:0, D:31, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value. This field could be written only once.
15:0	0000h RW	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value. This field could be written only once.

3.61.8 Capability List Pointer (PCIE_REG_CAP_POINTER)—Offset 34h

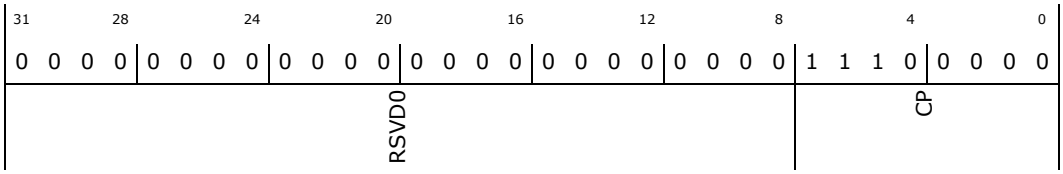
This optional register is used to point to a linked list of new capabilities implemented by this device. This register is only valid if the Capabilities List bit in the Status Register is set. If implemented, the bottom two bits are reserved and should be set to 00b. Software should mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_CAP_POINTER: [B:0, D:31, F:0] + 34h

Default: 000000E0h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	E0h RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

3.61.9 ABASE (ACPI_BASE_ADDRESS)—Offset 40h

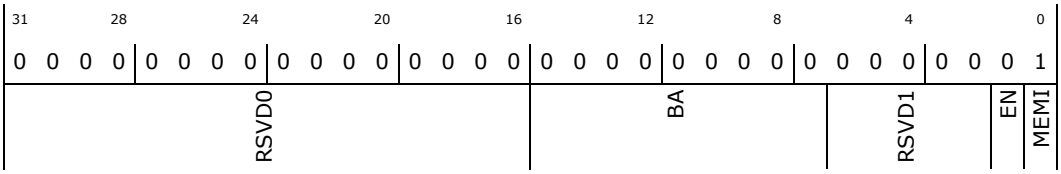
ACPI is mapped into I/O space. It is used by the PMC. Base Address registers that map into I/O Space are always 32 bits wide with bit 0 hardwired to a 1. Bit 1 is used to enable IO range pointed by this base address. Bits 31:16 are reserved and must return 0 on reads and the other bits could be used to map the device into I/O Space.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS: [B:0, D:31, F:0] + 40h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:7	000h RW	**Base Address (BA):** Provides the 128 bytes of I/O space for ACPI and TCO logic
6:2	0b RO	**RSVD1:** Reserved
1	0b RW	**Enable (EN):** When set, decode of the IO range pointed to by the ABASE is enabled.
0	1b RO	**Memory Space Indication (MEMI):** This read-only bit always is 1, indicating that this BAR is IO mapped

3.61.10 PBASE (PMC_BASE_ADDRESS)—Offset 44h

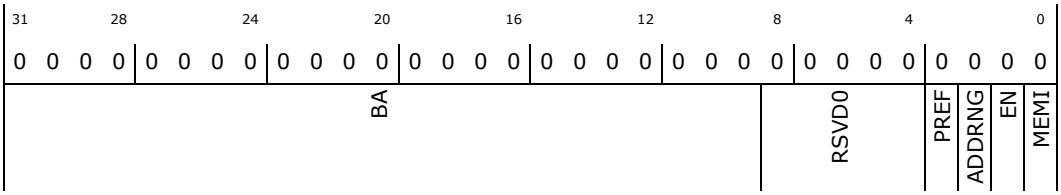
PMC registers are mapped into memory space. It is used by the PMC. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	000000h RW	**Base Address (BA):** Provides 512 byte system memory base address for the PMC logic
8:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the PBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

3.61.11 GBASE (GPIO_BASE_ADDRESS)—Offset 48h

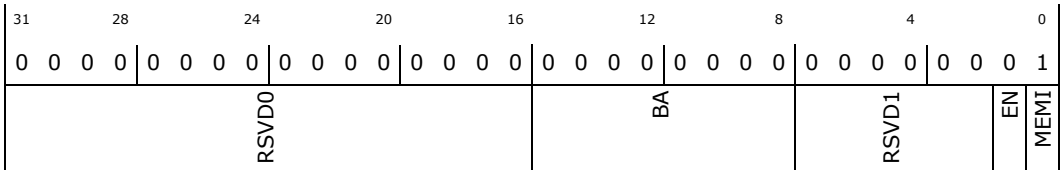
GPIO registers are mapped into I/O space. It is used by the Proxy agent (to IO controllers). Base Address registers that map into I/O Space are always 32 bits wide with bit 0 hardwired to a 1. Bit 1 is used to enable IO range pointed by this base address. Bits 31:16 are reserved and must return 0 on reads and the other bits could be used to map the device into I/O Space.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GPIO_BASE_ADDRESS: [B:0, D:31, F:0] + 48h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RW	**Base Address (BA):** Provides the 256 bytes of I/O space for GPIO logic
7:2	0b RO	**RSVD1:** Reserved
1	0b RW	**Enable (EN):** When set, decode of the IO range pointed to by the GBASE is enabled.

Bit Range	Default & Access	Description
0	1b RO	**Memory Space Indication (MEMI):** This read-only bit always is 1, indicating that this BAR is IO mapped

3.61.12 IOBASE (IO_CONTROLLER_BASE_ADDRESS)—Offset 4Ch

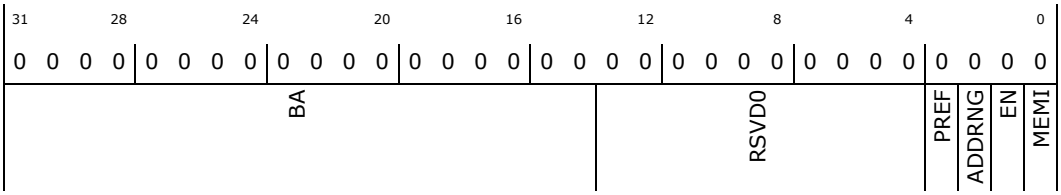
IO Controllers registers are mapped into memory space. It is used by the Proxy agent (to IO controllers). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IO_CONTROLLER_BASE_ADDRESS: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:14	00000h RW	**Base Address (BA):** Provides 8K byte system memory base address for the IO controllers logic
13:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the IOBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

3.61.13 IBASE (ILB_BASE_ADDRESS)—Offset 50h

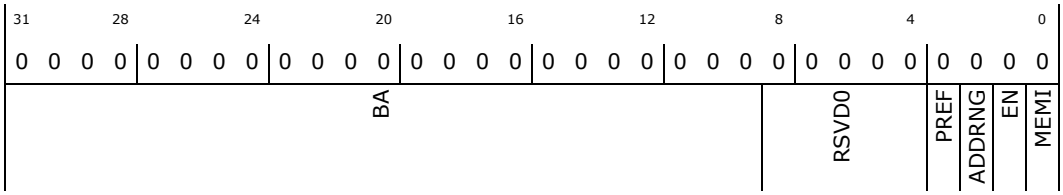
iLB registers are mapped into memory space. It is used by the iLB. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	000000h RW	**Base Address (BA):** Provides 512 byte system memory base address for the iLB logic
8:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the IBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

3.61.14 SBASE (SPI_BASE_ADDRESS)—Offset 54h

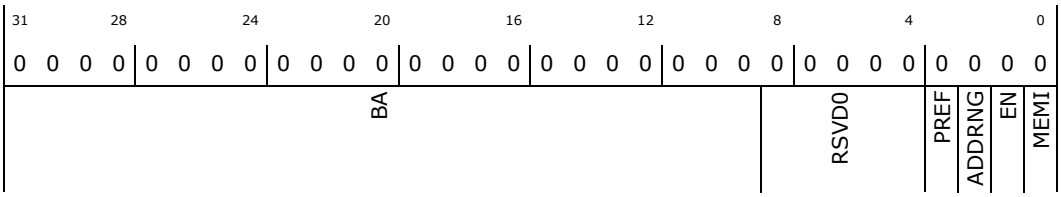
SPI registers are mapped into memory space. It is used by the SPI. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	000000h RW	**Base Address (BA):** Provides 512 byte system memory base address for the SPI logic
8:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the SBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

3.61.15 MPBASE (MPHY_BASE_ADDRESS)—Offset 58h

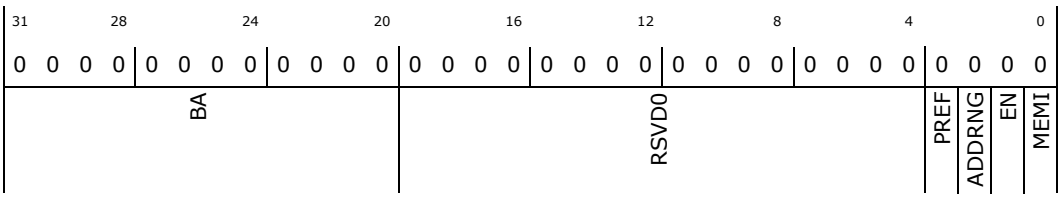
M-phys registers are mapped into memory space. It is used by the Proxy agent (to M-phys). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MPHY_BASE_ADDRESS: [B:0, D:31, F:0] + 58h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	000h RW	**Base Address (BA):** Provides 1M byte system memory base address for the M phys logic
19:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the MPBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

3.61.16 PUBASE (PUNIT_BASE_ADDRESS)—Offset 5Ch

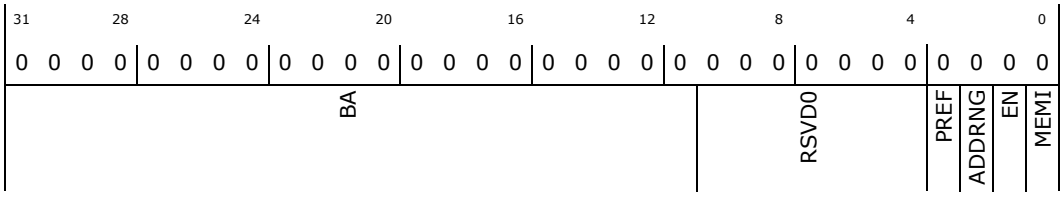
P-Unit registers are mapped into memory space. It is used by the Proxy agent (to P-Unit). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PUNIT_BASE_ADDRESS: [B:0, D:31, F:0] + 5Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:11	00000h RW	**Base Address (BA):** Provides 2K byte system memory base address for the P-Unit registers
10:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.

Bit Range	Default & Access	Description
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the PUBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

3.61.17 UART Control (UART_CONT)—Offset 80h

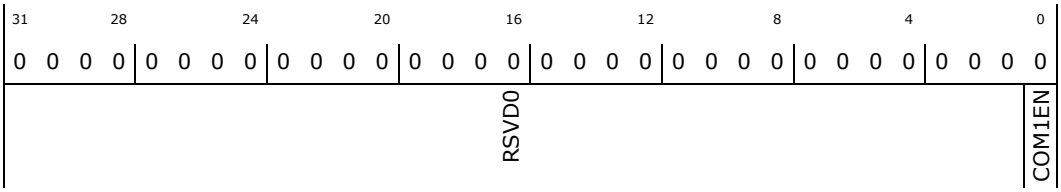
Controls the internal PCU UART ports

Access Method

Type: PCI Configuration Register (Size: 32 bits)

UART_CONT: [B:0, D:31, F:0] + 80h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0b RW	**COM1 Enable (COM1EN):** When set, enables the internal PCU COM1 UART port.

3.61.18 BIOS Decode Enable (PCIE_REG_BIOS_DECODE_EN)—Offset D8h

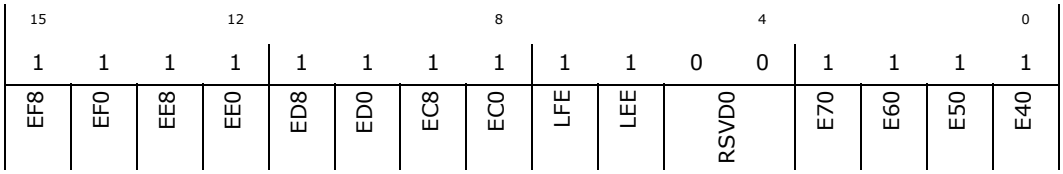
This register enables ranges in the BIOS for decoding purposes. Note that this register affects the BIOS decode regardless of whether the BIOS is resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based flash. PCU EP simply decodes these ranges as memory accesses when enabled for the SPI/LPC flash interface.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCIE_REG_BIOS_DECODE_EN: [B:0, D:31, F:0] + D8h

Default: FFCFh



Bit Range	Default & Access	Description
15	1b RW	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFF80000 - 0xFFFFFFFF - Feature space: 0xFFB80000 - 0xFFBFFFFF
14	1b RW	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFF00000 - 0xFFF7FFFF - Feature space: 0xFFB00000 - 0xFFB7FFFF
13	1b RW	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFE80000 - 0xFFEFFFFF - Feature space: 0xFFA80000 - 0xFFAFFFFF
12	1b RW	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFE00000 - 0xFFE7FFFF - Feature space: 0xFFA00000 - 0xFFA7FFFF
11	1b RW	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFD80000 - 0xFFDFFFFF - Feature space: 0XFF980000 - 0xFF9FFFFF
10	1b RW	**D0-D8 Enable (ED0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFD00000 - 0xFFD7FFFF - Feature space: 0XFF900000 - 0xFF97FFFF
9	1b RW	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFC80000h - 0xFFCFFFFF - Feature space: 0xFF880000h - 0xFF8FFFFF
8	1b RW	**C0-C8 Enable (EC0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFC00000 - 0xFFC7FFFF - Feature space: 0xFF800000 - 0xFF87FFFF
7	1b RW	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at 0xF0000 - 0xFFFFF
6	1b RW	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at 0xE0000 - 0xEFFFF
5:4	0b RO	**RSVD0:** Reserved
3	1b RW	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF700000 - 0xFF7FFFFF - Feature space: 0xFF300000 - 0xFF3FFFFF
2	1b RW	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF600000 - 0xFF6FFFFF - Feature Space: 0xFF200000 - 0xFF2FFFFF
1	1b RW	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF500000 - 0xFF5FFFFF - Feature space: 0xFF100000 - 0xFF1FFFFF

Bit Range	Default & Access	Description
0	1b RW	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF400000 - 0xFF4FFFFF - Feature Space: 0xFF000000 - 0xFF0FFFFF

3.61.19 FDCAP (Feature_Detection_Capability_ID)—Offset E0h

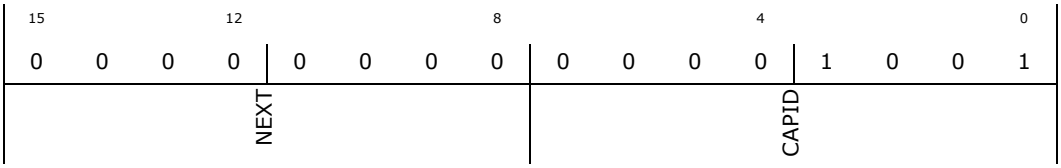
Feature detection capability ID.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Feature_Detection_Capability_ID: [B:0, D:31, F:0] + E0h

Default: 0009h



Bit Range	Default & Access	Description
15:8	00h RO	**Next Item Pointer (NEXT):** Configuration offset of the next Capability Item. 0x00 indicates the last item in the Capability List.
7:0	09h RO	**Capability ID (CAPID):** Value of 0x09 indicates a Vendor Specific Capability

3.61.20 FDLEN (Feature_Detection_Capability_Length)—Offset E2h

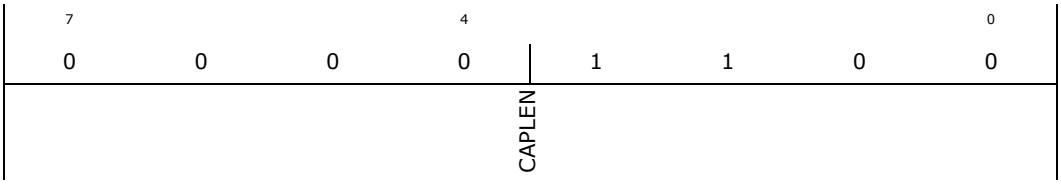
Feature detection capability length.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Feature_Detection_Capability_Length: [B:0, D:31, F:0] + E2h

Default: 0Ch



Bit Range	Default & Access	Description
7:0	0Ch RO	**Capability Length (CAPLEN):** Indicates the length of this Vendor Specific capability, as required by PCI Spec

3.61.21 FDVER (Feature_Detection_Version_Register)—Offset E3h

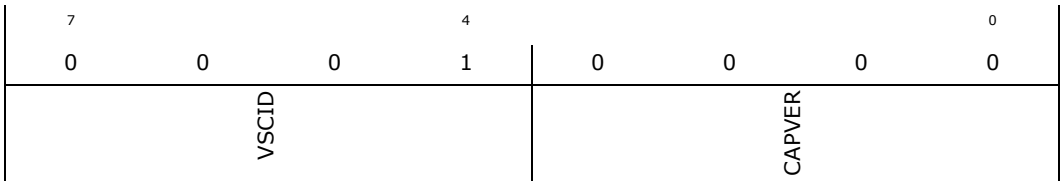
Feature detection version register.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Feature_Detection_Version_Register: [B:0, D:31, F:0] + E3h

Default: 10h



Bit Range	Default & Access	Description
7:4	1h RO	**Vendor-Specific Capability ID (VSCID):** A value of 0x1 in this 4-bit field identifies this Capability as Feature Detection Type. This field allows software to differentiate the Feature Detection Capability from other Vendor-Specific capabilities.
3:0	0h RO	**Capability Version (CAPVER):** This field indicates the version of the Feature Detection capability

3.61.22 FVECTIDX (Feature_Vector_Index)—Offset E4h

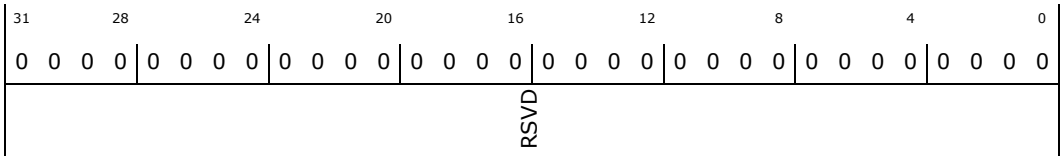
Feature vector index - Reserved

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Feature_Vector_Index: [B:0, D:31, F:0] + E4h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**RSVD:** RSVD

3.61.23 FVECTD (Feature_Vector_Data)—Offset E8h

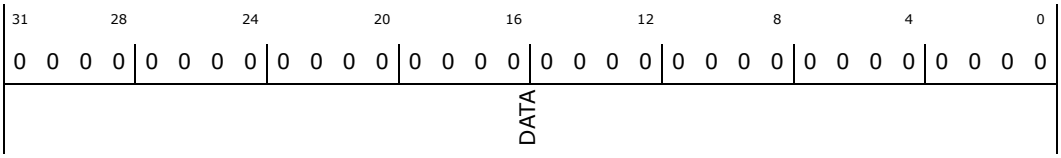
Feature vector data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Feature_Vector_Data: [B:0, D:31, F:0] + E8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Data (DATA):** 32-bit data value that is taken from capability feature fuses

3.61.24 RCBA (RCRB_BASE_ADDRESS)—Offset F0h

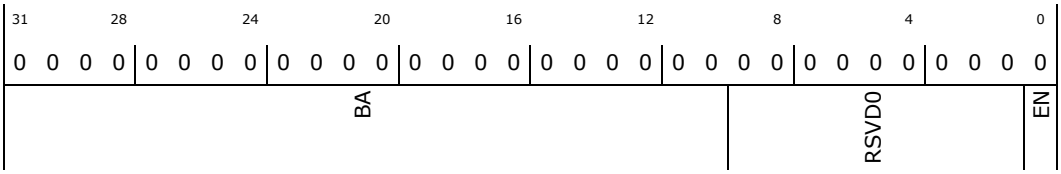
Root Complex registers are mapped into memory space. It is used by the PCU EP and Proxy engine.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RCRB_BASE_ADDRESS: [B:0, D:31, F:0] + F0h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	000000h RW	**Base Address (BA):** Base Address for the root complex register block decode range. This address is aligned on a 1KB boundary.
9:1	0b RO	**RSVD0:** Reserved
0	0b RW	**Enable (EN):** When set, enables the range specified in BA to be claimed as the RCRB.

3.61.25 ULT Observability (PCIE_REG_ULT_OBSERVABILITY)—Offset F4h

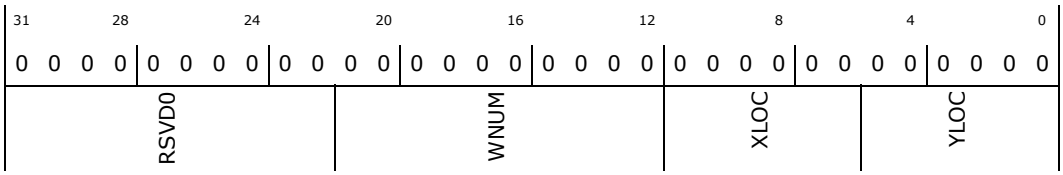
Not EDS :Provides the ability to read the Unit Level Tracking information (as long as the ULT read enable fuse allows it.)

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_ULT_OBSERVABILITY: [B:0, D:31, F:0] + F4h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0b RO	**RSVD0:** Reserved
21:12	X RO	**Wafer Number (WNUM):** Reserved
11:6	X RO	**X Location (XLOC):** Reserved
5:0	X RO	**Y Location (YLOC):** Reserved

3.61.26 Manufacturer ID (PCIE_REG_MANUFACTURER_ID)—Offset F8h

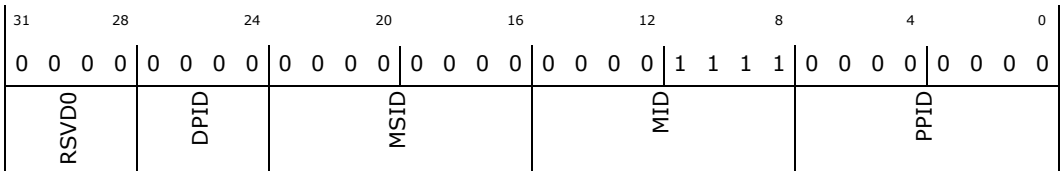
Not EDS :Manufacturer ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_MANUFACTURER_ID: [B:0, D:31, F:0] + F8h

Default: 00000F00h



Bit Range	Default & Access	Description
31:28	0b RO	**RSVD0:** Reserved
27:24	X RO	**Dot portion of Process ID (DPID):** This filed is controlled by fuses. Indicates the dot as '.1' Note: Process/Dot(PD) is 1271.1. Process is reflected in bits [7:0] Coming from the SETIDVALUE message Dot Portion of Process ID field
23:16	X RO	**Manufacturing Stepping Identifier (MSID):** This filed is controlled by fuses. This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Stepping Revision ID may not change. A single Manufacturing Stepping ID can be implemented that is readable from all functions in the chip because all of them are incremented in lock-step. Coming from the SETIDVALUE message Manufacturing Stepping ID field

Bit Range	Default & Access	Description
15:8	0Fh RO	**Manufacturing Identifier (MID):** 0Fh indicates Intel Coming from the SETIDVALUE message Manufacturing ID field
7:0	X RO	**Process portion of process ID (PPID):** This filed is controlled by fuses. Indicates the process as 1271. Note: Process/Dot (PD) is 1271.1. Dot is reflected in bits [27:24] Implementation Note: It is recommended that the Manufacturing ID is implemented in one place and readable from all functions. This minimizes the changes required for a process shrink. Coming from the SETIDVALUE message Process Portion of Process ID field

3.61.27 Clock Gating Control (CLOCK_GATING_CONTROL)—Offset FCh

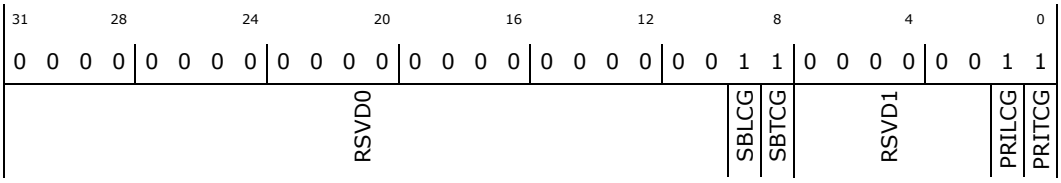
Not EDS :Clock Gating Control

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLOCK_GATING_CONTROL: [B:0, D:31, F:0] + FCh

Default: 00000303h



Bit Range	Default & Access	Description
31:10	0b RO	**RSVD0:** Reserved
9	1b RW	**SBLCG:** IOSF-SB local clock gating disable
8	1b RW	**SBTCG:** IOSF-SB trunk clock gating (request) disable
7:2	0b RO	**RSVD1:** Reserved
1	1b RW	**PRILCG:** IOSF-PRI local clock gating disable
0	1b RW	**PRITCG:** IOSF-PRI trunk clock gating (request) disable

3.62 PCU iLB LPC BIOS Control Memory Mapped I/O Registers

Table 70. Summary of PCU iLB LPC BIOS Control Memory Mapped I/O Registers—RCRB_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"GCS (RCRB_GENERAL_CONTROL)—Offset 0h" on page 3206	00000000h

3.62.1 GCS (RCRB_GENERAL_CONTROL)—Offset 0h

General Control and Status - contains BIOS configuration and status

Access Method

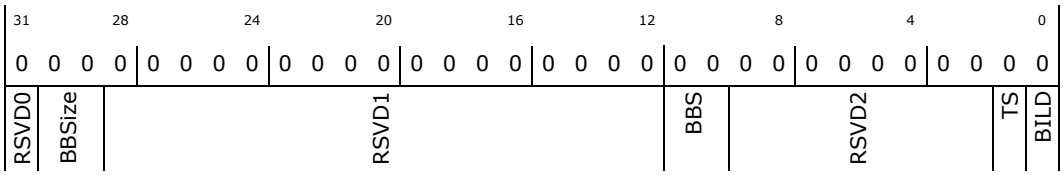
Type: Memory Mapped I/O Register (Size: 32 bits)

RCRB_GENERAL_CONTROL: [RCRB_BASE_ADDRESS] + 0h

RCRB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

RCRB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + F0h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**RSVD0:** Reserved
30:29	X RO	**Boot Block Size (BBSize):** This field determines the size of the BIOS boot block. Default is controlled by 'Boot Block Size' soft strap. 00 : 64KB (Default) : Invert A16 if Top Swap is enabled 01 : 128KB : Invert A17 if Top Swap is enabled 10 : 256KB : Invert A18 if Top Swap is enabled 11 : Reserved This soft strap only applies when booting from SPI. Boot from LPC (FWH) only supports a 64KB boot block size (Invert A16) and this soft strap value is a don't care.
28:12	0b RO	**RSVD1:** Reserved
11:10	X RW	**Boot BIOS Straps (BBS):** This field determines the destination of accesses to the BIOS memory range. Default is controlled by 'Boot BIOS Straps' pin strap. 00 LPC 01 Reserved 10 Reserved 11 SPI The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) is not set.
9:2	0b RO	**RSVD2:** Reserved

Bit Range	Default & Access	Description
1	X RW	**Top Swap (TS):** When set, PCU EP will invert either A16, A17, or A18 for cycles going to the BIOS space (but not the feature space) in the FWH. When cleared, PCU EP will not invert A16. If booting from LPC (FWH), then the Boot Blook size is 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, or A18 should be inverted if Top Swap is enabled. If Top-Swap pin-strap is active, then this bit cannot be cleared by software. This bit should be kept in RTC well and should be reset only by SRTCRST_b
0	0h RW	**BIOS Interface Lock-Down (BILD):** When set, prevents GCS.TS and GCS.BBS from being changed. This bit can only be written from 0 to 1 once.

3.63 PCU iLB Real Time Clock (RTC) I/O Registers

Table 71. Summary of PCU iLB Real Time Clock (RTC) I/O Registers—

Offset	Size	Register ID—Description	Default Value
70h	1	"IR (reg_RTC_IR_type)—Offset 70h" on page 3208	00h
71h	1	"TR (reg_RTC_TR_type)—Offset 71h" on page 3208	00h
72h	1	"RIR (reg_RTC_RIR_type)—Offset 72h" on page 3209	00h
73h	1	"RTR (reg_RTC_RTR_type)—Offset 73h" on page 3209	00h

3.63.1 IR (reg_RTC_IR_type)—Offset 70h

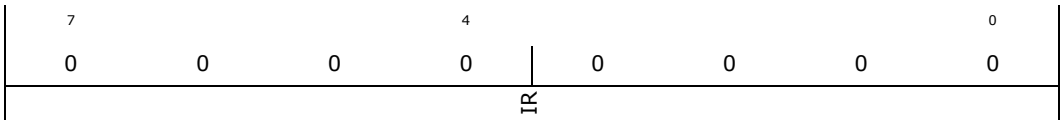
Indexed Registers

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_IR_type: 70h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**IR:** Real-Time Clock (Standard RAM) Index Register Note: Writes to 72h, 74h, and 76h do not affect the NMI enable (bit 7 of 70h)

3.63.2 TR (reg_RTC_TR_type)—Offset 71h

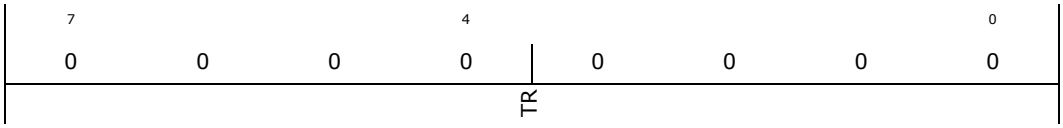
Target Registers

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_TR_type: 71h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**TR:** Real-Time Clock (Standard RAM) Target Register

3.63.3 RIR (reg_RTC_RIR_type)—Offset 72h

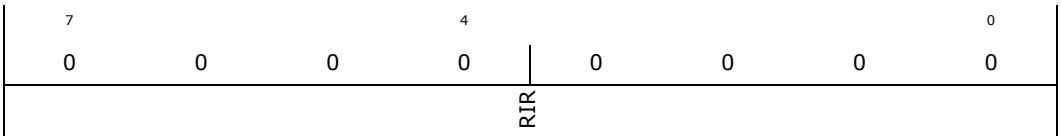
Extended RAM Index Register

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_RIR_type: 72h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**RIR:** Extended RAM Index Register

3.63.4 RTR (reg_RTC_RTR_type)—Offset 73h

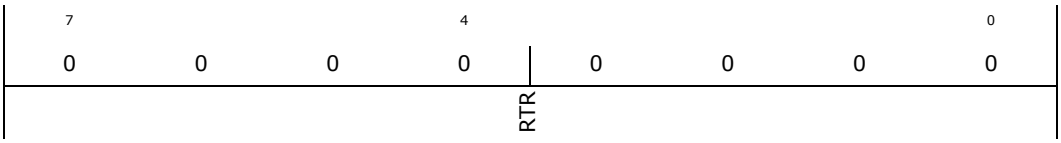
Extended RAM Target Register

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_RTR_type: 73h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**RTR:** Extended RAM Target Register

3.64 PCU iLB 8254 Timers IO Registers

Table 72. Summary of PCU iLB 8254 Timers I/O Registers—

Offset	Size	Register ID—Description	Default Value
40h	1	"C0TS—Offset 40h" on page 3210	00h
41h	1	"C1TS—Offset 41h" on page 3211	00h
42h	1	"C2TS—Offset 42h" on page 3212	00h
43h	1	"TCW—Offset 43h" on page 3212	00h
50h	1	"C0AP—Offset 50h" on page 3213	00h
51h	1	"C1AP—Offset 51h" on page 3213	00h
52h	1	"C2AP—Offset 52h" on page 3214	00h
61h	1	"NSC—Offset 61h" on page 3214	20h

3.64.1 C0TS—Offset 40h

Counter 0 Interval Time Status Byte Format.Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 0, the next read from this register returns the status byte.

Access Method

Type: I/O Register (Size: 8 bits)

C0TS: 40h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CS	CR	RWS		MD			CT

Bit Range	Default & Access	Description
7	0b RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB

Bit Range	Default & Access	Description
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

3.64.2 C1TS—Offset 41h

Counter 1 Interval Time Status Byte Format. Counter 1 Interval Time Status Byte Format. Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 1, the next read from this register returns the status byte.

Access Method

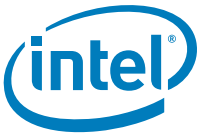
Type: I/O Register
(Size: 8 bits)

C1TS: 41h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CS	CR	RWS		MD			CT

Bit Range	Default & Access	Description
7	0b RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.



3.64.3 C2TS—Offset 42h

Counter 2 Interval Time Status Byte Format. Counter 2 Interval Time Status Byte Format. Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 2, the next read from this register returns the status byte.

Access Method

Type: I/O Register
(Size: 8 bits)

C2TS: 42h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CS	CR	RWS		MD			CT

Bit Range	Default & Access	Description
7	0b RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

3.64.4 TCW—Offset 43h

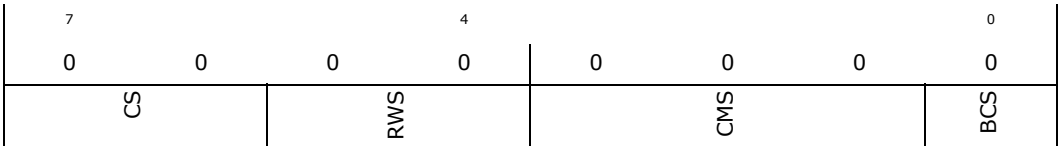
Timer Control Word Register. This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

Access Method

Type: I/O Register
(Size: 8 bits)

TCW: 43h

Default: 00h



Bit Range	Default & Access	Description
7:6	X WO	**CS:** Counter Select (CS): The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1 00 Counter 0 select 01 Counter 1 select 10 Counter 2 select 11 Read Back Command
5:4	X WO	**RWS:** Read/Write Select RWS): The counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2) 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X WO	**CMS:** Counter Mode Selection (CMS): Selects one of six modes of operation for the selected counter. 000 = Out signal on end of count (=0) 001 = Hardware retriggerable one-shot x10 = Rate generator (divide by n counter) x11 = Square wave output 100 = Software triggered strobe 101 = Hardware triggered strobe
0	X WO	**BCS:** Binary/BCD Countdown Select (BCS): 0 Binary countdown is used. The largest possible binary count is 216 1 Binary coded decimal (BCD) count is used. The largest possible BCD count is 104

3.64.5 C0AP—Offset 50h

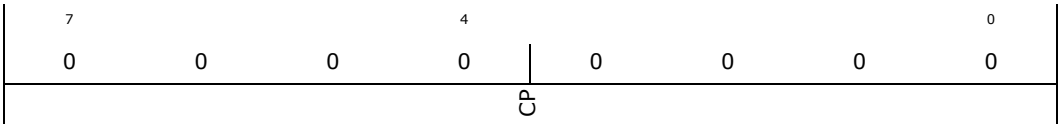
Counter 0 Counter Access Port Register

Access Method

Type: I/O Register (Size: 8 bits)

C0AP: 50h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

3.64.6 C1AP—Offset 51h

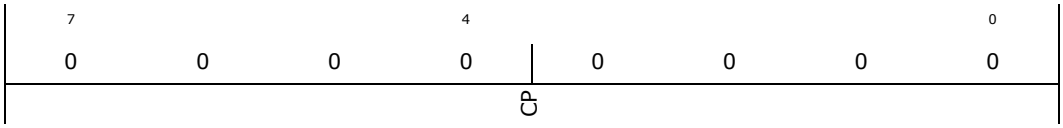
Counter 1 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

C1AP: 51h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

3.64.7 C2AP—Offset 52h

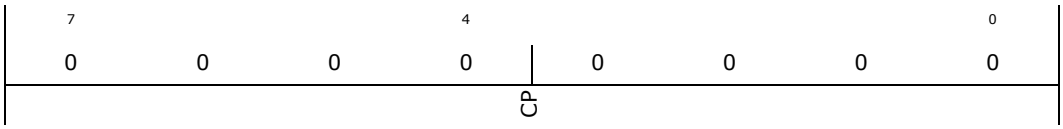
Counter 2 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

C2AP: 52h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

3.64.8 NSC—Offset 61h

NMI Status and Control

Access Method

Type: I/O Register
(Size: 8 bits)

NSC: 61h

Default: 20h

7			4				0
0	0	1	0	0	0	0	0
SNS	INS	T2S	RTS	INE	SNE	SDE	TC2E

Bit Range	Default & Access	Description
7	0b RO	**SNS:** SERR# NMI Status (SNS): Set on errors from a PCIe port or internal functions that generate SERR#. SNE in this register must be cleared in order for this bit to be set. To reset the interrupt, set bit 2 to 1 and then set it to 0.
6	0b RO	**INS:** IOCHK NMI Status (INS): Set when SERIRQ asserts IOCHK# and INE in this register is cleared. To reset the interrupt, set bit 3 to 1 and then set it to 0.
5	1b RO	**RTS (T2S):** Timer Counter 2 Status (T2S): Reflects the current state of the 8254 counter 2 outputs. Counter 2 must be programmed for this bit to have a determinate value.
4	0b RO	**RTS:** Refresh Cycle Toggle Status (RTS): Reflects the current state of 8254 counter 1
3	X RW	**INE:** IOCHK NMI Enable (INE): When set, IOCHK# NMIs are disabled. When cleared, IOCHK# NMIs are enabled.
2	0b RW	**SNE:** SERR# NMI Enable (SNE): When set, SERR# NMIs are disabled. When cleared, SERR# NMIs are enabled.
1	0b RW	**SDE:** Speaker Data Enable (SDE): When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0b RW	**TC2E:** Timer Counter 2 Enable (TC2E): When cleared, counter 2 counting is disabled. When set, counting is enabled.

3.65 PCU iLB High Performance Event Timer (HPET) Memory Mapped IO Registers

Table 73. Summary of PCU iLB High Performance Event Timer (HPET) Memory Mapped I/O Registers—

Offset	Size	Register ID—Description	Default Value
FED00000h	8	"GCID (HPET_GCID)—Offset FED00000h" on page 3216	0429B17F8086A201h
FED00010h	8	"GCFG (HPET_GCFG)—Offset FED00010h" on page 3217	0000000000000000h
FED00020h	8	"GIS (HPET_GIS)—Offset FED00020h" on page 3217	0000000000000000h
FED000F0h	8	"MCV (HPET_MCV)—Offset FED000F0h" on page 3218	0000000000000000h
FED00100h	8	"T0C (HPET_T0C)—Offset FED00100h" on page 3218	00F0000000000030h
FED00108h	4	"T0CV_L (HPET_T0CV_L)—Offset FED00108h" on page 3220	FFFFFFFFh
FED0010Ch	4	"T0CV_U (HPET_T0CV_U)—Offset FED0010Ch" on page 3220	FFFFFFFFh
FED00120h	8	"T1C (HPET_T1C)—Offset FED00120h" on page 3221	00F0000000000000h
FED00128h	8	"T1CV (HPET_T1CV)—Offset FED00128h" on page 3222	00000000FFFFFFFFh
FED00140h	8	"T2C (HPET_T2C)—Offset FED00140h" on page 3222	00F0080000000000h
FED00148h	8	"T2CV (HPET_T2CV)—Offset FED00148h" on page 3224	00000000FFFFFFFFh

3.65.1 GCID (HPET_GCID)—Offset FED00000h

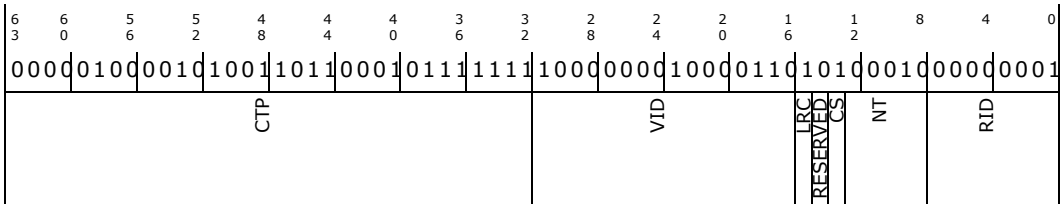
General Capabilities and ID

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_GCID: FED00000h

Default: 0429B17F8086A201h



Bit Range	Default & Access	Description
63:32	0429B17Fh RO	**CTP:** Counter Tick Period (CTP): Indicates a period of 69.841279ns, (14.1318 MHz clock period)

Bit Range	Default & Access	Description
31:16	8086h RO	**VID:** Vendor ID (VID): Value of 8086h indicates Intel.
15	1b RO	**LRC:** Legacy Rout Capable (LRC): Indicates support for Legacy Interrupt Rout.
14	0b RO	**RESERVED:** Reserved.
13	1b RO	**CS:** Counter Size (CS): This bit is set to indicate that the main counter is 64 bits wide.
12:8	02h RO	**NT:** Number of Timers (NT): Indicates that 3 timers are supported.
7:0	01h RO	**RID:** Revision ID (RID): Indicates that revision 1.0 of the specification is implemented.

3.65.2 GCFG (HPET_GCFG)—Offset FED00010h

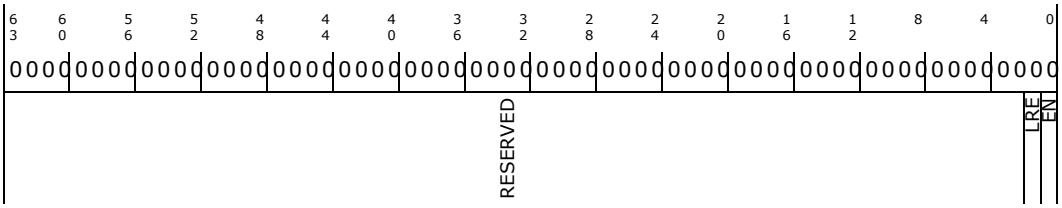
General Configuration

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_GCFG: FED00010h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RESERVED:** Reserved.
1	0b RW	**LRE:** Legacy Rout Enable (LRE): When set, interrupts will be routed as follows: Timer 0 will be routed to IRQ0 in 8259 or IRQ2 in the I/O APIC Timer 1 will be routed to IRQ8 in 8259 and I/O APIC Timer 2 will be routed as per the routing in T2C When set, the T[1:0]C.IR will have no impact for timers 0 and 1.
0	0b RW	**EN:** Overall Enable (EN): When set, the timers can generate interrupts. When cleared, the main counter will halt and no interrupts will be caused by any timer. For level-triggered interrupts, if an interrupt is pending when this bit is cleared, the GIS.Tx will not be cleared.

3.65.3 GIS (HPET_GIS)—Offset FED00020h

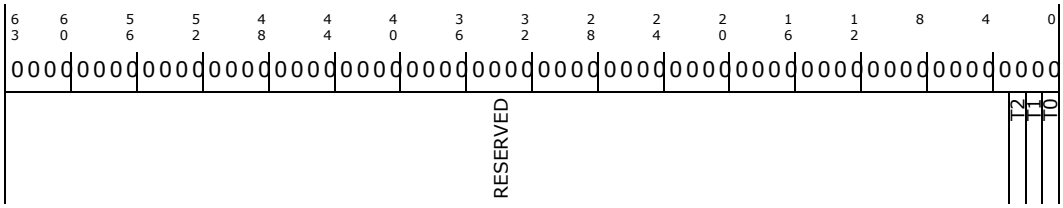
General Interrupt Status

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_GIS: FED00020h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:3	0b RO	**RESERVED:** Reserved.
2	0b RW	**T2:** Timer 2 Status (T2): Same functionality as T0, for timer 2.
1	0b RW	**T1:** Timer 1 Status (T1): Same functionality as T0, for timer 1.
0	0b RW	**T0:** Timer 0 Status (T0): In edge triggered mode, this bit always reads as 0. In level triggered mode, this bit is set when an interrupt is active.

3.65.4 MCV (HPET_MCV)—Offset FED000F0h

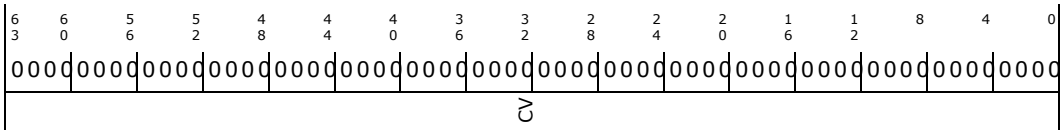
Main Counter Value

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_MCV: FED000F0h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:0	0b RW	**CV:** Counter Value (CV): Reads return the current value of the counter. Writes load the new value to the counter. Timers 1 and 2 return 0 for the upper 32-bits of this register.

3.65.5 T0C (HPET_T0C)—Offset FED00100h

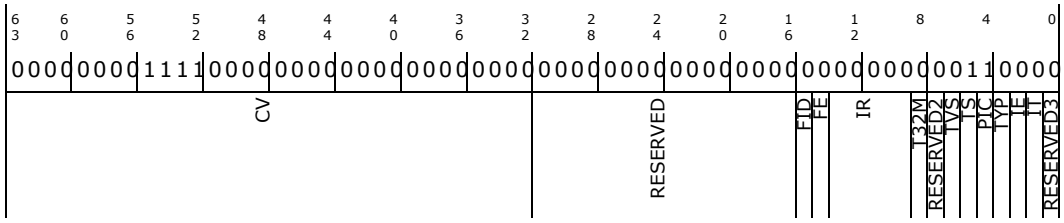
Timer 0 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T0C: FED00100h

Default: 00F0000000000030h



Bit Range	Default & Access	Description
63:32	00f00000h RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0h RO	**RESERVED:** Reserved.
15	0b RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0b RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0b RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this particular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0b RW	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0b RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0b RW	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	1b RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	1b RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0b RW	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0b RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.

Bit Range	Default & Access	Description
1	0b RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0b RO	**RESERVED (RESERVED3):** Reserved.

3.65.6 T0CV_L (HPET_T0CV_L)—Offset FED00108h

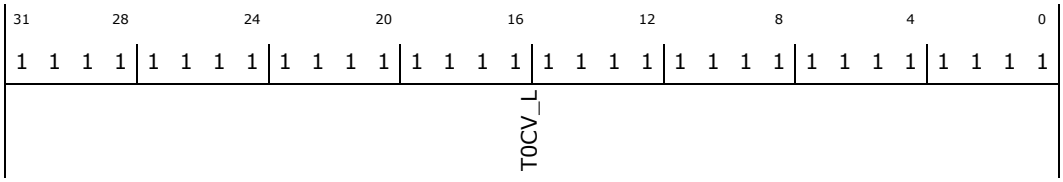
Lower Timer 0 Comparator Value

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HPET_T0CV_L: FED00108h

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW	**T0CV_L:** Lower Timer 0 Comparator Value

3.65.7 T0CV_U (HPET_T0CV_U)—Offset FED0010Ch

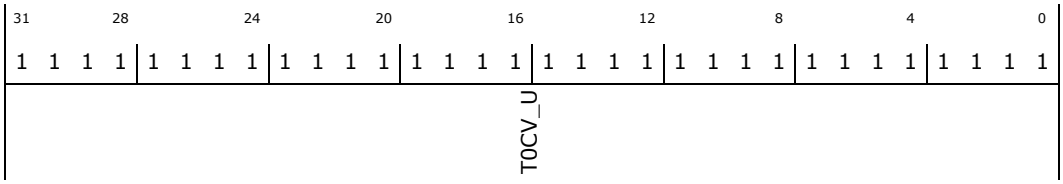
Upper Timer 0 Comparator Value

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HPET_T0CV_U: FED0010Ch

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW	**T0CV_U:** Upper Timer 0 Comparator Value

3.65.8 T1C (HPET_T1C)—Offset FED00120h

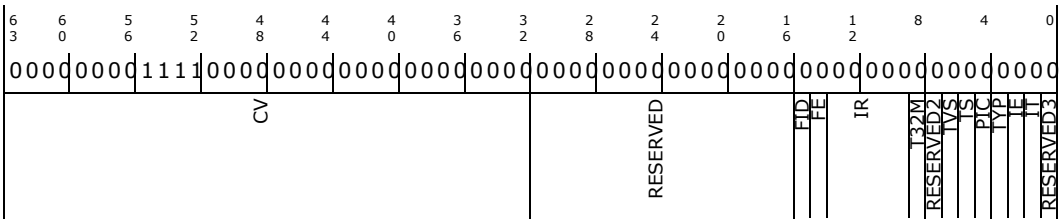
Timer 1 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T1C: FED00120h

Default: 00F0000000000000h



Bit Range	Default & Access	Description
63:32	00f00000h RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0h RO	**RESERVED:** Reserved.
15	0b RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0b RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0b RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this particular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0b RO	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0b RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0b RO	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	0b RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	0b RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0b RO	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.

Bit Range	Default & Access	Description
2	0b RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0b RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0b RO	**RESERVED (RESERVED3):** Reserved.

3.65.9 T1CV (HPET_T1CV)—Offset FED00128h

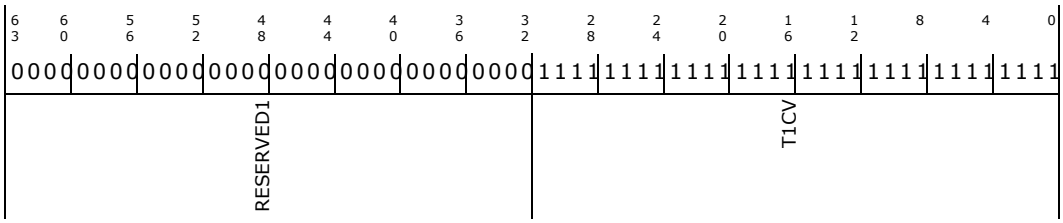
Timer 1 Comparator Value

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T1CV: FED00128h

Default: 00000000FFFFFFFFh



Bit Range	Default & Access	Description
63:32	0b RO	**RESERVED (RESERVED1):** Reserved.
31:0	FFFFFFFFh RO	**T1CV:** Timer 1 Comparator Value

3.65.10 T2C (HPET_T2C)—Offset FED00140h

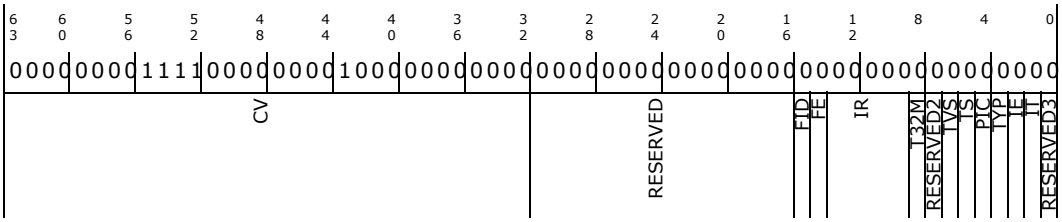
Timer 2 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T2C: FED00140h

Default: 00F0080000000000h



Bit Range	Default & Access	Description
63:32	00f00800h RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0h RO	**RESERVED:** Reserved.
15	0b RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0b RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0b RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this particular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0b RO	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0b RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0b RO	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	0b RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	0b RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0b RO	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0b RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0b RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0b RO	**RESERVED (RESERVED3):** Reserved.

3.65.11 T2CV (HPET_T2CV)—Offset FED00148h

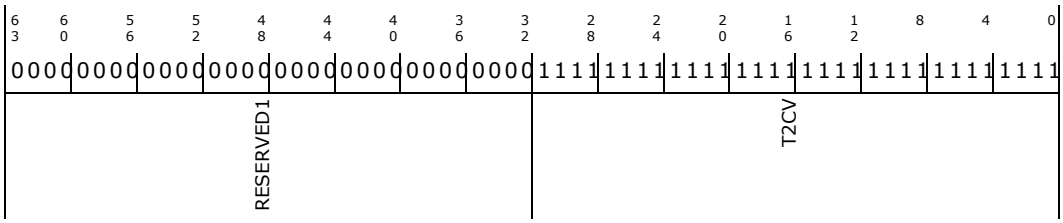
Timer 2 Comparator Value

Access Method

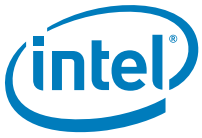
Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T2CV: FED00148h

Default: 00000000FFFFFFFFh



Bit Range	Default & Access	Description
63:32	0b RO	**RESERVED (RESERVED1):** Reserved.
31:0	FFFFFFFFh RO	**T2CV:** Timer 2 Comparator Value



3.66 PCU iLB GPIO CFIO_SCORE_IO Address Map

Table 74. Summary of PCU iLB GPIO IO Registers—GPIO_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"South Core Use Select 1 (cfio_ioreg_SC_USE_SEL_31_0_)—Offset 0h" on page 3226	00000000h
4h	4	"South Core Io Select 1 (cfio_ioreg_SC_IO_SEL_31_0_)—Offset 4h" on page 3227	00000000h
8h	4	"South Core Gpio Level 1 (cfio_ioreg_SC_GP_LVL_31_0_)—Offset 8h" on page 3227	00000000h
Ch	4	"South Core Trigger Positive Edge Enable 1 (cfio_ioreg_SC_TPE_31_0_)—Offset Ch" on page 3228	00000000h
10h	4	"South Core Trigger Negative Enable 1 (cfio_ioreg_SC_TNE_31_0_)—Offset 10h" on page 3229	00000000h
14h	4	"South Core Trigger Status 1 (cfio_ioreg_SC_TS_31_0_)—Offset 14h" on page 3229	00000000h
20h	4	"South Core Use Select 2 (cfio_ioreg_SC_USE_SEL_63_32_)—Offset 20h" on page 3230	00000000h
24h	4	"South Core Io Select 2 (cfio_ioreg_SC_IO_SEL_63_32_)—Offset 24h" on page 3231	00000000h
28h	4	"South Core Gpio Level 2 (cfio_ioreg_SC_GP_LVL_63_32_)—Offset 28h" on page 3231	00000000h
2Ch	4	"South Core Trigger Positive Edge Enable 2 (cfio_ioreg_SC_TPE_63_32_)—Offset 2Ch" on page 3232	00000000h
30h	4	"South Core Trigger Negative Enable 2 (cfio_ioreg_SC_TNE_63_32_)—Offset 30h" on page 3233	00000000h
34h	4	"South Core Trigger Status 2 (cfio_ioreg_SC_TS_63_32_)—Offset 34h" on page 3233	00000000h
40h	4	"South Core Use Select 3 (cfio_ioreg_SC_USE_SEL_95_64_)—Offset 40h" on page 3234	00000000h
44h	4	"South Core Io Select 3 (cfio_ioreg_SC_IO_SEL_95_64_)—Offset 44h" on page 3235	00000000h
48h	4	"South Core Gpio Level 3 (cfio_ioreg_SC_GP_LVL_95_64_)—Offset 48h" on page 3235	00000000h
4Ch	4	"South Core Trigger Positive Edge Enable 3 (cfio_ioreg_SC_TPE_95_64_)—Offset 4Ch" on page 3236	00000000h
50h	4	"South Core Trigger Negative Enable 3 (cfio_ioreg_SC_TNE_95_64_)—Offset 50h" on page 3237	00000000h
54h	4	"South Core Trigger Status 3 (cfio_ioreg_SC_TS_95_64_)—Offset 54h" on page 3237	00000000h
60h	4	"South Core Use Select 4 (cfio_ioreg_SC_USE_SEL_127_96_)—Offset 60h" on page 3238	00000000h
64h	4	"South Core Io Select 4 (cfio_ioreg_SC_IO_SEL_127_96_)—Offset 64h" on page 3239	00000000h

Table 74. Summary of PCU iLB GPIO IO Registers—GPIO_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
68h	4	"South Core Gpio Level 4 (cfio_ioreg_SC_GP_LVL_127_96_)—Offset 68h" on page 3239	00000000h
6Ch	4	"South Core Trigger Positive Edge Enable 4 (cfio_ioreg_SC_TPE_127_96_)—Offset 6Ch" on page 3240	00000000h
70h	4	"South Core Trigger Negative Enable 4 (cfio_ioreg_SC_TNE_127_96_)—Offset 70h" on page 3241	00000000h
74h	4	"South Core Trigger Status 4 (cfio_ioreg_SC_TS_127_96_)—Offset 74h" on page 3241	00000000h

3.66.1 South Core Use Select 1 (cfio_ioreg_SC_USE_SEL_31_0_)—Offset 0h

Access via PCU proxy, the register is setting the corresponding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[0], and bit 1 will set GPIO[1] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

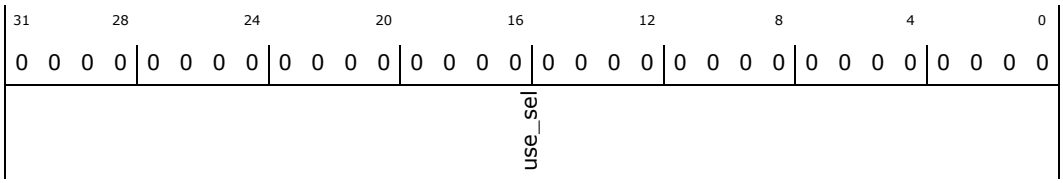
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_USE_SEL_31_0_: [GBASE] + 0h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000b RW	**Use Select (use_sel):** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

3.66.2 South Core Io Select 1 (cfio_ioreg_SC_IO_SEL_31_0_)—Offset 4h

Access via PCU proxy, define the Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

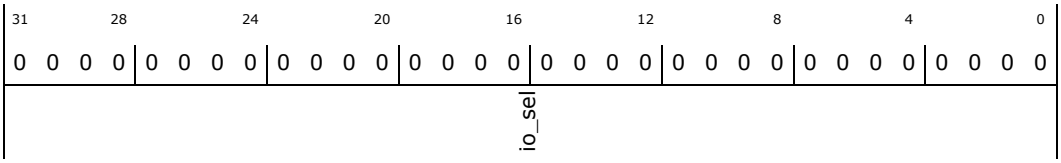
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_IO_SEL_31_0_: [GBASE] + 4h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Io Select (io_sel):** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

3.66.3 South Core Gpio Level 1 (cfio_ioreg_SC_GP_LVL_31_0_)—Offset 8h

Access via PCU proxy, the registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

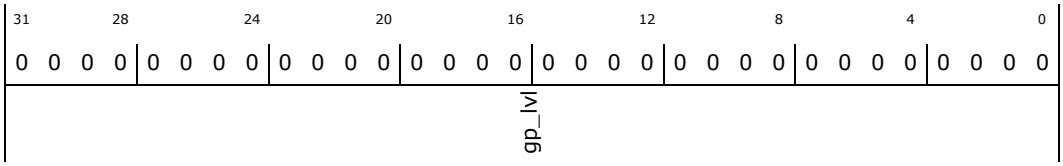
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_GP_LVL_31_0_: [GBASE] + 8h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b WO	**Gpio Level (gp_lvl):** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

3.66.4 South Core Trigger Positive Edge Enable 1 (cfio_ioreg_SC_TPE_31_0_)—Offset Ch

Access via PCU proxy, it is trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

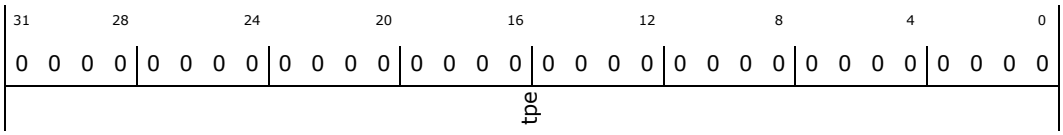
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TPE_31_0_: [GBASE] + Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Tpe (tpe):** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

3.66.5 South Core Trigger Negative Enable 1 (cfio_ioreg_SC_TNE_31_0_)—Offset 10h

Trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

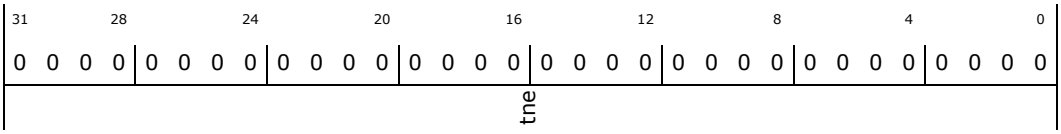
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TNE_31_0_: [GBASE] + 10h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Tne (tne):** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

3.66.6 South Core Trigger Status 1 (cfio_ioreg_SC_TS_31_0_)—Offset 14h

Access via PCU proxy, when set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV and it cannot be tested by the host

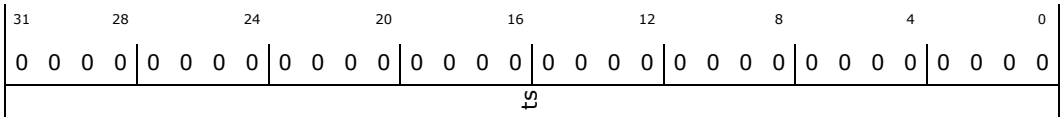
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TS_31_0_: [GBASE] + 14h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b WOC	**ts:** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

3.66.7 South Core Use Select 2 (cfio_ioreg_SC_USE_SEL_63_32_)—Offset 20h

Access via PCU proxy, the register is setting the corresponding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[32], and bit 1 will set GPIO[33] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

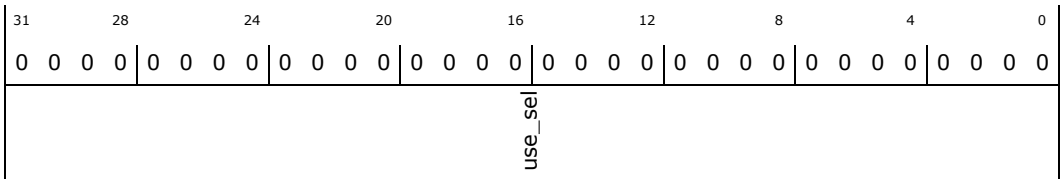
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_USE_SEL_63_32_: [GBASE] + 20h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Use Select (use_sel):** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

3.66.8 South Core Io Select 2 (cfio_ioreg_SC_IO_SEL_63_32_)—Offset 24h

Access via PCU proxy, define the Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

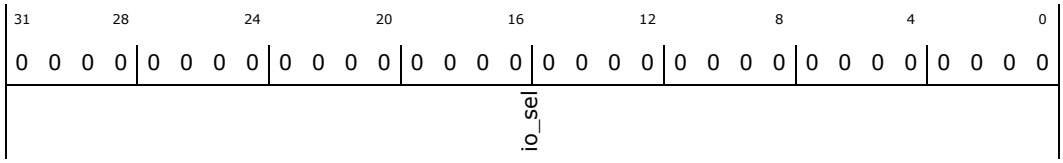
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_IO_SEL_63_32_: [GBASE] + 24h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Io Select (io_sel):** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

3.66.9 South Core Gpio Level 2 (cfio_ioreg_SC_GP_LVL_63_32_)—Offset 28h

Access via PCU proxy, the registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

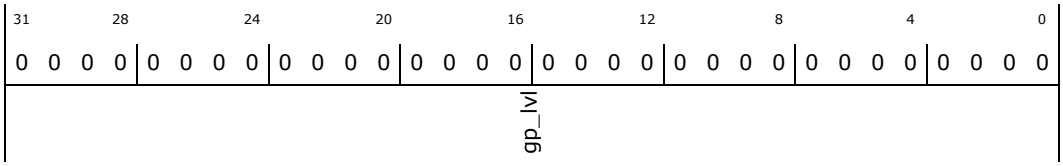
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_GP_LVL_63_32_: [GBASE] + 28h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b WO	**Gpio Level (gp_lvl):** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

3.66.10 South Core Trigger Positive Edge Enable 2 (cfio_ioreg_SC_TPE_63_32_)—Offset 2Ch

Access via PCU proxy, the register trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

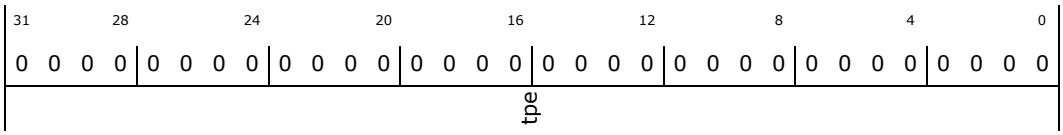
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TPE_63_32_: [GBASE] + 2Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Tpe (tpe):** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

3.66.11 South Core Trigger Negative Enable 2 (cfio_ioreg_SC_TNE_63_32_)—Offset 30h

Access via PCU proxy, the register trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

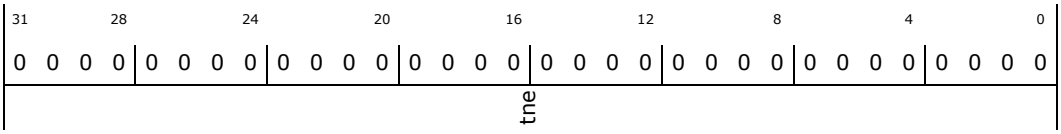
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TNE_63_32_: [GBASE] + 30h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Tne (tne):** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

3.66.12 South Core Trigger Status 2 (cfio_ioreg_SC_TS_63_32_)—Offset 34h

When set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV

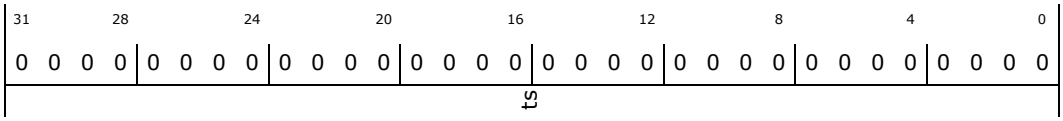
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TS_63_32_: [GBASE] + 34h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b WOC	**ts:** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

3.66.13 South Core Use Select 3 (cfio_ioreg_SC_USE_SEL_95_64_)—Offset 40h

Access via PCU proxy, the register is setting the corresponding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[0], and bit 1 will set GPIO[1] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

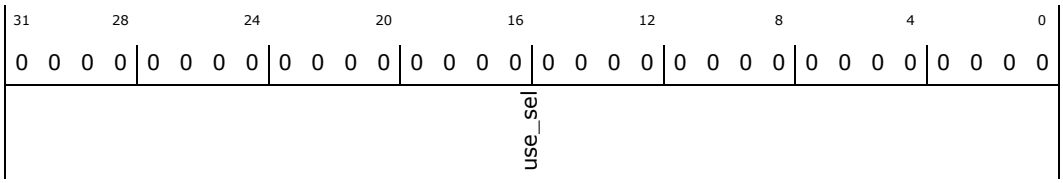
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_USE_SEL_95_64_: [GBASE] + 40h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Use Select (use_sel):** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

3.66.14 South Core Io Select 3 (cfio_ioreg_SC_IO_SEL_95_64_)—Offset 44h

Access via PCU proxy, it defines Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

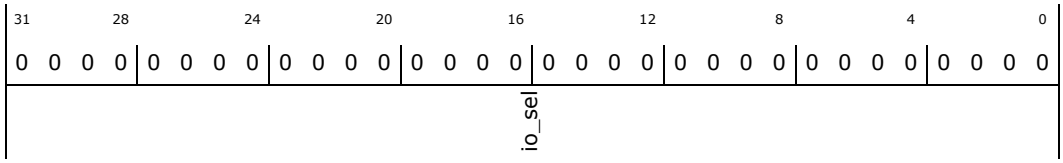
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_IO_SEL_95_64_: [GBASE] + 44h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Io Select (io_sel):** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

3.66.15 South Core Gpio Level 3 (cfio_ioreg_SC_GP_LVL_95_64_)—Offset 48h

This registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

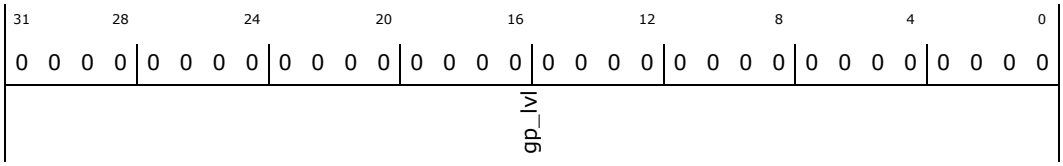
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_GP_LVL_95_64_: [GBASE] + 48h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b WO	**Gpio Level (gp_lvl):** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

3.66.16 South Core Trigger Positive Edge Enable 3 (cfio_ioreg_SC_TPE_95_64_)—Offset 4Ch

Access via PCU proxy, the register trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

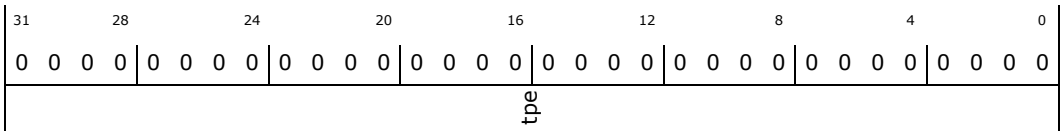
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TPE_95_64_: [GBASE] + 4Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Tpe (tpe):** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

3.66.17 South Core Trigger Negative Enable 3 (cfio_ioreg_SC_TNE_95_64_)—Offset 50h

Access via PCU proxy, the register trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

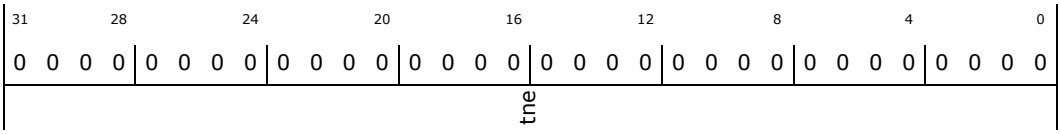
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TNE_95_64_: [GBASE] + 50h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b RW	**Tne (tne):** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

3.66.18 South Core Trigger Status 3 (cfio_ioreg_SC_TS_95_64_)—Offset 54h

When set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV

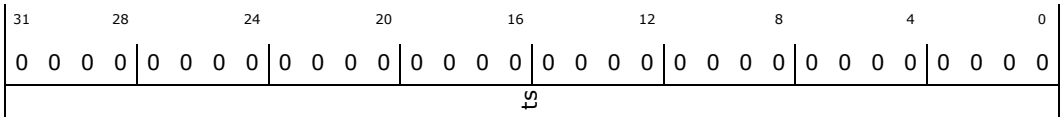
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TS_95_64_: [GBASE] + 54h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000000000000000000000000000b WOC	**ts:** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

3.66.19 South Core Use Select 4 (cfio_ioreg_SC_USE_SEL_127_96_)—Offset 60h

Access via PCU proxy, the register is setting the corresponding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[0], and bit 1 will set GPIO[1] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

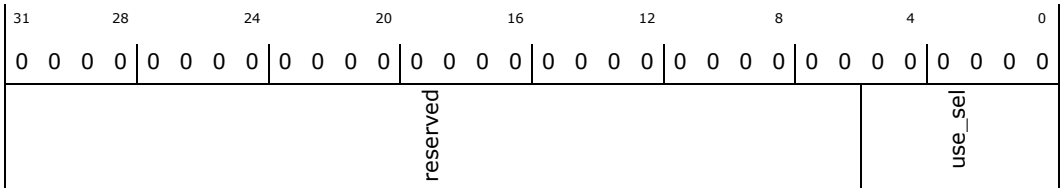
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_USE_SEL_127_96_: [GBASE] + 60h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	00000000000000000000000000b RO	**Reserved (reserved):** reserved
5:0	0b RW	**Use Select (use_sel):** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

3.66.20 South Core Io Select 4 (cfio_ioreg_SC_IO_SEL_127_96_)—Offset 64h

Access via PCU proxy, it defines Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

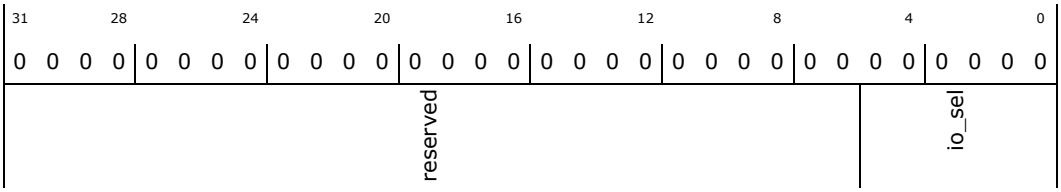
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_IO_SEL_127_96_: [GBASE] + 64h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	00000000 00000000 00000000b RO	**Reserved (reserved):** reserved
5:0	0b RW	**Io Select (io_sel):** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

3.66.21 South Core Gpio Level 4 (cfio_ioreg_SC_GP_LVL_127_96_)—Offset 68h

This registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

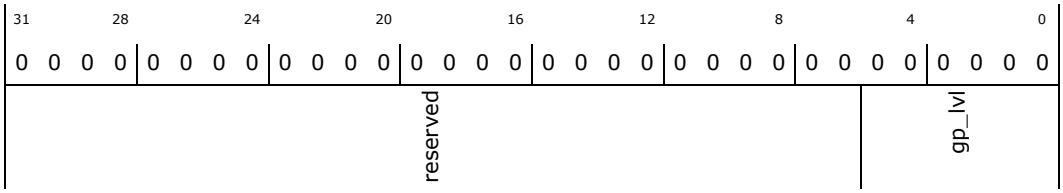
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_GP_LVL_127_96_: [GBASE] + 68h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	000000000 000000000 00000000b RO	**Reserved (reserved):** reserved
5:0	0b RW	**Gpio Level (gp_lvl):** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

3.66.22 South Core Trigger Positive Edge Enable 4 (cfio_ioreg_SC_TPE_127_96_)—Offset 6Ch

Access via PCU proxy, the register trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

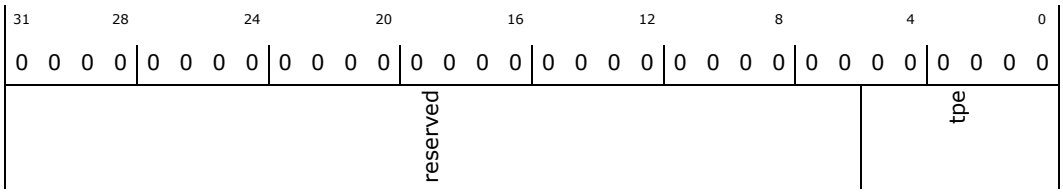
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TPE_127_96_: [GBASE] + 6Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	000000000 000000000 00000000b RO	**Reserved (reserved):** reserved
5:0	0b RW	**Tpe (tpe):** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

3.66.23 South Core Trigger Negative Enable 4 (cfio_ioreg_SC_TNE_127_96_)—Offset 70h

Access via PCU proxy, the register trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

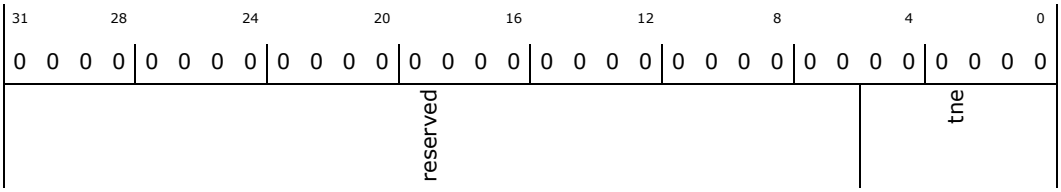
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SC_TNE_127_96_: [GBASE] + 70h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	00000000 00000000 00000000b RO	**Reserved (reserved):** reserved
5:0	0b RW	**Tne (tne):** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

3.66.24 South Core Trigger Status 4 (cfio_ioreg_SC_TS_127_96_)—Offset 74h

When set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV

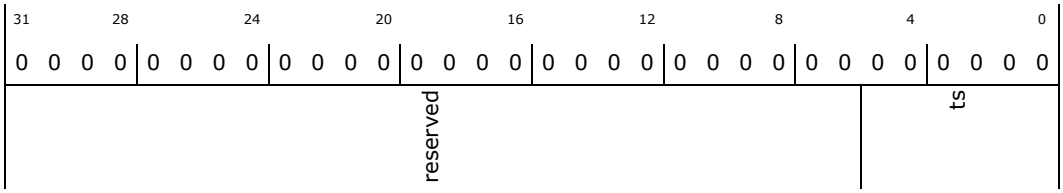
Access Method

Type: I/O Register (Size: 32 bits)

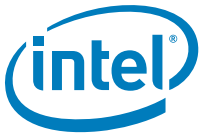
cfio_ioreg_SC_TS_127_96_: [GBASE] + 74h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	00000000 00000000 00000000b RO	**Reserved (reserved):** reserved
5:0	0b WOC	**ts:** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0



3.67 PCU iLB GPIO CFIO_SCORE Address Map

Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"Uart1 Rts B Pad Configuration (cfio_regs_pad_uart1_rts_b_PCONF0)—Offset 0h" on page 3266	2003CC80h
4h	4	"Uart1 Rts B Delay Line Multiplexer (cfio_regs_pad_uart1_rts_b_PCONF1)—Offset 4h" on page 3268	00008000h
8h	4	"Uart1 Rts B Pad Value (cfio_regs_pad_uart1_rts_b_PAD_VAL)—Offset 8h" on page 3269	00000002h
10h	4	"Uart1 Txd Pad Configuration (cfio_regs_pad_uart1_txd_PCONF0)—Offset 10h" on page 3270	2003CC80h
14h	4	"Uart1 Txd Delay Line Multiplexer (cfio_regs_pad_uart1_txd_PCONF1)—Offset 14h" on page 3271	00008000h
18h	4	"Uart1 Txd Pad Value (cfio_regs_pad_uart1_txd_PAD_VAL)—Offset 18h" on page 3272	00000002h
20h	4	"Uart1 Rxd Pad Configuration (cfio_regs_pad_uart1_rxd_PCONF0)—Offset 20h" on page 3273	2003CC80h
24h	4	"Uart1 Rxd Delay Line Multiplexer (cfio_regs_pad_uart1_rxd_PCONF1)—Offset 24h" on page 3275	00008000h
28h	4	"Uart1 Rxd Pad Value (cfio_regs_pad_uart1_rxd_PAD_VAL)—Offset 28h" on page 3276	00000002h
30h	4	"I2c Nfc Scl Pad Configuration (cfio_regs_pad_i2c_nfc_scl_PCONF0)—Offset 30h" on page 3276	2003CC80h
34h	4	"I2c Nfc Scl Delay Line Multiplexer (cfio_regs_pad_i2c_nfc_scl_PCONF1)—Offset 34h" on page 3278	00008000h
38h	4	"I2c Nfc Scl Pad Value (cfio_regs_pad_i2c_nfc_scl_PAD_VAL)—Offset 38h" on page 3279	00000002h
40h	4	"Uart1 Cts B Pad Configuration (cfio_regs_pad_uart1_cts_b_PCONF0)—Offset 40h" on page 3280	2003CC80h
44h	4	"Uart1 Cts B Delay Line Multiplexer (cfio_regs_pad_uart1_cts_b_PCONF1)—Offset 44h" on page 3281	00008000h
48h	4	"Uart1 Cts B Pad Value (cfio_regs_pad_uart1_cts_b_PAD_VAL)—Offset 48h" on page 3282	00000002h
50h	4	"I2c Nfc Sda Pad Configuration (cfio_regs_pad_i2c_nfc_sda_PCONF0)—Offset 50h" on page 3283	2003CC80h
54h	4	"I2c Nfc Sda Delay Line Multiplexer (cfio_regs_pad_i2c_nfc_sda_PCONF1)—Offset 54h" on page 3285	00008000h
58h	4	"I2c Nfc Sda Pad Value (cfio_regs_pad_i2c_nfc_sda_PAD_VAL)—Offset 58h" on page 3286	00000002h
60h	4	"Uart2 Rxd Pad Configuration (cfio_regs_pad_uart2_rxd_PCONF0)—Offset 60h" on page 3286	2003CC80h

Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
64h	4	"Uart2 Rxd Delay Line Multiplexer (cfio_regs_pad_uart2_rxd_PCONF1)—Offset 64h" on page 3288	00008000h
68h	4	"Uart2 Rxd Pad Value (cfio_regs_pad_uart2_rxd_PAD_VAL)—Offset 68h" on page 3289	00000002h
70h	4	"Uart2 Txd Pad Configuration (cfio_regs_pad_uart2_txd_PCONF0)—Offset 70h" on page 3290	2003CC80h
74h	4	"Uart2 Txd Delay Line Multiplexer (cfio_regs_pad_uart2_txd_PCONF1)—Offset 74h" on page 3291	00008000h
78h	4	"Uart2 Txd Pad Value (cfio_regs_pad_uart2_txd_PAD_VAL)—Offset 78h" on page 3292	00000002h
80h	4	"Uart2 Cts B Pad Configuration (cfio_regs_pad_uart2_cts_b_PCONF0)—Offset 80h" on page 3293	2003CC80h
84h	4	"Uart2 Cts B Delay Line Multiplexer (cfio_regs_pad_uart2_cts_b_PCONF1)—Offset 84h" on page 3295	00008000h
88h	4	"Uart2 Cts B Pad Value (cfio_regs_pad_uart2_cts_b_PAD_VAL)—Offset 88h" on page 3296	00000002h
90h	4	"Uart2 Rts B Pad Configuration (cfio_regs_pad_uart2_rts_b_PCONF0)—Offset 90h" on page 3296	2003CC80h
94h	4	"Uart2 Rts B Delay Line Multiplexer (cfio_regs_pad_uart2_rts_b_PCONF1)—Offset 94h" on page 3298	00008000h
98h	4	"Uart2 Rts B Pad Value (cfio_regs_pad_uart2_rts_b_PAD_VAL)—Offset 98h" on page 3299	00000002h
A0h	4	"Pwm0 Pad Configuration (cfio_regs_pad_pwm0_PCONF0)—Offset A0h" on page 3300	2003CD00h
A4h	4	"Pwm0 Delay Line Multiplexer (cfio_regs_pad_pwm0_PCONF1)—Offset A4h" on page 3301	00008000h
A8h	4	"Pwm0 Pad Value (cfio_regs_pad_pwm0_PAD_VAL)—Offset A8h" on page 3302	00000002h
B0h	4	"Pwm1 Pad Configuration (cfio_regs_pad_pwm1_PCONF0)—Offset B0h" on page 3303	2003CD00h
B4h	4	"Pwm1 Delay Line Multiplexer (cfio_regs_pad_pwm1_PCONF1)—Offset B4h" on page 3305	00008000h
B8h	4	"Pwm1 Pad Value (cfio_regs_pad_pwm1_PAD_VAL)—Offset B8h" on page 3306	00000002h
C0h	4	"Gp Ssp 2 Fs Pad Configuration (cfio_regs_pad_gp_ssp_2_fs_PCONF0)—Offset C0h" on page 3306	2003CC80h
C4h	4	"Gp Ssp 2 Fs Delay Line Multiplexer (cfio_regs_pad_gp_ssp_2_fs_PCONF1)—Offset C4h" on page 3308	00008000h
C8h	4	"Gp Ssp 2 Fs Pad Value (cfio_regs_pad_gp_ssp_2_fs_PAD_VAL)—Offset C8h" on page 3309	00000002h
D0h	4	"Gp Ssp 2 Clk Pad Configuration (cfio_regs_pad_gp_ssp_2_clk_PCONF0)—Offset D0h" on page 3310	2003CD00h

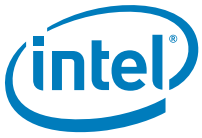


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
D4h	4	"Gp Ssp 2 Clk Delay Line Multiplexer (cfio_regs_pad_gp_ssp_2_clk_PCONF1)—Offset D4h" on page 3312	00008000h
D8h	4	"Gp Ssp 2 Clk Pad Value (cfio_regs_pad_gp_ssp_2_clk_PAD_VAL)—Offset D8h" on page 3312	00000002h
E0h	4	"Gp Ssp 2 Txd Pad Configuration (cfio_regs_pad_gp_ssp_2_txd_PCONF0)—Offset E0h" on page 3313	2003CC80h
E4h	4	"Gp Ssp 2 Txd Delay Line Multiplexer (cfio_regs_pad_gp_ssp_2_txd_PCONF1)—Offset E4h" on page 3315	00008000h
E8h	4	"Gp Ssp 2 Txd Pad Value (cfio_regs_pad_gp_ssp_2_txd_PAD_VAL)—Offset E8h" on page 3316	00000002h
F0h	4	"Gp Ssp 2 Rxd Pad Configuration (cfio_regs_pad_gp_ssp_2_rxd_PCONF0)—Offset F0h" on page 3317	2003CD00h
F4h	4	"Gp Ssp 2 Rxd Delay Line Multiplexer (cfio_regs_pad_gp_ssp_2_rxd_PCONF1)—Offset F4h" on page 3318	00008000h
F8h	4	"Gp Ssp 2 Rxd Pad Value (cfio_regs_pad_gp_ssp_2_rxd_PAD_VAL)—Offset F8h" on page 3319	00000002h
100h	4	"Spi1 Clk Pad Configuration (cfio_regs_pad_spi1_clk_PCONF0)—Offset 100h" on page 3320	2003CD00h
104h	4	"Spi1 Clk Delay Line Multiplexer (cfio_regs_pad_spi1_clk_PCONF1)—Offset 104h" on page 3322	00008000h
108h	4	"Spi1 Clk Pad Value (cfio_regs_pad_spi1_clk_PAD_VAL)—Offset 108h" on page 3323	00000002h
110h	4	"Spi1 Cs0 B Pad Configuration (cfio_regs_pad_spi1_cs0_b_PCONF0)—Offset 110h" on page 3323	2003CC80h
114h	4	"Spi1 Cs0 B Delay Line Multiplexer (cfio_regs_pad_spi1_cs0_b_PCONF1)—Offset 114h" on page 3325	00008000h
118h	4	"Spi1 Cs0 B Pad Value (cfio_regs_pad_spi1_cs0_b_PAD_VAL)—Offset 118h" on page 3326	00000002h
120h	4	"Spi1 Miso Pad Configuration (cfio_regs_pad_spi1_miso_PCONF0)—Offset 120h" on page 3327	2003CC80h
124h	4	"Spi1 Miso Delay Line Multiplexer (cfio_regs_pad_spi1_miso_PCONF1)—Offset 124h" on page 3328	00008000h
128h	4	"Spi1 Miso Pad Value (cfio_regs_pad_spi1_miso_PAD_VAL)—Offset 128h" on page 3329	00000002h
130h	4	"Spi1 Mosi Pad Configuration (cfio_regs_pad_spi1_mosi_PCONF0)—Offset 130h" on page 3330	2003CC80h
134h	4	"Spi1 Mosi Delay Line Multiplexer (cfio_regs_pad_spi1_mosi_PCONF1)—Offset 134h" on page 3332	00008000h
138h	4	"Spi1 Mosi Pad Value (cfio_regs_pad_spi1_mosi_PAD_VAL)—Offset 138h" on page 3333	00000002h
140h	4	"I2c5 Scl Pad Configuration (cfio_regs_pad_i2c5_scl_PCONF0)—Offset 140h" on page 3333	2003CC80h

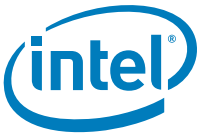


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
144h	4	"I2c5 Scl Delay Line Multiplexer (cfio_regs_pad_i2c5_scl_PCONF1)—Offset 144h" on page 3335	00008000h
148h	4	"I2c5 Scl Pad Value (cfio_regs_pad_i2c5_scl_PAD_VAL)—Offset 148h" on page 3336	00000002h
150h	4	"I2c5 Sda Pad Configuration (cfio_regs_pad_i2c5_sda_PCONF0)—Offset 150h" on page 3337	2003CC80h
154h	4	"I2c5 Sda Delay Line Multiplexer (cfio_regs_pad_i2c5_sda_PCONF1)—Offset 154h" on page 3338	00008000h
158h	4	"I2c5 Sda Pad Value (cfio_regs_pad_i2c5_sda_PAD_VAL)—Offset 158h" on page 3339	00000002h
160h	4	"I2c6 Scl Pad Configuration (cfio_regs_pad_i2c6_scl_PCONF0)—Offset 160h" on page 3340	2003CC80h
164h	4	"I2c6 Scl Delay Line Multiplexer (cfio_regs_pad_i2c6_scl_PCONF1)—Offset 164h" on page 3342	00008000h
168h	4	"I2c6 Scl Pad Value (cfio_regs_pad_i2c6_scl_PAD_VAL)—Offset 168h" on page 3343	00000002h
170h	4	"I2c4 Scl Pad Configuration (cfio_regs_pad_i2c4_scl_PCONF0)—Offset 170h" on page 3343	2003CC80h
174h	4	"I2c4 Scl Delay Line Multiplexer (cfio_regs_pad_i2c4_scl_PCONF1)—Offset 174h" on page 3345	00008000h
178h	4	"I2c4 Scl Pad Value (cfio_regs_pad_i2c4_scl_PAD_VAL)—Offset 178h" on page 3346	00000002h
180h	4	"I2c6 Sda Pad Configuration (cfio_regs_pad_i2c6_sda_PCONF0)—Offset 180h" on page 3347	2003CC80h
184h	4	"I2c6 Sda Delay Line Multiplexer (cfio_regs_pad_i2c6_sda_PCONF1)—Offset 184h" on page 3348	00008000h
188h	4	"I2c6 Sda Pad Value (cfio_regs_pad_i2c6_sda_PAD_VAL)—Offset 188h" on page 3349	00000002h
190h	4	"I2c3 Sda Pad Configuration (cfio_regs_pad_i2c3_sda_PCONF0)—Offset 190h" on page 3350	2003CC80h
194h	4	"I2c3 Sda Delay Line Multiplexer (cfio_regs_pad_i2c3_sda_PCONF1)—Offset 194h" on page 3352	00008000h
198h	4	"I2c3 Sda Pad Value (cfio_regs_pad_i2c3_sda_PAD_VAL)—Offset 198h" on page 3353	00000002h
1A0h	4	"I2c4 Sda Pad Configuration (cfio_regs_pad_i2c4_sda_PCONF0)—Offset 1A0h" on page 3353	2003CC80h
1A4h	4	"I2c4 Sda Delay Line Multiplexer (cfio_regs_pad_i2c4_sda_PCONF1)—Offset 1A4h" on page 3355	00008000h
1A8h	4	"I2c4 Sda Pad Value (cfio_regs_pad_i2c4_sda_PAD_VAL)—Offset 1A8h" on page 3356	00000002h
1B0h	4	"I2c2 Scl Pad Configuration (cfio_regs_pad_i2c2_scl_PCONF0)—Offset 1B0h" on page 3357	2003CC80h

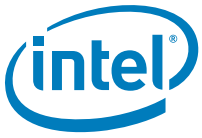


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
1B4h	4	"I2c2 Scl Delay Line Multiplexer (cfio_regs_pad_i2c2_scl_PCONF1)—Offset 1B4h" on page 3358	00008000h
1B8h	4	"I2c2 Scl Pad Value (cfio_regs_pad_i2c2_scl_PAD_VAL)—Offset 1B8h" on page 3359	00000002h
1C0h	4	"I2c3 Scl Pad Configuration (cfio_regs_pad_i2c3_scl_PCONF0)—Offset 1C0h" on page 3360	2003CC80h
1C4h	4	"I2c3 Scl Delay Line Multiplexer (cfio_regs_pad_i2c3_scl_PCONF1)—Offset 1C4h" on page 3362	00008000h
1C8h	4	"I2c3 Scl Pad Value (cfio_regs_pad_i2c3_scl_PAD_VAL)—Offset 1C8h" on page 3363	00000002h
1D0h	4	"I2c2 Sda Pad Configuration (cfio_regs_pad_i2c2_sda_PCONF0)—Offset 1D0h" on page 3363	2003CC80h
1D4h	4	"I2c2 Sda Delay Line Multiplexer (cfio_regs_pad_i2c2_sda_PCONF1)—Offset 1D4h" on page 3365	00008000h
1D8h	4	"I2c2 Sda Pad Value (cfio_regs_pad_i2c2_sda_PAD_VAL)—Offset 1D8h" on page 3366	00000002h
1E0h	4	"I2c1 Scl Pad Configuration (cfio_regs_pad_i2c1_scl_PCONF0)—Offset 1E0h" on page 3367	2003CC80h
1E4h	4	"I2c1 Scl Delay Line Multiplexer (cfio_regs_pad_i2c1_scl_PCONF1)—Offset 1E4h" on page 3368	00008000h
1E8h	4	"I2c1 Scl Pad Value (cfio_regs_pad_i2c1_scl_PAD_VAL)—Offset 1E8h" on page 3369	00000002h
1F0h	4	"I2c1 Sda Pad Configuration (cfio_regs_pad_i2c1_sda_PCONF0)—Offset 1F0h" on page 3370	2003CC80h
1F4h	4	"I2c1 Sda Delay Line Multiplexer (cfio_regs_pad_i2c1_sda_PCONF1)—Offset 1F4h" on page 3372	00008000h
1F8h	4	"I2c1 Sda Pad Value (cfio_regs_pad_i2c1_sda_PAD_VAL)—Offset 1F8h" on page 3373	00000002h
200h	4	"I2c0 Scl Pad Configuration (cfio_regs_pad_i2c0_scl_PCONF0)—Offset 200h" on page 3373	2003CC80h
204h	4	"I2c0 Scl Delay Line Multiplexer (cfio_regs_pad_i2c0_scl_PCONF1)—Offset 204h" on page 3375	00008000h
208h	4	"I2c0 Scl Pad Value (cfio_regs_pad_i2c0_scl_PAD_VAL)—Offset 208h" on page 3376	00000002h
210h	4	"I2c0 Sda Pad Configuration (cfio_regs_pad_i2c0_sda_PCONF0)—Offset 210h" on page 3377	2003CC80h
214h	4	"I2c0 Sda Delay Line Multiplexer (cfio_regs_pad_i2c0_sda_PCONF1)—Offset 214h" on page 3378	00008000h
218h	4	"I2c0 Sda Pad Value (cfio_regs_pad_i2c0_sda_PAD_VAL)—Offset 218h" on page 3379	00000002h
220h	4	"Hda Rstb Pad Configuration (cfio_regs_pad_hda_rstb_PCONF0)—Offset 220h" on page 3380	2003ED00h

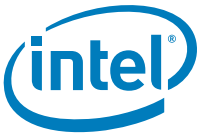


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
224h	4	"Hda Rstb Delay Line Multiplexer (cfio_regs_pad_hda_rstb_PCONF1)—Offset 224h" on page 3382	00008000h
228h	4	"Hda Rstb Pad Value (cfio_regs_pad_hda_rstb_PAD_VAL)—Offset 228h" on page 3383	00000002h
230h	4	"Hda Sdi1 Pad Configuration (cfio_regs_pad_hda_sdi1_PCONF0)—Offset 230h" on page 3383	2003ED00h
234h	4	"Hda Sdi1 Delay Line Multiplexer (cfio_regs_pad_hda_sdi1_PCONF1)—Offset 234h" on page 3385	00008000h
238h	4	"Hda Sdi1 Pad Value (cfio_regs_pad_hda_sdi1_PAD_VAL)—Offset 238h" on page 3386	00000002h
240h	4	"Hda Clk Pad Configuration (cfio_regs_pad_hda_clk_PCONF0)—Offset 240h" on page 3387	2003ED00h
244h	4	"Hda Clk Delay Line Multiplexer (cfio_regs_pad_hda_clk_PCONF1)—Offset 244h" on page 3388	00008000h
248h	4	"Hda Clk Pad Value (cfio_regs_pad_hda_clk_PAD_VAL)—Offset 248h" on page 3389	00000002h
250h	4	"Hda Sync Pad Configuration (cfio_regs_pad_hda_sync_PCONF0)—Offset 250h" on page 3390	2003ED00h
254h	4	"Hda Sync Delay Line Multiplexer (cfio_regs_pad_hda_sync_PCONF1)—Offset 254h" on page 3392	00008000h
258h	4	"Hda Sync Pad Value (cfio_regs_pad_hda_sync_PAD_VAL)—Offset 258h" on page 3393	00000002h
260h	4	"Hda Sdo Pad Configuration (cfio_regs_pad_hda_sdo_PCONF0)—Offset 260h" on page 3393	2003ED00h
264h	4	"Hda Sdo Delay Line Multiplexer (cfio_regs_pad_hda_sdo_PCONF1)—Offset 264h" on page 3395	00008000h
268h	4	"Hda Sdo Pad Value (cfio_regs_pad_hda_sdo_PAD_VAL)—Offset 268h" on page 3396	00000002h
270h	4	"Hda Sdi0 Pad Configuration (cfio_regs_pad_hda_sdi0_PCONF0)—Offset 270h" on page 3397	2003ED00h
274h	4	"Hda Sdi0 Delay Line Multiplexer (cfio_regs_pad_hda_sdi0_PCONF1)—Offset 274h" on page 3399	00008000h
278h	4	"Hda Sdi0 Pad Value (cfio_regs_pad_hda_sdi0_PAD_VAL)—Offset 278h" on page 3399	00000002h
280h	4	"Hda Dockrstb Pad Configuration (cfio_regs_pad_hda_dockrstb_PCONF0)—Offset 280h" on page 3400	2003ED00h
284h	4	"Hda Dockrstb Delay Line Multiplexer (cfio_regs_pad_hda_dockrstb_PCONF1)—Offset 284h" on page 3402	00008000h
288h	4	"Hda Dockrstb Pad Value (cfio_regs_pad_hda_dockrstb_PAD_VAL)—Offset 288h" on page 3403	00000002h
290h	4	"Sdmmc3 D1 Pad Configuration (cfio_regs_pad_sdmmc3_d1_PCONF0)—Offset 290h" on page 3404	20038C80h

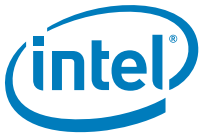


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
294h	4	"Sdmmc3 D1 Delay Line Multiplexer (cfio_regs_pad_sdmmc3_d1_PCONF1)—Offset 294h" on page 3406	00008000h
298h	4	"Sdmmc3 D1 Pad Value (cfio_regs_pad_sdmmc3_d1_PAD_VAL)—Offset 298h" on page 3406	00000002h
2A0h	4	"Sdmmc3 D3 Pad Configuration (cfio_regs_pad_sdmmc3_d3_PCONF0)—Offset 2A0h" on page 3407	20038C80h
2A4h	4	"Sdmmc3 D3 Delay Line Multiplexer (cfio_regs_pad_sdmmc3_d3_PCONF1)—Offset 2A4h" on page 3409	00008000h
2A8h	4	"Sdmmc3 D3 Pad Value (cfio_regs_pad_sdmmc3_d3_PAD_VAL)—Offset 2A8h" on page 3410	00000002h
2B0h	4	"Sdmmc3 Clk Pad Configuration (cfio_regs_pad_sdmmc3_clk_PCONF0)—Offset 2B0h" on page 3411	20038D00h
2B4h	4	"Sdmmc3 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc3_clk_PCONF1)—Offset 2B4h" on page 3412	00008000h
2B8h	4	"Sdmmc3 Clk Pad Value (cfio_regs_pad_sdmmc3_clk_PAD_VAL)—Offset 2B8h" on page 3413	00000002h
2C0h	4	"Sdmmc3 Cmd Pad Configuration (cfio_regs_pad_sdmmc3_cmd_PCONF0)—Offset 2C0h" on page 3414	20038C80h
2C4h	4	"Sdmmc3 Cmd Delay Line Multiplexer (cfio_regs_pad_sdmmc3_cmd_PCONF1)—Offset 2C4h" on page 3416	00008000h
2C8h	4	"Sdmmc3 Cmd Pad Value (cfio_regs_pad_sdmmc3_cmd_PAD_VAL)—Offset 2C8h" on page 3417	00000002h
2D0h	4	"Sdmmc3 D2 Pad Configuration (cfio_regs_pad_sdmmc3_d2_PCONF0)—Offset 2D0h" on page 3417	20038C80h
2D4h	4	"Sdmmc3 D2 Delay Line Multiplexer (cfio_regs_pad_sdmmc3_d2_PCONF1)—Offset 2D4h" on page 3419	00008000h
2D8h	4	"Sdmmc3 D2 Pad Value (cfio_regs_pad_sdmmc3_d2_PAD_VAL)—Offset 2D8h" on page 3420	00000002h
2E0h	4	"Sdmmc3 D0 Pad Configuration (cfio_regs_pad_sdmmc3_d0_PCONF0)—Offset 2E0h" on page 3421	20038C80h
2E4h	4	"Sdmmc3 D0 Delay Line Multiplexer (cfio_regs_pad_sdmmc3_d0_PCONF1)—Offset 2E4h" on page 3422	00008000h
2E8h	4	"Sdmmc3 D0 Pad Value (cfio_regs_pad_sdmmc3_d0_PAD_VAL)—Offset 2E8h" on page 3423	00000002h
2F0h	4	"Sdmmc2 D1 Pad Configuration (cfio_regs_pad_sdmmc2_d1_PCONF0)—Offset 2F0h" on page 3424	2003EC80h
2F4h	4	"Sdmmc2 D1 Delay Line Multiplexer (cfio_regs_pad_sdmmc2_d1_PCONF1)—Offset 2F4h" on page 3426	00008000h
2F8h	4	"Sdmmc2 D1 Pad Value (cfio_regs_pad_sdmmc2_d1_PAD_VAL)—Offset 2F8h" on page 3427	00000002h
300h	4	"Sdmmc2 Cmd Pad Configuration (cfio_regs_pad_sdmmc2_cmd_PCONF0)—Offset 300h" on page 3427	2003EC80h

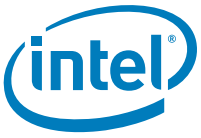


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
304h	4	"Sdmmc2 Cmd Delay Line Multiplexer (cfio_regs_pad_sdmmc2_cmd_PCONF1)—Offset 304h" on page 3429	00008000h
308h	4	"Sdmmc2 Cmd Pad Value (cfio_regs_pad_sdmmc2_cmd_PAD_VAL)—Offset 308h" on page 3430	00000002h
310h	4	"Sdmmc2 D3 Cd B Pad Configuration (cfio_regs_pad_sdmmc2_d3_cd_b_PCONF0)—Offset 310h" on page 3431	2003EC80h
314h	4	"Sdmmc2 D3 Cd B Delay Line Multiplexer (cfio_regs_pad_sdmmc2_d3_cd_b_PCONF1)—Offset 314h" on page 3432	00008000h
318h	4	"Sdmmc2 D3 Cd B Pad Value (cfio_regs_pad_sdmmc2_d3_cd_b_PAD_VAL)—Offset 318h" on page 3433	00000002h
320h	4	"Sdmmc2 Clk Pad Configuration (cfio_regs_pad_sdmmc2_clk_PCONF0)—Offset 320h" on page 3434	2003ED00h
324h	4	"Sdmmc2 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc2_clk_PCONF1)—Offset 324h" on page 3436	00008000h
328h	4	"Sdmmc2 Clk Pad Value (cfio_regs_pad_sdmmc2_clk_PAD_VAL)—Offset 328h" on page 3437	00000002h
330h	4	"Mmc1 Reset B Pad Configuration (cfio_regs_pad_mmc1_reset_b_PCONF0)—Offset 330h" on page 3437	2003ED00h
334h	4	"Mmc1 Reset B Delay Line Multiplexer (cfio_regs_pad_mmc1_reset_b_PCONF1)—Offset 334h" on page 3439	00008000h
338h	4	"Mmc1 Reset B Pad Value (cfio_regs_pad_mmc1_reset_b_PAD_VAL)—Offset 338h" on page 3440	00000002h
340h	4	"Sdmmc2 D2 Pad Configuration (cfio_regs_pad_sdmmc2_d2_PCONF0)—Offset 340h" on page 3441	2003EC80h
344h	4	"Sdmmc2 D2 Delay Line Multiplexer (cfio_regs_pad_sdmmc2_d2_PCONF1)—Offset 344h" on page 3442	00008000h
348h	4	"Sdmmc2 D2 Pad Value (cfio_regs_pad_sdmmc2_d2_PAD_VAL)—Offset 348h" on page 3443	00000002h
350h	4	"Sdmmc2 D0 Pad Configuration (cfio_regs_pad_sdmmc2_d0_PCONF0)—Offset 350h" on page 3444	2003EC80h
354h	4	"Sdmmc2 D0 Delay Line Multiplexer (cfio_regs_pad_sdmmc2_d0_PCONF1)—Offset 354h" on page 3446	00008000h
358h	4	"Sdmmc2 D0 Pad Value (cfio_regs_pad_sdmmc2_d0_PAD_VAL)—Offset 358h" on page 3447	00000002h
360h	4	"Sdmmc1 D3 Cd B Pad Configuration (cfio_regs_pad_sdmmc1_d3_cd_b_PCONF0)—Offset 360h" on page 3447	2003EC80h
364h	4	"Sdmmc1 D3 Cd B Delay Line Multiplexer (cfio_regs_pad_sdmmc1_d3_cd_b_PCONF1)—Offset 364h" on page 3449	00008000h

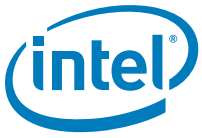


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
368h	4	"Sdmmc1 D3 Cd B Pad Value (cfio_regs_pad_sdmmc1_d3_cd_b_PAD_VAL)—Offset 368h" on page 3450	00000002h
370h	4	"Mmc1 D6 Pad Configuration (cfio_regs_pad_mmc1_d6_PCONF0)—Offset 370h" on page 3451	2003EC80h
374h	4	"Mmc1 D6 Delay Line Multiplexer (cfio_regs_pad_mmc1_d6_PCONF1)—Offset 374h" on page 3453	00008000h
378h	4	"Mmc1 D6 Pad Value (cfio_regs_pad_mmc1_d6_PAD_VAL)—Offset 378h" on page 3453	00000002h
380h	4	"Mmc1 D4 Sd We Pad Configuration (cfio_regs_pad_mmc1_d4_sd_we_PCONF0)—Offset 380h" on page 3454	2003EC80h
384h	4	"Mmc1 D4 Sd We Delay Line Multiplexer (cfio_regs_pad_mmc1_d4_sd_we_PCONF1)—Offset 384h" on page 3456	00008000h
388h	4	"Mmc1 D4 Sd We Pad Value (cfio_regs_pad_mmc1_d4_sd_we_PAD_VAL)—Offset 388h" on page 3457	00000002h
390h	4	"Sdmmc1 Cmd Pad Configuration (cfio_regs_pad_sdmmc1_cmd_PCONF0)—Offset 390h" on page 3458	2003EC80h
394h	4	"Sdmmc1 Cmd Delay Line Multiplexer (cfio_regs_pad_sdmmc1_cmd_PCONF1)—Offset 394h" on page 3460	00008000h
398h	4	"Sdmmc1 Cmd Pad Value (cfio_regs_pad_sdmmc1_cmd_PAD_VAL)—Offset 398h" on page 3460	00000002h
3A0h	4	"Sdmmc3 Cd B Pad Configuration (cfio_regs_pad_sdmmc3_cd_b_PCONF0)—Offset 3A0h" on page 3461	2003CC80h
3A4h	4	"Sdmmc3 Cd B Delay Line Multiplexer (cfio_regs_pad_sdmmc3_cd_b_PCONF1)—Offset 3A4h" on page 3463	00008000h
3A8h	4	"Sdmmc3 Cd B Pad Value (cfio_regs_pad_sdmmc3_cd_b_PAD_VAL)—Offset 3A8h" on page 3464	00000002h
3B0h	4	"Sdmmc1 D2 Pad Configuration (cfio_regs_pad_sdmmc1_d2_PCONF0)—Offset 3B0h" on page 3465	2003EC80h
3B4h	4	"Sdmmc1 D2 Delay Line Multiplexer (cfio_regs_pad_sdmmc1_d2_PCONF1)—Offset 3B4h" on page 3466	00008000h
3B8h	4	"Sdmmc1 D2 Pad Value (cfio_regs_pad_sdmmc1_d2_PAD_VAL)—Offset 3B8h" on page 3467	00000002h
3C0h	4	"Mmc1 D5 Pad Configuration (cfio_regs_pad_mmc1_d5_PCONF0)—Offset 3C0h" on page 3468	2003EC80h
3C4h	4	"Mmc1 D5 Delay Line Multiplexer (cfio_regs_pad_mmc1_d5_PCONF1)—Offset 3C4h" on page 3470	00008000h
3C8h	4	"Mmc1 D5 Pad Value (cfio_regs_pad_mmc1_d5_PAD_VAL)—Offset 3C8h" on page 3471	00000002h
3D0h	4	"Sdmmc1 D0 Pad Configuration (cfio_regs_pad_sdmmc1_d0_PCONF0)—Offset 3D0h" on page 3471	2003EC80h

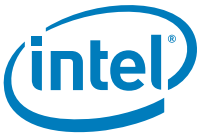


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
3D4h	4	"Sdmmc1 D0 Delay Line Multiplexer (cfio_regs_pad_sdmmc1_d0_PCONF1)—Offset 3D4h" on page 3473	00008000h
3D8h	4	"Sdmmc1 D0 Pad Value (cfio_regs_pad_sdmmc1_d0_PAD_VAL)—Offset 3D8h" on page 3474	00000002h
3E0h	4	"Sdmmc1 Clk Pad Configuration (cfio_regs_pad_sdmmc1_clk_PCONF0)—Offset 3E0h" on page 3475	2003ED00h
3E4h	4	"Sdmmc1 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc1_clk_PCONF1)—Offset 3E4h" on page 3476	00008000h
3E8h	4	"Sdmmc1 Clk Pad Value (cfio_regs_pad_sdmmc1_clk_PAD_VAL)—Offset 3E8h" on page 3477	00000002h
3F0h	4	"Mmc1 D7 Pad Configuration (cfio_regs_pad_mmc1_d7_PCONF0)—Offset 3F0h" on page 3478	2003EC80h
3F4h	4	"Mmc1 D7 Delay Line Multiplexer (cfio_regs_pad_mmc1_d7_PCONF1)—Offset 3F4h" on page 3480	00008000h
3F8h	4	"Mmc1 D7 Pad Value (cfio_regs_pad_mmc1_d7_PAD_VAL)—Offset 3F8h" on page 3481	00000002h
400h	4	"Sdmmc1 D1 Pad Configuration (cfio_regs_pad_sdmmc1_d1_PCONF0)—Offset 400h" on page 3481	2003EC80h
404h	4	"Sdmmc1 D1 Delay Line Multiplexer (cfio_regs_pad_sdmmc1_d1_PCONF1)—Offset 404h" on page 3483	00008000h
408h	4	"Sdmmc1 D1 Pad Value (cfio_regs_pad_sdmmc1_d1_PAD_VAL)—Offset 408h" on page 3484	00000002h
410h	4	"Lpc Clkout1 Pad Configuration (cfio_regs_pad_lpc_clkout1_PCONF0)—Offset 410h" on page 3485	20038D00h
414h	4	"Lpc Clkout1 Delay Line Multiplexer (cfio_regs_pad_lpc_clkout1_PCONF1)—Offset 414h" on page 3486	00008000h
418h	4	"Lpc Clkout1 Pad Value (cfio_regs_pad_lpc_clkout1_PAD_VAL)—Offset 418h" on page 3487	00000002h
420h	4	"Lpc Ad3 Pad Configuration (cfio_regs_pad_lpc_ad3_PCONF0)—Offset 420h" on page 3488	20038C80h
424h	4	"Lpc Ad3 Delay Line Multiplexer (cfio_regs_pad_lpc_ad3_PCONF1)—Offset 424h" on page 3490	00008000h
428h	4	"Lpc Ad3 Pad Value (cfio_regs_pad_lpc_ad3_PAD_VAL)—Offset 428h" on page 3491	00000002h
430h	4	"Lpc Ad2 Pad Configuration (cfio_regs_pad_lpc_ad2_PCONF0)—Offset 430h" on page 3491	20038C80h
434h	4	"Lpc Ad2 Delay Line Multiplexer (cfio_regs_pad_lpc_ad2_PCONF1)—Offset 434h" on page 3493	00008000h
438h	4	"Lpc Ad2 Pad Value (cfio_regs_pad_lpc_ad2_PAD_VAL)—Offset 438h" on page 3494	00000002h
440h	4	"Lpc Ad1 Pad Configuration (cfio_regs_pad_lpc_ad1_PCONF0)—Offset 440h" on page 3495	20038C80h

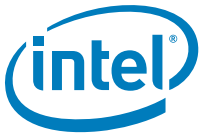


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
444h	4	"Lpc Ad1 Delay Line Multiplexer (cfio_regs_pad_lpc_ad1_PCONF1)—Offset 444h" on page 3496	00008000h
448h	4	"Lpc Ad1 Pad Value (cfio_regs_pad_lpc_ad1_PAD_VAL)—Offset 448h" on page 3497	00000002h
450h	4	"Lpc Frameb Pad Configuration (cfio_regs_pad_lpc_frameb_PCONF0)—Offset 450h" on page 3498	20038C80h
454h	4	"Lpc Frameb Delay Line Multiplexer (cfio_regs_pad_lpc_frameb_PCONF1)—Offset 454h" on page 3500	00008000h
458h	4	"Lpc Frameb Pad Value (cfio_regs_pad_lpc_frameb_PAD_VAL)—Offset 458h" on page 3501	00000002h
460h	4	"Lpc Ad0 Pad Configuration (cfio_regs_pad_lpc_ad0_PCONF0)—Offset 460h" on page 3501	20038C80h
464h	4	"Lpc Ad0 Delay Line Multiplexer (cfio_regs_pad_lpc_ad0_PCONF1)—Offset 464h" on page 3503	00008000h
468h	4	"Lpc Ad0 Pad Value (cfio_regs_pad_lpc_ad0_PAD_VAL)—Offset 468h" on page 3504	00000002h
470h	4	"Lpc Clkout0 Pad Configuration (cfio_regs_pad_lpc_clkout0_PCONF0)—Offset 470h" on page 3505	20038D00h
474h	4	"Lpc Clkout0 Delay Line Multiplexer (cfio_regs_pad_lpc_clkout0_PCONF1)—Offset 474h" on page 3506	00008000h
478h	4	"Lpc Clkout0 Pad Value (cfio_regs_pad_lpc_clkout0_PAD_VAL)—Offset 478h" on page 3507	00000002h
480h	4	"Lpc Clkrunb Pad Configuration (cfio_regs_pad_lpc_clkrunb_PCONF0)—Offset 480h" on page 3508	20038C80h
484h	4	"Lpc Clkrunb Delay Line Multiplexer (cfio_regs_pad_lpc_clkrunb_PCONF1)—Offset 484h" on page 3510	00008000h
488h	4	"Lpc Clkrunb Pad Value (cfio_regs_pad_lpc_clkrunb_PAD_VAL)—Offset 488h" on page 3511	00000002h
490h	4	"Hv Crt Ddc Clk Pad Configuration (cfio_regs_pad_hv_crt_ddc_clk_PCONF0)—Offset 490h" on page 3511	2003C800h
494h	4	"Hv Crt Ddc Clk Delay Line Multiplexer (cfio_regs_pad_hv_crt_ddc_clk_PCONF1)—Offset 494h" on page 3513	00008000h
498h	4	"Hv Crt Ddc Clk Pad Value (cfio_regs_pad_hv_crt_ddc_clk_PAD_VAL)—Offset 498h" on page 3514	00000002h
4A0h	4	"Hv Crt Vsync Pad Configuration (cfio_regs_pad_hv_crt_vsync_PCONF0)—Offset 4A0h" on page 3515	20038800h
4A4h	4	"Hv Crt Vsync Delay Line Multiplexer (cfio_regs_pad_hv_crt_vsync_PCONF1)—Offset 4A4h" on page 3516	00008000h
4A8h	4	"Hv Crt Vsync Pad Value (cfio_regs_pad_hv_crt_vsync_PAD_VAL)—Offset 4A8h" on page 3517	00000002h
4B0h	4	"Hv Crt Hsync Pad Configuration (cfio_regs_pad_hv_crt_hsync_PCONF0)—Offset 4B0h" on page 3518	20038800h

Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
4B4h	4	"Hv Crt Hsync Delay Line Multiplexer (cfio_regs_pad_hv_crt_hsync_PCONF1)—Offset 4B4h" on page 3520	00008000h
4B8h	4	"Hv Crt Hsync Pad Value (cfio_regs_pad_hv_crt_hsync_PAD_VAL)—Offset 4B8h" on page 3521	00000002h
4C0h	4	"Hv Crt Ddc Data Pad Configuration (cfio_regs_pad_hv_crt_ddc_data_PCONF0)—Offset 4C0h" on page 3521	2003C800h
4C4h	4	"Hv Crt Ddc Data Delay Line Multiplexer (cfio_regs_pad_hv_crt_ddc_data_PCONF1)—Offset 4C4h" on page 3523	00008000h
4C8h	4	"Hv Crt Ddc Data Pad Value (cfio_regs_pad_hv_crt_ddc_data_PAD_VAL)—Offset 4C8h" on page 3524	00000002h
4D0h	4	"Mhsi Acdata Pad Configuration (cfio_regs_pad_mhsi_acdata_PCONF0)—Offset 4D0h" on page 3525	2003CD00h
4D4h	4	"Mhsi Acdata Delay Line Multiplexer (cfio_regs_pad_mhsi_acdata_PCONF1)—Offset 4D4h" on page 3526	00008000h
4D8h	4	"Mhsi Acdata Pad Value (cfio_regs_pad_mhsi_acdata_PAD_VAL)—Offset 4D8h" on page 3527	00000002h
4E0h	4	"Mhsi Acwake Pad Configuration (cfio_regs_pad_mhsi_acwake_PCONF0)—Offset 4E0h" on page 3528	2003CD00h
4E4h	4	"Mhsi Acwake Delay Line Multiplexer (cfio_regs_pad_mhsi_acwake_PCONF1)—Offset 4E4h" on page 3530	00008000h
4E8h	4	"Mhsi Acwake Pad Value (cfio_regs_pad_mhsi_acwake_PAD_VAL)—Offset 4E8h" on page 3531	00000002h
4F0h	4	"Mhsi Acflag Pad Configuration (cfio_regs_pad_mhsi_acflag_PCONF0)—Offset 4F0h" on page 3531	2003CC80h
4F4h	4	"Mhsi Acflag Delay Line Multiplexer (cfio_regs_pad_mhsi_acflag_PCONF1)—Offset 4F4h" on page 3533	00008000h
4F8h	4	"Mhsi Acflag Pad Value (cfio_regs_pad_mhsi_acflag_PAD_VAL)—Offset 4F8h" on page 3534	00000002h
500h	4	"Mhsi Caflag Pad Configuration (cfio_regs_pad_mhsi_caflag_PCONF0)—Offset 500h" on page 3535	2003CD00h
504h	4	"Mhsi Caflag Delay Line Multiplexer (cfio_regs_pad_mhsi_caflag_PCONF1)—Offset 504h" on page 3536	00008000h
508h	4	"Mhsi Caflag Pad Value (cfio_regs_pad_mhsi_caflag_PAD_VAL)—Offset 508h" on page 3537	00000002h
510h	4	"Mhsi Cadata Pad Configuration (cfio_regs_pad_mhsi_cadata_PCONF0)—Offset 510h" on page 3538	2003CD00h
514h	4	"Mhsi Cadata Delay Line Multiplexer (cfio_regs_pad_mhsi_cadata_PCONF1)—Offset 514h" on page 3540	00008000h
518h	4	"Mhsi Cadata Pad Value (cfio_regs_pad_mhsi_cadata_PAD_VAL)—Offset 518h" on page 3541	00000002h
520h	4	"Mhsi Caready Pad Configuration (cfio_regs_pad_mhsi_caready_PCONF0)—Offset 520h" on page 3541	2003CC80h

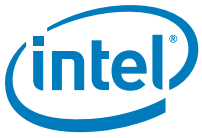


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
524h	4	"Mhsi Caready Delay Line Multiplexer (cfio_regs_pad_mhsi_caready_PCONF1)—Offset 524h" on page 3543	00008000h
528h	4	"Mhsi Caready Pad Value (cfio_regs_pad_mhsi_caready_PAD_VAL)—Offset 528h" on page 3544	00000002h
530h	4	"Mhsi Acready Pad Configuration (cfio_regs_pad_mhsi_acready_PCONF0)—Offset 530h" on page 3545	2003CD00h
534h	4	"Mhsi Acready Delay Line Multiplexer (cfio_regs_pad_mhsi_acready_PCONF1)—Offset 534h" on page 3547	00008000h
538h	4	"Mhsi Acready Pad Value (cfio_regs_pad_mhsi_acready_PAD_VAL)—Offset 538h" on page 3547	00000002h
540h	4	"Hda Dockenb Pad Configuration (cfio_regs_pad_hda_dockenb_PCONF0)—Offset 540h" on page 3548	2003CD00h
544h	4	"Hda Dockenb Delay Line Multiplexer (cfio_regs_pad_hda_dockenb_PCONF1)—Offset 544h" on page 3550	00008000h
548h	4	"Hda Dockenb Pad Value (cfio_regs_pad_hda_dockenb_PAD_VAL)—Offset 548h" on page 3551	00000002h
550h	4	"Sata Gp0 Pad Configuration (cfio_regs_pad_sata_gp0_PCONF0)—Offset 550h" on page 3552	2003CD00h
554h	4	"Sata Gp0 Delay Line Multiplexer (cfio_regs_pad_sata_gp0_PCONF1)—Offset 554h" on page 3553	00008000h
558h	4	"Sata Gp0 Pad Value (cfio_regs_pad_sata_gp0_PAD_VAL)—Offset 558h" on page 3554	00000002h
560h	4	"Ilb Serirq Pad Configuration (cfio_regs_pad_ilb_serirq_PCONF0)—Offset 560h" on page 3555	2003CC80h
564h	4	"Ilb Serirq Delay Line Multiplexer (cfio_regs_pad_ilb_serirq_PCONF1)—Offset 564h" on page 3557	00008000h
568h	4	"Ilb Serirq Pad Value (cfio_regs_pad_ilb_serirq_PAD_VAL)—Offset 568h" on page 3558	00000002h
570h	4	"Plt Clk1 Pad Configuration (cfio_regs_pad_plt_clk1_PCONF0)—Offset 570h" on page 3558	2003CD00h
574h	4	"Plt Clk1 Delay Line Multiplexer (cfio_regs_pad_plt_clk1_PCONF1)—Offset 574h" on page 3560	00008000h
578h	4	"Plt Clk1 Pad Value (cfio_regs_pad_plt_clk1_PAD_VAL)—Offset 578h" on page 3561	00000002h
580h	4	"Smb Clk Pad Configuration (cfio_regs_pad_smb_clk_PCONF0)—Offset 580h" on page 3562	2003CC80h
584h	4	"Smb Clk Delay Line Multiplexer (cfio_regs_pad_smb_clk_PCONF1)—Offset 584h" on page 3563	00008000h
588h	4	"Smb Clk Pad Value (cfio_regs_pad_smb_clk_PAD_VAL)—Offset 588h" on page 3564	00000002h
590h	4	"Sata Gp1 Pad Configuration (cfio_regs_pad_sata_gp1_PCONF0)—Offset 590h" on page 3565	2003CD00h

Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
594h	4	"Sata Gp1 Delay Line Multiplexer (cfio_regs_pad_sata_gp1_PCONF1)—Offset 594h" on page 3567	00008000h
598h	4	"Sata Gp1 Pad Value (cfio_regs_pad_sata_gp1_PAD_VAL)—Offset 598h" on page 3568	00000002h
5A0h	4	"Smb Data Pad Configuration (cfio_regs_pad_smb_data_PCONF0)—Offset 5A0h" on page 3568	2003CC80h
5A4h	4	"Smb Data Delay Line Multiplexer (cfio_regs_pad_smb_data_PCONF1)—Offset 5A4h" on page 3570	00008000h
5A8h	4	"Smb Data Pad Value (cfio_regs_pad_smb_data_PAD_VAL)—Offset 5A8h" on page 3571	00000002h
5B0h	4	"Plt Clk2 Pad Configuration (cfio_regs_pad_plt_clk2_PCONF0)—Offset 5B0h" on page 3572	2003CD00h
5B4h	4	"Plt Clk2 Delay Line Multiplexer (cfio_regs_pad_plt_clk2_PCONF1)—Offset 5B4h" on page 3573	00008000h
5B8h	4	"Plt Clk2 Pad Value (cfio_regs_pad_plt_clk2_PAD_VAL)—Offset 5B8h" on page 3574	00000002h
5C0h	4	"Smb Alertb Pad Configuration (cfio_regs_pad_smb_alertb_PCONF0)—Offset 5C0h" on page 3575	2003CC80h
5C4h	4	"Smb Alertb Delay Line Multiplexer (cfio_regs_pad_smb_alertb_PCONF1)—Offset 5C4h" on page 3577	00008000h
5C8h	4	"Smb Alertb Pad Value (cfio_regs_pad_smb_alertb_PAD_VAL)—Offset 5C8h" on page 3578	00000002h
5D0h	4	"Sata Ledn Pad Configuration (cfio_regs_pad_sata_ledn_PCONF0)—Offset 5D0h" on page 3578	2003CC80h
5D4h	4	"Sata Ledn Delay Line Multiplexer (cfio_regs_pad_sata_ledn_PCONF1)—Offset 5D4h" on page 3580	00008000h
5D8h	4	"Sata Ledn Pad Value (cfio_regs_pad_sata_ledn_PAD_VAL)—Offset 5D8h" on page 3581	00000002h
5E0h	4	"Pmu Resetbutton B Pad Configuration (cfio_regs_pad_pmu_resetbutton_b_PCONF0)—Offset 5E0h" on page 3582	2003CC80h
5E4h	4	"Pmu Resetbutton B Delay Line Multiplexer (cfio_regs_pad_pmu_resetbutton_b_PCONF1)—Offset 5E4h" on page 3583	00008000h
5E8h	4	"Pmu Resetbutton B Pad Value (cfio_regs_pad_pmu_resetbutton_b_PAD_VAL)—Offset 5E8h" on page 3584	00000006h
5F0h	4	"Sdmmc3 1p8 En Pad Configuration (cfio_regs_pad_sdmmc3_1p8_en_PCONF0)—Offset 5F0h" on page 3585	2003CD00h
5F4h	4	"Sdmmc3 1p8 En Delay Line Multiplexer (cfio_regs_pad_sdmmc3_1p8_en_PCONF1)—Offset 5F4h" on page 3587	00008000h

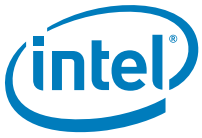


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
5F8h	4	"Sdmmc3 1p8 En Pad Value (cfio_regs_pad_sdmmc3_1p8_en_PAD_VAL)—Offset 5F8h" on page 3588	00000002h
600h	4	"Pcie Clkreq0b Pad Configuration (cfio_regs_pad_pcie_clkreq0b_PCONF0)—Offset 600h" on page 3588	2003CC80h
604h	4	"Pcie Clkreq0b Delay Line Multiplexer (cfio_regs_pad_pcie_clkreq0b_PCONF1)—Offset 604h" on page 3590	00008000h
608h	4	"Pcie Clkreq0b Pad Value (cfio_regs_pad_pcie_clkreq0b_PAD_VAL)—Offset 608h" on page 3591	00000002h
610h	4	"Plt Clk4 Pad Configuration (cfio_regs_pad_plt_clk4_PCONF0)—Offset 610h" on page 3592	2003CD00h
614h	4	"Plt Clk4 Delay Line Multiplexer (cfio_regs_pad_plt_clk4_PCONF1)—Offset 614h" on page 3593	00008000h
618h	4	"Plt Clk4 Pad Value (cfio_regs_pad_plt_clk4_PAD_VAL)—Offset 618h" on page 3594	00000002h
620h	4	"Pcie Clkreq3b Pad Configuration (cfio_regs_pad_pcie_clkreq3b_PCONF0)—Offset 620h" on page 3595	2003CC80h
624h	4	"Pcie Clkreq3b Delay Line Multiplexer (cfio_regs_pad_pcie_clkreq3b_PCONF1)—Offset 624h" on page 3597	00008000h
628h	4	"Pcie Clkreq3b Pad Value (cfio_regs_pad_pcie_clkreq3b_PAD_VAL)—Offset 628h" on page 3598	00000002h
630h	4	"Pcie Clkreq1b Pad Configuration (cfio_regs_pad_pcie_clkreq1b_PCONF0)—Offset 630h" on page 3598	2003CC80h
634h	4	"Pcie Clkreq1b Delay Line Multiplexer (cfio_regs_pad_pcie_clkreq1b_PCONF1)—Offset 634h" on page 3600	00008000h
638h	4	"Pcie Clkreq1b Pad Value (cfio_regs_pad_pcie_clkreq1b_PAD_VAL)—Offset 638h" on page 3601	00000002h
640h	4	"Plt Clk5 Pad Configuration (cfio_regs_pad_plt_clk5_PCONF0)—Offset 640h" on page 3602	2003CD00h
644h	4	"Plt Clk5 Delay Line Multiplexer (cfio_regs_pad_plt_clk5_PCONF1)—Offset 644h" on page 3603	00008000h
648h	4	"Plt Clk5 Pad Value (cfio_regs_pad_plt_clk5_PAD_VAL)—Offset 648h" on page 3604	00000002h
650h	4	"Pcie Clkreq4b Pad Configuration (cfio_regs_pad_pcie_clkreq4b_PCONF0)—Offset 650h" on page 3605	2003CC80h
654h	4	"Pcie Clkreq4b Delay Line Multiplexer (cfio_regs_pad_pcie_clkreq4b_PCONF1)—Offset 654h" on page 3607	00008000h
658h	4	"Pcie Clkreq4b Pad Value (cfio_regs_pad_pcie_clkreq4b_PAD_VAL)—Offset 658h" on page 3608	00000002h
660h	4	"Pcie Clkreq2b Pad Configuration (cfio_regs_pad_pcie_clkreq2b_PCONF0)—Offset 660h" on page 3608	2003CC80h

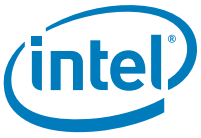


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
664h	4	"Pcie Clkreq2b Delay Line Multiplexer (cfio_regs_pad_pcie_clkreq2b_PCONF1)—Offset 664h" on page 3610	00008000h
668h	4	"Pcie Clkreq2b Pad Value (cfio_regs_pad_pcie_clkreq2b_PAD_VAL)—Offset 668h" on page 3611	00000002h
670h	4	"Spkr Pad Configuration (cfio_regs_pad_spkr_PCONF0)—Offset 670h" on page 3612	2003CC80h
674h	4	"Spkr Delay Line Multiplexer (cfio_regs_pad_spkr_PCONF1)—Offset 674h" on page 3613	00008000h
678h	4	"Spkr Pad Value (cfio_regs_pad_spkr_PAD_VAL)—Offset 678h" on page 3614	00000002h
680h	4	"Plt Clk3 Pad Configuration (cfio_regs_pad_plt_clk3_PCONF0)—Offset 680h" on page 3615	2003CD00h
684h	4	"Plt Clk3 Delay Line Multiplexer (cfio_regs_pad_plt_clk3_PCONF1)—Offset 684h" on page 3617	00008000h
688h	4	"Plt Clk3 Pad Value (cfio_regs_pad_plt_clk3_PAD_VAL)—Offset 688h" on page 3618	00000002h
690h	4	"Sdmmc3 Pwr En B Pad Configuration (cfio_regs_pad_sdmmc3_pwr_en_b_PCONF0)—Offset 690h" on page 3618	2003CC80h
694h	4	"Sdmmc3 Pwr En B Delay Line Multiplexer (cfio_regs_pad_sdmmc3_pwr_en_b_PCONF1)—Offset 694h" on page 3620	00008000h
698h	4	"Sdmmc3 Pwr En B Pad Value (cfio_regs_pad_sdmmc3_pwr_en_b_PAD_VAL)—Offset 698h" on page 3621	00000002h
6A0h	4	"Plt Clk0 Pad Configuration (cfio_regs_pad_plt_clk0_PCONF0)—Offset 6A0h" on page 3622	2003CD00h
6A4h	4	"Plt Clk0 Delay Line Multiplexer (cfio_regs_pad_plt_clk0_PCONF1)—Offset 6A4h" on page 3624	00008000h
6A8h	4	"Plt Clk0 Pad Value (cfio_regs_pad_plt_clk0_PAD_VAL)—Offset 6A8h" on page 3624	00000002h
6B0h	4	"Vgpio 0 Pad Configuration (cfio_regs_pad_vgpio_0_PCONF0)—Offset 6B0h" on page 3625	20038800h
6B4h	4	"Vgpio 0 Delay Line Multiplexer (cfio_regs_pad_vgpio_0_PCONF1)—Offset 6B4h" on page 3627	00008000h
6B8h	4	"Vgpio 0 Pad Value (cfio_regs_pad_vgpio_0_PAD_VAL)—Offset 6B8h" on page 3628	00000004h
6C0h	4	"Vgpio 1 Pad Configuration (cfio_regs_pad_vgpio_1_PCONF0)—Offset 6C0h" on page 3629	20038800h
6C4h	4	"Vgpio 1 Delay Line Multiplexer (cfio_regs_pad_vgpio_1_PCONF1)—Offset 6C4h" on page 3630	00008000h
6C8h	4	"Vgpio 1 Pad Value (cfio_regs_pad_vgpio_1_PAD_VAL)—Offset 6C8h" on page 3631	00000004h

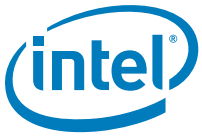


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
6D0h	4	"Vgpio 2 Pad Configuration (cfio_regs_pad_vgpio_2_PCONF0)—Offset 6D0h" on page 3632	20038800h
6D4h	4	"Vgpio 2 Delay Line Multiplexer (cfio_regs_pad_vgpio_2_PCONF1)—Offset 6D4h" on page 3634	00008000h
6D8h	4	"Vgpio 2 Pad Value (cfio_regs_pad_vgpio_2_PAD_VAL)—Offset 6D8h" on page 3635	00000004h
6E0h	4	"Vgpio 3 Pad Configuration (cfio_regs_pad_vgpio_3_PCONF0)—Offset 6E0h" on page 3635	20038800h
6E4h	4	"Vgpio 3 Delay Line Multiplexer (cfio_regs_pad_vgpio_3_PCONF1)—Offset 6E4h" on page 3637	00008000h
6E8h	4	"Vgpio 3 Pad Value (cfio_regs_pad_vgpio_3_PAD_VAL)—Offset 6E8h" on page 3638	00000004h
6F0h	4	"Vgpio 4 Pad Configuration (cfio_regs_pad_vgpio_4_PCONF0)—Offset 6F0h" on page 3639	20038800h
6F4h	4	"Vgpio 4 Delay Line Multiplexer (cfio_regs_pad_vgpio_4_PCONF1)—Offset 6F4h" on page 3640	00008000h
6F8h	4	"Vgpio 4 Pad Value (cfio_regs_pad_vgpio_4_PAD_VAL)—Offset 6F8h" on page 3641	00000006h
700h	4	"Vgpio 5 Pad Configuration (cfio_regs_pad_vgpio_5_PCONF0)—Offset 700h" on page 3642	20038800h
704h	4	"Vgpio 5 Delay Line Multiplexer (cfio_regs_pad_vgpio_5_PCONF1)—Offset 704h" on page 3644	00008000h
708h	4	"Vgpio 5 Pad Value (cfio_regs_pad_vgpio_5_PAD_VAL)—Offset 708h" on page 3645	00000004h
710h	4	"Vgpio 6 Pad Configuration (cfio_regs_pad_vgpio_6_PCONF0)—Offset 710h" on page 3645	20038800h
714h	4	"Vgpio 6 Delay Line Multiplexer (cfio_regs_pad_vgpio_6_PCONF1)—Offset 714h" on page 3647	00008000h
718h	4	"Vgpio 6 Pad Value (cfio_regs_pad_vgpio_6_PAD_VAL)—Offset 718h" on page 3648	00000004h
720h	4	"Vgpio 7 Pad Configuration (cfio_regs_pad_vgpio_7_PCONF0)—Offset 720h" on page 3649	20038800h
724h	4	"Vgpio 7 Delay Line Multiplexer (cfio_regs_pad_vgpio_7_PCONF1)—Offset 724h" on page 3650	00008000h
728h	4	"Vgpio 7 Pad Value (cfio_regs_pad_vgpio_7_PAD_VAL)—Offset 728h" on page 3651	00000004h
730h	4	"Vgpio 8 Pad Configuration (cfio_regs_pad_vgpio_8_PCONF0)—Offset 730h" on page 3652	20038800h
734h	4	"Vgpio 8 Delay Line Multiplexer (cfio_regs_pad_vgpio_8_PCONF1)—Offset 734h" on page 3654	00008000h
738h	4	"Vgpio 8 Pad Value (cfio_regs_pad_vgpio_8_PAD_VAL)—Offset 738h" on page 3655	00000004h

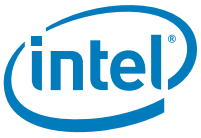


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
740h	4	"Vgpio 9 Pad Configuration (cfio_regs_pad_vgpio_9_PCONF0)—Offset 740h" on page 3655	20038800h
744h	4	"Vgpio 9 Delay Line Multiplexer (cfio_regs_pad_vgpio_9_PCONF1)—Offset 744h" on page 3657	00008000h
748h	4	"Vgpio 9 Pad Value (cfio_regs_pad_vgpio_9_PAD_VAL)—Offset 748h" on page 3658	00000004h
750h	4	"Vgpio 10 Pad Configuration (cfio_regs_pad_vgpio_10_PCONF0)—Offset 750h" on page 3659	20038800h
754h	4	"Vgpio 10 Delay Line Multiplexer (cfio_regs_pad_vgpio_10_PCONF1)—Offset 754h" on page 3660	00008000h
758h	4	"Vgpio 10 Pad Value (cfio_regs_pad_vgpio_10_PAD_VAL)—Offset 758h" on page 3661	00000004h
760h	4	"Vgpio 11 Pad Configuration (cfio_regs_pad_vgpio_11_PCONF0)—Offset 760h" on page 3662	20038800h
764h	4	"Vgpio 11 Delay Line Multiplexer (cfio_regs_pad_vgpio_11_PCONF1)—Offset 764h" on page 3664	00008000h
768h	4	"Vgpio 11 Pad Value (cfio_regs_pad_vgpio_11_PAD_VAL)—Offset 768h" on page 3665	00000004h
770h	4	"Vgpio 12 Pad Configuration (cfio_regs_pad_vgpio_12_PCONF0)—Offset 770h" on page 3665	20038800h
774h	4	"Vgpio 12 Delay Line Multiplexer (cfio_regs_pad_vgpio_12_PCONF1)—Offset 774h" on page 3667	00008000h
778h	4	"Vgpio 12 Pad Value (cfio_regs_pad_vgpio_12_PAD_VAL)—Offset 778h" on page 3668	00000004h
780h	4	"Vgpio 13 Pad Configuration (cfio_regs_pad_vgpio_13_PCONF0)—Offset 780h" on page 3669	20038800h
784h	4	"Vgpio 13 Delay Line Multiplexer (cfio_regs_pad_vgpio_13_PCONF1)—Offset 784h" on page 3670	00008000h
788h	4	"Vgpio 13 Pad Value (cfio_regs_pad_vgpio_13_PAD_VAL)—Offset 788h" on page 3671	00000004h
790h	4	"Vgpio 14 Pad Configuration (cfio_regs_pad_vgpio_14_PCONF0)—Offset 790h" on page 3672	20038800h
794h	4	"Vgpio 14 Delay Line Multiplexer (cfio_regs_pad_vgpio_14_PCONF1)—Offset 794h" on page 3674	00008000h
798h	4	"Vgpio 14 Pad Value (cfio_regs_pad_vgpio_14_PAD_VAL)—Offset 798h" on page 3675	00000004h
7A0h	4	"Vgpio 15 Pad Configuration (cfio_regs_pad_vgpio_15_PCONF0)—Offset 7A0h" on page 3675	20038800h
7A4h	4	"Vgpio 15 Delay Line Multiplexer (cfio_regs_pad_vgpio_15_PCONF1)—Offset 7A4h" on page 3677	00008000h
7A8h	4	"Vgpio 15 Pad Value (cfio_regs_pad_vgpio_15_PAD_VAL)—Offset 7A8h" on page 3678	00000004h

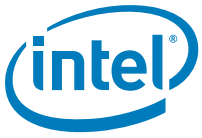


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
7B0h	4	"Vgpio 16 Pad Configuration (cfio_regs_pad_vgpio_16_PCONF0)—Offset 7B0h" on page 3679	20038800h
7B4h	4	"Vgpio 16 Delay Line Multiplexer (cfio_regs_pad_vgpio_16_PCONF1)—Offset 7B4h" on page 3680	00008000h
7B8h	4	"Vgpio 16 Pad Value (cfio_regs_pad_vgpio_16_PAD_VAL)—Offset 7B8h" on page 3681	00000004h
7C0h	4	"Vgpio 17 Pad Configuration (cfio_regs_pad_vgpio_17_PCONF0)—Offset 7C0h" on page 3682	20038800h
7C4h	4	"Vgpio 17 Delay Line Multiplexer (cfio_regs_pad_vgpio_17_PCONF1)—Offset 7C4h" on page 3684	00008000h
7C8h	4	"Vgpio 17 Pad Value (cfio_regs_pad_vgpio_17_PAD_VAL)—Offset 7C8h" on page 3685	00000004h
7D0h	4	"Vgpio 18 Pad Configuration (cfio_regs_pad_vgpio_18_PCONF0)—Offset 7D0h" on page 3685	20038800h
7D4h	4	"Vgpio 18 Delay Line Multiplexer (cfio_regs_pad_vgpio_18_PCONF1)—Offset 7D4h" on page 3687	00008000h
7D8h	4	"Vgpio 18 Pad Value (cfio_regs_pad_vgpio_18_PAD_VAL)—Offset 7D8h" on page 3688	00000004h
7E0h	4	"Vgpio 19 Pad Configuration (cfio_regs_pad_vgpio_19_PCONF0)—Offset 7E0h" on page 3689	20038800h
7E4h	4	"Vgpio 19 Delay Line Multiplexer (cfio_regs_pad_vgpio_19_PCONF1)—Offset 7E4h" on page 3690	00008000h
7E8h	4	"Vgpio 19 Pad Value (cfio_regs_pad_vgpio_19_PAD_VAL)—Offset 7E8h" on page 3691	00000004h
7F0h	4	"Vgpio 20 Pad Configuration (cfio_regs_pad_vgpio_20_PCONF0)—Offset 7F0h" on page 3692	20038800h
7F4h	4	"Vgpio 20 Delay Line Multiplexer (cfio_regs_pad_vgpio_20_PCONF1)—Offset 7F4h" on page 3694	00008000h
7F8h	4	"Vgpio 20 Pad Value (cfio_regs_pad_vgpio_20_PAD_VAL)—Offset 7F8h" on page 3695	00000004h
800h	4	"TS0 SCORE Interrupt Status 0 (cfio_regs_REG_TS0_SCORE_IRQ_TS_0)—Offset 800h" on page 3695	00000000h
804h	4	"TS1 SCORE Interrupt Status 1 (cfio_regs_REG_TS1_SCORE_IRQ_TS_1)—Offset 804h" on page 3696	00000000h
808h	4	"TS2 SCORE Interrupt Status 2 (cfio_regs_REG_TS2_SCORE_IRQ_TS_2)—Offset 808h" on page 3697	00000000h
80Ch	4	"TS3 SCORE Interrupt Status 3 (cfio_regs_REG_TS3_SCORE_IRQ_TS_3)—Offset 80Ch" on page 3698	00000000h
810h	4	"C71p1cfiomvscoreaza Compensation Configuration (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_CFG)—Offset 810h" on page 3699	00078080h

Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
814h	4	"C71p1cfiomvscoreaza Compensation Override (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_OV)—Offset 814h" on page 3700	001F000Fh
818h	4	"C71p1cfiomvscoreaza Compensation Initial Values (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_INIT)—Offset 818h" on page 3701	0000FFFFh
81Ch	4	"C71p1cfiomvscoreaza Compensation DFX Override (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_DFX)—Offset 81Ch" on page 3701	01000080h
820h	4	"C71p1cfiomvrscoresdio1 Compensation Configuration (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_CFG)—Offset 820h" on page 3702	00078080h
824h	4	"C71p1cfiomvrscoresdio1 Compensation Override (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_OV)—Offset 824h" on page 3703	001F000Fh
828h	4	"C71p1cfiomvrscoresdio1 Compensation Initial Values (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_INIT)—Offset 828h" on page 3704	0000FFFFh
82Ch	4	"C71p1cfiomvrscoresdio1 Compensation DFX Override (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_DFX)—Offset 82Ch" on page 3704	01000080h
830h	4	"C71p1cfiohvrscorepsdio3 Compensation Configuration (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_CFG)—Offset 830h" on page 3705	00078080h
834h	4	"C71p1cfiohvrscorepsdio3 Compensation Override (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_OV)—Offset 834h" on page 3706	003F001Fh
838h	4	"C71p1cfiohvrscorepsdio3 Compensation Initial Values (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_INIT)—Offset 838h" on page 3707	0000FFFFh
83Ch	4	"C71p1cfiohvrscorepsdio3 Compensation DFX Override (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_DFX)—Offset 83Ch" on page 3707	01000080h
840h	4	"C71p1cfiohvrscoreplpc Compensation Configuration (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_CFG)—Offset 840h" on page 3708	00078080h
844h	4	"C71p1cfiohvrscoreplpc Compensation Override (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_OV)—Offset 844h" on page 3710	001F000Fh
848h	4	"C71p1cfiohvrscoreplpc Compensation Initial Values (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_INIT)—Offset 848h" on page 3710	0000FFFFh
84Ch	4	"C71p1cfiohvrscoreplpc Compensation DFX Override (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_DFX)—Offset 84Ch" on page 3711	01000080h

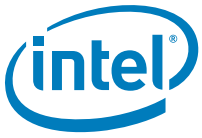


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
850h	4	"Aza1 Strength Group (cfio_regs_aza1_STRENGTH)—Offset 850h" on page 3711	BABECAFEh
854h	4	"Clkreq Strength Group (cfio_regs_clkreq_STRENGTH)—Offset 854h" on page 3712	0003000Fh
858h	4	"Crt I2c Clk Strength Group (cfio_regs_crt_i2c_clk_STRENGTH)—Offset 858h" on page 3712	00020002h
85Ch	4	"Crt I2c Data Strength Group (cfio_regs_crt_i2c_data_STRENGTH)—Offset 85Ch" on page 3713	00020002h
860h	4	"Hsi Strength Group (cfio_regs_hsi_STRENGTH)—Offset 860h" on page 3713	0003000Fh
864h	4	"I2c Strength Group (cfio_regs_i2c_STRENGTH)—Offset 864h" on page 3714	0003000Fh
868h	4	"Lpc Strength Group (cfio_regs_lpc_STRENGTH)—Offset 868h" on page 3714	BABECAFEh
86Ch	4	"Mmc3 Strength Group (cfio_regs_mmc3_STRENGTH)—Offset 86Ch" on page 3715	BABECAFEh
870h	4	"Mvt Mmc3 Strength Group (cfio_regs_mvt_mmc3_STRENGTH)—Offset 870h" on page 3715	0003000Fh
874h	4	"Mvt Rcomp Strength Group (cfio_regs_mvt_rcomp_STRENGTH)—Offset 874h" on page 3716	BABECAFEh
878h	4	"Nfc Strength Group (cfio_regs_nfc_STRENGTH)—Offset 878h" on page 3716	0003000Fh
87Ch	4	"Pltclk Strength Group (cfio_regs_pltclk_STRENGTH)—Offset 87Ch" on page 3717	0003000Fh
880h	4	"Pwm Strength Group (cfio_regs_pwm_STRENGTH)—Offset 880h" on page 3717	0003000Fh
884h	4	"Sata Strength Group (cfio_regs_sata_STRENGTH)—Offset 884h" on page 3718	0003000Fh
888h	4	"Smb Strength Group (cfio_regs_smb_STRENGTH)—Offset 888h" on page 3718	0003000Fh
88Ch	4	"Spi Strength Group (cfio_regs_spi_STRENGTH)—Offset 88Ch" on page 3719	0003000Fh
890h	4	"Spkr Strength Group (cfio_regs_spkr_STRENGTH)—Offset 890h" on page 3719	0003000Fh
894h	4	"Ssp Strength Group (cfio_regs_ssp_STRENGTH)—Offset 894h" on page 3720	0003000Fh
898h	4	"Uart1 Strength Group (cfio_regs_uart1_STRENGTH)—Offset 898h" on page 3720	0003000Fh
89Ch	4	"Aza1 Electrical Group (cfio_regs_aza1_ELECTRICAL)—Offset 89Ch" on page 3721	00000003h
8A0h	4	"Aza2 Electrical Group (cfio_regs_aza2_ELECTRICAL)—Offset 8A0h" on page 3721	00000003h

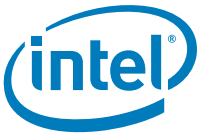


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
8A4h	4	"Clkreq Electrical Group (cfio_regs_clkreq_ELECTRICAL)—Offset 8A4h" on page 3722	00000003h
8A8h	4	"Crt Electrical Group (cfio_regs_crt_ELECTRICAL)—Offset 8A8h" on page 3723	0000002Bh
8ACh	4	"Crt I2c Clk Electrical Group (cfio_regs_crt_i2c_clk_ELECTRICAL)—Offset 8ACh" on page 3724	00000014h
8B0h	4	"Crt I2c Data Electrical Group (cfio_regs_crt_i2c_data_ELECTRICAL)—Offset 8B0h" on page 3724	00000014h
8B4h	4	"Hsi Electrical Group (cfio_regs_hsi_ELECTRICAL)—Offset 8B4h" on page 3725	00000003h
8B8h	4	"I2c Electrical Group (cfio_regs_i2c_ELECTRICAL)—Offset 8B8h" on page 3726	00000003h
8BCh	4	"Lpc Electrical Group (cfio_regs_lpc_ELECTRICAL)—Offset 8BCh" on page 3726	0000002Bh
8C0h	4	"Mmc1 Electrical Group (cfio_regs_mmc1_ELECTRICAL)—Offset 8C0h" on page 3727	00000003h
8C4h	4	"Mmc1 Clk Electrical Group (cfio_regs_mmc1_clk_ELECTRICAL)—Offset 8C4h" on page 3728	00000003h
8C8h	4	"Mmc2 Electrical Group (cfio_regs_mmc2_ELECTRICAL)—Offset 8C8h" on page 3728	00000003h
8CCh	4	"Mmc3 Electrical Group (cfio_regs_mmc3_ELECTRICAL)—Offset 8CCh" on page 3729	0000002Bh
8D0h	4	"Mmc3 Cd Electrical Group (cfio_regs_mmc3_cd_ELECTRICAL)—Offset 8D0h" on page 3730	00000003h
8D4h	4	"Mvt Mmc3 Electrical Group (cfio_regs_mvt_mmc3_ELECTRICAL)—Offset 8D4h" on page 3730	00000003h
8D8h	4	"Nfc Electrical Group (cfio_regs_nfc_ELECTRICAL)—Offset 8D8h" on page 3731	00000003h
8DCh	4	"Pltclk Electrical Group (cfio_regs_pltclk_ELECTRICAL)—Offset 8DCh" on page 3732	00000003h
8E0h	4	"Pwm Electrical Group (cfio_regs_pwm_ELECTRICAL)—Offset 8E0h" on page 3732	00000003h
8E4h	4	"Sata Electrical Group (cfio_regs_sata_ELECTRICAL)—Offset 8E4h" on page 3733	00000003h
8E8h	4	"Smb Electrical Group (cfio_regs_smb_ELECTRICAL)—Offset 8E8h" on page 3734	00000003h
8ECh	4	"Spi Electrical Group (cfio_regs_spi_ELECTRICAL)—Offset 8ECh" on page 3734	00000003h
8F0h	4	"Spkr Electrical Group (cfio_regs_spkr_ELECTRICAL)—Offset 8F0h" on page 3735	00000003h
8F4h	4	"Ssp Electrical Group (cfio_regs_ssp_ELECTRICAL)—Offset 8F4h" on page 3736	00000003h

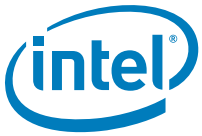


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
8F8h	4	"Uart1 Electrical Group (cfio_regs_uart1_ELECTRICAL)—Offset 8F8h" on page 3736	00000003h
8FCh	4	"Uart2 Electrical Group (cfio_regs_uart2_ELECTRICAL)—Offset 8FCh" on page 3737	00000003h
900h	4	"CFG SCORE PSB Configuration (cfio_regs_COM_CFG_SCORE_PB_CONFIG)—Offset 900h" on page 3738	01071003h
904h	4	"IRQ TYPE SCORE Interrupt Type (cfio_regs_REG_IRQ_TYPE_SCORE_IRQ_TYPE)—Offset 904h" on page 3738	00000003h
950h	4	"WR PATH SCORE Master Delay Line Write Address (cfio_regs_DLL_WR_PATH_SCORE_MDL_WRITE_PATH_C_F_ADDR)—Offset 950h" on page 3739	00080000h
954h	4	"WR PATH1 MUX SCORE Delay Line Write Multiplexer 1 (cfio_regs_DLL_WR_PATH1_MUX_SCORE_DLL_WRITE_PATH1_MUX)—Offset 954h" on page 3740	00000000h
958h	4	"WR PATH2 MUX SCORE Delay Line Write Multiplexer 2 (cfio_regs_DLL_WR_PATH2_MUX_SCORE_DLL_WRITE_PATH2_MUX)—Offset 958h" on page 3740	00000000h
95Ch	4	"WR PATH3 MUX SCORE Delay Line Write Multiplexer 3 (cfio_regs_DLL_WR_PATH3_MUX_SCORE_DLL_WRITE_PATH3_MUX)—Offset 95Ch" on page 3741	00000000h
960h	4	"FIFO SCORE Emmc Fifo Control (cfio_regs_EMMC_FIFO_SCORE_EMMC_FIFO)—Offset 960h" on page 3742	00000000h
964h	4	"INIT SCORE Master Delay Line Initial Values (cfio_regs_DLL_INIT_SCORE_MDL_CF_INIT)—Offset 964h" on page 3742	00000000h
968h	4	"SW MODE SCORE Master Delay Line Software Values (cfio_regs_DLL_SW_MODE_SCORE_MDL_CF_SW)—Offset 968h" on page 3743	00000000h
96Ch	4	"VALS SCORE Master Delay Line Fsm Values (cfio_regs_DLL_VALS_SCORE_MDL_FSM_VALS)—Offset 96Ch" on page 3744	00078000h
970h	4	"CTRL SCORE Master Delay Line Fsm Control (cfio_regs_DLL_CTRL_SCORE_MDL_FSM_CTRL)—Offset 970h" on page 3744	00000000h
980h	4	"DIRECT IRQ0 SCORE Direct Interrupt Multiplexer 0 (cfio_regs_REG_DIRECT_IRQ0_SCORE_DIRECT_IRQ_0)—Offset 980h" on page 3745	00000000h
984h	4	"DIRECT IRQ1 SCORE Direct Interrupt Multiplexer 1 (cfio_regs_REG_DIRECT_IRQ1_SCORE_DIRECT_IRQ_1)—Offset 984h" on page 3746	00000000h
988h	4	"DIRECT IRQ2 SCORE Direct Interrupt Multiplexer 2 (cfio_regs_REG_DIRECT_IRQ2_SCORE_DIRECT_IRQ_2)—Offset 988h" on page 3747	00000000h

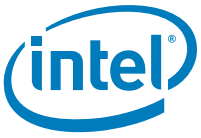


Table 75. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
98Ch	4	"DIRECT IRQ3 SCORE Direct Interrupt Multiplexer 3 (cfio_regs_REG_DIRECT_IRQ3_SCORE_DIRECT_IRQ_3)—Offset 98Ch" on page 3748	00000000h
9A0h	4	"E eMMC 4.5 delay control register (cfio_regs_SCORE_EMMC_45_DLY_CTRL)—Offset 9A0h" on page 3748	00000000h
9A4h	4	"E Emmc 4.5 max high speed mux (cfio_regs_SCORE_EMMC_45_HSMAX)—Offset 9A4h" on page 3749	00000000h
9A8h	4	"E Emmc 4.5 sdr50 speed mux (cfio_regs_SCORE_EMMC_45_SDR50)—Offset 9A8h" on page 3750	00000000h
9ACh	4	"E Emmc 4.5 ddr50 speed mux (cfio_regs_SCORE_EMMC_45_DDR50)—Offset 9ACh" on page 3751	00000000h
9B0h	4	"E Emmc 4.5 max high speed mux (cfio_regs_SCORE_EMMC_45_HSMAX)—Offset 9A4h" on page 3749	00000000h
9B4h	4	"E Emmc 4.5 norm speed mux (cfio_regs_SCORE_EMMC_45_NORM)—Offset 9B4h" on page 3752	00000000h
9B8h	4	"E Emmc 4.5 software override value (cfio_regs_SCORE_EMMC_45_OV)—Offset 9B8h" on page 3753	00000000h
9C0h	4	"E Special configuration bits (cfio_regs_SCORE_SPECIAL_BITS)—Offset 9C0h" on page 3754	00000000h
9D0h	4	"E Debounce Control (cfio_regs_SCORE_DEBOUNCE_CTRL)—Offset 9D0h" on page 3755	00000000h
9F4h	4	"E eMMC 4.5 TAP select register (cfio_regs_SCORE_TAP_SEL_REG)—Offset 9F4h" on page 3755	00000000h

3.67.1 Uart1 Rts B Pad Configuration (cfio_regs_pad_uart1_rts_b_PCONF0)—Offset 0h

PADs Memory space configuration register (access via PCU proxy)

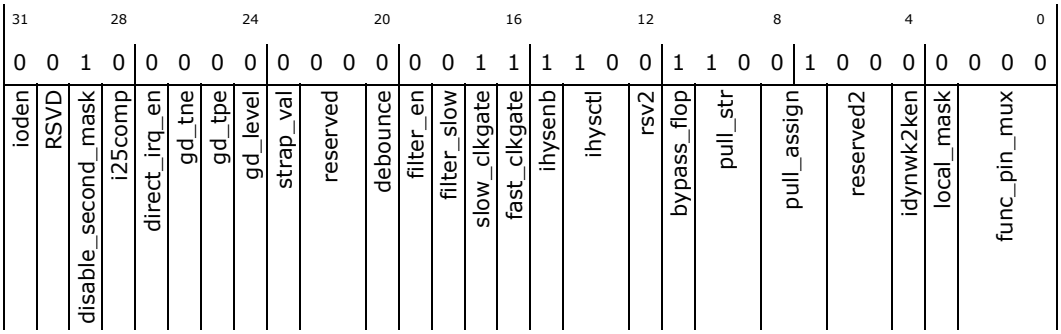
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_rts_b_PCONF0: [IOBASE] + 0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_72 function 1 is UART1_RTS_B

3.67.2 Uart1 Rts B Delay Line Multiplexer (cfio_regs_pad_uart1_rts_b_PCONF1)—Offset 4h

DLL Multiplexer

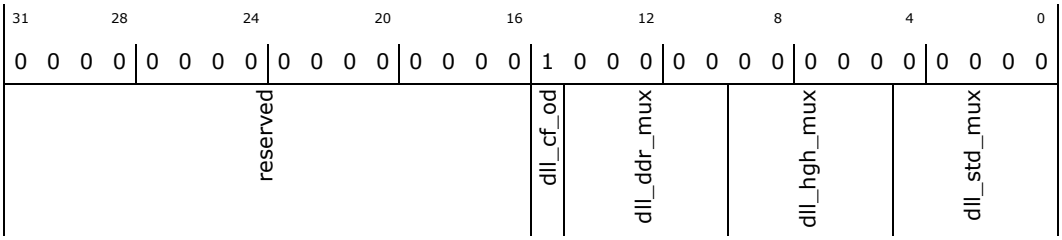
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_rts_b_PCONF1: [IOBASE] + 4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.3 Uart1 Rts B Pad Value (cfio_regs_pad_uart1_rts_b_PAD_VAL)—Offset 8h

PADs Memory space Value register (access via PCU proxy)

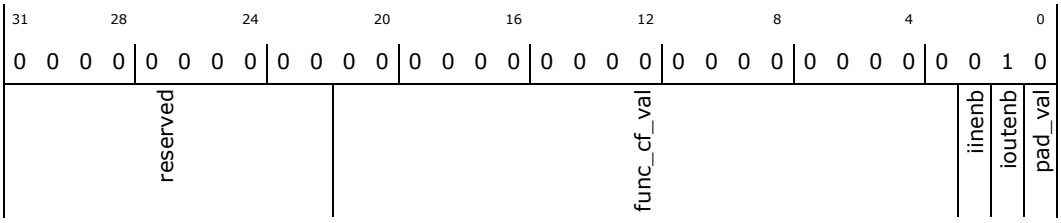
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_rts_b_PAD_VAL: [IOBASE] + 8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.4 Uart1 Txd Pad Configuration (cfio_regs_pad_uart1_txd_PCONF0)—Offset 10h

PADs Memory space configuration register (access via PCU proxy)

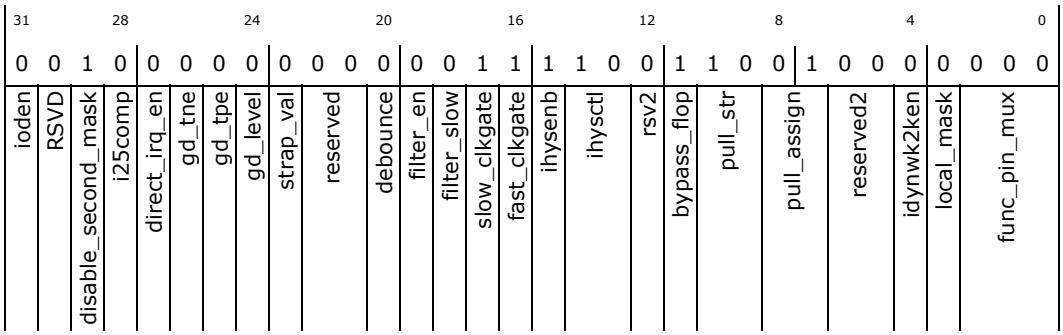
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_txd_PCONF0: [IOBASE] + 10h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_71 function 1 is UART1_TXD function 2 is MHSI_ACREADY

3.67.5 Uart1 Txd Delay Line Multiplexer (cfio_regs_pad_uart1_txd_PCONF1)—Offset 14h

DLL Multiplexer

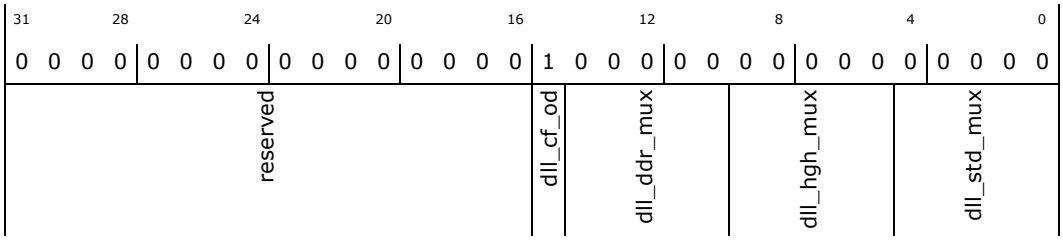
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_txd_PCONF1: [IOBASE] + 14h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.6 Uart1 Txd Pad Value (cfio_regs_pad_uart1_txd_PAD_VAL)—Offset 18h

PADs Memory space Value register (access via PCU proxy)

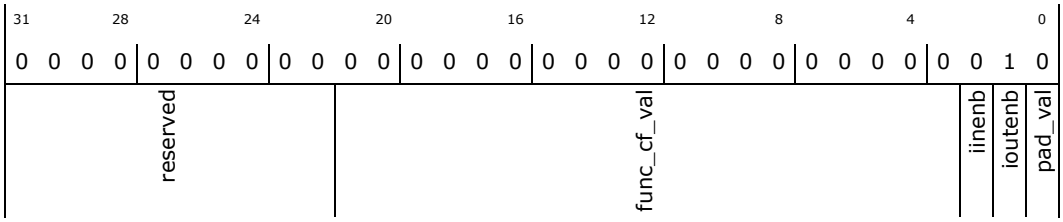
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_txd_PAD_VAL: [IOBASE] + 18h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.7 Uart1 Rxd Pad Configuration (cfio_regs_pad_uart1_rxd_PCONF0)—Offset 20h

PADs Memory space configuration register (access via PCU proxy)

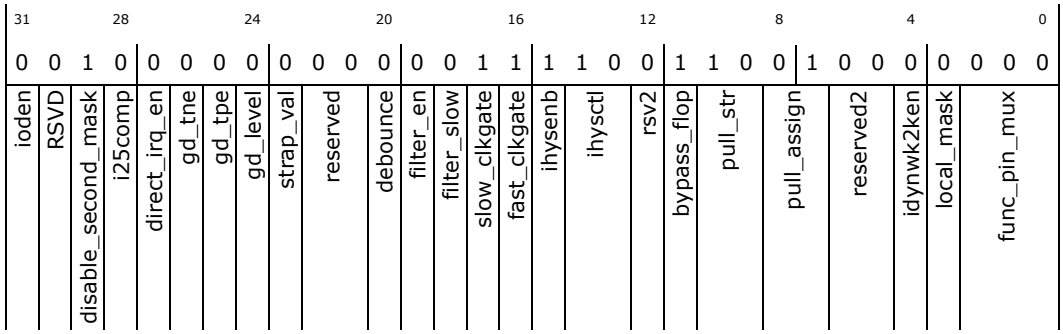
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_rxd_PCONF0: [IOBASE] + 20h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_70 function 1 is UART1_RXD function 2 is MHSI_CAREADY

3.67.8 Uart1 Rxd Delay Line Multiplexer (cfio_regs_pad_uart1_rxd_PCONF1)—Offset 24h

DLL Multiplexer

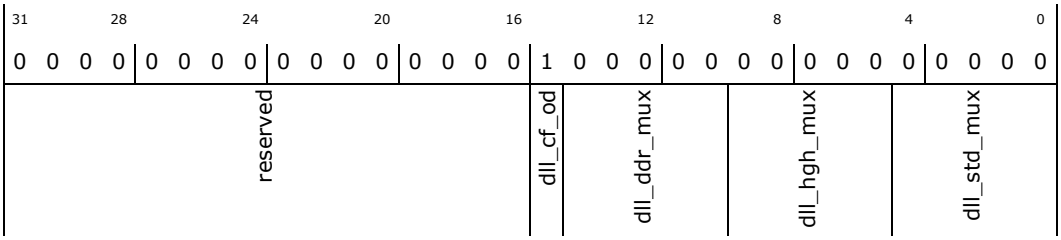
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_rxd_PCONF1: [IOBASE] + 24h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.9 Uart1 Rxd Pad Value (cfio_regs_pad_uart1_rxd_PAD_VAL)—Offset 28h

PADs Memory space Value register (access via PCU proxy)

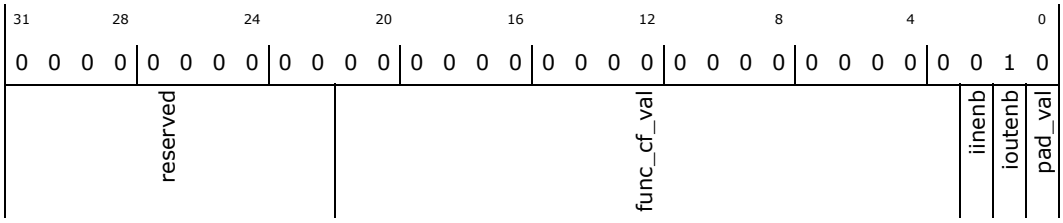
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_rxd_PAD_VAL: [IOBASE] + 28h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.10 I2c Nfc Scl Pad Configuration (cfio_regs_pad_i2c_nfc_scl_PCONF0)—Offset 30h

PADs Memory space configuration register (access via PCU proxy)

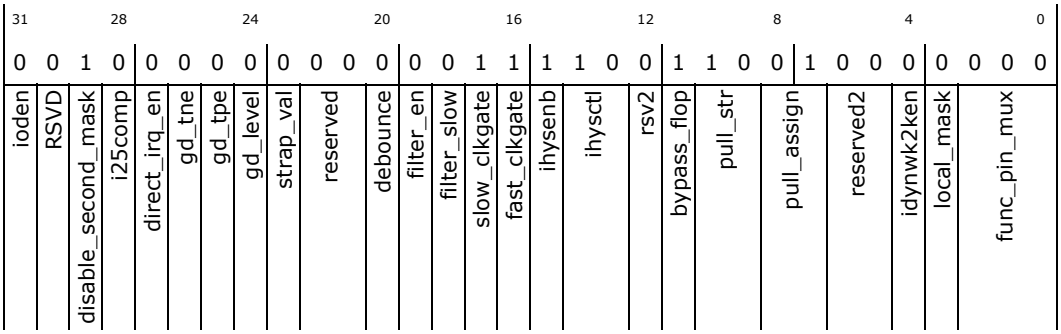
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c_nfc_scl_PCONF0: [IOBASE] + 30h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is I2C_NFC_SCL function 1 is GPIOC_93

3.67.11 I2c Nfc Scl Delay Line Multiplexer (cfio_regs_pad_i2c_nfc_scl_PCONF1)—Offset 34h

DLL Multiplexer

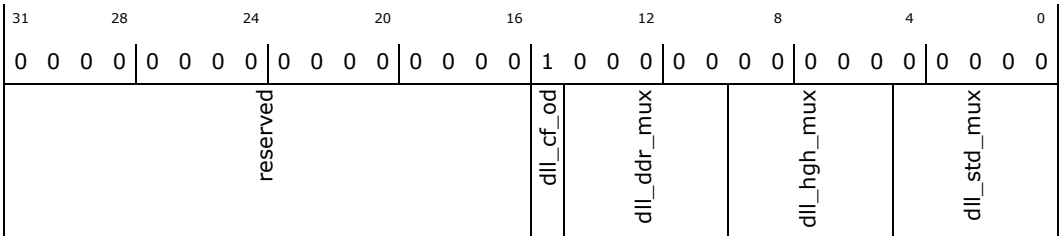
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c_nfc_scl_PCONF1: [IOBASE] + 34h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.12 I2c Nfc Scl Pad Value (cfio_regs_pad_i2c_nfc_scl_PAD_VAL)—Offset 38h

PADs Memory space Value register (access via PCU proxy)

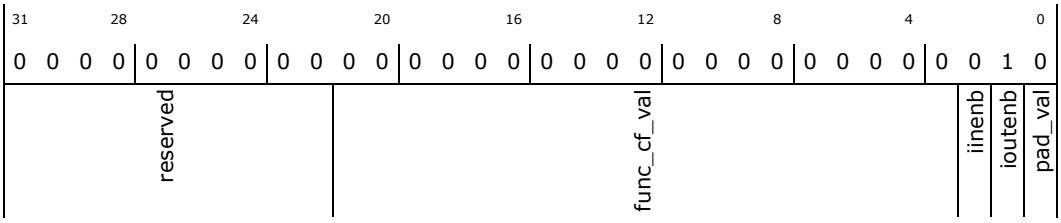
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c_nfc_scl_PAD_VAL: [IOBASE] + 38h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.13 Uart1 Cts B Pad Configuration (cfio_regs_pad_uart1_cts_b_PCONF0)—Offset 40h

PADs Memory space configuration register (access via PCU proxy)

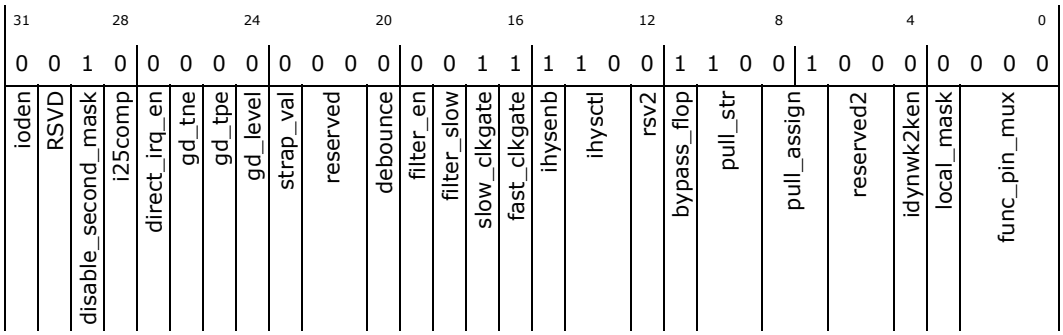
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_cts_b_PCONF0: [IOBASE] + 40h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_73 function 1 is UART1_CTS_B

3.67.14 Uart1 Cts B Delay Line Multiplexer (cfio_regs_pad_uart1_cts_b_PCONF1)—Offset 44h

DLL Multiplexer

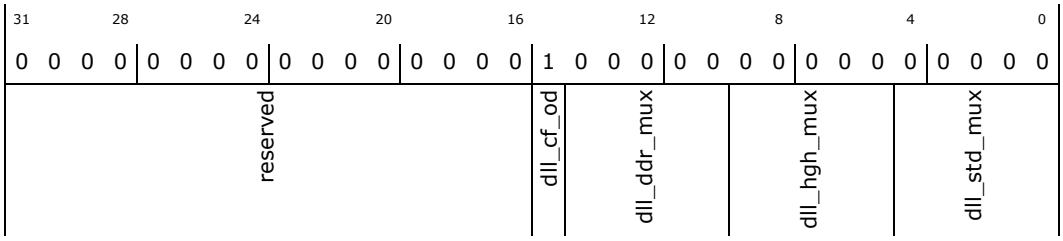
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_cts_b_PCONF1: [IOBASE] + 44h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.15 Uart1 Cts B Pad Value (cfio_regs_pad_uart1_cts_b_PAD_VAL)—Offset 48h

PADs Memory space Value register (access via PCU proxy)

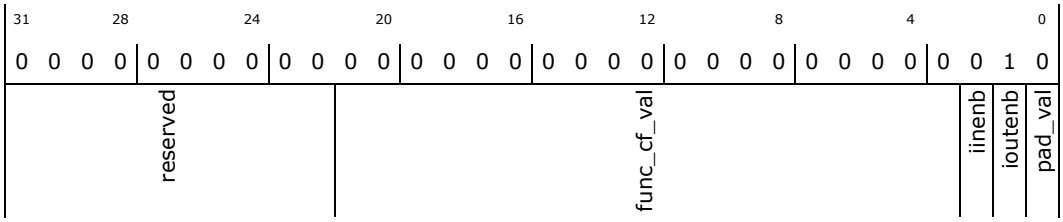
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart1_cts_b_PAD_VAL: [IOBASE] + 48h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.16 I2c Nfc Sda Pad Configuration (cfio_regs_pad_i2c_nfc_sda_PCONF0)—Offset 50h

PADs Memory space configuration register (access via PCU proxy)

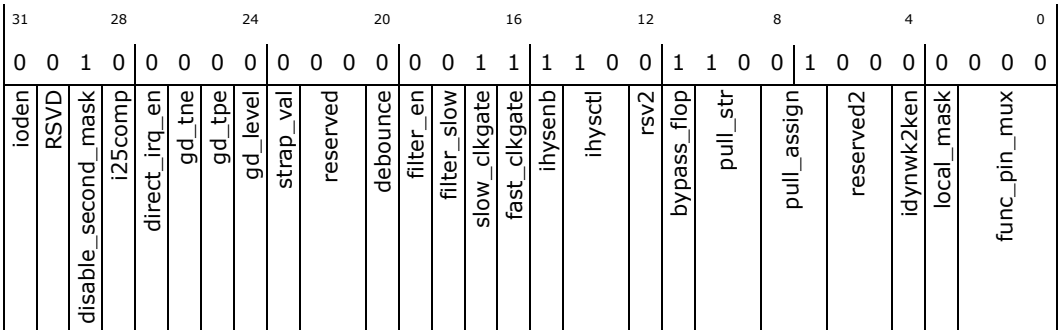
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c_nfc_sda_PCONF0: [IOBASE] + 50h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is I2C_NFC_SDA function 1 is GPIOC_92

3.67.17 I2c Nfc Sda Delay Line Multiplexer (cfio_regs_pad_i2c_nfc_sda_PCONF1)—Offset 54h

DLL Multiplexer

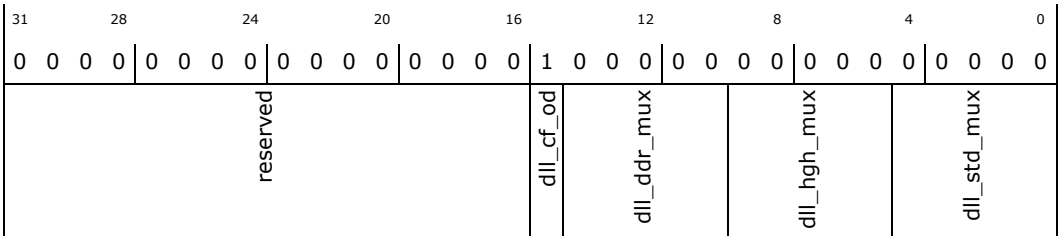
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c_nfc_sda_PCONF1: [IOBASE] + 54h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.18 I2c Nfc Sda Pad Value (cfio_regs_pad_i2c_nfc_sda_PAD_VAL)—Offset 58h

PADs Memory space Value register (access via PCU proxy)

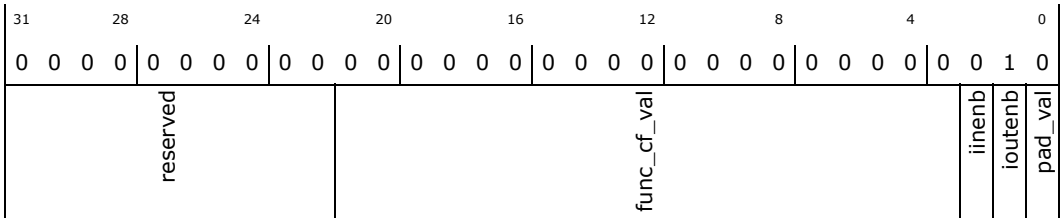
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c_nfc_sda_PAD_VAL: [IOBASE] + 58h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.19 Uart2 Rxd Pad Configuration (cfio_regs_pad_uart2_rxd_PCONF0)—Offset 60h

PADs Memory space configuration register (access via PCU proxy)

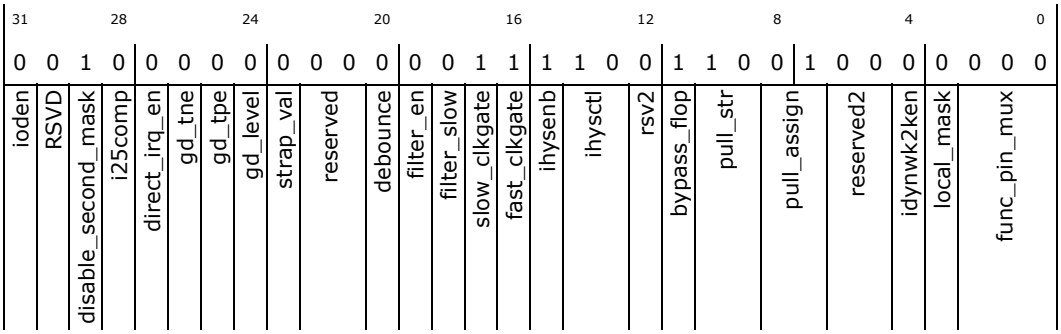
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_rxd_PCONF0: [IOBASE] + 60h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_74 function 1 is UART2_RXD

3.67.20 Uart2 Rxd Delay Line Multiplexer (cfio_regs_pad_uart2_rxd_PCONF1)—Offset 64h

DLL Multiplexer

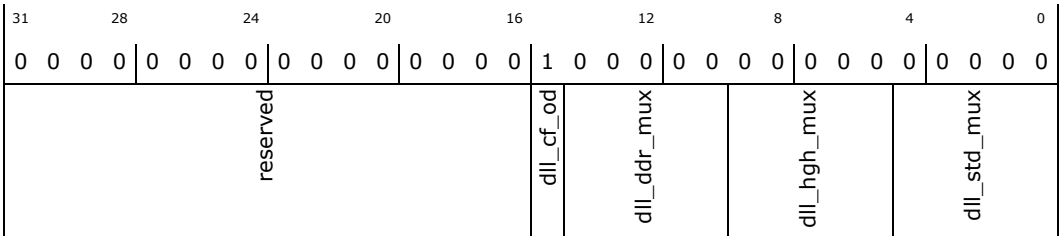
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_rxd_PCONF1: [IOBASE] + 64h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.21 Uart2 Rxd Pad Value (cfio_regs_pad_uart2_rxd_PAD_VAL)—Offset 68h

PADs Memory space Value register (access via PCU proxy)

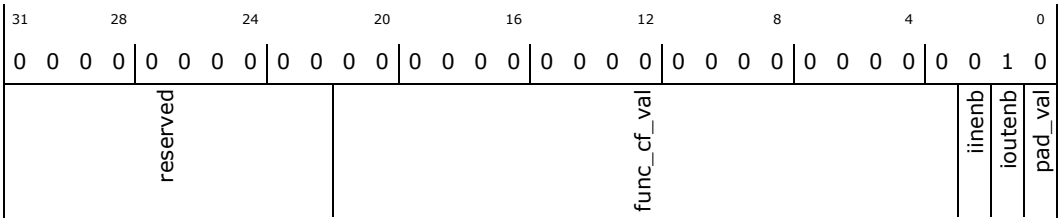
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_rxd_PAD_VAL: [IOBASE] + 68h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.22 Uart2 Txd Pad Configuration (cfio_regs_pad_uart2_txd_PCONF0)—Offset 70h

PADs Memory space configuration register (access via PCU proxy)

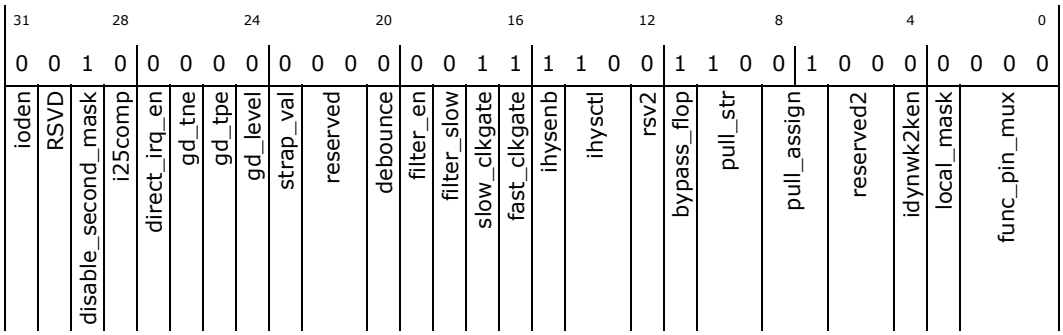
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_txd_PCONF0: [IOBASE] + 70h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_75 function 1 is UART2_TXD

3.67.23 Uart2 Txd Delay Line Multiplexer (cfio_regs_pad_uart2_txd_PCONF1)—Offset 74h

DLL Multiplexer

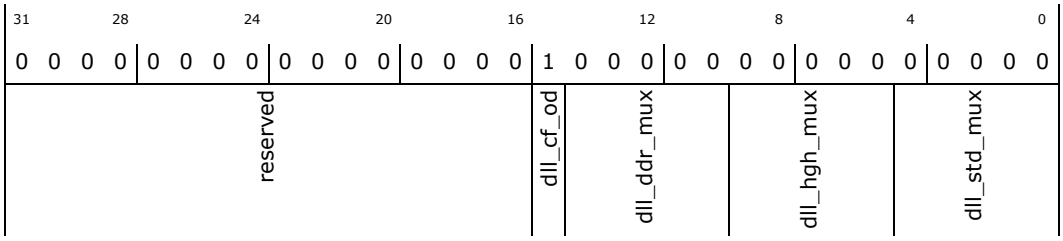
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_txd_PCONF1: [IOBASE] + 74h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.24 Uart2 Txd Pad Value (cfio_regs_pad_uart2_txd_PAD_VAL)—Offset 78h

PADs Memory space Value register (access via PCU proxy)

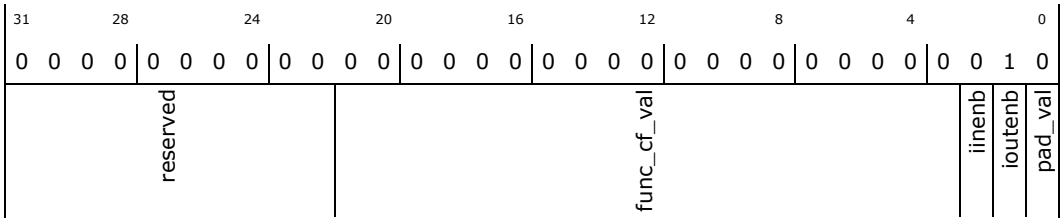
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_txd_PAD_VAL: [IOBASE] + 78h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.25 Uart2 Cts B Pad Configuration (cfio_regs_pad_uart2_cts_b_PCONF0)—Offset 80h

PADs Memory space configuration register (access via PCU proxy)

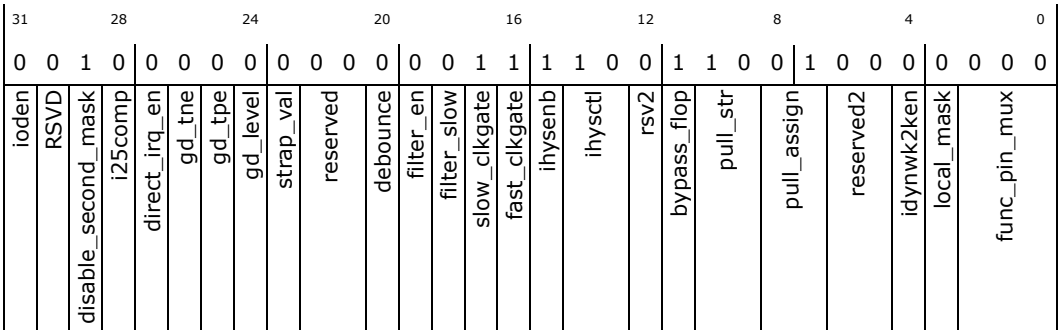
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_cts_b_PCONF0: [IOBASE] + 80h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_77 function 1 is UART2_CTS_B

3.67.26 Uart2 Cts B Delay Line Multiplexer (cfio_regs_pad_uart2_cts_b_PCONF1)—Offset 84h

DLL Multiplexer

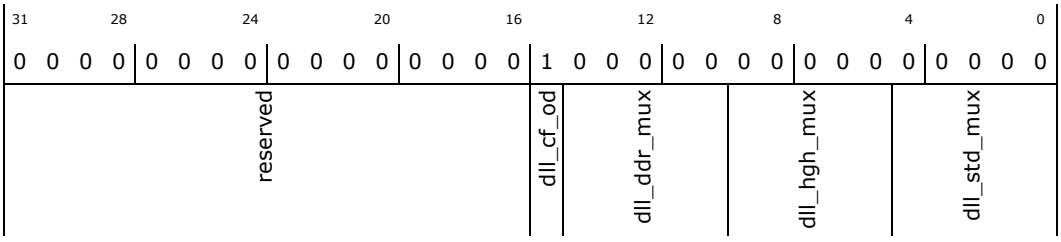
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_cts_b_PCONF1: [IOBASE] + 84h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.27 Uart2 Cts B Pad Value (cfio_regs_pad_uart2_cts_b_PAD_VAL)—Offset 88h

PADs Memory space Value register (access via PCU proxy)

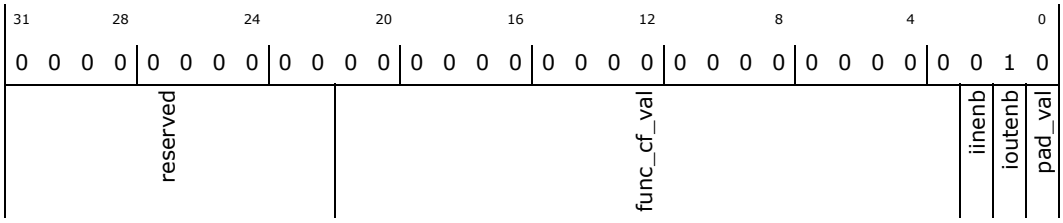
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_cts_b_PAD_VAL: [IOBASE] + 88h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.28 Uart2 Rts B Pad Configuration (cfio_regs_pad_uart2_rts_b_PCONF0)—Offset 90h

PADs Memory space configuration register (access via PCU proxy)

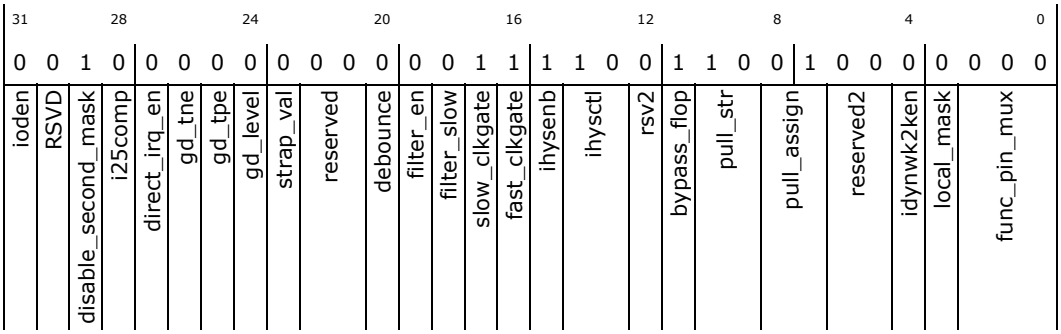
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_rts_b_PCONF0: [IOBASE] + 90h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_76 function 1 is UART2_RTS_B

3.67.29 Uart2 Rts B Delay Line Multiplexer (cfio_regs_pad_uart2_rts_b_PCONF1)—Offset 94h

DLL Multiplexer

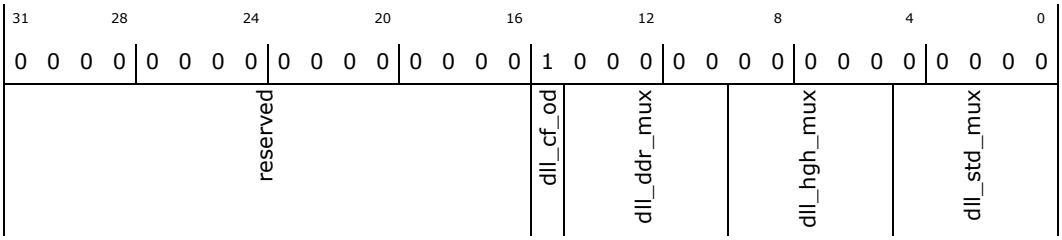
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_rts_b_PCONF1: [IOBASE] + 94h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.30 Uart2 Rts B Pad Value (cfio_regs_pad_uart2_rts_b_PAD_VAL)—Offset 98h

PADs Memory space Value register (access via PCU proxy)

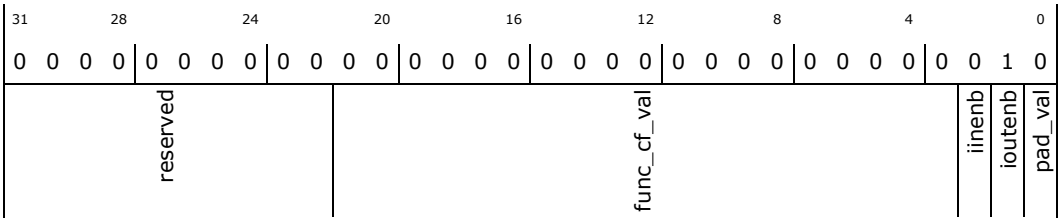
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_uart2_rts_b_PAD_VAL: [IOBASE] + 98h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.31 Pwm0 Pad Configuration (cfio_regs_pad_pwm0_PCONF0)—Offset A0h

PADs Memory space configuration register (access via PCU proxy)

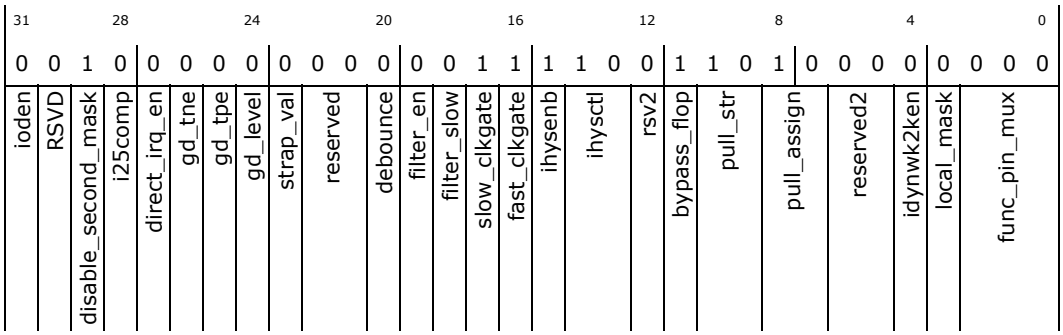
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pwm0_PCONF0: [IOBASE] + A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_94 function 1 is PWM0

3.67.32 Pwm0 Delay Line Multiplexer (cfio_regs_pad_pwm0_PCONF1)—Offset A4h

DLL Multiplexer

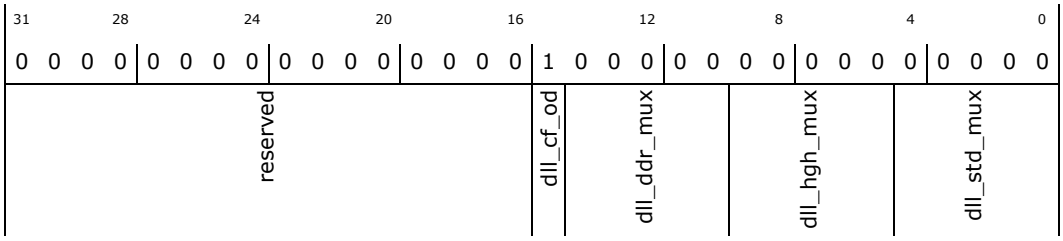
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pwm0_PCONF1: [IOBASE] + A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.33 Pwm0 Pad Value (cfio_regs_pad_pwm0_PAD_VAL)—Offset A8h

PADs Memory space Value register (access via PCU proxy)

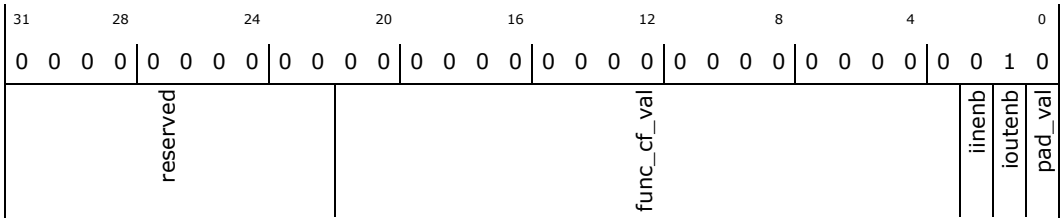
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pwm0_PAD_VAL: [IOBASE] + A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.34 Pwm1 Pad Configuration (cfio_regs_pad_pwm1_PCONF0)—Offset B0h

PADs Memory space configuration register (access via PCU proxy)

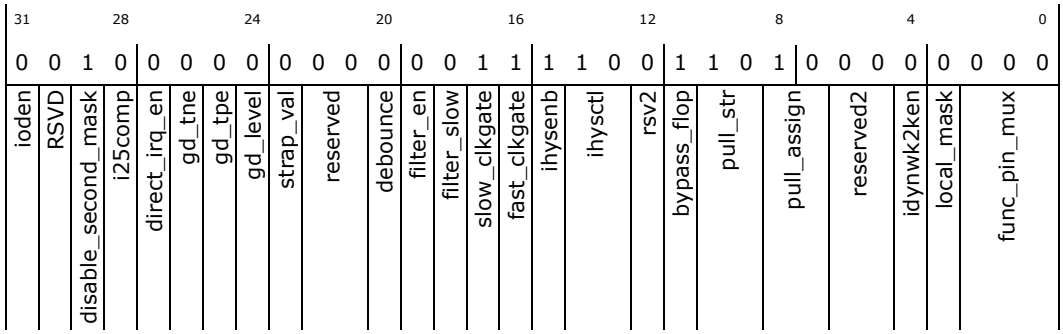
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pwm1_PCONF0: [IOBASE] + B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_95 function 1 is PWM1

3.67.35 Pwm1 Delay Line Multiplexer (cfio_regs_pad_pwm1_PCONF1)—Offset B4h

DLL Multiplexer

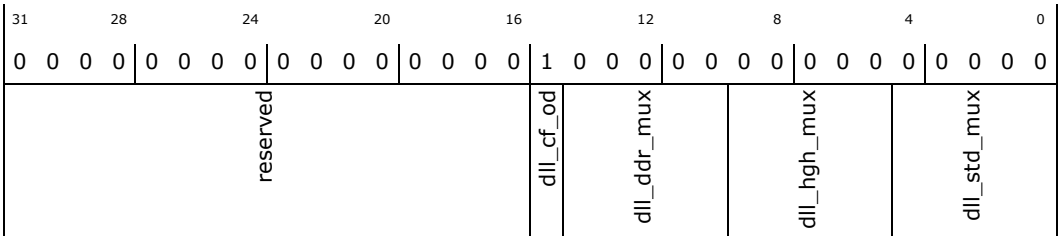
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pwm1_PCONF1: [IOBASE] + B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.36 Pwm1 Pad Value (cfio_regs_pad_pwm1_PAD_VAL)—Offset B8h

PADs Memory space Value register (access via PCU proxy)

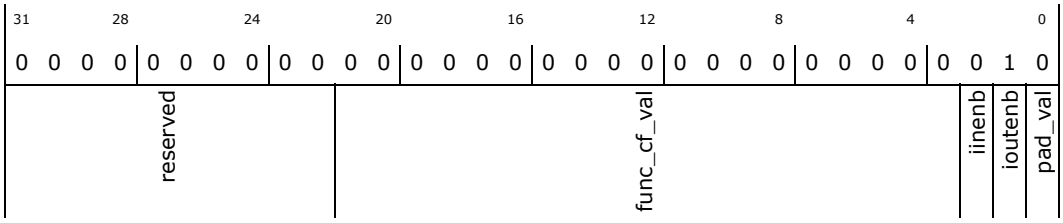
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pwm1_PAD_VAL: [IOBASE] + B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.37 Gp Ssp 2 Fs Pad Configuration (cfio_regs_pad_gp_ssp_2_fs_PCONF0)—Offset C0h

PADs Memory space configuration register (access via PCU proxy)

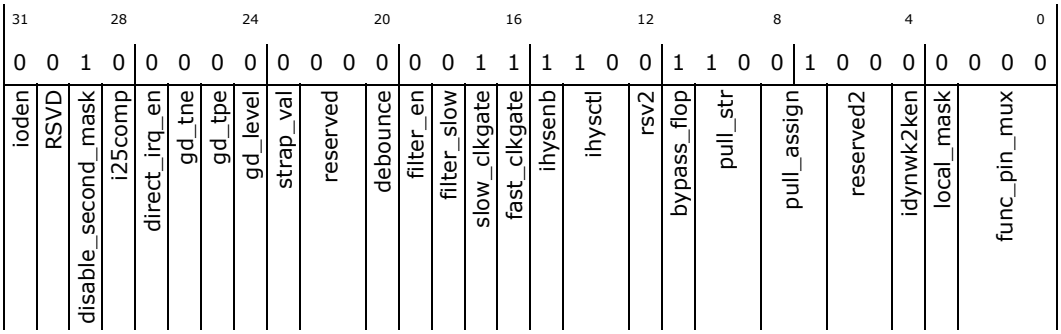
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_fs_PCONF0: [IOBASE] + C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_63 function 1 is GP_SSP_2_FS For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10 function 2 is MHSI_CAWAKE For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

3.67.38 Gp Ssp 2 Fs Delay Line Multiplexer (cfio_regs_pad_gp_ssp_2_fs_PCONF1)—Offset C4h

DLL Multiplexer

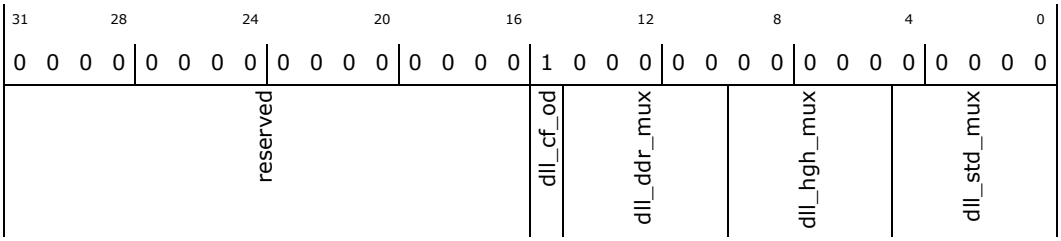
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_fs_PCONF1: [IOBASE] + C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.39 Gp Ssp 2 Fs Pad Value (cfio_regs_pad_gp_ssp_2_fs_PAD_VAL)—Offset C8h

PADs Memory space Value register (access via PCU proxy)

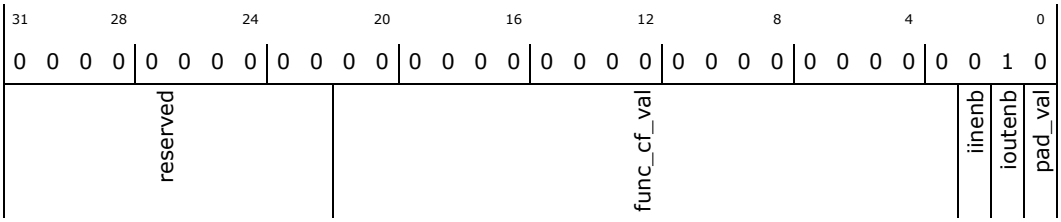
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_fs_PAD_VAL: [IOBASE] + C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low

Bit Range	Default & Access	Description
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.40 Gp Ssp 2 Clk Pad Configuration (cfio_regs_pad_gp_ssp_2_clk_PCONF0)—Offset D0h

PADs Memory space configuration register (access via PCU proxy)

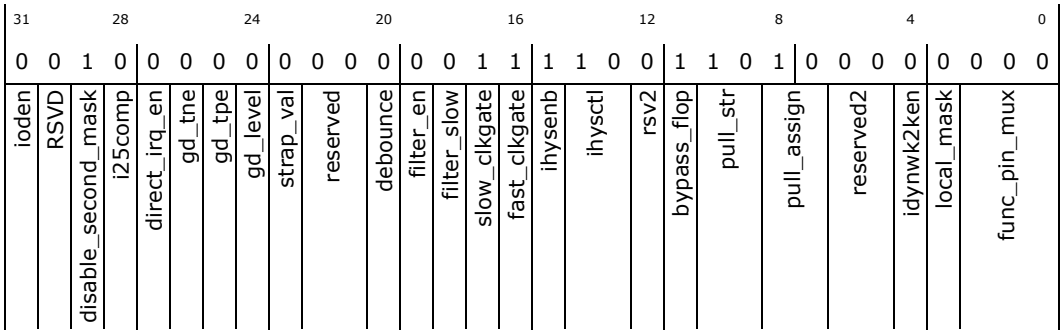
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_clk_PCONF0: [IOBASE] + D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_62 function 1 is GP_SSP_2_CLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is SATA_DEVSLP1 function 3 is EDM_CFIO

3.67.41 Gp Ssp 2 Clk Delay Line Multiplexer (cfio_regs_pad_gp_ssp_2_clk_PCONF1)—Offset D4h

DLL Multiplexer

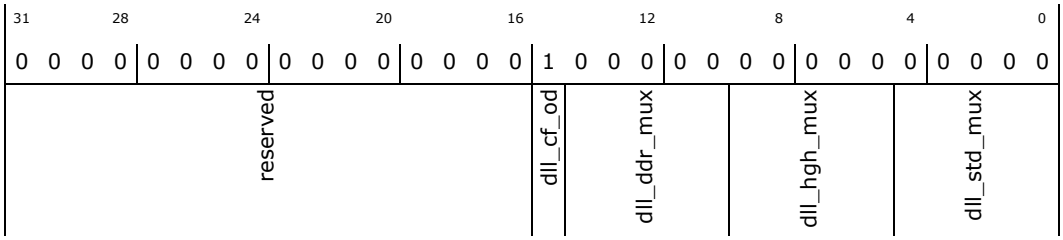
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_clk_PCONF1: [IOBASE] + D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.42 Gp Ssp 2 Clk Pad Value (cfio_regs_pad_gp_ssp_2_clk_PAD_VAL)—Offset D8h

PADs Memory space Value register (access via PCU proxy)

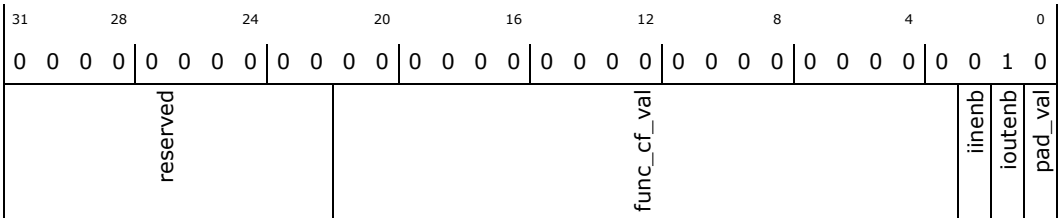
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_clk_PAD_VAL: [IOBASE] + D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.43 Gp Ssp 2 Txd Pad Configuration (cfio_regs_pad_gp_ssp_2_txd_PCONF0)—Offset E0h

PADs Memory space configuration register (access via PCU proxy)

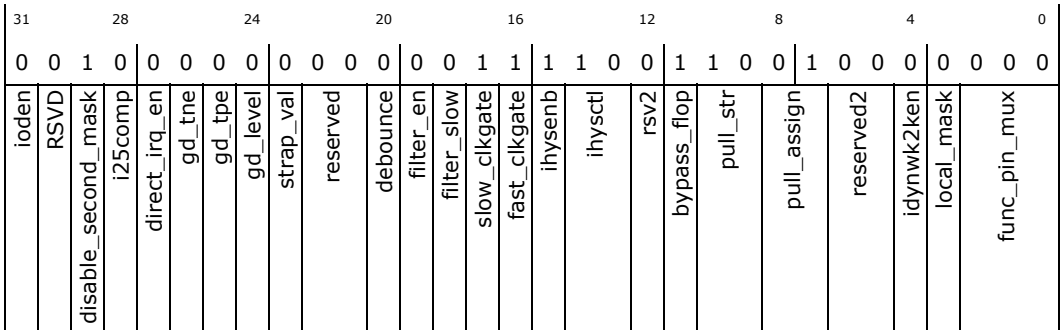
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_txd_PCONF0: [IOBASE] + E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_65 function 1 is GP_SSP_2_TXD For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

3.67.44 Gp Ssp 2 Txd Delay Line Multiplexer (cfio_regs_pad_gp_ssp_2_txd_PCONF1)—Offset E4h

DLL Multiplexer

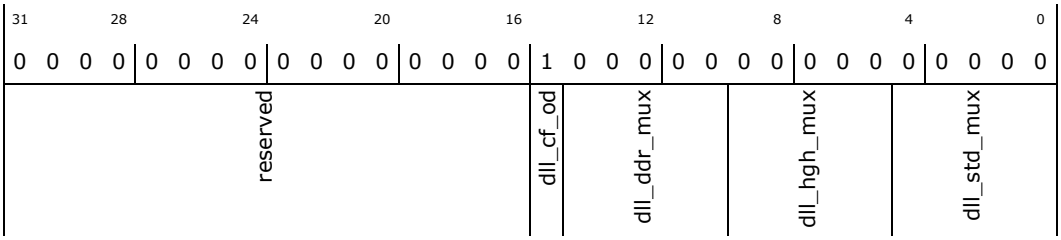
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_txd_PCONF1: [IOBASE] + E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.45 Gp Ssp 2 Txd Pad Value (cfio_regs_pad_gp_ssp_2_txd_PAD_VAL)—Offset E8h

PADs Memory space Value register (access via PCU proxy)

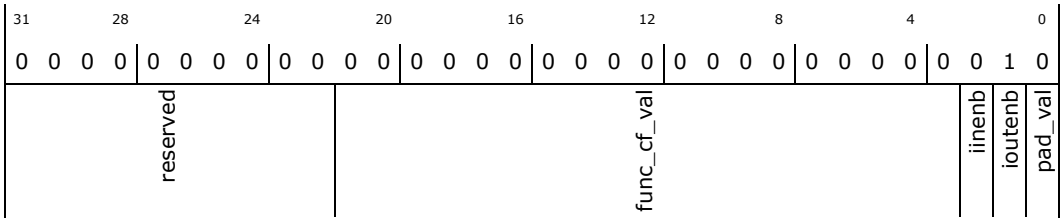
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_txd_PAD_VAL: [IOBASE] + E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.46 Gp Ssp 2 Rxd Pad Configuration (cfio_regs_pad_gp_ssp_2_rxd_PCONF0)—Offset F0h

PADs Memory space configuration register (access via PCU proxy)

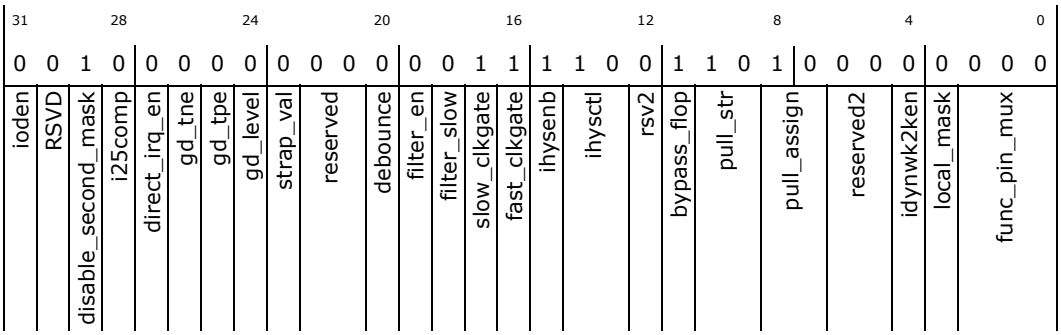
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_rxd_PCONF0: [IOBASE] + F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_64 function 1 is GP_SSP_2_RXD

3.67.47 Gp Ssp 2 Rxd Delay Line Multiplexer (cfio_regs_pad_gp_ssp_2_rxd_PCONF1)—Offset F4h

DLL Multiplexer

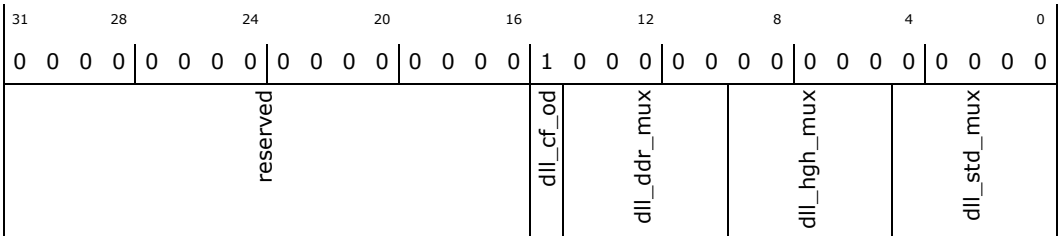
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_rxd_PCONF1: [IOBASE] + F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.48 Gp Ssp 2 Rxd Pad Value (cfio_regs_pad_gp_ssp_2_rxd_PAD_VAL)—Offset F8h

PADs Memory space Value register (access via PCU proxy)

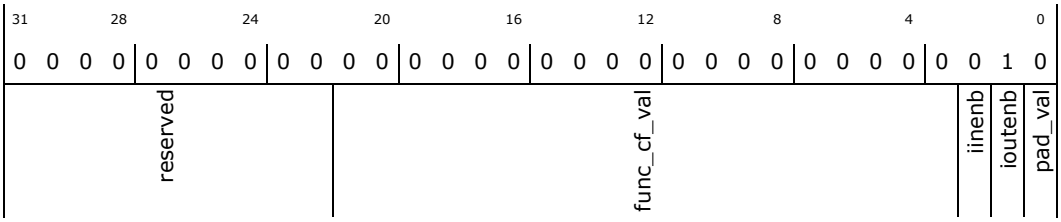
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gp_ssp_2_rxd_PAD_VAL: [IOBASE] + F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.49 Spi1 Clk Pad Configuration (cfio_regs_pad_spi1_clk_PCONF0)—Offset 100h

PADs Memory space configuration register (access via PCU proxy)

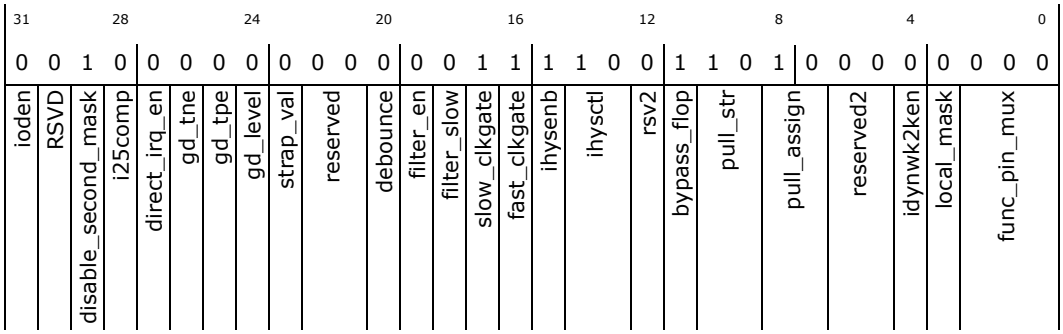
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_clk_PCONF0: [IOBASE] + 100h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_69 function 1 is SPI1_CLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01

3.67.50 Spi1 Clk Delay Line Multiplexer (cfio_regs_pad_spi1_clk_PCONF1)—Offset 104h

DLL Multiplexer

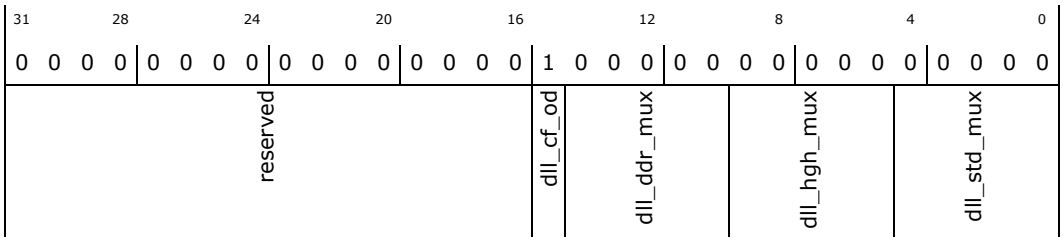
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_clk_PCONF1: [IOBASE] + 104h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.51 Spi1 Clk Pad Value (cfio_regs_pad_spi1_clk_PAD_VAL)—Offset 108h

PADs Memory space Value register (access via PCU proxy)

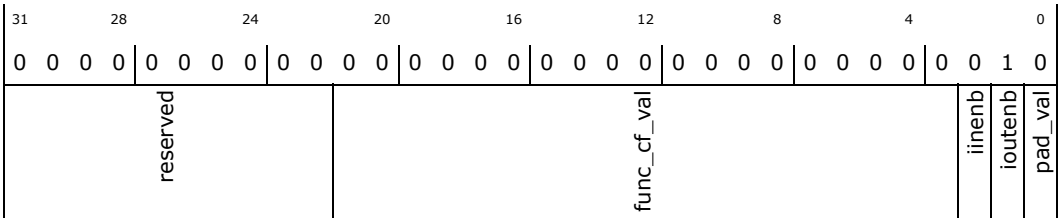
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_clk_PAD_VAL: [IOBASE] + 108h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.52 Spi1 Cs0 B Pad Configuration (cfio_regs_pad_spi1_cs0_b_PCONF0)—Offset 110h

PADs Memory space configuration register (access via PCU proxy)

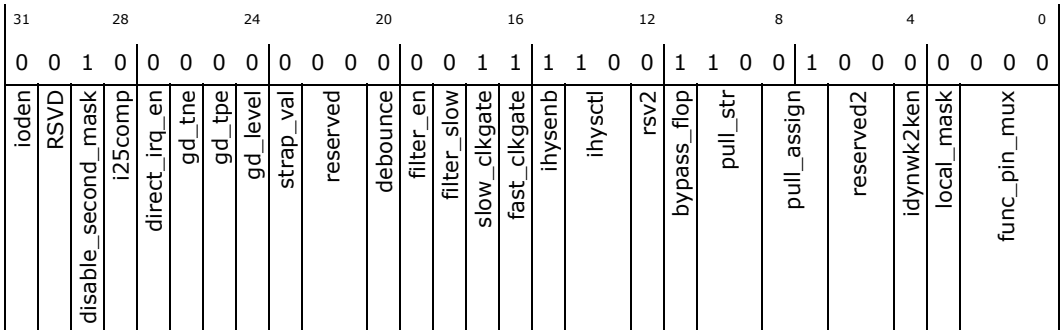
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_cs0_b_PCONF0: [IOBASE] + 110h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_66 function 1 is SPI1_CS0_B For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

3.67.53 Spi1 Cs0 B Delay Line Multiplexer (cfio_regs_pad_spi1_cs0_b_PCONF1)—Offset 114h

DLL Multiplexer

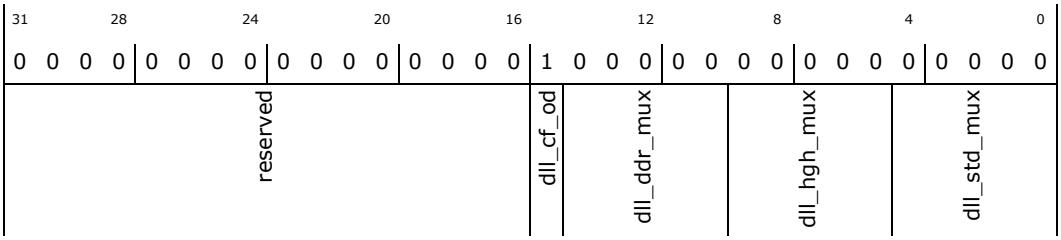
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_cs0_b_PCONF1: [IOBASE] + 114h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.54 Spi1 Cs0 B Pad Value (cfio_regs_pad_spi1_cs0_b_PAD_VAL)—Offset 118h

PADs Memory space Value register (access via PCU proxy)

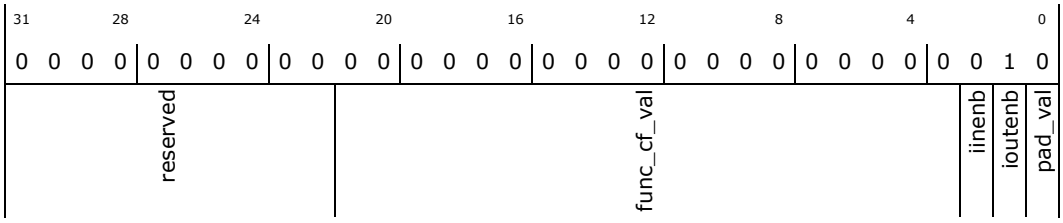
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_cs0_b_PAD_VAL: [IOBASE] + 118h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.55 Spi1 Miso Pad Configuration (cfio_regs_pad_spi1_miso_PCONF0)—Offset 120h

PADs Memory space configuration register (access via PCU proxy)

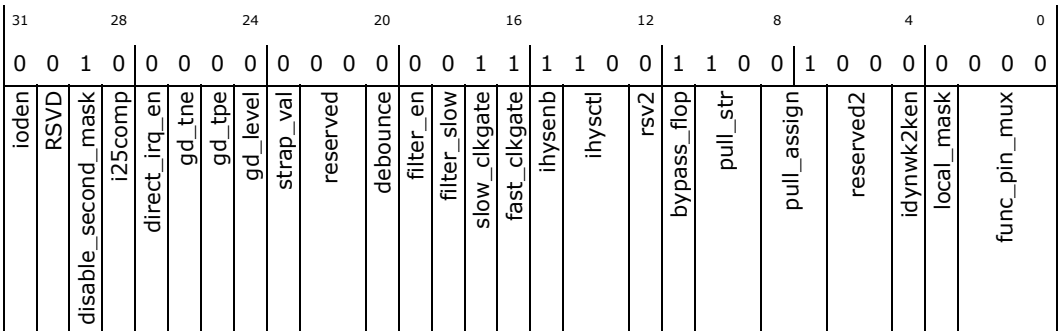
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_miso_PCONF0: [IOBASE] + 120h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_67 function 1 is SPI1_MISO

3.67.56 Spi1 Miso Delay Line Multiplexer (cfio_regs_pad_spi1_miso_PCONF1)—Offset 124h

DLL Multiplexer

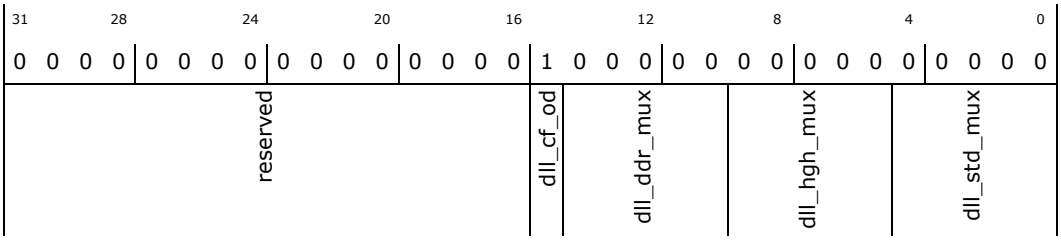
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_miso_PCONF1: [IOBASE] + 124h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.57 Spi1 Miso Pad Value (cfio_regs_pad_spi1_miso_PAD_VAL)—Offset 128h

PADs Memory space Value register (access via PCU proxy)

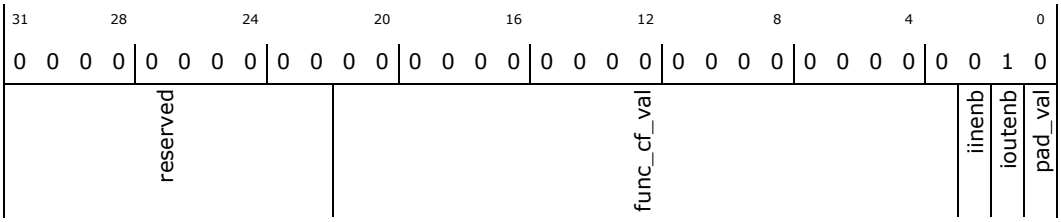
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_miso_PAD_VAL: [IOBASE] + 128h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.58 Spi1 Mosi Pad Configuration (cfio_regs_pad_spi1_mosi_PCONF0)—Offset 130h

PADs Memory space configuration register (access via PCU proxy)

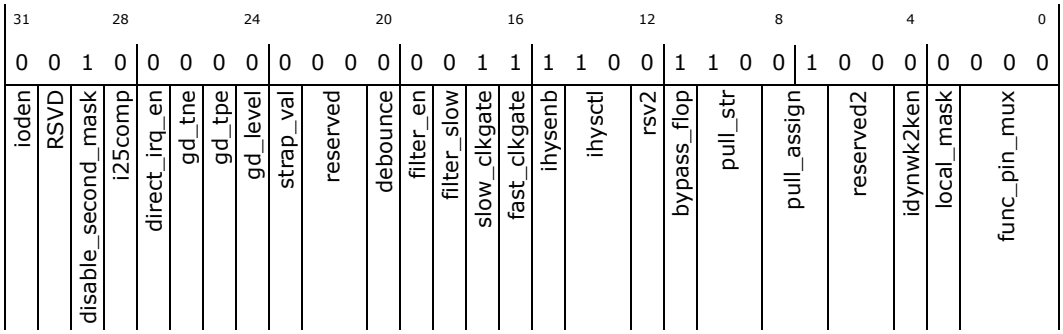
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_mosi_PCONF0: [IOBASE] + 130h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_68 function 1 is SPI1_MOSI

3.67.59 Spi1 Mosi Delay Line Multiplexer (cfio_regs_pad_spi1_mosi_PCONF1)—Offset 134h

DLL Multiplexer

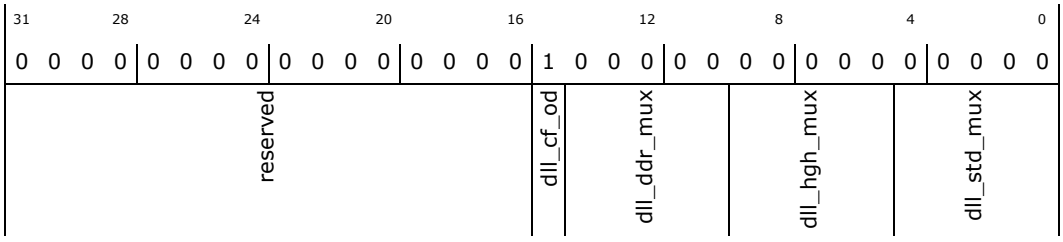
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_mosi_PCONF1: [IOBASE] + 134h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.60 Spi1 Mosi Pad Value (cfio_regs_pad_spi1_mosi_PAD_VAL)—Offset 138h

PADs Memory space Value register (access via PCU proxy)

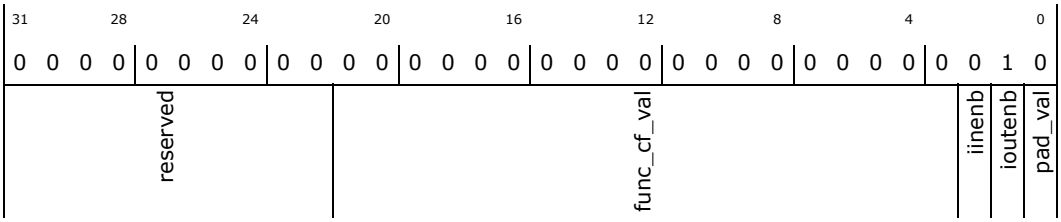
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi1_mosi_PAD_VAL: [IOBASE] + 138h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.61 I2c5 Scl Pad Configuration (cfio_regs_pad_i2c5_scl_PCONF0)—Offset 140h

PADs Memory space configuration register (access via PCU proxy)

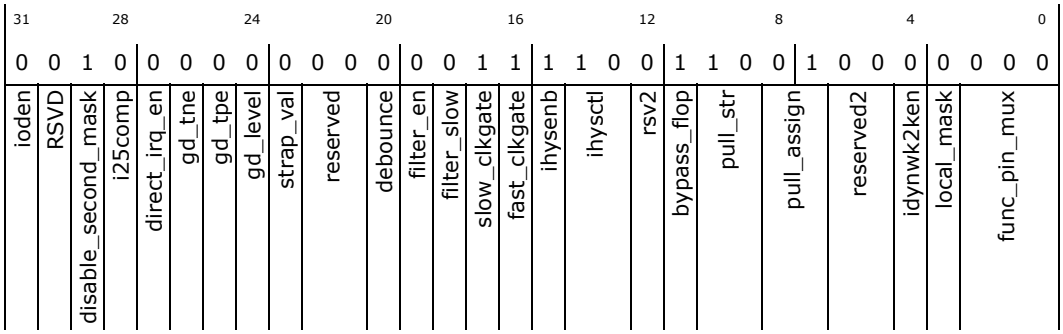
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c5_scl_PCONF0: [IOBASE] + 140h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_89 function 1 is I2C5_SCL

3.67.62 I2c5 Scl Delay Line Multiplexer (cfio_regs_pad_i2c5_scl_PCONF1)—Offset 144h

DLL Multiplexer

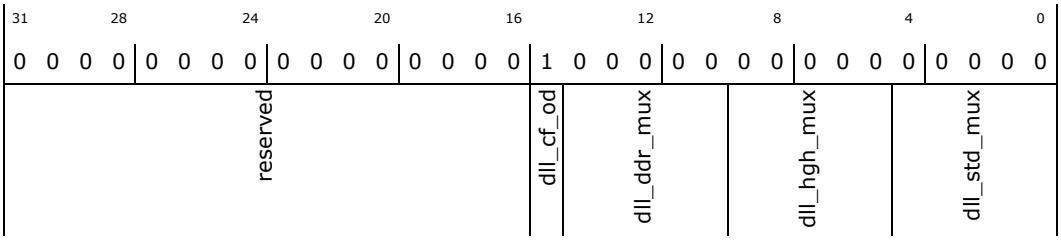
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c5_scl_PCONF1: [IOBASE] + 144h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.63 I2c5 Scl Pad Value (cfio_regs_pad_i2c5_scl_PAD_VAL)—Offset 148h

PADs Memory space Value register (access via PCU proxy)

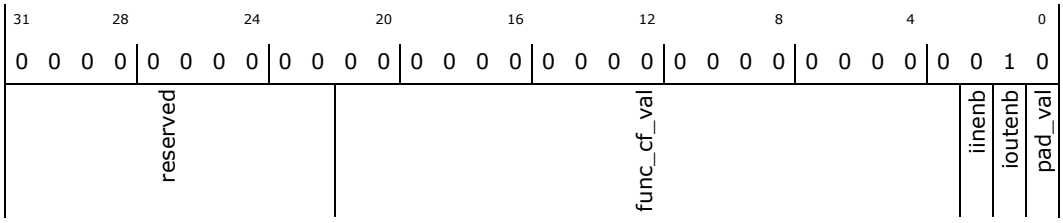
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c5_scl_PAD_VAL: [IOBASE] + 148h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.64 I2c5 Sda Pad Configuration (cfio_regs_pad_i2c5_sda_PCONF0)—Offset 150h

PADs Memory space configuration register (access via PCU proxy)

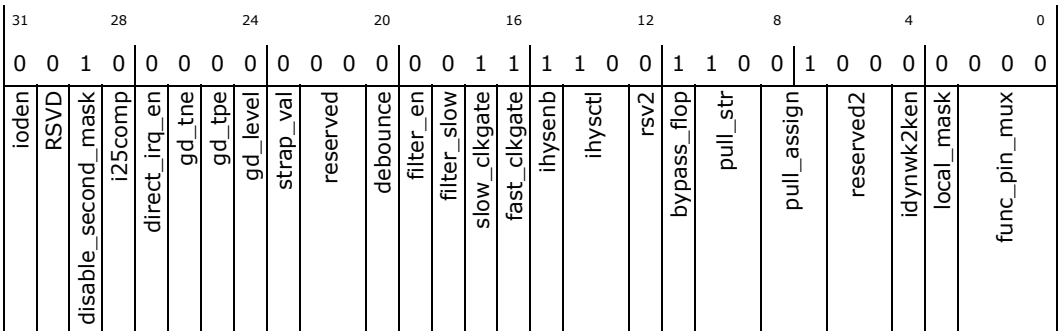
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c5_sda_PCONF0: [IOBASE] + 150h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_88 function 1 is I2C5_SDA

3.67.65 I2c5 Sda Delay Line Multiplexer (cfio_regs_pad_i2c5_sda_PCONF1)—Offset 154h

DLL Multiplexer

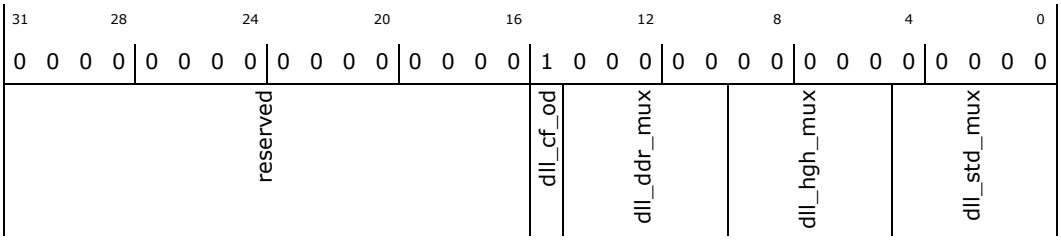
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c5_sda_PCONF1: [IOBASE] + 154h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.66 I2c5 Sda Pad Value (cfio_regs_pad_i2c5_sda_PAD_VAL)—Offset 158h

PADs Memory space Value register (access via PCU proxy)

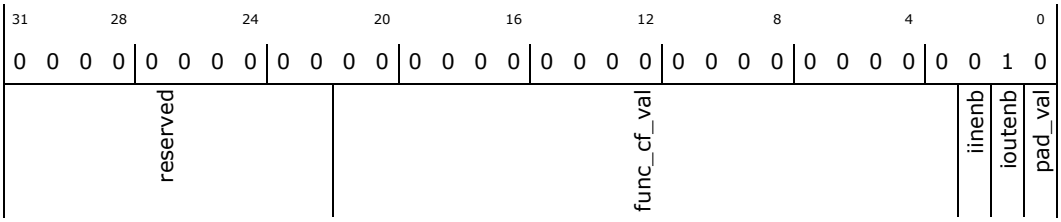
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c5_sda_PAD_VAL: [IOBASE] + 158h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.67 I2c6 Scl Pad Configuration (cfio_regs_pad_i2c6_scl_PCONF0)—Offset 160h

PADs Memory space configuration register (access via PCU proxy)

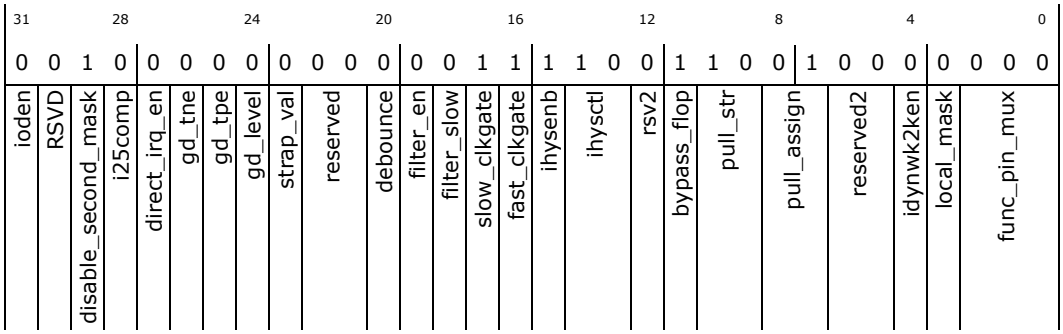
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c6_scl_PCONF0: [IOBASE] + 160h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_91 function 1 is I2C6_SCL function 2 is SDMMC3_WP

3.67.68 I2c6 Scl Delay Line Multiplexer (cfio_regs_pad_i2c6_scl_PCONF1)—Offset 164h

DLL Multiplexer

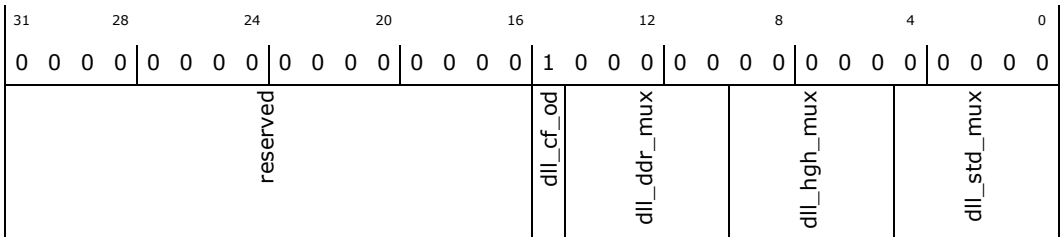
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c6_scl_PCONF1: [IOBASE] + 164h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.69 I2c6 Scl Pad Value (cfio_regs_pad_i2c6_scl_PAD_VAL)—Offset 168h

PADs Memory space Value register (access via PCU proxy)

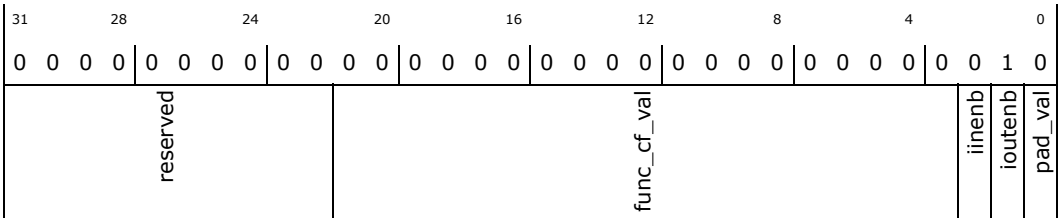
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c6_scl_PAD_VAL: [IOBASE] + 168h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.70 I2c4 Scl Pad Configuration (cfio_regs_pad_i2c4_scl_PCONF0)—Offset 170h

PADs Memory space configuration register (access via PCU proxy)

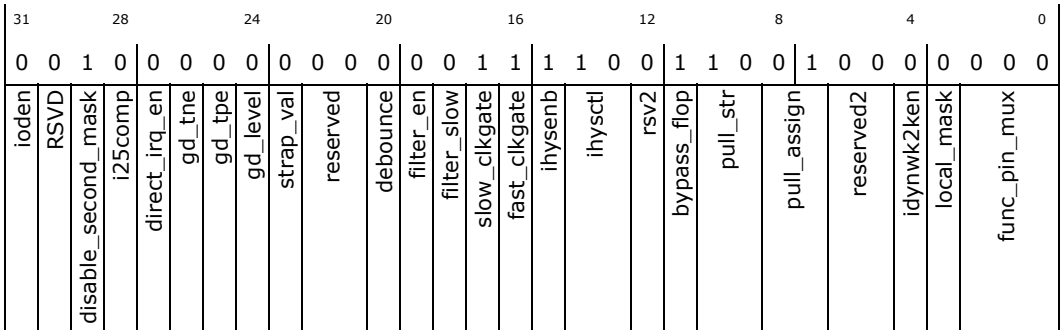
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c4_scl_PCONF0: [IOBASE] + 170h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_87 function 1 is I2C4_SCL

3.67.71 I2c4 Scl Delay Line Multiplexer (cfio_regs_pad_i2c4_scl_PCONF1)—Offset 174h

DLL Multiplexer

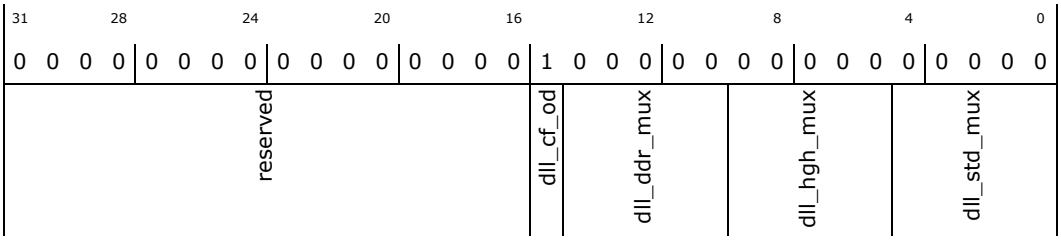
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c4_scl_PCONF1: [IOBASE] + 174h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.72 I2c4 Scl Pad Value (cfio_regs_pad_i2c4_scl_PAD_VAL)—Offset 178h

PADs Memory space Value register (access via PCU proxy)

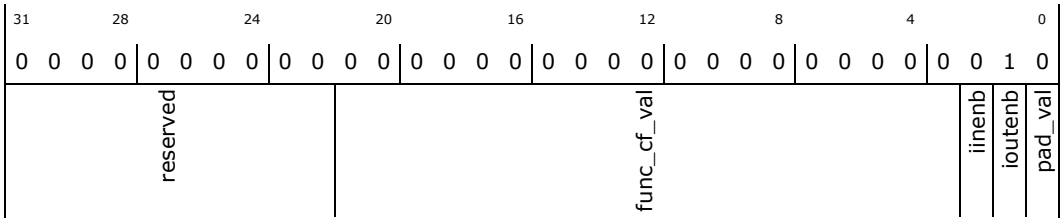
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c4_scl_PAD_VAL: [IOBASE] + 178h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.73 I2c6 Sda Pad Configuration (cfio_regs_pad_i2c6_sda_PCONF0)—Offset 180h

PADs Memory space configuration register (access via PCU proxy)

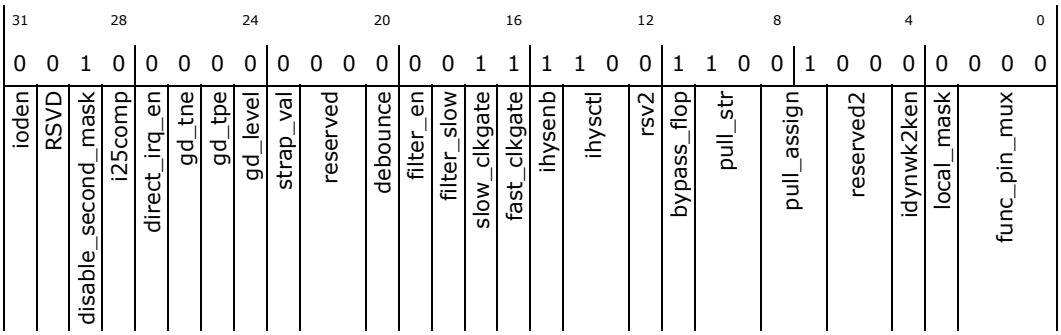
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c6_sda_PCONF0: [IOBASE] + 180h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_90 function 1 is I2C6_SDA function 2 is NMI For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

3.67.74 I2c6 Sda Delay Line Multiplexer (cfio_regs_pad_i2c6_sda_PCONF1)—Offset 184h

DLL Multiplexer

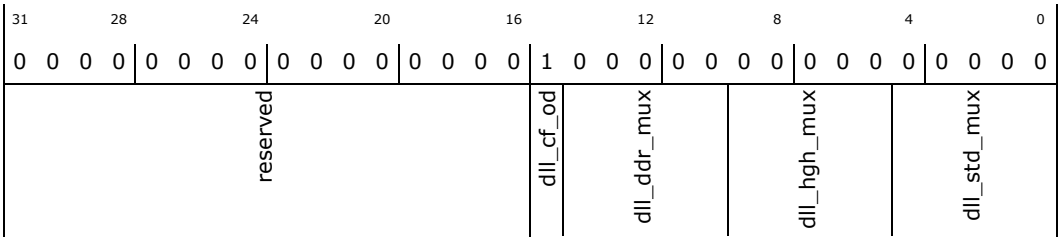
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c6_sda_PCONF1: [IOBASE] + 184h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.75 I2c6 Sda Pad Value (cfio_regs_pad_i2c6_sda_PAD_VAL)—Offset 188h

PADs Memory space Value register (access via PCU proxy)

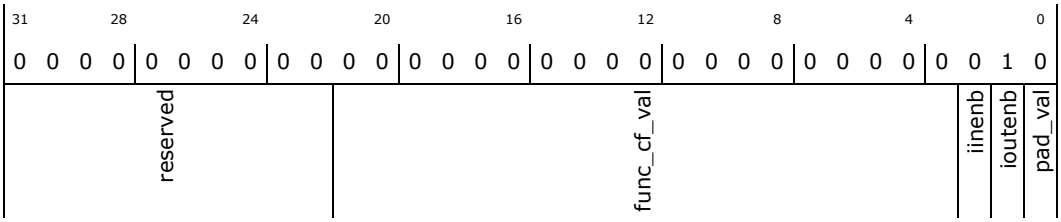
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c6_sda_PAD_VAL: [IOBASE] + 188h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.76 I2c3 Sda Pad Configuration (cfio_regs_pad_i2c3_sda_PCONF0)—Offset 190h

PADs Memory space configuration register (access via PCU proxy)

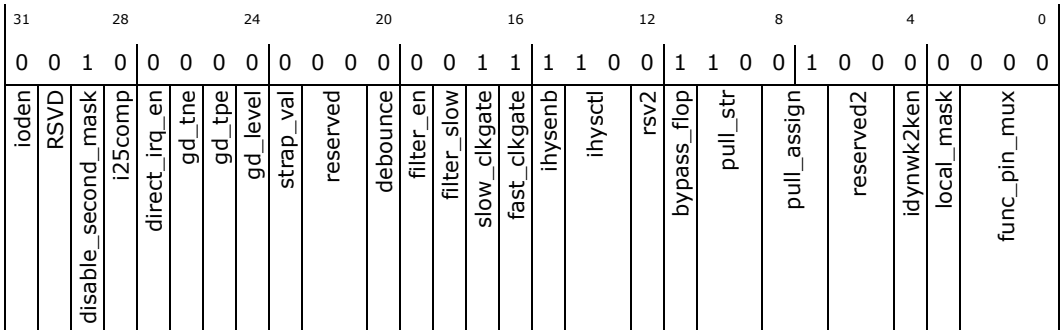
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c3_sda_PCONF0: [IOBASE] + 190h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_84 function 1 is I2C3_SDA function 2 is Unused

3.67.77 I2c3 Sda Delay Line Multiplexer (cfio_regs_pad_i2c3_sda_PCONF1)—Offset 194h

DLL Multiplexer

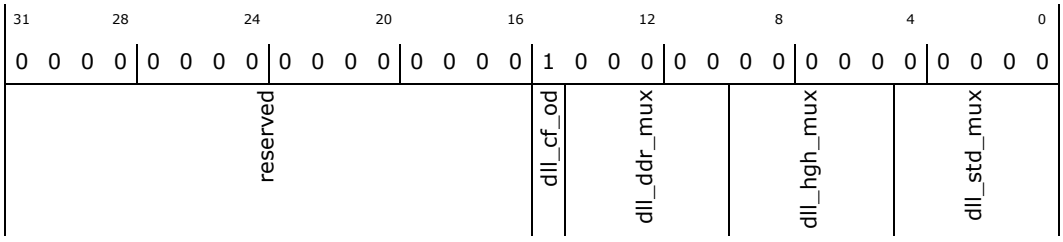
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c3_sda_PCONF1: [IOBASE] + 194h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.78 I2c3 Sda Pad Value (cfio_regs_pad_i2c3_sda_PAD_VAL)—Offset 198h

PADs Memory space Value register (access via PCU proxy)

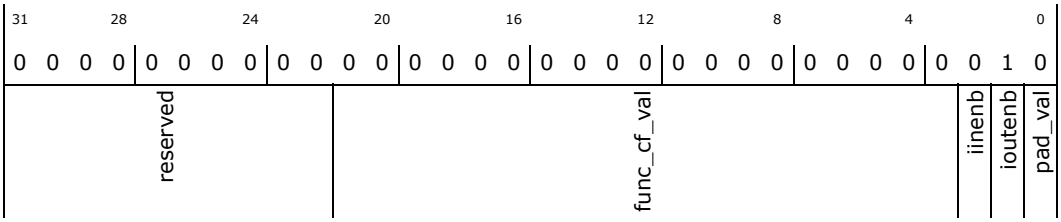
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c3_sda_PAD_VAL: [IOBASE] + 198h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.79 I2c4 Sda Pad Configuration (cfio_regs_pad_i2c4_sda_PCONF0)—Offset 1A0h

PADs Memory space configuration register (access via PCU proxy)

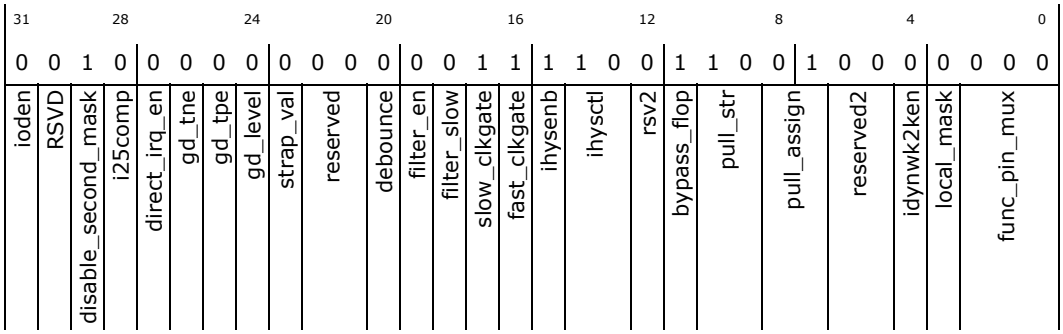
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c4_sda_PCONF0: [IOBASE] + 1A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_86 function 1 is I2C4_SDA function 2 is Unused

3.67.80 I2c4 Sda Delay Line Multiplexer (cfio_regs_pad_i2c4_sda_PCONF1)—Offset 1A4h

DLL Multiplexer

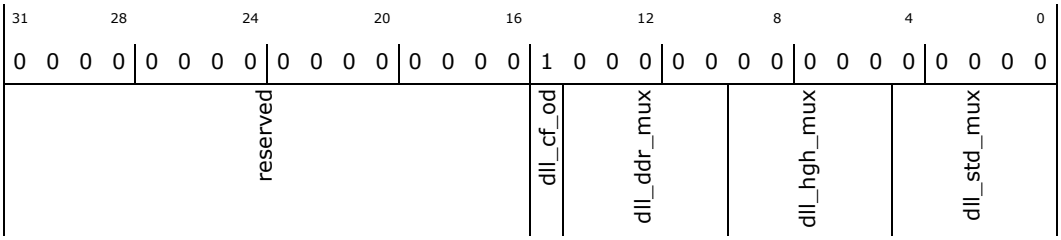
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c4_sda_PCONF1: [IOBASE] + 1A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.81 I2c4 Sda Pad Value (cfio_regs_pad_i2c4_sda_PAD_VAL)—Offset 1A8h

PADs Memory space Value register (access via PCU proxy)

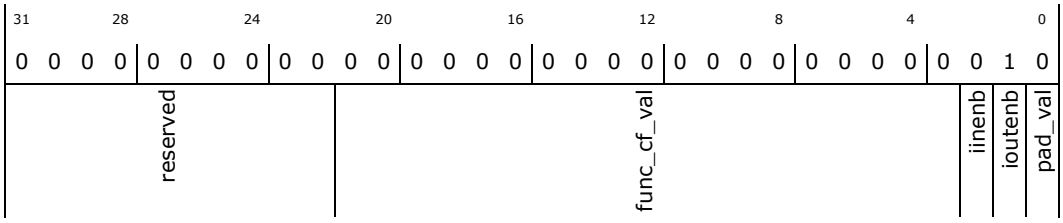
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c4_sda_PAD_VAL: [IOBASE] + 1A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.82 I2c2 Scl Pad Configuration (cfio_regs_pad_i2c2_scl_PCONF0)—Offset 1B0h

PADs Memory space configuration register (access via PCU proxy)

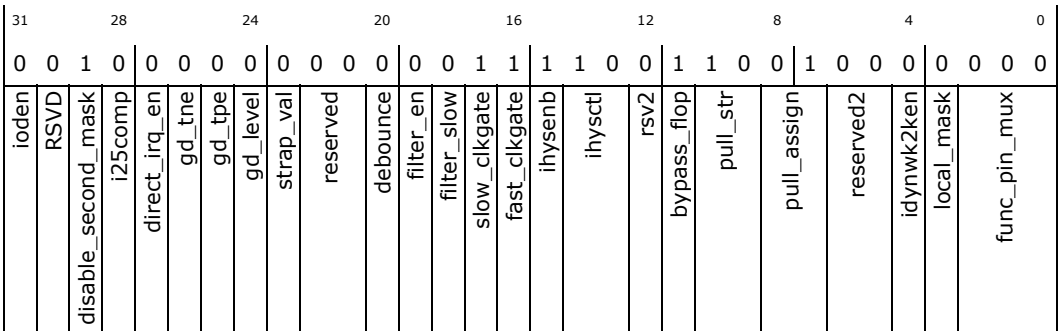
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c2_scl_PCONF0: [IOBASE] + 1B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_83 function 1 is I2C2_SCL function 2 is Unused

3.67.83 I2c2 Scl Delay Line Multiplexer (cfio_regs_pad_i2c2_scl_PCONF1)—Offset 1B4h

DLL Multiplexer

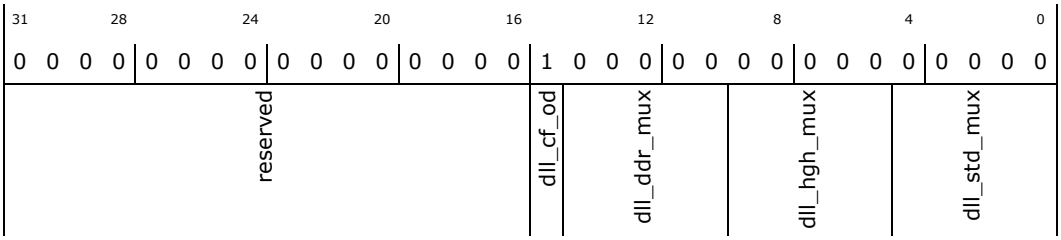
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c2_scl_PCONF1: [IOBASE] + 1B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.84 I2c2 Scl Pad Value (cfio_regs_pad_i2c2_scl_PAD_VAL)—Offset 1B8h

PADs Memory space Value register (access via PCU proxy)

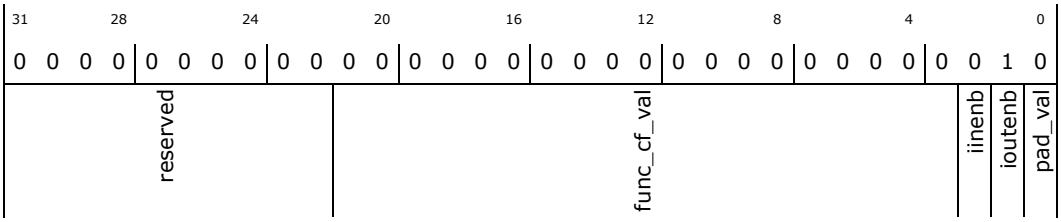
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c2_scl_PAD_VAL: [IOBASE] + 1B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.85 I2c3 Scl Pad Configuration (cfio_regs_pad_i2c3_scl_PCONF0)—Offset 1C0h

PADs Memory space configuration register (access via PCU proxy)

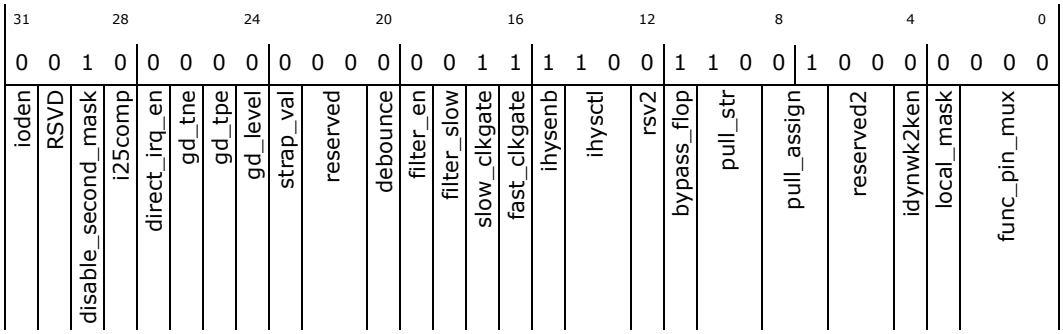
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c3_scl_PCONF0: [IOBASE] + 1C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_85 function 1 is I2C3_SCL function 2 is Unused

3.67.86 I2c3 Scl Delay Line Multiplexer (cfio_regs_pad_i2c3_scl_PCONF1)—Offset 1C4h

DLL Multiplexer

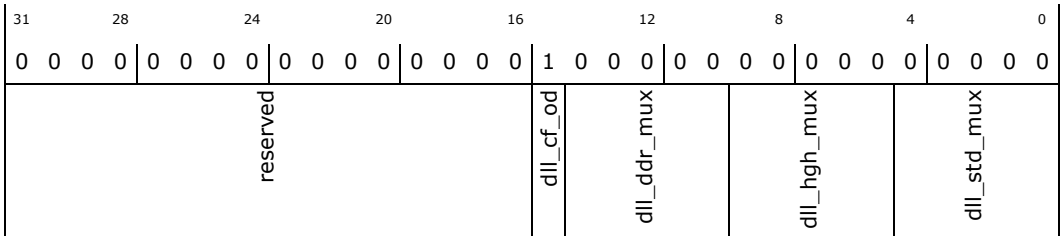
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c3_scl_PCONF1: [IOBASE] + 1C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.87 I2c3 Scl Pad Value (cfio_regs_pad_i2c3_scl_PAD_VAL)—Offset 1C8h

PADs Memory space Value register (access via PCU proxy)

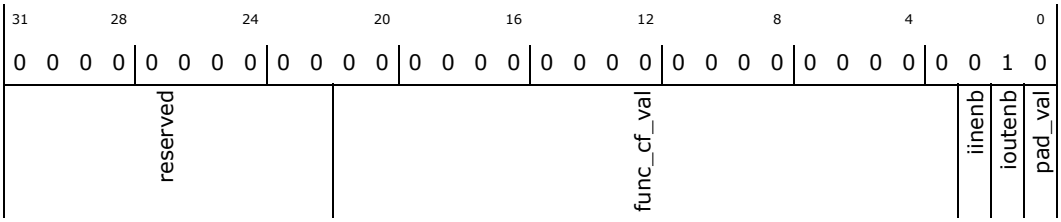
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c3_scl_PAD_VAL: [IOBASE] + 1C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.88 I2c2 Sda Pad Configuration (cfio_regs_pad_i2c2_sda_PCONF0)—Offset 1D0h

PADs Memory space configuration register (access via PCU proxy)

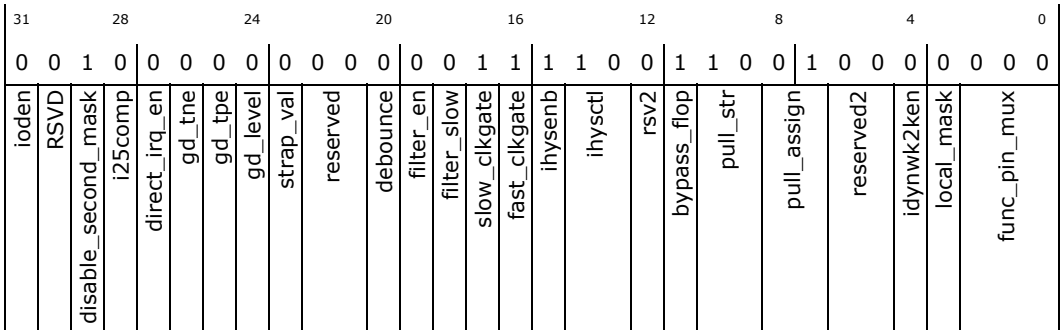
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c2_sda_PCONF0: [IOBASE] + 1D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_82 function 1 is I2C2_SDA function 2 is Unused

3.67.89 I2c2 Sda Delay Line Multiplexer (cfio_regs_pad_i2c2_sda_PCONF1)—Offset 1D4h

DLL Multiplexer

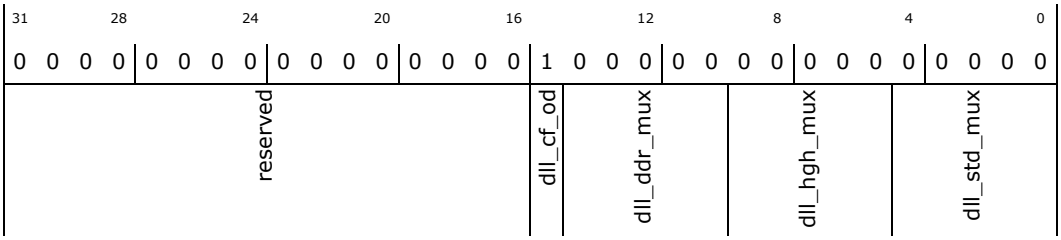
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c2_sda_PCONF1: [IOBASE] + 1D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.90 I2c2 Sda Pad Value (cfio_regs_pad_i2c2_sda_PAD_VAL)—Offset 1D8h

PADs Memory space Value register (access via PCU proxy)

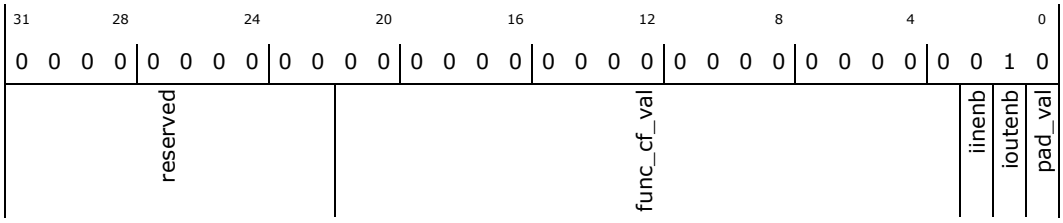
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c2_sda_PAD_VAL: [IOBASE] + 1D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.91 I2c1 Scl Pad Configuration (cfio_regs_pad_i2c1_scl_PCONF0)—Offset 1E0h

PADs Memory space configuration register (access via PCU proxy)

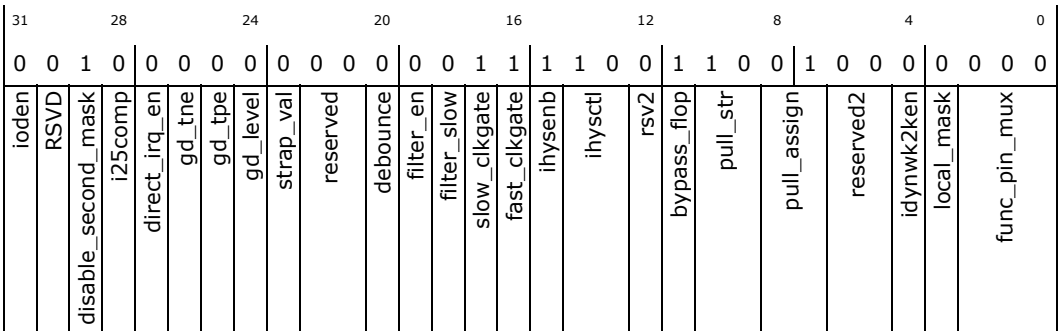
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c1_scl_PCONF0: [IOBASE] + 1E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_81 function 1 is I2C1_SCL function 2 is CCU_PLL_LOCKEN

3.67.92 I2c1 Scl Delay Line Multiplexer (cfio_regs_pad_i2c1_scl_PCONF1)—Offset 1E4h

DLL Multiplexer

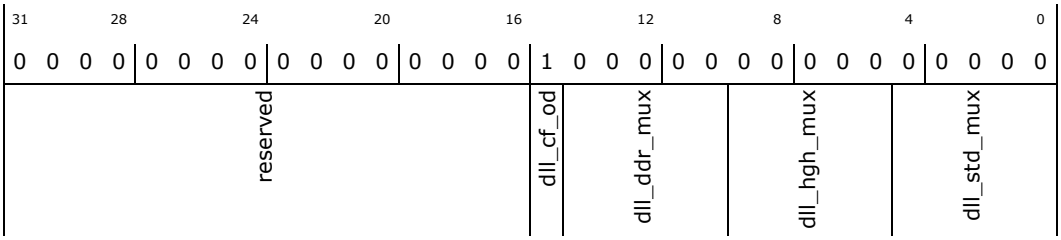
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c1_scl_PCONF1: [IOBASE] + 1E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.93 I2c1 Scl Pad Value (cfio_regs_pad_i2c1_scl_PAD_VAL)—Offset 1E8h

PADs Memory space Value register (access via PCU proxy)

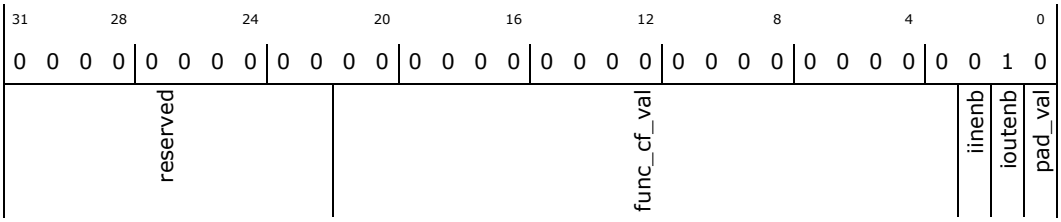
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c1_scl_PAD_VAL: [IOBASE] + 1E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.94 I2c1 Sda Pad Configuration (cfio_regs_pad_i2c1_sda_PCONF0)—Offset 1F0h

PADs Memory space configuration register (access via PCU proxy)

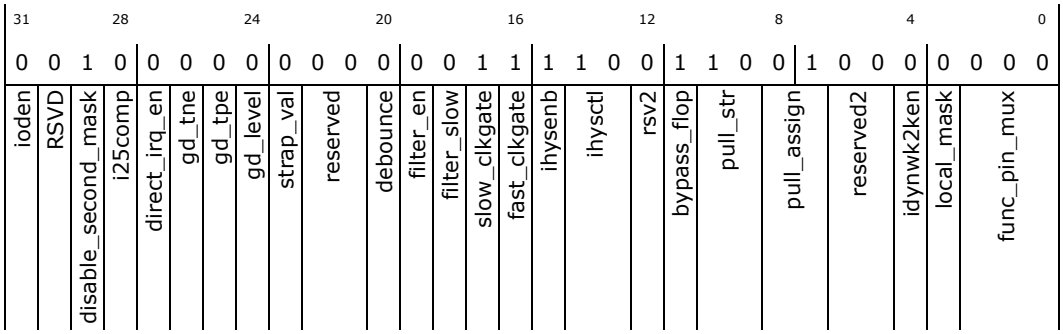
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c1_sda_PCONF0: [IOBASE] + 1F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_80 function 1 is I2C1_SDA function 2 is Unused

3.67.95 I2c1 Sda Delay Line Multiplexer (cfio_regs_pad_i2c1_sda_PCONF1)—Offset 1F4h

DLL Multiplexer

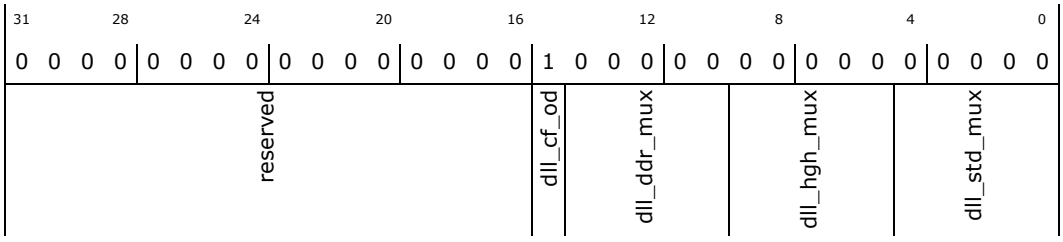
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c1_sda_PCONF1: [IOBASE] + 1F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.96 I2c1 Sda Pad Value (cfio_regs_pad_i2c1_sda_PAD_VAL)—Offset 1F8h

PADs Memory space Value register (access via PCU proxy)

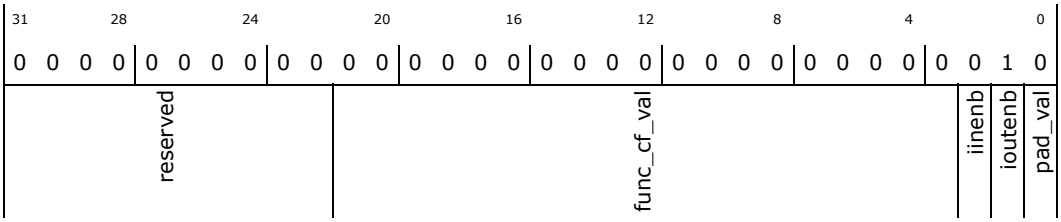
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c1_sda_PAD_VAL: [IOBASE] + 1F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.97 I2c0 Scl Pad Configuration (cfio_regs_pad_i2c0_scl_PCONF0)—Offset 200h

PADs Memory space configuration register (access via PCU proxy)

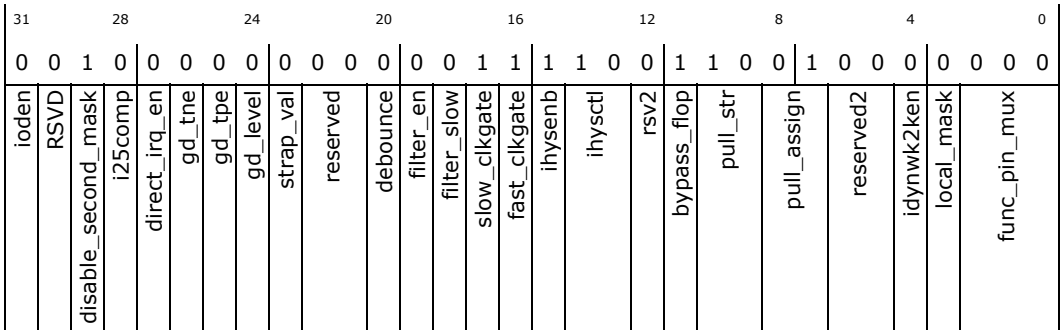
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c0_scl_PCONF0: [IOBASE] + 200h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_79 function 1 is I2C0_SCL function 2 is Unused

3.67.98 I2c0 Scl Delay Line Multiplexer (cfio_regs_pad_i2c0_scl_PCONF1)—Offset 204h

DLL Multiplexer

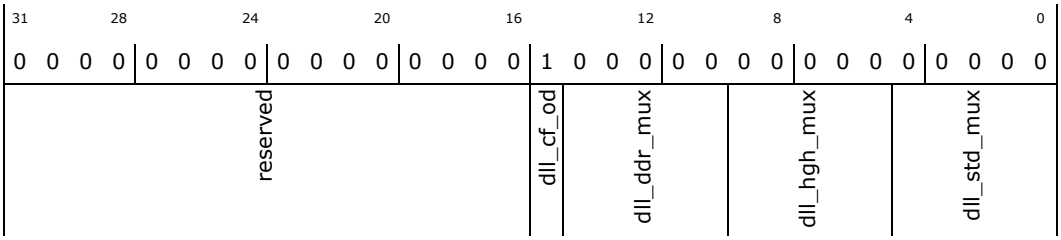
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c0_scl_PCONF1: [IOBASE] + 204h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.99 I2c0 Scl Pad Value (cfio_regs_pad_i2c0_scl_PAD_VAL)—Offset 208h

PADs Memory space Value register (access via PCU proxy)

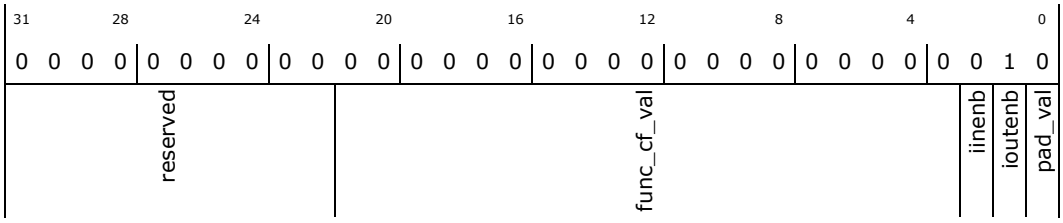
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c0_scl_PAD_VAL: [IOBASE] + 208h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.100 I2c0 Sda Pad Configuration (cfio_regs_pad_i2c0_sda_PCONF0)—Offset 210h

PADs Memory space configuration register (access via PCU proxy)

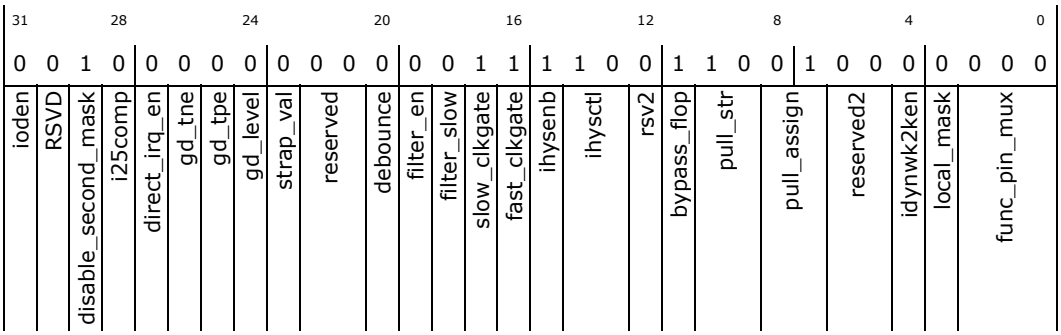
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c0_sda_PCONF0: [IOBASE] + 210h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_78 function 1 is I2C0_SDA function 2 is Unused

3.67.101 I2c0 Sda Delay Line Multiplexer (cfio_regs_pad_i2c0_sda_PCONF1)—Offset 214h

DLL Multiplexer

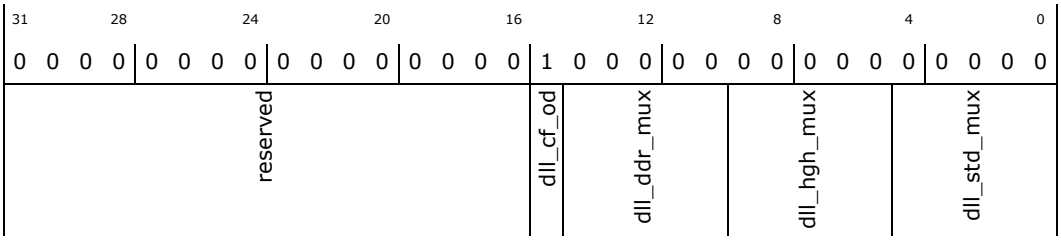
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c0_sda_PCONF1: [IOBASE] + 214h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.102 I2c0 Sda Pad Value (cfio_regs_pad_i2c0_sda_PAD_VAL)—Offset 218h

PADs Memory space Value register (access via PCU proxy)

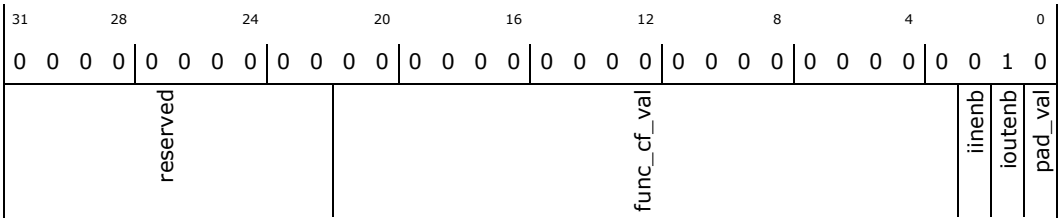
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_i2c0_sda_PAD_VAL: [IOBASE] + 218h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.103 Hda Rstb Pad Configuration (cfio_regs_pad_hda_rstb_PCONF0)—Offset 220h

PADs Memory space configuration register (access via PCU proxy)

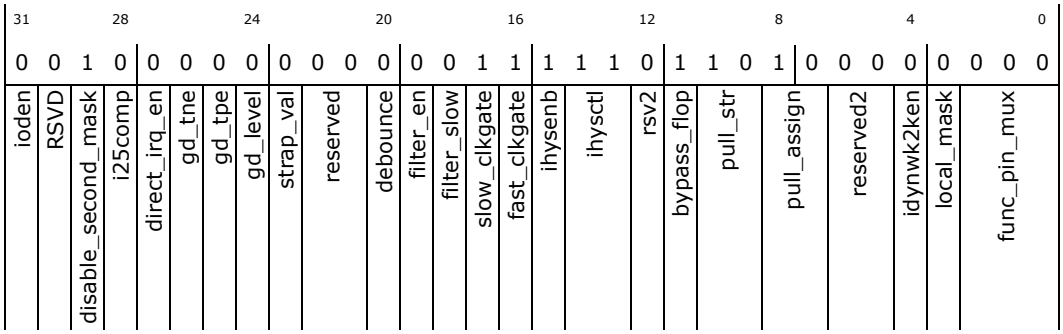
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_rstb_PCONF0: [IOBASE] + 220h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_8 function 1 is GP_SSP_0_I2S_CLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_RSTB

3.67.104 Hda Rstb Delay Line Multiplexer (cfio_regs_pad_hda_rstb_PCONF1)—Offset 224h

DLL Multiplexer

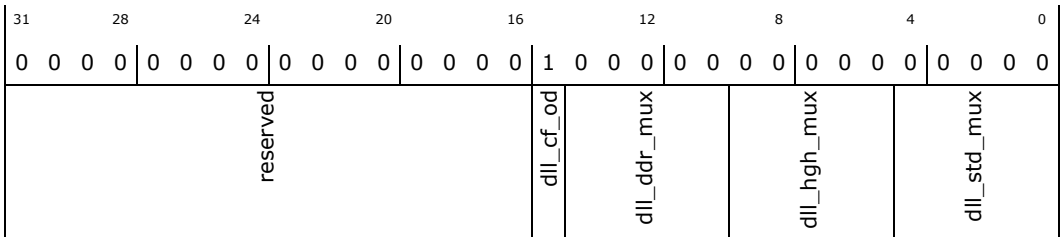
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_rstb_PCONF1: [IOBASE] + 224h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.105 Hda Rstb Pad Value (cfio_regs_pad_hda_rstb_PAD_VAL)—Offset 228h

PADs Memory space Value register (access via PCU proxy)

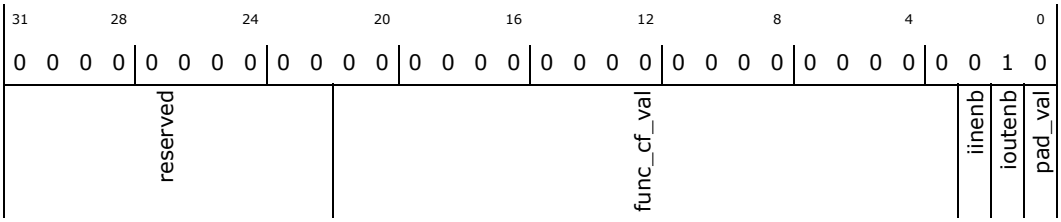
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_rstb_PAD_VAL: [IOBASE] + 228h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.106 Hda Sdi1 Pad Configuration (cfio_regs_pad_hda_sdi1_PCONF0)—Offset 230h

PADs Memory space configuration register (access via PCU proxy)

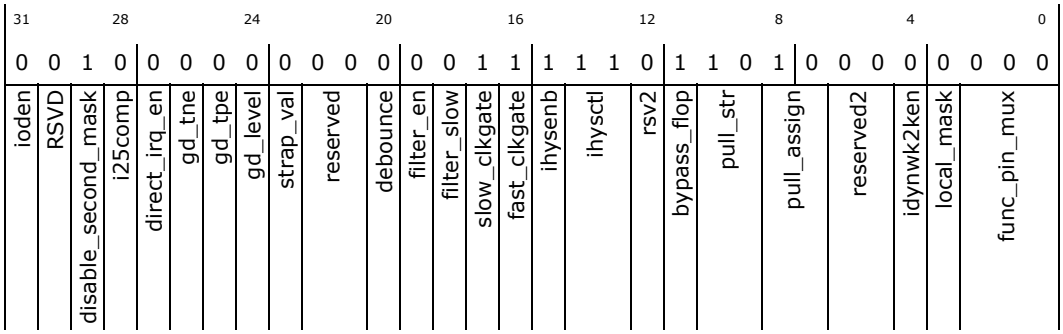
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sdi1_PCONF0: [IOBASE] + 230h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_13 function 1 is GP_SSP_1_I2S_FS For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_SDI1

3.67.107 Hda Sdi1 Delay Line Multiplexer (cfio_regs_pad_hda_sdi1_PCONF1)—Offset 234h

DLL Multiplexer

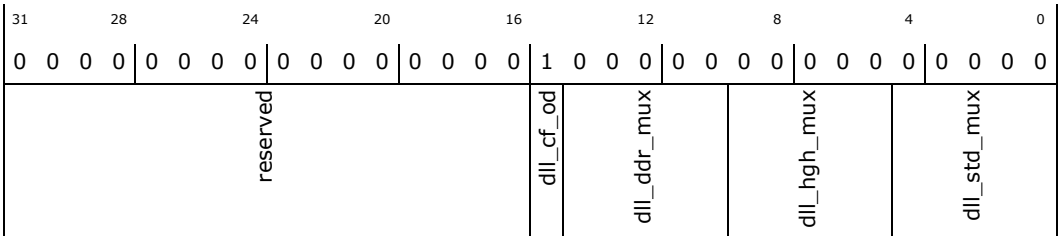
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sdi1_PCONF1: [IOBASE] + 234h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.108 Hda Sdi1 Pad Value (cfio_regs_pad_hda_sdi1_PAD_VAL)—Offset 238h

PADs Memory space Value register (access via PCU proxy)

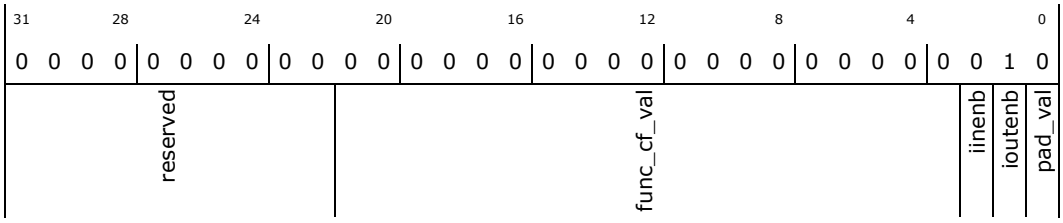
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sdi1_PAD_VAL: [IOBASE] + 238h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.109 Hda Clk Pad Configuration (cfio_regs_pad_hda_clk_PCONF0)—Offset 240h

PADs Memory space configuration register (access via PCU proxy)

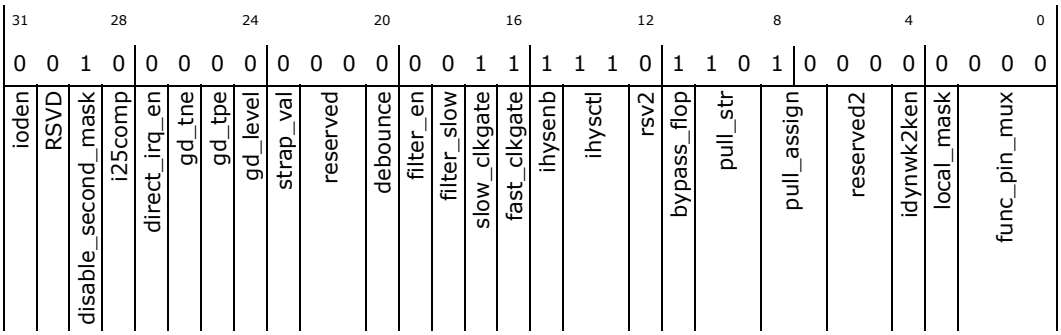
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_clk_PCONF0: [IOBASE] + 240h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_10 function 1 is GP_SSP_0_I2S_TXD For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_CLK

3.67.110 Hda Clk Delay Line Multiplexer (cfio_regs_pad_hda_clk_PCONF1)—Offset 244h

DLL Multiplexer

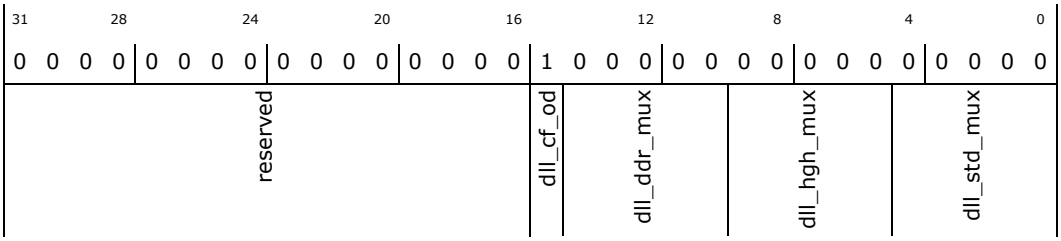
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_clk_PCONF1: [IOBASE] + 244h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.111 Hda Clk Pad Value (cfio_regs_pad_hda_clk_PAD_VAL)—Offset 248h

PADs Memory space Value register (access via PCU proxy)

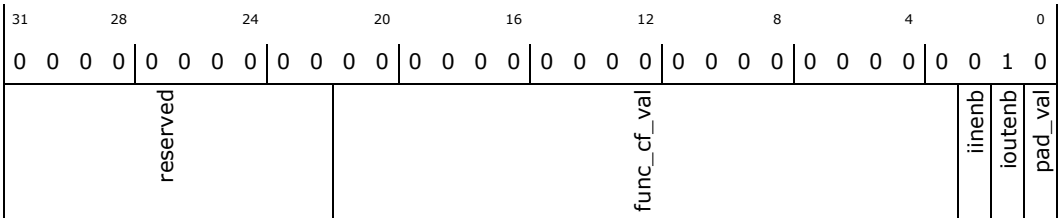
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_clk_PAD_VAL: [IOBASE] + 248h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.112 Hda Sync Pad Configuration (cfio_regs_pad_hda_sync_PCONF0)—Offset 250h

PADs Memory space configuration register (access via PCU proxy)

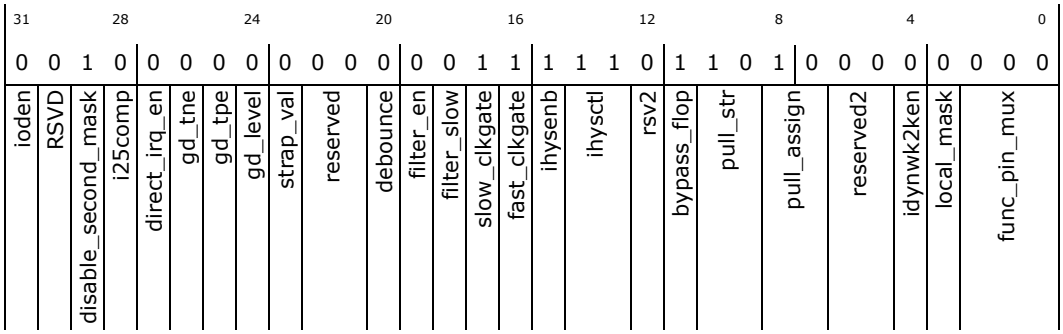
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sync_PCONF0: [IOBASE] + 250h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_9 function 1 is GP_SSP_0_I2S_FS For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_SYNC For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01

3.67.113 Hda Sync Delay Line Multiplexer (cfio_regs_pad_hda_sync_PCONF1)—Offset 254h

DLL Multiplexer

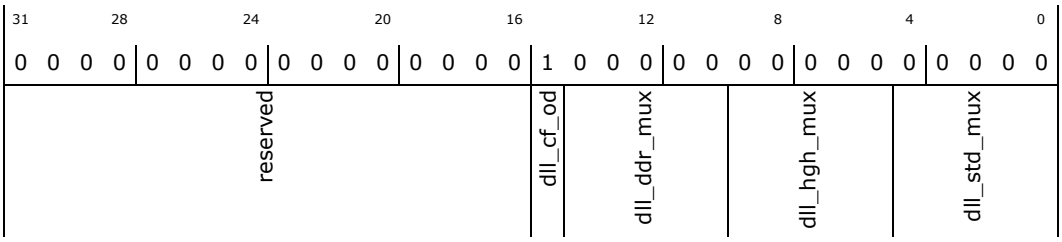
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sync_PCONF1: [IOBASE] + 254h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux

Bit Range	Default & Access	Description
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.114 Hda Sync Pad Value (cfio_regs_pad_hda_sync_PAD_VAL)—Offset 258h

PADs Memory space Value register (access via PCU proxy)

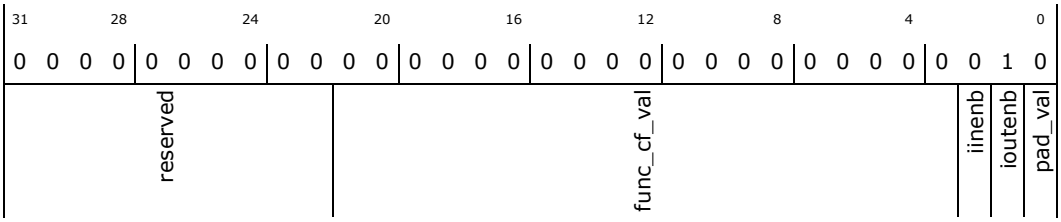
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sync_PAD_VAL: [IOBASE] + 258h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.115 Hda Sdo Pad Configuration (cfio_regs_pad_hda_sdo_PCONF0)—Offset 260h

PADs Memory space configuration register (access via PCU proxy)

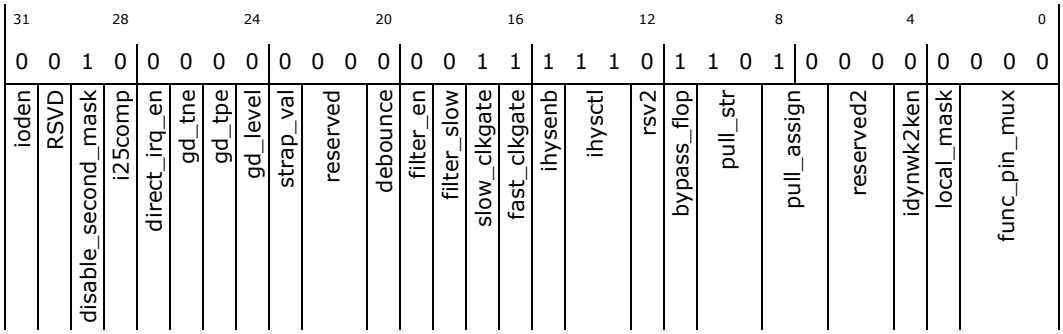
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sdo_PCONF0: [IOBASE] + 260h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register

Bit Range	Default & Access	Description
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_11 function 1 is GP_SSP_0_I2S_RXD function 2 is HDA_SDO For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01

3.67.116 Hda Sdo Delay Line Multiplexer (cfio_regs_pad_hda_sdo_PCONF1)—Offset 264h

DLL Multiplexer

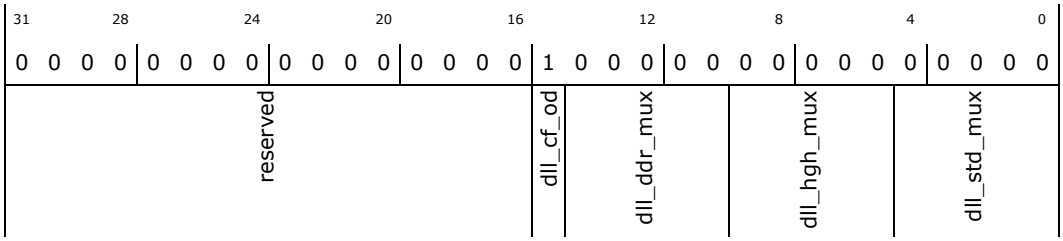
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sdo_PCONF1: [IOBASE] + 264h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.117 Hda Sdo Pad Value (cfio_regs_pad_hda_sdo_PAD_VAL)—Offset 268h

PADs Memory space Value register (access via PCU proxy)

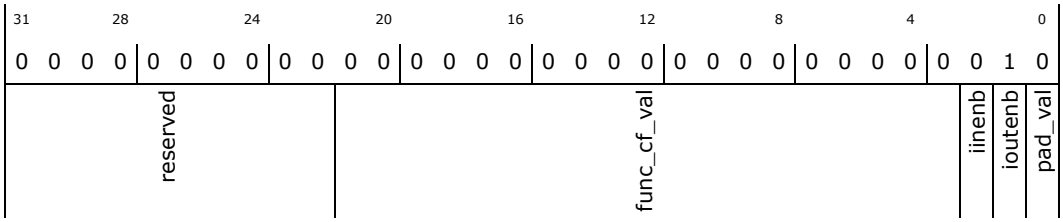
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sdo_PAD_VAL: [IOBASE] + 268h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low

Bit Range	Default & Access	Description
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.118 Hda Sdi0 Pad Configuration (cfio_regs_pad_hda_sdi0_PCONF0)—Offset 270h

PADs Memory space configuration register (access via PCU proxy)

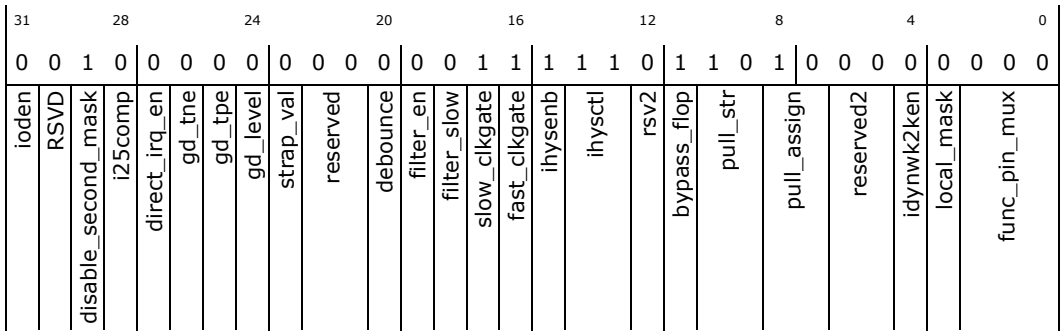
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sdi0_PCONF0: [IOBASE] + 270h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_12 function 1 is GP_SSP_1_I2S_CLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_SDI0

3.67.119 Hda Sdi0 Delay Line Multiplexer (cfio_regs_pad_hda_sdi0_PCONF1)—Offset 274h

DLL Multiplexer

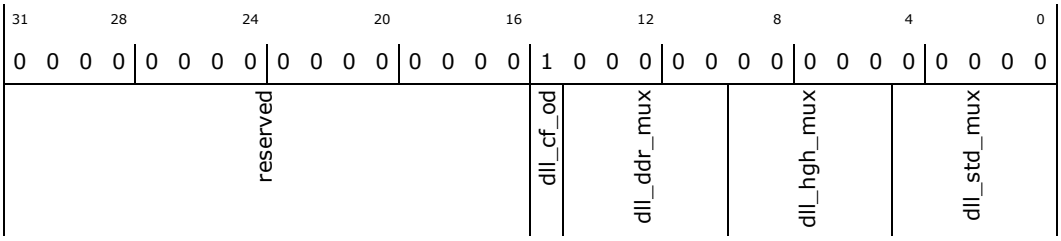
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sdi0_PCONF1: [IOBASE] + 274h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.120 Hda Sdi0 Pad Value (cfio_regs_pad_hda_sdi0_PAD_VAL)—Offset 278h

PADs Memory space Value register (access via PCU proxy)

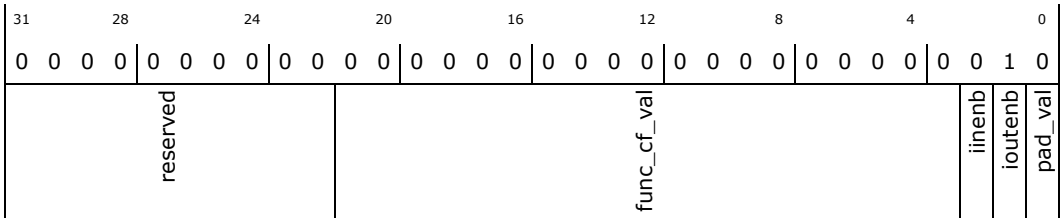
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_sdi0_PAD_VAL: [IOBASE] + 278h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.121 Hda Dockrstb Pad Configuration (cfio_regs_pad_hda_dockrstb_PCONF0)—Offset 280h

PADs Memory space configuration register (access via PCU proxy)

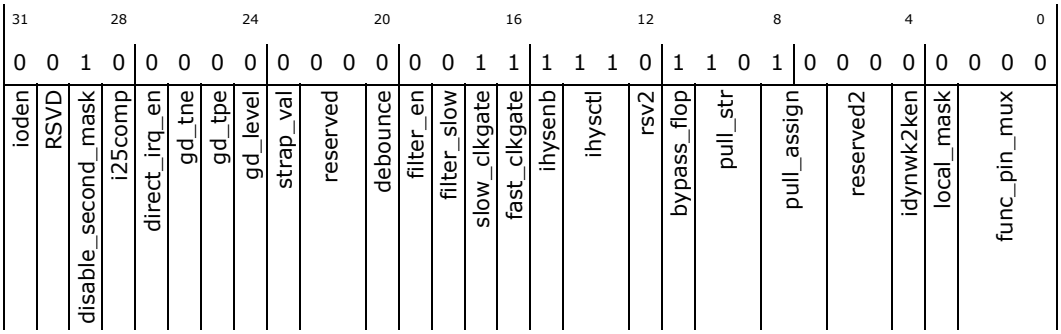
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_dockrstb_PCONF0: [IOBASE] + 280h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_14 function 1 is GP_SSP_1_I2S_TXD For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_DOCKRSTB

3.67.122 Hda Dockrstb Delay Line Multiplexer (cfio_regs_pad_hda_dockrstb_PCONF1)—Offset 284h

DLL Multiplexer

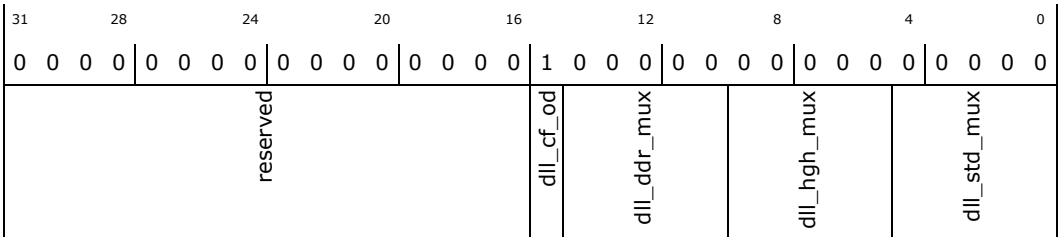
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_dockrstb_PCONF1: [IOBASE] + 284h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.123 Hda Dockrstb Pad Value (cfio_regs_pad_hda_dockrstb_PAD_VAL)—Offset 288h

PADs Memory space Value register (access via PCU proxy)

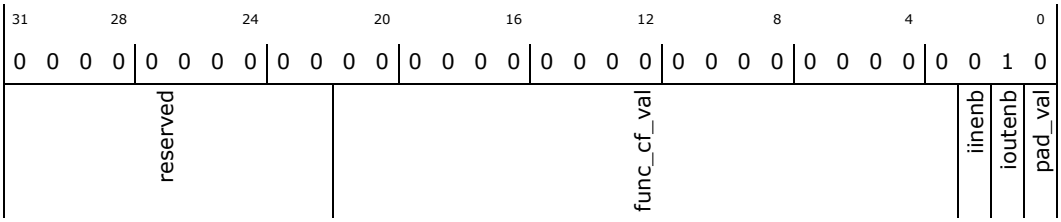
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_dockrstb_PAD_VAL: [IOBASE] + 288h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low

Bit Range	Default & Access	Description
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.124 Sdmmc3 D1 Pad Configuration (cfio_regs_pad_sdmmc3_d1_PCONF0)—Offset 290h

PADs Memory space configuration register (access via PCU proxy)

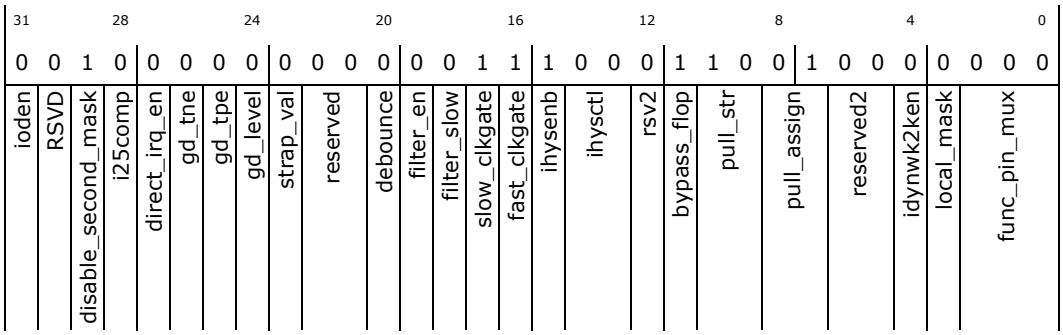
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d1_PCONF0: [IOBASE] + 290h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_35 function 1 is SDMMC3_D1

3.67.125 Sdmmc3 D1 Delay Line Multiplexer (cfio_regs_pad_sdmmc3_d1_PCONF1)—Offset 294h

DLL Multiplexer

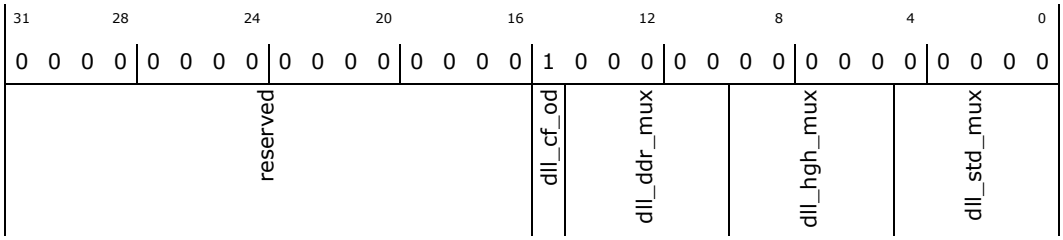
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d1_PCONF1: [IOBASE] + 294h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.126 Sdmmc3 D1 Pad Value (cfio_regs_pad_sdmmc3_d1_PAD_VAL)—Offset 298h

PADs Memory space Value register (access via PCU proxy)

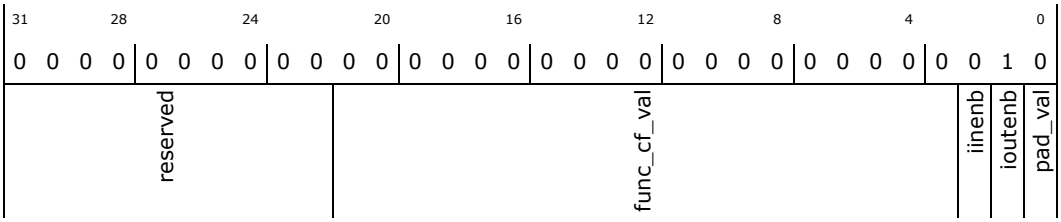
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d1_PAD_VAL: [IOBASE] + 298h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.127 Sdmmc3 D3 Pad Configuration (cfio_regs_pad_sdmmc3_d3_PCONF0)—Offset 2A0h

PADs Memory space configuration register (access via PCU proxy)

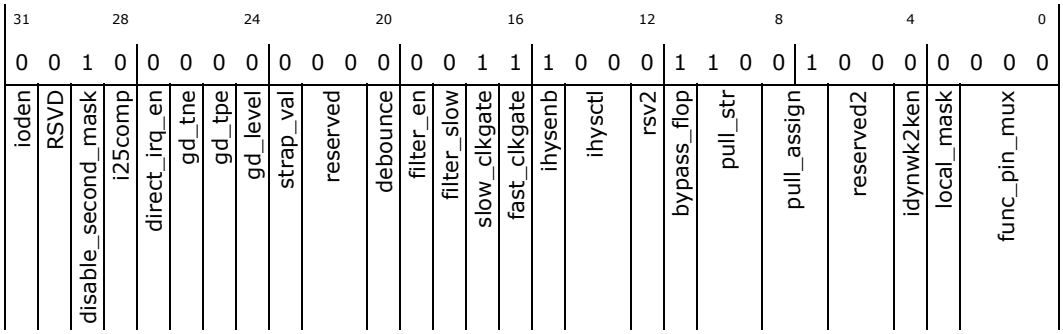
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d3_PCONF0: [IOBASE] + 2A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_37 function 1 is SDMMC3_D3

3.67.128 Sdmmc3 D3 Delay Line Multiplexer (cfio_regs_pad_sdmmc3_d3_PCONF1)—Offset 2A4h

DLL Multiplexer

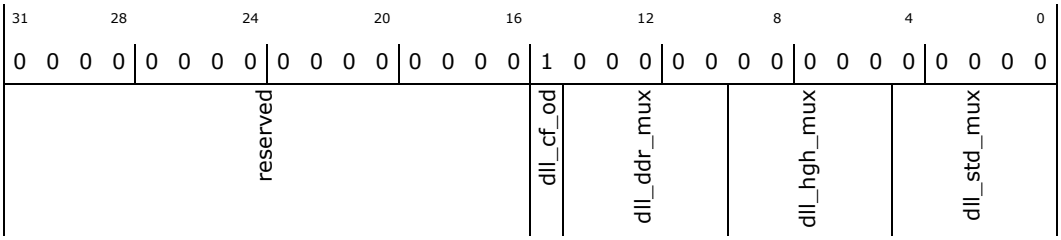
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d3_PCONF1: [IOBASE] + 2A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.129 Sdmmc3 D3 Pad Value (cfio_regs_pad_sdmmc3_d3_PAD_VAL)—Offset 2A8h

PADs Memory space Value register (access via PCU proxy)

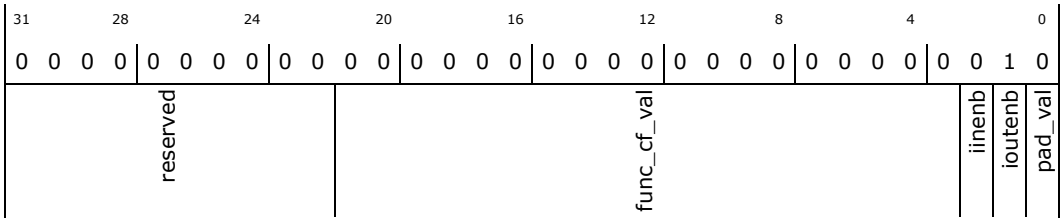
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d3_PAD_VAL: [IOBASE] + 2A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.130 Sdmmc3 Clk Pad Configuration (cfio_regs_pad_sdmmc3_clk_PCONF0)—Offset 2B0h

PADs Memory space configuration register (access via PCU proxy)

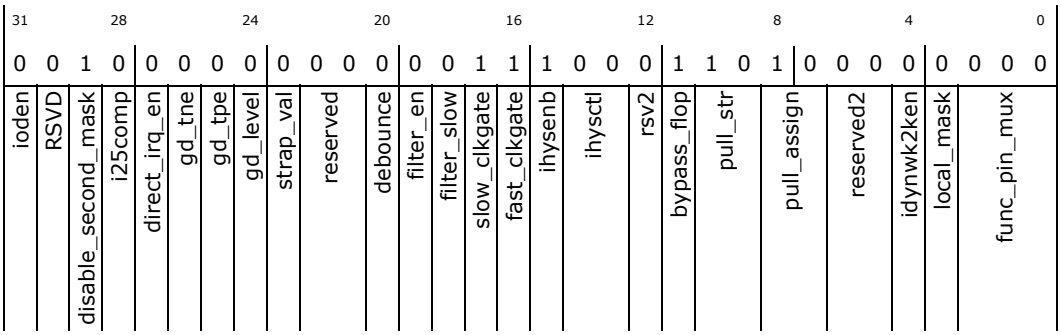
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_clk_PCONF0: [IOBASE] + 2B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038D00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_33 function 1 is SDMMC3_CLK

3.67.131 Sdmmc3 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc3_clk_PCONF1)—Offset 2B4h

DLL Multiplexer

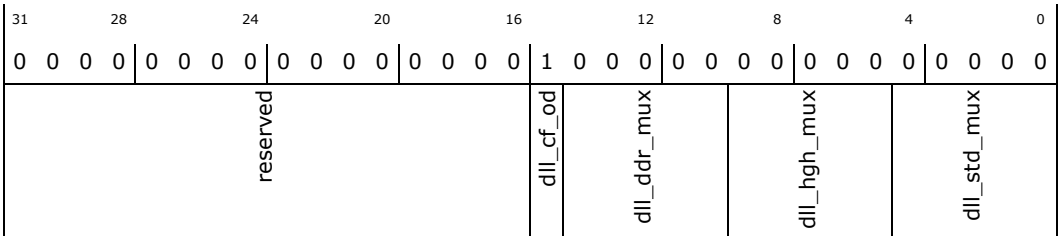
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_clk_PCONF1: [IOBASE] + 2B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RW	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RW	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RW	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RW	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.132 Sdmmc3 Clk Pad Value (cfio_regs_pad_sdmmc3_clk_PAD_VAL)—Offset 2B8h

PADs Memory space Value register (access via PCU proxy)

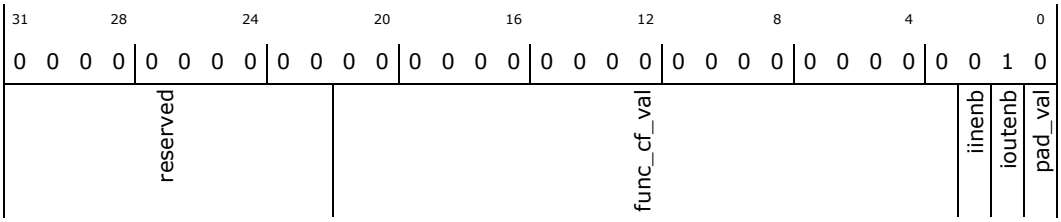
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_clk_PAD_VAL: [IOBASE] + 2B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.133 Sdmmc3 Cmd Pad Configuration (cfio_regs_pad_sdmmc3_cmd_PCONF0)—Offset 2C0h

PADs Memory space configuration register (access via PCU proxy)

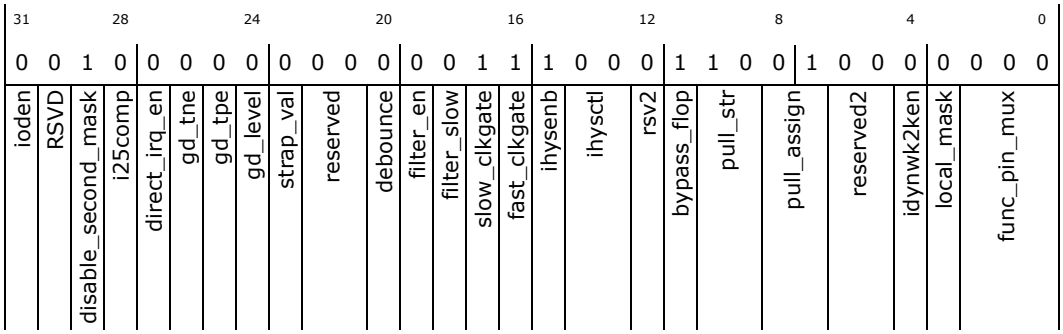
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_cmd_PCONF0: [IOBASE] + 2C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_39 function 1 is SDMMC3_CMD

3.67.134 Sdmmc3 Cmd Delay Line Multiplexer (cfio_regs_pad_sdmmc3_cmd_PCONF1)—Offset 2C4h

DLL Multiplexer

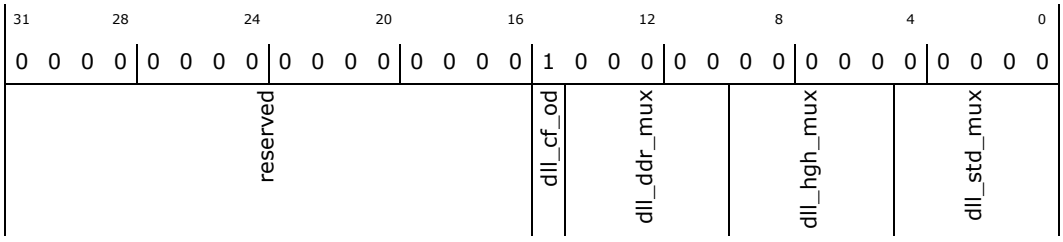
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_cmd_PCONF1: [IOBASE] + 2C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.135 Sdmmc3 Cmd Pad Value (cfio_regs_pad_sdmmc3_cmd_PAD_VAL)—Offset 2C8h

PADs Memory space Value register (access via PCU proxy)

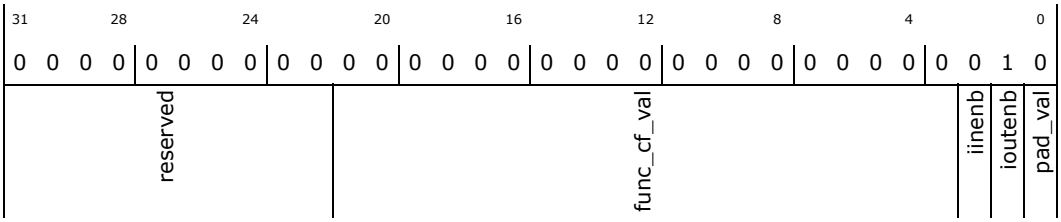
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_cmd_PAD_VAL: [IOBASE] + 2C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.136 Sdmmc3 D2 Pad Configuration (cfio_regs_pad_sdmmc3_d2_PCONF0)—Offset 2D0h

PADs Memory space configuration register (access via PCU proxy)

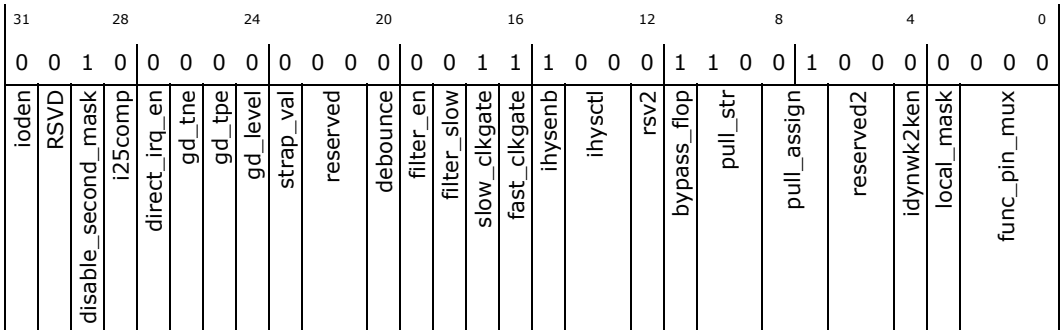
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d2_PCONF0: [IOBASE] + 2D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_36 function 1 is SDMMC3_D2

3.67.137 Sdmmc3 D2 Delay Line Multiplexer (cfio_regs_pad_sdmmc3_d2_PCONF1)—Offset 2D4h

DLL Multiplexer

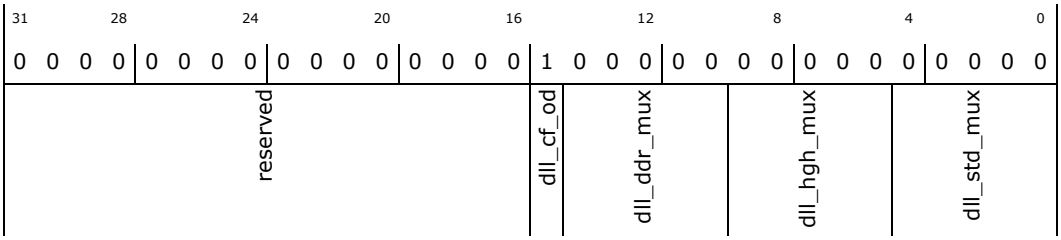
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d2_PCONF1: [IOBASE] + 2D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.138 Sdmmc3 D2 Pad Value (cfio_regs_pad_sdmmc3_d2_PAD_VAL)—Offset 2D8h

PADs Memory space Value register (access via PCU proxy)

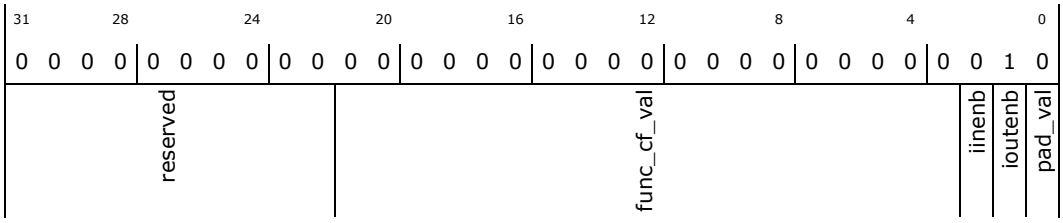
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d2_PAD_VAL: [IOBASE] + 2D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.139 Sdmmc3 D0 Pad Configuration (cfio_regs_pad_sdmmc3_d0_PCONF0)—Offset 2E0h

PADs Memory space configuration register (access via PCU proxy)

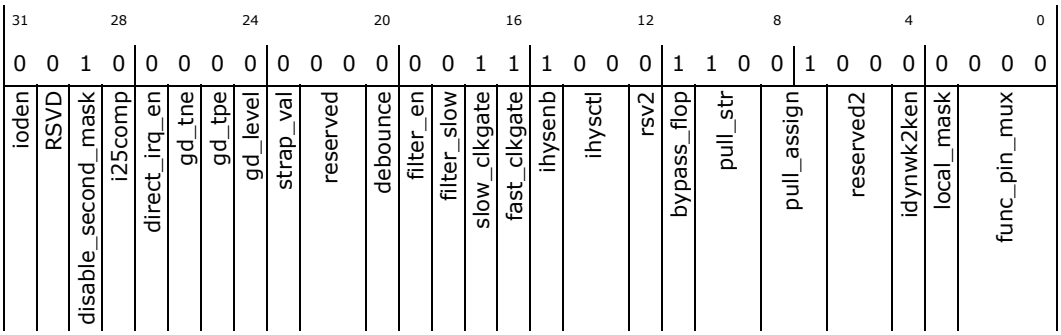
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d0_PCONF0: [IOBASE] + 2E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_34 function 1 is SDMMC3_D0

3.67.140 Sdmmc3 D0 Delay Line Multiplexer (cfio_regs_pad_sdmmc3_d0_PCONF1)—Offset 2E4h

DLL Multiplexer

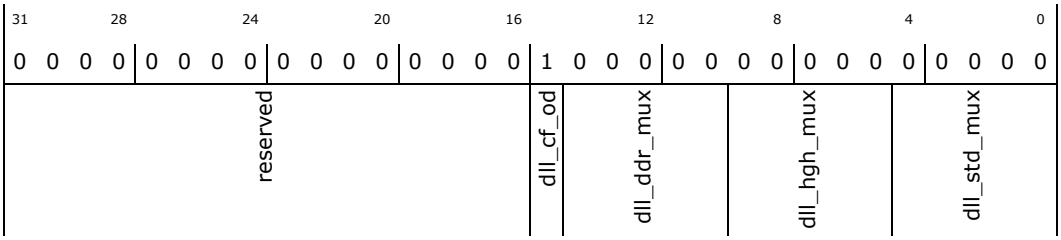
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d0_PCONF1: [IOBASE] + 2E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.141 Sdmmc3 D0 Pad Value (cfio_regs_pad_sdmmc3_d0_PAD_VAL)—Offset 2E8h

PADs Memory space Value register (access via PCU proxy)

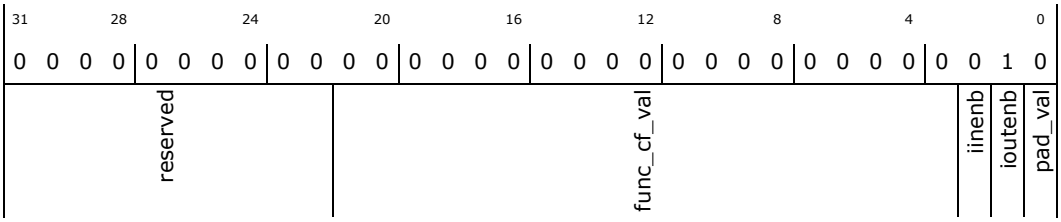
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_d0_PAD_VAL: [IOBASE] + 2E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.142 Sdmmc2 D1 Pad Configuration (cfio_regs_pad_sdmmc2_d1_PCONF0)—Offset 2F0h

PADs Memory space configuration register (access via PCU proxy)

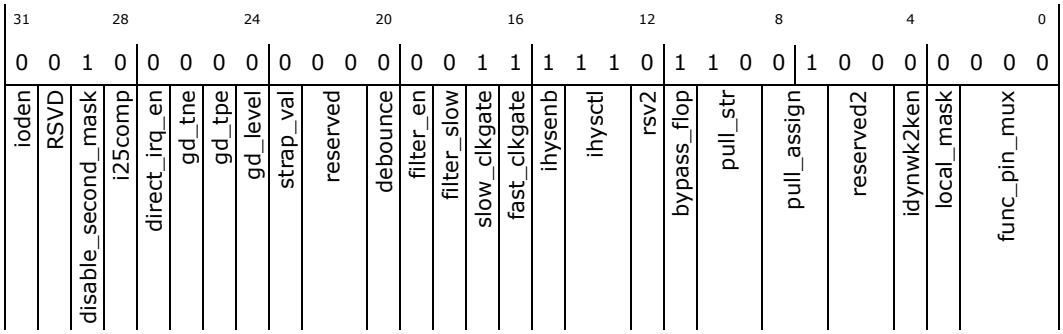
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d1_PCONF0: [IOBASE] + 2F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_29 function 1 is SDMMC2_D1

3.67.143 Sdmmc2 D1 Delay Line Multiplexer (cfio_regs_pad_sdmmc2_d1_PCONF1)—Offset 2F4h

DLL Multiplexer

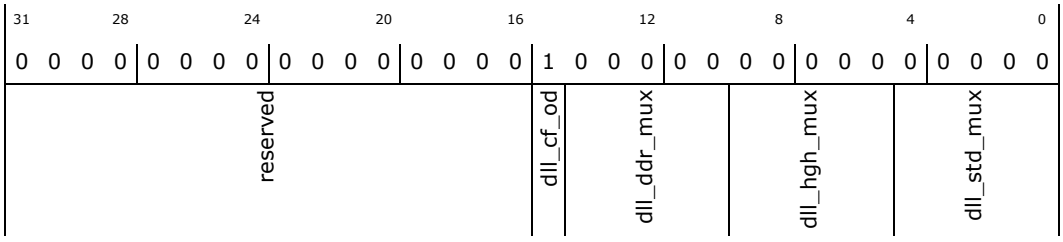
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d1_PCONF1: [IOBASE] + 2F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.144 Sdmmc2 D1 Pad Value (cfio_regs_pad_sdmmc2_d1_PAD_VAL)—Offset 2F8h

PADs Memory space Value register (access via PCU proxy)

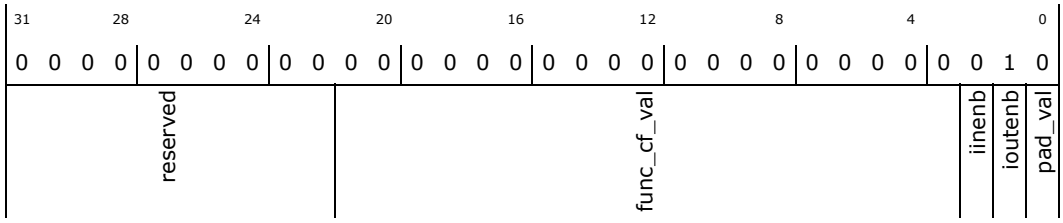
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d1_PAD_VAL: [IOBASE] + 2F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.145 Sdmmc2 Cmd Pad Configuration (cfio_regs_pad_sdmmc2_cmd_PCONF0)—Offset 300h

PADs Memory space configuration register (access via PCU proxy)

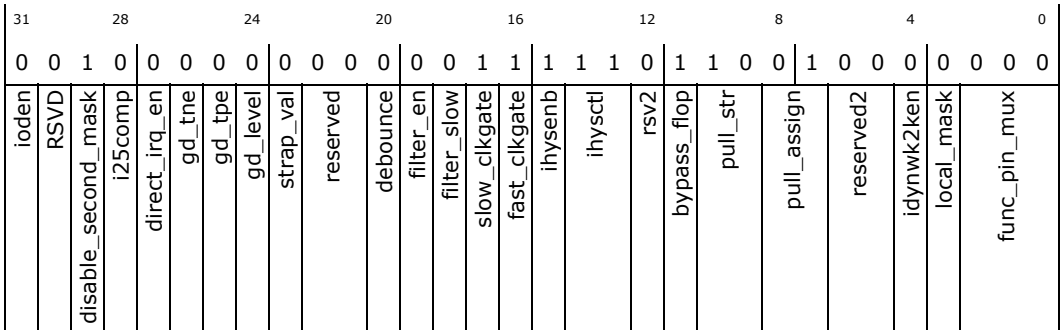
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_cmd_PCONF0: [IOBASE] + 300h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_32 function 1 is SDMMC2_CMD

3.67.146 Sdmmc2 Cmd Delay Line Multiplexer (cfio_regs_pad_sdmmc2_cmd_PCONF1)—Offset 304h

DLL Multiplexer

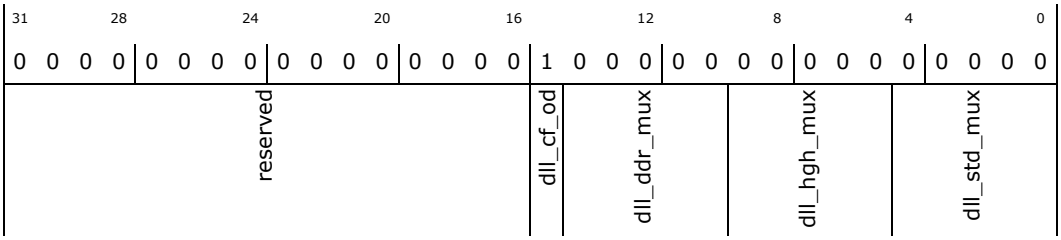
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_cmd_PCONF1: [IOBASE] + 304h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.147 Sdmmc2 Cmd Pad Value (cfio_regs_pad_sdmmc2_cmd_PAD_VAL)—Offset 308h

PADs Memory space Value register (access via PCU proxy)

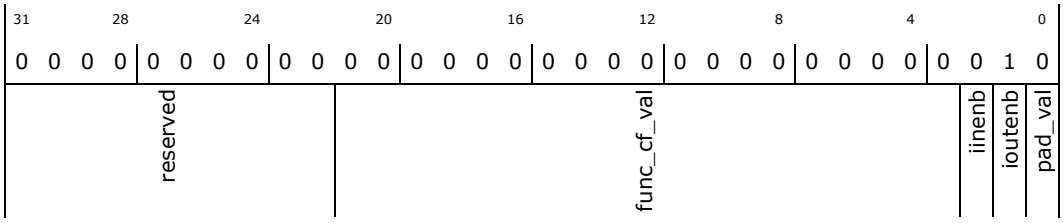
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_cmd_PAD_VAL: [IOBASE] + 308h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.148 Sdmmc2 D3 Cd B Pad Configuration (cfio_regs_pad_sdmmc2_d3_cd_b_PCONF0)—Offset 310h

PADs Memory space configuration register (access via PCU proxy)

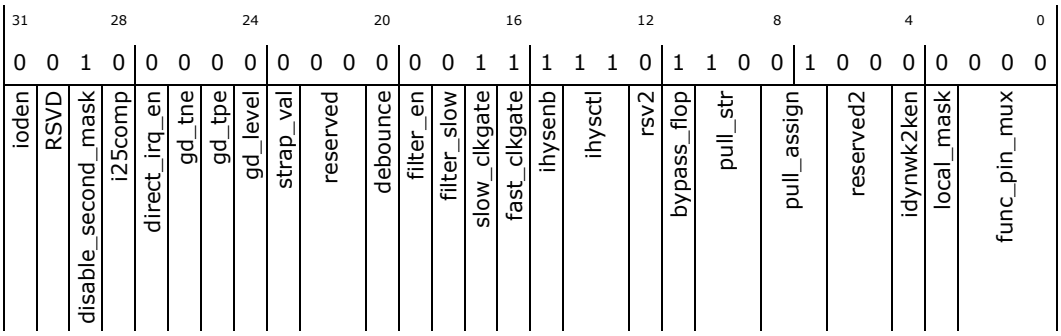
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d3_cd_b_PCONF0: [IOBASE] + 310h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_31 function 1 is SDMMC2_D3_CD_B

3.67.149 Sdmmc2 D3 Cd B Delay Line Multiplexer (cfio_regs_pad_sdmmc2_d3_cd_b_PCONF1)—Offset 314h

DLL Multiplexer

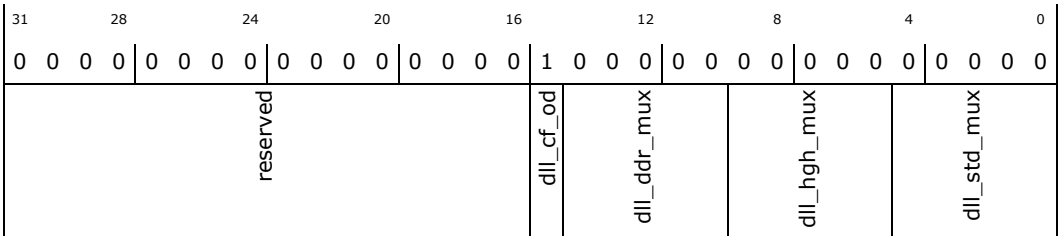
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d3_cd_b_PCONF1: [IOBASE] + 314h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.150 Sdmmc2 D3 Cd B Pad Value (cfio_regs_pad_sdmmc2_d3_cd_b_PAD_VAL)—Offset 318h

PADs Memory space Value register (access via PCU proxy)

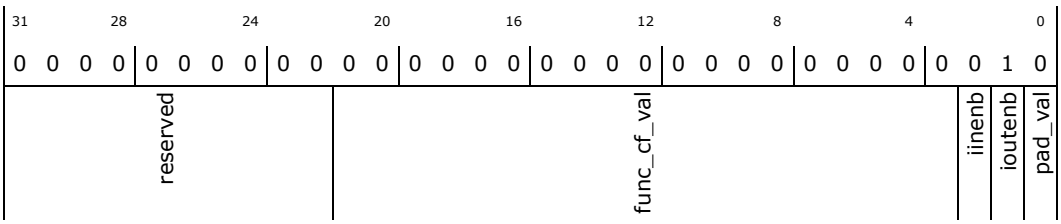
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d3_cd_b_PAD_VAL: [IOBASE] + 318h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.151 Sdmmc2 Clk Pad Configuration (cfio_regs_pad_sdmmc2_clk_PCONF0)—Offset 320h

PADs Memory space configuration register (access via PCU proxy)

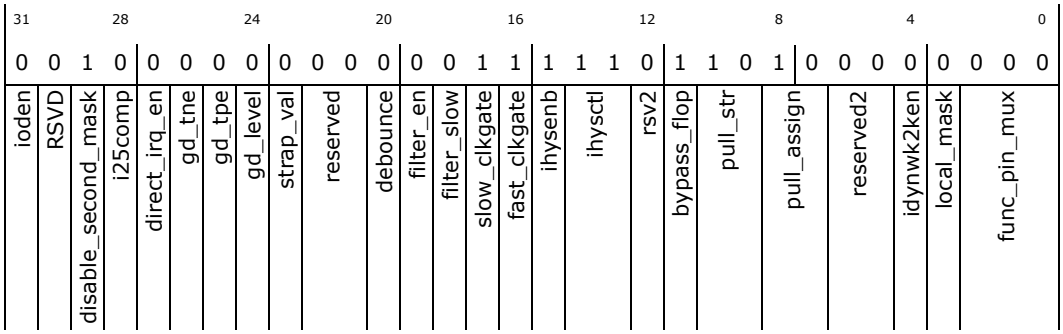
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_clk_PCONF0: [IOBASE] + 320h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_27 function 1 is SDMMC2_CLK

3.67.152 Sdmmc2 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc2_clk_PCONF1)—Offset 324h

DLL Multiplexer

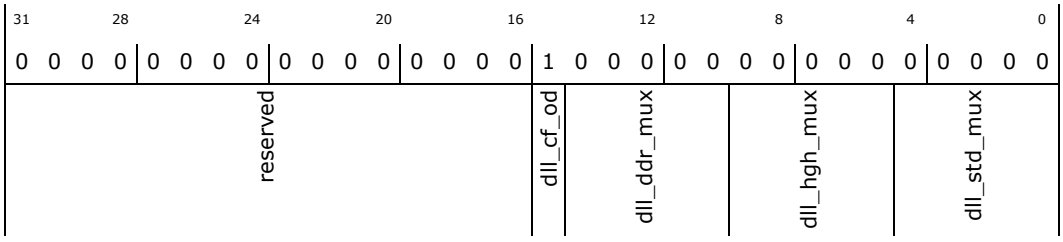
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_clk_PCONF1: [IOBASE] + 324h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RW	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RW	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RW	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RW	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.153 Sdmmc2 Clk Pad Value (cfio_regs_pad_sdmmc2_clk_PAD_VAL)—Offset 328h

PADs Memory space Value register (access via PCU proxy)

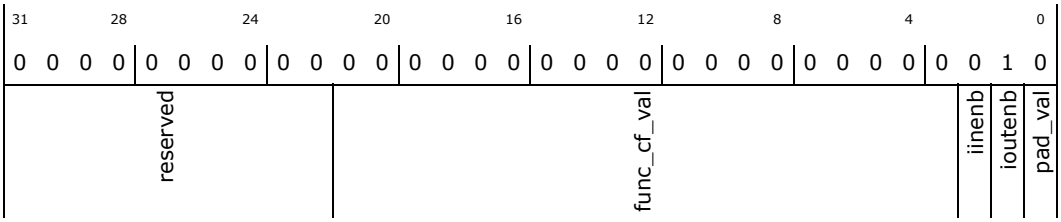
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_clk_PAD_VAL: [IOBASE] + 328h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.154 Mmc1 Reset B Pad Configuration (cfio_regs_pad_mmc1_reset_b_PCONF0)—Offset 330h

PADs Memory space configuration register (access via PCU proxy)

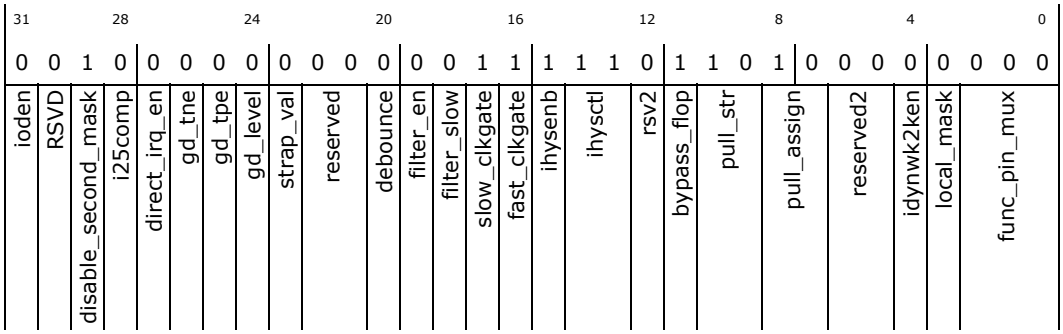
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_reset_b_PCONF0: [IOBASE] + 330h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_26 function 1 is MMC1_RESET_B function 2 is SATA_DEVSLP0 function 3 is MMC_45_RESET_B

3.67.155 Mmc1 Reset B Delay Line Multiplexer (cfio_regs_pad_mmc1_reset_b_PCONF1)—Offset 334h

DLL Multiplexer

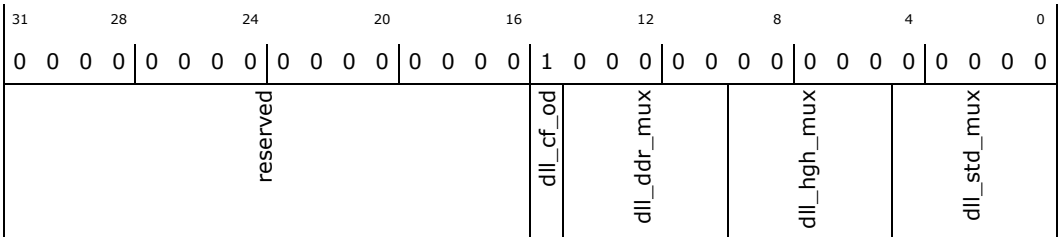
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_reset_b_PCONF1: [IOBASE] + 334h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.156 Mmc1 Reset B Pad Value (cfio_regs_pad_mmc1_reset_b_PAD_VAL)—Offset 338h

PADs Memory space Value register (access via PCU proxy)

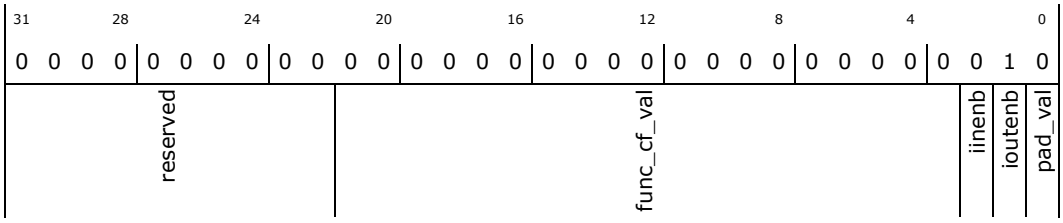
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_reset_b_PAD_VAL: [IOBASE] + 338h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.157 Sdmmc2 D2 Pad Configuration (cfio_regs_pad_sdmmc2_d2_PCONF0)—Offset 340h

PADs Memory space configuration register (access via PCU proxy)

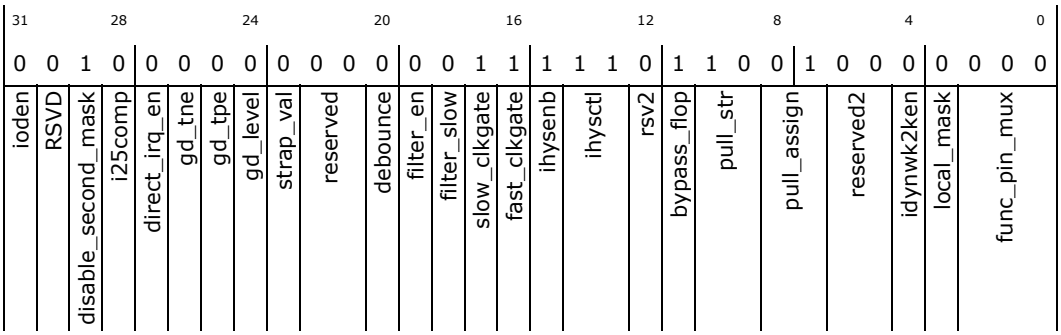
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d2_PCONF0: [IOBASE] + 340h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_30 function 1 is SDMMC2_D2

3.67.158 Sdmmc2 D2 Delay Line Multiplexer (cfio_regs_pad_sdmmc2_d2_PCONF1)—Offset 344h

DLL Multiplexer

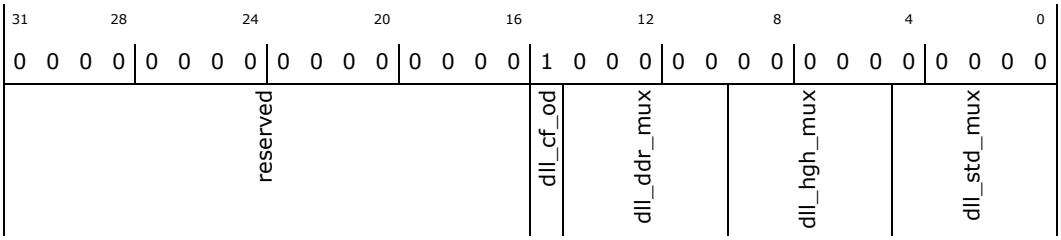
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d2_PCONF1: [IOBASE] + 344h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.159 Sdmmc2 D2 Pad Value (cfio_regs_pad_sdmmc2_d2_PAD_VAL)—Offset 348h

PADs Memory space Value register (access via PCU proxy)

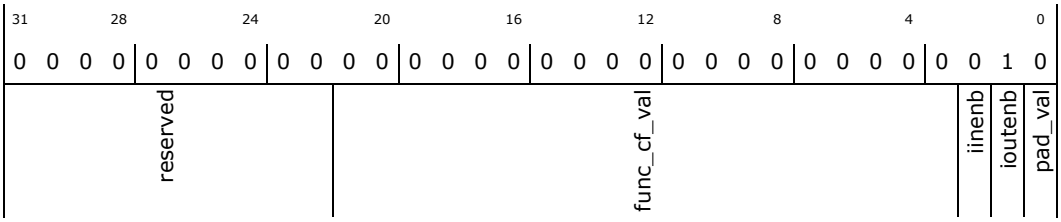
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d2_PAD_VAL: [IOBASE] + 348h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.160 Sdmmc2 D0 Pad Configuration (cfio_regs_pad_sdmmc2_d0_PCONF0)—Offset 350h

PADs Memory space configuration register (access via PCU proxy)

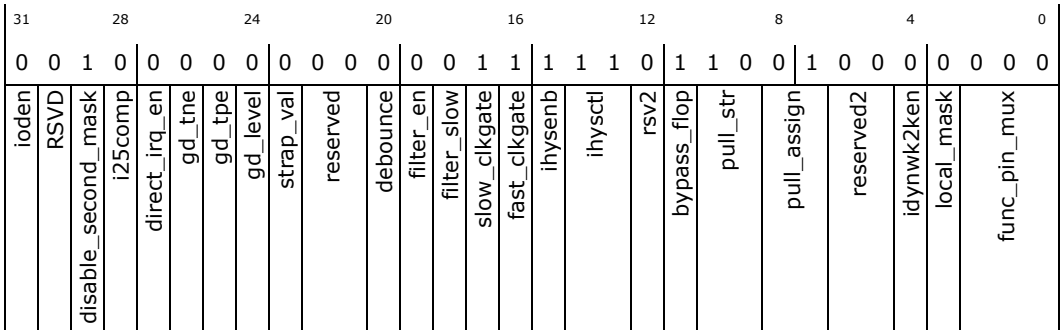
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d0_PCONF0: [IOBASE] + 350h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_28 function 1 is SDMMC2_D0

3.67.161 Sdmmc2 D0 Delay Line Multiplexer (cfio_regs_pad_sdmmc2_d0_PCONF1)—Offset 354h

DLL Multiplexer

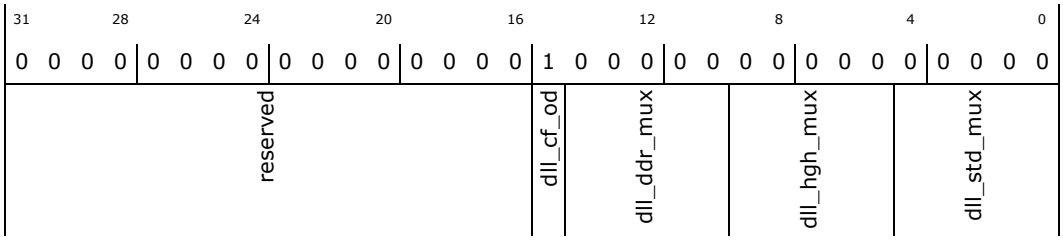
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d0_PCONF1: [IOBASE] + 354h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.162 Sdmmc2 D0 Pad Value (cfio_regs_pad_sdmmc2_d0_PAD_VAL)—Offset 358h

PADs Memory space Value register (access via PCU proxy)

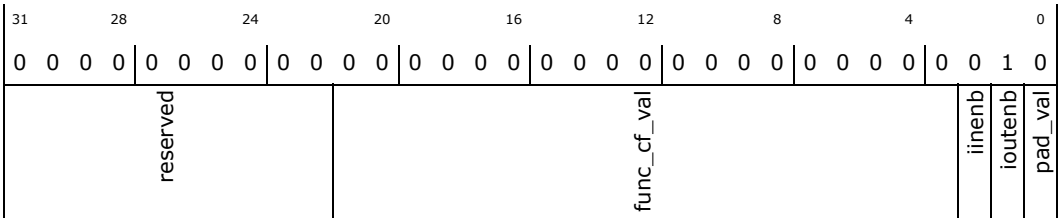
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc2_d0_PAD_VAL: [IOBASE] + 358h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.163 Sdmmc1 D3 Cd B Pad Configuration (cfio_regs_pad_sdmmc1_d3_cd_b_PCONF0)—Offset 360h

PADs Memory space configuration register (access via PCU proxy)

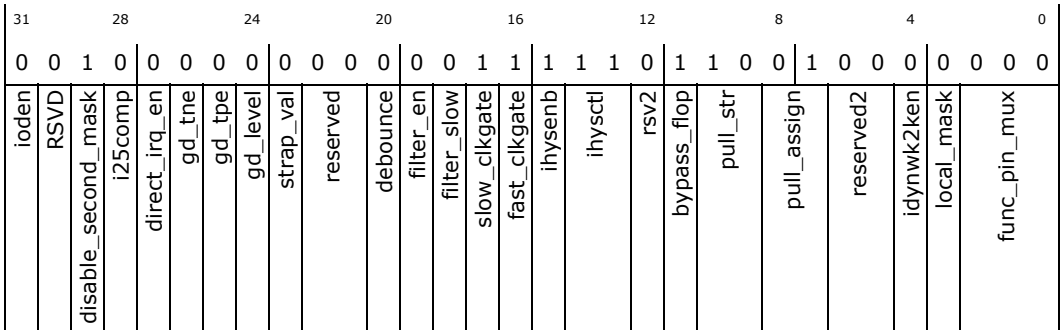
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d3_cd_b_PCONF0: [IOBASE] + 360h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_20 function 1 is SDMMC1_D3_CD_B function 2 is Unused function 3 is SDMMC_45_D3_CD_B

3.67.164 Sdmmc1 D3 Cd B Delay Line Multiplexer (cfio_regs_pad_sdmmc1_d3_cd_b_PCONF1)—Offset 364h

DLL Multiplexer

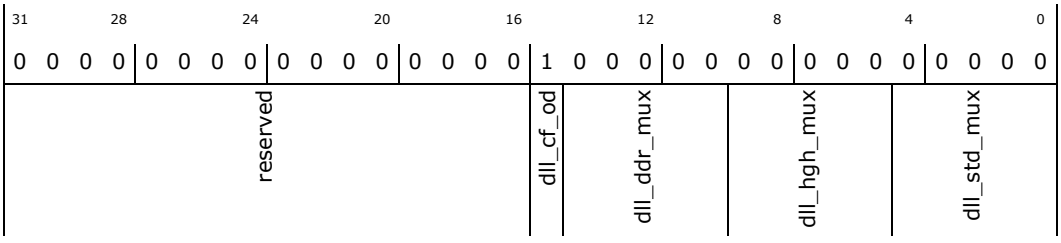
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d3_cd_b_PCONF1: [IOBASE] + 364h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.165 Sdmmc1 D3 Cd B Pad Value (cfio_regs_pad_sdmmc1_d3_cd_b_PAD_VAL)—Offset 368h

PADs Memory space Value register (access via PCU proxy)

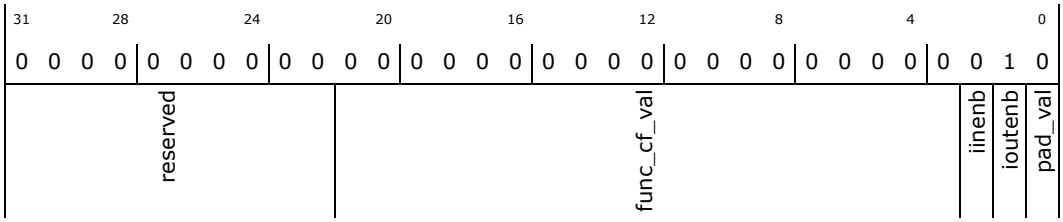
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d3_cd_b_PAD_VAL: [IOBASE] + 368h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low

Bit Range	Default & Access	Description
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.166 Mmc1 D6 Pad Configuration (cfio_regs_pad_mmc1_d6_PCONF0)—Offset 370h

PADs Memory space configuration register (access via PCU proxy)

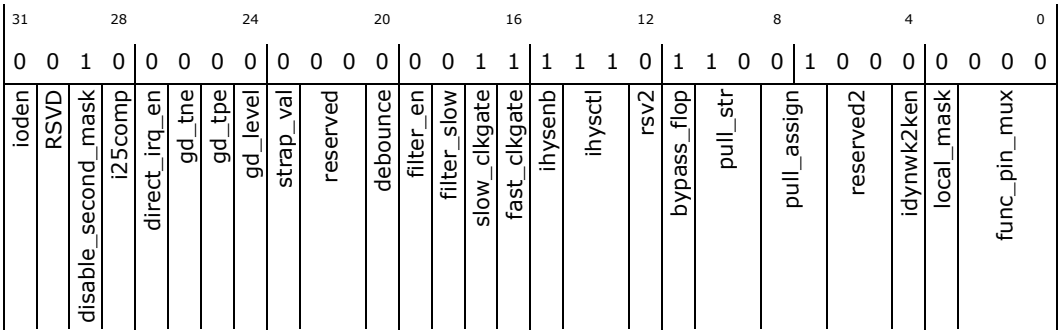
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d6_PCONF0: [IOBASE] + 370h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_23 function 1 is MMC1_D6 function 2 is Unused function 3 is MMC_45_D6

3.67.167 Mmc1 D6 Delay Line Multiplexer (cfio_regs_pad_mmc1_d6_PCONF1)—Offset 374h

DLL Multiplexer

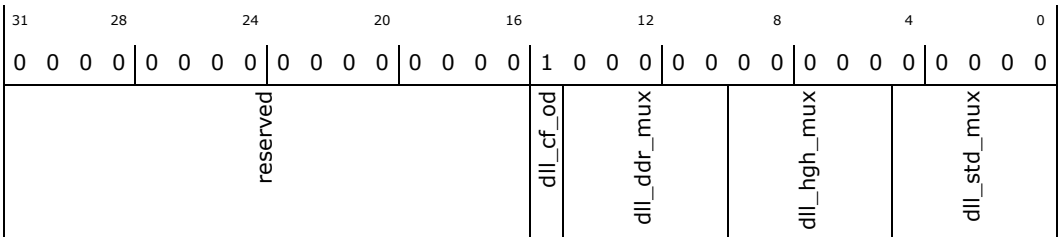
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d6_PCONF1: [IOBASE] + 374h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.168 Mmc1 D6 Pad Value (cfio_regs_pad_mmc1_d6_PAD_VAL)—Offset 378h

PADs Memory space Value register (access via PCU proxy)

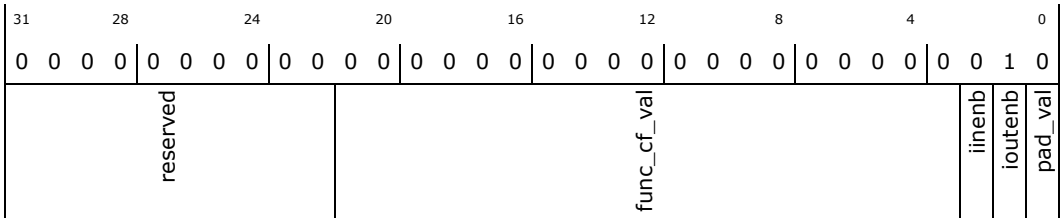
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d6_PAD_VAL: [IOBASE] + 378h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.169 Mmc1 D4 Sd We Pad Configuration (cfio_regs_pad_mmc1_d4_sd_we_PCONF0)—Offset 380h

PADs Memory space configuration register (access via PCU proxy)

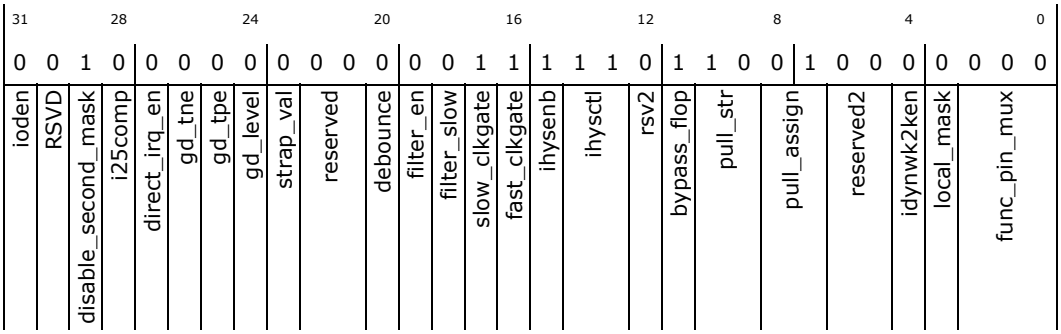
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d4_sd_we_PCONF0: [IOBASE] + 380h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_21 function 1 is MMC1_D4_SD_WE function 2 is Unused function 3 is MMC_45_D4_SD_WE

3.67.170 Mmc1 D4 Sd We Delay Line Multiplexer (cfio_regs_pad_mmc1_d4_sd_we_PCONF1)—Offset 384h

DLL Multiplexer

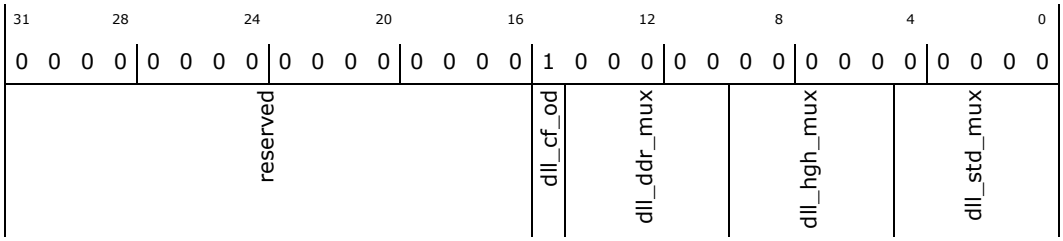
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d4_sd_we_PCONF1: [IOBASE] + 384h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.171 Mmc1 D4 Sd We Pad Value (cfio_regs_pad_mmc1_d4_sd_we_PAD_VAL)—Offset 388h

PADs Memory space Value register (access via PCU proxy)

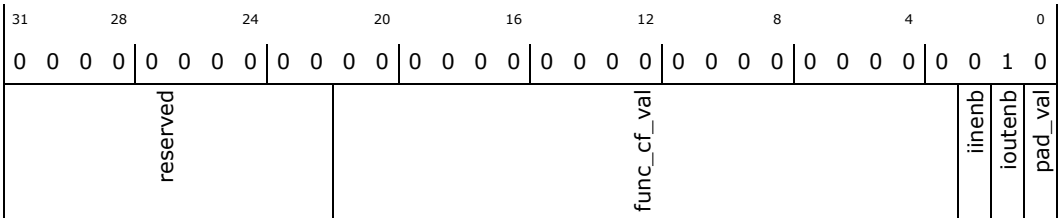
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d4_sd_we_PAD_VAL: [IOBASE] + 388h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low

Bit Range	Default & Access	Description
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.172 Sdmmc1 Cmd Pad Configuration (cfio_regs_pad_sdmmc1_cmd_PCONF0)—Offset 390h

PADs Memory space configuration register (access via PCU proxy)

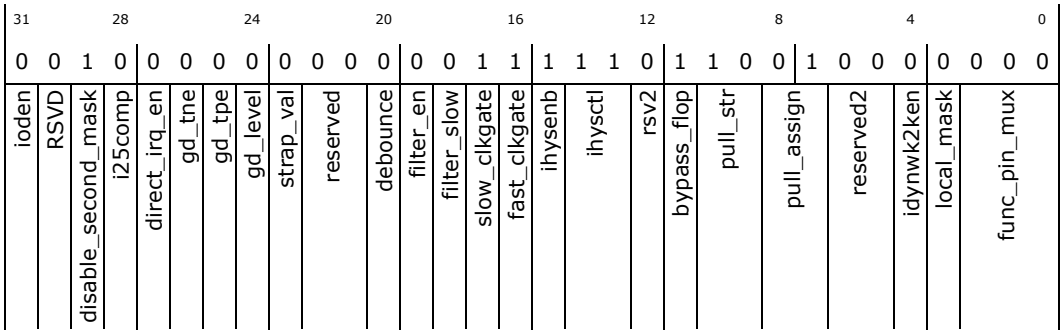
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_cmd_PCONF0: [IOBASE] + 390h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_25 function 1 is SDMMC1_CMD function 2 is Unused function 3 is SDMMC_45_CMD

3.67.173 Sdmmc1 Cmd Delay Line Multiplexer (cfio_regs_pad_sdmmc1_cmd_PCONF1)—Offset 394h

DLL Multiplexer

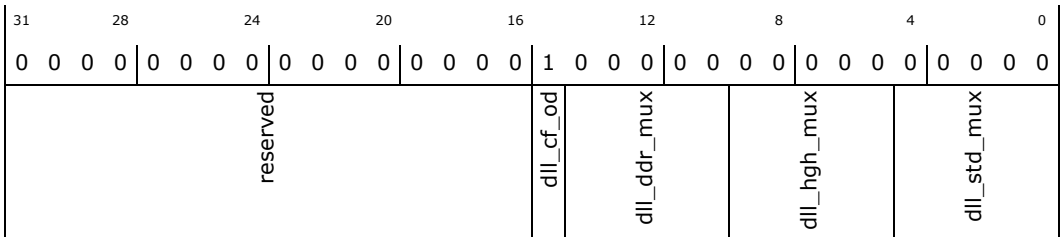
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_cmd_PCONF1: [IOBASE] + 394h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.174 Sdmmc1 Cmd Pad Value (cfio_regs_pad_sdmmc1_cmd_PAD_VAL)—Offset 398h

PADs Memory space Value register (access via PCU proxy)

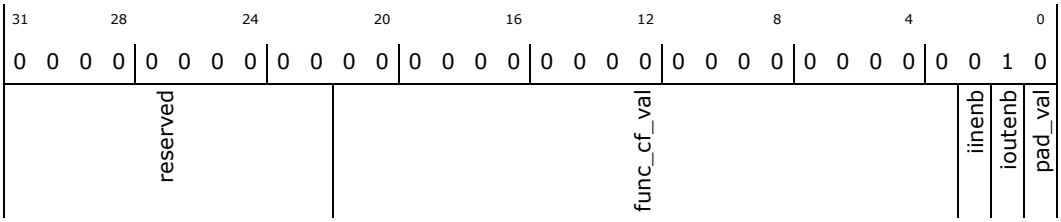
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_cmd_PAD_VAL: [IOBASE] + 398h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.175 Sdmmc3 Cd B Pad Configuration (cfio_regs_pad_sdmmc3_cd_b_PCONF0)—Offset 3A0h

PADs Memory space configuration register (access via PCU proxy)

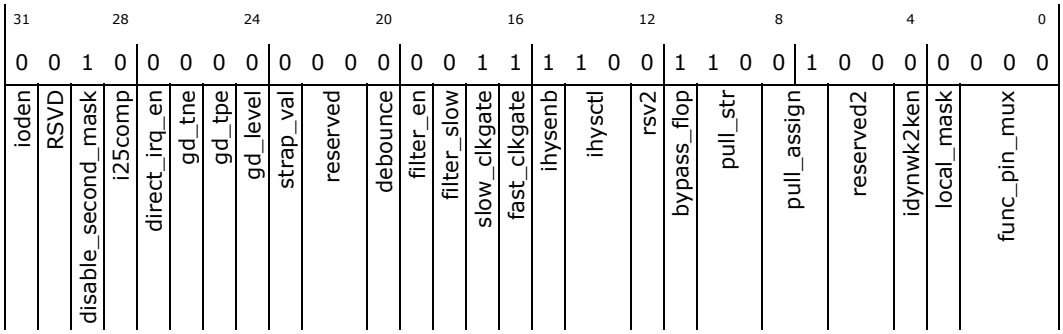
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_cd_b_PCONF0: [IOBASE] + 3A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_38 function 1 is SDMMC3_CD_B

3.67.176 Sdmmc3 Cd B Delay Line Multiplexer (cfio_regs_pad_sdmmc3_cd_b_PCONF1)—Offset 3A4h

DLL Multiplexer

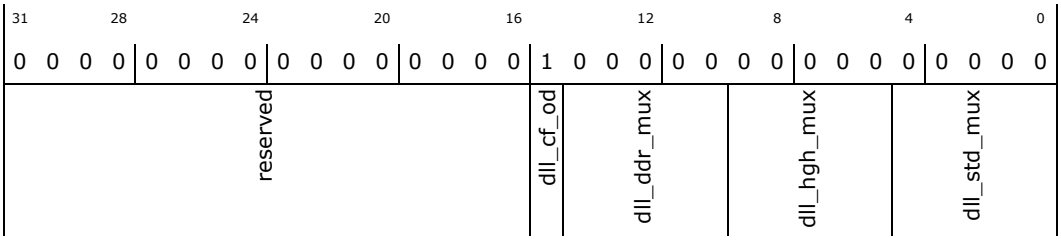
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_cd_b_PCONF1: [IOBASE] + 3A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.177 Sdmmc3 Cd B Pad Value (cfio_regs_pad_sdmmc3_cd_b_PAD_VAL)—Offset 3A8h

PADs Memory space Value register (access via PCU proxy)

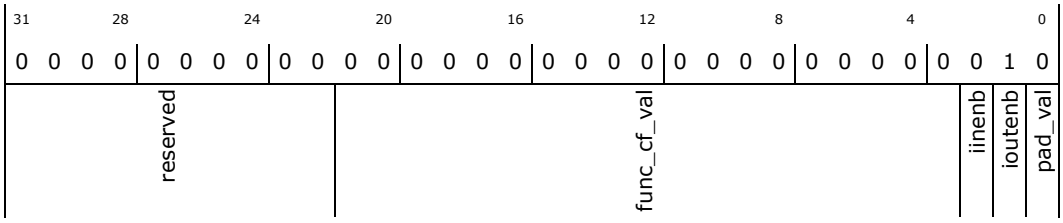
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_cd_b_PAD_VAL: [IOBASE] + 3A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.178 Sdmmc1 D2 Pad Configuration (cfio_regs_pad_sdmmc1_d2_PCONF0)—Offset 3B0h

PADs Memory space configuration register (access via PCU proxy)

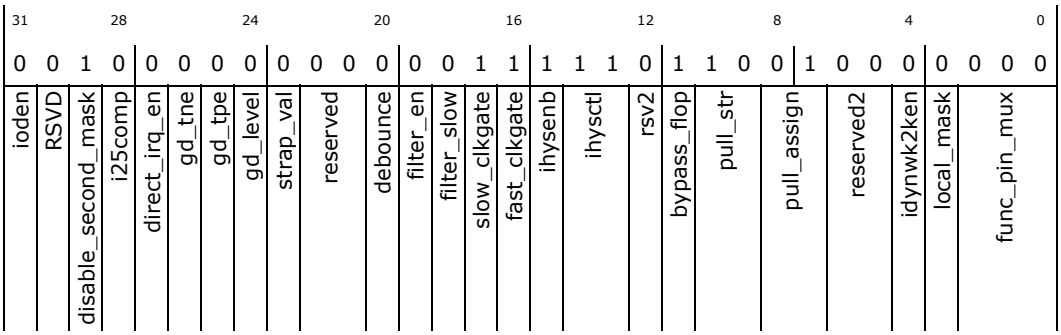
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d2_PCONF0: [IOBASE] + 3B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_19 function 1 is SDMMC1_D2 function 2 is Unused function 3 is SDMMC_45_D2

3.67.179 Sdmmc1 D2 Delay Line Multiplexer (cfio_regs_pad_sdmmc1_d2_PCONF1)—Offset 3B4h

DLL Multiplexer

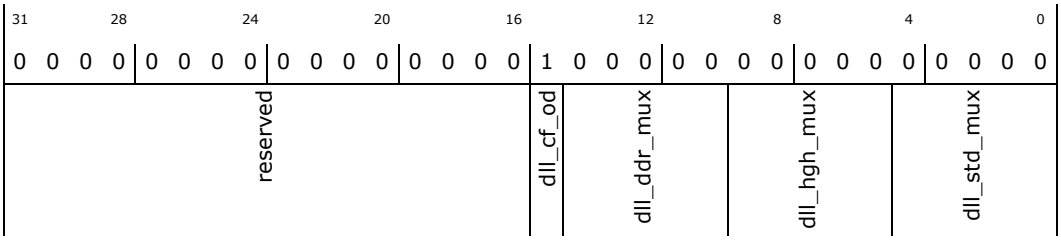
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d2_PCONF1: [IOBASE] + 3B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.180 Sdmmc1 D2 Pad Value (cfio_regs_pad_sdmmc1_d2_PAD_VAL)—Offset 3B8h

PADs Memory space Value register (access via PCU proxy)

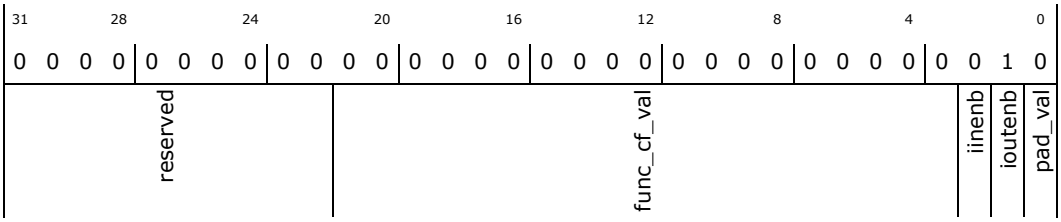
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d2_PAD_VAL: [IOBASE] + 3B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.181 Mmc1 D5 Pad Configuration (cfio_regs_pad_mmc1_d5_PCONF0)—Offset 3C0h

PADs Memory space configuration register (access via PCU proxy)

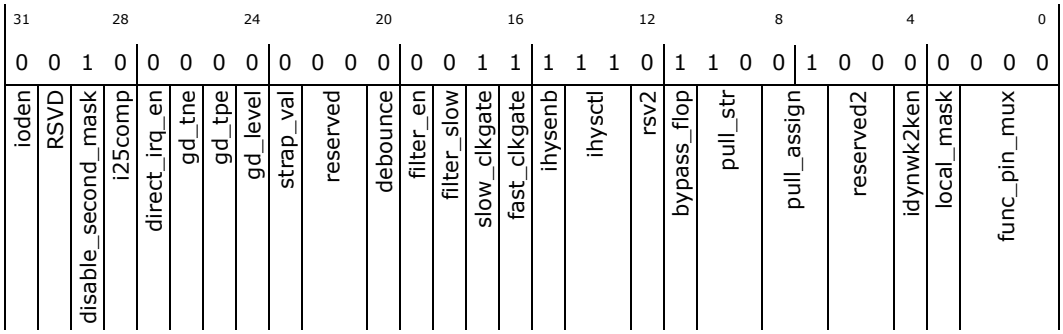
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d5_PCONF0: [IOBASE] + 3C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_22 function 1 is MMC1_D5 function 2 is Unused function 3 is MMC_45_D5

3.67.182 Mmc1 D5 Delay Line Multiplexer (cfio_regs_pad_mmc1_d5_PCONF1)—Offset 3C4h

DLL Multiplexer

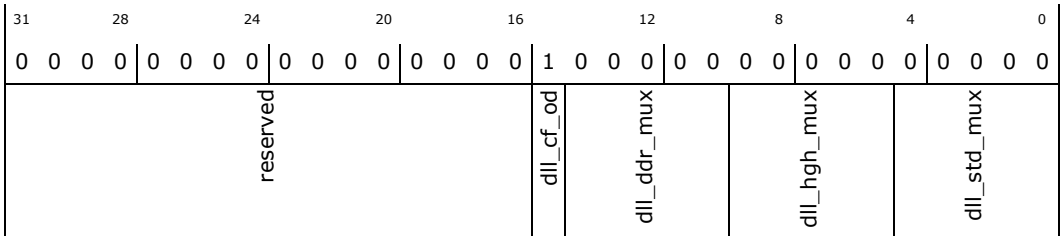
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d5_PCONF1: [IOBASE] + 3C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.183 Mmc1 D5 Pad Value (cfio_regs_pad_mmc1_d5_PAD_VAL)—Offset 3C8h

PADs Memory space Value register (access via PCU proxy)

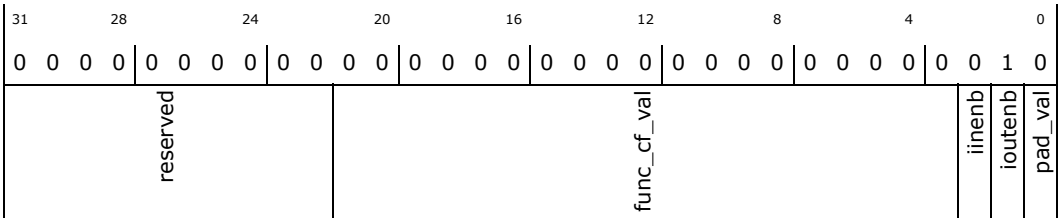
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d5_PAD_VAL: [IOBASE] + 3C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.184 Sdmmc1 D0 Pad Configuration (cfio_regs_pad_sdmmc1_d0_PCONF0)—Offset 3D0h

PADs Memory space configuration register (access via PCU proxy)

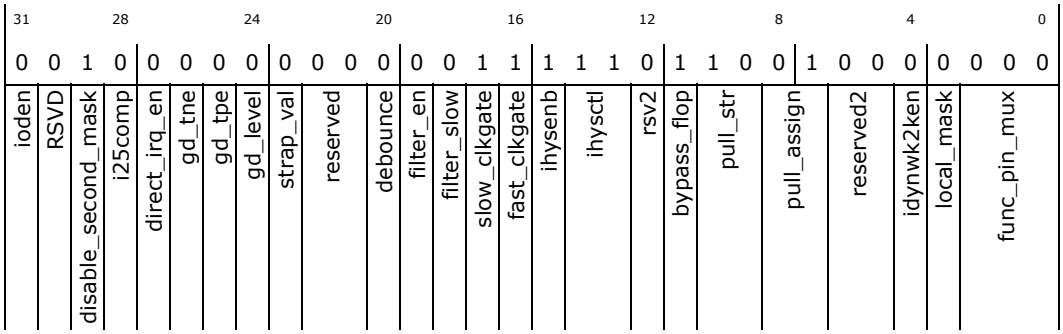
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d0_PCONF0: [IOBASE] + 3D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_17 function 1 is SDMMC1_D0 function 2 is Unused function 3 is SDMMC_45_D0

3.67.185 Sdmmc1 D0 Delay Line Multiplexer (cfio_regs_pad_sdmmc1_d0_PCONF1)—Offset 3D4h

DLL Multiplexer

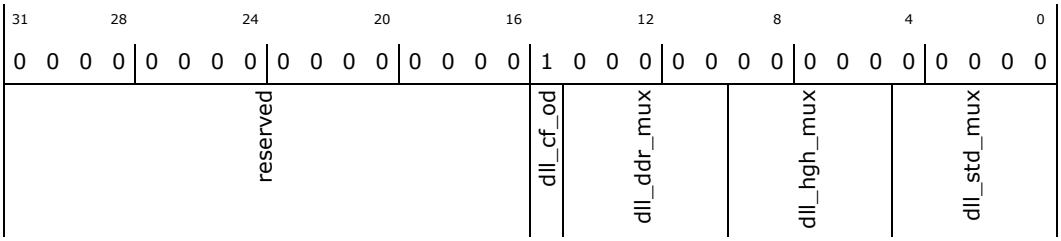
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d0_PCONF1: [IOBASE] + 3D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.186 Sdmmc1 D0 Pad Value (cfio_regs_pad_sdmmc1_d0_PAD_VAL)—Offset 3D8h

PADs Memory space Value register (access via PCU proxy)

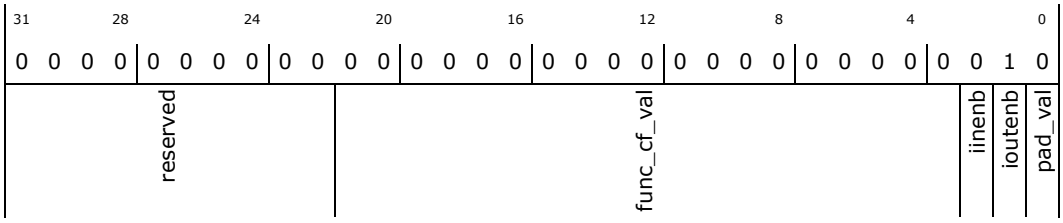
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d0_PAD_VAL: [IOBASE] + 3D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.187 Sdmmc1 Clk Pad Configuration (cfio_regs_pad_sdmmc1_clk_PCONF0)—Offset 3E0h

PADs Memory space configuration register (access via PCU proxy)

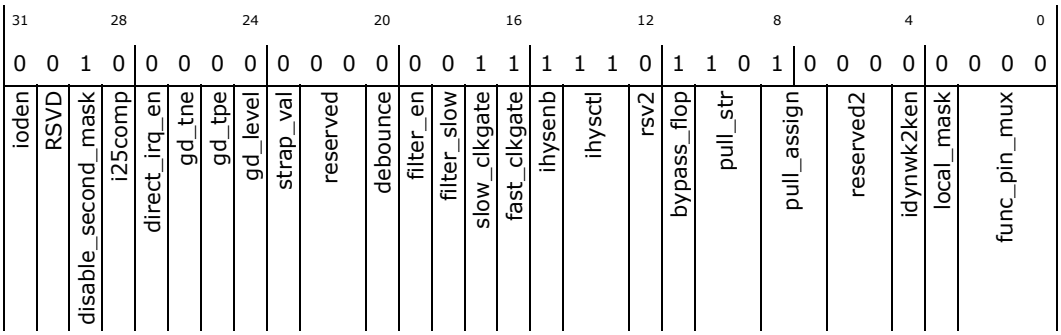
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_clk_PCONF0: [IOBASE] + 3E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_16 function 1 is SDMMC1_CLK function 2 is Unused function 3 is SDMMC_45_CLK

3.67.188 Sdmmc1 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc1_clk_PCONF1)—Offset 3E4h

DLL Multiplexer

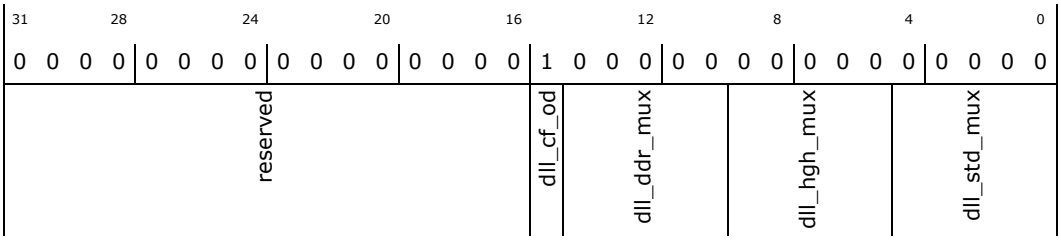
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_clk_PCONF1: [IOBASE] + 3E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RW	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RW	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RW	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RW	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.189 Sdmmc1 Clk Pad Value (cfio_regs_pad_sdmmc1_clk_PAD_VAL)—Offset 3E8h

PADs Memory space Value register (access via PCU proxy)

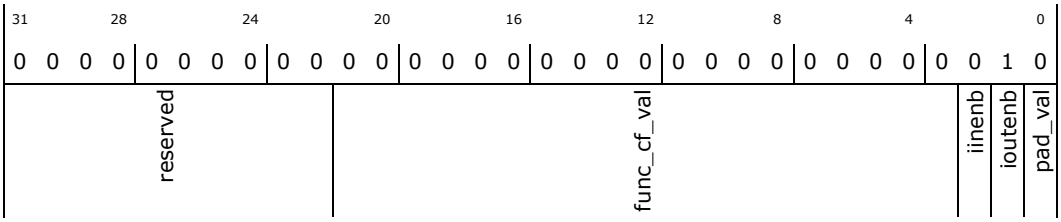
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_clk_PAD_VAL: [IOBASE] + 3E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.190 Mmc1 D7 Pad Configuration (cfio_regs_pad_mmc1_d7_PCONF0)—Offset 3F0h

PADs Memory space configuration register (access via PCU proxy)

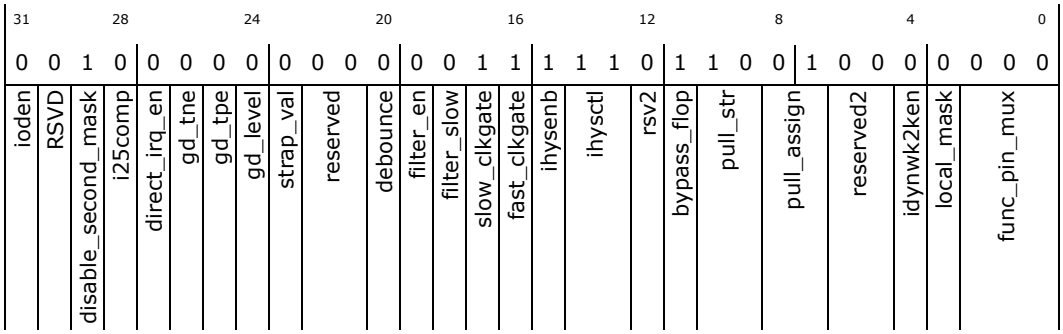
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d7_PCONF0: [IOBASE] + 3F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_24 function 1 is MMC1_D7 function 2 is Unused function 3 is MMC_45_D7

3.67.191 Mmc1 D7 Delay Line Multiplexer (cfio_regs_pad_mmc1_d7_PCONF1)—Offset 3F4h

DLL Multiplexer

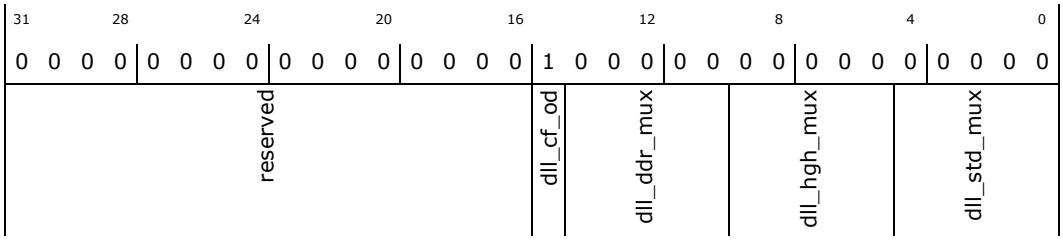
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d7_PCONF1: [IOBASE] + 3F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.192 Mmc1 D7 Pad Value (cfio_regs_pad_mmc1_d7_PAD_VAL)—Offset 3F8h

PADs Memory space Value register (access via PCU proxy)

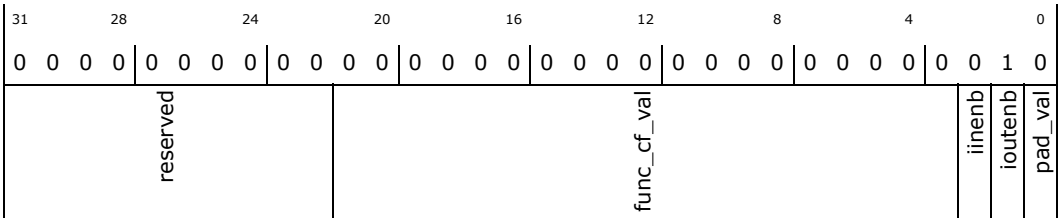
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mmc1_d7_PAD_VAL: [IOBASE] + 3F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.193 Sdmmc1 D1 Pad Configuration (cfio_regs_pad_sdmmc1_d1_PCONF0)—Offset 400h

PADs Memory space configuration register (access via PCU proxy)

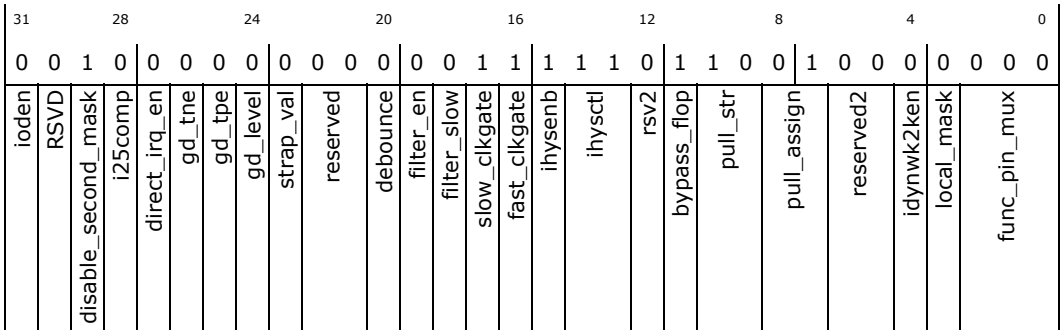
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d1_PCONF0: [IOBASE] + 400h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_18 function 1 is SDMMC1_D1 function 2 is Unused function 3 is SDMMC_45_D1

3.67.194 Sdmmc1 D1 Delay Line Multiplexer (cfio_regs_pad_sdmmc1_d1_PCONF1)—Offset 404h

DLL Multiplexer

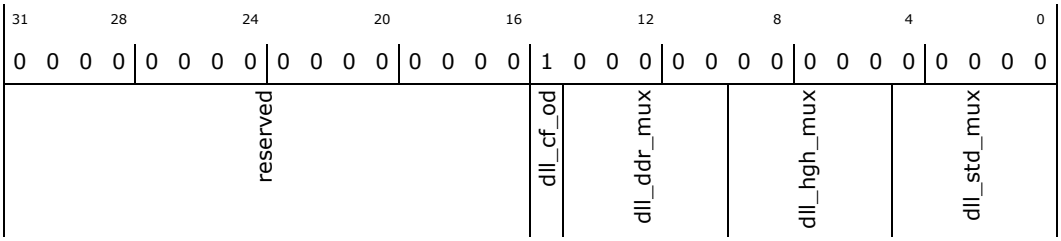
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d1_PCONF1: [IOBASE] + 404h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.195 Sdmmc1 D1 Pad Value (cfio_regs_pad_sdmmc1_d1_PAD_VAL)—Offset 408h

PADs Memory space Value register (access via PCU proxy)

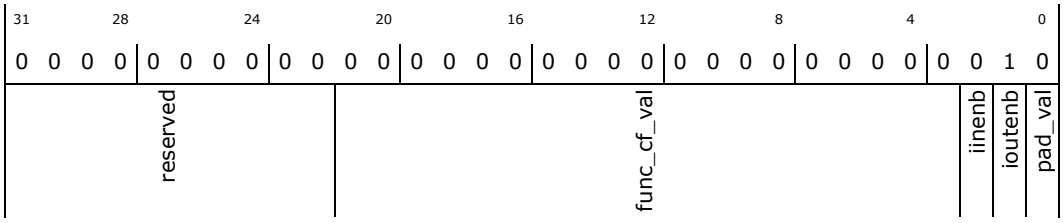
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc1_d1_PAD_VAL: [IOBASE] + 408h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.196 Lpc Clkout1 Pad Configuration (cfio_regs_pad_lpc_clkout1_PCONF0)—Offset 410h

PADs Memory space configuration register (access via PCU proxy)

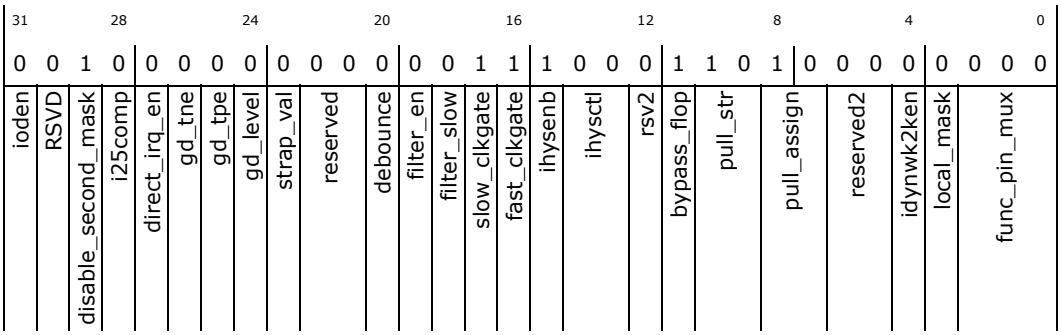
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_clkout1_PCONF0: [IOBASE] + 410h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038D00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_48 function 1 is LPC_CLKOUT1

3.67.197 Lpc Clkout1 Delay Line Multiplexer (cfio_regs_pad_lpc_clkout1_PCONF1)—Offset 414h

DLL Multiplexer

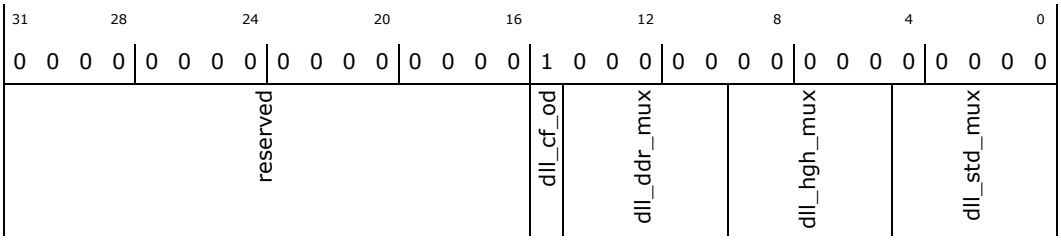
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_clkout1_PCONF1: [IOBASE] + 414h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.198 Lpc Clkout1 Pad Value (cfio_regs_pad_lpc_clkout1_PAD_VAL)—Offset 418h

PADs Memory space Value register (access via PCU proxy)

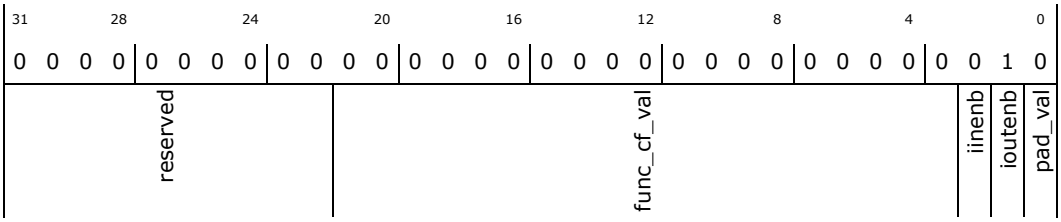
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_clkout1_PAD_VAL: [IOBASE] + 418h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.199 Lpc Ad3 Pad Configuration (cfio_regs_pad_lpc_ad3_PCONF0)—Offset 420h

PADs Memory space configuration register (access via PCU proxy)

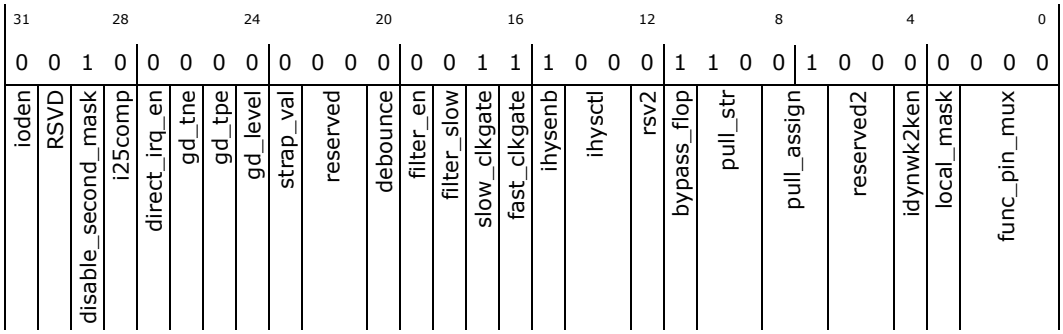
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad3_PCONF0: [IOBASE] + 420h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_45 function 1 is LPC_AD3

3.67.200 Lpc Ad3 Delay Line Multiplexer (cfio_regs_pad_lpc_ad3_PCONF1)—Offset 424h

DLL Multiplexer

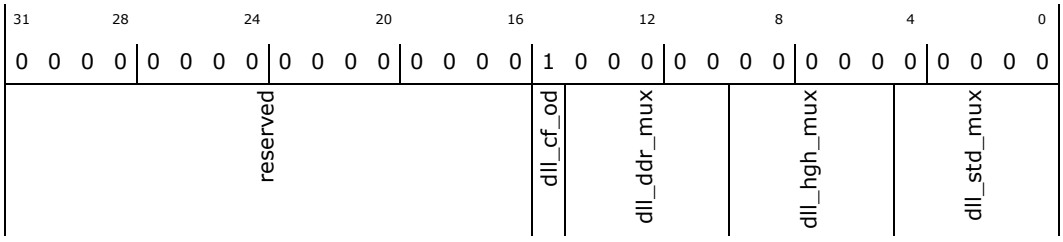
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad3_PCONF1: [IOBASE] + 424h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.201 Lpc Ad3 Pad Value (cfio_regs_pad_lpc_ad3_PAD_VAL)—Offset 428h

PADs Memory space Value register (access via PCU proxy)

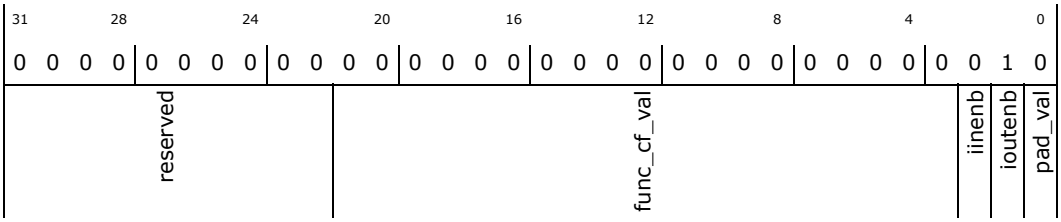
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad3_PAD_VAL: [IOBASE] + 428h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.202 Lpc Ad2 Pad Configuration (cfio_regs_pad_lpc_ad2_PCONF0)—Offset 430h

PADs Memory space configuration register (access via PCU proxy)

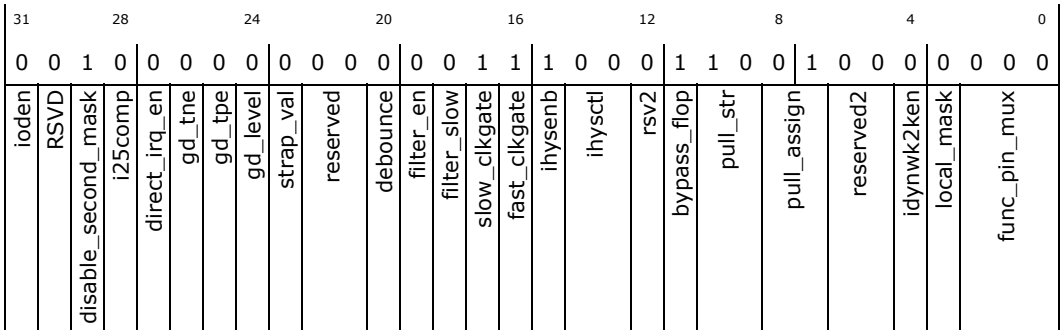
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad2_PCONF0: [IOBASE] + 430h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_44 function 1 is LPC_AD2

3.67.203 Lpc Ad2 Delay Line Multiplexer (cfio_regs_pad_lpc_ad2_PCONF1)—Offset 434h

DLL Multiplexer

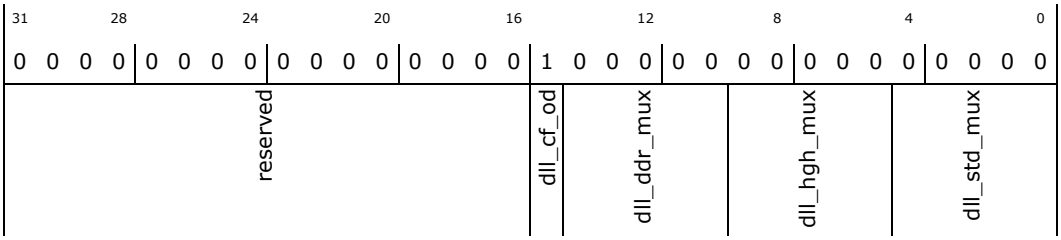
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad2_PCONF1: [IOBASE] + 434h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.204 Lpc Ad2 Pad Value (cfio_regs_pad_lpc_ad2_PAD_VAL)—Offset 438h

PADs Memory space Value register (access via PCU proxy)

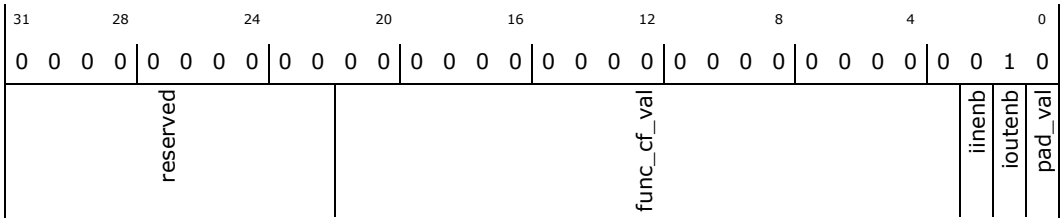
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad2_PAD_VAL: [IOBASE] + 438h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.205 Lpc Ad1 Pad Configuration (cfio_regs_pad_lpc_ad1_PCONF0)—Offset 440h

PADs Memory space configuration register (access via PCU proxy)

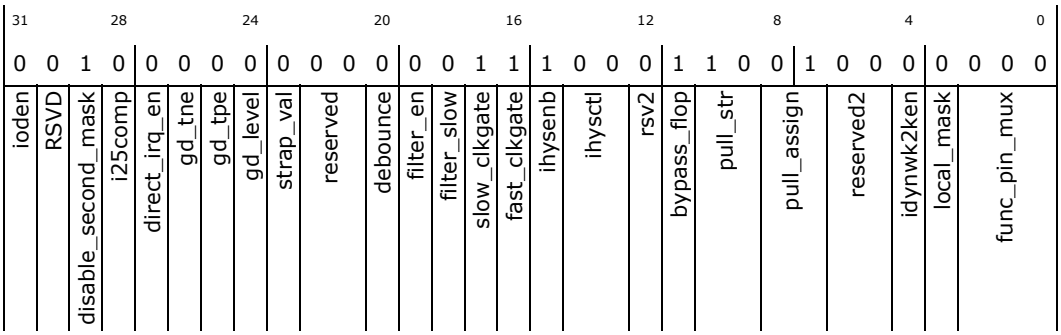
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad1_PCONF0: [IOBASE] + 440h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_43 function 1 is LPC_AD1

3.67.206 Lpc Ad1 Delay Line Multiplexer (cfio_regs_pad_lpc_ad1_PCONF1)—Offset 444h

DLL Multiplexer

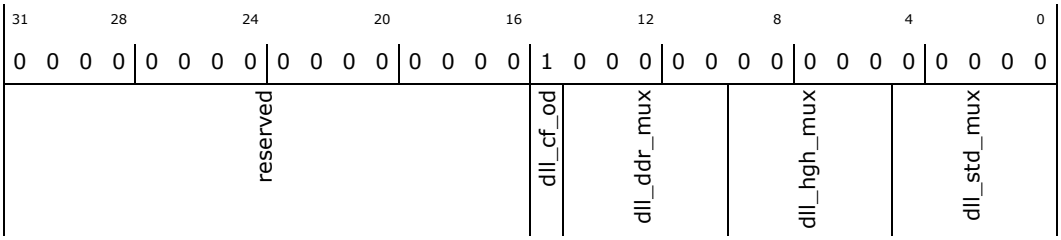
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad1_PCONF1: [IOBASE] + 444h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.207 Lpc Ad1 Pad Value (cfio_regs_pad_lpc_ad1_PAD_VAL)—Offset 448h

PADs Memory space Value register (access via PCU proxy)

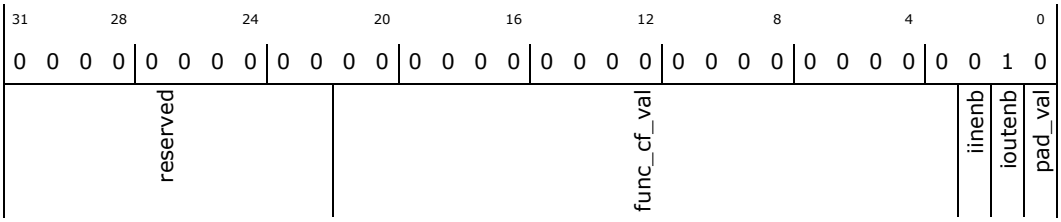
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad1_PAD_VAL: [IOBASE] + 448h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.208 Lpc Frameb Pad Configuration (cfio_regs_pad_lpc_frameb_PCONF0)—Offset 450h

PADs Memory space configuration register (access via PCU proxy)

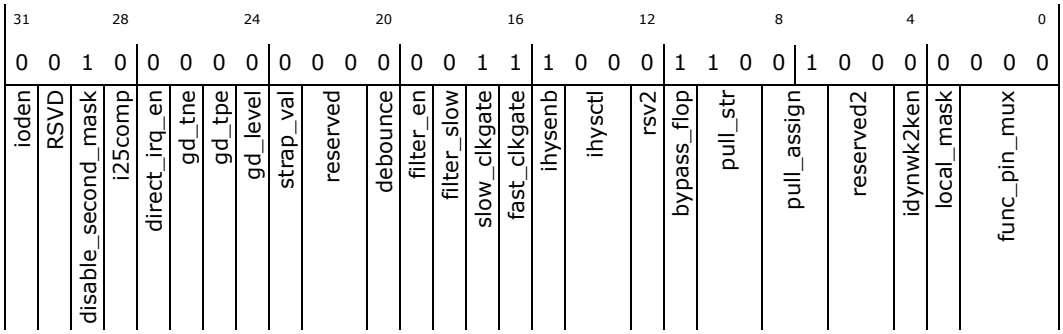
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_frameb_PCONF0: [IOBASE] + 450h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_46 function 1 is LPC_FRAMEB

3.67.209 Lpc Frameb Delay Line Multiplexer (cfio_regs_pad_lpc_frameb_PCONF1)—Offset 454h

DLL Multiplexer

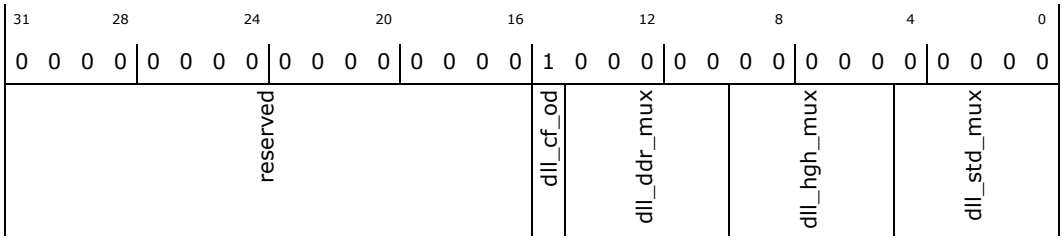
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_frameb_PCONF1: [IOBASE] + 454h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.210 Lpc Frameb Pad Value (cfio_regs_pad_lpc_frameb_PAD_VAL)—Offset 458h

PADs Memory space Value register (access via PCU proxy)

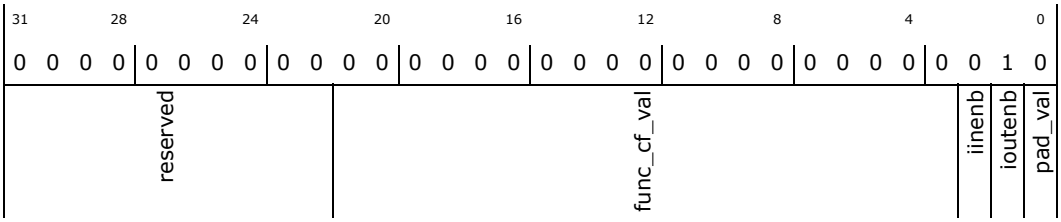
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_frameb_PAD_VAL: [IOBASE] + 458h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.211 Lpc Ad0 Pad Configuration (cfio_regs_pad_lpc_ad0_PCONF0)—Offset 460h

PADs Memory space configuration register (access via PCU proxy)

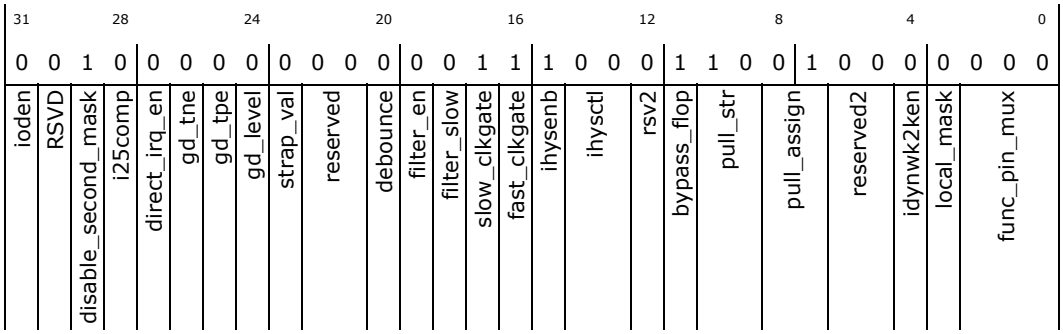
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad0_PCONF0: [IOBASE] + 460h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_42 function 1 is LPC_AD0

3.67.212 Lpc Ad0 Delay Line Multiplexer (cfio_regs_pad_lpc_ad0_PCONF1)—Offset 464h

DLL Multiplexer

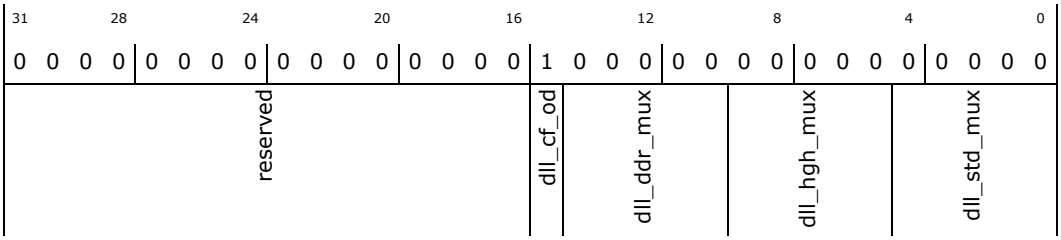
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad0_PCONF1: [IOBASE] + 464h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.213 Lpc Ad0 Pad Value (cfio_regs_pad_lpc_ad0_PAD_VAL)—Offset 468h

PADs Memory space Value register (access via PCU proxy)

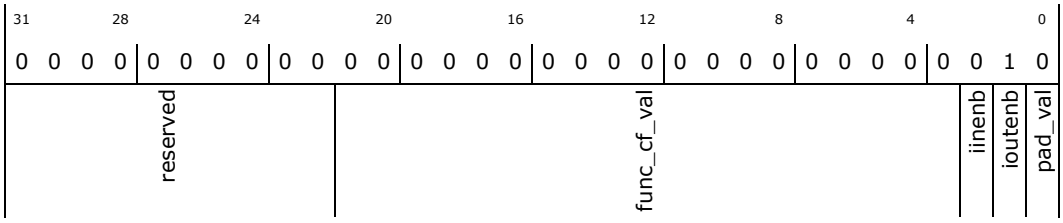
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_ad0_PAD_VAL: [IOBASE] + 468h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.214 Lpc Clkout0 Pad Configuration (cfio_regs_pad_lpc_clkout0_PCONF0)—Offset 470h

PADs Memory space configuration register (access via PCU proxy)

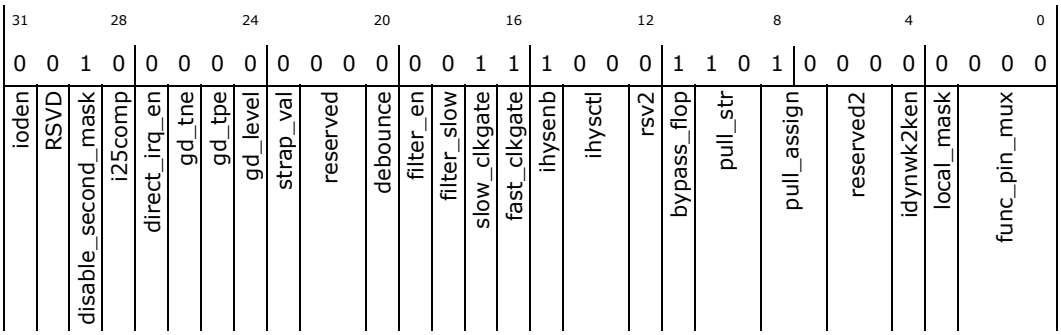
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_clkout0_PCONF0: [IOBASE] + 470h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038D00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_47 function 1 is LPC_CLKOUT0

3.67.215 Lpc Clkout0 Delay Line Multiplexer (cfio_regs_pad_lpc_clkout0_PCONF1)—Offset 474h

DLL Multiplexer

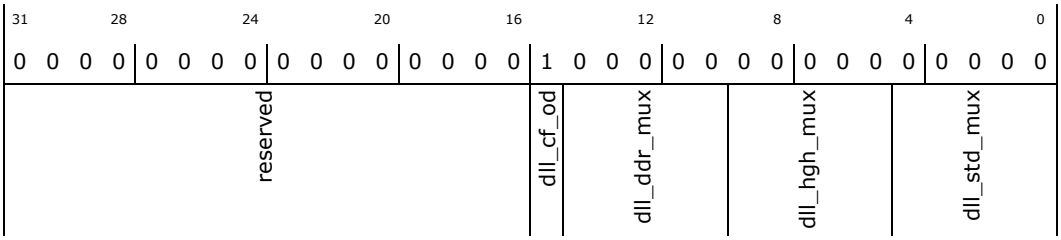
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_clkout0_PCONF1: [IOBASE] + 474h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.216 Lpc Clkout0 Pad Value (cfio_regs_pad_lpc_clkout0_PAD_VAL)—Offset 478h

PADs Memory space Value register (access via PCU proxy)

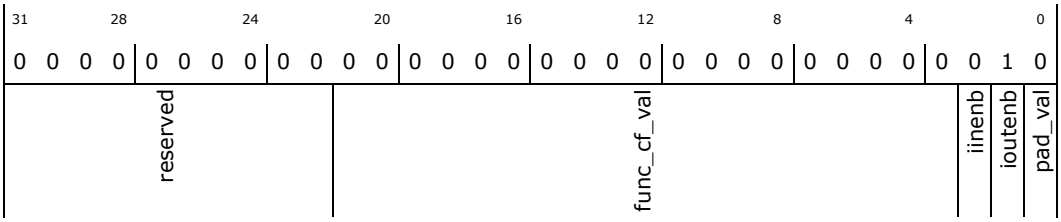
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_clkout0_PAD_VAL: [IOBASE] + 478h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.217 Lpc Clkrunb Pad Configuration (cfio_regs_pad_lpc_clkrunb_PCONF0)—Offset 480h

PADs Memory space configuration register (access via PCU proxy)

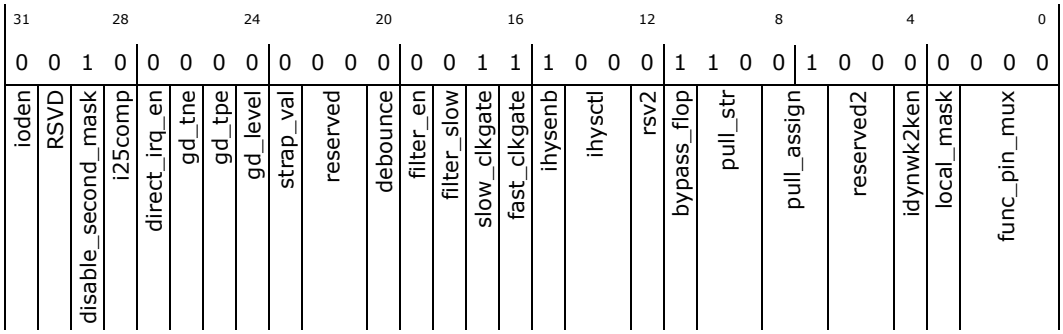
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_clkrunb_PCONF0: [IOBASE] + 480h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_49 function 1 is LPC_CLKRUNB

3.67.218 Lpc Clkrunb Delay Line Multiplexer (cfio_regs_pad_lpc_clkrunb_PCONF1)—Offset 484h

DLL Multiplexer

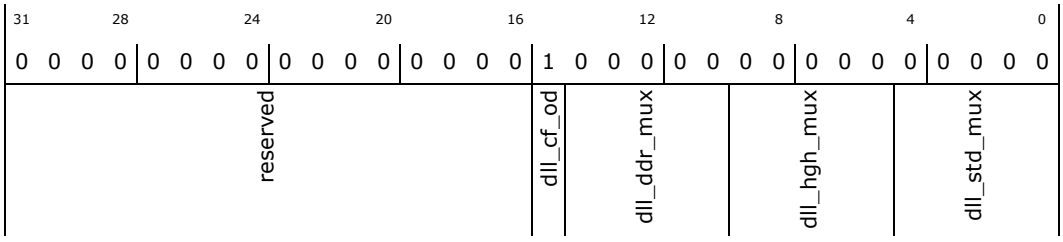
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_clkrunb_PCONF1: [IOBASE] + 484h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.219 Lpc Clkrunb Pad Value (cfio_regs_pad_lpc_clkrunb_PAD_VAL)—Offset 488h

PADs Memory space Value register (access via PCU proxy)

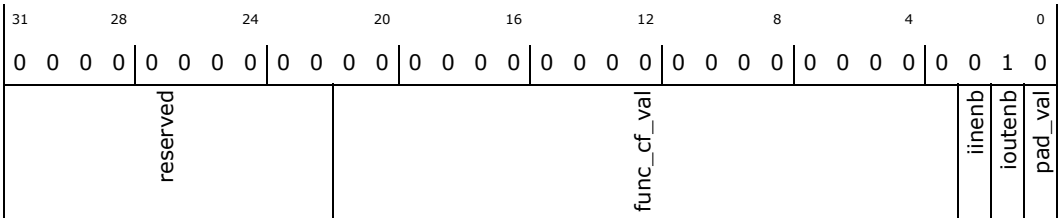
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_lpc_clkrunb_PAD_VAL: [IOBASE] + 488h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.220 Hv Crt Ddc Clk Pad Configuration (cfio_regs_pad_hv_crt_ddc_clk_PCONF0)—Offset 490h

PADs Memory space configuration register (access via PCU proxy)

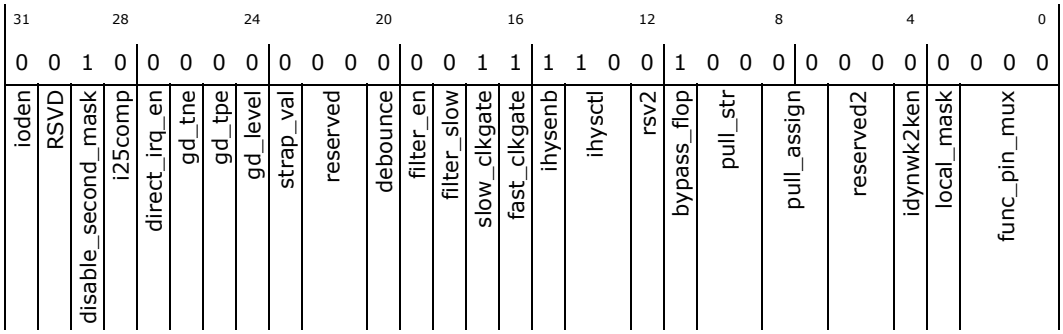
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_ddc_clk_PCONF0: [IOBASE] + 490h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is HV_CRT_DDC_CLK

3.67.221 Hv Crt Ddc Clk Delay Line Multiplexer (cfio_regs_pad_hv_crt_ddc_clk_PCONF1)—Offset 494h

DLL Multiplexer

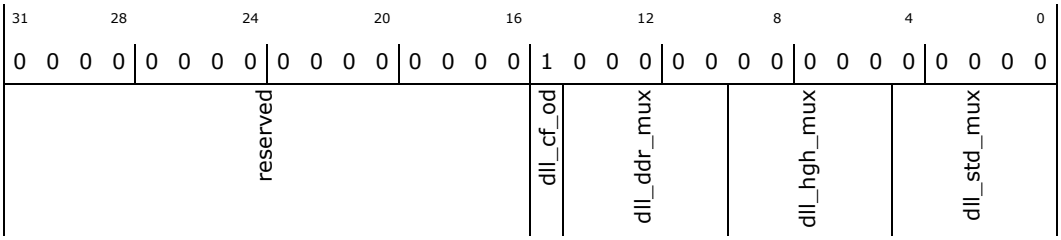
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_ddc_clk_PCONF1: [IOBASE] + 494h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.222 Hv Crt Ddc Clk Pad Value (cfio_regs_pad_hv_crt_ddc_clk_PAD_VAL)—Offset 498h

PADs Memory space Value register (access via PCU proxy)

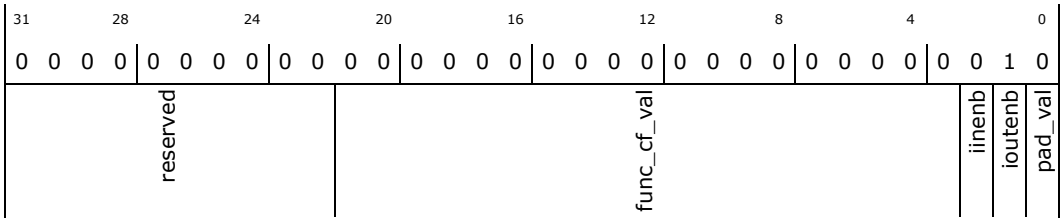
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_ddc_clk_PAD_VAL: [IOBASE] + 498h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.223 Hv Crt Vsync Pad Configuration (cfio_regs_pad_hv_crt_vsync_PCONF0)—Offset 4A0h

PADs Memory space configuration register (access via PCU proxy)

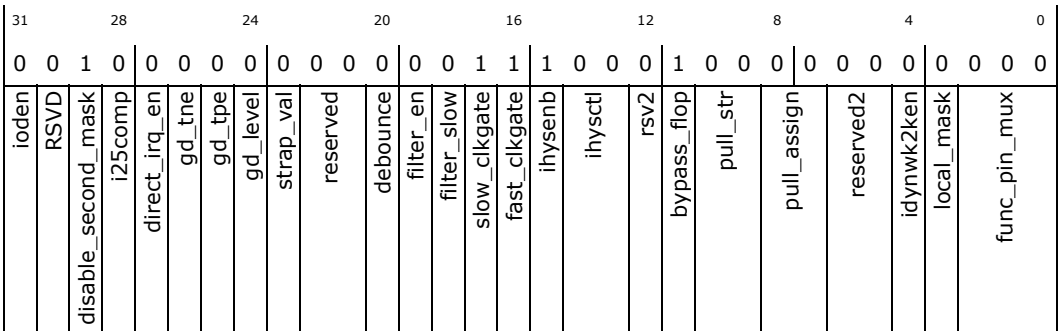
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_vsync_PCONF0: [IOBASE] + 4A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RW	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is HV_CRT_VSYNC

3.67.224 Hv Crt Vsync Delay Line Multiplexer (cfio_regs_pad_hv_crt_vsync_PCONF1)—Offset 4A4h

DLL Multiplexer

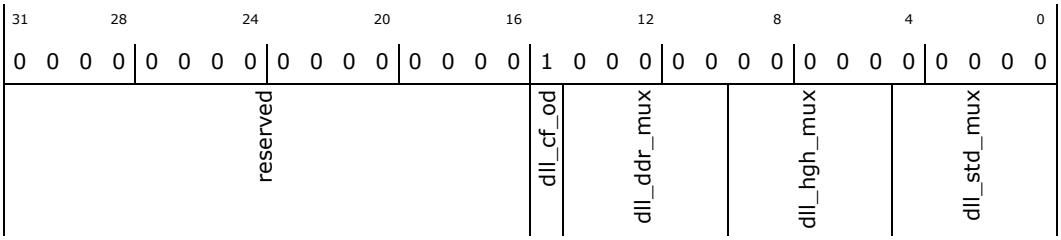
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_vsync_PCONF1: [IOBASE] + 4A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.225 Hv Crt Vsync Pad Value (cfio_regs_pad_hv_crt_vsync_PAD_VAL)—Offset 4A8h

PADs Memory space Value register (access via PCU proxy)

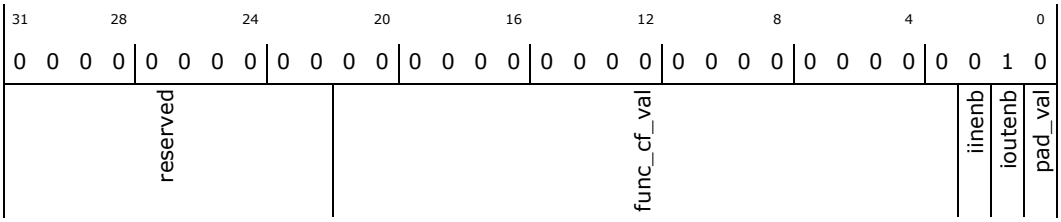
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_vsync_PAD_VAL: [IOBASE] + 4A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.226 Hv Crt Hsync Pad Configuration (cfio_regs_pad_hv_crt_hsync_PCONF0)—Offset 4B0h

PADs Memory space configuration register (access via PCU proxy)

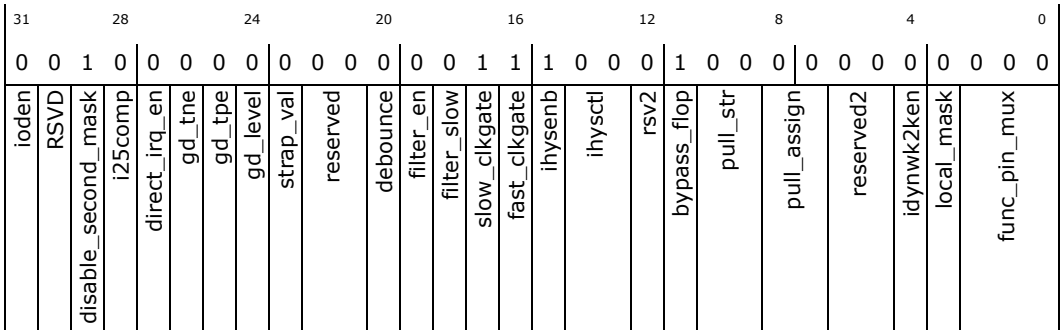
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

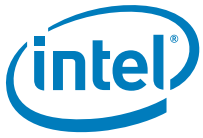
cfio_regs_pad_hv_crt_hsync_PCONF0: [IOBASE] + 4B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.



Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RW	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is HV_CRT_HSYNC

3.67.227 Hv Crt Hsync Delay Line Multiplexer (cfio_regs_pad_hv_crt_hsync_PCONF1)—Offset 4B4h

DLL Multiplexer

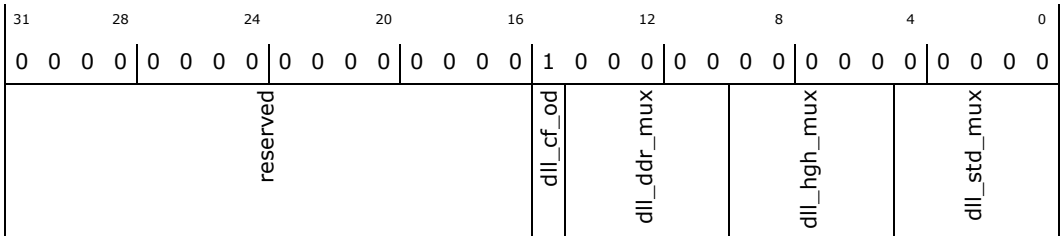
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_hsync_PCONF1: [IOBASE] + 4B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.228 Hv Crt Hsync Pad Value (cfio_regs_pad_hv_crt_hsync_PAD_VAL)—Offset 4B8h

PADs Memory space Value register (access via PCU proxy)

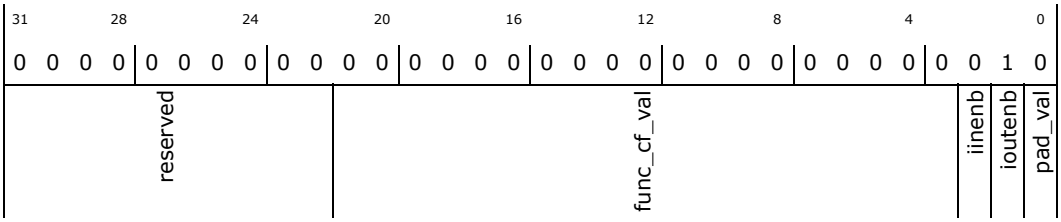
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_hsync_PAD_VAL: [IOBASE] + 4B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.229 Hv Crt Ddc Data Pad Configuration (cfio_regs_pad_hv_crt_ddc_data_PCONF0)—Offset 4C0h

PADs Memory space configuration register (access via PCU proxy)

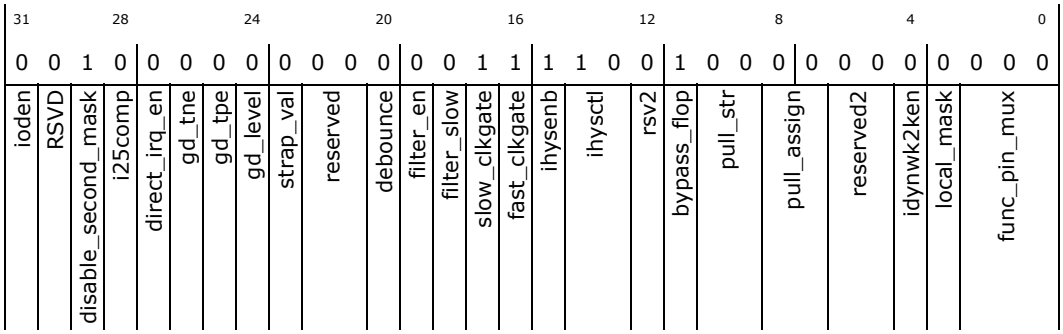
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_ddc_data_PCONF0: [IOBASE] + 4C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is HV_CRT_DDC_DATA

3.67.230 Hv Crt Ddc Data Delay Line Multiplexer (cfio_regs_pad_hv_crt_ddc_data_PCONF1)—Offset 4C4h

DLL Multiplexer

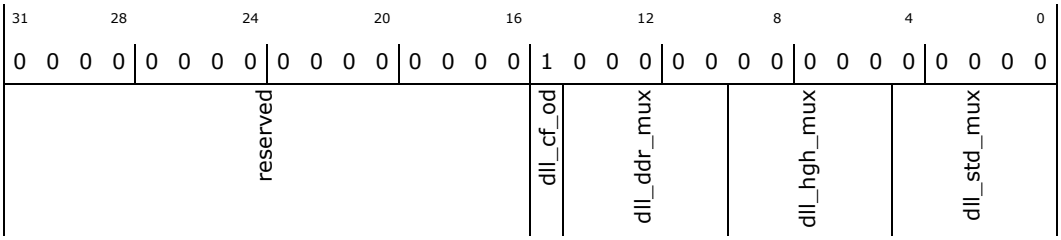
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_ddc_data_PCONF1: [IOBASE] + 4C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.231 Hv Crt Ddc Data Pad Value (cfio_regs_pad_hv_crt_ddc_data_PAD_VAL)—Offset 4C8h

PADs Memory space Value register (access via PCU proxy)

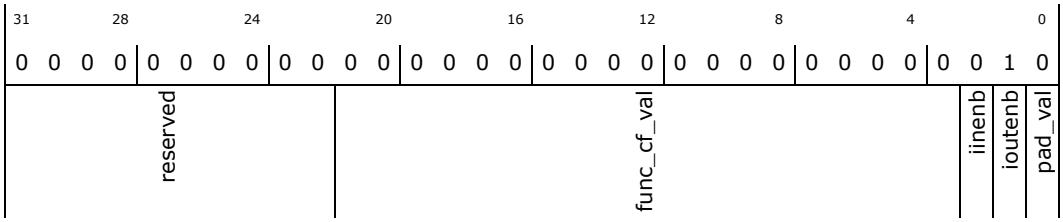
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hv_crt_ddc_data_PAD_VAL: [IOBASE] + 4C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.232 Mhsi Acdata Pad Configuration (cfio_regs_pad_mhsi_acdata_PCONF0)—Offset 4D0h

PADs Memory space configuration register (access via PCU proxy)

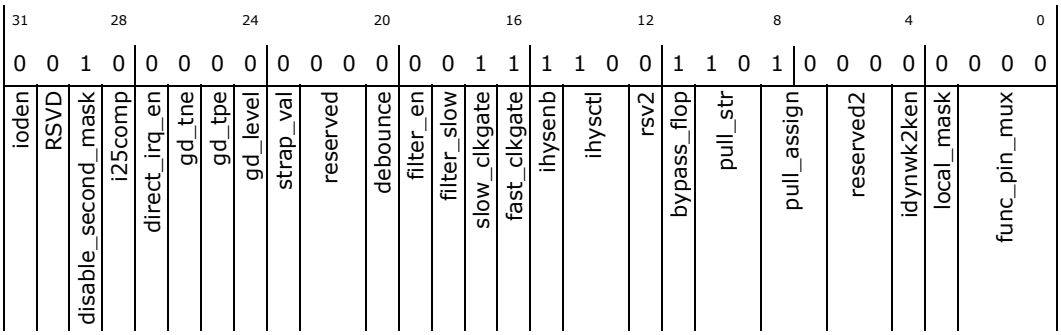
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acdata_PCONF0: [IOBASE] + 4D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_55 function 1 is MHSI_ACDATA

3.67.233 Mhsi Acdata Delay Line Multiplexer (cfio_regs_pad_mhsi_acdata_PCONF1)—Offset 4D4h

DLL Multiplexer

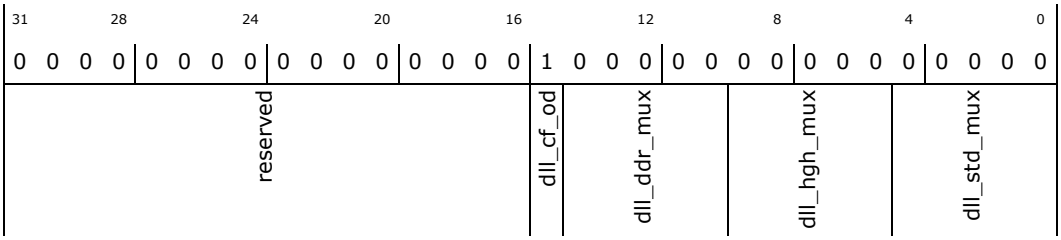
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acdata_PCONF1: [IOBASE] + 4D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.234 Mhsi Acdata Pad Value (cfio_regs_pad_mhsi_acdata_PAD_VAL)—Offset 4D8h

PADs Memory space Value register (access via PCU proxy)

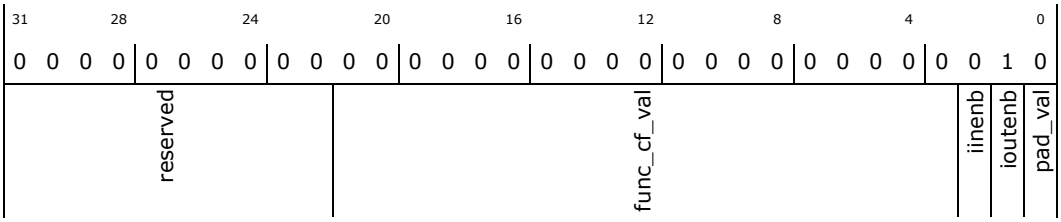
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acdata_PAD_VAL: [IOBASE] + 4D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.235 Mhsi Acwake Pad Configuration (cfio_regs_pad_mhsi_acwake_PCONF0)—Offset 4E0h

PADs Memory space configuration register (access via PCU proxy)

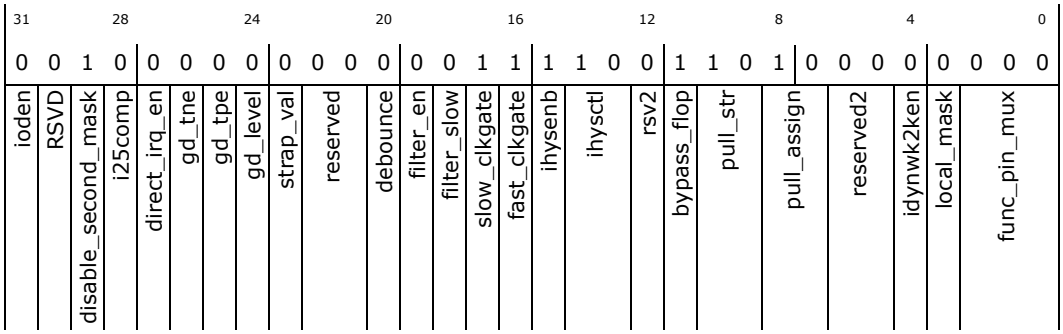
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acwake_PCONF0: [IOBASE] + 4E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_58 function 1 is MHSI_ACWAKE

3.67.236 Mhsi Acwake Delay Line Multiplexer (cfio_regs_pad_mhsi_acwake_PCONF1)—Offset 4E4h

DLL Multiplexer

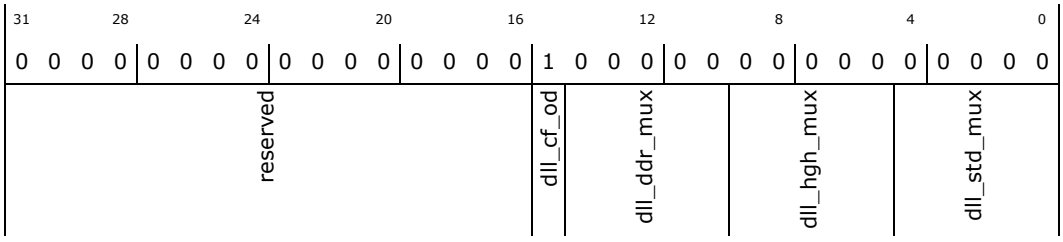
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acwake_PCONF1: [IOBASE] + 4E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.237 Mhsi Acwake Pad Value (cfio_regs_pad_mhsi_acwake_PAD_VAL)—Offset 4E8h

PADs Memory space Value register (access via PCU proxy)

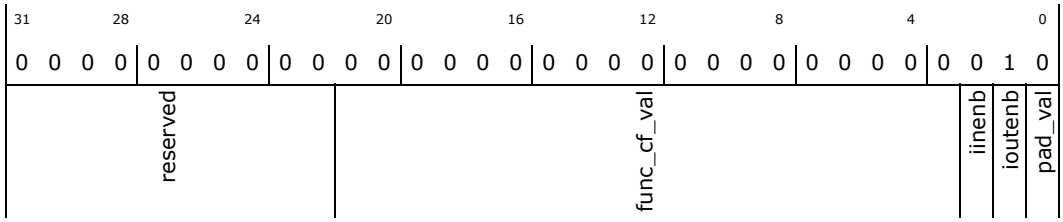
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acwake_PAD_VAL: [IOBASE] + 4E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.238 Mhsi Acflag Pad Configuration (cfio_regs_pad_mhsi_acflag_PCONF0)—Offset 4F0h

PADs Memory space configuration register (access via PCU proxy)

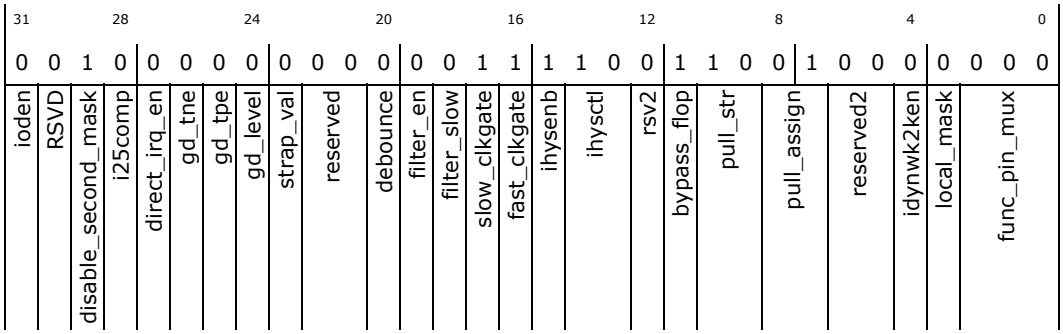
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acflag_PCONF0: [IOBASE] + 4F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_56 function 1 is MHSI_ACFLAG

3.67.239 Mhsi Acflag Delay Line Multiplexer (cfio_regs_pad_mhsi_acflag_PCONF1)—Offset 4F4h

DLL Multiplexer

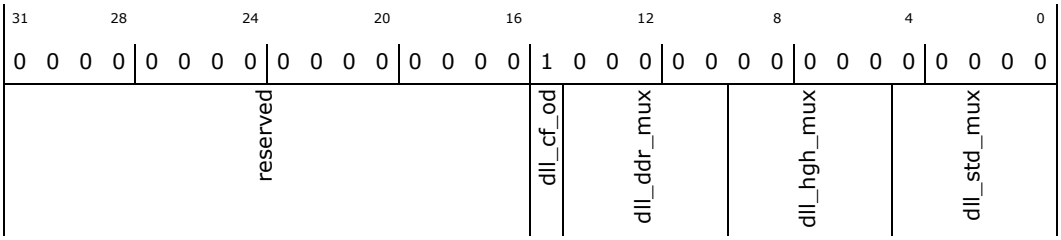
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acflag_PCONF1: [IOBASE] + 4F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.240 Mhsi Acflag Pad Value (cfio_regs_pad_mhsi_acflag_PAD_VAL)—Offset 4F8h

PADs Memory space Value register (access via PCU proxy)

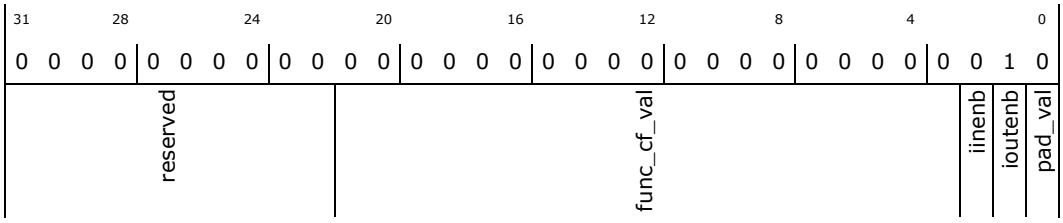
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acflag_PAD_VAL: [IOBASE] + 4F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.241 Mhsi Caflag Pad Configuration (cfio_regs_pad_mhsi_caflag_PCONF0)—Offset 500h

PADs Memory space configuration register (access via PCU proxy)

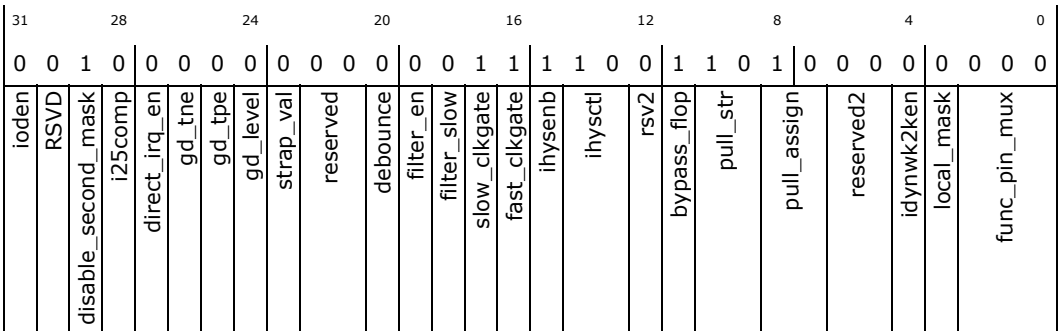
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_caflag_PCONF0: [IOBASE] + 500h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_60 function 1 is MHSI_CAFLAG

3.67.242 Mhsi Caflag Delay Line Multiplexer (cfio_regs_pad_mhsi_caflag_PCONF1)—Offset 504h

DLL Multiplexer

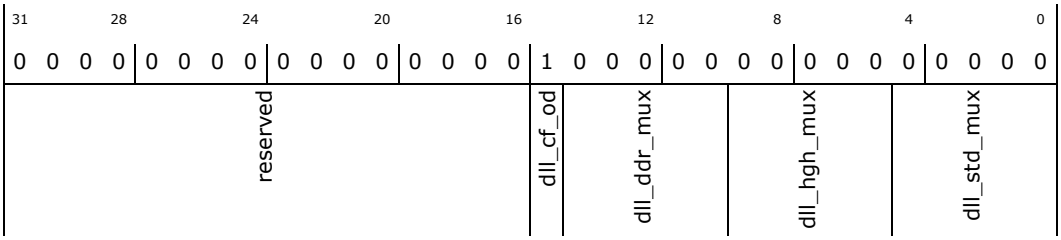
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_caflag_PCONF1: [IOBASE] + 504h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RW	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RW	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RW	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RW	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.243 Mhsi Caflag Pad Value (cfio_regs_pad_mhsi_caflag_PAD_VAL)—Offset 508h

PADs Memory space Value register (access via PCU proxy)

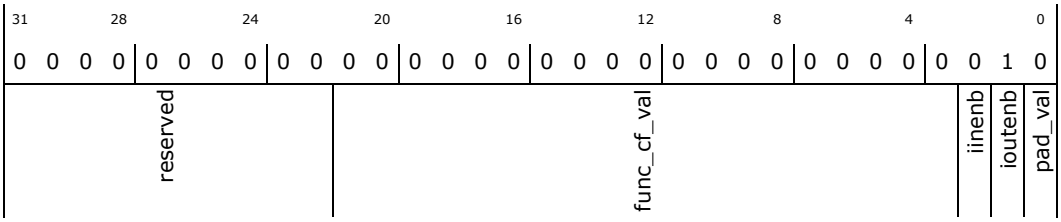
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_caflag_PAD_VAL: [IOBASE] + 508h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.244 Mhsi Cadata Pad Configuration (cfio_regs_pad_mhsi_cadata_PCONF0)—Offset 510h

PADs Memory space configuration register (access via PCU proxy)

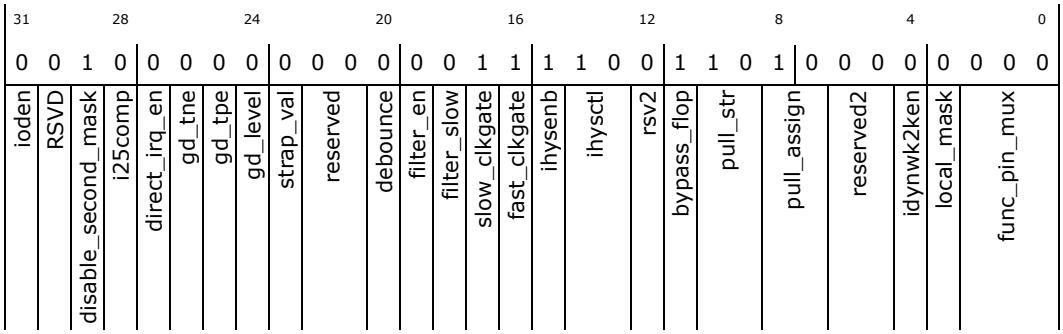
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_cadata_PCONF0: [IOBASE] + 510h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_59 function 1 is MHSI_CADATA function 2 is DLL_FBCLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 3 is DLL_REFCLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01

3.67.245 Mhsi Cadata Delay Line Multiplexer (cfio_regs_pad_mhsi_cadata_PCONF1)—Offset 514h

DLL Multiplexer

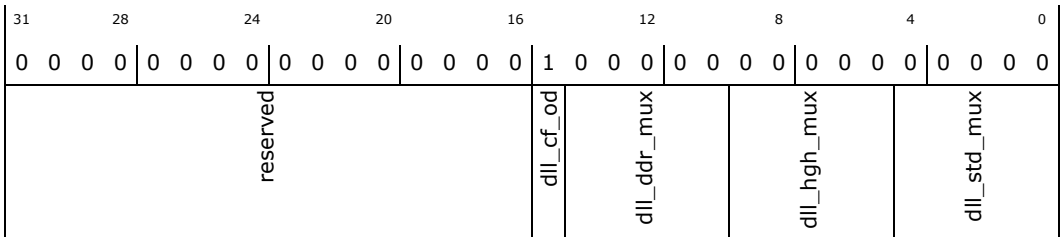
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_cadata_PCONF1: [IOBASE] + 514h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RW	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RW	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RW	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux

Bit Range	Default & Access	Description
4:0	00000b RW	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.246 Mhsi Cadata Pad Value (cfio_regs_pad_mhsi_cadata_PAD_VAL)—Offset 518h

PADs Memory space Value register (access via PCU proxy)

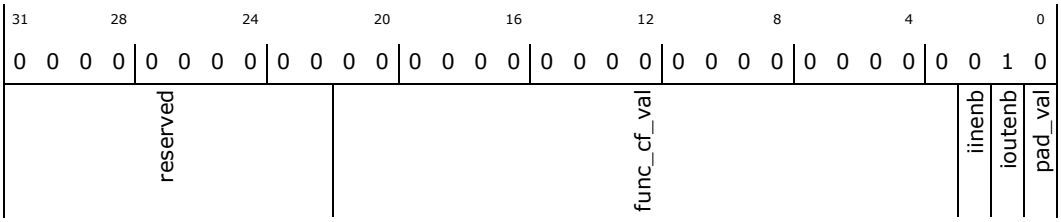
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_cadata_PAD_VAL: [IOBASE] + 518h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.247 Mhsi Caready Pad Configuration (cfio_regs_pad_mhsi_caready_PCONF0)—Offset 520h

PADs Memory space configuration register (access via PCU proxy)

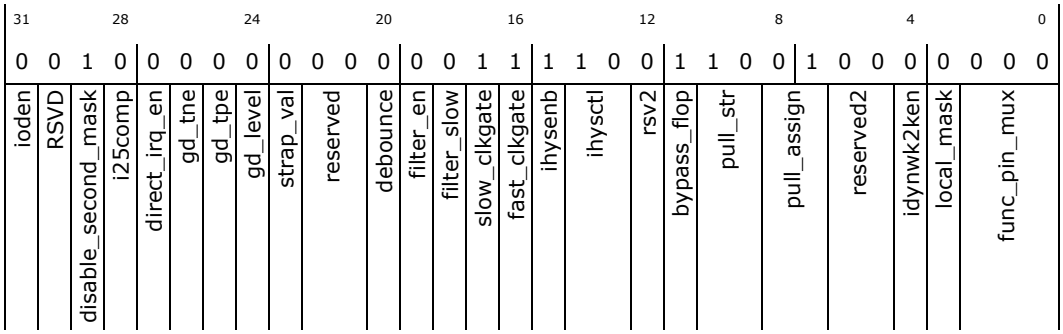
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_caready_PCONF0: [IOBASE] + 520h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register

Bit Range	Default & Access	Description
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_61 function 1 is UART3_RXD

3.67.248 Mhsi Caready Delay Line Multiplexer (cfio_regs_pad_mhsi_caready_PCONF1)—Offset 524h

DLL Multiplexer

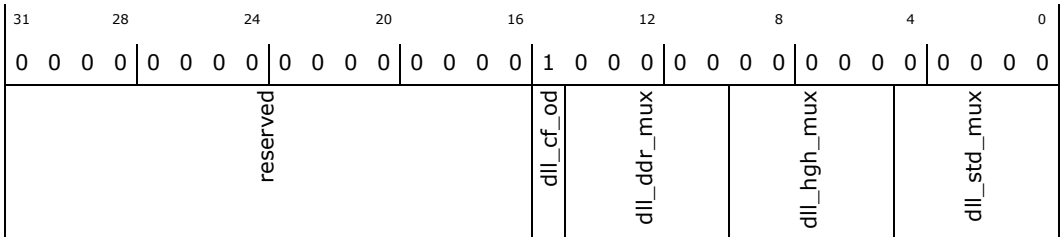
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_caready_PCONF1: [IOBASE] + 524h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.249 Mhsi Caready Pad Value (cfio_regs_pad_mhsi_caready_PAD_VAL)—Offset 528h

PADs Memory space Value register (access via PCU proxy)

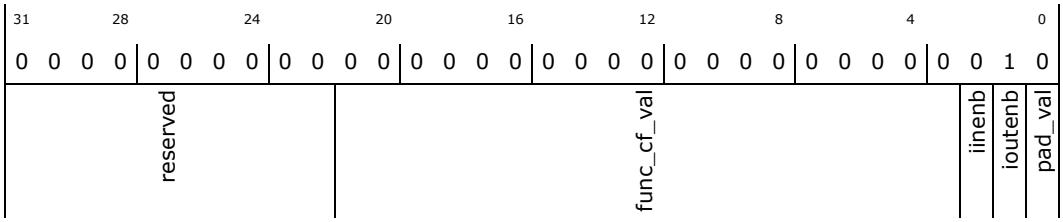
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_caready_PAD_VAL: [IOBASE] + 528h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low

Bit Range	Default & Access	Description
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.250 Mhsi Acready Pad Configuration (cfio_regs_pad_mhsi_acready_PCONF0)—Offset 530h

PADs Memory space configuration register (access via PCU proxy)

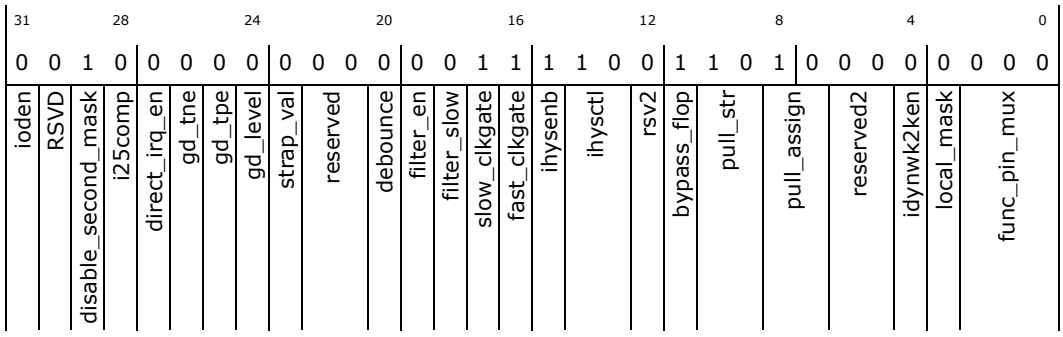
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acready_PCONF0: [IOBASE] + 530h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_57 function 1 is UART3_TXD

3.67.251 Mhsi Acready Delay Line Multiplexer (cfio_regs_pad_mhsi_acready_PCONF1)—Offset 534h

DLL Multiplexer

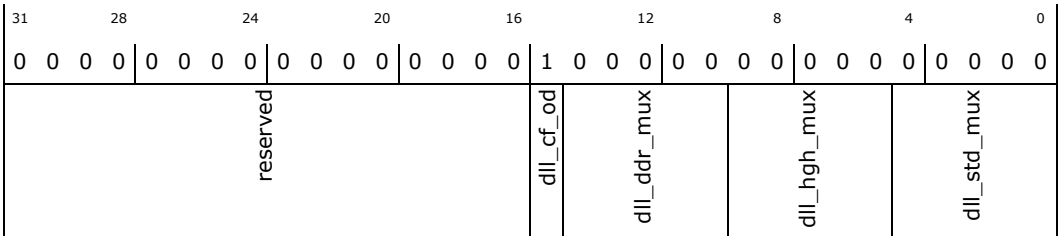
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acready_PCONF1: [IOBASE] + 534h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.252 Mhsi Acready Pad Value (cfio_regs_pad_mhsi_acready_PAD_VAL)—Offset 538h

PADs Memory space Value register (access via PCU proxy)

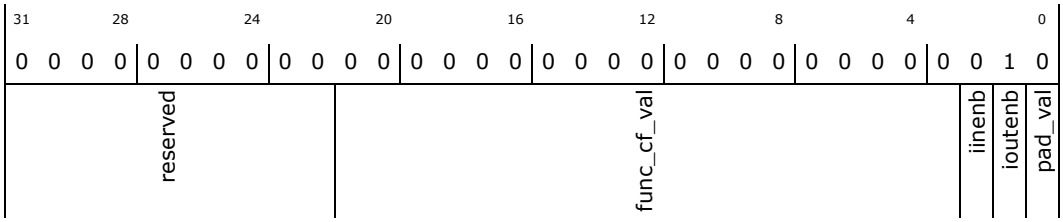
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_mhsi_acready_PAD_VAL: [IOBASE] + 538h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.253 Hda Dockenb Pad Configuration (cfio_regs_pad_hda_dockenb_PCONF0)—Offset 540h

PADs Memory space configuration register (access via PCU proxy)

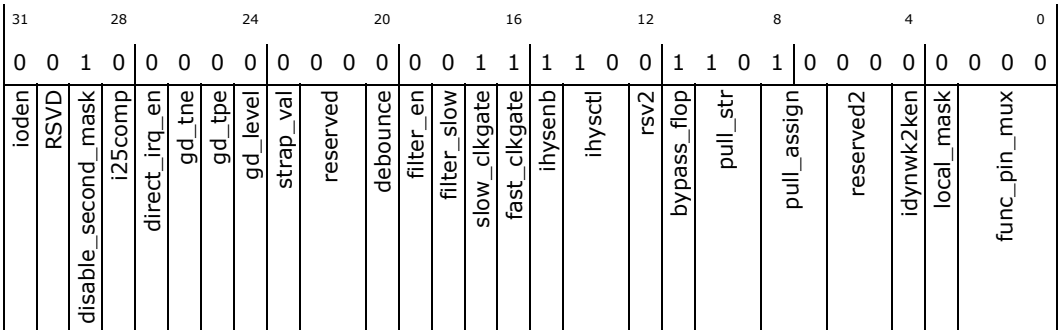
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_dockenb_PCONF0: [IOBASE] + 540h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_15 function 1 is GP_SSP_1_I2S_RXD function 2 is HDA_DOCKENB

3.67.254 Hda Dockenb Delay Line Multiplexer (cfio_regs_pad_hda_dockenb_PCONF1)—Offset 544h

DLL Multiplexer

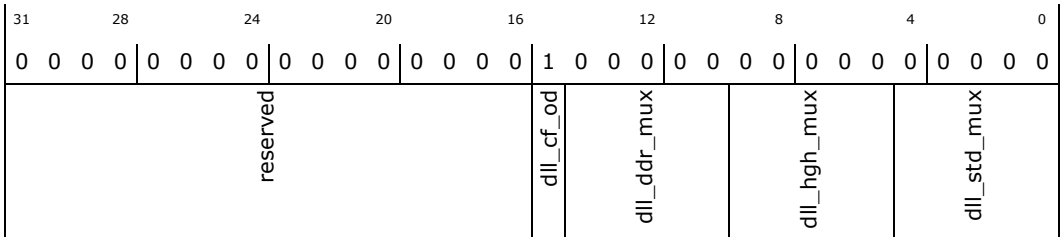
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_dockenb_PCONF1: [IOBASE] + 544h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.255 Hda Dockenb Pad Value (cfio_regs_pad_hda_dockenb_PAD_VAL)—Offset 548h

PADs Memory space Value register (access via PCU proxy)

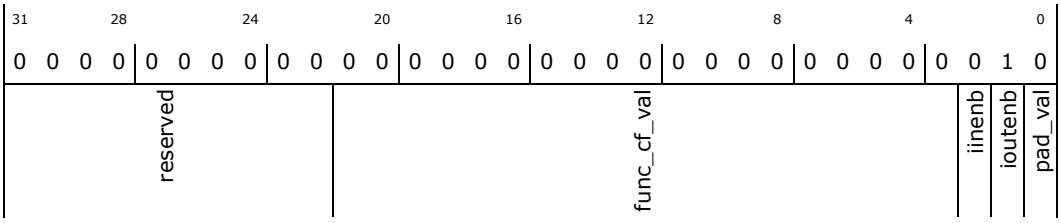
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_hda_dockenb_PAD_VAL: [IOBASE] + 548h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.256 Sata Gp0 Pad Configuration (cfio_regs_pad_sata_gp0_PCONF0)—Offset 550h

PADs Memory space configuration register (access via PCU proxy)

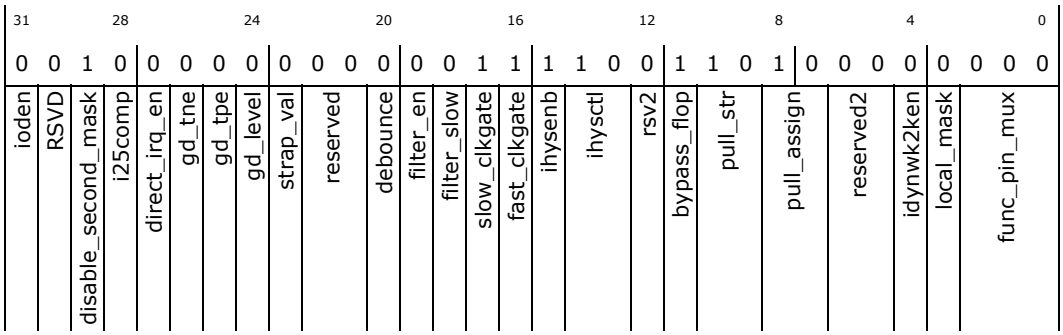
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sata_gp0_PCONF0: [IOBASE] + 550h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_0 function 1 is SATA_GP0

3.67.257 Sata Gp0 Delay Line Multiplexer (cfio_regs_pad_sata_gp0_PCONF1)—Offset 554h

DLL Multiplexer

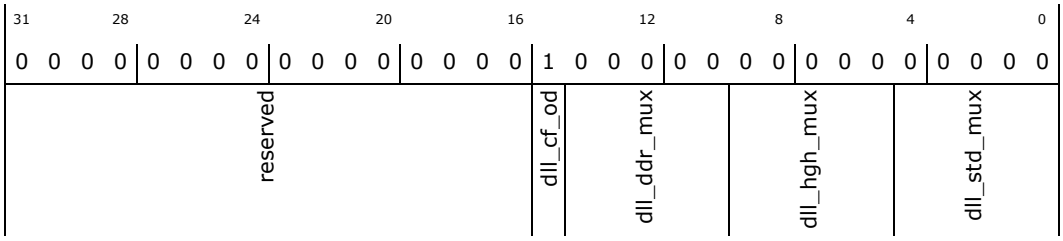
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sata_gp0_PCONF1: [IOBASE] + 554h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.258 Sata Gp0 Pad Value (cfio_regs_pad_sata_gp0_PAD_VAL)—Offset 558h

PADs Memory space Value register (access via PCU proxy)

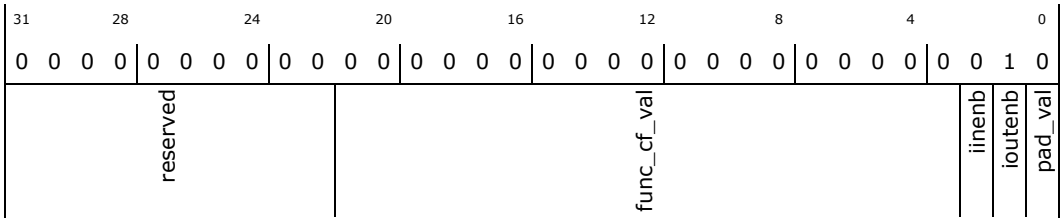
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sata_gp0_PAD_VAL: [IOBASE] + 558h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.259 Ilb Serirq Pad Configuration (cfio_regs_pad_ilb_serirq_PCONF0)—Offset 560h

PADs Memory space configuration register (access via PCU proxy)

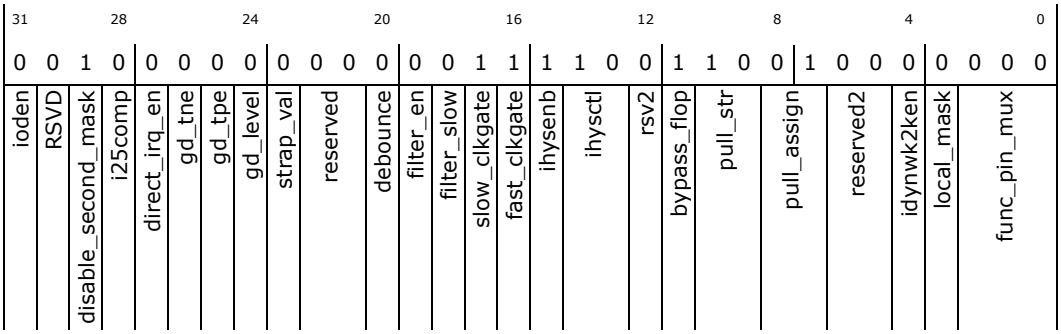
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_ilb_serirq_PCONF0: [IOBASE] + 560h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_50 function 1 is ILB_SERIRQ

3.67.260 Ilb Serirq Delay Line Multiplexer (cfio_regs_pad_ilb_serirq_PCONF1)—Offset 564h

DLL Multiplexer

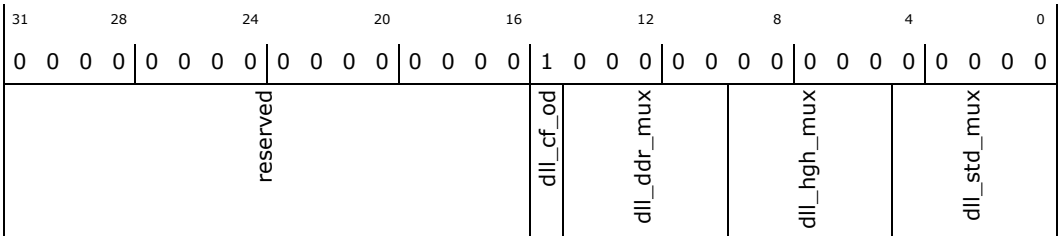
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_ilb_serirq_PCONF1: [IOBASE] + 564h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.261 Ilb Serirq Pad Value (cfio_regs_pad_ilb_serirq_PAD_VAL)—Offset 568h

PADs Memory space Value register (access via PCU proxy)

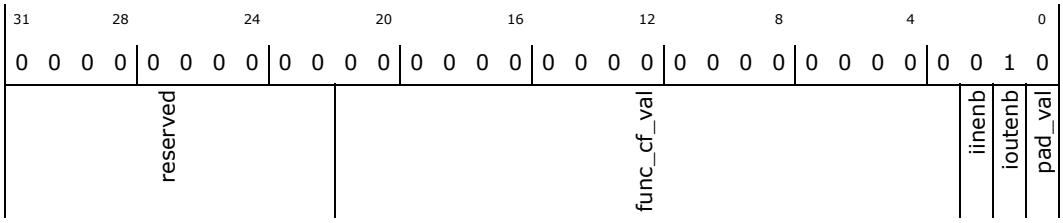
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_ilb_serirq_PAD_VAL: [IOBASE] + 568h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.262 Plt Clk1 Pad Configuration (cfio_regs_pad_plt_clk1_PCONF0)—Offset 570h

PADs Memory space configuration register (access via PCU proxy)

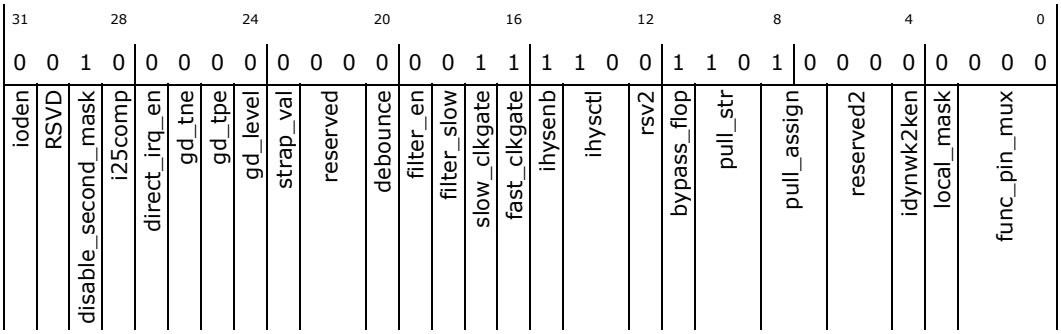
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk1_PCONF0: [IOBASE] + 570h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_97 function 1 is PLT_CLK1

3.67.263 Plt Clk1 Delay Line Multiplexer (cfio_regs_pad_plt_clk1_PCONF1)—Offset 574h

DLL Multiplexer

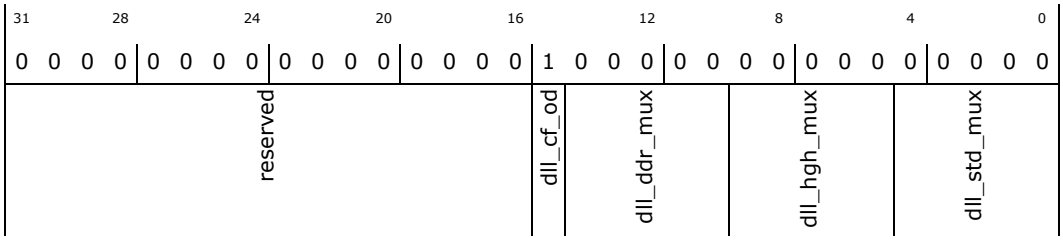
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk1_PCONF1: [IOBASE] + 574h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.264 Plt Clk1 Pad Value (cfio_regs_pad_plt_clk1_PAD_VAL)—Offset 578h

PADs Memory space Value register (access via PCU proxy)

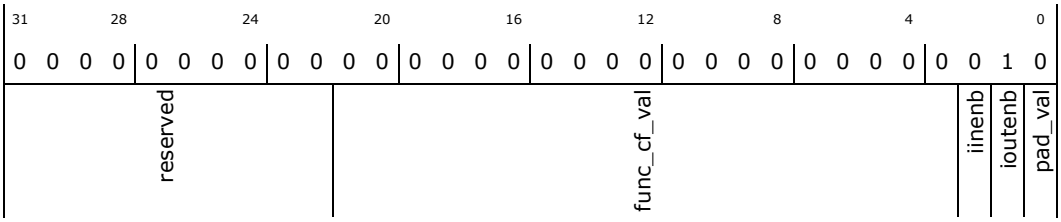
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk1_PAD_VAL: [IOBASE] + 578h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.265 Smb Clk Pad Configuration (cfio_regs_pad_smb_clk_PCONF0)—Offset 580h

PADs Memory space configuration register (access via PCU proxy)

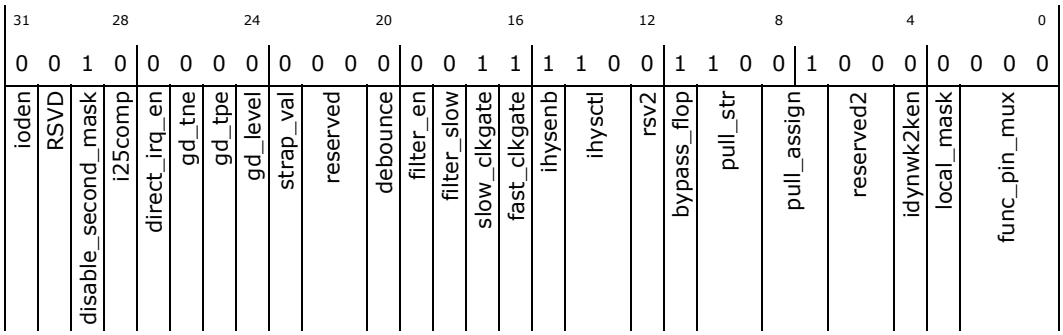
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_smb_clk_PCONF0: [IOBASE] + 580h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_52 function 1 is SMB_CLK

3.67.266 Smb Clk Delay Line Multiplexer (cfio_regs_pad_smb_clk_PCONF1)—Offset 584h

DLL Multiplexer

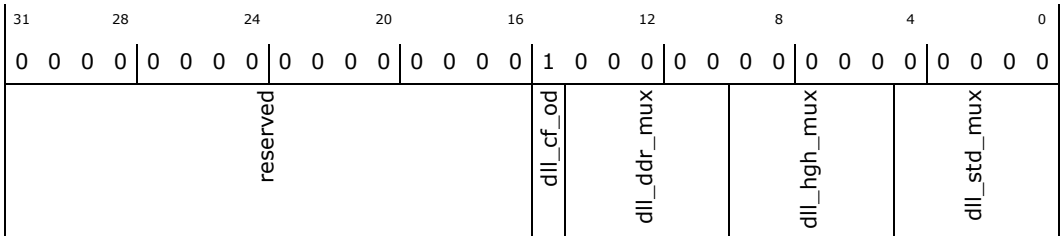
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_smb_clk_PCONF1: [IOBASE] + 584h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.267 Smb Clk Pad Value (cfio_regs_pad_smb_clk_PAD_VAL)—Offset 588h

PADs Memory space Value register (access via PCU proxy)

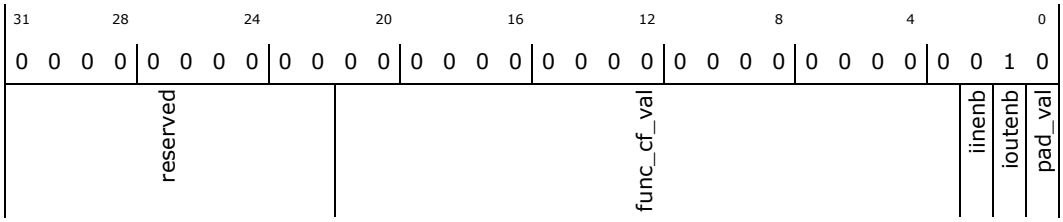
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_smb_clk_PAD_VAL: [IOBASE] + 588h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.268 Sata Gp1 Pad Configuration (cfio_regs_pad_sata_gp1_PCONF0)—Offset 590h

PADs Memory space configuration register (access via PCU proxy)

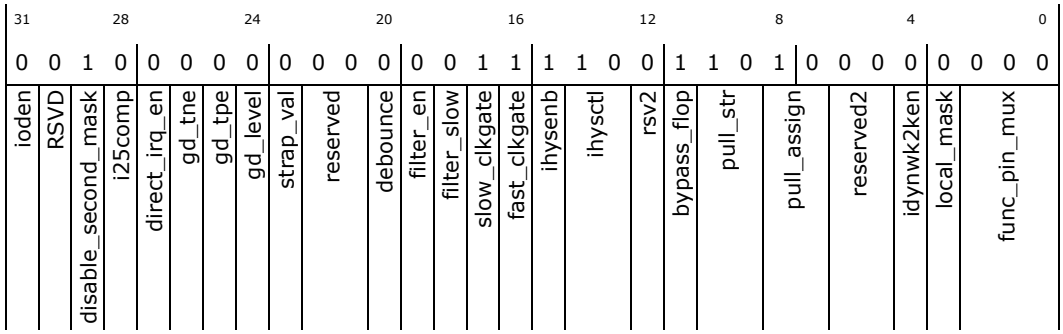
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sata_gp1_PCONF0: [IOBASE] + 590h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_1 function 1 is SATA_GP1 function 2 is SATA_DEVSLP0

3.67.269 Sata Gp1 Delay Line Multiplexer (cfio_regs_pad_sata_gp1_PCONF1)—Offset 594h

DLL Multiplexer

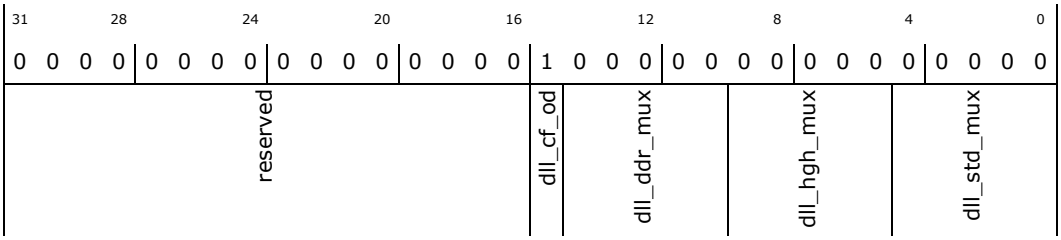
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sata_gp1_PCONF1: [IOBASE] + 594h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.270 Sata Gp1 Pad Value (cfio_regs_pad_sata_gp1_PAD_VAL)—Offset 598h

PADs Memory space Value register (access via PCU proxy)

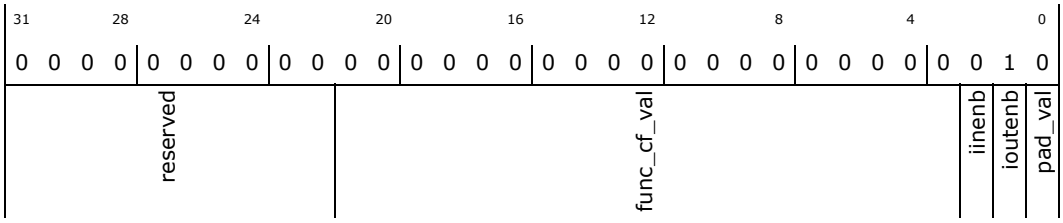
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sata_gp1_PAD_VAL: [IOBASE] + 598h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.271 Smb Data Pad Configuration (cfio_regs_pad_smb_data_PCONF0)—Offset 5A0h

PADs Memory space configuration register (access via PCU proxy)

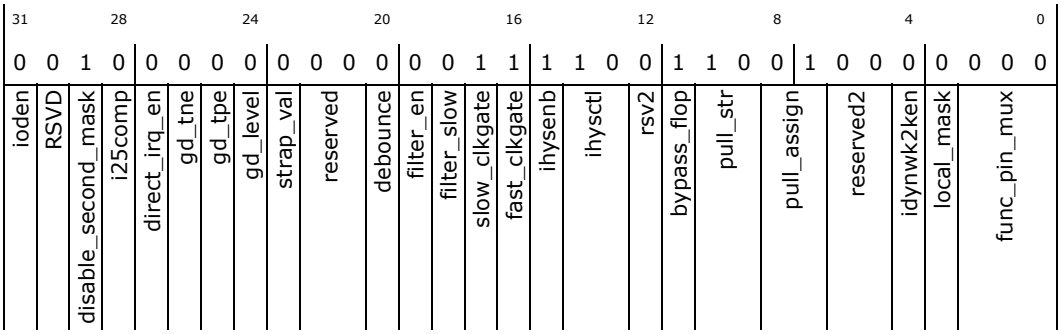
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_smb_data_PCONF0: [IOBASE] + 5A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_51 function 1 is SMB_DATA

3.67.272 Smb Data Delay Line Multiplexer (cfio_regs_pad_smb_data_PCONF1)—Offset 5A4h

DLL Multiplexer

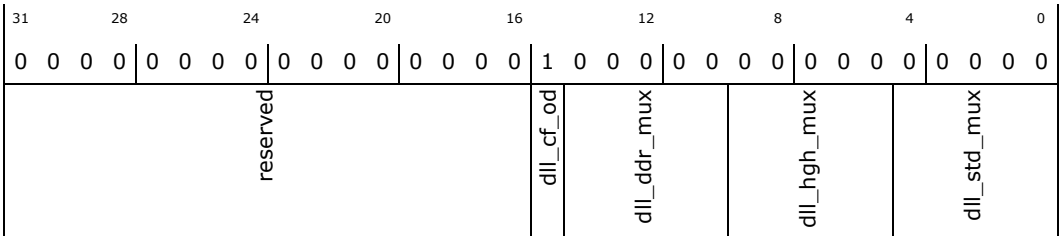
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_smb_data_PCONF1: [IOBASE] + 5A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.273 Smb Data Pad Value (cfio_regs_pad_smb_data_PAD_VAL)—Offset 5A8h

PADs Memory space Value register (access via PCU proxy)

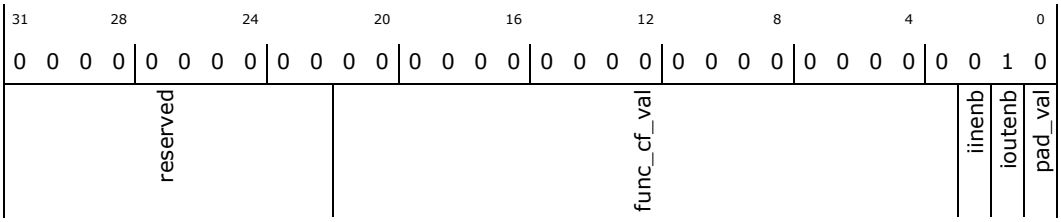
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_smb_data_PAD_VAL: [IOBASE] + 5A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.274 Plt Clk2 Pad Configuration (cfio_regs_pad_plt_clk2_PCONF0)—Offset 5B0h

PADs Memory space configuration register (access via PCU proxy)

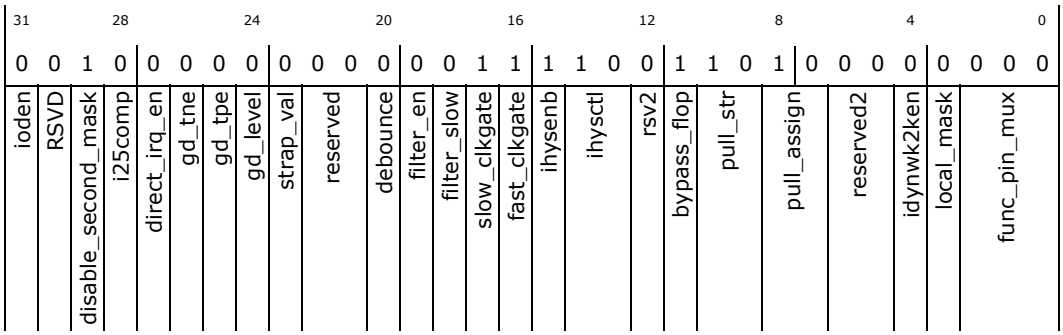
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk2_PCONF0: [IOBASE] + 5B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_98 function 1 is PLT_CLK2

3.67.275 Plt Clk2 Delay Line Multiplexer (cfio_regs_pad_plt_clk2_PCONF1)—Offset 5B4h

DLL Multiplexer

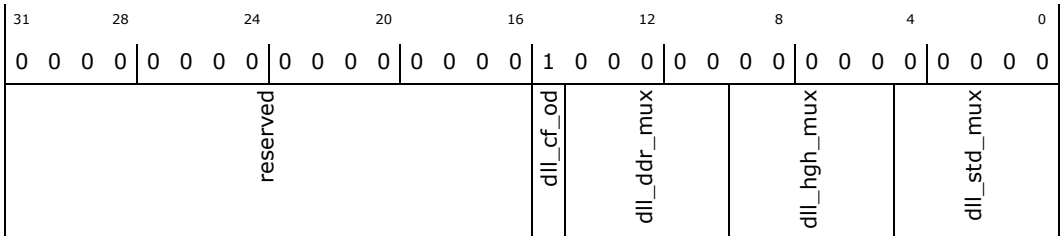
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk2_PCONF1: [IOBASE] + 5B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.276 Plt Clk2 Pad Value (cfio_regs_pad_plt_clk2_PAD_VAL)—Offset 5B8h

PADs Memory space Value register (access via PCU proxy)

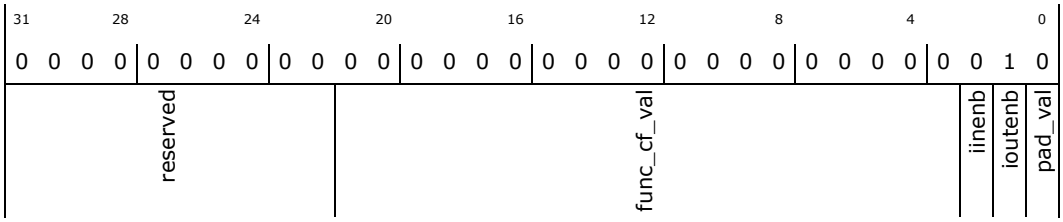
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk2_PAD_VAL: [IOBASE] + 5B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.277 Smb Alertb Pad Configuration (cfio_regs_pad_smb_alertb_PCONF0)—Offset 5C0h

PADs Memory space configuration register (access via PCU proxy)

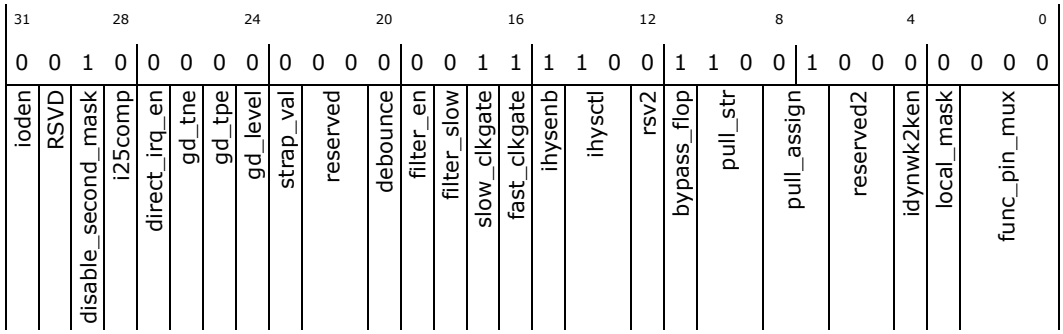
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_smb_alertb_PCONF0: [IOBASE] + 5C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_53 function 1 is SMB_ALERTB

3.67.278 Smb Alertb Delay Line Multiplexer (cfio_regs_pad_smb_alertb_PCONF1)—Offset 5C4h

DLL Multiplexer

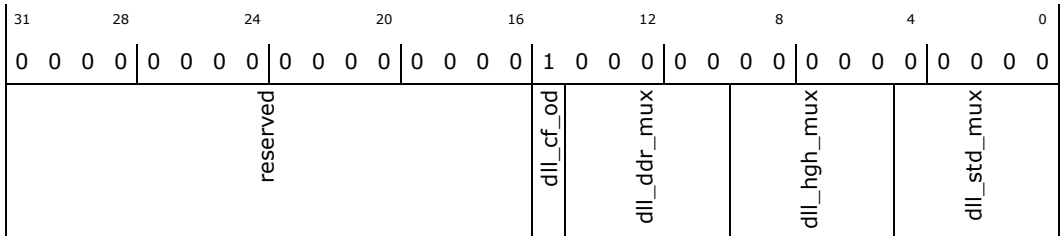
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_smb_alertb_PCONF1: [IOBASE] + 5C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.279 Smb Alertb Pad Value (cfio_regs_pad_smb_alertb_PAD_VAL)—Offset 5C8h

PADs Memory space Value register (access via PCU proxy)

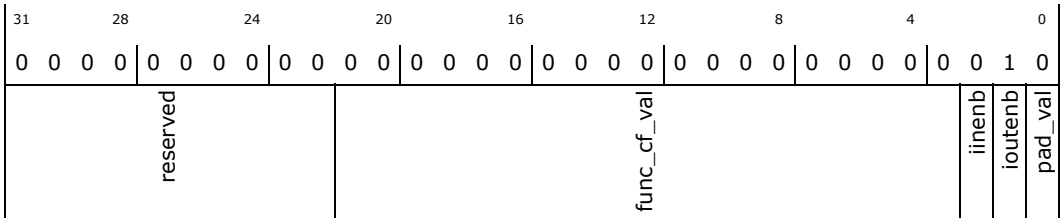
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_smb_alertb_PAD_VAL: [IOBASE] + 5C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.280 Sata Ledn Pad Configuration (cfio_regs_pad_sata_ledn_PCONF0)—Offset 5D0h

PADs Memory space configuration register (access via PCU proxy)

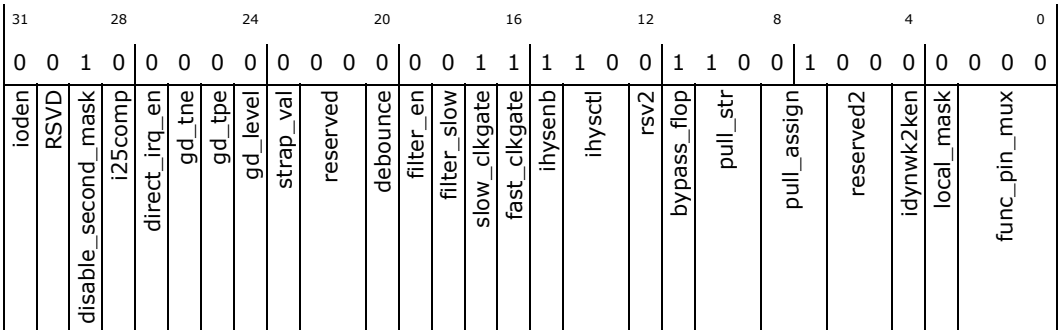
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sata_ledn_PCONF0: [IOBASE] + 5D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_2 function 1 is SATA_LEDN

3.67.281 Sata Ledn Delay Line Multiplexer (cfio_regs_pad_sata_ledn_PCONF1)—Offset 5D4h

DLL Multiplexer

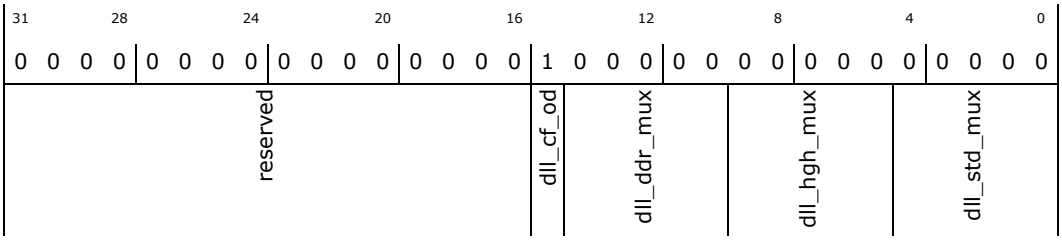
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sata_ledn_PCONF1: [IOBASE] + 5D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.282 Sata Ledn Pad Value (cfio_regs_pad_sata_ledn_PAD_VAL)—Offset 5D8h

PADs Memory space Value register (access via PCU proxy)

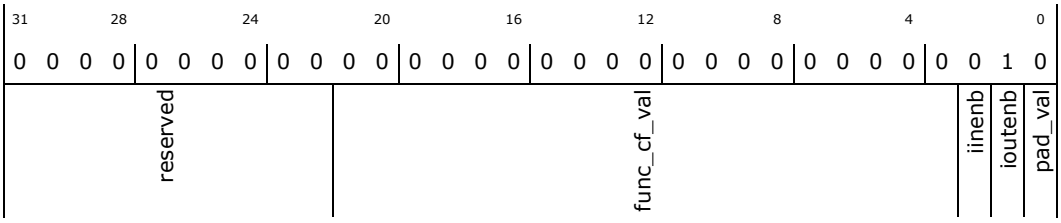
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sata_ledn_PAD_VAL: [IOBASE] + 5D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.283 Pmu Resetbutton B Pad Configuration (cfio_regs_pad_pmu_resetbutton_b_PCONF0)—Offset 5E0h

PADs Memory space configuration register (access via PCU proxy)

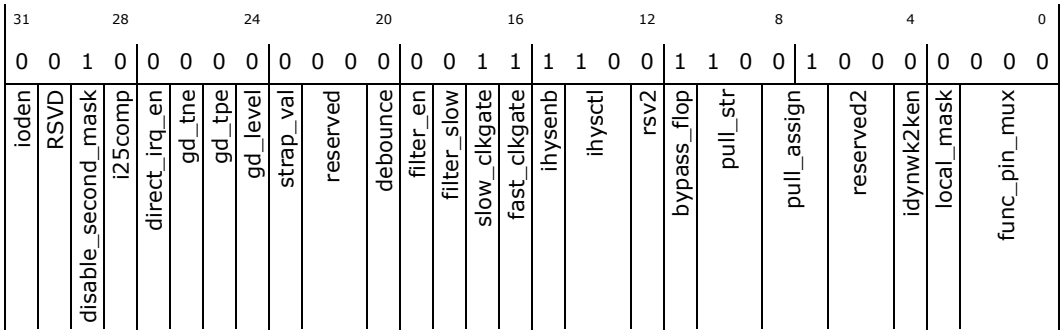
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_resetbutton_b_PCONF0: [IOBASE] + 5E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq

Bit Range	Default & Access	Description
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_RESETBUTTON_B

3.67.284 Pmu Resetbutton B Delay Line Multiplexer (cfio_regs_pad_pmu_resetbutton_b_PCONF1)—Offset 5E4h

DLL Multiplexer

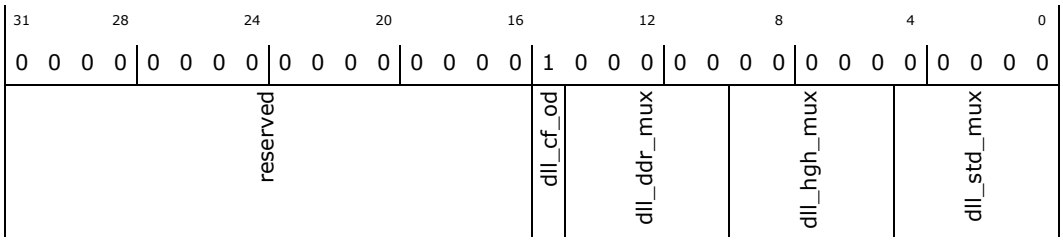
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_resetbutton_b_PCONF1: [IOBASE] + 5E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.285 Pmu Resetbutton B Pad Value (cfio_regs_pad_pmu_resetbutton_b_PAD_VAL)—Offset 5E8h

PADs Memory space Value register (access via PCU proxy)

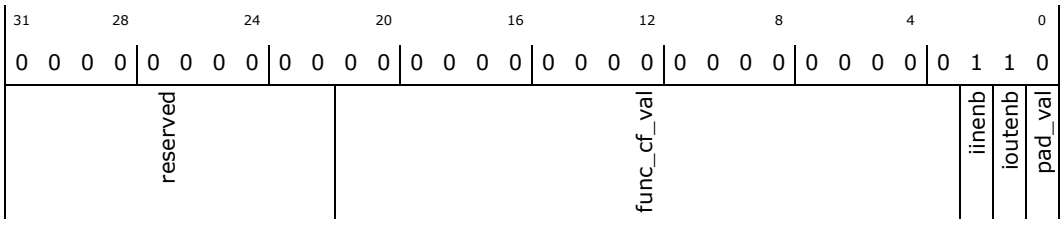
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_resetbutton_b_PAD_VAL: [IOBASE] + 5E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.286 Sdmmc3 1p8 En Pad Configuration (cfio_regs_pad_sdmmc3_1p8_en_PCONF0)—Offset 5F0h

PADs Memory space configuration register (access via PCU proxy)

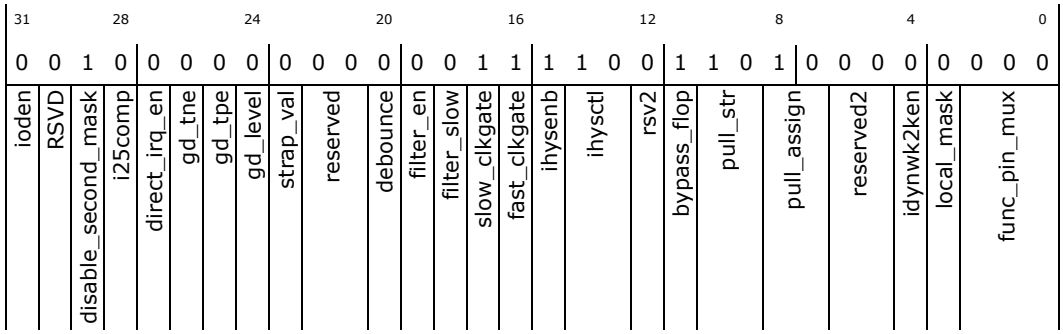
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_1p8_en_PCONF0: [IOBASE] + 5F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_40 function 1 is SDMMC3_1P8_EN

3.67.287 Sdmmc3 1p8 En Delay Line Multiplexer (cfio_regs_pad_sdmmc3_1p8_en_PCONF1)—Offset 5F4h

DLL Multiplexer

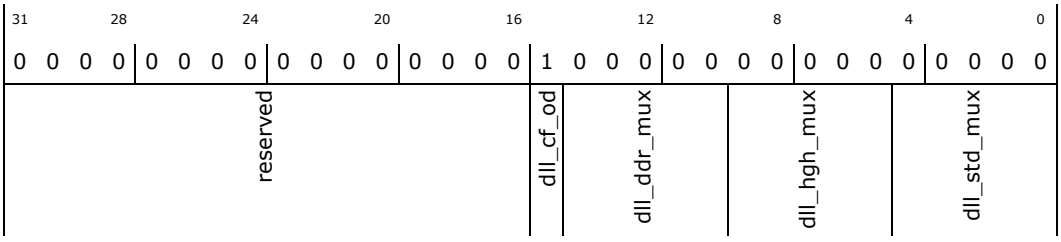
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_1p8_en_PCONF1: [IOBASE] + 5F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.288 Sdmmc3 1p8 En Pad Value (cfio_regs_pad_sdmmc3_1p8_en_PAD_VAL)—Offset 5F8h

PADs Memory space Value register (access via PCU proxy)

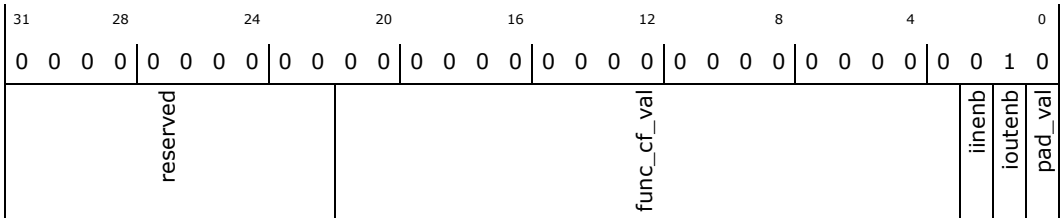
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_1p8_en_PAD_VAL: [IOBASE] + 5F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.289 Pcie Clkreq0b Pad Configuration (cfio_regs_pad_pcie_clkreq0b_PCONF0)—Offset 600h

PADs Memory space configuration register (access via PCU proxy)

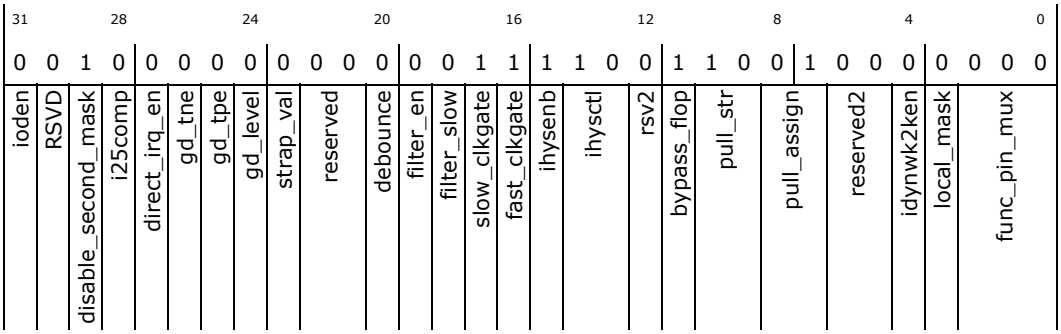
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq0b_PCONF0: [IOBASE] + 600h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_3 function 1 is PCIE_CLKREQ0B

3.67.290 Pcie Clkreq0b Delay Line Multiplexer (cfio_regs_pad_pcie_clkreq0b_PCONF1)—Offset 604h

DLL Multiplexer

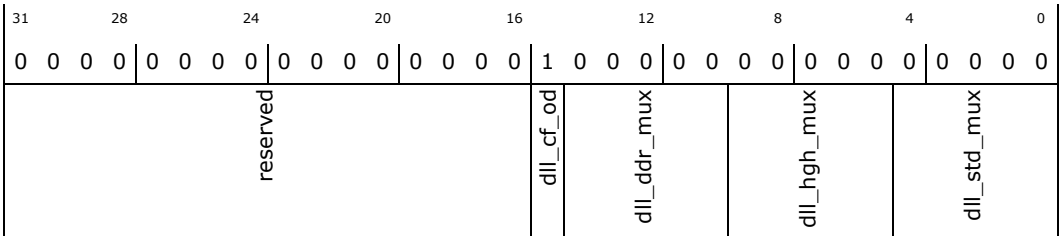
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq0b_PCONF1: [IOBASE] + 604h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.291 Pcie Clkreq0b Pad Value (cfio_regs_pad_pcie_clkreq0b_PAD_VAL)—Offset 608h

PADs Memory space Value register (access via PCU proxy)

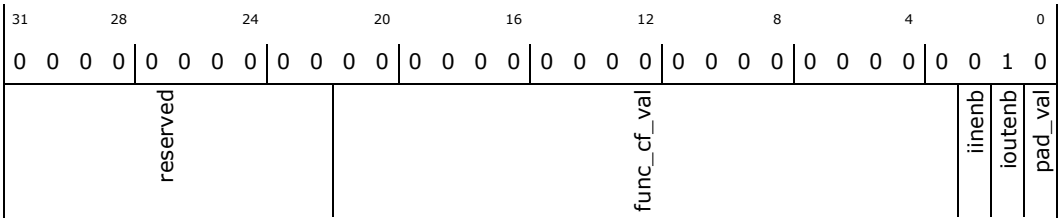
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq0b_PAD_VAL: [IOBASE] + 608h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.292 Plt Clk4 Pad Configuration (cfio_regs_pad_plt_clk4_PCONF0)—Offset 610h

PADs Memory space configuration register (access via PCU proxy)

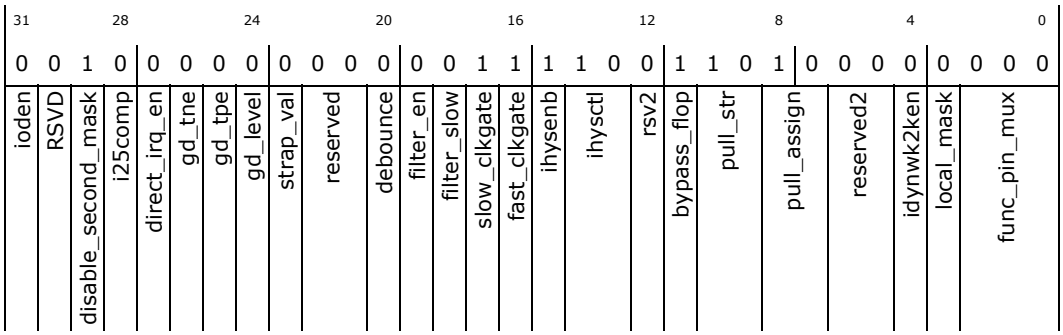
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk4_PCONF0: [IOBASE] + 610h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_100 function 1 is PLT_CLK4

3.67.293 Plt Clk4 Delay Line Multiplexer (cfio_regs_pad_plt_clk4_PCONF1)—Offset 614h

DLL Multiplexer

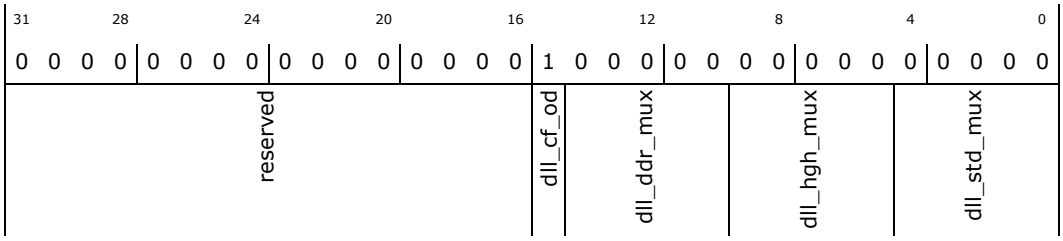
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk4_PCONF1: [IOBASE] + 614h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.294 Plt Clk4 Pad Value (cfio_regs_pad_plt_clk4_PAD_VAL)—Offset 618h

PADs Memory space Value register (access via PCU proxy)

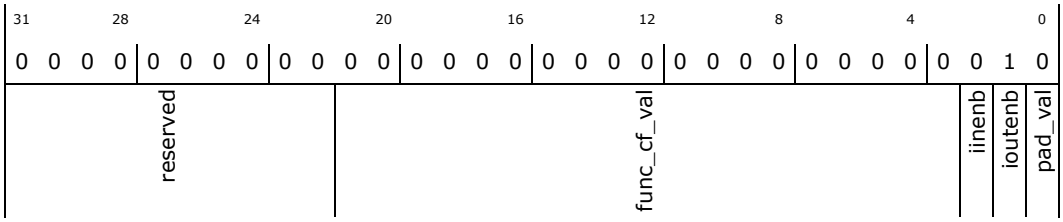
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk4_PAD_VAL: [IOBASE] + 618h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.295 Pcie Clkreq3b Pad Configuration (cfio_regs_pad_pcie_clkreq3b_PCONF0)—Offset 620h

PADs Memory space configuration register (access via PCU proxy)

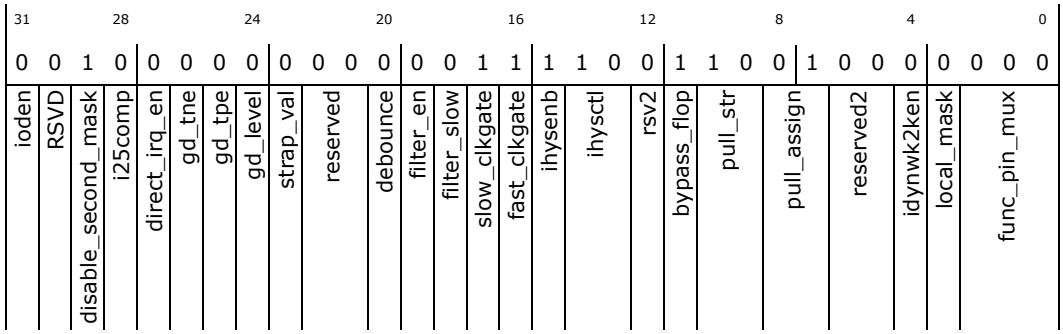
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq3b_PCONF0: [IOBASE] + 620h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_6 function 1 is PCIE_CLKREQ3B

3.67.296 Pcie Clkreq3b Delay Line Multiplexer (cfio_regs_pad_pcie_clkreq3b_PCONF1)—Offset 624h

DLL Multiplexer

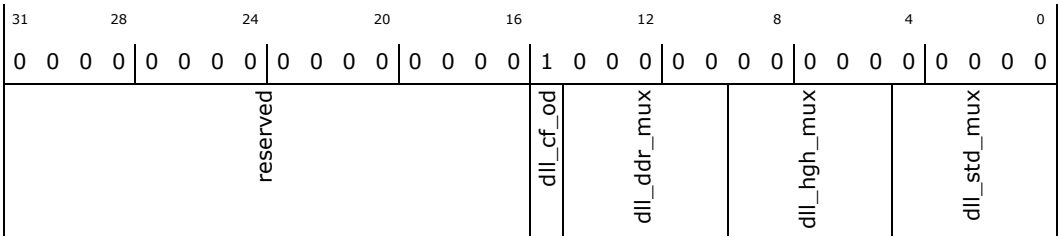
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq3b_PCONF1: [IOBASE] + 624h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.297 Pcie Clkreq3b Pad Value (cfio_regs_pad_pcie_clkreq3b_PAD_VAL)—Offset 628h

PADs Memory space Value register (access via PCU proxy)

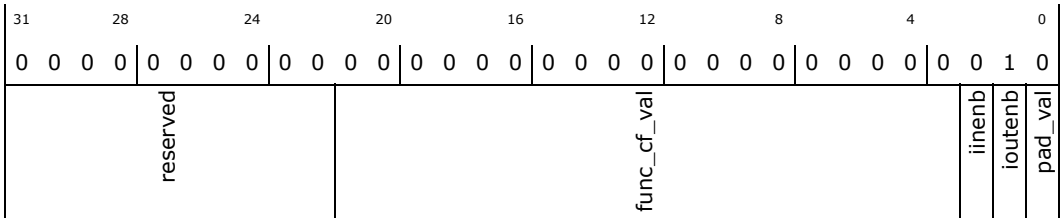
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq3b_PAD_VAL: [IOBASE] + 628h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.298 Pcie Clkreq1b Pad Configuration (cfio_regs_pad_pcie_clkreq1b_PCONF0)—Offset 630h

PADs Memory space configuration register (access via PCU proxy)

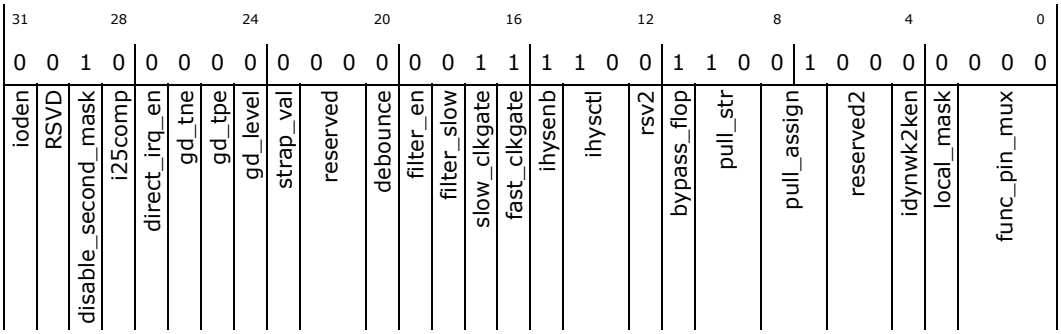
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq1b_PCONF0: [IOBASE] + 630h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_4 function 1 is PCIE_CLKREQ1B

3.67.299 Pcie Clkreq1b Delay Line Multiplexer (cfio_regs_pad_pcie_clkreq1b_PCONF1)—Offset 634h

DLL Multiplexer

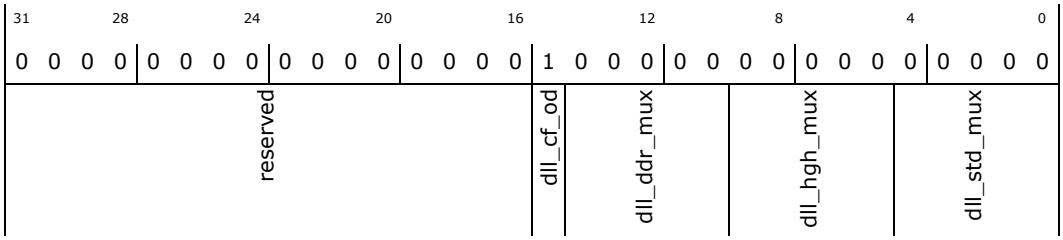
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq1b_PCONF1: [IOBASE] + 634h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.300 Pcie Clkreq1b Pad Value (cfio_regs_pad_pcie_clkreq1b_PAD_VAL)—Offset 638h

PADs Memory space Value register (access via PCU proxy)

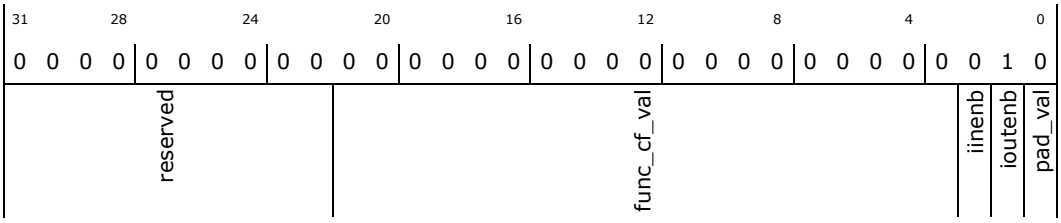
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq1b_PAD_VAL: [IOBASE] + 638h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.301 Plt Clk5 Pad Configuration (cfio_regs_pad_plt_clk5_PCONF0)—Offset 640h

PADs Memory space configuration register (access via PCU proxy)

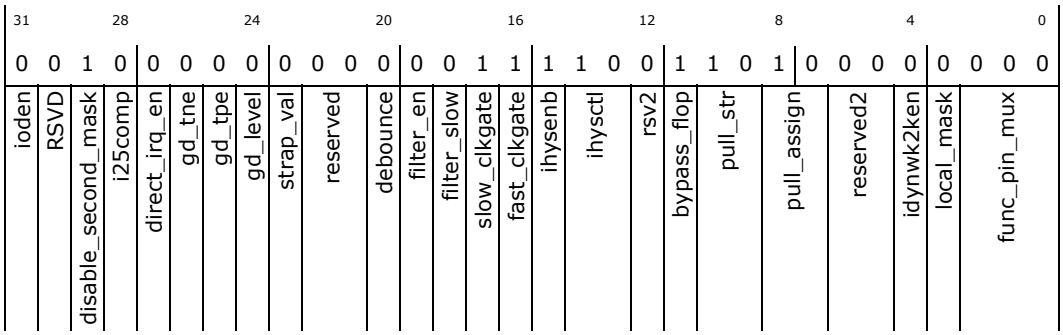
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk5_PCONF0: [IOBASE] + 640h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_101 function 1 is PLT_CLK5

3.67.302 Plt Clk5 Delay Line Multiplexer (cfio_regs_pad_plt_clk5_PCONF1)—Offset 644h

DLL Multiplexer

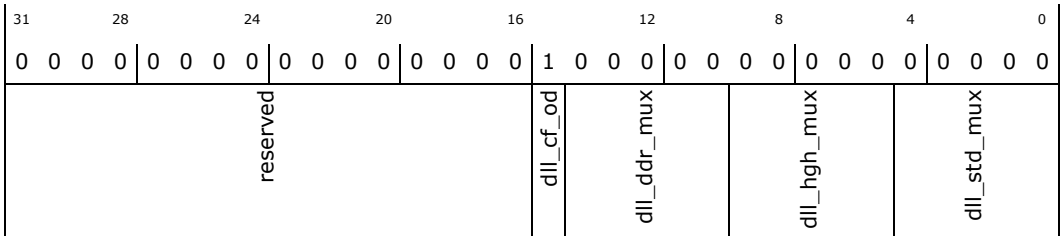
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk5_PCONF1: [IOBASE] + 644h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.303 Plt Clk5 Pad Value (cfio_regs_pad_plt_clk5_PAD_VAL)—Offset 648h

PADs Memory space Value register (access via PCU proxy)

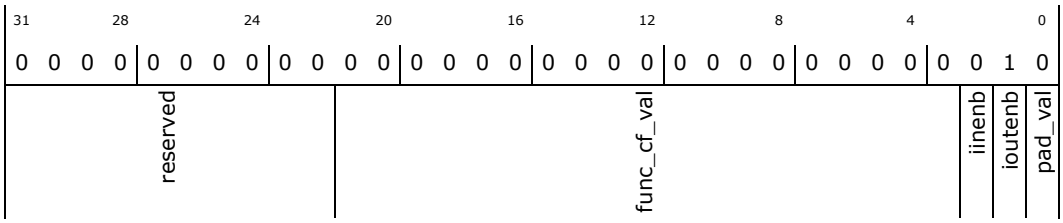
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk5_PAD_VAL: [IOBASE] + 648h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.304 Pcie Clkreq4b Pad Configuration (cfio_regs_pad_pcie_clkreq4b_PCONF0)—Offset 650h

PADs Memory space configuration register (access via PCU proxy)

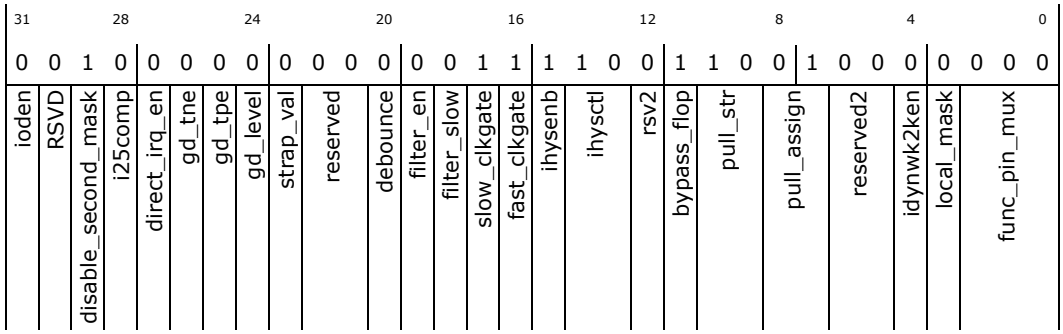
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq4b_PCONF0: [IOBASE] + 650h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_7 function 1 is PCIE_CLKREQ4B function 2 is SDMMC3_WP

3.67.305 Pcie Clkreq4b Delay Line Multiplexer (cfio_regs_pad_pcie_clkreq4b_PCONF1)—Offset 654h

DLL Multiplexer

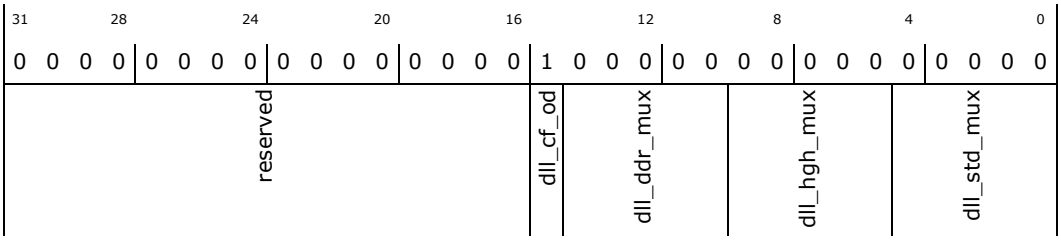
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq4b_PCONF1: [IOBASE] + 654h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.306 Pcie Clkreq4b Pad Value (cfio_regs_pad_pcie_clkreq4b_PAD_VAL)—Offset 658h

PADs Memory space Value register (access via PCU proxy)

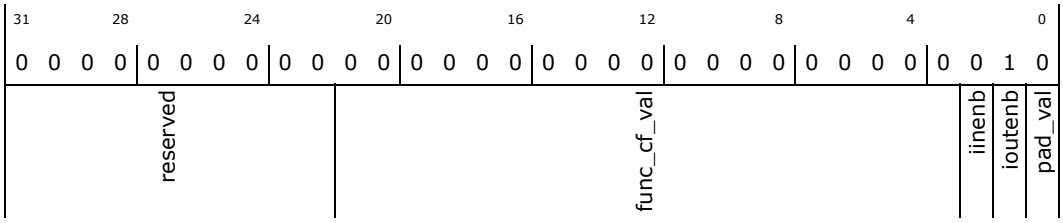
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq4b_PAD_VAL: [IOBASE] + 658h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.307 Pcie Clkreq2b Pad Configuration (cfio_regs_pad_pcie_clkreq2b_PCONF0)—Offset 660h

PADs Memory space configuration register (access via PCU proxy)

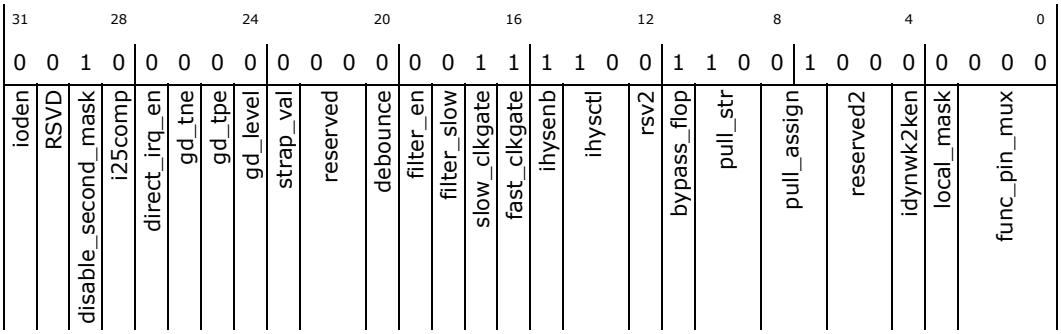
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq2b_PCONF0: [IOBASE] + 660h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_5 function 1 is PCIE_CLKREQ2B

3.67.308 Pcie Clkreq2b Delay Line Multiplexer (cfio_regs_pad_pcie_clkreq2b_PCONF1)—Offset 664h

DLL Multiplexer

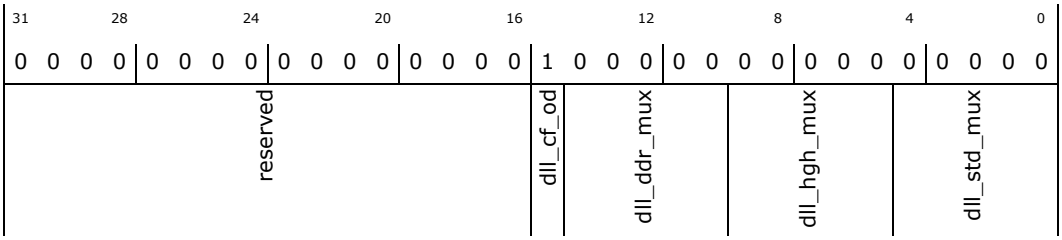
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq2b_PCONF1: [IOBASE] + 664h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.309 Pcie Clkreq2b Pad Value (cfio_regs_pad_pcie_clkreq2b_PAD_VAL)—Offset 668h

PADs Memory space Value register (access via PCU proxy)

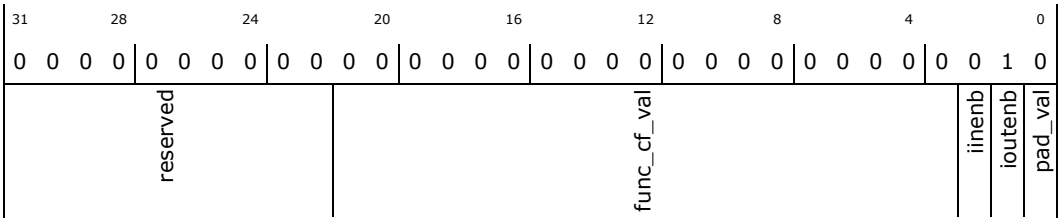
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pcie_clkreq2b_PAD_VAL: [IOBASE] + 668h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.310 Spkr Pad Configuration (cfio_regs_pad_spkr_PCONF0)—Offset 670h

PADs Memory space configuration register (access via PCU proxy)

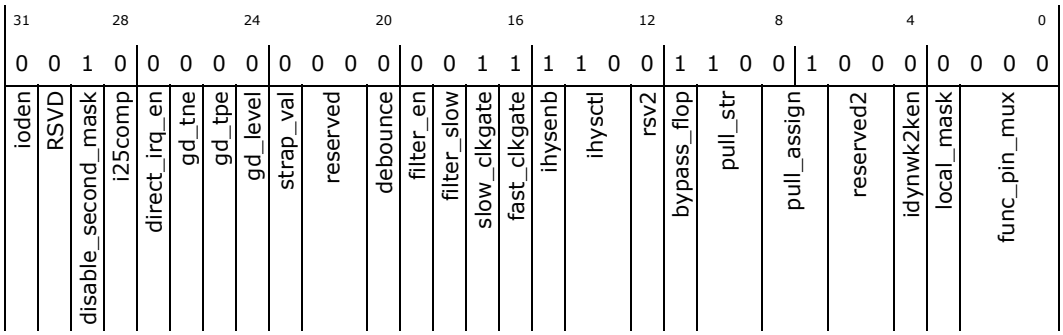
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spkr_PCONF0: [IOBASE] + 670h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_54 function 1 is SPKR function 2 is DLL_REFCLK For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10 function 3 is DLL_UPDN

3.67.311 Spkr Delay Line Multiplexer (cfio_regs_pad_spkr_PCONF1)—Offset 674h

DLL Multiplexer

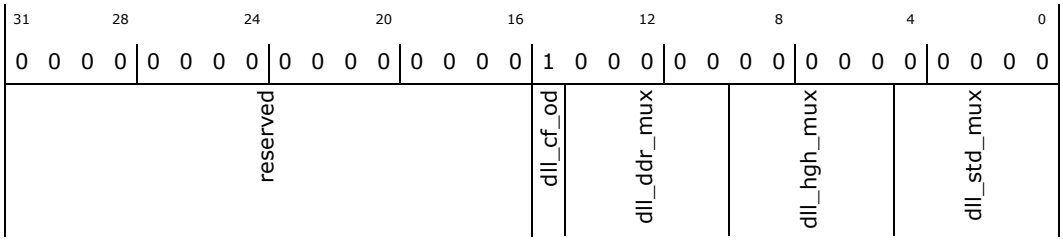
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spkr_PCONF1: [IOBASE] + 674h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.312 Spkr Pad Value (cfio_regs_pad_spkr_PAD_VAL)—Offset 678h

PADs Memory space Value register (access via PCU proxy)

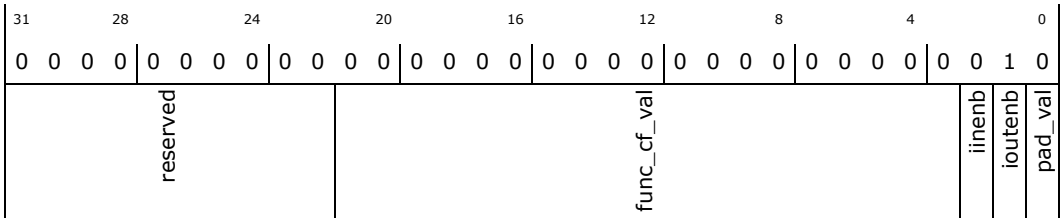
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spkr_PAD_VAL: [IOBASE] + 678h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.313 Plt Clk3 Pad Configuration (cfio_regs_pad_plt_clk3_PCONF0)—Offset 680h

PADs Memory space configuration register (access via PCU proxy)

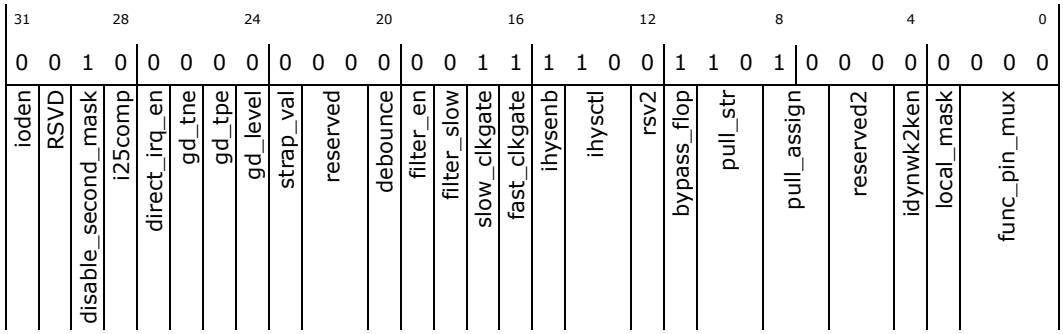
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk3_PCONF0: [IOBASE] + 680h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_99 function 1 is PLT_CLK3

3.67.314 Plt Clk3 Delay Line Multiplexer (cfio_regs_pad_plt_clk3_PCONF1)—Offset 684h

DLL Multiplexer

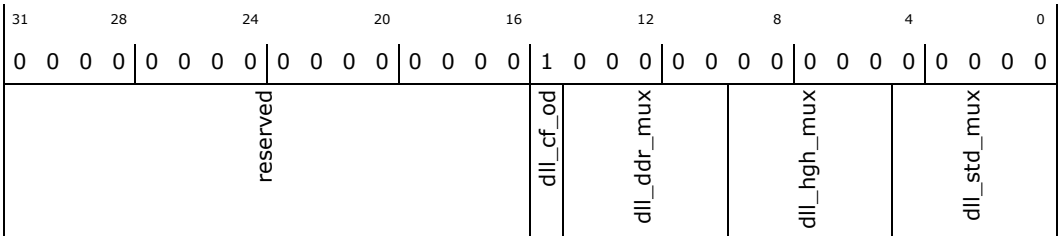
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk3_PCONF1: [IOBASE] + 684h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.315 Plt Clk3 Pad Value (cfio_regs_pad_plt_clk3_PAD_VAL)—Offset 688h

PADs Memory space Value register (access via PCU proxy)

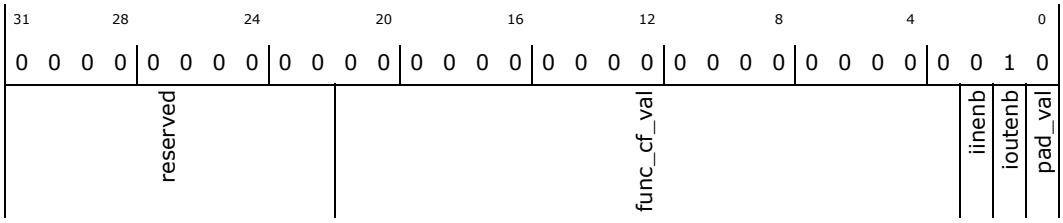
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk3_PAD_VAL: [IOBASE] + 688h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.316 Sdmmc3 Pwr En B Pad Configuration (cfio_regs_pad_sdmmc3_pwr_en_b_PCONF0)—Offset 690h

PADs Memory space configuration register (access via PCU proxy)

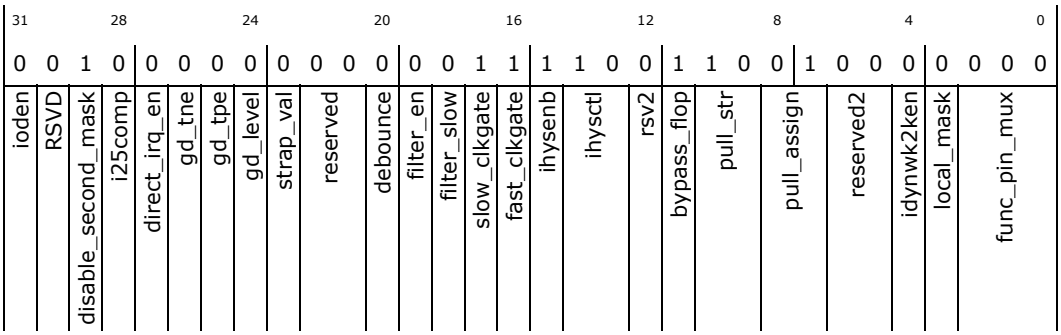
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_pwr_en_b_PCONF0: [IOBASE] + 690h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad

Bit Range	Default & Access	Description
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_41 function 1 is SDMMC3_PWR_EN_B

3.67.317 Sdmmc3 Pwr En B Delay Line Multiplexer (cfio_regs_pad_sdmmc3_pwr_en_b_PCONF1)—Offset 694h

DLL Multiplexer

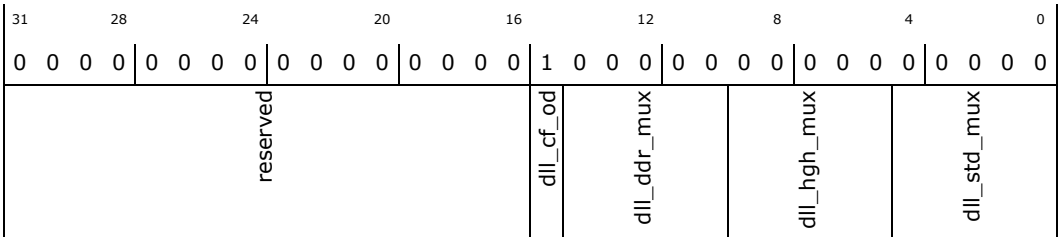
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_pwr_en_b_PCONF1: [IOBASE] + 694h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.318 Sdmmc3 Pwr En B Pad Value (cfio_regs_pad_sdmmc3_pwr_en_b_PAD_VAL)—Offset 698h

PADs Memory space Value register (access via PCU proxy)

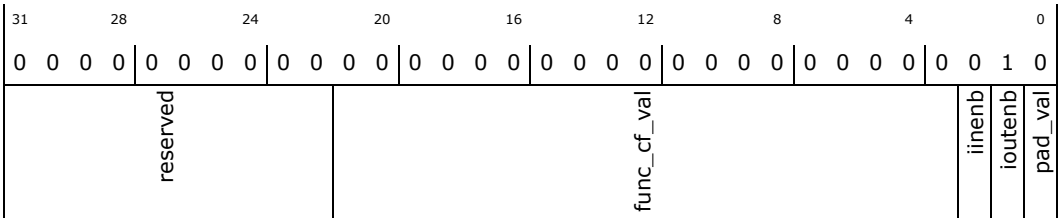
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sdmmc3_pwr_en_b_PAD_VAL: [IOBASE] + 698h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.319 Plt Clk0 Pad Configuration (cfio_regs_pad_plt_clk0_PCONF0)—Offset 6A0h

PADs Memory space configuration register (access via PCU proxy)

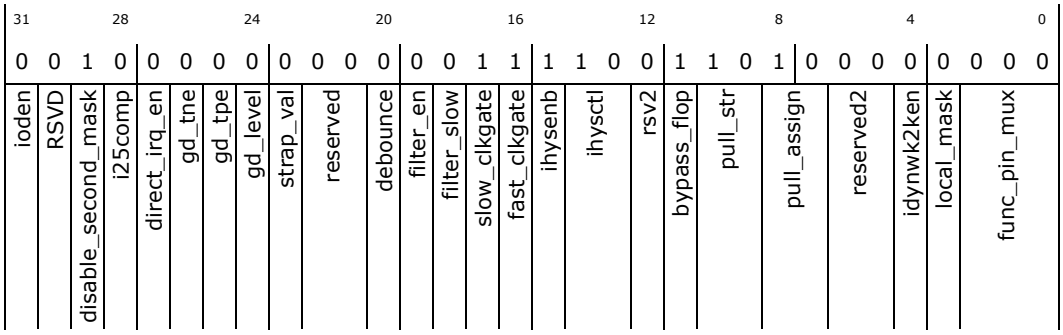
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk0_PCONF0: [IOBASE] + 6A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOC_96 function 1 is PLT_CLK0

3.67.320 Plt Clk0 Delay Line Multiplexer (cfio_regs_pad_plt_clk0_PCONF1)—Offset 6A4h

DLL Multiplexer

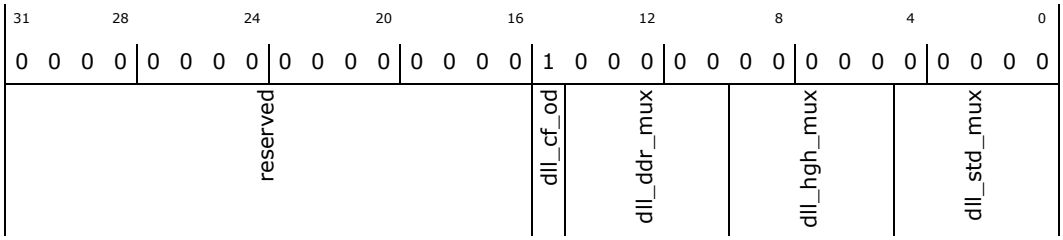
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk0_PCONF1: [IOBASE] + 6A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.321 Plt Clk0 Pad Value (cfio_regs_pad_plt_clk0_PAD_VAL)—Offset 6A8h

PADs Memory space Value register (access via PCU proxy)

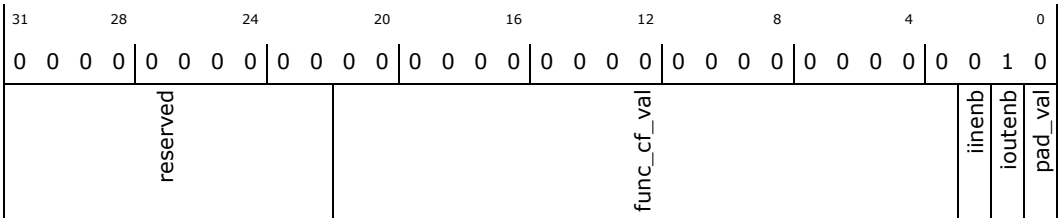
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_plt_clk0_PAD_VAL: [IOBASE] + 6A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.322 Vgpio 0 Pad Configuration (cfio_regs_pad_vgpio_0_PCONF0)—Offset 6B0h

PADs Memory space configuration register (access via PCU proxy)

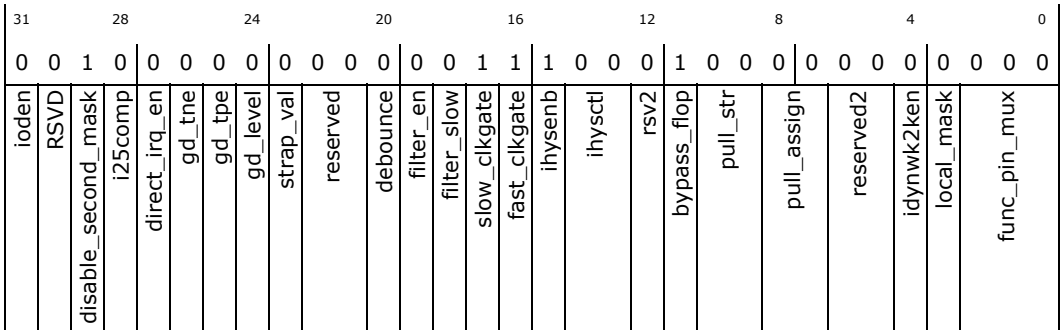
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_0_PCONF0: [IOBASE] + 6B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.323 Vgpio 0 Delay Line Multiplexer (cfio_regs_pad_vgpio_0_PCONF1)—Offset 6B4h

DLL Multiplexer

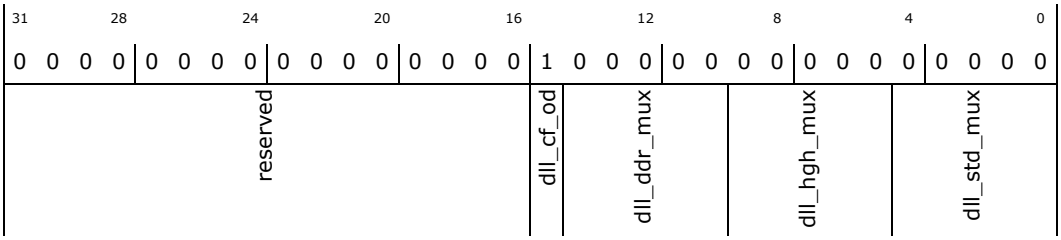
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_0_PCONF1: [IOBASE] + 6B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.324 Vgpio 0 Pad Value (cfio_regs_pad_vgpio_0_PAD_VAL)—Offset 6B8h

PADs Memory space Value register (access via PCU proxy)

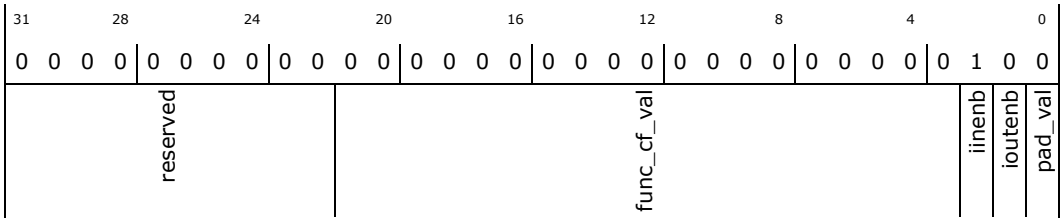
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_0_PAD_VAL: [IOBASE] + 6B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.325 Vgpio 1 Pad Configuration (cfio_regs_pad_vgpio_1_PCONF0)—Offset 6C0h

PADs Memory space configuration register (access via PCU proxy)

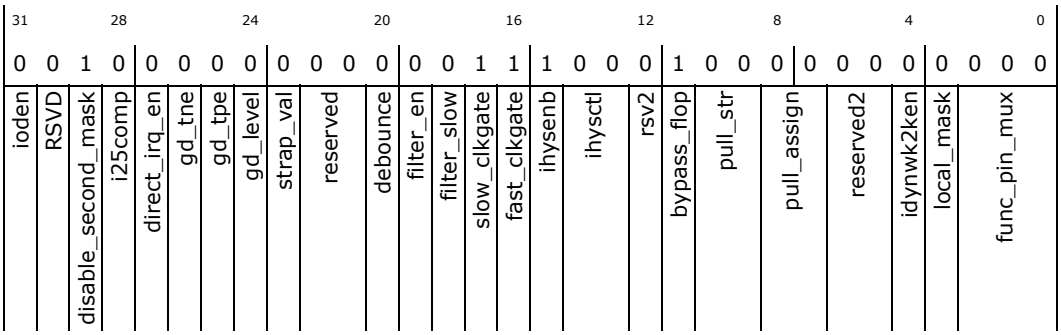
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_1_PCONF0: [IOBASE] + 6C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.326 Vgpio 1 Delay Line Multiplexer (cfio_regs_pad_vgpio_1_PCONF1)—Offset 6C4h

DLL Multiplexer

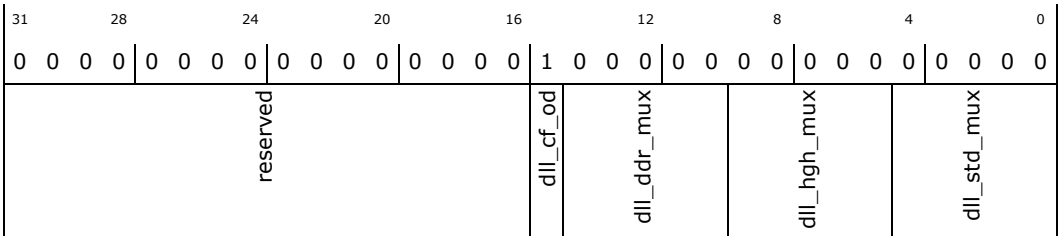
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_1_PCONF1: [IOBASE] + 6C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.327 Vgpio 1 Pad Value (cfio_regs_pad_vgpio_1_PAD_VAL)—Offset 6C8h

PADs Memory space Value register (access via PCU proxy)

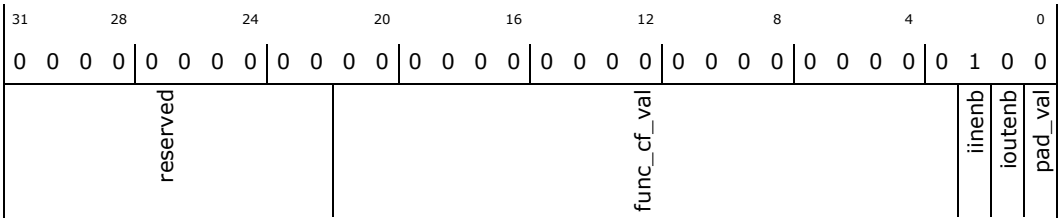
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_1_PAD_VAL: [IOBASE] + 6C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.328 Vgpio 2 Pad Configuration (cfio_regs_pad_vgpio_2_PCONF0)—Offset 6D0h

PADs Memory space configuration register (access via PCU proxy)

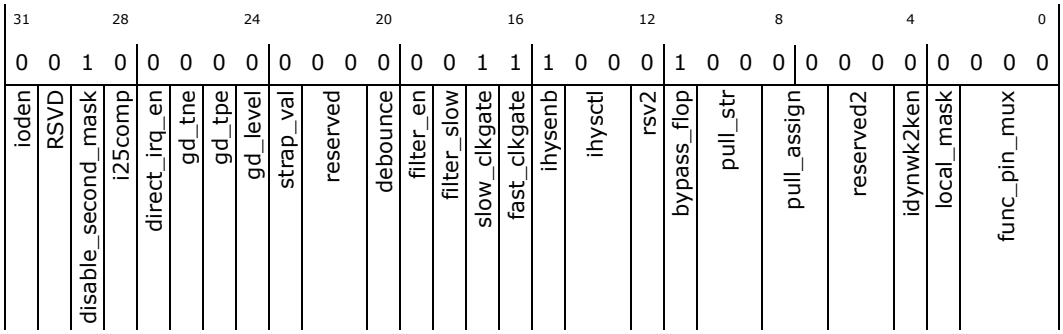
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_2_PCONF0: [IOBASE] + 6D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.329 Vgpio 2 Delay Line Multiplexer (cfio_regs_pad_vgpio_2_PCONF1)—Offset 6D4h

DLL Multiplexer

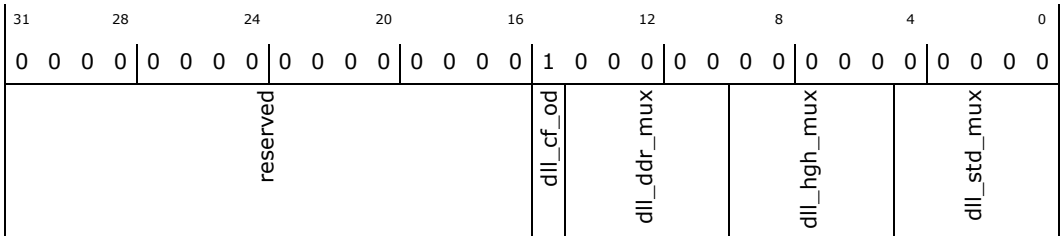
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_2_PCONF1: [IOBASE] + 6D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.330 Vgpio 2 Pad Value (cfio_regs_pad_vgpio_2_PAD_VAL)—Offset 6D8h

PADs Memory space Value register (access via PCU proxy)

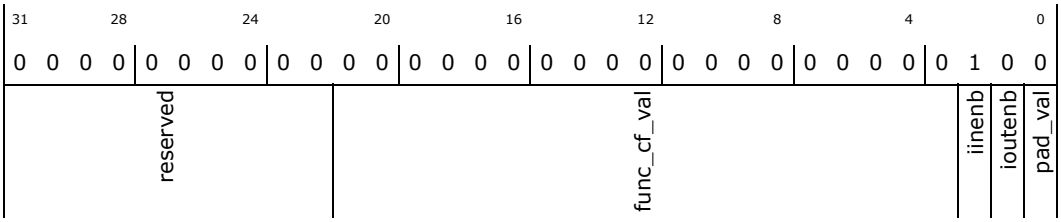
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_2_PAD_VAL: [IOBASE] + 6D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.331 Vgpio 3 Pad Configuration (cfio_regs_pad_vgpio_3_PCONF0)—Offset 6E0h

PADs Memory space configuration register (access via PCU proxy)

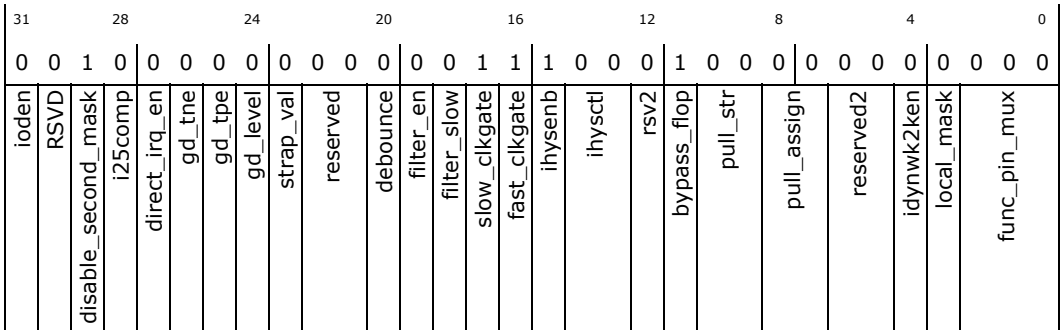
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_3_PCONF0: [IOBASE] + 6E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.332 Vgpio 3 Delay Line Multiplexer (cfio_regs_pad_vgpio_3_PCONF1)—Offset 6E4h

DLL Multiplexer

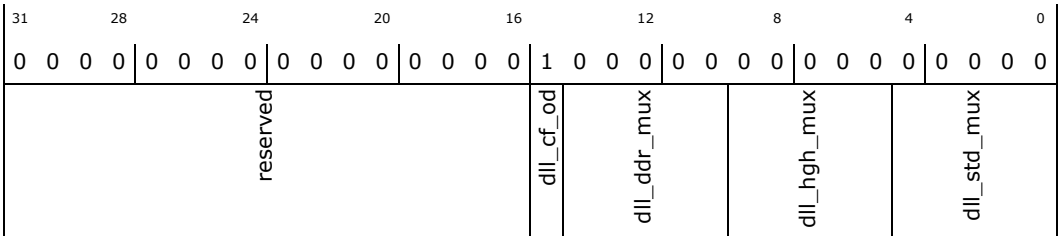
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_3_PCONF1: [IOBASE] + 6E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.333 Vgpio 3 Pad Value (cfio_regs_pad_vgpio_3_PAD_VAL)—Offset 6E8h

PADs Memory space Value register (access via PCU proxy)

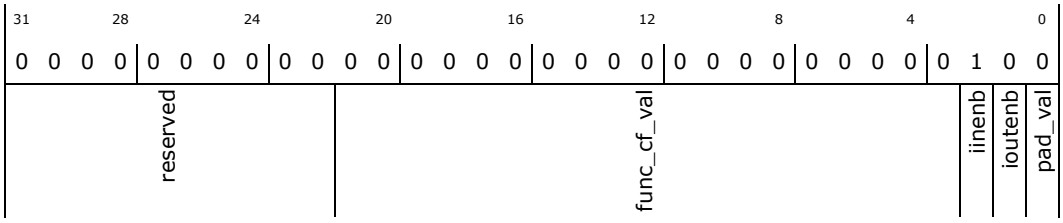
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_3_PAD_VAL: [IOBASE] + 6E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.334 Vgpio 4 Pad Configuration (cfio_regs_pad_vgpio_4_PCONF0)—Offset 6F0h

PADs Memory space configuration register (access via PCU proxy)

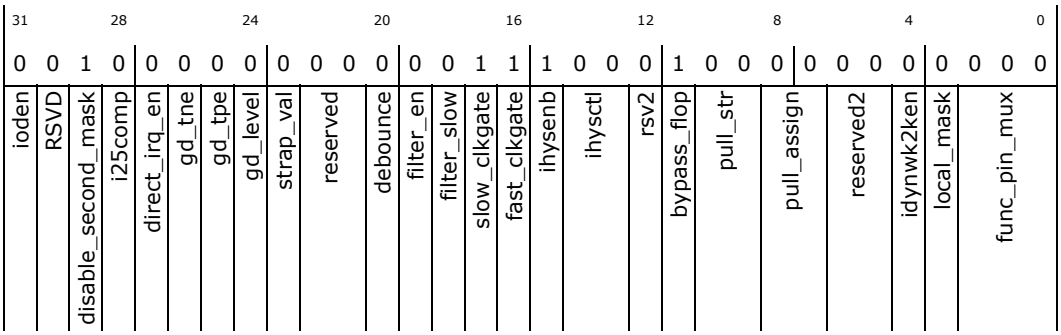
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_4_PCONF0: [IOBASE] + 6F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.335 Vgpio 4 Delay Line Multiplexer (cfio_regs_pad_vgpio_4_PCONF1)—Offset 6F4h

DLL Multiplexer

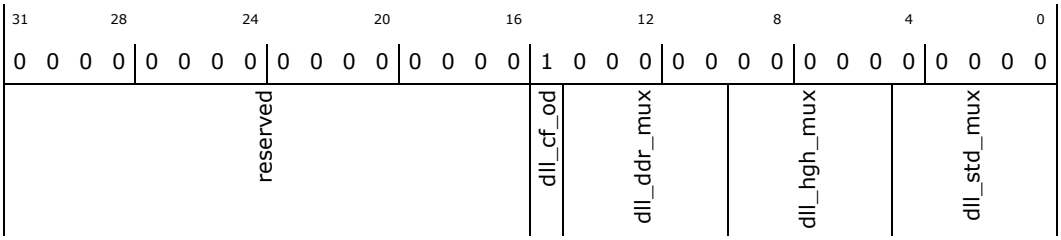
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_4_PCONF1: [IOBASE] + 6F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.336 Vgpio 4 Pad Value (cfio_regs_pad_vgpio_4_PAD_VAL)—Offset 6F8h

PADs Memory space Value register (access via PCU proxy)

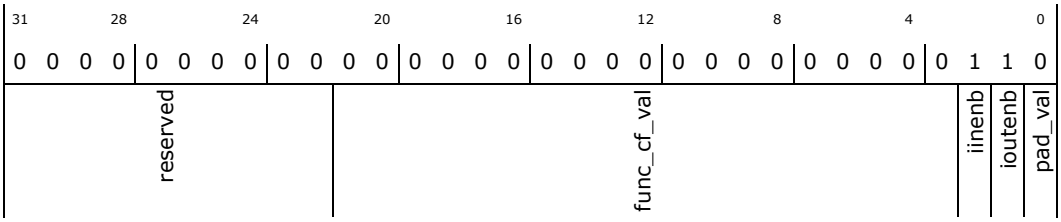
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_4_PAD_VAL: [IOBASE] + 6F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.337 Vgpio 5 Pad Configuration (cfio_regs_pad_vgpio_5_PCONF0)—Offset 700h

PADs Memory space configuration register (access via PCU proxy)

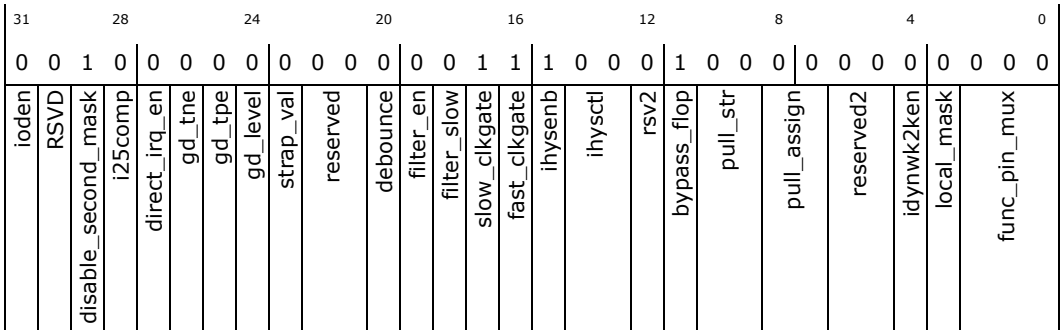
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_5_PCONF0: [IOBASE] + 700h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.338 Vgpio 5 Delay Line Multiplexer (cfio_regs_pad_vgpio_5_PCONF1)—Offset 704h

DLL Multiplexer

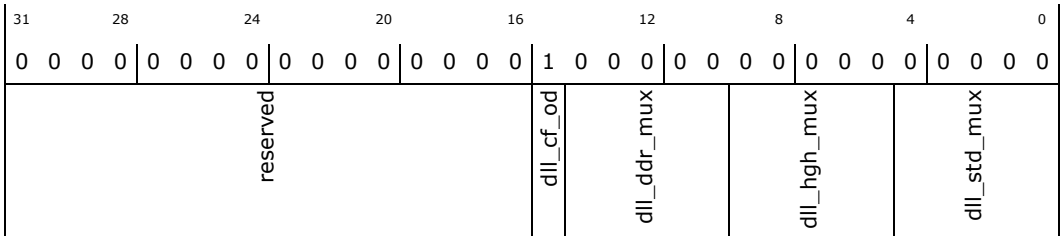
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_5_PCONF1: [IOBASE] + 704h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.339 Vgpio 5 Pad Value (cfio_regs_pad_vgpio_5_PAD_VAL)—Offset 708h

PADs Memory space Value register (access via PCU proxy)

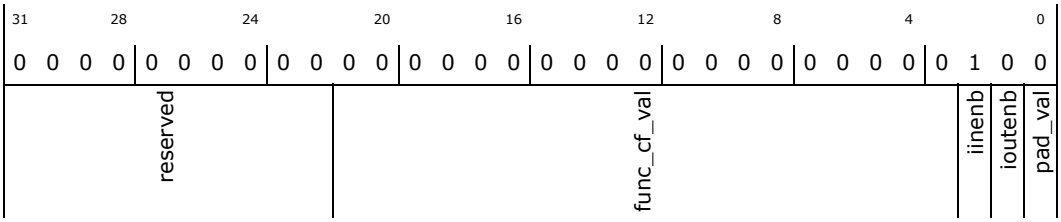
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_5_PAD_VAL: [IOBASE] + 708h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.340 Vgpio 6 Pad Configuration (cfio_regs_pad_vgpio_6_PCONF0)—Offset 710h

PADs Memory space configuration register (access via PCU proxy)

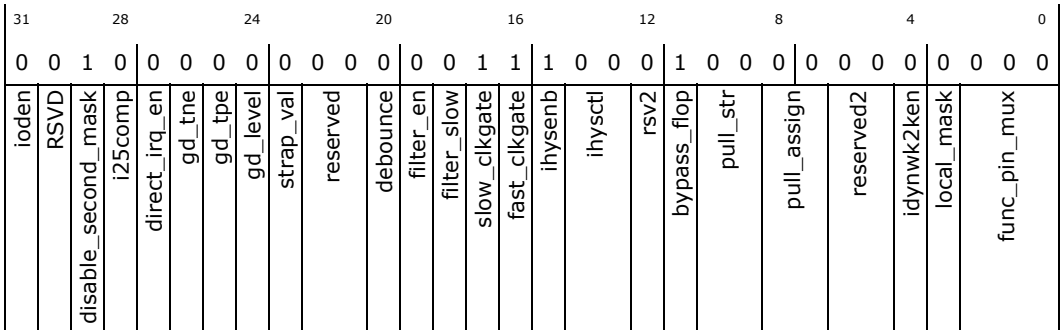
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_6_PCONF0: [IOBASE] + 710h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.341 Vgpio 6 Delay Line Multiplexer (cfio_regs_pad_vgpio_6_PCONF1)—Offset 714h

DLL Multiplexer

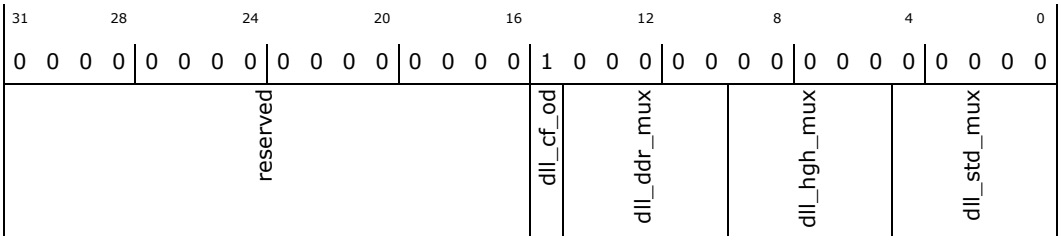
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_6_PCONF1: [IOBASE] + 714h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.342 Vgpio 6 Pad Value (cfio_regs_pad_vgpio_6_PAD_VAL)—Offset 718h

PADs Memory space Value register (access via PCU proxy)

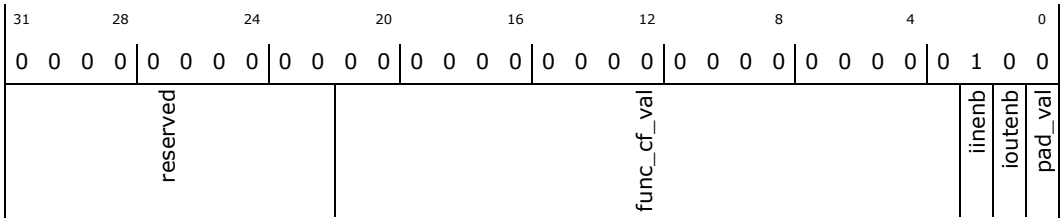
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_6_PAD_VAL: [IOBASE] + 718h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.343 Vgpio 7 Pad Configuration (cfio_regs_pad_vgpio_7_PCONF0)—Offset 720h

PADs Memory space configuration register (access via PCU proxy)

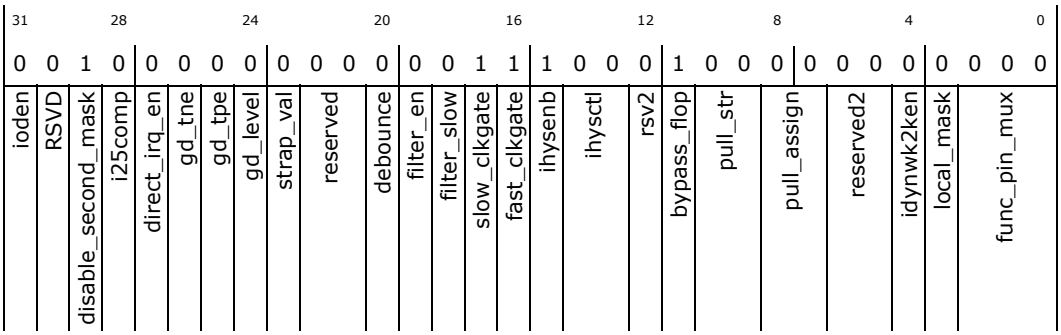
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_7_PCONF0: [IOBASE] + 720h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.344 Vgpio 7 Delay Line Multiplexer (cfio_regs_pad_vgpio_7_PCONF1)—Offset 724h

DLL Multiplexer

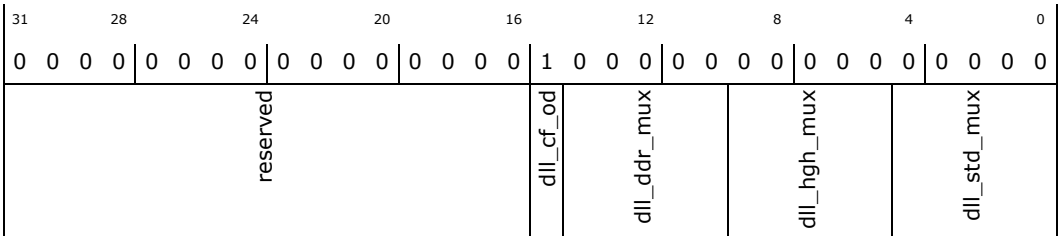
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_7_PCONF1: [IOBASE] + 724h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.345 Vgpio 7 Pad Value (cfio_regs_pad_vgpio_7_PAD_VAL)—Offset 728h

PADs Memory space Value register (access via PCU proxy)

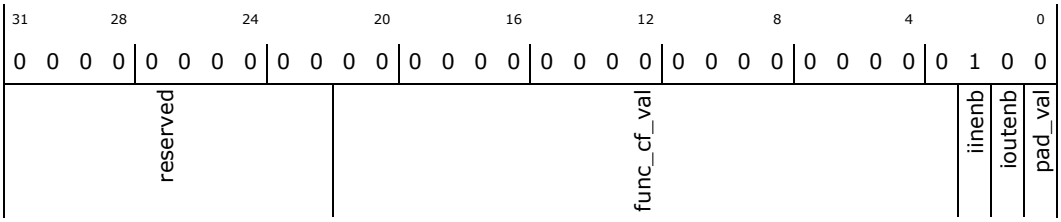
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_7_PAD_VAL: [IOBASE] + 728h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.346 Vgpio 8 Pad Configuration (cfio_regs_pad_vgpio_8_PCONF0)—Offset 730h

PADs Memory space configuration register (access via PCU proxy)

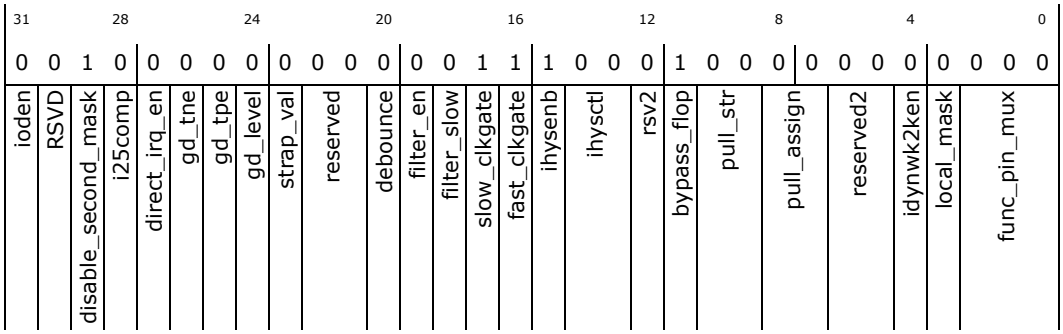
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_8_PCONF0: [IOBASE] + 730h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.347 Vgpio 8 Delay Line Multiplexer (cfio_regs_pad_vgpio_8_PCONF1)—Offset 734h

DLL Multiplexer

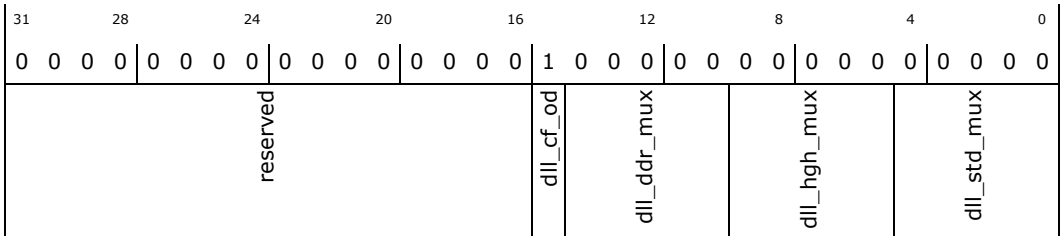
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_8_PCONF1: [IOBASE] + 734h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.348 Vgpio 8 Pad Value (cfio_regs_pad_vgpio_8_PAD_VAL)—Offset 738h

PADs Memory space Value register (access via PCU proxy)

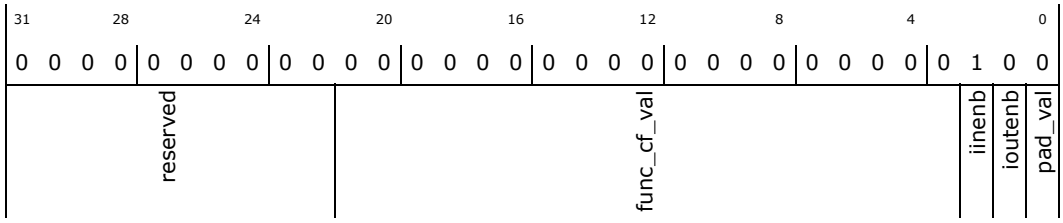
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_8_PAD_VAL: [IOBASE] + 738h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.349 Vgpio 9 Pad Configuration (cfio_regs_pad_vgpio_9_PCONF0)—Offset 740h

PADs Memory space configuration register (access via PCU proxy)

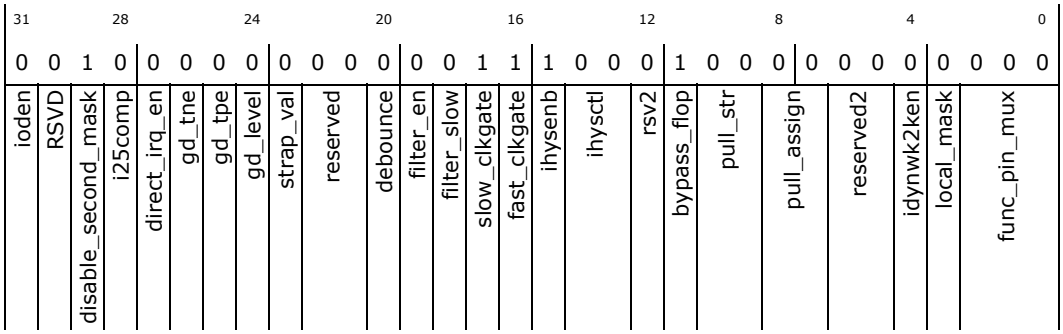
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_9_PCONF0: [IOBASE] + 740h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.350 Vgpio 9 Delay Line Multiplexer (cfio_regs_pad_vgpio_9_PCONF1)—Offset 744h

DLL Multiplexer

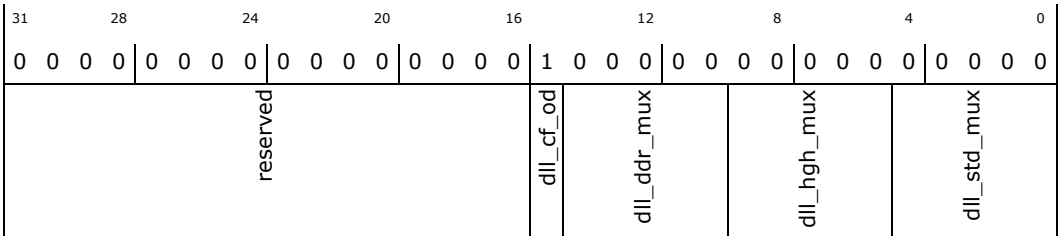
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_9_PCONF1: [IOBASE] + 744h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.351 Vgpio 9 Pad Value (cfio_regs_pad_vgpio_9_PAD_VAL)—Offset 748h

PADs Memory space Value register (access via PCU proxy)

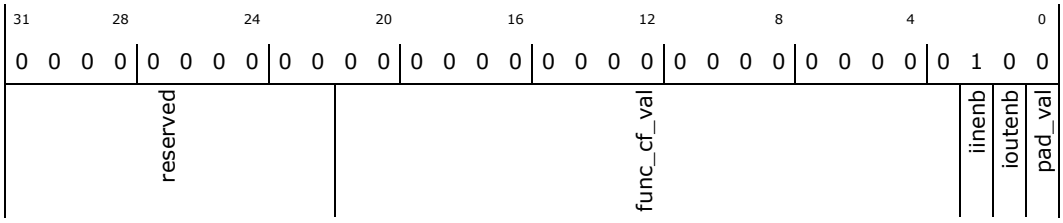
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_9_PAD_VAL: [IOBASE] + 748h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.352 Vgpio 10 Pad Configuration (cfio_regs_pad_vgpio_10_PCONF0)—Offset 750h

PADs Memory space configuration register (access via PCU proxy)

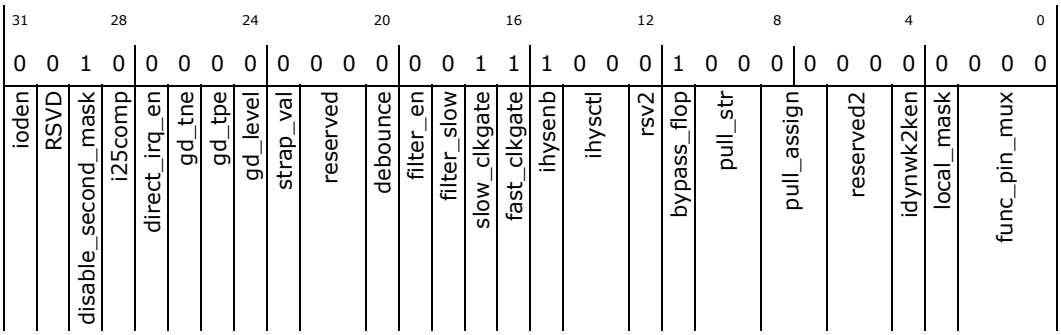
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_10_PCONF0: [IOBASE] + 750h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.353 Vgpio 10 Delay Line Multiplexer (cfio_regs_pad_vgpio_10_PCONF1)—Offset 754h

DLL Multiplexer

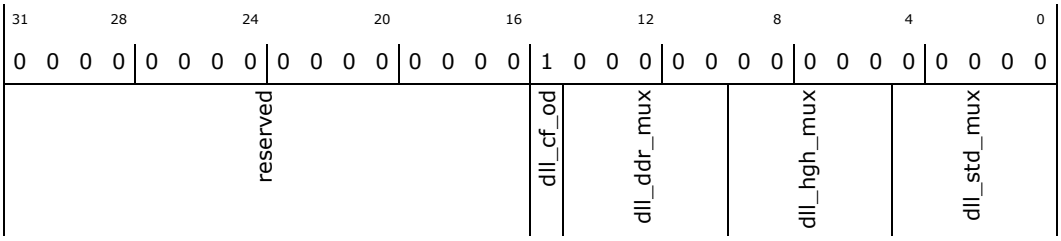
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_10_PCONF1: [IOBASE] + 754h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.354 Vgpio 10 Pad Value (cfio_regs_pad_vgpio_10_PAD_VAL)—Offset 758h

PADs Memory space Value register (access via PCU proxy)

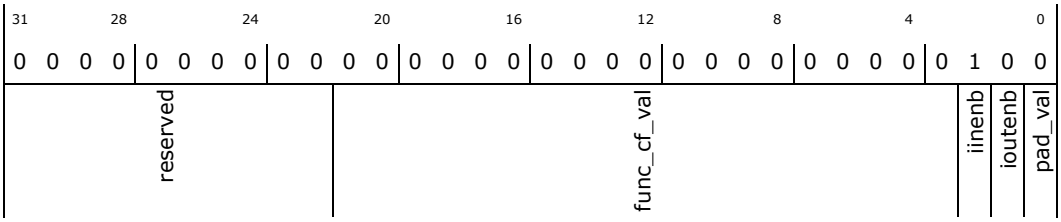
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_10_PAD_VAL: [IOBASE] + 758h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.355 Vgpio 11 Pad Configuration (cfio_regs_pad_vgpio_11_PCONF0)—Offset 760h

PADs Memory space configuration register (access via PCU proxy)

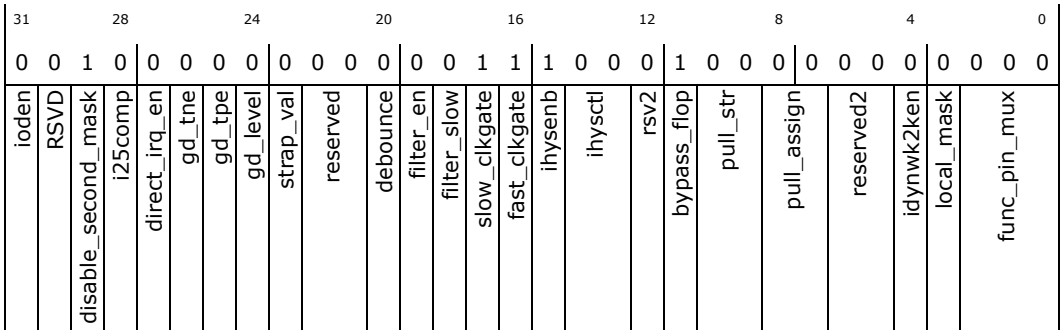
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_11_PCONF0: [IOBASE] + 760h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.356 Vgpio 11 Delay Line Multiplexer (cfio_regs_pad_vgpio_11_PCONF1)—Offset 764h

DLL Multiplexer

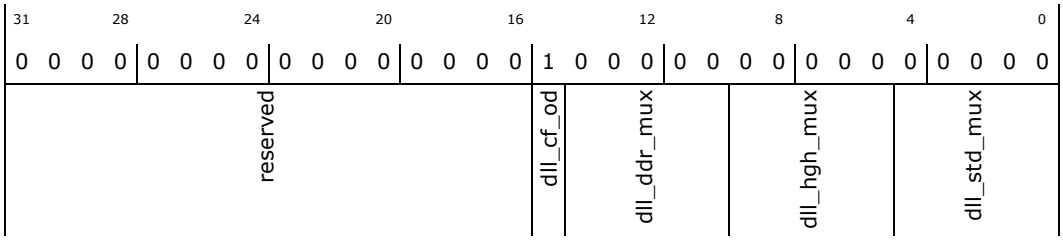
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_11_PCONF1: [IOBASE] + 764h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.357 Vgpio 11 Pad Value (cfio_regs_pad_vgpio_11_PAD_VAL)—Offset 768h

PADs Memory space Value register (access via PCU proxy)

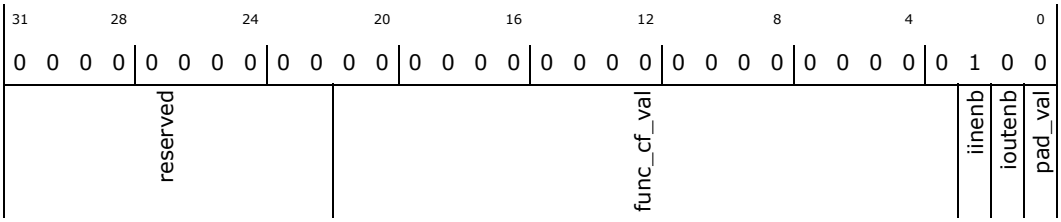
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_11_PAD_VAL: [IOBASE] + 768h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.358 Vgpio 12 Pad Configuration (cfio_regs_pad_vgpio_12_PCONF0)—Offset 770h

PADs Memory space configuration register (access via PCU proxy)

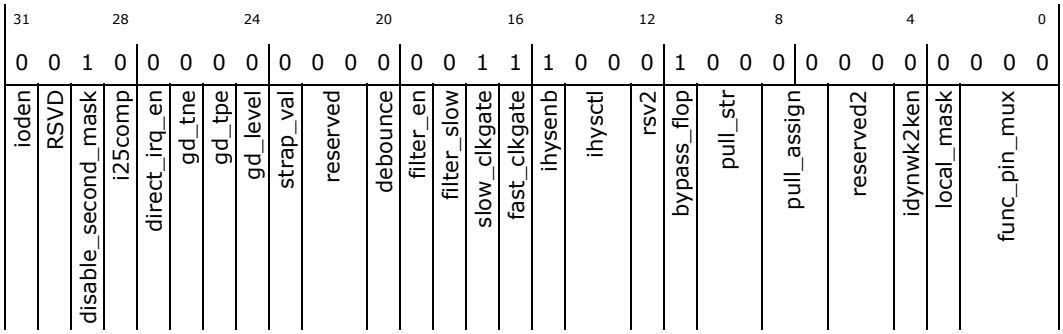
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_12_PCONF0: [IOBASE] + 770h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.359 Vgpio 12 Delay Line Multiplexer (cfio_regs_pad_vgpio_12_PCONF1)—Offset 774h

DLL Multiplexer

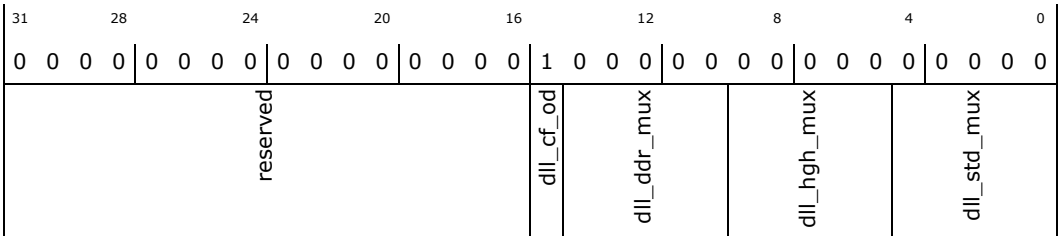
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_12_PCONF1: [IOBASE] + 774h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.360 Vgpio 12 Pad Value (cfio_regs_pad_vgpio_12_PAD_VAL)—Offset 778h

PADs Memory space Value register (access via PCU proxy)

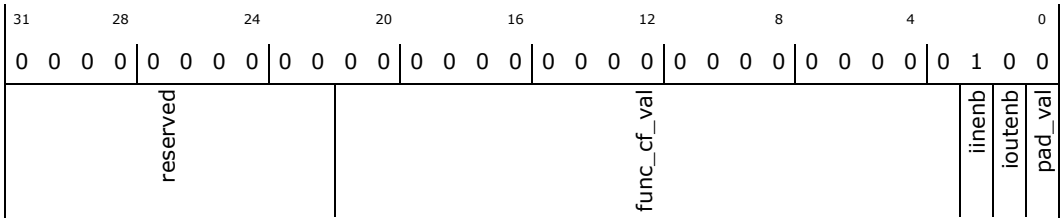
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_12_PAD_VAL: [IOBASE] + 778h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.361 Vgpio 13 Pad Configuration (cfio_regs_pad_vgpio_13_PCONF0)—Offset 780h

PADs Memory space configuration register (access via PCU proxy)

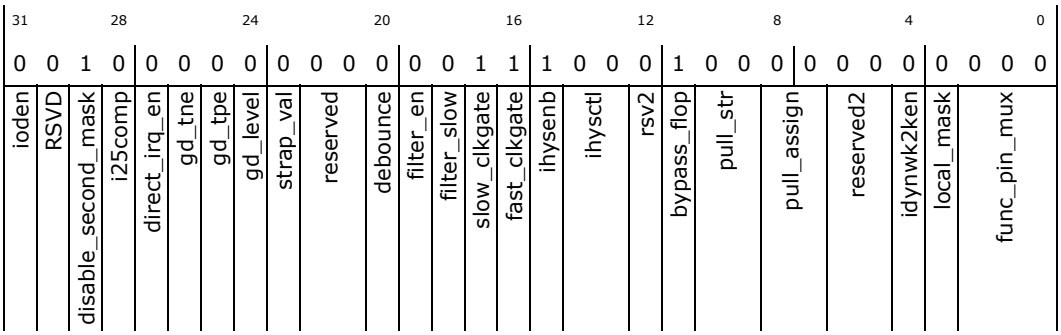
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_13_PCONF0: [IOBASE] + 780h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.362 Vgpio 13 Delay Line Multiplexer (cfio_regs_pad_vgpio_13_PCONF1)—Offset 784h

DLL Multiplexer

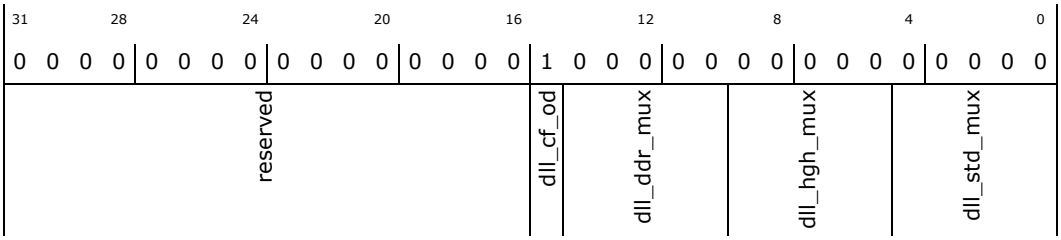
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_13_PCONF1: [IOBASE] + 784h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.363 Vgpio 13 Pad Value (cfio_regs_pad_vgpio_13_PAD_VAL)—Offset 788h

PADs Memory space Value register (access via PCU proxy)

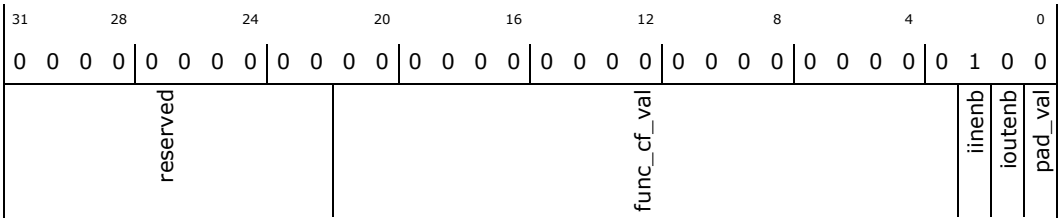
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_13_PAD_VAL: [IOBASE] + 788h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.364 Vgpio 14 Pad Configuration (cfio_regs_pad_vgpio_14_PCONF0)—Offset 790h

PADs Memory space configuration register (access via PCU proxy)

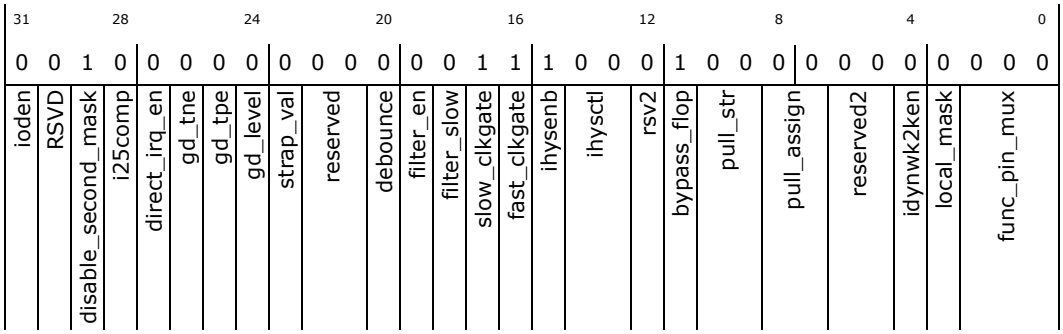
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_14_PCONF0: [IOBASE] + 790h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.365 Vgpio 14 Delay Line Multiplexer (cfio_regs_pad_vgpio_14_PCONF1)—Offset 794h

DLL Multiplexer

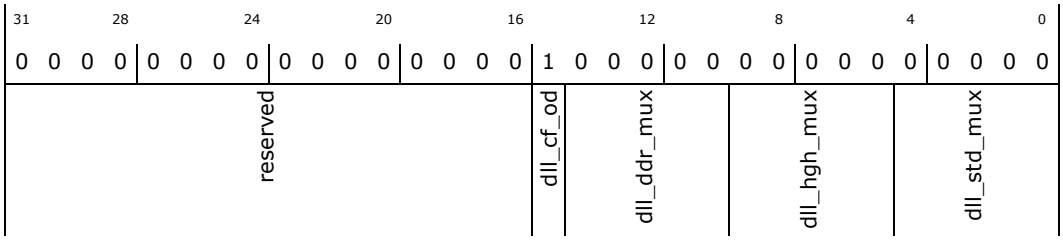
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_14_PCONF1: [IOBASE] + 794h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.366 Vgpio 14 Pad Value (cfio_regs_pad_vgpio_14_PAD_VAL)—Offset 798h

PADs Memory space Value register (access via PCU proxy)

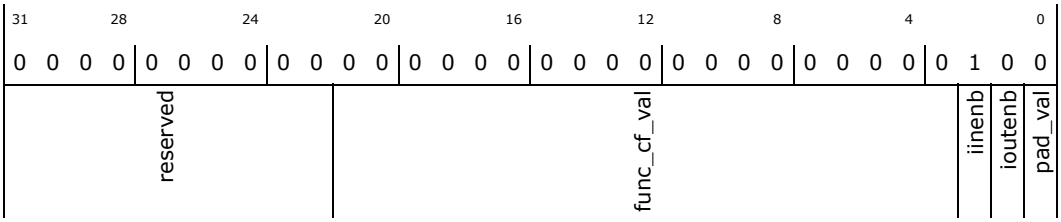
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_14_PAD_VAL: [IOBASE] + 798h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.367 Vgpio 15 Pad Configuration (cfio_regs_pad_vgpio_15_PCONF0)—Offset 7A0h

PADs Memory space configuration register (access via PCU proxy)

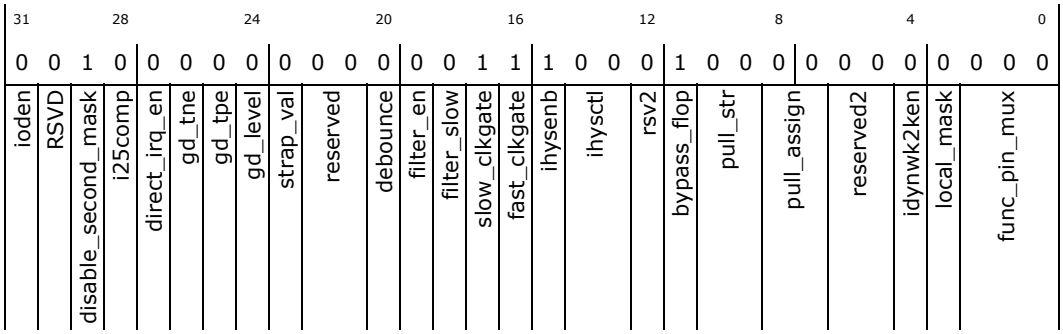
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_15_PCONF0: [IOBASE] + 7A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.368 Vgpio 15 Delay Line Multiplexer (cfio_regs_pad_vgpio_15_PCONF1)—Offset 7A4h

DLL Multiplexer

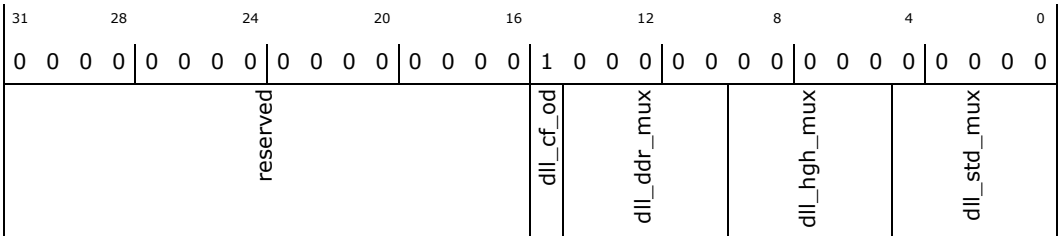
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_15_PCONF1: [IOBASE] + 7A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.369 Vgpio 15 Pad Value (cfio_regs_pad_vgpio_15_PAD_VAL)—Offset 7A8h

PADs Memory space Value register (access via PCU proxy)

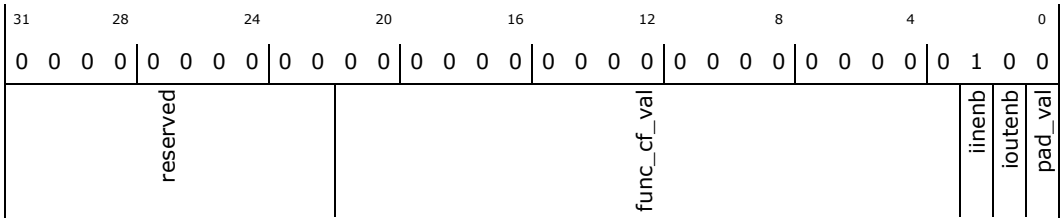
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_15_PAD_VAL: [IOBASE] + 7A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.370 Vgpio 16 Pad Configuration (cfio_regs_pad_vgpio_16_PCONF0)—Offset 7B0h

PADs Memory space configuration register (access via PCU proxy)

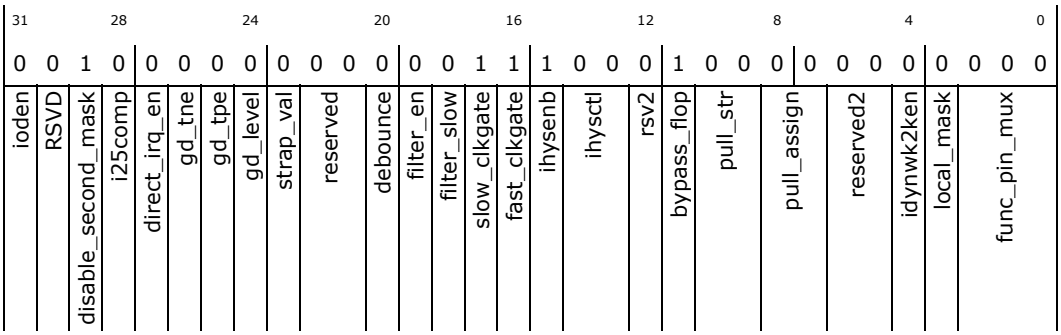
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_16_PCONF0: [IOBASE] + 7B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.371 Vgpio 16 Delay Line Multiplexer (cfio_regs_pad_vgpio_16_PCONF1)—Offset 7B4h

DLL Multiplexer

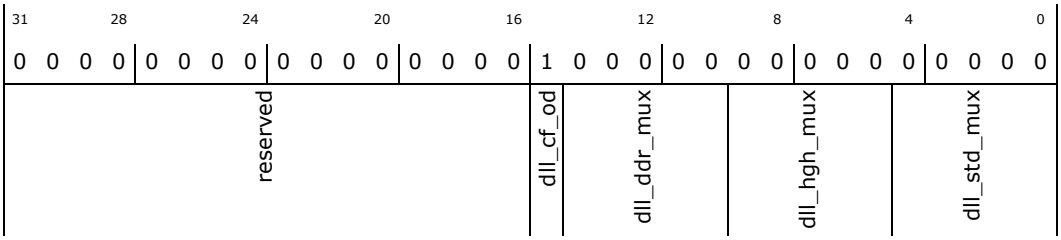
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_16_PCONF1: [IOBASE] + 7B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.372 Vgpio 16 Pad Value (cfio_regs_pad_vgpio_16_PAD_VAL)—Offset 7B8h

PADs Memory space Value register (access via PCU proxy)

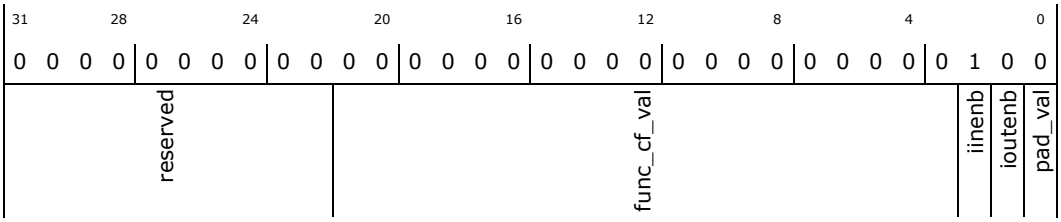
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_16_PAD_VAL: [IOBASE] + 7B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.373 Vgpio 17 Pad Configuration (cfio_regs_pad_vgpio_17_PCONF0)—Offset 7C0h

PADs Memory space configuration register (access via PCU proxy)

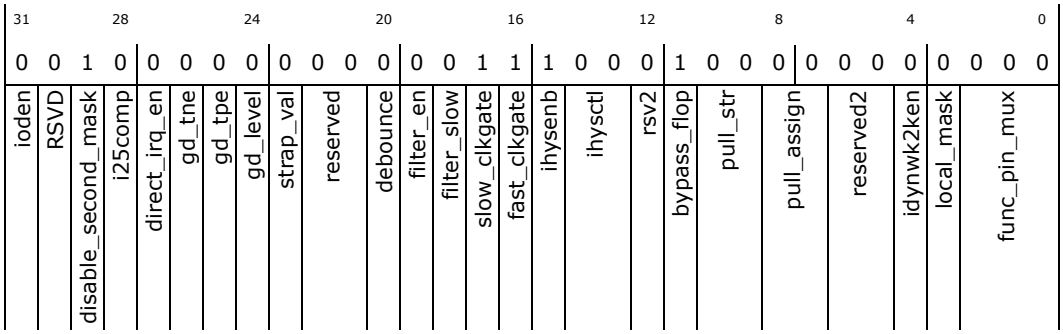
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_17_PCONF0: [IOBASE] + 7C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.374 Vgpio 17 Delay Line Multiplexer (cfio_regs_pad_vgpio_17_PCONF1)—Offset 7C4h

DLL Multiplexer

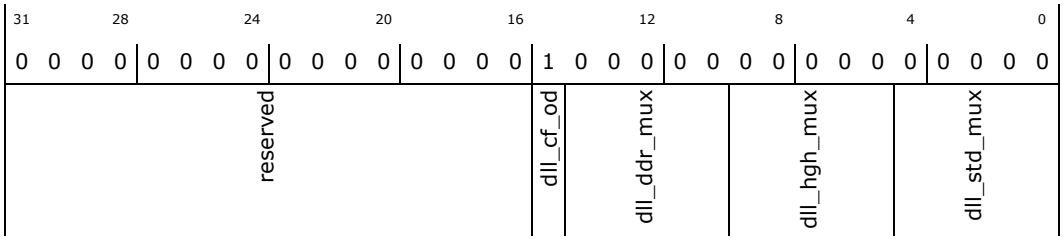
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_17_PCONF1: [IOBASE] + 7C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.375 Vgpio 17 Pad Value (cfio_regs_pad_vgpio_17_PAD_VAL)—Offset 7C8h

PADs Memory space Value register (access via PCU proxy)

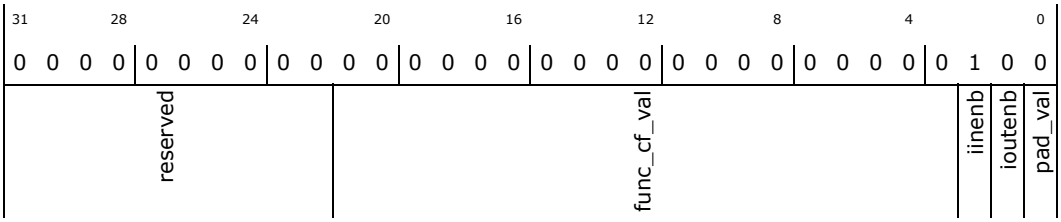
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_17_PAD_VAL: [IOBASE] + 7C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.376 Vgpio 18 Pad Configuration (cfio_regs_pad_vgpio_18_PCONF0)—Offset 7D0h

PADs Memory space configuration register (access via PCU proxy)

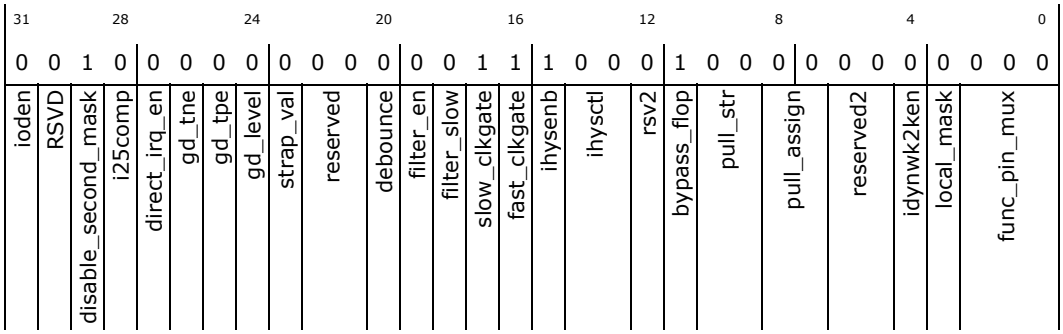
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_18_PCONF0: [IOBASE] + 7D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.377 Vgpio 18 Delay Line Multiplexer (cfio_regs_pad_vgpio_18_PCONF1)—Offset 7D4h

DLL Multiplexer

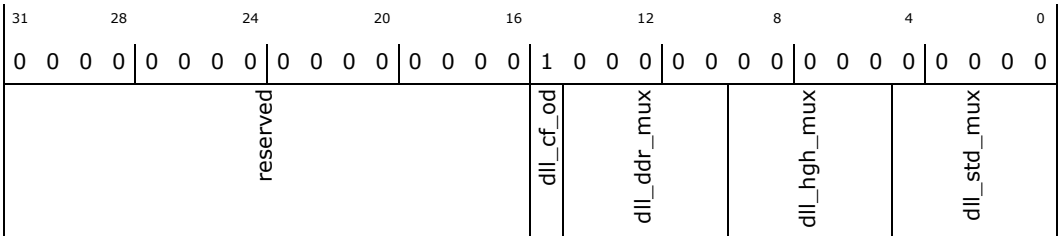
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_18_PCONF1: [IOBASE] + 7D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.378 Vgpio 18 Pad Value (cfio_regs_pad_vgpio_18_PAD_VAL)—Offset 7D8h

PADs Memory space Value register (access via PCU proxy)

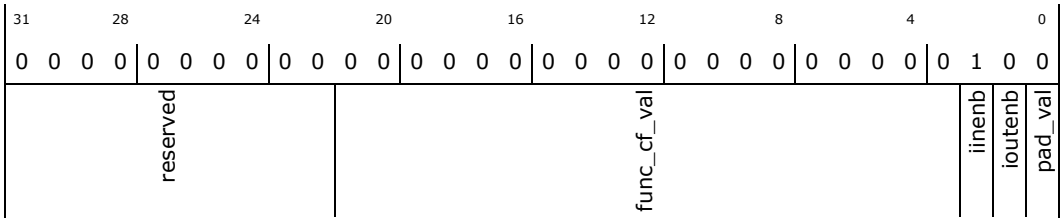
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_18_PAD_VAL: [IOBASE] + 7D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.379 Vgpio 19 Pad Configuration (cfio_regs_pad_vgpio_19_PCONF0)—Offset 7E0h

PADs Memory space configuration register (access via PCU proxy)

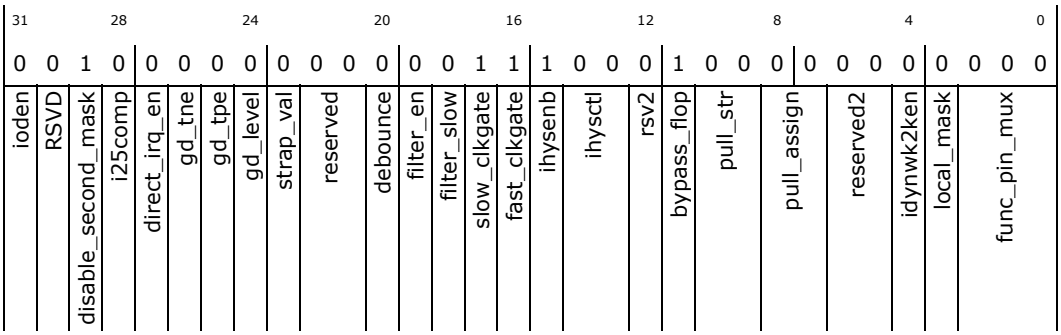
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_19_PCONF0: [IOBASE] + 7E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.380 Vgpio 19 Delay Line Multiplexer (cfio_regs_pad_vgpio_19_PCONF1)—Offset 7E4h

DLL Multiplexer

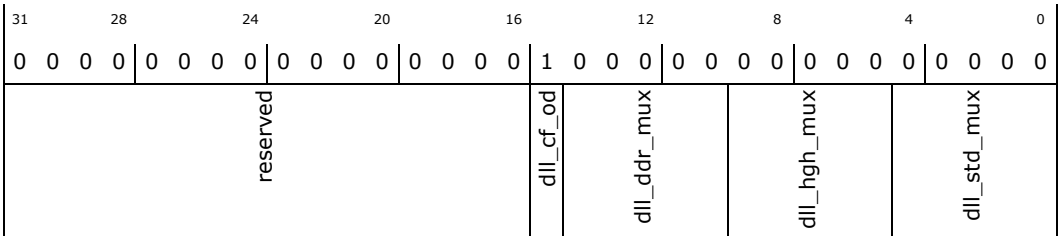
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_19_PCONF1: [IOBASE] + 7E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.381 Vgpio 19 Pad Value (cfio_regs_pad_vgpio_19_PAD_VAL)—Offset 7E8h

PADs Memory space Value register (access via PCU proxy)

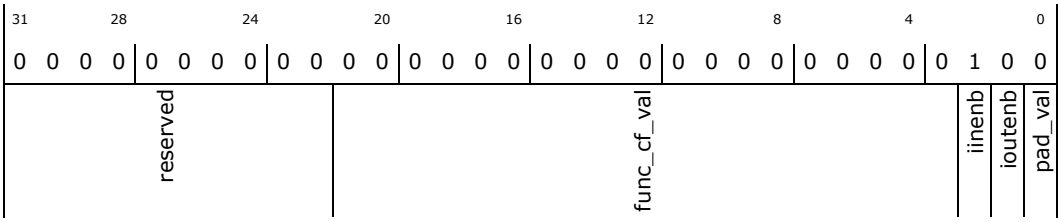
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_19_PAD_VAL: [IOBASE] + 7E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.382 Vgpio 20 Pad Configuration (cfio_regs_pad_vgpio_20_PCONF0)—Offset 7F0h

PADs Memory space configuration register (access via PCU proxy)

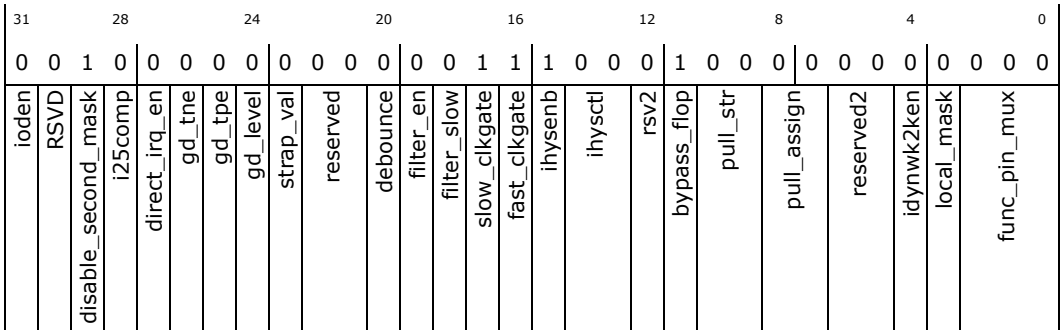
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_20_PCONF0: [IOBASE] + 7F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h



Bit Range	Default & Access	Description
31	0b RO	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	00b RO	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RO	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function.

3.67.383 Vgpio 20 Delay Line Multiplexer (cfio_regs_pad_vgpio_20_PCONF1)—Offset 7F4h

DLL Multiplexer

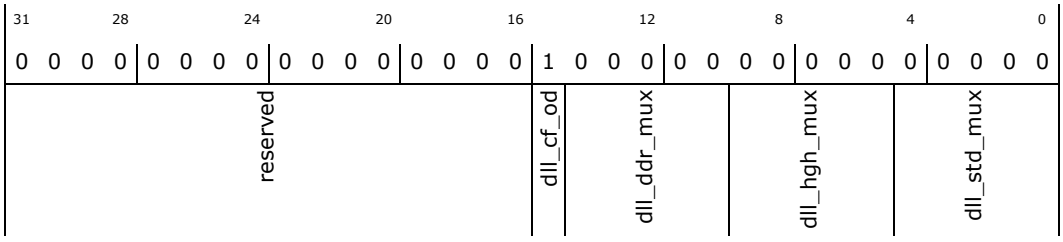
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_20_PCONF1: [IOBASE] + 7F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.67.384 Vgpio 20 Pad Value (cfio_regs_pad_vgpio_20_PAD_VAL)—Offset 7F8h

PADs Memory space Value register (access via PCU proxy)

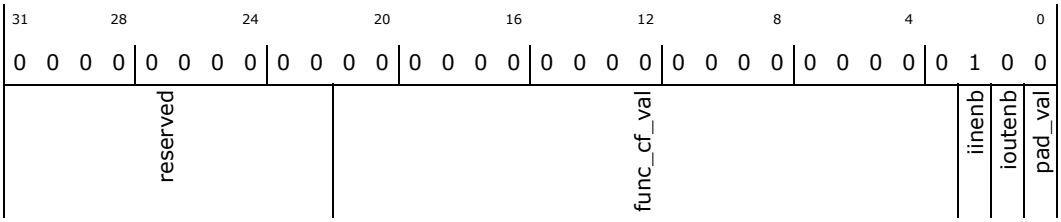
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_vgpio_20_PAD_VAL: [IOBASE] + 7F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	0b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.67.385 TS0 SCORE Interrupt Status 0 (cfio_regs_REG_TS0_SCORE_IRQ_TS_0)—Offset 800h

IRQ TS 0 status register

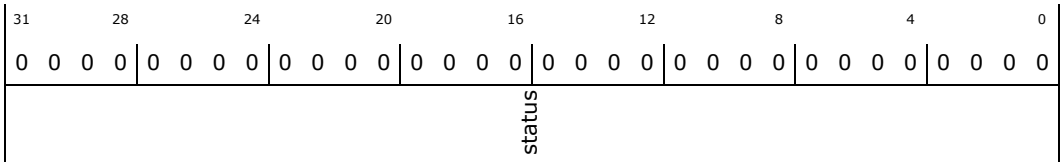
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_TS0_SCORE_IRQ_TS_0: [IOBASE] + 800h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RWOC	**Status (status):** TS: Trigger Status: When set to a 1, the corresponding GPIO (if disabled in the GPIO_USE_SEL register) if enabled as input via , triggered an IRQ event. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. Each bit is associated with different PAD controller, see RDL. Bellow is the given list of gpio number and pads, the irq status refers to bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

3.67.386 TS1 SCORE Interrupt Status 1 (cfio_regs_REG_TS1_SCORE_IRQ_TS_1)—Offset 804h

IRQ TS 1 status register

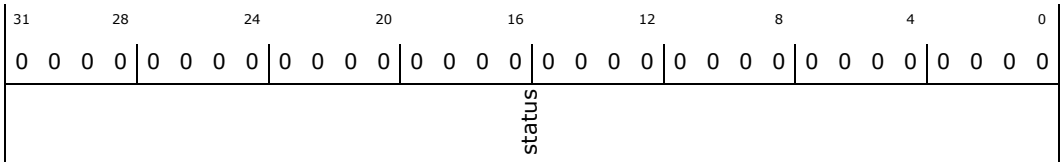
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_TS1_SCORE_IRQ_TS_1: [IOBASE] + 804h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RWOC	**Status (status):** TS: Trigger Status: When set to a 1, the corresponding GPIO (if disabled in the GPIO_USE_SEL register) if enabled as input via , triggered an IRQ event. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. Each bit is associated with different PAD controller, see RDL. Bellow is the given list of gpio number and pads, the irq status refers to bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

3.67.387 TS2 SCORE Interrupt Status 2 (cfio_regs_REG_TS2_SCORE_IRQ_TS_2)—Offset 808h

IRQ TS 2 status register

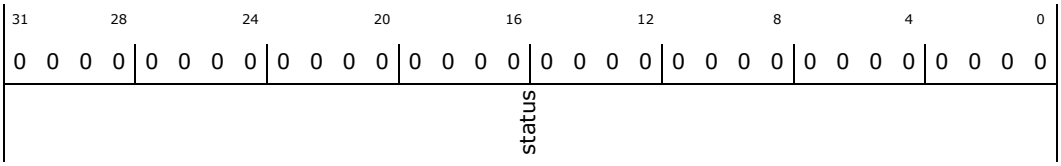
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_TS2_SCORE_IRQ_TS_2: [IOBASE] + 808h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RWOC	**Status (status):** TS: Trigger Status: When set to a 1, the corresponding GPIO (if disabled in the GPIO_USE_SEL register) if enabled as input via , triggered an IRQ event. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. Each bit is associated with different PAD controller, see RDL. Bellow is the given list of gpio number and pads, the irq status refers to bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

3.67.388 TS3 SCORE Interrupt Status 3 (cfio_regs_REG_TS3_SCORE_IRQ_TS_3)—Offset 80Ch

IRQ TS 3 status register

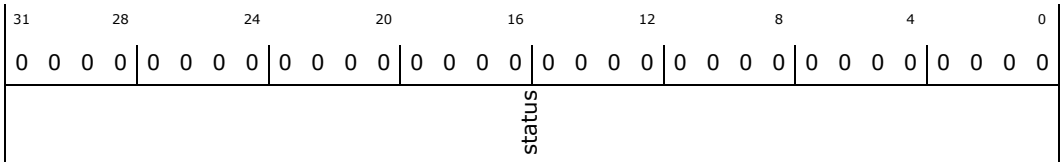
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_TS3_SCORE_IRQ_TS_3: [IOBASE] + 80Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RWOC	**Status (status):** TS: Trigger Status: When set to a 1, the corresponding GPIO (if disabled in the GPIO_USE_SEL register) if enabled as input via , triggered an IRQ event. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. Each bit is associated with different PAD controller, see RDL. Bellow is the given list of gpio number and pads, the irq status refers to bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

3.67.389 C71p1cfiomvscoreaza Compensation Configuration (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_CFG) —Offset 810h

FAMs Memory space Value register

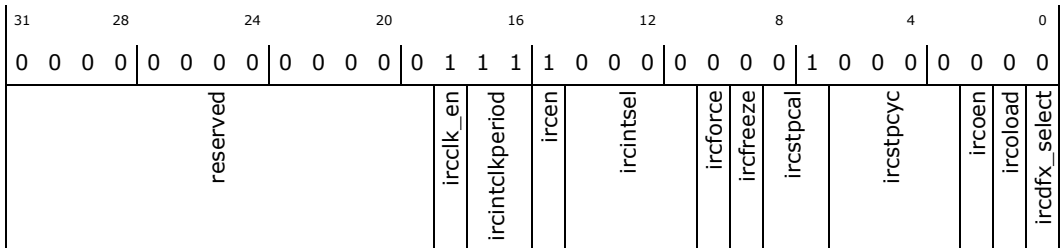
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_CFG: [IOBASE] + 810h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078080h



Bit Range	Default & Access	Description
31:19	0000h RO	**Reserved (reserved):** reserved
18	1b RW	**Ircclk En (ircclk_en):** This is enabling the rcomp clock. When rcomp clock is gated, rcomp reset is forced too, so when it is ungated again it will compensate
17:16	11b RW	**Ircintclkperiod (ircintclkperiod):** reserved
15	1b RW	**Ircen (ircen):** Enable RCOMP state machine for periodic RCOMP mode. This has to be enabled throughout periodic mode .0 state machine disabled 1 state machine enabled (default)
14:11	0000b RW	**Ircintsel (ircintsel):** Interval select this will select the periodic RCOMP update interval. All are periodic mode except 0000 option. 0000 non-periodic mode 0.5ms - 0001 1ms 0010 2ms 0011 3ms - 0100 4ms - 0101 5ms - 0110 10ms 0111 (Default) 15ms - 1000 25ms - 1001 50ms - 1010 100ms - 1011 200ms 1100 500ms - 1101 1000ms - 1110 2000ms - 1111 (non-periodic mode RCOMP update is not automatically triggered after the initial RCOMP cycle)
10	0b RW	**Ircforce (ircforce):** Force rcomp. only valid during non-periodic mode. RCOMP SM will trigger upon this signal goes high, so need first to clear it, and then set it high
9	0b RW	**Ircfreeze (ircfreeze):** Freeze rcomp. only valid during periodic mode. Setting this bit to 1 will stop the RCOMP S/M by stopping and clearing the 1ms and 10ms counter. Clearing it (0) would enable 1ms and 10ms counter again.

Bit Range	Default & Access	Description
8:7	01b RW	**Ircstpcal (ircstpcal):** Stop calibration option. RCOMP SM (pullup and pulldown) will finish calibrating once orcpupen/orcpdnen toggle/s. The toggling would indicate the compensation value has been reached. This options is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by ircstpcyc input). 00 single edge detect (10 or 01) 01 double edge detect (101 or 010) (default) 10 triple edge detect (1010 or 0101) 11 stop after x cycles (depending on ircompstpcyc[3:0] value -- This is meant for debug) Default is 01 (double edge detect 101 or 010)
6:3	0000b RW	**Ircstpcyc (ircstpcyc):** Number of cycles calibration would be going through before stopping.0000 0 cycle 0001 1 cycle 0010 2 cycles ..... 1110 14 cycles 1111 15 cycles (maximum allowed with this options) valid only when ircompstpcal[1:0]=2b11. This is meant for debug.
2	0b RW	**Ircoen (ircoen):** Override enable. Setting this bit would allow system to go and override RCOMP value with data from config registers (which will drive ircpuov and ircpdov)
1	0b RW	**Ircoload (ircoload):** Do override now. only valid with ircoen enabled. once this bit is set, data from ircpuov and ircpdov will be loaded into each buffer
0	0b RW	**Ircdfx Select (ircdfx_select):** Bypass RCOMP calibration values and use DFX values instead. Setting this bit (1) would let ircdfx_pstr and ircdfx_nstr value loaded into all buffers.

3.67.390 C71p1cfiomvscoreaza Compensation Override (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_OV)—Offset 814h

FAMs Memory space Value register

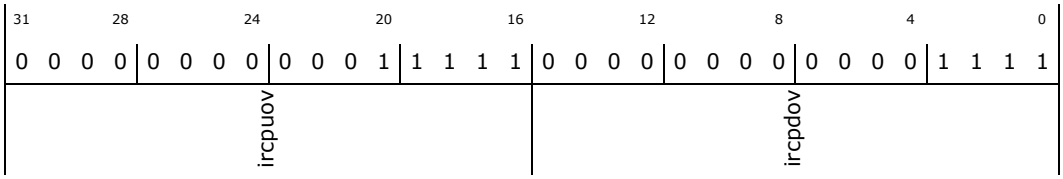
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_OV: [IOBASE] + 814h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 001F000Fh



Bit Range	Default & Access	Description
31:16	001fh RW	**Ircpuov (ircpuov):** override RCOMP value for pullup Should be 50ohm typical corner.
15:0	000fh RW	**Ircpdov (ircpdov):** override RCOMP value for pulldown Should be 50ohm typical corner.

3.67.391 C71p1cfiomvscoreaza Compensation Initial Values (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_INIT)—Offset 818h

FAMs Memory space Value register

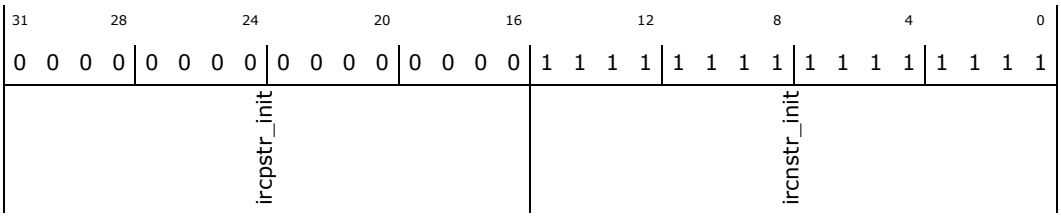
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_INIT: [IOBASE] + 818h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0000FFFFh



Bit Range	Default & Access	Description
31:16	0000h RW	**Ircpstr Init (ircpstr_init):** Initial pleg calibration value. Should not be changed.
15:0	FFFFh RW	**Ircnstr Init (ircnstr_init):** Initial nleg calibration value. Should not be changed.

3.67.392 C71p1cfiomvscoreaza Compensation DFX Override (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_DFX)—Offset 81Ch

FAMs Memory space Value register

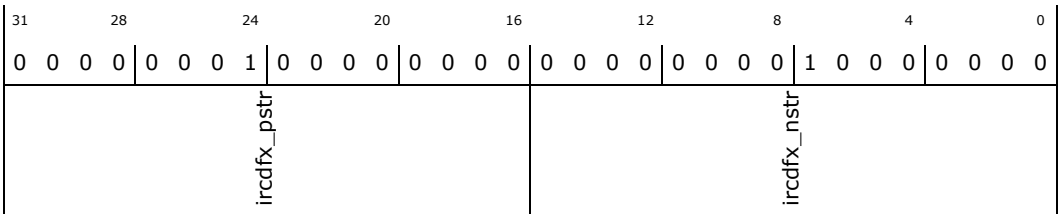
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_DFX: [IOBASE] + 81Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01000080h



Bit Range	Default & Access	Description
31:16	0100h RW	**Ircdfx Pstr (ircdfx_pstr):** DFX compensation p-leg value. Should be 50ohm typical corner.
15:0	0080h RW	**Ircdfx Nstr (ircdfx_nstr):** DFX compensation n-leg value Should be 50ohm typical corner.

3.67.393 C71p1cfiomvrscoresdio1 Compensation Configuration (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_CFG)—Offset 820h

FAMs Memory space Value register

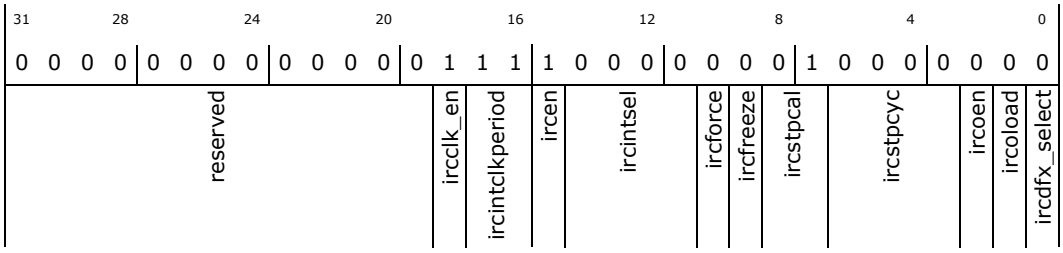
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_CFG : [IOBASE] + 820h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078080h



Bit Range	Default & Access	Description
31:19	0000h RO	**Reserved (reserved):** reserved
18	1b RW	**Ircclk En (ircclk_en):** This is enabling the rcomp clock. When rcomp clock is gated, rcomp reset is forced too, so when it is ungated again it will compensate
17:16	11b RW	**Ircintclkperiod (ircintclkperiod):** reserved
15	1b RW	**Ircen (ircen):** Enable RCOMP state machine for periodic RCOMP mode. This has to be enabled throughout periodic mode .0 state machine disabled 1 state machine enabled (default)
14:11	0000b RW	**Ircintsel (ircintsel):** Interval select this will select the periodic RCOMP update interval. All are periodic mode except 0000 option. 0000 non-periodic mode 0.5ms - 0001 1ms 0010 2ms 0011 3ms - 0100 4ms - 0101 5ms - 0110 10ms 0111 (Default) 15ms - 1000 25ms - 1001 50ms - 1010 100ms - 1011 200ms 1100 500ms - 1101 1000ms - 1110 2000ms - 1111 (non-periodic mode RCOMP update is not automatically triggered after the initial RCOMP cycle)

Bit Range	Default & Access	Description
10	0b RW	**Ircforce (ircforce):** Force rcomp. only valid during non-periodic mode. RCOMP SM will trigger upon this signal goes high, so need first to clear it, and then set it high
9	0b RW	**Ircfreeze (ircfreeze):** Freeze rcomp. only valid during periodic mode. Setting this bit to 1 will stop the RCOMP S/M by stopping and clearing the 1ms and 10ms counter. Clearing it (0) would enable 1ms and 10ms counter again.
8:7	01b RW	**Ircstpcal (ircstpcal):** Stop calibration option. RCOMP SM (pullup and pulldown) will finish calibrating once orcpupen/orcpdnen toggle/s. The toggling would indicate the compensation value has been reached. This options is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by ircstpcyc input). 00 single edge detect (10 or 01) 01 double edge detect (101 or 010) (default) 10 triple edge detect (1010 or 0101) 11 stop after x cycles (depending on ircompstpcyc[3:0] value -- This is meant for debug) Default is 01 (double edge detect 101 or 010)
6:3	0000b RW	**Ircstpcyc (ircstpcyc):** Number of cycles calibration would be going through before stopping.0000 0 cycle 0001 1 cycle 0010 2 cycles ..... 1110 14 cycles 1111 15 cycles (maximum allowed with this options) valid only when ircompstpcal[1:0]=2b11. This is meant for debug.
2	0b RW	**Ircoen (ircoen):** Override enable. Setting this bit would allow system to go and override RCOMP value with data from config registers (which will drive ircpuov and ircpdov)
1	0b RW	**Ircoload (ircoload):** Do override now. only valid with ircoen enabled. once this bit is set, data from ircpuov and ircpdov will be loaded into each buffer
0	0b RW	**Ircdfx Select (ircdfx_select):** Bypass RCOMP calibration values and use DFX values instead. Setting this bit (1) would let ircdfx_pstr and ircdfx_nstr value loaded into all buffers.

3.67.394 C71p1cfiomvrscoresdio1 Compensation Override (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_OV)—Offset 824h

FAMs Memory space Value register

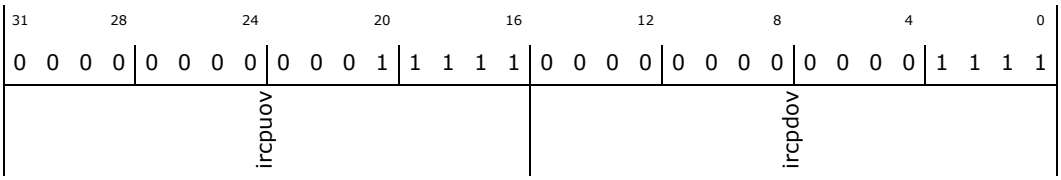
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_OV: [IOBASE] + 824h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 001F000Fh



Bit Range	Default & Access	Description
31:16	001fh RW	**Ircpuov (ircpuov):** override RCOMP value for pullup Should be 50ohm typical corner.
15:0	000fh RW	**Ircpdov (ircpdov):** override RCOMP value for pulldown Should be 50ohm typical corner.

3.67.395 C71p1cfiomvrscoresdio1 Compensation Initial Values (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_INIT)—Offset 828h

FAMs Memory space Value register

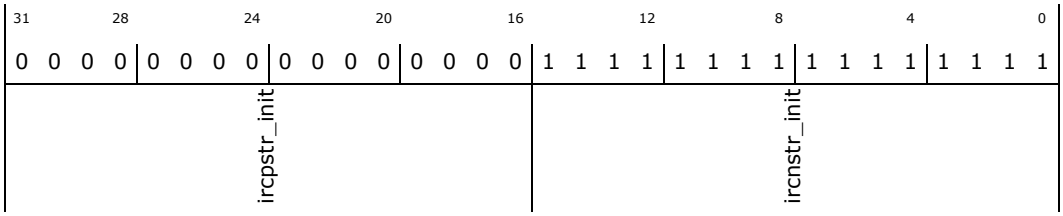
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_INIT: [IOBASE] + 828h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0000FFFFh



Bit Range	Default & Access	Description
31:16	0000h RW	**Ircpstr Init (ircpstr_init):** Initial pleg calibration value. Should not be changed.
15:0	FFFFh RW	**Ircnstr Init (ircnstr_init):** Initial nleg calibration value. Should not be changed.

3.67.396 C71p1cfiomvrscoresdio1 Compensation DFX Override (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_DFX)—Offset 82Ch

FAMs Memory space Value register

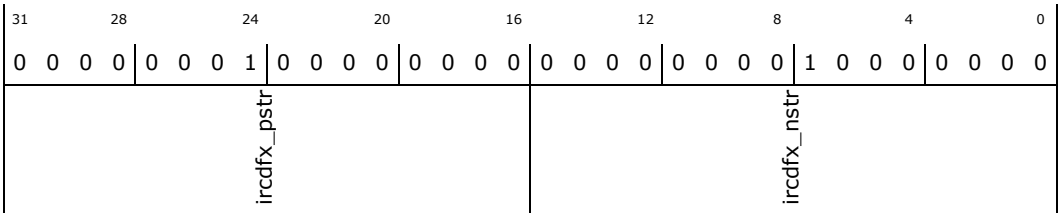
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_DFX: [IOBASE] + 82Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01000080h



Bit Range	Default & Access	Description
31:16	0100h RW	**Ircdfx Pstr (ircdfx_pstr):** DFX compensation p-leg value. Should be 50ohm typical corner.
15:0	0080h RW	**Ircdfx Nstr (ircdfx_nstr):** DFX compensation n-leg value Should be 50ohm typical corner.

3.67.397 C71p1cfiohvrscorepsdio3 Compensation Configuration (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_CFG)—Offset 830h

FAMs Memory space Value register

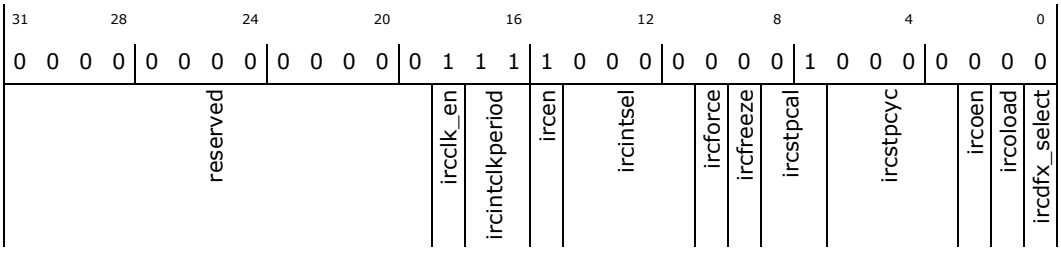
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_CFG : [IOBASE] + 830h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078080h



Bit Range	Default & Access	Description
31:19	0000h RO	**Reserved (reserved):** reserved
18	1b RW	**Ircclk En (ircclk_en):** This is enabling the rcomp clock. When rcomp clock is gated, rcomp reset is forced too, so when it is ungated again it will compensate
17:16	11b RW	**Ircintclkperiod (ircintclkperiod):** reserved
15	1b RW	**Ircen (ircen):** Enable RCOMP state machine for periodic RCOMP mode. This has to be enabled throughout periodic mode .0 state machine disabled 1 state machine enabled (default)

Bit Range	Default & Access	Description
14:11	0000b RW	**Ircintsel (ircintsel):** Interval select this will select the periodic RCOMP update interval. All are periodic mode except 0000 option. 0000 non-periodic mode 0.5ms - 0001 1ms 0010 2ms 0011 3ms - 0100 4ms - 0101 5ms - 0110 10ms 0111 (Default) 15ms - 1000 25ms - 1001 50ms - 1010 100ms - 1011 200ms 1100 500ms - 1101 1000ms - 1110 2000ms - 1111 (non-periodic mode RCOMP update is not automatically triggered after the initial RCOMP cycle)
10	0b RW	**Ircforce (ircforce):** Force rcomp. only valid during non-periodic mode. RCOMP SM will trigger upon this signal goes high, so need first to clear it, and then set it high
9	0b RW	**Ircfreeze (ircfreeze):** Freeze rcomp. only valid during periodic mode. Setting this bit to 1 will stop the RCOMP S/M by stopping and clearing the 1ms and 10ms counter. Clearing it (0) would enable 1ms and 10ms counter again.
8:7	01b RW	**Ircstpcal (ircstpcal):** Stop calibration option. RCOMP SM (pullup and pulldown) will finish calibrating once orcpupen/orcpdnen toggle/s. The toggling would indicate the compensation value has been reached. This options is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by ircstpcyc input). 00 single edge detect (10 or 01) 01 double edge detect (101 or 010) (default) 10 triple edge detect (1010 or 0101) 11 stop after x cycles (depending on ircompstpcyc[3:0] value -- This is meant for debug) Default is 01 (double edge detect 101 or 010)
6:3	0000b RW	**Ircstpcyc (ircstpcyc):** Number of cycles calibration would be going through before stopping.0000 0 cycle 0001 1 cycle 0010 2 cycles ..... 1110 14 cycles 1111 15 cycles (maximum allowed with this options) valid only when ircompstpcal[1:0]=2b11. This is meant for debug.
2	0b RW	**Ircoen (ircoen):** Override enable. Setting this bit would allow system to go and override RCOMP value with data from config registers (which will drive ircpuov and ircpdov)
1	0b RW	**Ircoload (ircoload):** Do override now. only valid with ircoen enabled. once this bit is set, data from ircpuov and ircpdov will be loaded into each buffer
0	0b RW	**Ircdfx Select (ircdfx_select):** Bypass RCOMP calibration values and use DFX values instead. Setting this bit (1) would let ircdfx_pstr and ircdfx_nstr value loaded into all buffers.

3.67.398 C71p1cfiohvrscorepsdio3 Compensation Override (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_OV)—Offset 834h

FAMs Memory space Value register

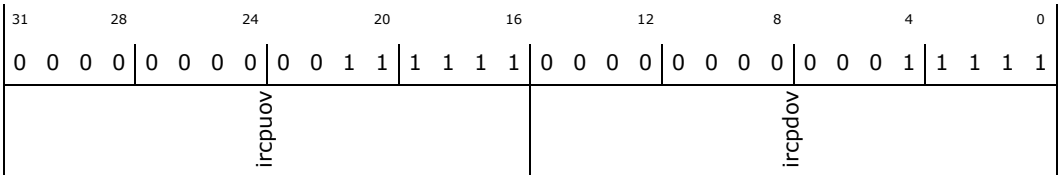
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_OV: [IOBASE] + 834h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 003F001Fh



Bit Range	Default & Access	Description
31:16	003fh RW	**Ircpuov (ircpuov):** override RCOMP value for pullup Should be 50ohm typical corner.
15:0	001fh RW	**Ircpdov (ircpdov):** override RCOMP value for pulldown Should be 50ohm typical corner.

3.67.399 C71p1cfiohvrscorepsdio3 Compensation Initial Values (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_INIT)—Offset 838h

FAMs Memory space Value register

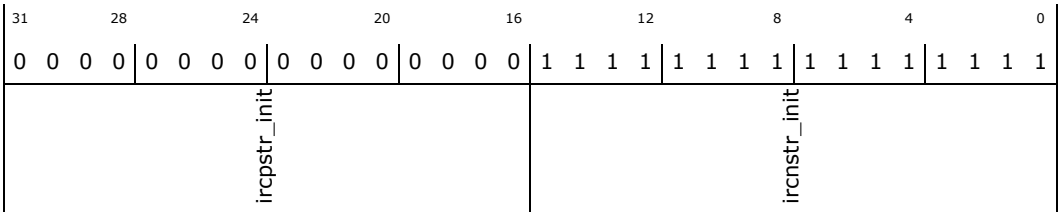
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_INIT: [IOBASE] + 838h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0000FFFFh



Bit Range	Default & Access	Description
31:16	0000h RW	**Ircpstr Init (ircpstr_init):** Initial pleg calibration value. Should not be changed.
15:0	FFFFh RW	**Ircnstr Init (ircnstr_init):** Initial nleg calibration value. Should not be changed.

3.67.400 C71p1cfiohvrscorepsdio3 Compensation DFX Override (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_DFX)—Offset 83Ch

FAMs Memory space Value register

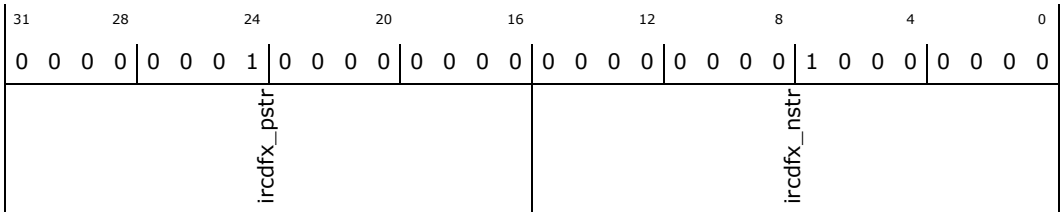
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_DFX: [IOBASE] + 83Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01000080h



Bit Range	Default & Access	Description
31:16	0100h RW	**Ircdfx Pstr (ircdfx_pstr):** DFX compensation p-leg value. Should be 50ohm typical corner.
15:0	0080h RW	**Ircdfx Nstr (ircdfx_nstr):** DFX compensation n-leg value Should be 50ohm typical corner.

3.67.401 C71p1cfiohvrscoreplpc Compensation Configuration (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_CFG)—Offset 840h

FAMs Memory space Value register

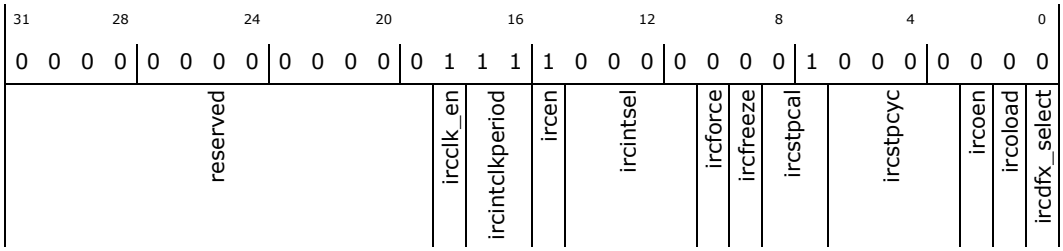
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

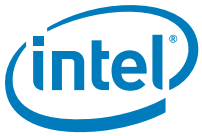
cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_CFG: [IOBASE] + 840h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078080h



Bit Range	Default & Access	Description
31:19	0000h RO	**Reserved (reserved):** reserved



Bit Range	Default & Access	Description
18	1b RW	**Ircclk En (ircclk_en):** This is enabling the rcomp clock. When rcomp clock is gated, rcomp reset is forced too, so when it is ungated again it will compensate
17:16	11b RW	**Ircintclkperiod (ircintclkperiod):** reserved
15	1b RW	**Ircen (ircen):** Enable RCOMP state machine for periodic RCOMP mode. This has to be enabled throughout periodic mode .0 state machine disabled 1 state machine enabled (default)
14:11	0000b RW	**Ircintsel (ircintsel):** Interval select this will select the periodic RCOMP update interval. All are periodic mode except 0000 option. 0000 non-periodic mode 0.5ms - 0001 1ms 0010 2ms 0011 3ms - 0100 4ms - 0101 5ms - 0110 10ms 0111 (Default) 15ms - 1000 25ms - 1001 50ms - 1010 100ms - 1011 200ms 1100 500ms - 1101 1000ms - 1110 2000ms - 1111 (non-periodic mode RCOMP update is not automatically triggered after the initial RCOMP cycle)
10	0b RW	**Ircforce (ircforce):** Force rcomp. only valid during non-periodic mode. RCOMP SM will trigger upon this signal goes high, so need first to clear it, and then set it high
9	0b RW	**Ircfreeze (ircfreeze):** Freeze rcomp. only valid during periodic mode. Setting this bit to 1 will stop the RCOMP S/M by stopping and clearing the 1ms and 10ms counter. Clearing it (0) would enable 1ms and 10ms counter again.
8:7	01b RW	**Ircstpcal (ircstpcal):** Stop calibration option. RCOMP SM (pullup and pulldown) will finish calibrating once orcpupen/orcpdnen toggle/s. The toggling would indicate the compensation value has been reached. This options is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by ircstpcyc input). 00 single edge detect (10 or 01) 01 double edge detect (101 or 010) (default) 10 triple edge detect (1010 or 0101) 11 stop after x cycles (depending on ircompstpcyc[3:0] value -- This is meant for debug) Default is 01 (double edge detect 101 or 010)
6:3	0000b RW	**Ircstpcyc (ircstpcyc):** Number of cycles calibration would be going through before stopping.0000 0 cycle 0001 1 cycle 0010 2 cycles ..... 1110 14 cycles 1111 15 cycles (maximum allowed with this options) valid only when ircompstpcal[1:0]=2b11. This is meant for debug.
2	0b RW	**Ircoen (ircoen):** Override enable. Setting this bit would allow system to go and override RCOMP value with data from config registers (which will drive ircpuov and ircpdov)
1	0b RW	**Ircoload (ircoload):** Do override now. only valid with ircoen enabled. once this bit is set, data from ircpuov and ircpdov will be loaded into each buffer
0	0b RW	**Ircdfx Select (ircdfx_select):** Bypass RCOMP calibration values and use DFX values instead. Setting this bit (1) would let ircdfx_pstr and ircdfx_nstr value loaded into all buffers.

3.67.402 C71p1cfiohvrscoreplpc Compensation Override (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_OV)—Offset 844h

FAMs Memory space Value register

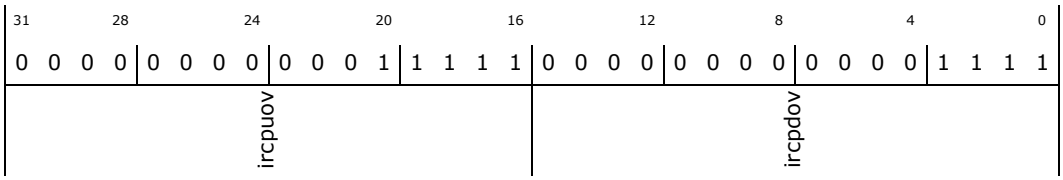
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_OV: [IOBASE] + 844h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 001F000Fh



Bit Range	Default & Access	Description
31:16	001fh RW	**Ircpuov (ircpuov):** override RCOMP value for pullup Should be 50ohm typical corner.
15:0	000fh RW	**Ircpdov (ircpdov):** override RCOMP value for pulldown Should be 50ohm typical corner.

3.67.403 C71p1cfiohvrscoreplpc Compensation Initial Values (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_INIT)—Offset 848h

FAMs Memory space Value register

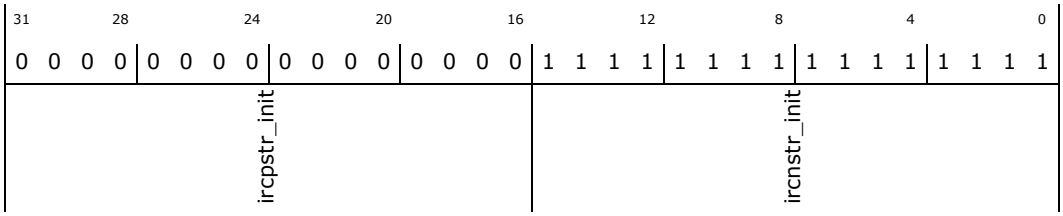
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_INIT: [IOBASE] + 848h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0000FFFFh



Bit Range	Default & Access	Description
31:16	0000h RW	**Ircpstr Init (ircpstr_init):** Initial pleg calibration value. Should not be changed.
15:0	FFFFh RW	**Ircnstr Init (ircnstr_init):** Initial nleg calibration value. Should not be changed.

3.67.404 C71p1cfiohvrscoreplpc Compensation DFX Override (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_DFX)—Offset 84Ch

FAMs Memory space Value register

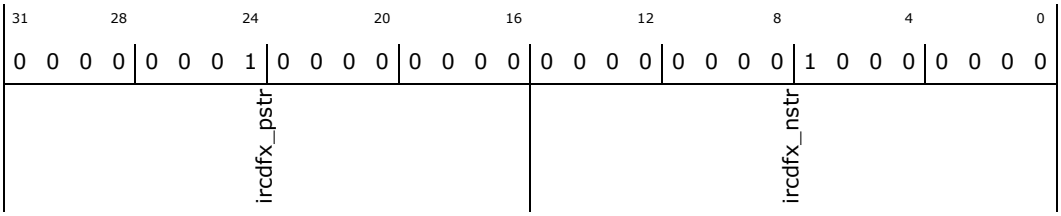
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_DFX: [IOBASE] + 84Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01000080h



Bit Range	Default & Access	Description
31:16	0100h RW	**Ircdfx Pstr (ircdfx_pstr):** DFX compensation p-leg value. Should be 50ohm typical corner.
15:0	0080h RW	**Ircdfx Nstr (ircdfx_nstr):** DFX compensation n-leg value Should be 50ohm typical corner.

3.67.405 Aza1 Strength Group (cfio_regs_aza1_STRENGTH)—Offset 850h

P and N strength register

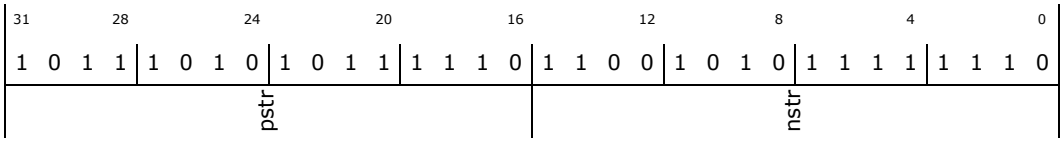
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_aza1_STRENGTH: [IOBASE] + 850h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: BABECAFEh



Bit Range	Default & Access	Description
31:16	babeh RO	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	cafeh RO	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.406 Clkreq Strength Group (cfio_regs_clkreq_STRENGTH)—Offset 854h

P and N strength register

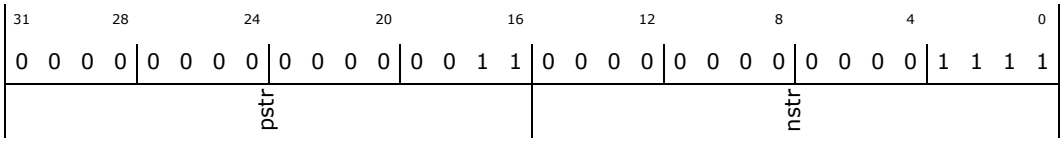
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_clkreq_STRENGTH: [IOBASE] + 854h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.407 Crt I2c Clk Strength Group (cfio_regs_crt_i2c_clk_STRENGTH)—Offset 858h

P and N strength register

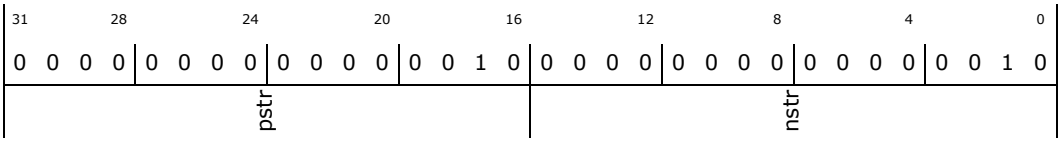
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_crt_i2c_clk_STRENGTH: [IOBASE] + 858h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00020002h



Bit Range	Default & Access	Description
31:16	0002h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	0002h RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.408 Crt I2c Data Strength Group (cfio_regs_crt_i2c_data_STRENGTH)—Offset 85Ch

P and N strength register

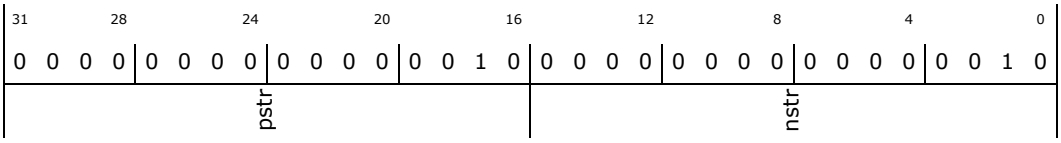
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_crt_i2c_data_STRENGTH: [IOBASE] + 85Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00020002h



Bit Range	Default & Access	Description
31:16	0002h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	0002h RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.409 Hsi Strength Group (cfio_regs_hsi_STRENGTH)—Offset 860h

P and N strength register

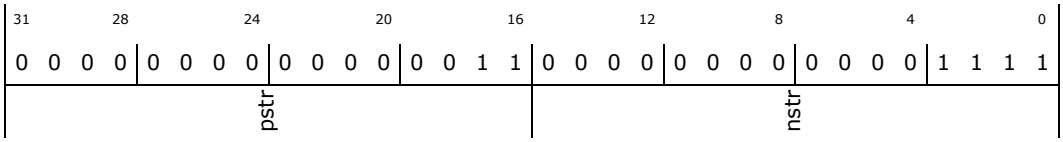
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_hsi_STRENGTH: [IOBASE] + 860h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.410 I2c Strength Group (cfio_regs_i2c_STRENGTH)—Offset 864h

P and N strength register

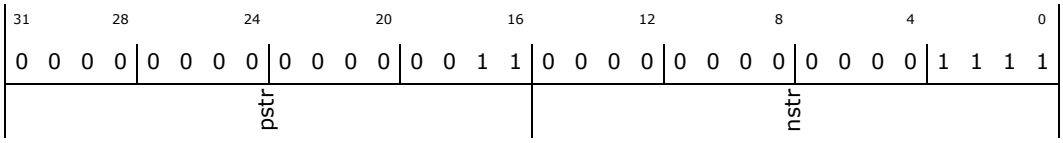
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_i2c_STRENGTH: [IOBASE] + 864h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.411 Lpc Strength Group (cfio_regs_lpc_STRENGTH)—Offset 868h

P and N strength register

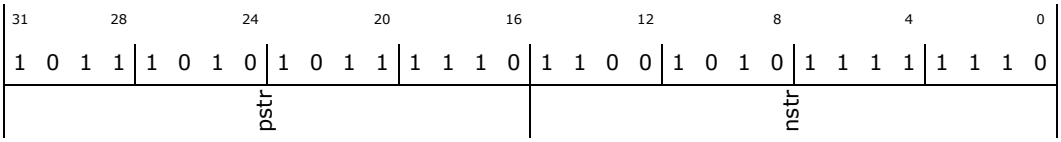
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_lpc_STRENGTH: [IOBASE] + 868h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: BABECAFEh



Bit Range	Default & Access	Description
31:16	babeh RO	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	cafeh RO	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.412 Mmc3 Strength Group (cfio_regs_mmc3_STRENGTH)—Offset 86Ch

P and N strength register

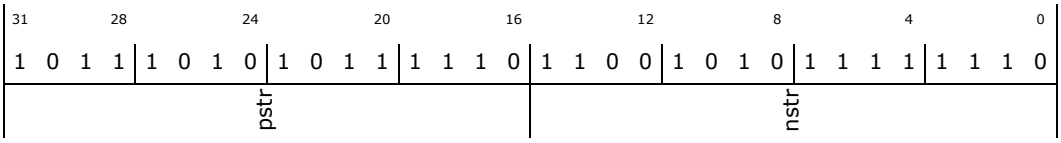
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_mmc3_STRENGTH: [IOBASE] + 86Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: BABECAFEh



Bit Range	Default & Access	Description
31:16	babeh RO	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	cafeh RO	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.413 Mvt Mmc3 Strength Group (cfio_regs_mvt_mmc3_STRENGTH)—Offset 870h

P and N strength register

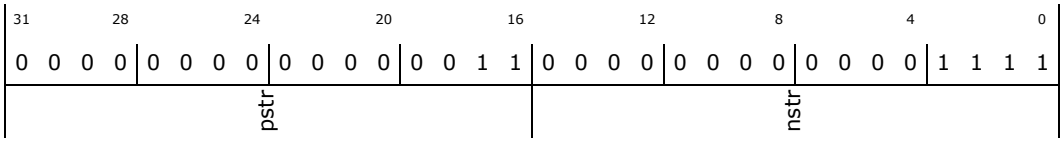
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_mvt_mmc3_STRENGTH: [IOBASE] + 870h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.414 Mvt Rcomp Strength Group (cfio_regs_mvt_rcomp_STRENGTH)—Offset 874h

P and N strength register

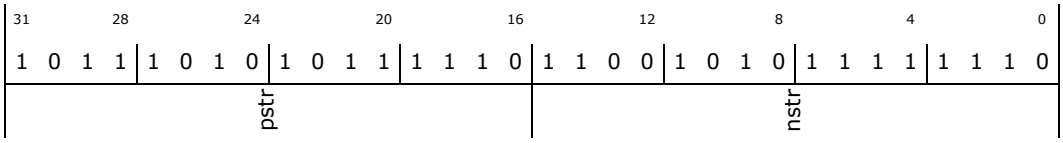
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_mvt_rcomp_STRENGTH: [IOBASE] + 874h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: BABECAFEh



Bit Range	Default & Access	Description
31:16	babeh RO	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	cafeh RO	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.415 Nfc Strength Group (cfio_regs_nfc_STRENGTH)—Offset 878h

P and N strength register

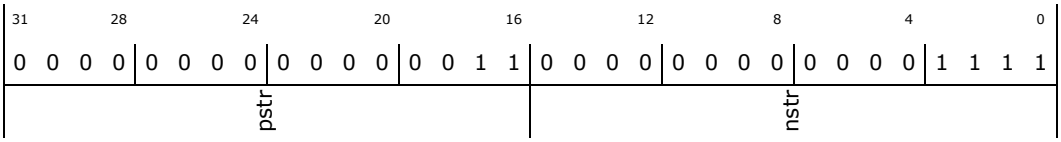
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_nfc_STRENGTH: [IOBASE] + 878h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.416 Pltclk Strength Group (cfio_regs_pltclk_STRENGTH)—Offset 87Ch

P and N strength register

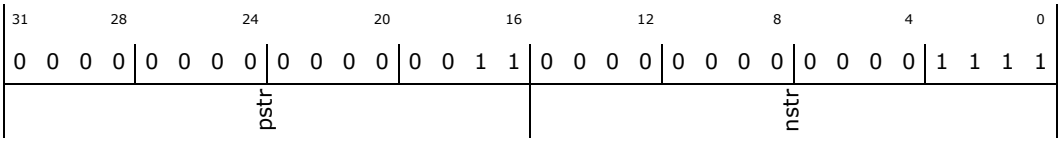
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pltclk_STRENGTH: [IOBASE] + 87Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.417 Pwm Strength Group (cfio_regs_pwm_STRENGTH)—Offset 880h

P and N strength register

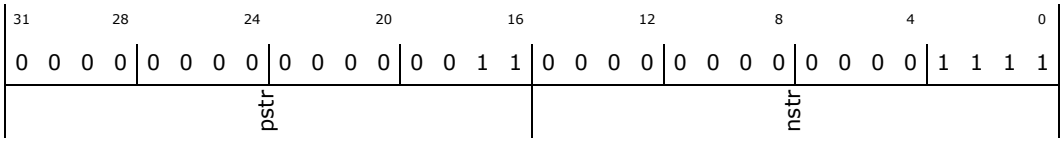
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pwm_STRENGTH: [IOBASE] + 880h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.418 Sata Strength Group (cfio_regs_sata_STRENGTH)—Offset 884h

P and N strength register

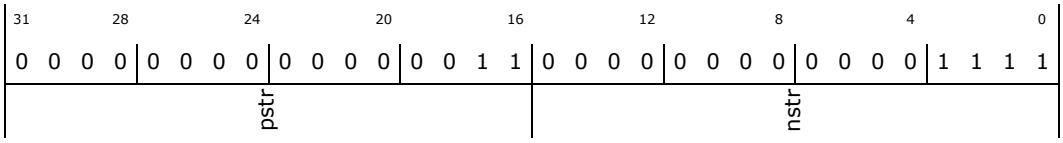
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sata_STRENGTH: [IOBASE] + 884h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.419 Smb Strength Group (cfio_regs_smb_STRENGTH)—Offset 888h

P and N strength register

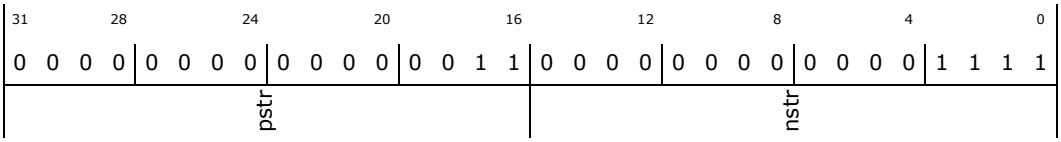
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_smb_STRENGTH: [IOBASE] + 888h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.420 Spi Strength Group (cfio_regs_spi_STRENGTH)—Offset 88Ch

P and N strength register

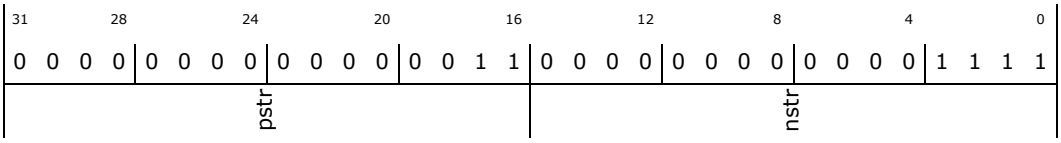
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_spi_STRENGTH: [IOBASE] + 88Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.421 Spkr Strength Group (cfio_regs_spkr_STRENGTH)—Offset 890h

P and N strength register

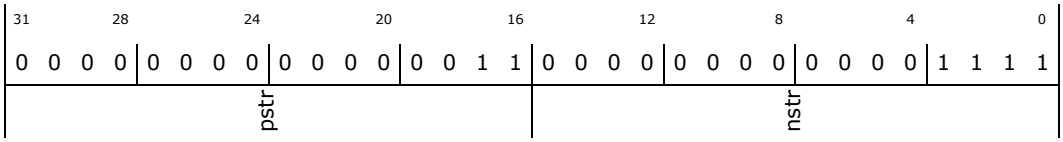
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_spkr_STRENGTH: [IOBASE] + 890h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.422 Ssp Strength Group (cfio_regs_ssp_STRENGTH)—Offset 894h

P and N strength register

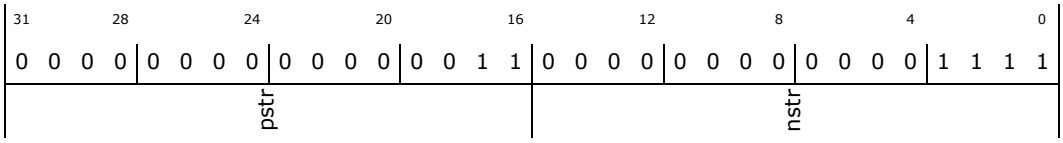
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_ssp_STRENGTH: [IOBASE] + 894h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.423 Uart1 Strength Group (cfio_regs_uart1_STRENGTH)—Offset 898h

P and N strength register

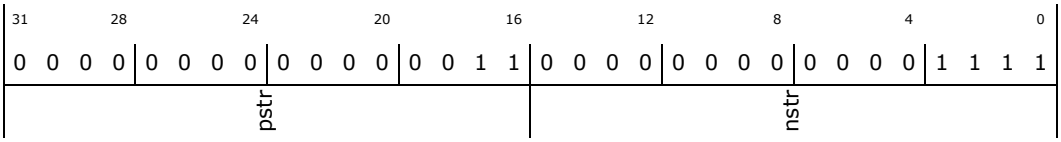
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_uart1_STRENGTH: [IOBASE] + 898h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.67.424 Aza1 Electrical Group (cfio_regs_aza1_ELECTRICAL)—Offset 89Ch

Electrical register includes slew and static values

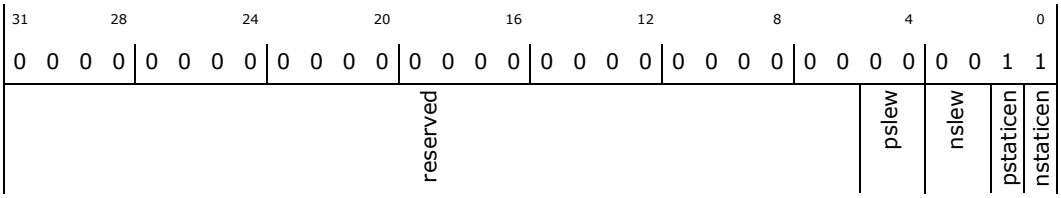
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_aza1_ELECTRICAL: [IOBASE] + 89Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.425 Aza2 Electrical Group (cfio_regs_aza2_ELECTRICAL)—Offset 8A0h

Electrical register includes slew and static values

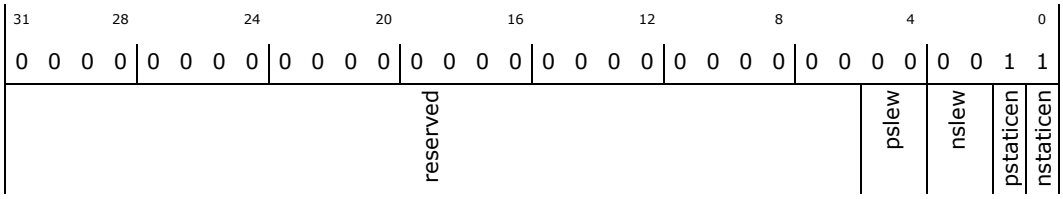
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_aza2_ELECTRICAL: [IOBASE] + 8A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.426 Clkreq Electrical Group (cfio_regs_clkreq_ELECTRICAL)—Offset 8A4h

Electrical register includes slew and static values

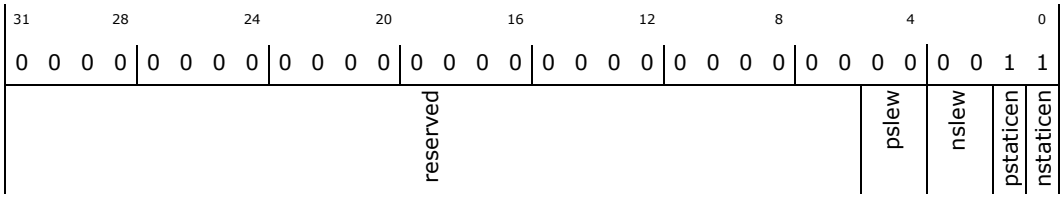
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_clkreq_ELECTRICAL: [IOBASE] + 8A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.427 Crt Electrical Group (cfio_regs_crt_ELECTRICAL)—Offset 8A8h

Electrical register includes slew and static values

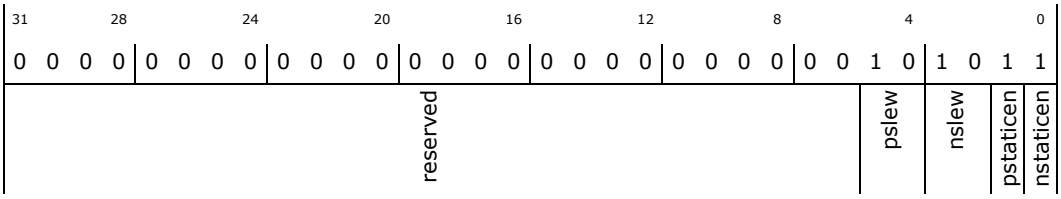
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_crt_ELECTRICAL: [IOBASE] + 8A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0000002Bh



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	10b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	10b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.428 Crt I2c Clk Electrical Group (cfio_regs_crt_i2c_clk_ELECTRICAL)—Offset 8ACh

Electrical register includes slew and static values

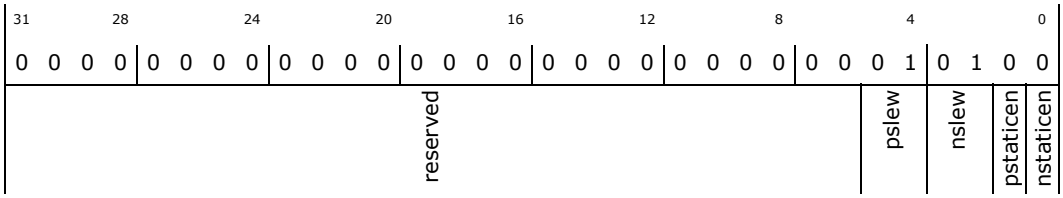
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_crt_i2c_clk_ELECTRICAL: [IOBASE] + 8ACh

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000014h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	01b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	01b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	0b RO	**Pstaticen (pstaticen):** enable positive static
0	0b RO	**Nstaticen (nstaticen):** enable negative static

3.67.429 Crt I2c Data Electrical Group (cfio_regs_crt_i2c_data_ELECTRICAL)—Offset 8B0h

Electrical register includes slew and static values

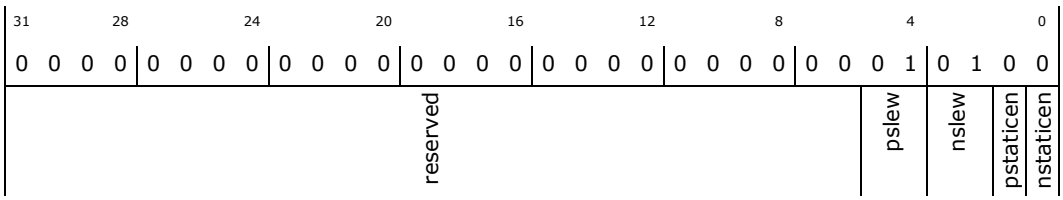
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_crt_i2c_data_ELECTRICAL: [IOBASE] + 8B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000014h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	01b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	01b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	0b RO	**Pstaticen (pstaticen):** enable positive static
0	0b RO	**Nstaticen (nstaticen):** enable negative static

3.67.430 Hsi Electrical Group (cfio_regs_hsi_ELECTRICAL)—Offset 8B4h

Electrical register includes slew and static values

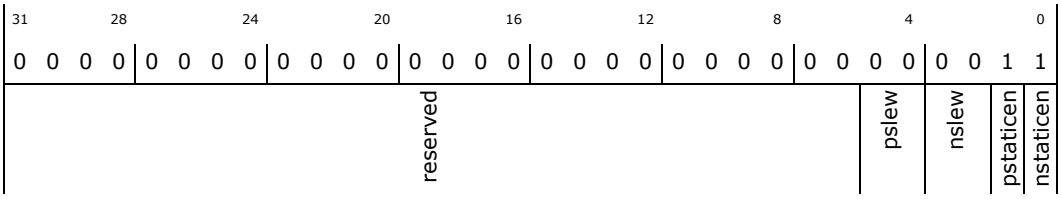
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_hsi_ELECTRICAL: [IOBASE] + 8B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.431 I2c Electrical Group (cfio_regs_i2c_ELECTRICAL)—Offset 8B8h

Electrical register includes slew and static values

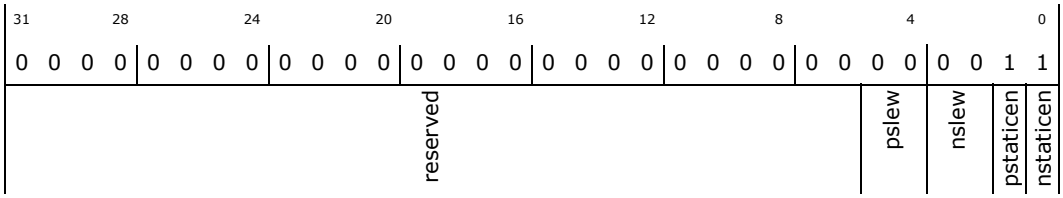
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_i2c_ELECTRICAL: [IOBASE] + 8B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.432 Lpc Electrical Group (cfio_regs_lpc_ELECTRICAL)—Offset 8BCh

Electrical register includes slew and static values

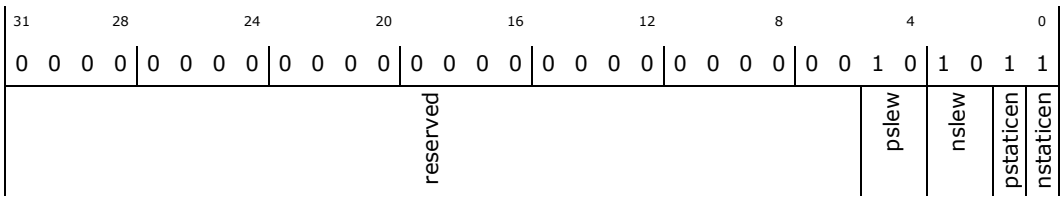
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_lpc_ELECTRICAL: [IOBASE] + 8BCh

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0000002Bh



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	10b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	10b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.433 Mmc1 Electrical Group (cfio_regs_mmc1_ELECTRICAL)—Offset 8C0h

Electrical register includes slew and static values

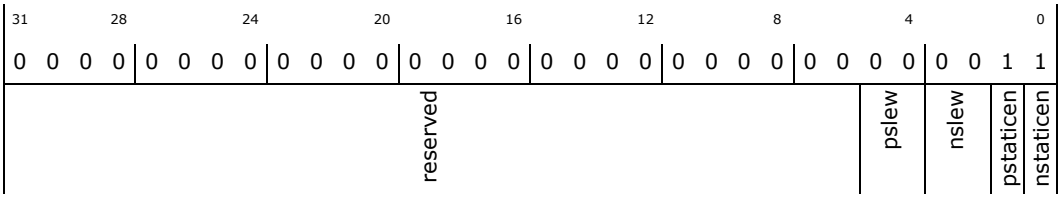
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_mmc1_ELECTRICAL: [IOBASE] + 8C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.434 Mmc1 Clk Electrical Group (cfio_regs_mmc1_clk_ELECTRICAL)—Offset 8C4h

Electrical register includes slew and static values

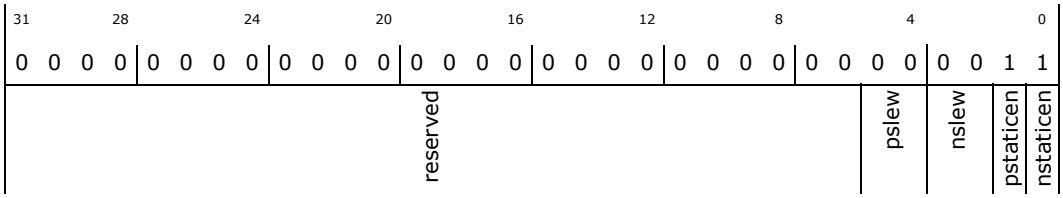
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_mmc1_clk_ELECTRICAL: [IOBASE] + 8C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.435 Mmc2 Electrical Group (cfio_regs_mmc2_ELECTRICAL)—Offset 8C8h

Electrical register includes slew and static values

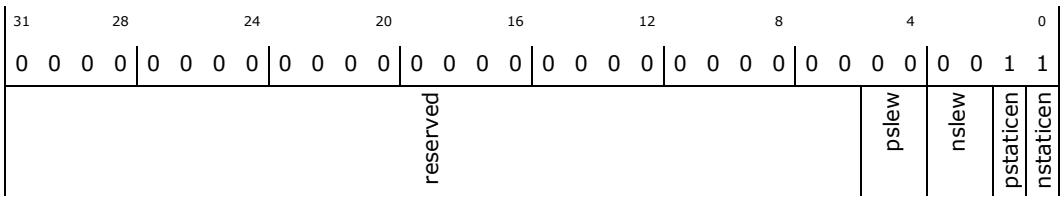
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_mmc2_ELECTRICAL: [IOBASE] + 8C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.436 Mmc3 Electrical Group (cfio_regs_mmc3_ELECTRICAL)—Offset 8CCh

Electrical register includes slew and static values

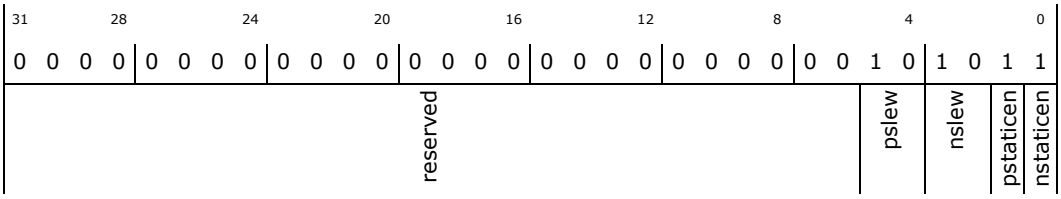
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_mmc3_ELECTRICAL: [IOBASE] + 8CCh

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0000002Bh



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	10b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	10b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.437 Mmc3 Cd Electrical Group (cfio_regs_mmc3_cd_ELECTRICAL)—Offset 8D0h

Electrical register includes slew and static values

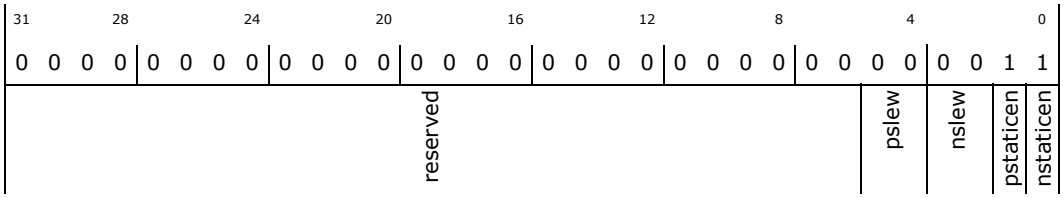
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_mmc3_cd_ELECTRICAL: [IOBASE] + 8D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.438 Mvt Mmc3 Electrical Group (cfio_regs_mvt_mmc3_ELECTRICAL)—Offset 8D4h

Electrical register includes slew and static values

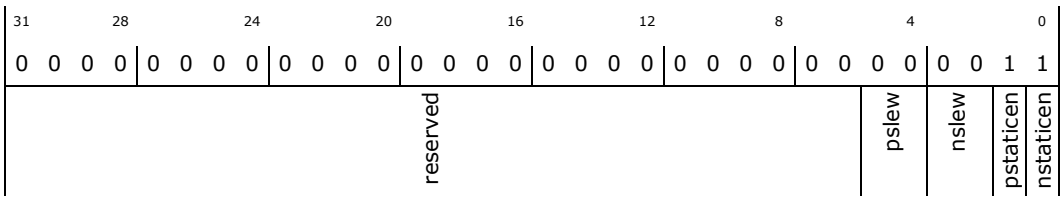
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_mvt_mmc3_ELECTRICAL: [IOBASE] + 8D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.439 Nfc Electrical Group (cfio_regs_nfc_ELECTRICAL)—Offset 8D8h

Electrical register includes slew and static values

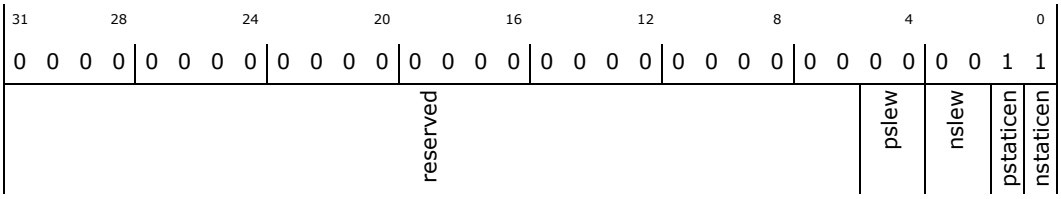
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_nfc_ELECTRICAL: [IOBASE] + 8D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.440 Pltclk Electrical Group (cfio_regs_pltclk_ELECTRICAL)—Offset 8DCh

Electrical register includes slew and static values

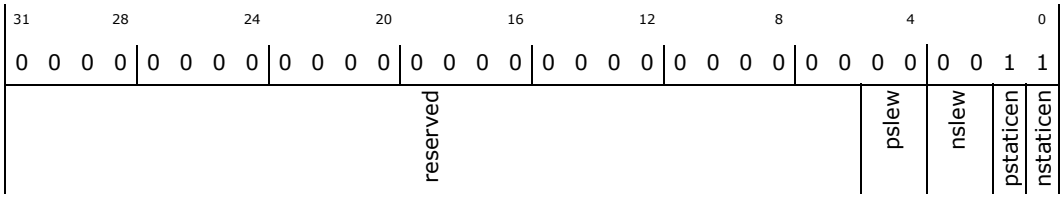
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pltclk_ELECTRICAL: [IOBASE] + 8DCh

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.441 Pwm Electrical Group (cfio_regs_pwm_ELECTRICAL)—Offset 8E0h

Electrical register includes slew and static values

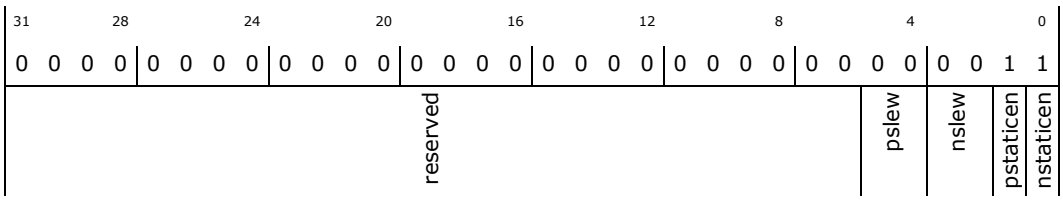
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pwm_ELECTRICAL: [IOBASE] + 8E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.442 Sata Electrical Group (cfio_regs_sata_ELECTRICAL)—Offset 8E4h

Electrical register includes slew and static values

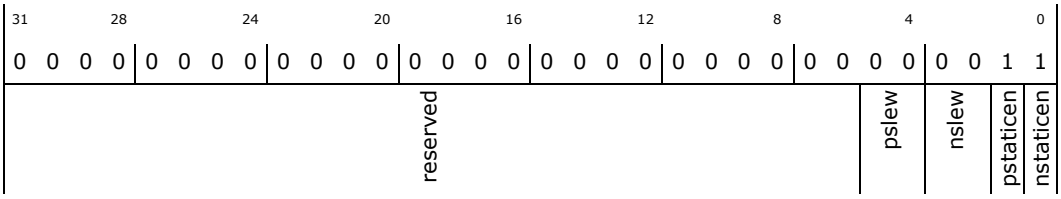
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sata_ELECTRICAL: [IOBASE] + 8E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.443 Smb Electrical Group (cfio_regs_smb_ELECTRICAL)—Offset 8E8h

Electrical register includes slew and static values

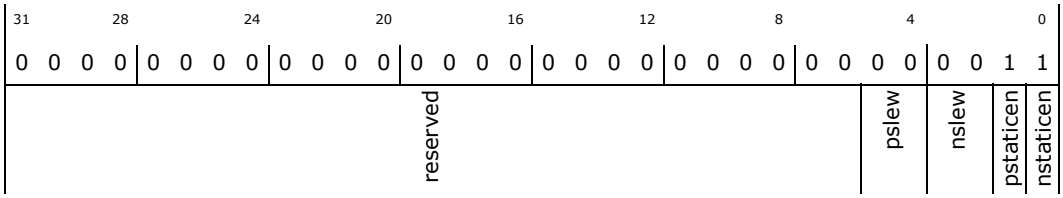
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_smb_ELECTRICAL: [IOBASE] + 8E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.444 Spi Electrical Group (cfio_regs_spi_ELECTRICAL)—Offset 8ECh

Electrical register includes slew and static values

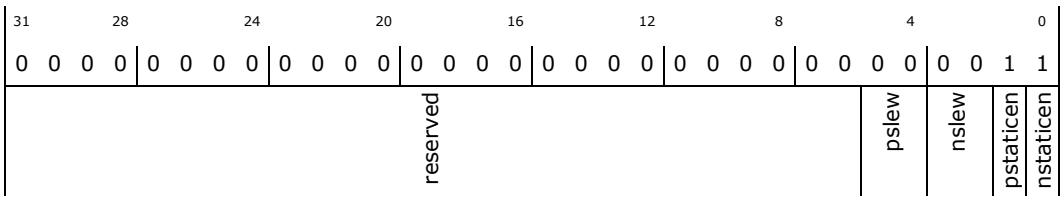
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_spi_ELECTRICAL: [IOBASE] + 8ECh

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.445 Spkr Electrical Group (cfio_regs_spkr_ELECTRICAL)—Offset 8F0h

Electrical register includes slew and static values

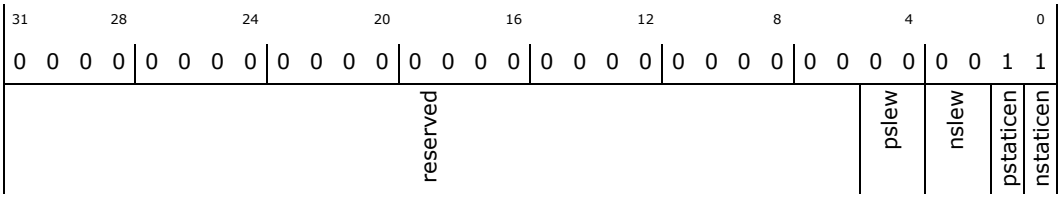
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_spkr_ELECTRICAL: [IOBASE] + 8F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.446 Ssp Electrical Group (cfio_regs_ssp_ELECTRICAL)—Offset 8F4h

Electrical register includes slew and static values

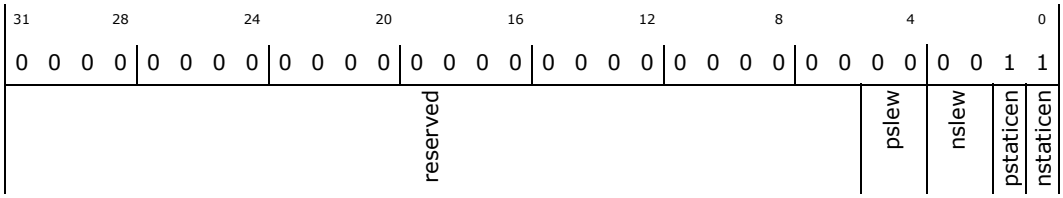
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_ssp_ELECTRICAL: [IOBASE] + 8F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.447 Uart1 Electrical Group (cfio_regs_uart1_ELECTRICAL)—Offset 8F8h

Electrical register includes slew and static values

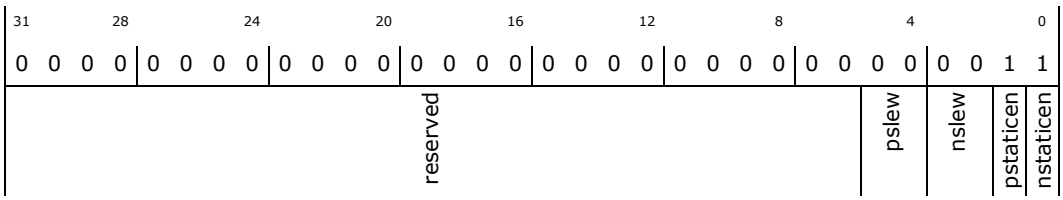
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_uart1_ELECTRICAL: [IOBASE] + 8F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.448 Uart2 Electrical Group (cfio_regs_uart2_ELECTRICAL)—Offset 8FCh

Electrical register includes slew and static values

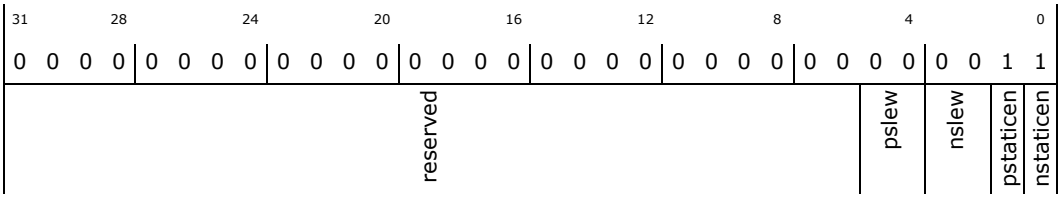
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_uart2_ELECTRICAL: [IOBASE] + 8FCh

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.67.449 CFG SCORE PSB Configuration (cfio_regs_COM_CFG_SCORE_PB_CONFIG)—Offset 900h

PSB configuration register for setup and hold times configuration.

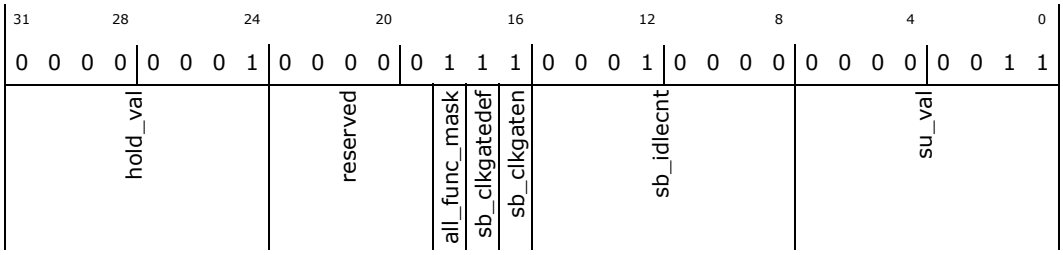
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_COM_CFG_SCORE_PB_CONFIG: [IOBASE] + 900h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01071003h



Bit Range	Default & Access	Description
31:24	01h RW	**Hold Val (hold_val):** Hold Value - number of cycles to for hold.
23:19	00000b RO	**Reserved (reserved):** reserved
18	1b RW	**All Func Mask (all_func_mask):** all_func_mask - masking the functional function select for south cfio, reserved for north use
17	1b RW	**Sb Clkgatedef (sb_clkgatedef):** Sideband clock gate default
16	1b RW	**Sb Clkgaten (sb_clkgaten):** Sideband clock gate enable
15:8	10h RW	**Sb Idlecnt (sb_idlecnt):** Sideband idle count
7:0	03h RW	**Su Val (su_val):** Setup Value - number of cycles to for setup.

3.67.450 IRQ TYPE SCORE Interrupt Type (cfio_regs_REG_IRQ_TYPE_SCORE_IRQ_TYPE)—Offset 904h

IRQ TYPE register

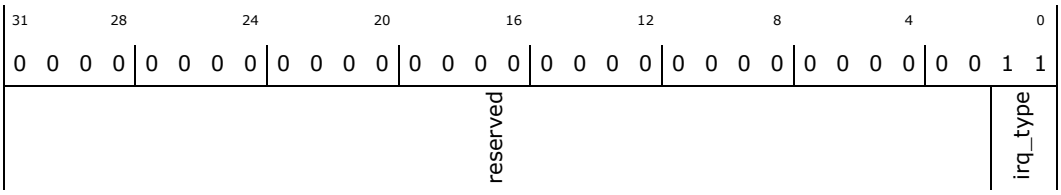
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_IRQ_TYPE_SCORE_IRQ_TYPE: [IOBASE] + 904h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved (reserved):** reserved
1:0	11b RO	**Irq Type (irq_type):** IRQ message type. This field defines the IRQ message type that community will send to ILB 00 =) IRQ5 opcode assert = C0, deassert = C1 01 =) IRQ6 opcode assert = C2, deassert = C3 10 =) IRQ7 opcode assert = CE, deassert = CF 11 =) IRQ13 opcode assert = D2, deassert = D3 - reserved, unused in VLV2

3.67.451 WR PATH SCORE Master Delay Line Write Address (cfio_regs_DLL_WR_PATH_SCORE_MDL_WRITE_PATH_C_F_ADDR)—Offset 950h

Master delay line write path values

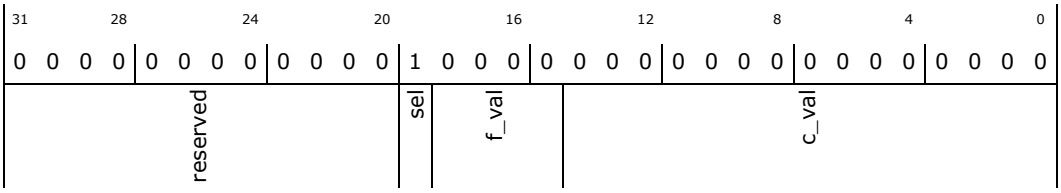
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_WR_PATH_SCORE_MDL_WRITE_PATH_C_F_ADDR: [IOBASE] + 950h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00080000h



Bit Range	Default & Access	Description
31:20	000h RO	**Reserved (reserved):** reserved
19	1b RW	**Sel (sel):** DLL f_c select
18:15	0000b RW	**F Val (f_val):** write path f value
14:0	0h RW	**C Val (c_val):** write path c value

3.67.452 WR PATH1 MUX SCORE Delay Line Write Multiplexer 1 (cfio_regs_DLL_WR_PATH1_MUX_SCORE_DLL_WRITE_PATH1_MUX)—Offset 954h

Master delay line write path mux values

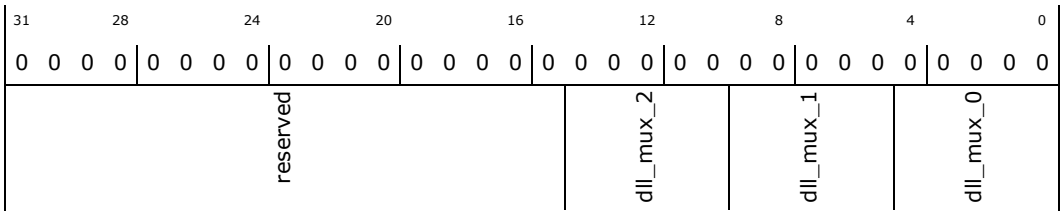
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_WR_PATH1_MUX_SCORE_DLL_WRITE_PATH1_MUX: [IOBASE] + 954h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RO	**Reserved (reserved):** reserved
14:10	0h RW	**Dll Mux 2 (dll_mux_2):** mux select 2 for dll
9:5	0h RW	**Dll Mux 1 (dll_mux_1):** mux select 1 for dll
4:0	0h RW	**Dll Mux 0 (dll_mux_0):** mux select 0 for dll

3.67.453 WR PATH2 MUX SCORE Delay Line Write Multiplexer 2 (cfio_regs_DLL_WR_PATH2_MUX_SCORE_DLL_WRITE_PATH2_MUX)—Offset 958h

Master delay line write path mux values

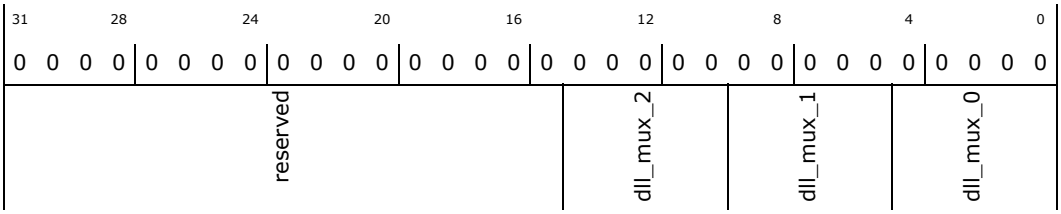
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_WR_PATH2_MUX_SCORE_DLL_WRITE_PATH2_MUX: [IOBASE] + 958h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RO	**Reserved (reserved):** reserved
14:10	0h RW	**Dll Mux 2 (dll_mux_2):** mux select 2 for dll
9:5	0h RW	**Dll Mux 1 (dll_mux_1):** mux select 1 for dll
4:0	0h RW	**Dll Mux 0 (dll_mux_0):** mux select 0 for dll

3.67.454 WR PATH3 MUX SCORE Delay Line Write Multiplexer 3 (cfio_regs_DLL_WR_PATH3_MUX_SCORE_DLL_WRITE_PATH3_MUX)—Offset 95Ch

Master delay line write path mux values

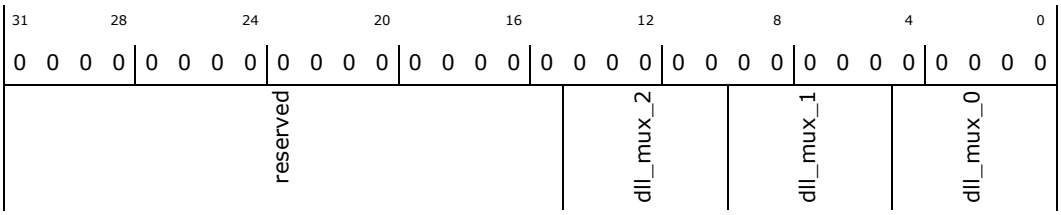
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_WR_PATH3_MUX_SCORE_DLL_WRITE_PATH3_MUX: [IOBASE] + 95Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RO	**Reserved (reserved):** reserved
14:10	0h RW	**Dll Mux 2 (dll_mux_2):** mux select 2 for dll
9:5	0h RW	**Dll Mux 1 (dll_mux_1):** mux select 1 for dll

Bit Range	Default & Access	Description
4:0	0h RW	**Dll Mux 0 (dll_mux_0):** mux select 0 for dll

3.67.455 FIFO SCORE Emmc Fifo Control (cfio_regs_EMMC_FIFO_SCORE_EMMC_FIFO)—Offset 960h

EMMC fifo controller

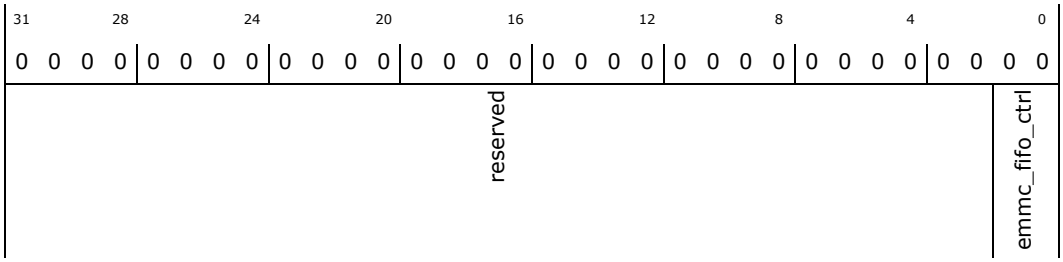
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_EMMC_FIFO_SCORE_EMMC_FIFO: [IOBASE] + 960h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved (reserved):** reserved
1:0	00b RW	**Emmc Fifo Ctrl (emmc_fifo_ctrl):** reserved

3.67.456 INIT SCORE Master Delay Line Initial Values (cfio_regs_DLL_INIT_SCORE_MDL_CF_INIT)—Offset 964h

Master delay line c and f init values

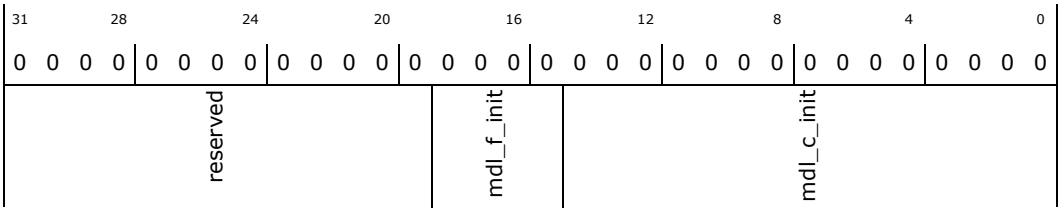
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_INIT_SCORE_MDL_CF_INIT: [IOBASE] + 964h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0000h RO	**Reserved (reserved):** reserved
18:15	0h RW	**Mdl F Init (mdl_f_init):** Master delay f init value
14:0	0000h RW	**Mdl C Init (mdl_c_init):** Master delay c init value

3.67.457 SW MODE SCORE Master Delay Line Software Values (cfio_regs_DLL_SW_MODE_SCORE_MDL_CF_SW)—Offset 968h

Master delay line c and f software values

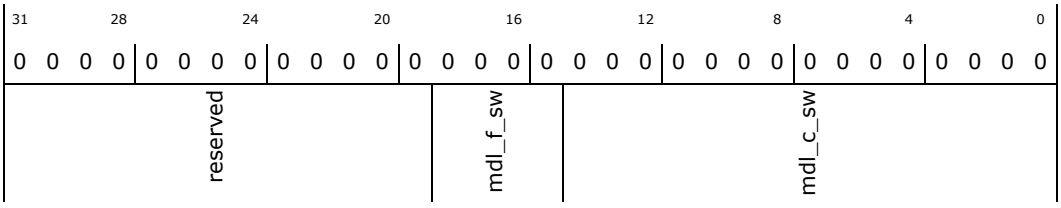
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_SW_MODE_SCORE_MDL_CF_SW: [IOBASE] + 968h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0000h RO	**Reserved (reserved):** reserved
18:15	0h RW	**Mdl F Sw (mdl_f_sw):** Master delay f software value
14:0	0000h RW	**Mdl C Sw (mdl_c_sw):** Master delay c software value

3.67.458 VALS SCORE Master Delay Line Fsm Values (cfio_regs_DLL_VALS_SCORE_MDL_FSM_VALS)—Offset 96Ch

Master delay line fsm values

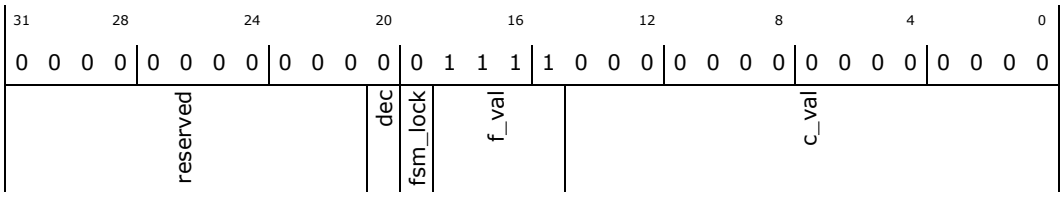
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_VALS_SCORE_MDL_FSM_VALS: [IOBASE] + 96Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078000h



Bit Range	Default & Access	Description
31:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Dec (dec):** fsm decrease
19	0b RO	**Fsm Lock (fsm_lock):** fsm lock
18:15	1111b RO	**F Val (f_val):** fsm f value
14:0	0h RO	**C Val (c_val):** fsm c value

3.67.459 CTRL SCORE Master Delay Line Fsm Control (cfio_regs_DLL_CTRL_SCORE_MDL_FSM_CTRL)—Offset 970h

Master delay line fsm controller

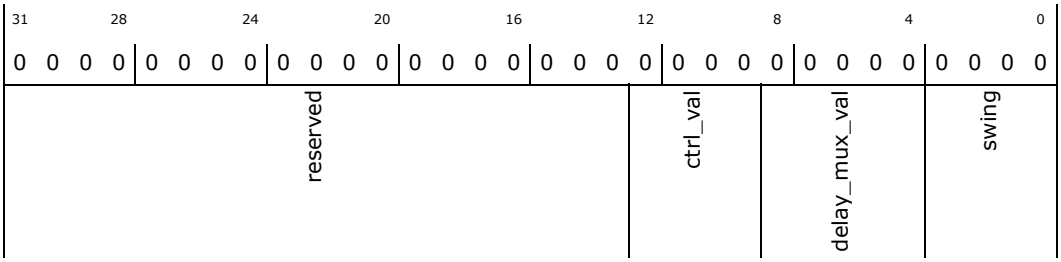
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_CTRL_SCORE_MDL_FSM_CTRL: [IOBASE] + 970h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:13	0h RO	**Reserved (reserved):** reserved
12:9	0b RW	**Ctrl Val (ctrl_val):** fsm control value
8:4	00000b RW	**Delay Mux Val (delay_mux_val):** fsm delay mux value
3:0	0000b RW	**Swing (swing):** swing value

3.67.460 DIRECT IRQ0 SCORE Direct Interrupt Multiplexer 0 (cfio_regs_REG_DIRECT_IRQ0_SCORE_DIRECT_IRQ_0)—Offset 980h

Direct irq select register for irq 0 - 3

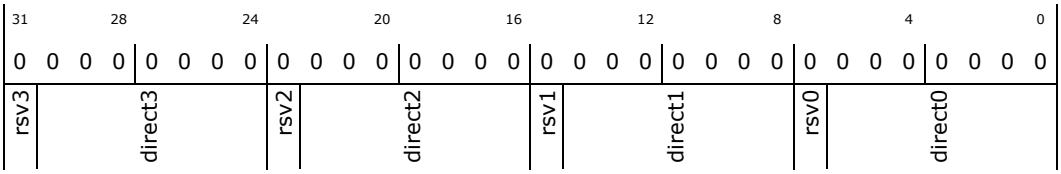
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_DIRECT_IRQ0_SCORE_DIRECT_IRQ_0: [IOBASE] + 980h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31	0b R0	**Rsv3 (rsv3):** reserved
30:24	0000000b RW	**Direct3 (direct3):** Selects the 4th direct irq
23	0b R0	**Rsv2 (rsv2):** reserved

Bit Range	Default & Access	Description
22:16	0000000b RW	**Direct2 (direct2):** Selects the 3th direct irq
15	0b R0	**Rsv1 (rsv1):** reserved
14:8	0000000b RW	**Direct1 (direct1):** Selects the 2nd direct irq
7	0b R0	**Rsv0 (rsv0):** reserved
6:0	0000000b RW	**Direct0 (direct0):** Selects the 1st direct irq

3.67.461 DIRECT IRQ1 SCORE Direct Interrupt Multiplexer 1 (cfio_regs_REG_DIRECT_IRQ1_SCORE_DIRECT_IRQ_1)—Offset 984h

Direct irq select register for irq 4 - 7

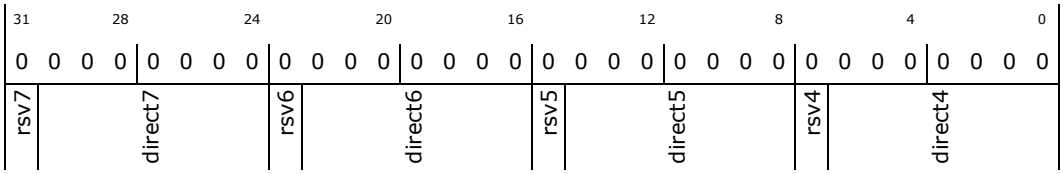
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_DIRECT_IRQ1_SCORE_DIRECT_IRQ_1: [IOBASE] + 984h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31	0b R0	**Rsv7 (rsv7):** reserved
30:24	0000000b RW	**Direct7 (direct7):** Selects the 8th direct irq
23	0b R0	**Rsv6 (rsv6):** reserved
22:16	0000000b RW	**Direct6 (direct6):** Selects the 7th direct irq
15	0b R0	**Rsv5 (rsv5):** reserved
14:8	0000000b RW	**Direct5 (direct5):** Selects the 5th direct irq
7	0b R0	**Rsv4 (rsv4):** reserved

Bit Range	Default & Access	Description
6:0	0000000b RW	**Direct4 (direct4):** Selects the 4th direct irq

3.67.462 DIRECT IRQ2 SCORE Direct Interrupt Multiplexer 2 (cfio_regs_REG_DIRECT_IRQ2_SCORE_DIRECT_IRQ_2)—Offset 988h

Direct irq select register for irq 8 - 11

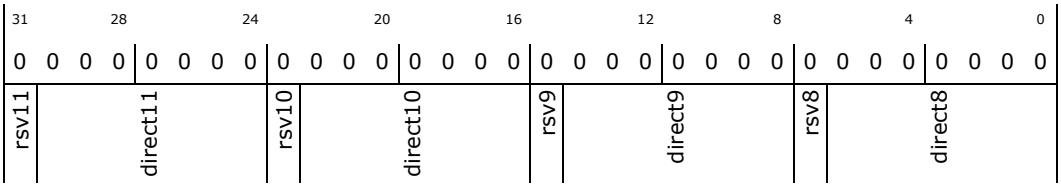
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_DIRECT_IRQ2_SCORE_DIRECT_IRQ_2: [IOBASE] + 988h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31	0b R0	**Rsv11 (rsv11):** reserved
30:24	0000000b RW	**Direct11 (direct11):** Selects the 11th direct irq
23	0b R0	**Rsv10 (rsv10):** reserved
22:16	0000000b RW	**Direct10 (direct10):** Selects the 10th direct irq
15	0b R0	**Rsv9 (rsv9):** reserved
14:8	0000000b RW	**Direct9 (direct9):** Selects the 9th direct irq
7	0b R0	**Rsv8 (rsv8):** reserved
6:0	0000000b RW	**Direct8 (direct8):** Selects the 8th direct irq

3.67.463 DIRECT IRQ3 SCORE Direct Interrupt Multiplexer 3 (cfio_regs_REG_DIRECT_IRQ3_SCORE_DIRECT_IRQ_3)—Offset 98Ch

Direct irq select register for irq 12 - 15

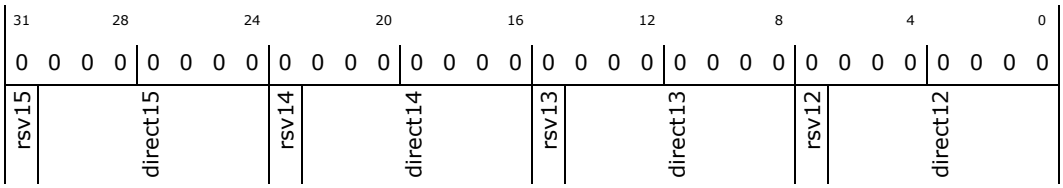
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_DIRECT_IRQ3_SCORE_DIRECT_IRQ_3: [IOBASE] + 98Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31	0b R0	**Rsv15 (rsv15):** reserved
30:24	0000000b RW	**Direct15 (direct15):** Selects the 15th direct irq
23	0b R0	**Rsv14 (rsv14):** reserved
22:16	0000000b RW	**Direct14 (direct14):** Selects the 14th direct irq
15	0b R0	**Rsv13 (rsv13):** reserved
14:8	0000000b RW	**Direct13 (direct13):** Selects the 13th direct irq
7	0b R0	**Rsv12 (rsv12):** reserved
6:0	0000000b RW	**Direct12 (direct12):** Selects the 12th direct irq

3.67.464 E eMMC 4.5 delay control register (cfio_regs_SCORE_EMMC_45_DLY_CTRL)—Offset 9A0h

Shift DLL building blocks count to start from 8 instead of 0

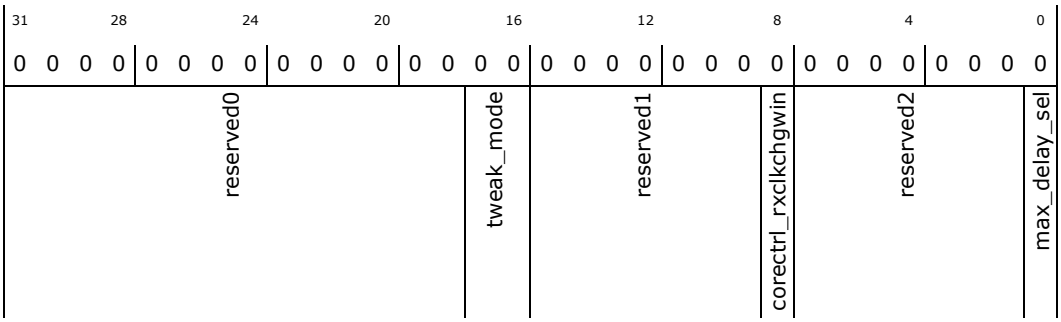
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_SCORE_EMMC_45_DLY_CTRL: [IOBASE] + 9A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:18	0h RO	**Reserved0 (reserved0):** reserved
17:16	0h RW	**Tweak Mode (tweak_mode):** 0 - no tweak, 1 - add value to strength, 2 - substract values to strength, 3 - unknown
15:9	0h RO	**Reserved1 (reserved1):** reserved
8	0b RW	**Corectrl Rxclkchgwin (corectrl_rxclkchgwin):** This bit is used to gate the Rx Clock while the delay value is changing
7:1	0h RO	**Reserved2 (reserved2):** reserved
0	0b RW	**Max Delay Sel (max_delay_sel):** When set, the DLL building block delay value will be shifted from 0 - 31 to 8 - 39. Must be cleared, software should not set this bit.

3.67.465 E Emmc 4.5 max high speed mux (cfio_regs_SCORE_EMMC_45_HSMAX)—Offset 9A4h

Setting the DLL mux when highest speed is selected

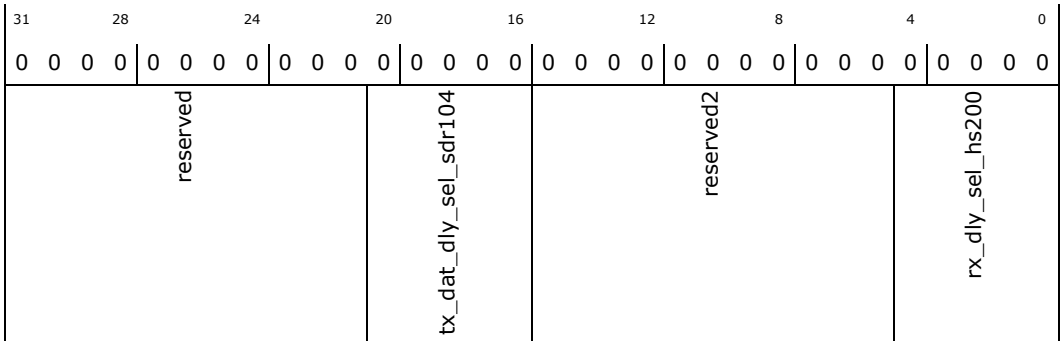
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_SCORE_EMMC_45_HSMAX: [IOBASE] + 9A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:21	0h RO	**Reserved (reserved):** reserved
20:16	0b RW	**Tx Dat Dly Sel Sdr104 (tx_dat_dly_sel_sdr104):** Set the tx delay for sdr104
15:5	0h RO	**Reserved2 (reserved2):** reserved
4:0	0b RW	**Rx Dly Sel Hs200 (rx_dly_sel_hs200):** Set the rx delay for hs200

3.67.466 E Emmc 4.5 sdr50 speed mux (cfio_regs_SCORE_EMMC_45_SDR50)—Offset 9A8h

Setting the DLL mux when sdr50 speed is selected

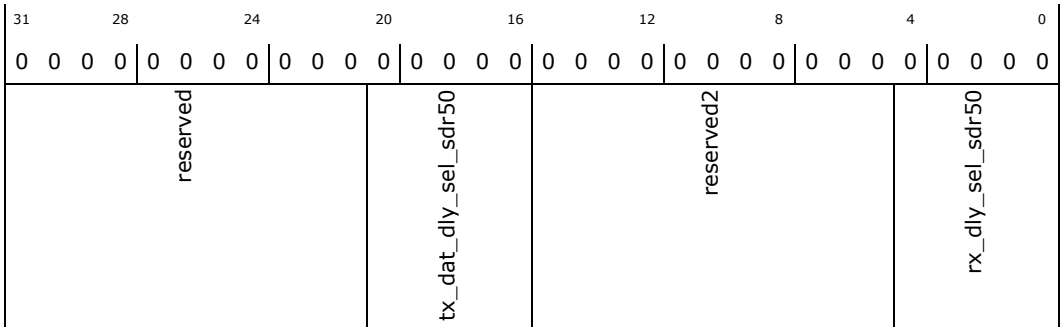
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_SCORE_EMMC_45_SDR50: [IOBASE] + 9A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:21	0h RO	**Reserved (reserved):** reserved
20:16	0b RW	**Tx Dat Dly Sel Sdr50 (tx_dat_dly_sel_sdr50):** Set the tx delay for sdr50
15:5	0h RO	**Reserved2 (reserved2):** reserved
4:0	0b RW	**Rx Dly Sel Sdr50 (rx_dly_sel_sdr50):** Set the rx delay for sdr50

3.67.467 E Emmc 4.5 ddr50 speed mux (cfio_regs_SCORE_EMMC_45_DDR50)—Offset 9ACh

Setting the DLL mux when ddr50 speed is selected and 1.8v is used

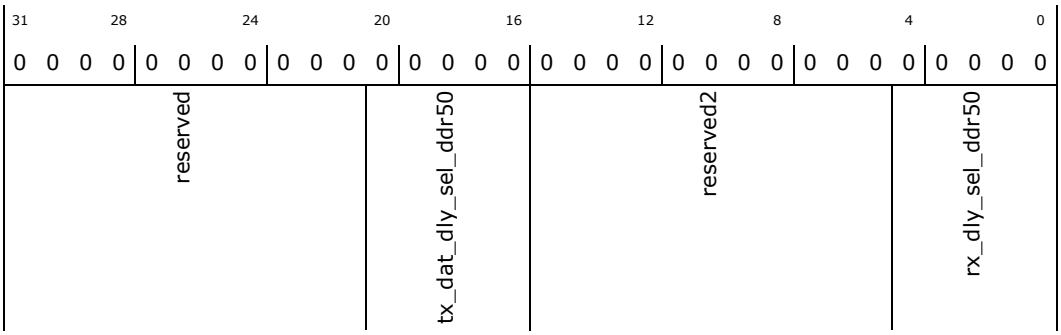
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_SCORE_EMMC_45_DDR50: [IOBASE] + 9ACh

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:21	0h RO	**Reserved (reserved):** reserved
20:16	0b RW	**Tx Dat Dly Sel Ddr50 (tx_dat_dly_sel_ddr50):** Set the tx delay for ddr50
15:5	0h RO	**Reserved2 (reserved2):** reserved
4:0	0b RW	**Rx Dly Sel Ddr50 (rx_dly_sel_ddr50):** Set the rx delay for ddr50

3.67.468 E Emmc 4.5 hs speed mux (cfio_regs_SCORE_EMMC_45_HS)—Offset 9B0h

Setting the DLL mux when 1. hs speed is selected or 2. ddr 50 and 1.8V Signaling Enable is set to 0. The SDMCC1 IO will still use 1.8V.

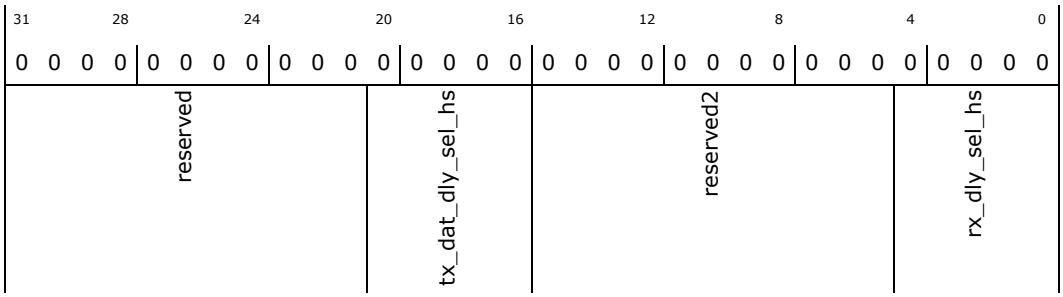
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_SCORE_EMMC_45_HS: [IOBASE] + 9B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:21	0h RO	**Reserved (reserved):** reserved
20:16	0b RW	**Tx Dat Dly Sel Hs (tx_dat_dly_sel_hs):** Set the tx delay for hs
15:5	0h RO	**Reserved2 (reserved2):** reserved
4:0	0b RW	**Rx Dly Sel Hs (rx_dly_sel_hs):** Set the rx delay for hs

3.67.469 E Emmc 4.5 norm speed mux (cfio_regs_SCORE_EMMC_45_NORM)—Offset 9B4h

Setting the DLL mux when norm speed is selected

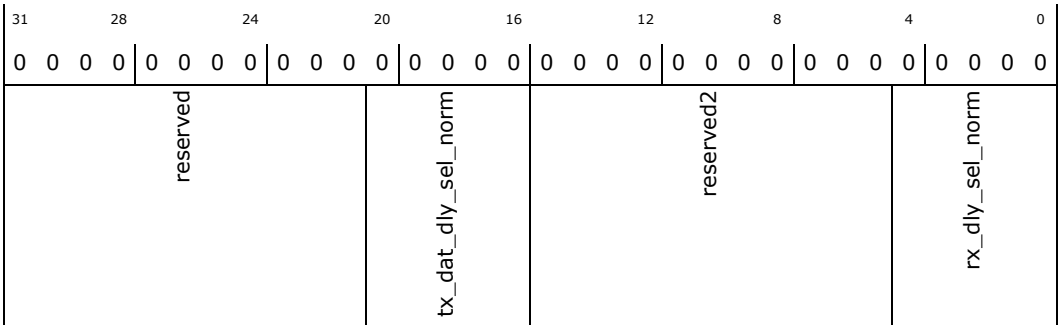
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_SCORE_EMMC_45_NORM: [IOBASE] + 9B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:21	0h RO	**Reserved (reserved):** reserved
20:16	0b RW	**Tx Dat Dly Sel Norm (tx_dat_dly_sel_norm):** Set the tx delay for norm
15:5	0h RO	**Reserved2 (reserved2):** reserved
4:0	0b RW	**Rx Dly Sel Norm (rx_dly_sel_norm):** Set the rx delay for norm

3.67.470 E Emmc 4.5 software override value (cfio_regs_SCORE_EMMC_45_OV)—Offset 9B8h

Overriding the coarse and fine tune values

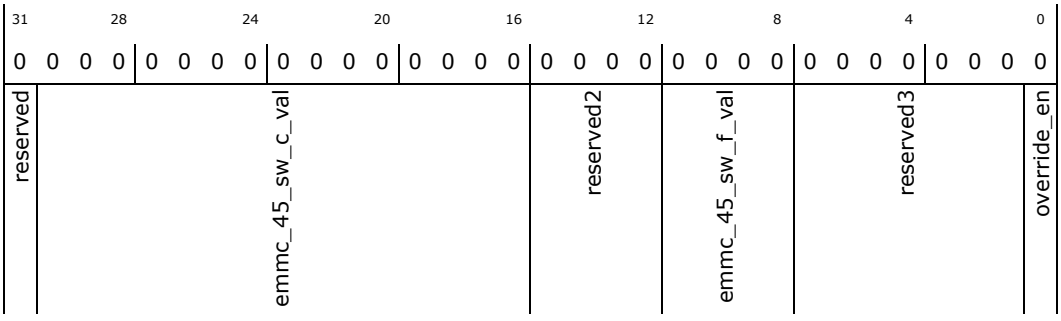
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_SCORE_EMMC_45_OV: [IOBASE] + 9B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RO	**Reserved (reserved):** reserved

Bit Range	Default & Access	Description
30:16	0b RW	**Emmc 45 Sw C Val (emmc_45_sw_c_val):** Set the software override value for coarse tuning
15:12	0h RO	**Reserved2 (reserved2):** reserved
11:8	0b RW	**Emmc 45 Sw F Val (emmc_45_sw_f_val):** Set the software override value for fine tuning
7:1	0h RO	**Reserved3 (reserved3):** reserved
0	0b RW	**Override En (override_en):** Enable software override

3.67.471 E Special configuration bits (cfio_regs_SCORE_SPECIAL_BITS)—Offset 9C0h

The register is holding enable bits for last minutes features, like Mipi hsi active and SDcard input disable when power down

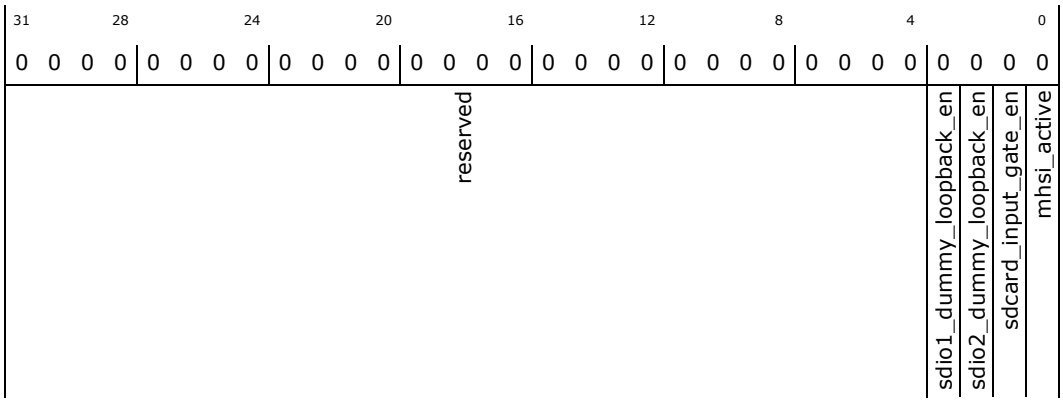
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_SCORE_SPECIAL_BITS: [IOBASE] + 9C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RO	**Reserved (reserved):** reserved
3	0b RW	**Sdio1 Dummy Loopback En (sdio1_dummy_loopback_en):** Enable dummy pad loopback to avoid board reflection, for eMMC (4.4.1 and 4.5)
2	0b RW	**Sdio2 Dummy Loopback En (sdio2_dummy_loopback_en):** Enable dummy pad loopback to avoid board reflection, for sdio

Bit Range	Default & Access	Description
1	0b RW	**Sdcard Input Gate En (sdcard_input_gate_en):** Enable input disable when sd card power is down. Affect SD card input pads only SDMMC3_D0 SDMMC3_D1 SDMMC3_D2 SDMMC3_D3 SDMMC3_CMD
0	0b RW	**Mhsi Active (mhsi_active):** When set, MIPI HSI is active. Otherwise LPSS can control SPI1_MOSI output enable

3.67.472 E Debounce Control (cfio_regs_SCORE_DEBOUNCE_CTRL)—Offset 9D0h

The register is controlling the community debounce

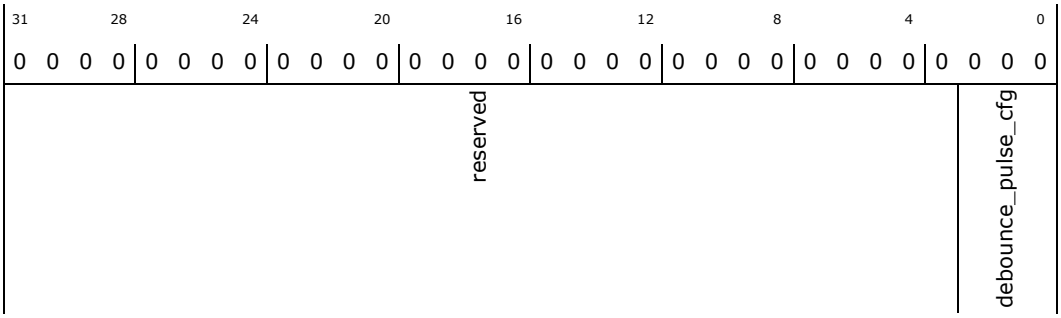
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_SCORE_DEBOUNCE_CTRL: [IOBASE] + 9D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RO	**Reserved (reserved):** reserved
2:0	0h RW	**Debounce Pulse Cfg (debounce_pulse_cfg):** This will divide the rtc clock, for generating the pulse of the debounce. When all cleared, pulse will be always high. 3'b001 375us debounce 3'b010 750us debounce 3'b011 1.5ms debounce 3'b100 3ms debounce 3'b101 6ms debounce 3'b110 12ms debounce 3'b111 24ms debounce Recommended values are between 3 to 12 ms

3.67.473 E eMMC 4.5 TAP select register (cfio_regs_SCORE_TAP_SEL_REG)—Offset 9F4h

The register is controlling the community debounce

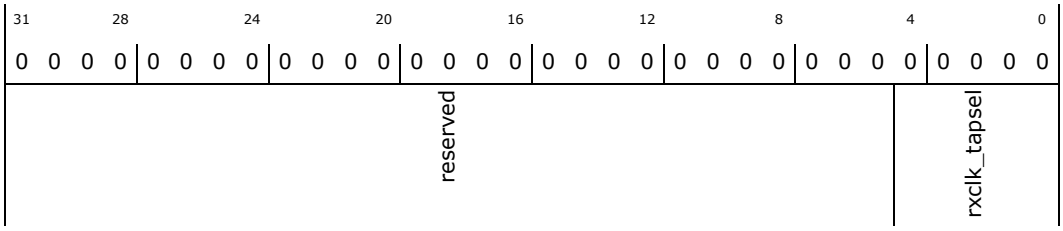
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

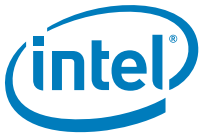
cfio_regs_SCORE_TAP_SEL_REG: [IOBASE] + 9F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:5	0h RW	**Reserved (reserved):** reserved
4:0	0h RO	**Rxclk Tapsel (rxclk_tapsel):** This is the actual tap select value for the rx clock of eMMC 4.5



3.68 PCU iLB GPIO CFIO_SSUS_IO Address Map

Table 76. Summary of PCU iLB GPIO IO Registers—GPIO_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"Sus Use Select 1 (cfio_ioreg_SUS_USE_SEL_31_0_)—Offset 0h" on page 3757	00000000h
4h	4	"Sus Io Select 1 (cfio_ioreg_SUS_IO_SEL_31_0_)—Offset 4h" on page 3758	00000000h
8h	4	"Sus Gpio Level 1 (cfio_ioreg_SUS_GP_LVL_31_0_)—Offset 8h" on page 3759	00000000h
Ch	4	"Sus Trigger Positive Edge Enable 1 (cfio_ioreg_SUS_TPE_31_0_)—Offset Ch" on page 3760	00000000h
10h	4	"Sus Trigger Negative Edge Enable 1 (cfio_ioreg_SUS_TNE_31_0_)—Offset 10h" on page 3760	00000000h
14h	4	"Sus Trigger Status 1 (cfio_ioreg_SUS_TS_31_0_)—Offset 14h" on page 3761	00000000h
18h	4	"Sus Wake Enable 1 (cfio_ioreg_SUS_WAKE_EN_31_0_)—Offset 18h" on page 3762	00000000h
20h	4	"Sus Use Select 2 (cfio_ioreg_SUS_USE_SEL_43_32_)—Offset 20h" on page 3763	00000000h
24h	4	"Sus Io Select 2 (cfio_ioreg_SUS_IO_SEL_43_32_)—Offset 24h" on page 3763	00000000h
28h	4	"Sus Gpio Level 2 (cfio_ioreg_SUS_GP_LVL_43_32_)—Offset 28h" on page 3764	00000000h
2Ch	4	"Sus Trigger Positive Edge Enable 2 (cfio_ioreg_SUS_TPE_43_32_)—Offset 2Ch" on page 3765	00000000h
30h	4	"Sus Trigger Negative Edge Enable 2 (cfio_ioreg_SUS_TNE_43_32_)—Offset 30h" on page 3765	00000000h
34h	4	"Sus Trigger Status (cfio_ioreg_SUS_TS_43_32_)—Offset 34h" on page 3766	00000000h
38h	4	"Sus Wake Enable 2 (cfio_ioreg_SUS_WAKE_EN_43_32_)—Offset 38h" on page 3767	00000000h

3.68.1 Sus Use Select 1 (cfio_ioreg_SUS_USE_SEL_31_0_)—Offset 0h

Access via PCU Proxy, the register is setting the corresponding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[0], and bit 1 will set GPIO[1] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

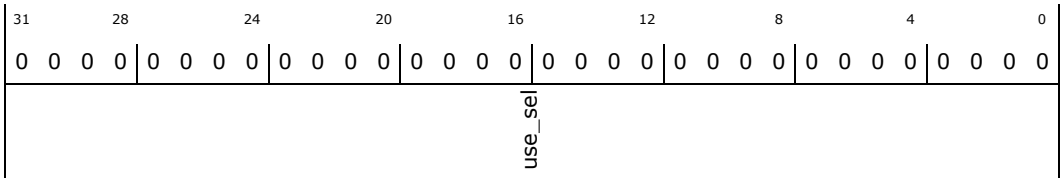
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_USE_SEL_31_0_: [GBASE + 0080h] + 0h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Use Select (use_sel):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

3.68.2 Sus Io Select 1 (cfio_ioreg_SUS_IO_SEL_31_0_)—Offset 4h

Access via PCU Proxy, it defines Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

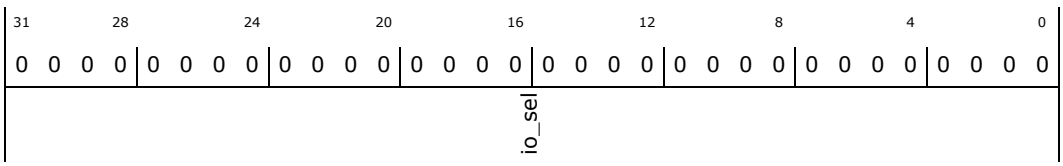
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_IO_SEL_31_0_: [GBASE + 0080h] + 4h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Io Select (io_sel):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

3.68.3 Sus Gpio Level 1 (cfio_ioreg_SUS_GP_LVL_31_0_)—Offset 8h

Access via PCU Proxy, the registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

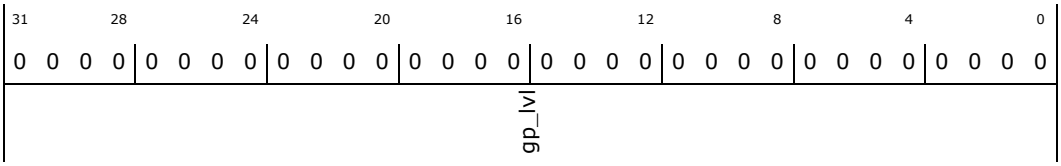
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_GP_LVL_31_0_: [GBASE + 0080h] + 8h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h WO	**Gpio Level (gp_lvl):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

3.68.4 Sus Trigger Positive Edge Enable 1 (cfio_ioreg_SUS_TPE_31_0_)—Offset Ch

Access via PCU Proxy, the register trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

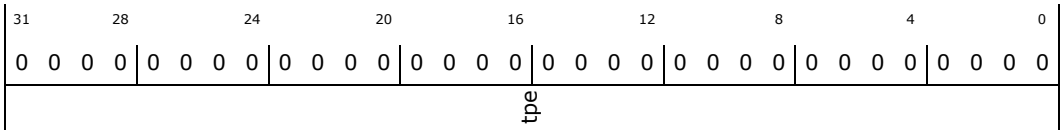
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_TPE_31_0_: [GBASE + 0080h] + Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Tpe (tpe):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

3.68.5 Sus Trigger Negative Edge Enable 1 (cfio_ioreg_SUS_TNE_31_0_)—Offset 10h

Access via PCU Proxy, the register trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

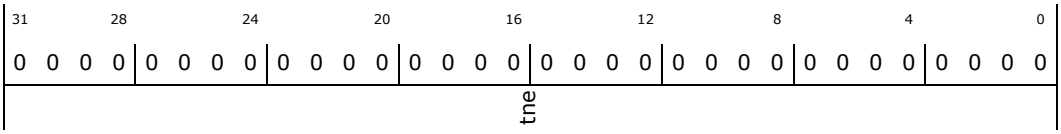
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_TNE_31_0_: [GBASE + 0080h] + 10h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Tne (tne):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

3.68.6 Sus Trigger Status 1 (cfio_ioreg_SUS_TS_31_0_)—Offset 14h

Access via PCU Proxy, When set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV and it cannot be tested by the host

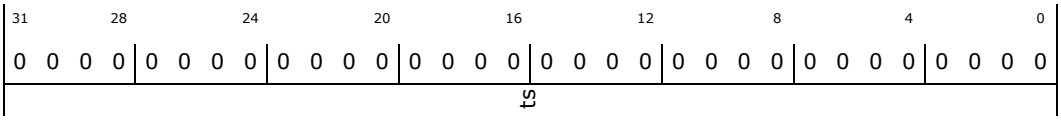
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_TS_31_0_: [GBASE + 0080h] + 14h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h WOC	**Ts (ts):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

3.68.7 Sus Wake Enable 1 (cfio_ioreg_SUS_WAKE_EN_31_0_)—Offset 18h

Access via PCU Proxy, Wake Enable: When set to a 1 and TS(n) is set, wake event should be initiated. - Only the 8 lsb are used in VLV

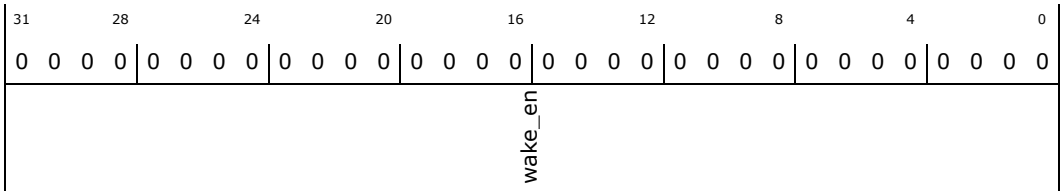
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_WAKE_EN_31_0_: [GBASE + 0080h] + 18h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Wake Enable (wake_en):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

3.68.8 Sus Use Select 2 (cfio_ioreg_SUS_USE_SEL_43_32_)—Offset 20h

Access via PCU Proxy, the register is setting the corresponding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[0], and bit 1 will set GPIO[1] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

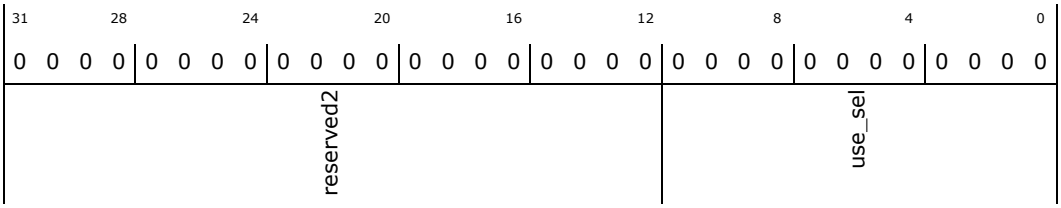
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_USE_SEL_43_32_: [GBASE + 0080h] + 20h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h RW	**Use Select (use_sel):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

3.68.9 Sus Io Select 2 (cfio_ioreg_SUS_IO_SEL_43_32_)—Offset 24h

Access via PCU Proxy, it defines Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

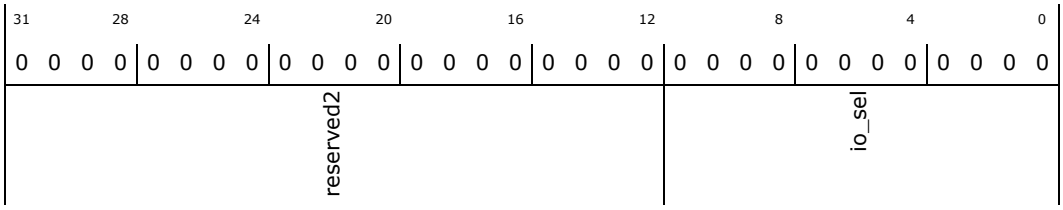
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_IO_SEL_43_32_: [GBASE + 0080h] + 24h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h RW	**Io Select (io_sel):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

3.68.10 Sus Gpio Level 2 (cfio_ioreg_SUS_GP_LVL_43_32_)—Offset 28h

This registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

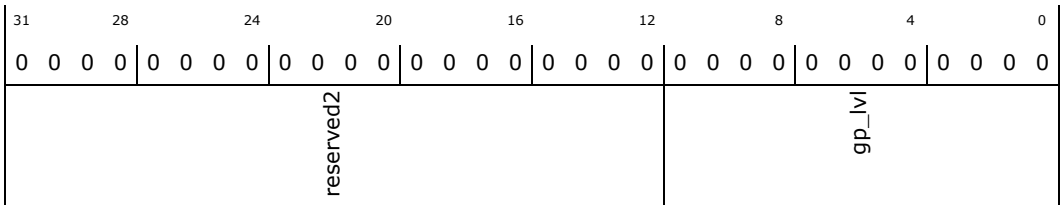
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_GP_LVL_43_32_: [GBASE + 0080h] + 28h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RO	**Reserved (reserved2):** Reserved.

Bit Range	Default & Access	Description
11:0	0h WO	**Gpio Level (gp_lvl):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

3.68.11 Sus Trigger Positive Edge Enable 2 (cfio_ioreg_SUS_TPE_43_32_)—Offset 2Ch

Access via PCU Proxy, the register trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

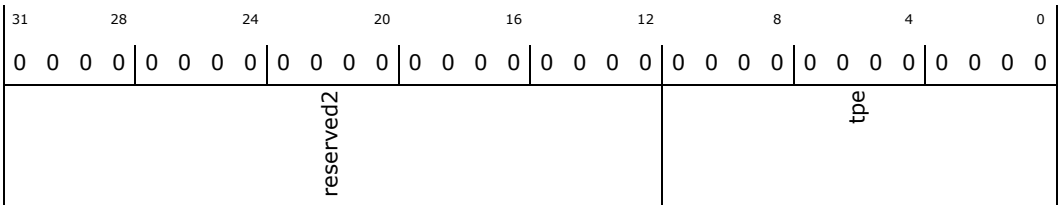
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_TPE_43_32_: [GBASE + 0080h] + 2Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h RW	**Tpe (tpe):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

3.68.12 Sus Trigger Negative Edge Enable 2 (cfio_ioreg_SUS_TNE_43_32_)—Offset 30h

Access via PCU Proxy, the register trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

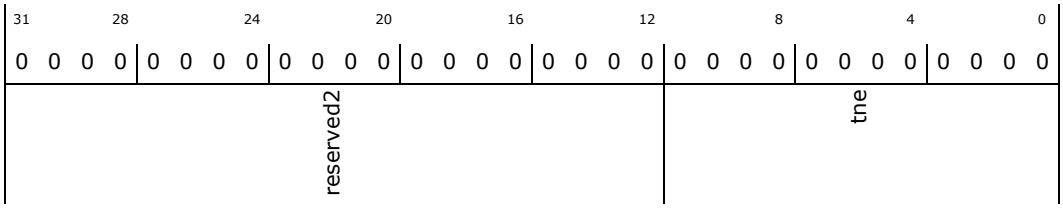
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_TNE_43_32_: [GBASE + 0080h] + 30h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h RW	**Tne (tne):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

3.68.13 Sus Trigger Status (cfio_ioreg_SUS_TS_43_32_)—Offset 34h

Access via PCU Proxy, When set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV

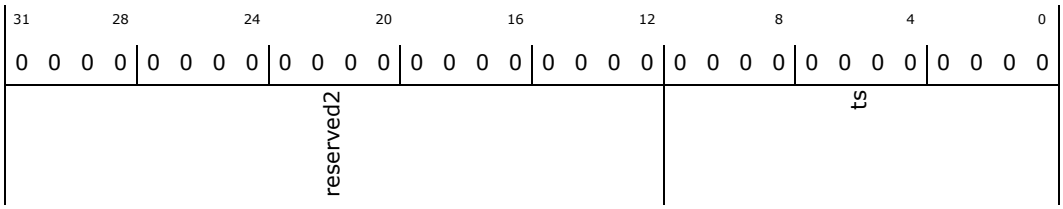
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_TS_43_32_: [GBASE + 0080h] + 34h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h WOC	**Ts (ts):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

3.68.14 Sus Wake Enable 2 (cfio_ioreg_SUS_WAKE_EN_43_32_)—Offset 38h

Access via PCU Proxy, When set to a 1 and TS(n) is set, wake event should be initiated. - Only the 8 lsb are used in VLV

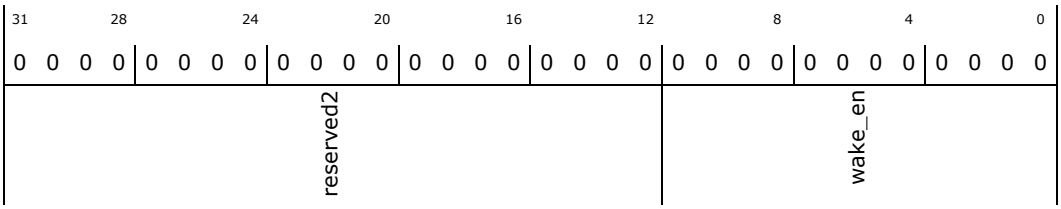
Access Method

Type: I/O Register (Size: 32 bits)

cfio_ioreg_SUS_WAKE_EN_43_32_: [GBASE + 0080h] + 38h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h RW	**Wake Enable (wake_en):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

3.69 PCU iLB GPIO CFIO_SSUS Address Map

Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"Usb Oc1 B Pad Configuration (cfio_regs_pad_usb_oc1_b_PCONF0)—Offset 0h" on page 3779	2003CC80h
4h	4	"Usb Oc1 B Delay Line Multiplexer (cfio_regs_pad_usb_oc1_b_PCONF1)—Offset 4h" on page 3781	00008000h
8h	4	"Usb Oc1 B Pad Value (cfio_regs_pad_usb_oc1_b_PAD_VAL)—Offset 8h" on page 3781	00000002h
10h	4	"Pmu Wake B Pad Configuration (cfio_regs_pad_pmu_wake_b_PCONF0)—Offset 10h" on page 3782	2003CC80h
14h	4	"Pmu Wake B Delay Line Multiplexer (cfio_regs_pad_pmu_wake_b_PCONF1)—Offset 14h" on page 3784	00008000h
18h	4	"Pmu Wake B Pad Value (cfio_regs_pad_pmu_wake_b_PAD_VAL)—Offset 18h" on page 3785	00000002h
20h	4	"Spi Cs1 B Pad Configuration (cfio_regs_pad_spi_cs1_b_PCONF0)—Offset 20h" on page 3786	2003EC80h
24h	4	"Spi Cs1 B Delay Line Multiplexer (cfio_regs_pad_spi_cs1_b_PCONF1)—Offset 24h" on page 3787	00008000h
28h	4	"Spi Cs1 B Pad Value (cfio_regs_pad_spi_cs1_b_PAD_VAL)—Offset 28h" on page 3788	00000002h
30h	4	"Spi Cs0 B Pad Configuration (cfio_regs_pad_spi_cs0_b_PCONF0)—Offset 30h" on page 3789	2003E800h
34h	4	"Spi Cs0 B Delay Line Multiplexer (cfio_regs_pad_spi_cs0_b_PCONF1)—Offset 34h" on page 3791	00008000h
38h	4	"Spi Cs0 B Pad Value (cfio_regs_pad_spi_cs0_b_PAD_VAL)—Offset 38h" on page 3792	00000002h
40h	4	"Spi Clk Pad Configuration (cfio_regs_pad_spi_clk_PCONF0)—Offset 40h" on page 3792	2003E800h
44h	4	"Spi Clk Delay Line Multiplexer (cfio_regs_pad_spi_clk_PCONF1)—Offset 44h" on page 3794	00008000h
48h	4	"Spi Clk Pad Value (cfio_regs_pad_spi_clk_PAD_VAL)—Offset 48h" on page 3795	00000002h
50h	4	"Spi Mosi Pad Configuration (cfio_regs_pad_spi_mosi_PCONF0)—Offset 50h" on page 3796	2003EC80h
54h	4	"Spi Mosi Delay Line Multiplexer (cfio_regs_pad_spi_mosi_PCONF1)—Offset 54h" on page 3797	00008000h
58h	4	"Spi Mosi Pad Value (cfio_regs_pad_spi_mosi_PAD_VAL)—Offset 58h" on page 3798	00000002h
60h	4	"Spi Miso Pad Configuration (cfio_regs_pad_spi_miso_PCONF0)—Offset 60h" on page 3799	2003EC80h

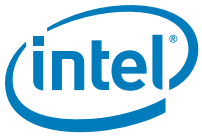


Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
64h	4	"Spi Miso Delay Line Multiplexer (cfio_regs_pad_spi_miso_PCONF1)—Offset 64h" on page 3801	00008000h
68h	4	"Spi Miso Pad Value (cfio_regs_pad_spi_miso_PAD_VAL)—Offset 68h" on page 3802	00000006h
70h	4	"Suspwrdnack Pad Configuration (cfio_regs_pad_suspwrdnack_PCONF0)—Offset 70h" on page 3802	2003CD00h
74h	4	"Suspwrdnack Delay Line Multiplexer (cfio_regs_pad_suspwrdnack_PCONF1)—Offset 74h" on page 3804	00008000h
78h	4	"Suspwrdnack Pad Value (cfio_regs_pad_suspwrdnack_PAD_VAL)—Offset 78h" on page 3805	00000002h
80h	4	"Pmu Pwrbtn B Pad Configuration (cfio_regs_pad_pmu_pwrbtn_b_PCONF0)—Offset 80h" on page 3806	2003CC80h
84h	4	"Pmu Pwrbtn B Delay Line Multiplexer (cfio_regs_pad_pmu_pwrbtn_b_PCONF1)—Offset 84h" on page 3807	00008000h
88h	4	"Pmu Pwrbtn B Pad Value (cfio_regs_pad_pmu_pwrbtn_b_PAD_VAL)—Offset 88h" on page 3808	00000002h
90h	4	"Pmu Batlow B Pad Configuration (cfio_regs_pad_pmu_batlow_b_PCONF0)—Offset 90h" on page 3809	2003CC80h
94h	4	"Pmu Batlow B Delay Line Multiplexer (cfio_regs_pad_pmu_batlow_b_PCONF1)—Offset 94h" on page 3811	00008000h
98h	4	"Pmu Batlow B Pad Value (cfio_regs_pad_pmu_batlow_b_PAD_VAL)—Offset 98h" on page 3812	00000006h
A0h	4	"Pmu Wake Lan B Pad Configuration (cfio_regs_pad_pmu_wake_lan_b_PCONF0)—Offset A0h" on page 3812	2003CC80h
A4h	4	"Pmu Wake Lan B Delay Line Multiplexer (cfio_regs_pad_pmu_wake_lan_b_PCONF1)—Offset A4h" on page 3814	00008000h
A8h	4	"Pmu Wake Lan B Pad Value (cfio_regs_pad_pmu_wake_lan_b_PAD_VAL)—Offset A8h" on page 3815	00000002h
B0h	4	"Pmu Susclk Pad Configuration (cfio_regs_pad_pmu_susclk_PCONF0)—Offset B0h" on page 3816	2003CD00h
B4h	4	"Pmu Susclk Delay Line Multiplexer (cfio_regs_pad_pmu_susclk_PCONF1)—Offset B4h" on page 3817	00008000h
B8h	4	"Pmu Susclk Pad Value (cfio_regs_pad_pmu_susclk_PAD_VAL)—Offset B8h" on page 3818	00000002h
C0h	4	"Usb Oc0 B Pad Configuration (cfio_regs_pad_usb_oc0_b_PCONF0)—Offset C0h" on page 3819	2003CC80h
C4h	4	"Usb Oc0 B Delay Line Multiplexer (cfio_regs_pad_usb_oc0_b_PCONF1)—Offset C4h" on page 3821	00008000h
C8h	4	"Usb Oc0 B Pad Value (cfio_regs_pad_usb_oc0_b_PAD_VAL)—Offset C8h" on page 3822	00000002h
D0h	4	"Pmu Slp S3 B Pad Configuration (cfio_regs_pad_pmu_slp_s3_b_PCONF0)—Offset D0h" on page 3822	2003C800h

Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
D4h	4	"Pmu Slp S3 B Delay Line Multiplexer (cfio_regs_pad_pmu_slp_s3_b_PCONF1)—Offset D4h" on page 3824	00008000h
D8h	4	"Pmu Slp S3 B Pad Value (cfio_regs_pad_pmu_slp_s3_b_PAD_VAL)—Offset D8h" on page 3825	00000002h
E0h	4	"Pmu Ac Present Pad Configuration (cfio_regs_pad_pmu_ac_present_PCONF0)—Offset E0h" on page 3826	2003CD00h
E4h	4	"Pmu Ac Present Delay Line Multiplexer (cfio_regs_pad_pmu_ac_present_PCONF1)—Offset E4h" on page 3827	00008000h
E8h	4	"Pmu Ac Present Pad Value (cfio_regs_pad_pmu_ac_present_PAD_VAL)—Offset E8h" on page 3828	00000006h
F0h	4	"Pmu Slp S4 B Pad Configuration (cfio_regs_pad_pmu_slp_s4_b_PCONF0)—Offset F0h" on page 3829	2003C800h
F4h	4	"Pmu Slp S4 B Delay Line Multiplexer (cfio_regs_pad_pmu_slp_s4_b_PCONF1)—Offset F4h" on page 3831	00008000h
F8h	4	"Pmu Slp S4 B Pad Value (cfio_regs_pad_pmu_slp_s4_b_PAD_VAL)—Offset F8h" on page 3832	00000002h
100h	4	"Pmu Pltrst B Pad Configuration (cfio_regs_pad_pmu_pltrst_b_PCONF0)—Offset 100h" on page 3832	2003C800h
104h	4	"Pmu Pltrst B Delay Line Multiplexer (cfio_regs_pad_pmu_pltrst_b_PCONF1)—Offset 104h" on page 3834	00008000h
108h	4	"Pmu Pltrst B Pad Value (cfio_regs_pad_pmu_pltrst_b_PAD_VAL)—Offset 108h" on page 3835	00000002h
110h	4	"Pmu Slp Lan B Pad Configuration (cfio_regs_pad_pmu_slp_lan_b_PCONF0)—Offset 110h" on page 3836	2003CC80h
114h	4	"Pmu Slp Lan B Delay Line Multiplexer (cfio_regs_pad_pmu_slp_lan_b_PCONF1)—Offset 114h" on page 3837	00008000h
118h	4	"Pmu Slp Lan B Pad Value (cfio_regs_pad_pmu_slp_lan_b_PAD_VAL)—Offset 118h" on page 3838	00000002h
120h	4	"Sec Gpio Sus10 Pad Configuration (cfio_regs_pad_sec_gpio_sus10_PCONF0)—Offset 120h" on page 3839	2003CC80h
124h	4	"Sec Gpio Sus10 Delay Line Multiplexer (cfio_regs_pad_sec_gpio_sus10_PCONF1)—Offset 124h" on page 3841	00008000h
128h	4	"Sec Gpio Sus10 Pad Value (cfio_regs_pad_sec_gpio_sus10_PAD_VAL)—Offset 128h" on page 3842	00000002h
130h	4	"Sus Stat B Pad Configuration (cfio_regs_pad_sus_stat_b_PCONF0)—Offset 130h" on page 3842	2003CD00h
134h	4	"Sus Stat B Delay Line Multiplexer (cfio_regs_pad_sus_stat_b_PCONF1)—Offset 134h" on page 3844	00008000h
138h	4	"Sus Stat B Pad Value (cfio_regs_pad_sus_stat_b_PAD_VAL)—Offset 138h" on page 3845	00000002h
140h	4	"Pmu Slp S0ix B Pad Configuration (cfio_regs_pad_pmu_slp_s0ix_b_PCONF0)—Offset 140h" on page 3846	2003CD00h

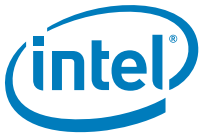


Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
144h	4	"Pmu Slp S0ix B Delay Line Multiplexer (cfio_regs_pad_pmu_slp_s0ix_b_PCONF1)—Offset 144h" on page 3848	00008000h
148h	4	"Pmu Slp S0ix B Pad Value (cfio_regs_pad_pmu_slp_s0ix_b_PAD_VAL)—Offset 148h" on page 3848	00000002h
150h	4	"Gpio Dfx5 Pad Configuration (cfio_regs_pad_gpio_dfx5_PCONF0)—Offset 150h" on page 3849	2003CC80h
154h	4	"Gpio Dfx5 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx5_PCONF1)—Offset 154h" on page 3851	00008000h
158h	4	"Gpio Dfx5 Pad Value (cfio_regs_pad_gpio_dfx5_PAD_VAL)—Offset 158h" on page 3852	00000002h
160h	4	"Gpio Dfx4 Pad Configuration (cfio_regs_pad_gpio_dfx4_PCONF0)—Offset 160h" on page 3853	2003CD00h
164h	4	"Gpio Dfx4 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx4_PCONF1)—Offset 164h" on page 3855	00008000h
168h	4	"Gpio Dfx4 Pad Value (cfio_regs_pad_gpio_dfx4_PAD_VAL)—Offset 168h" on page 3855	00000002h
170h	4	"Gpio Dfx0 Pad Configuration (cfio_regs_pad_gpio_dfx0_PCONF0)—Offset 170h" on page 3856	2003CD00h
174h	4	"Gpio Dfx0 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx0_PCONF1)—Offset 174h" on page 3858	00008000h
178h	4	"Gpio Dfx0 Pad Value (cfio_regs_pad_gpio_dfx0_PAD_VAL)—Offset 178h" on page 3859	00000002h
180h	4	"Gpio Dfx6 Pad Configuration (cfio_regs_pad_gpio_dfx6_PCONF0)—Offset 180h" on page 3860	2003CC80h
184h	4	"Gpio Dfx6 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx6_PCONF1)—Offset 184h" on page 3862	00008000h
188h	4	"Gpio Dfx6 Pad Value (cfio_regs_pad_gpio_dfx6_PAD_VAL)—Offset 188h" on page 3862	00000002h
190h	4	"Gpio Dfx7 Pad Configuration (cfio_regs_pad_gpio_dfx7_PCONF0)—Offset 190h" on page 3863	2003CC80h
194h	4	"Gpio Dfx7 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx7_PCONF1)—Offset 194h" on page 3865	00008000h
198h	4	"Gpio Dfx7 Pad Value (cfio_regs_pad_gpio_dfx7_PAD_VAL)—Offset 198h" on page 3866	00000002h
1A0h	4	"Gpio Dfx8 Pad Configuration (cfio_regs_pad_gpio_dfx8_PCONF0)—Offset 1A0h" on page 3867	2003CC80h
1A4h	4	"Gpio Dfx8 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx8_PCONF1)—Offset 1A4h" on page 3869	00008000h
1A8h	4	"Gpio Dfx8 Pad Value (cfio_regs_pad_gpio_dfx8_PAD_VAL)—Offset 1A8h" on page 3869	00000002h
1B0h	4	"Gpio Dfx3 Pad Configuration (cfio_regs_pad_gpio_dfx3_PCONF0)—Offset 1B0h" on page 3870	2003CD00h

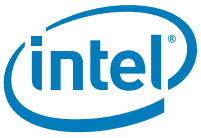


Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
1B4h	4	"Gpio Dfx3 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx3_PCONF1)—Offset 1B4h" on page 3872	00008000h
1B8h	4	"Gpio Dfx3 Pad Value (cfio_regs_pad_gpio_dfx3_PAD_VAL)—Offset 1B8h" on page 3873	00000002h
1C0h	4	"Gpio Dfx2 Pad Configuration (cfio_regs_pad_gpio_dfx2_PCONF0)—Offset 1C0h" on page 3874	2003CD00h
1C4h	4	"Gpio Dfx2 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx2_PCONF1)—Offset 1C4h" on page 3876	00008000h
1C8h	4	"Gpio Dfx2 Pad Value (cfio_regs_pad_gpio_dfx2_PAD_VAL)—Offset 1C8h" on page 3876	00000002h
1D0h	4	"Gpio Sus0 Pad Configuration (cfio_regs_pad_gpio_sus0_PCONF0)—Offset 1D0h" on page 3877	2003CC80h
1D4h	4	"Gpio Sus0 Delay Line Multiplexer (cfio_regs_pad_gpio_sus0_PCONF1)—Offset 1D4h" on page 3879	00008000h
1D8h	4	"Gpio Sus0 Pad Value (cfio_regs_pad_gpio_sus0_PAD_VAL)—Offset 1D8h" on page 3880	00000002h
1E0h	4	"Gpio Sus2 Pad Configuration (cfio_regs_pad_gpio_sus2_PCONF0)—Offset 1E0h" on page 3881	2003CC80h
1E4h	4	"Gpio Sus2 Delay Line Multiplexer (cfio_regs_pad_gpio_sus2_PCONF1)—Offset 1E4h" on page 3882	00008000h
1E8h	4	"Gpio Sus2 Pad Value (cfio_regs_pad_gpio_sus2_PAD_VAL)—Offset 1E8h" on page 3883	00000002h
1F0h	4	"Gpio Sus3 Pad Configuration (cfio_regs_pad_gpio_sus3_PCONF0)—Offset 1F0h" on page 3884	2003CC80h
1F4h	4	"Gpio Sus3 Delay Line Multiplexer (cfio_regs_pad_gpio_sus3_PCONF1)—Offset 1F4h" on page 3886	00008000h
1F8h	4	"Gpio Sus3 Pad Value (cfio_regs_pad_gpio_sus3_PAD_VAL)—Offset 1F8h" on page 3887	00000002h
200h	4	"Gpio Sus4 Pad Configuration (cfio_regs_pad_gpio_sus4_PCONF0)—Offset 200h" on page 3887	2003CD00h
204h	4	"Gpio Sus4 Delay Line Multiplexer (cfio_regs_pad_gpio_sus4_PCONF1)—Offset 204h" on page 3889	00008000h
208h	4	"Gpio Sus4 Pad Value (cfio_regs_pad_gpio_sus4_PAD_VAL)—Offset 208h" on page 3890	00000002h
210h	4	"Gpio Sus1 Pad Configuration (cfio_regs_pad_gpio_sus1_PCONF0)—Offset 210h" on page 3891	2003CC80h
214h	4	"Gpio Sus1 Delay Line Multiplexer (cfio_regs_pad_gpio_sus1_PCONF1)—Offset 214h" on page 3893	00008000h
218h	4	"Gpio Sus1 Pad Value (cfio_regs_pad_gpio_sus1_PAD_VAL)—Offset 218h" on page 3894	00000002h
220h	4	"Gpio Sus5 Pad Configuration (cfio_regs_pad_gpio_sus5_PCONF0)—Offset 220h" on page 3894	2003CD00h

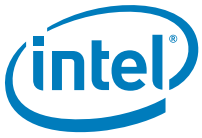


Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
224h	4	"Gpio Sus5 Delay Line Multiplexer (cfio_regs_pad_gpio_sus5_PCONF1)—Offset 224h" on page 3896	00008000h
228h	4	"Gpio Sus5 Pad Value (cfio_regs_pad_gpio_sus5_PAD_VAL)—Offset 228h" on page 3897	00000002h
230h	4	"Gpio Sus7 Pad Configuration (cfio_regs_pad_gpio_sus7_PCONF0)—Offset 230h" on page 3898	2003CD00h
234h	4	"Gpio Sus7 Delay Line Multiplexer (cfio_regs_pad_gpio_sus7_PCONF1)—Offset 234h" on page 3900	00008000h
238h	4	"Gpio Sus7 Pad Value (cfio_regs_pad_gpio_sus7_PAD_VAL)—Offset 238h" on page 3900	00000002h
240h	4	"Gpio Sus6 Pad Configuration (cfio_regs_pad_gpio_sus6_PCONF0)—Offset 240h" on page 3901	2003CD00h
244h	4	"Gpio Sus6 Delay Line Multiplexer (cfio_regs_pad_gpio_sus6_PCONF1)—Offset 244h" on page 3903	00008000h
248h	4	"Gpio Sus6 Pad Value (cfio_regs_pad_gpio_sus6_PAD_VAL)—Offset 248h" on page 3904	00000002h
250h	4	"Sec Gpio Sus9 Pad Configuration (cfio_regs_pad_sec_gpio_sus9_PCONF0)—Offset 250h" on page 3905	2003CD00h
254h	4	"Sec Gpio Sus9 Delay Line Multiplexer (cfio_regs_pad_sec_gpio_sus9_PCONF1)—Offset 254h" on page 3907	00008000h
258h	4	"Sec Gpio Sus9 Pad Value (cfio_regs_pad_sec_gpio_sus9_PAD_VAL)—Offset 258h" on page 3907	00000002h
260h	4	"Sec Gpio Sus8 Pad Configuration (cfio_regs_pad_sec_gpio_sus8_PCONF0)—Offset 260h" on page 3908	2003CD00h
264h	4	"Sec Gpio Sus8 Delay Line Multiplexer (cfio_regs_pad_sec_gpio_sus8_PCONF1)—Offset 264h" on page 3910	00008000h
268h	4	"Sec Gpio Sus8 Pad Value (cfio_regs_pad_sec_gpio_sus8_PAD_VAL)—Offset 268h" on page 3911	00000002h
270h	4	"Gpio Dfx1 Pad Configuration (cfio_regs_pad_gpio_dfx1_PCONF0)—Offset 270h" on page 3912	2003CD00h
274h	4	"Gpio Dfx1 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx1_PCONF1)—Offset 274h" on page 3914	00008000h
278h	4	"Gpio Dfx1 Pad Value (cfio_regs_pad_gpio_dfx1_PAD_VAL)—Offset 278h" on page 3914	00000002h
280h	4	"Usb Ulpi 0 Refclk Pad Configuration (cfio_regs_pad_usb_ulpi_0_refclk_PCONF0)—Offset 280h" on page 3915	2003CD00h
284h	4	"Usb Ulpi 0 Refclk Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_refclk_PCONF1)—Offset 284h" on page 3917	00008000h
288h	4	"Usb Ulpi 0 Refclk Pad Value (cfio_regs_pad_usb_ulpi_0_refclk_PAD_VAL)—Offset 288h" on page 3918	00000002h

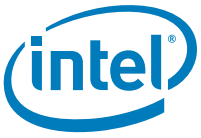


Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
290h	4	"Tck Pad Configuration (cfio_regs_pad_tck_PCONF0)—Offset 290h" on page 3919	2003C900h
294h	4	"Tck Delay Line Multiplexer (cfio_regs_pad_tck_PCONF1)—Offset 294h" on page 3921	00008000h
298h	4	"Tck Pad Value (cfio_regs_pad_tck_PAD_VAL)—Offset 298h" on page 3921	00000006h
2A0h	4	"Trst B Pad Configuration (cfio_regs_pad_trst_b_PCONF0)—Offset 2A0h" on page 3922	2003C880h
2A4h	4	"Trst B Delay Line Multiplexer (cfio_regs_pad_trst_b_PCONF1)—Offset 2A4h" on page 3924	00008000h
2A8h	4	"Trst B Pad Value (cfio_regs_pad_trst_b_PAD_VAL)—Offset 2A8h" on page 3925	00000006h
2B0h	4	"Tdi Pad Configuration (cfio_regs_pad_tdi_PCONF0)—Offset 2B0h" on page 3926	2003C880h
2B4h	4	"Tdi Delay Line Multiplexer (cfio_regs_pad_tdi_PCONF1)—Offset 2B4h" on page 3927	00008000h
2B8h	4	"Tdi Pad Value (cfio_regs_pad_tdi_PAD_VAL)—Offset 2B8h" on page 3928	00000006h
2C0h	4	"Tms Pad Configuration (cfio_regs_pad_tms_PCONF0)—Offset 2C0h" on page 3929	2003C880h
2C4h	4	"Tms Delay Line Multiplexer (cfio_regs_pad_tms_PCONF1)—Offset 2C4h" on page 3931	00008000h
2C8h	4	"Tms Pad Value (cfio_regs_pad_tms_PAD_VAL)—Offset 2C8h" on page 3932	00000006h
2D0h	4	"Cx Prdy B Pad Configuration (cfio_regs_pad_cx_prdy_b_PCONF0)—Offset 2D0h" on page 3932	2003C880h
2D4h	4	"Cx Prdy B Delay Line Multiplexer (cfio_regs_pad_cx_prdy_b_PCONF1)—Offset 2D4h" on page 3934	00008000h
2D8h	4	"Cx Prdy B Pad Value (cfio_regs_pad_cx_prdy_b_PAD_VAL)—Offset 2D8h" on page 3935	00000002h
2E0h	4	"Cx Preq B Pad Configuration (cfio_regs_pad_cx_preq_b_PCONF0)—Offset 2E0h" on page 3936	2003C880h
2E4h	4	"Cx Preq B Delay Line Multiplexer (cfio_regs_pad_cx_preq_b_PCONF1)—Offset 2E4h" on page 3938	00008000h
2E8h	4	"Cx Preq B Pad Value (cfio_regs_pad_cx_preq_b_PAD_VAL)—Offset 2E8h" on page 3938	00000006h
2F0h	4	"Tdo Pad Configuration (cfio_regs_pad_tdo_PCONF0)—Offset 2F0h" on page 3939	2003C800h
2F4h	4	"Tdo Delay Line Multiplexer (cfio_regs_pad_tdo_PCONF1)—Offset 2F4h" on page 3941	00008000h
2F8h	4	"Tdo Pad Value (cfio_regs_pad_tdo_PAD_VAL)—Offset 2F8h" on page 3942	00000002h

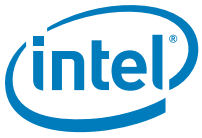


Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
300h	4	"Usb Ulpi 0 Data4 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data4_PCONF0)—Offset 300h" on page 3943	2003CD00h
304h	4	"Usb Ulpi 0 Data4 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data4_PCONF1)—Offset 304h" on page 3944	00008000h
308h	4	"Usb Ulpi 0 Data4 Pad Value (cfio_regs_pad_usb_ulpi_0_data4_PAD_VAL)—Offset 308h" on page 3945	00000002h
310h	4	"Usb Ulpi 0 Data2 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data2_PCONF0)—Offset 310h" on page 3946	2003CD00h
314h	4	"Usb Ulpi 0 Data2 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data2_PCONF1)—Offset 314h" on page 3948	00008000h
318h	4	"Usb Ulpi 0 Data2 Pad Value (cfio_regs_pad_usb_ulpi_0_data2_PAD_VAL)—Offset 318h" on page 3949	00000002h
320h	4	"Usb Ulpi 0 Data6 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data6_PCONF0)—Offset 320h" on page 3949	2003CD00h
324h	4	"Usb Ulpi 0 Data6 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data6_PCONF1)—Offset 324h" on page 3951	00008000h
328h	4	"Usb Ulpi 0 Data6 Pad Value (cfio_regs_pad_usb_ulpi_0_data6_PAD_VAL)—Offset 328h" on page 3952	00000002h
330h	4	"Usb Ulpi 0 Clk Pad Configuration (cfio_regs_pad_usb_ulpi_0_clk_PCONF0)—Offset 330h" on page 3953	2003CD00h
334h	4	"Usb Ulpi 0 Clk Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_clk_PCONF1)—Offset 334h" on page 3955	00008000h
338h	4	"Usb Ulpi 0 Clk Pad Value (cfio_regs_pad_usb_ulpi_0_clk_PAD_VAL)—Offset 338h" on page 3955	00000002h
340h	4	"Usb Ulpi 0 Dir Pad Configuration (cfio_regs_pad_usb_ulpi_0_dir_PCONF0)—Offset 340h" on page 3956	2003CC80h
344h	4	"Usb Ulpi 0 Dir Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_dir_PCONF1)—Offset 344h" on page 3958	00008000h
348h	4	"Usb Ulpi 0 Dir Pad Value (cfio_regs_pad_usb_ulpi_0_dir_PAD_VAL)—Offset 348h" on page 3959	00000002h
350h	4	"Usb Ulpi 0 Nxt Pad Configuration (cfio_regs_pad_usb_ulpi_0_nxt_PCONF0)—Offset 350h" on page 3960	2003CD00h
354h	4	"Usb Ulpi 0 Nxt Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_nxt_PCONF1)—Offset 354h" on page 3962	00008000h
358h	4	"Usb Ulpi 0 Nxt Pad Value (cfio_regs_pad_usb_ulpi_0_nxt_PAD_VAL)—Offset 358h" on page 3962	00000002h
360h	4	"Usb Ulpi 0 Data1 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data1_PCONF0)—Offset 360h" on page 3963	2003CD00h
364h	4	"Usb Ulpi 0 Data1 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data1_PCONF1)—Offset 364h" on page 3965	00008000h

Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
368h	4	"Usb Ulpi 0 Data1 Pad Value (cfio_regs_pad_usb_ulpi_0_data1_PAD_VAL)—Offset 368h" on page 3966	00000002h
370h	4	"Usb Ulpi 0 Data3 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data3_PCONF0)—Offset 370h" on page 3967	2003CD00h
374h	4	"Usb Ulpi 0 Data3 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data3_PCONF1)—Offset 374h" on page 3969	00008000h
378h	4	"Usb Ulpi 0 Data3 Pad Value (cfio_regs_pad_usb_ulpi_0_data3_PAD_VAL)—Offset 378h" on page 3969	00000002h
380h	4	"Usb Ulpi 0 Data0 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data0_PCONF0)—Offset 380h" on page 3970	2003CD00h
384h	4	"Usb Ulpi 0 Data0 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data0_PCONF1)—Offset 384h" on page 3972	00008000h
388h	4	"Usb Ulpi 0 Data0 Pad Value (cfio_regs_pad_usb_ulpi_0_data0_PAD_VAL)—Offset 388h" on page 3973	00000002h
390h	4	"Usb Ulpi 0 Data5 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data5_PCONF0)—Offset 390h" on page 3974	2003CD00h
394h	4	"Usb Ulpi 0 Data5 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data5_PCONF1)—Offset 394h" on page 3976	00008000h
398h	4	"Usb Ulpi 0 Data5 Pad Value (cfio_regs_pad_usb_ulpi_0_data5_PAD_VAL)—Offset 398h" on page 3976	00000002h
3A0h	4	"Usb Ulpi 0 Data7 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data7_PCONF0)—Offset 3A0h" on page 3977	2003CD00h
3A4h	4	"Usb Ulpi 0 Data7 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data7_PCONF1)—Offset 3A4h" on page 3979	00008000h
3A8h	4	"Usb Ulpi 0 Data7 Pad Value (cfio_regs_pad_usb_ulpi_0_data7_PAD_VAL)—Offset 3A8h" on page 3980	00000002h
3B0h	4	"Usb Ulpi 0 Stp Pad Configuration (cfio_regs_pad_usb_ulpi_0_stp_PCONF0)—Offset 3B0h" on page 3981	2003CC80h
3B4h	4	"Usb Ulpi 0 Stp Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_stp_PCONF1)—Offset 3B4h" on page 3983	00008000h
3B8h	4	"Usb Ulpi 0 Stp Pad Value (cfio_regs_pad_usb_ulpi_0_stp_PAD_VAL)—Offset 3B8h" on page 3983	00000002h
610h	4	"C71p1cfiomvnsusdfxgpio1 Compensation Configuration (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_CFG)—Offset 610h" on page 3984	00078080h
614h	4	"C71p1cfiomvnsusdfxgpio1 Compensation Override (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_OV)—Offset 614h" on page 3986	001F000Fh

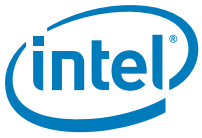


Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
618h	4	"C71p1cfiomvnsusdfxgpio1 Compensation Initial Values (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_INIT)—Offset 618h" on page 3986	0000FFFFh
61Ch	4	"C71p1cfiomvnsusdfxgpio1 Compensation DFX Override (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_DFX)—Offset 61Ch" on page 3987	01000080h
800h	4	"TS0 SSUS Interrupt Status 0 (cfio_regs_REG_TS0_SSUS_IRQ_TS_0)—Offset 800h" on page 3987	00000000h
804h	4	"TS1 SSUS Interrupt Status 1 (cfio_regs_REG_TS1_SSUS_IRQ_TS_1)—Offset 804h" on page 3988	00000000h
808h	4	"TS2 SSUS Interrupt Status 2 (cfio_regs_REG_TS2_SSUS_IRQ_TS_2)—Offset 808h" on page 3989	00000000h
80Ch	4	"TS3 SSUS Interrupt Status 3 (cfio_regs_REG_TS3_SSUS_IRQ_TS_3)—Offset 80Ch" on page 3989	00000000h
850h	4	"Itp Strength Group (cfio_regs_itp_STRENGTH)—Offset 850h" on page 3990	0003000Fh
854h	4	"Sus Rcomp Strength Group (cfio_regs_sus_rcomp_STRENGTH)—Offset 854h" on page 3991	BABECAFEh
858h	4	"Sus Spi Strength Group (cfio_regs_sus_spi_STRENGTH)—Offset 858h" on page 3991	0003000Fh
85Ch	4	"Ulpi Strength Group (cfio_regs_ulpi_STRENGTH)—Offset 85Ch" on page 3992	0003000Fh
860h	4	"Dfx Electrical Group (cfio_regs_dfx_ELECTRICAL)—Offset 860h" on page 3992	00000003h
864h	4	"Itp Electrical Group (cfio_regs_itp_ELECTRICAL)—Offset 864h" on page 3993	00000003h
868h	4	"Pmu Electrical Group (cfio_regs_pmu_ELECTRICAL)—Offset 868h" on page 3993	00000003h
86Ch	4	"Sec Electrical Group (cfio_regs_sec_ELECTRICAL)—Offset 86Ch" on page 3994	00000003h
870h	4	"Sec10 Electrical Group (cfio_regs_sec10_ELECTRICAL)—Offset 870h" on page 3995	00000003h
874h	4	"Sus1 Electrical Group (cfio_regs_sus1_ELECTRICAL)—Offset 874h" on page 3995	00000003h
878h	4	"Sus2 Electrical Group (cfio_regs_sus2_ELECTRICAL)—Offset 878h" on page 3996	00000003h
87Ch	4	"Sus3 Electrical Group (cfio_regs_sus3_ELECTRICAL)—Offset 87Ch" on page 3997	00000003h
880h	4	"Sus4 Electrical Group (cfio_regs_sus4_ELECTRICAL)—Offset 880h" on page 3998	00000003h
884h	4	"Sus Spi Electrical Group (cfio_regs_sus_spi_ELECTRICAL)—Offset 884h" on page 3998	00000003h

Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
888h	4	"Tap Electrical Group (cfio_regs_tap_ELECTRICAL)—Offset 888h" on page 3999	00000003h
88Ch	4	"Ulpi Electrical Group (cfio_regs_ulpi_ELECTRICAL)—Offset 88Ch" on page 4000	00000003h
890h	4	"Usb Electrical Group (cfio_regs_usb_ELECTRICAL)—Offset 890h" on page 4000	00000003h
900h	4	"CFG SSUS PSB Configuration (cfio_regs_COM_CFG_SSUS_PB_CONFIG)—Offset 900h" on page 4001	01071003h
904h	4	"IRQ TYPE SSUS Interrupt Type (cfio_regs_REG_IRQ_TYPE_SSUS_IRQ_TYPE)—Offset 904h" on page 4002	00000003h
950h	4	"WR PATH SSUS Master Delay Line Write Address (cfio_regs_DLL_WR_PATH_SSUS_MDL_WRITE_PATH_C_F_ADDR)—Offset 950h" on page 4002	00080000h
954h	4	"WR PATH1 MUX SSUS Delay Line Write Multiplexer 1 (cfio_regs_DLL_WR_PATH1_MUX_SSUS_DLL_WRITE_PATH1_MUX)—Offset 954h" on page 4003	00000000h
958h	4	"WR PATH2 MUX SSUS Delay Line Write Multiplexer 2 (cfio_regs_DLL_WR_PATH2_MUX_SSUS_DLL_WRITE_PATH2_MUX)—Offset 958h" on page 4004	00000000h
95Ch	4	"WR PATH3 MUX SSUS Delay Line Write Multiplexer 3 (cfio_regs_DLL_WR_PATH3_MUX_SSUS_DLL_WRITE_PATH3_MUX)—Offset 95Ch" on page 4004	00000000h
960h	4	"FIFO SSUS Emmc Fifo Control (cfio_regs_EMMC_FIFO_SSUS_EMMC_FIFO)—Offset 960h" on page 4005	00000000h
964h	4	"INIT SSUS Master Delay Line Initial Values (cfio_regs_DLL_INIT_SSUS_MDL_CF_INIT)—Offset 964h" on page 4006	00000000h
968h	4	"SW MODE SSUS Master Delay Line Software Values (cfio_regs_DLL_SW_MODE_SSUS_MDL_CF_SW)—Offset 968h" on page 4006	00000000h
96Ch	4	"VALS SSUS Master Delay Line Fsm Values (cfio_regs_DLL_VALS_SSUS_MDL_FSM_VALS)—Offset 96Ch" on page 4007	00078000h
970h	4	"CTRL SSUS Master Delay Line Fsm Control (cfio_regs_DLL_CTRL_SSUS_MDL_FSM_CTRL)—Offset 970h" on page 4007	00000000h
980h	4	"DIRECT IRQ0 SSUS Direct Interrupt Multiplexer 0 (cfio_regs_REG_DIRECT_IRQ0_SSUS_DIRECT_IRQ_0)—Offset 980h" on page 4008	00000000h

Table 77. Summary of PCU iLB GPIO Memory Mapped I/O Registers—IO_CONTROLLER_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
984h	4	"DIRECT IRQ1 SSUS Direct Interrupt Multiplexer 1 (cfio_regs_REG_DIRECT_IRQ1_SSUS_DIRECT_IRQ_1)—Offset 984h" on page 4009	00000000h
988h	4	"DIRECT IRQ2 SSUS Direct Interrupt Multiplexer 2 (cfio_regs_REG_DIRECT_IRQ2_SSUS_DIRECT_IRQ_2)—Offset 988h" on page 4010	00000000h
98Ch	4	"DIRECT IRQ3 SSUS Direct Interrupt Multiplexer 3 (cfio_regs_REG_DIRECT_IRQ3_SSUS_DIRECT_IRQ_3)—Offset 98Ch" on page 4011	00000000h

3.69.1 Usb Oc1 B Pad Configuration (cfio_regs_pad_usb_oc1_b_PCONF0)—Offset 0h

PADs Memory space configuration register (Access via PCU Proxy)

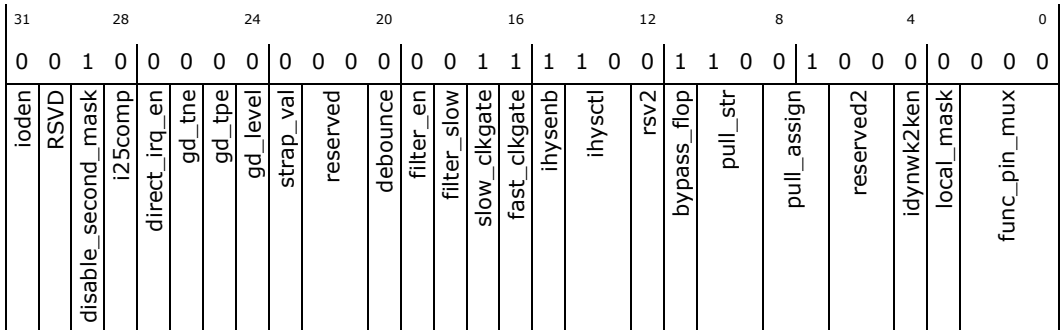
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_oc1_b_PCONF0: [IOBASE + 2000h] + 0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is USB_OC1_B function 1 is GPIOS_20

3.69.2 Usb Oc1 B Delay Line Multiplexer (cfio_regs_pad_usb_oc1_b_PCONF1)—Offset 4h

DLL Multiplexer

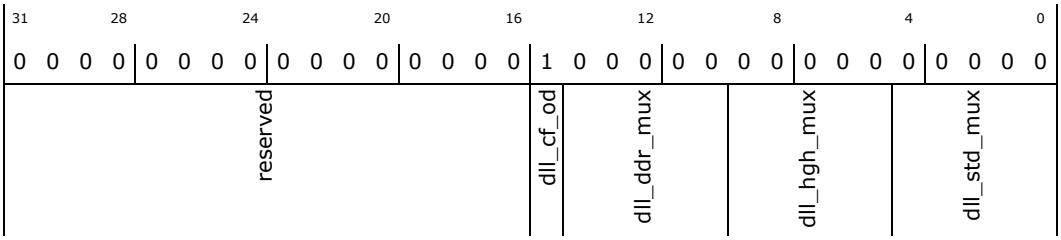
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_oc1_b_PCONF1: [IOBASE + 2000h] + 4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.3 Usb Oc1 B Pad Value (cfio_regs_pad_usb_oc1_b_PAD_VAL)—Offset 8h

PADs Memory space Value register (Access via PCU Proxy)

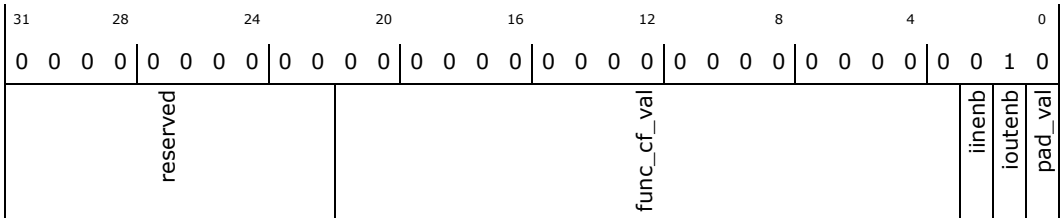
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_oc1_b_PAD_VAL: [IOBASE + 2000h] + 8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.4 Pmu Wake B Pad Configuration (cfio_regs_pad_pmu_wake_b_PCONF0)—Offset 10h

PADs Memory space configuration register (Access via PCU Proxy)

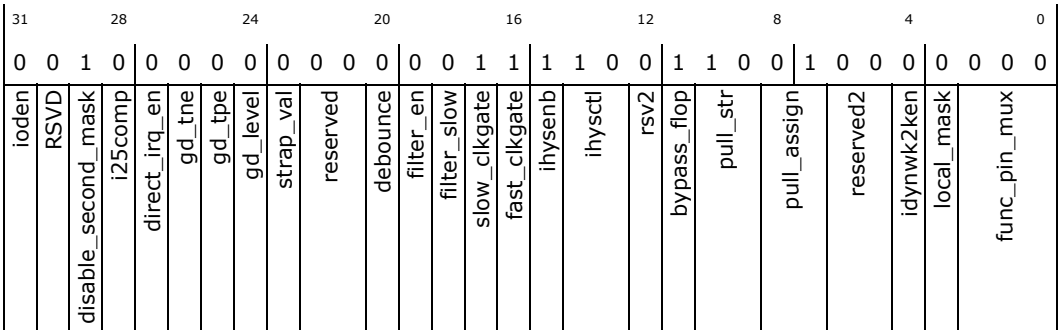
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_wake_b_PCONF0: [IOBASE + 2000h] + 10h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_WAKE_B function 1 is GPIOS_15

3.69.5 Pmu Wake B Delay Line Multiplexer (cfio_regs_pad_pmu_wake_b_PCONF1)—Offset 14h

DLL Multiplexer

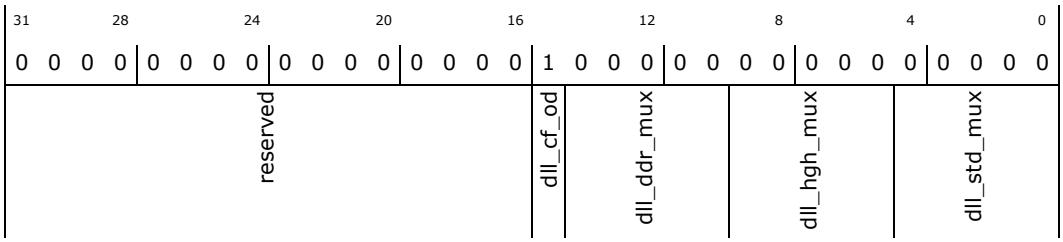
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_wake_b_PCONF1: [IOBASE + 2000h] + 14h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.6 Pmu Wake B Pad Value (cfio_regs_pad_pmu_wake_b_PAD_VAL)—Offset 18h

PADs Memory space Value register (Access via PCU Proxy)

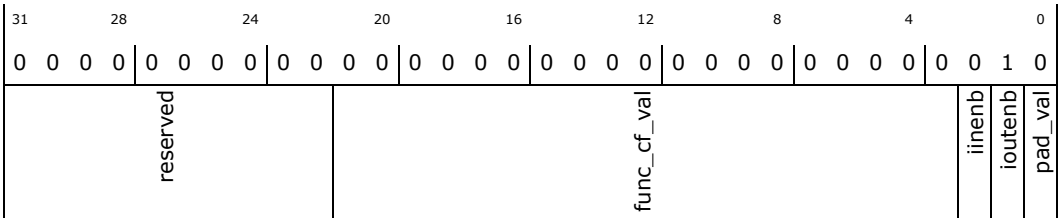
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_wake_b_PAD_VAL: [IOBASE + 2000h] + 18h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.7 Spi Cs1 B Pad Configuration (cfio_regs_pad_spi_cs1_b_PCONF0)—Offset 20h

PADs Memory space configuration register (Access via PCU Proxy)

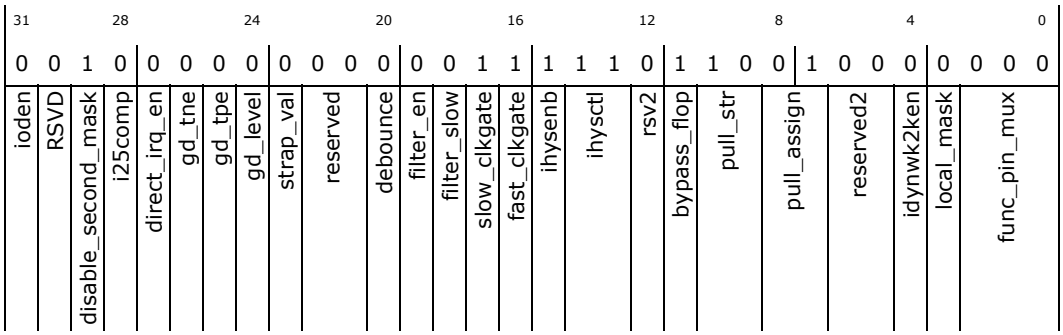
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_cs1_b_PCONF0: [IOBASE + 2000h] + 20h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is SPI_CS1_B function 1 is GPIOS_21

3.69.8 Spi Cs1 B Delay Line Multiplexer (cfio_regs_pad_spi_cs1_b_PCONF1)—Offset 24h

DLL Multiplexer

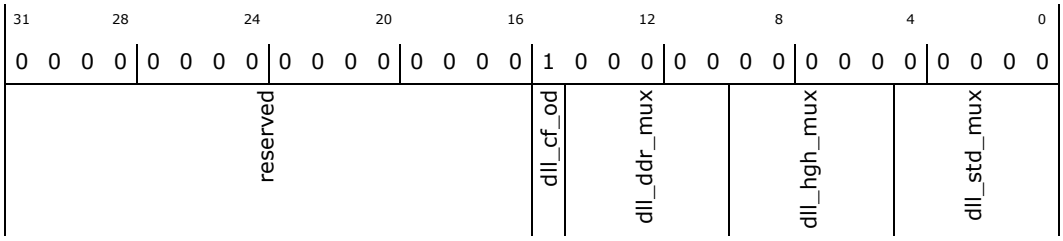
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_cs1_b_PCONF1: [IOBASE + 2000h] + 24h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.9 Spi Cs1 B Pad Value (cfio_regs_pad_spi_cs1_b_PAD_VAL)—Offset 28h

PADs Memory space Value register (Access via PCU Proxy)

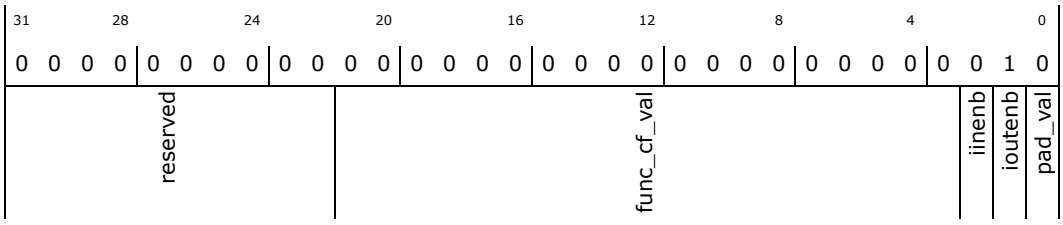
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_cs1_b_PAD_VAL: [IOBASE + 2000h] + 28h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.10 Spi Cs0 B Pad Configuration (cfio_regs_pad_spi_cs0_b_PCONF0)—Offset 30h

PADs Memory space configuration register (Access via PCU Proxy)

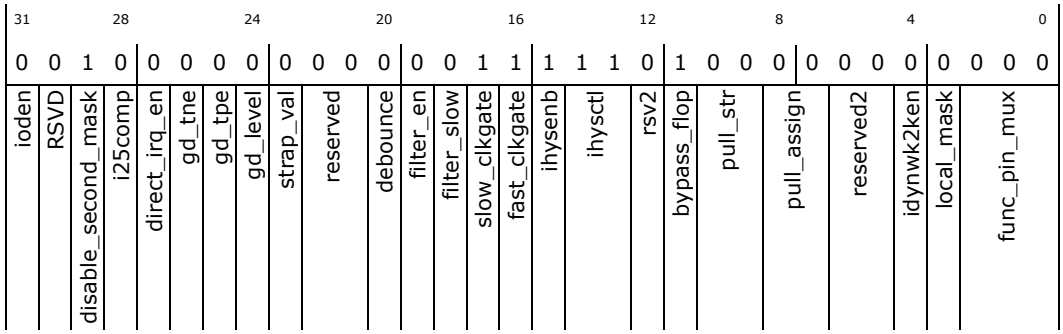
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_cs0_b_PCONF0: [IOBASE + 2000h] + 30h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003E800h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is SPI_CS0_B

3.69.11 Spi Cs0 B Delay Line Multiplexer (cfio_regs_pad_spi_cs0_b_PCONF1)—Offset 34h

DLL Multiplexer

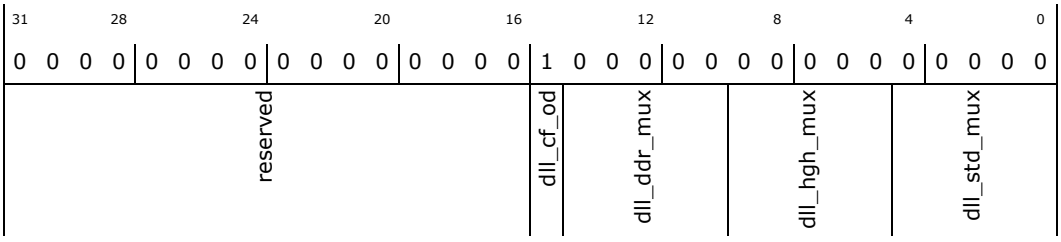
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_cs0_b_PCONF1: [IOBASE + 2000h] + 34h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.12 Spi Cs0 B Pad Value (cfio_regs_pad_spi_cs0_b_PAD_VAL)—Offset 38h

PADs Memory space Value register (Access via PCU Proxy)

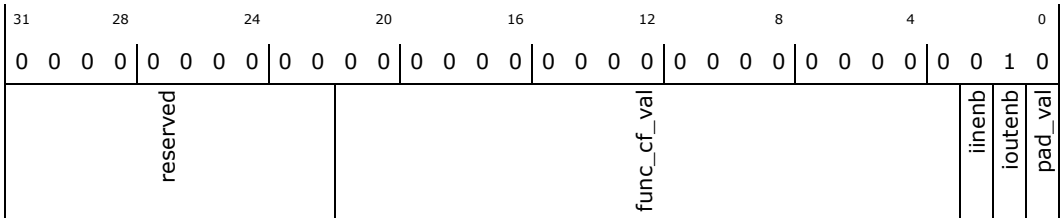
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_cs0_b_PAD_VAL: [IOBASE + 2000h] + 38h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.13 Spi Clk Pad Configuration (cfio_regs_pad_spi_clk_PCONF0)—Offset 40h

PADs Memory space configuration register (Access via PCU Proxy)

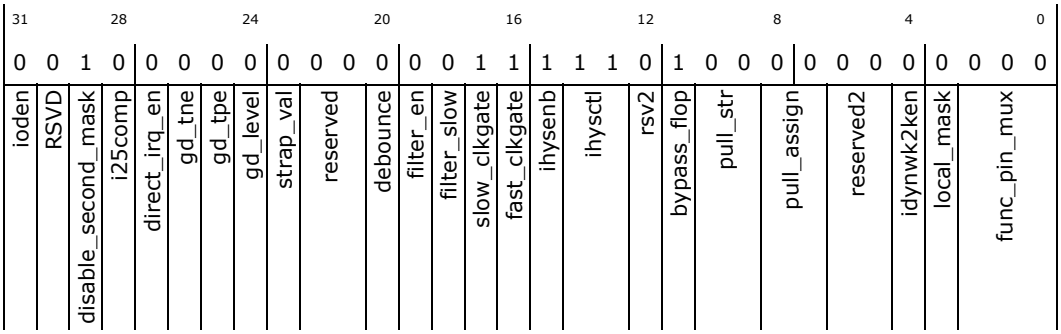
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_clk_PCONF0: [IOBASE + 2000h] + 40h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003E800h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is SPI_CLK

3.69.14 Spi Clk Delay Line Multiplexer (cfio_regs_pad_spi_clk_PCONF1)—Offset 44h

DLL Multiplexer

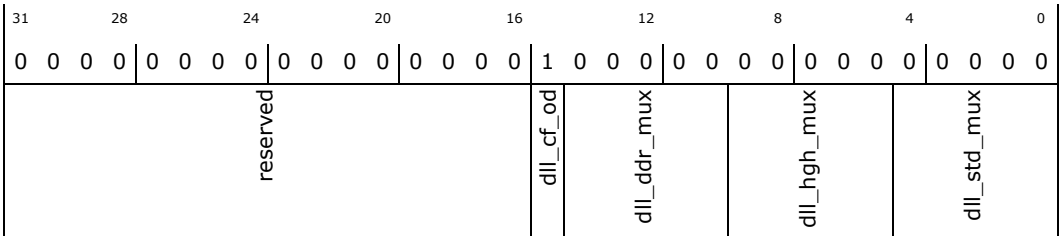
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_clk_PCONF1: [IOBASE + 2000h] + 44h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.15 Spi Clk Pad Value (cfio_regs_pad_spi_clk_PAD_VAL)—Offset 48h

PADs Memory space Value register (Access via PCU Proxy)

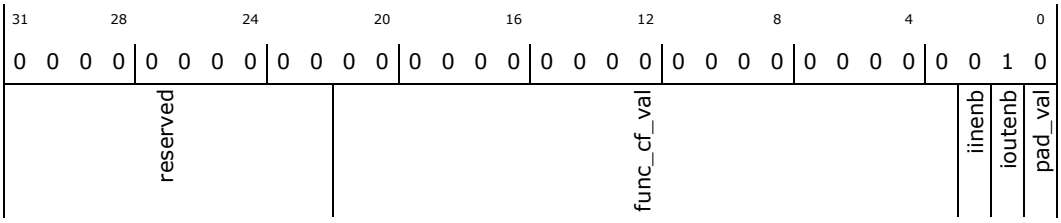
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_clk_PAD_VAL: [IOBASE + 2000h] + 48h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.16 Spi Mosi Pad Configuration (cfio_regs_pad_spi_mosi_PCONF0)—Offset 50h

PADs Memory space configuration register (Access via PCU Proxy)

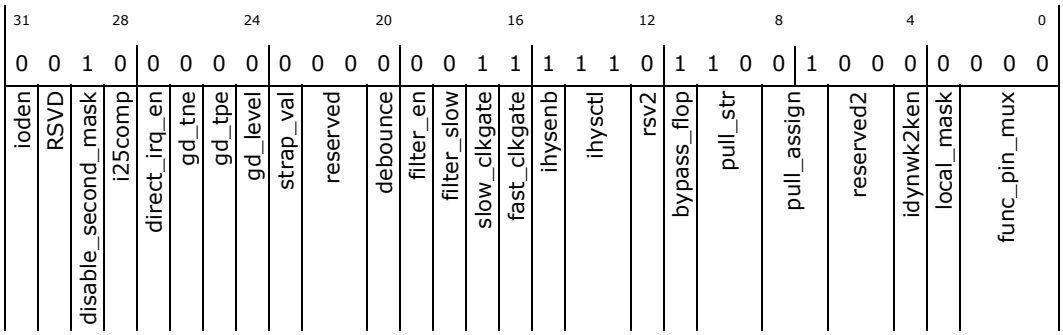
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_mosi_PCONF0: [IOBASE + 2000h] + 50h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is SPI_MOSI

3.69.17 Spi Mosi Delay Line Multiplexer (cfio_regs_pad_spi_mosi_PCONF1)—Offset 54h

DLL Multiplexer

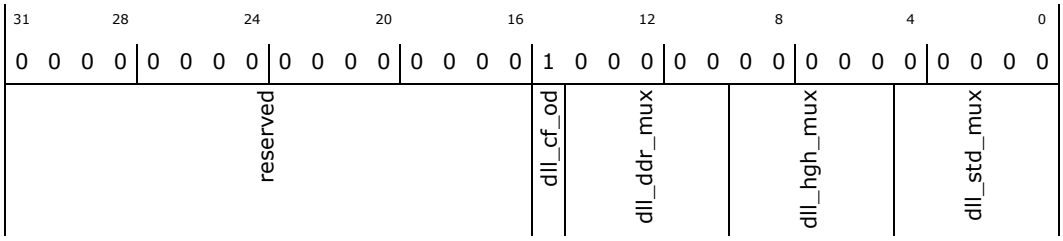
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_mosi_PCONF1: [IOBASE + 2000h] + 54h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.18 Spi Mosi Pad Value (cfio_regs_pad_spi_mosi_PAD_VAL)—Offset 58h

PADs Memory space Value register (Access via PCU Proxy)

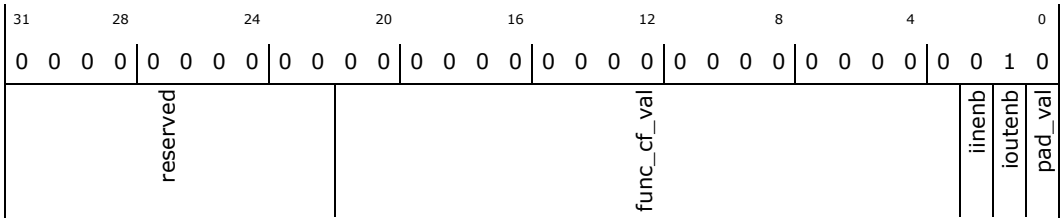
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_mosi_PAD_VAL: [IOBASE + 2000h] + 58h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.19 Spi Miso Pad Configuration (cfio_regs_pad_spi_miso_PCONF0)—Offset 60h

PADs Memory space configuration register (Access via PCU Proxy)

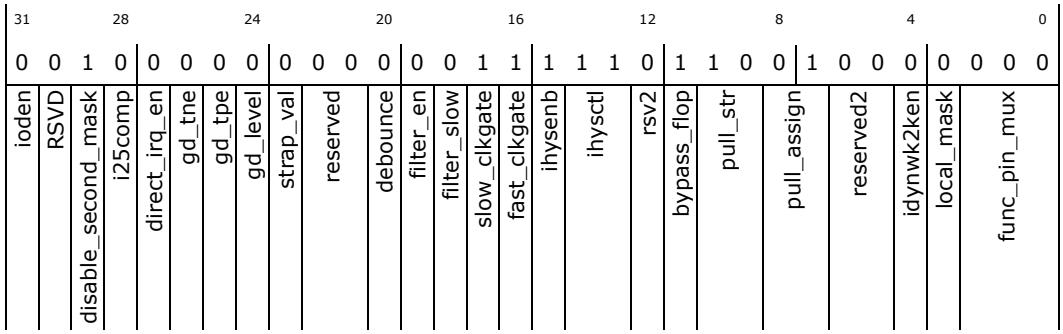
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_miso_PCONF0: [IOBASE + 2000h] + 60h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is SPI_MISO

3.69.20 Spi Miso Delay Line Multiplexer (cfio_regs_pad_spi_miso_PCONF1)—Offset 64h

DLL Multiplexer

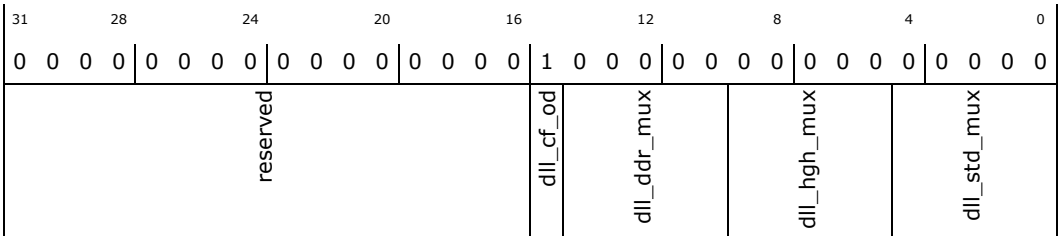
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_miso_PCONF1: [IOBASE + 2000h] + 64h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.21 Spi Miso Pad Value (cfio_regs_pad_spi_miso_PAD_VAL)—Offset 68h

PADs Memory space Value register (Access via PCU Proxy)

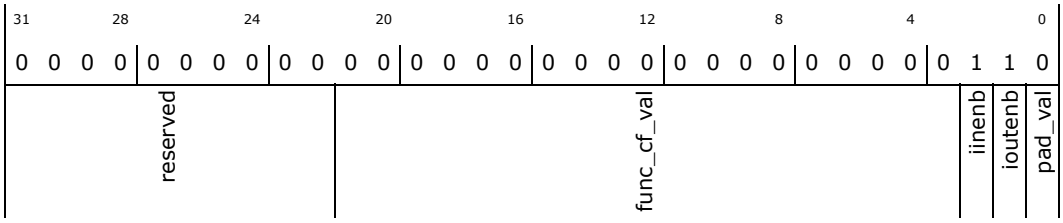
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_spi_miso_PAD_VAL: [IOBASE + 2000h] + 68h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.22 Suspwrdnack Pad Configuration (cfio_regs_pad_suspwrdnack_PCONF0)—Offset 70h

PADs Memory space configuration register (Access via PCU Proxy)

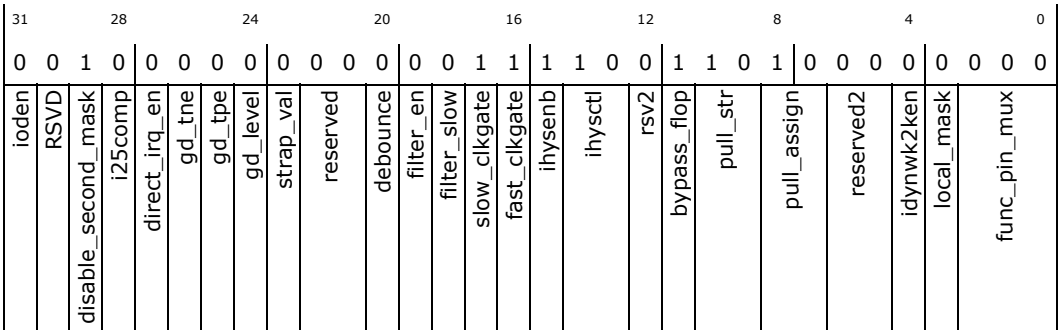
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_suspwrdnack_PCONF0: [IOBASE + 2000h] + 70h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is SUSPWRDNACK function 1 is GPIOS_11

3.69.23 Suspwrdnack Delay Line Multiplexer (cfio_regs_pad_suspwrdnack_PCONF1)—Offset 74h

DLL Multiplexer

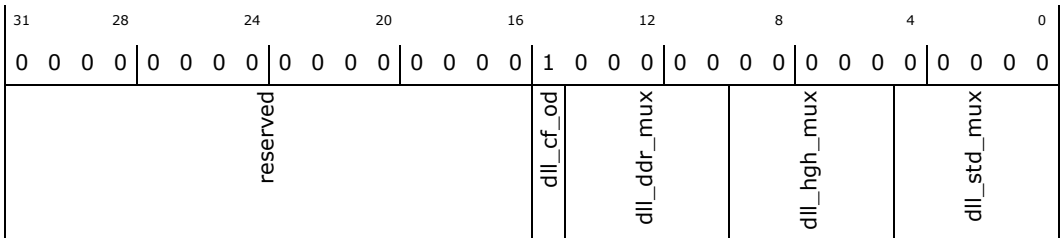
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_suspwrdnack_PCONF1: [IOBASE + 2000h] + 74h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.24 Suspwrdnack Pad Value (cfio_regs_pad_suspwrdnack_PAD_VAL)—Offset 78h

PADs Memory space Value register (Access via PCU Proxy)

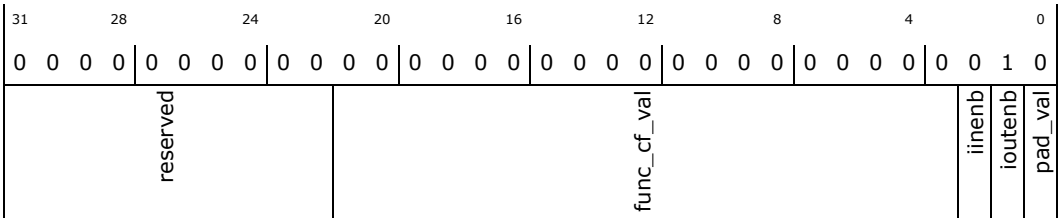
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_suspwrdnack_PAD_VAL: [IOBASE + 2000h] + 78h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.25 Pmu Pwrbtn B Pad Configuration (cfio_regs_pad_pmu_pwrbtn_b_PCONF0)—Offset 80h

PADs Memory space configuration register (Access via PCU Proxy)

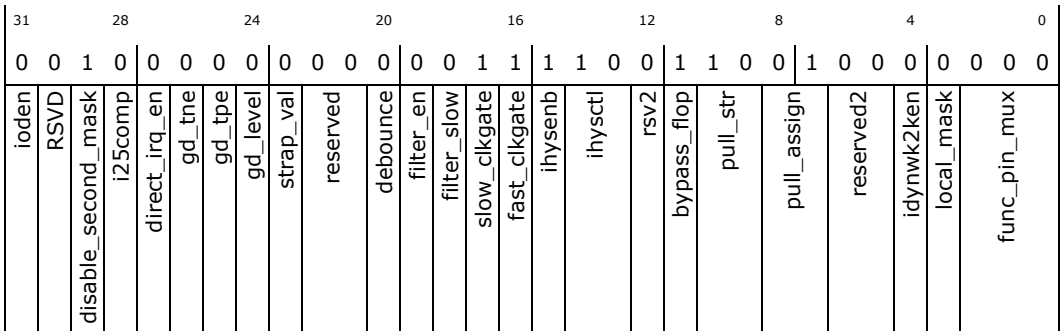
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_pwrbtn_b_PCONF0: [IOBASE + 2000h] + 80h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_PWRBTN_B function 1 is GPIOS_16

3.69.26 Pmu Pwrbtn B Delay Line Multiplexer (cfio_regs_pad_pmu_pwrbtn_b_PCONF1)—Offset 84h

DLL Multiplexer

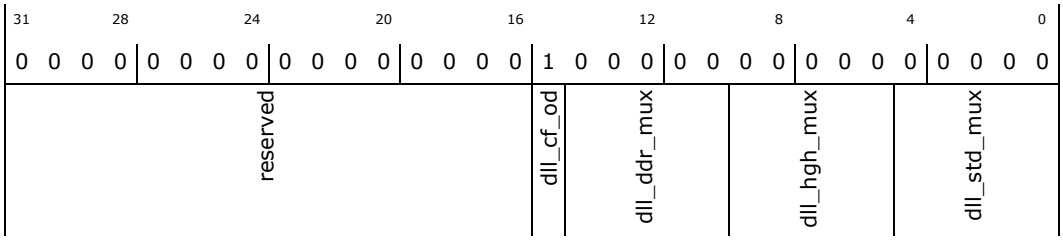
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_pwrbtn_b_PCONF1: [IOBASE + 2000h] + 84h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.27 Pmu Pwrbtn B Pad Value (cfio_regs_pad_pmu_pwrbtn_b_PAD_VAL)—Offset 88h

PADs Memory space Value register (Access via PCU Proxy)

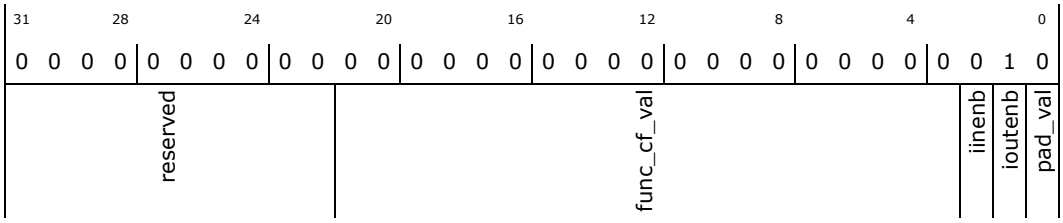
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_pwrbtn_b_PAD_VAL: [IOBASE + 2000h] + 88h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.28 Pmu Batlow B Pad Configuration (cfio_regs_pad_pmu_batlow_b_PCONF0)—Offset 90h

PADs Memory space configuration register (Access via PCU Proxy)

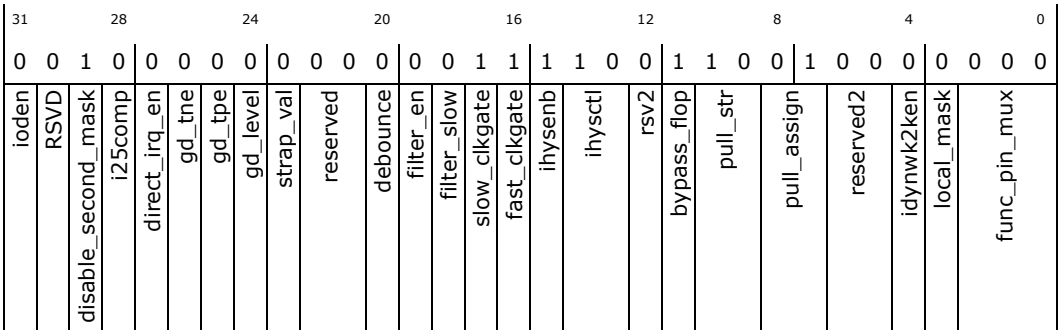
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_batlow_b_PCONF0: [IOBASE + 2000h] + 90h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_BATLOW_B

3.69.29 Pmu Batlow B Delay Line Multiplexer (cfio_regs_pad_pmu_batlow_b_PCONF1)—Offset 94h

DLL Multiplexer

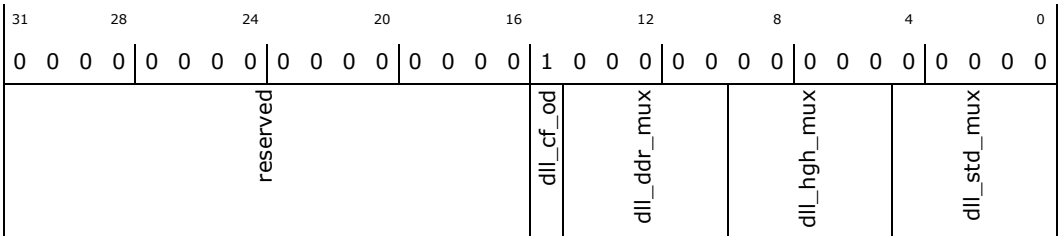
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_batlow_b_PCONF1: [IOBASE + 2000h] + 94h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.30 Pmu Batlow B Pad Value (cfio_regs_pad_pmu_batlow_b_PAD_VAL)—Offset 98h

PADs Memory space Value register (Access via PCU Proxy)

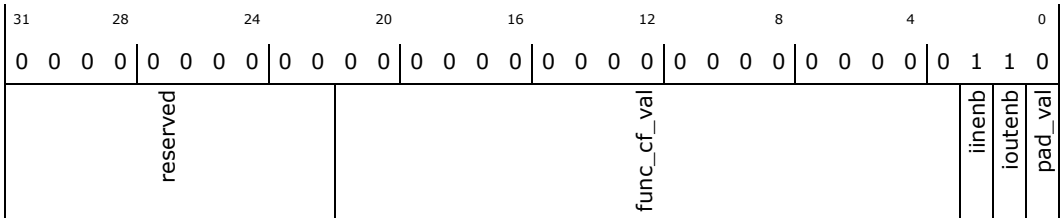
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_batlow_b_PAD_VAL: [IOBASE + 2000h] + 98h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.31 Pmu Wake Lan B Pad Configuration (cfio_regs_pad_pmu_wake_lan_b_PCONF0)—Offset A0h

PADs Memory space configuration register (Access via PCU Proxy)

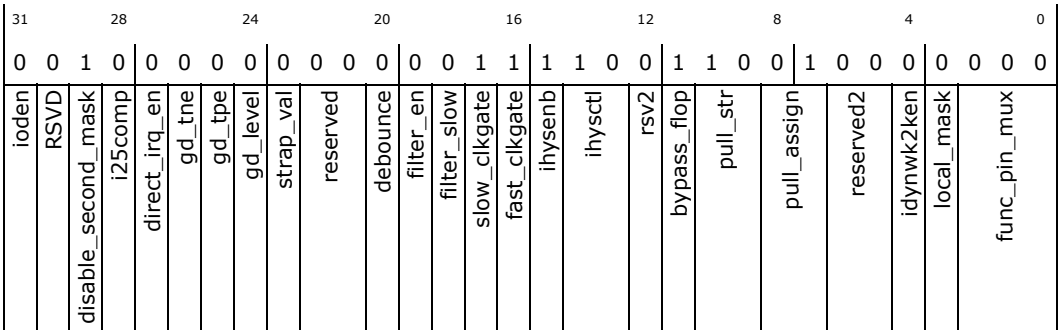
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_wake_lan_b_PCONF0: [IOBASE + 2000h] + A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_WAKE_LAN_B function 1 is GPIOS_17

3.69.32 Pmu Wake Lan B Delay Line Multiplexer (cfio_regs_pad_pmu_wake_lan_b_PCONF1)—Offset A4h

DLL Multiplexer

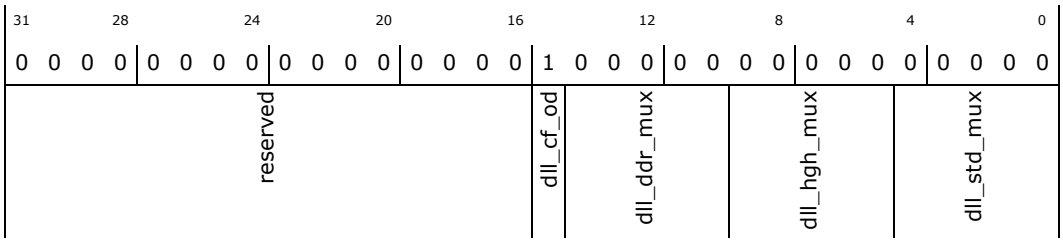
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_wake_lan_b_PCONF1: [IOBASE + 2000h] + A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.33 Pmu Wake Lan B Pad Value (cfio_regs_pad_pmu_wake_lan_b_PAD_VAL)—Offset A8h

PADs Memory space Value register (Access via PCU Proxy)

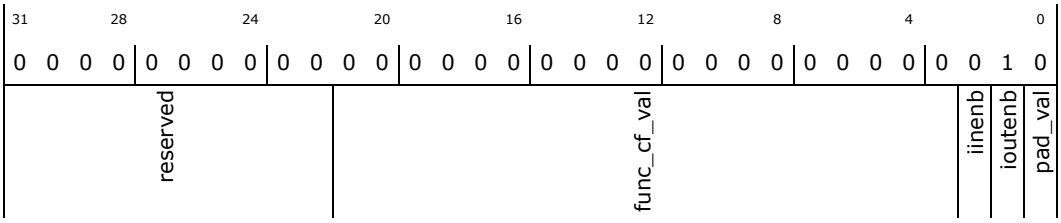
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_wake_lan_b_PAD_VAL: [IOBASE + 2000h] + A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.34 Pmu Susclk Pad Configuration (cfio_regs_pad_pmu_susclk_PCONF0)—Offset B0h

PADs Memory space configuration register (Access via PCU Proxy)

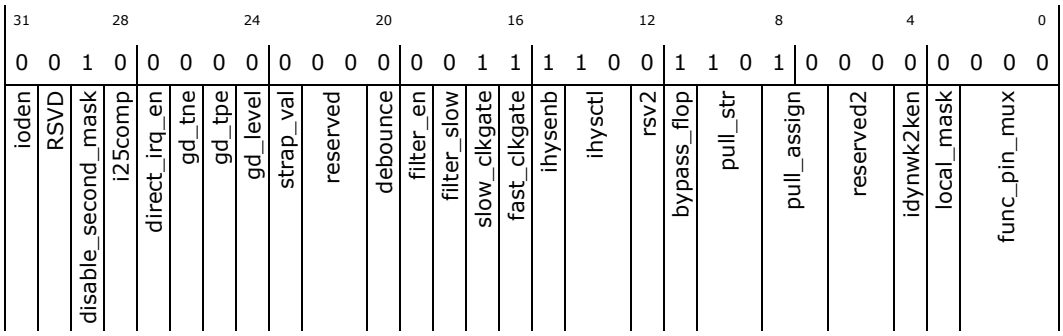
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_susclk_PCONF0: [IOBASE + 2000h] + B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_SUSCLK function 1 is GPIOS_12

3.69.35 Pmu Susclk Delay Line Multiplexer (cfio_regs_pad_pmu_susclk_PCONF1)—Offset B4h

DLL Multiplexer

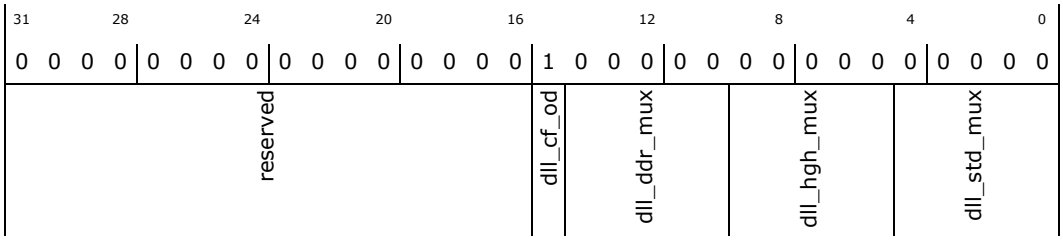
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_susclk_PCONF1: [IOBASE + 2000h] + B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.36 Pmu Susclk Pad Value (cfio_regs_pad_pmu_susclk_PAD_VAL)—Offset B8h

PADs Memory space Value register (Access via PCU Proxy)

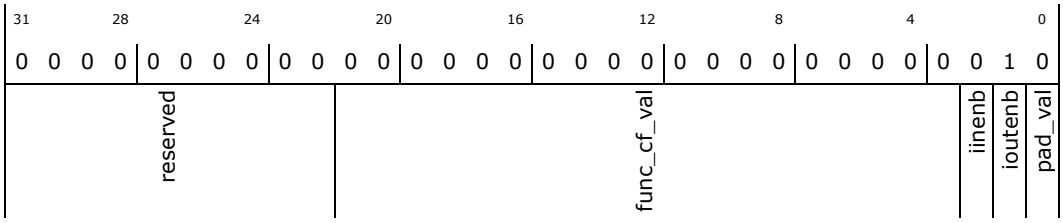
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_susclk_PAD_VAL: [IOBASE + 2000h] + B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.37 Usb Oc0 B Pad Configuration (cfio_regs_pad_usb_oc0_b_PCONF0)—Offset C0h

PADs Memory space configuration register (Access via PCU Proxy)

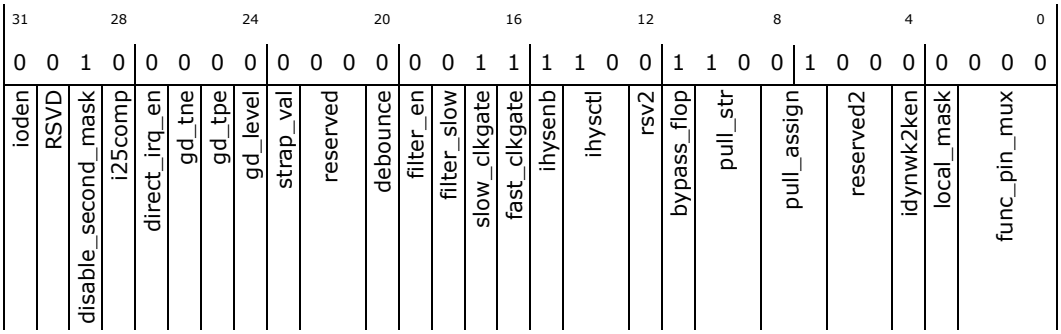
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_oc0_b_PCONF0: [IOBASE + 2000h] + C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is USB_OC0_B function 1 is GPIOS_19

3.69.38 Usb Oc0 B Delay Line Multiplexer (cfio_regs_pad_usb_oc0_b_PCONF1)—Offset C4h

DLL Multiplexer

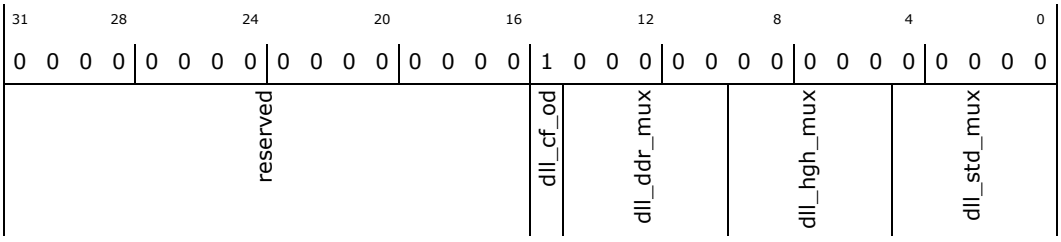
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_oc0_b_PCONF1: [IOBASE + 2000h] + C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.39 Usb Oc0 B Pad Value (cfio_regs_pad_usb_oc0_b_PAD_VAL)—Offset C8h

PADs Memory space Value register (Access via PCU Proxy)

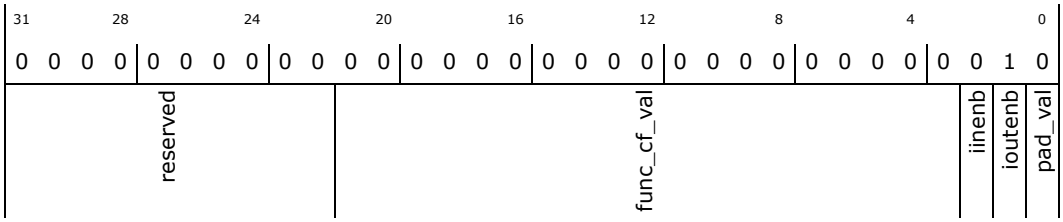
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_oc0_b_PAD_VAL: [IOBASE + 2000h] + C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.40 Pmu Slp S3 B Pad Configuration (cfio_regs_pad_pmu_slp_s3_b_PCONF0)—Offset D0h

PADs Memory space configuration register (Access via PCU Proxy)

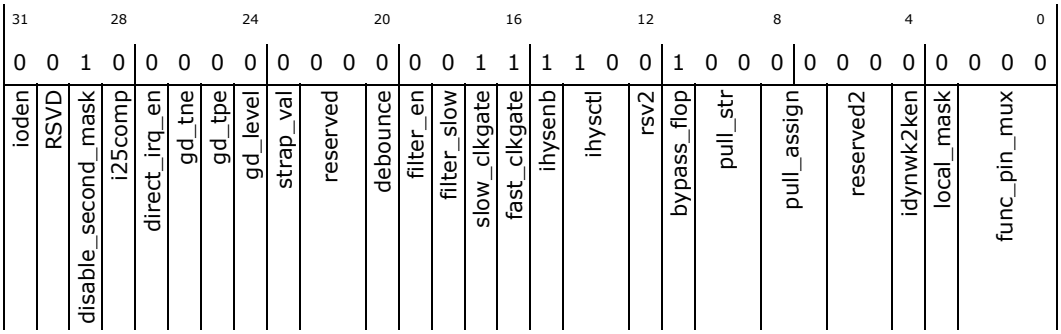
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_s3_b_PCONF0: [IOBASE + 2000h] + D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_SLP_S3_B

3.69.41 Pmu Slp S3 B Delay Line Multiplexer (cfio_regs_pad_pmu_slp_s3_b_PCONF1)—Offset D4h

DLL Multiplexer

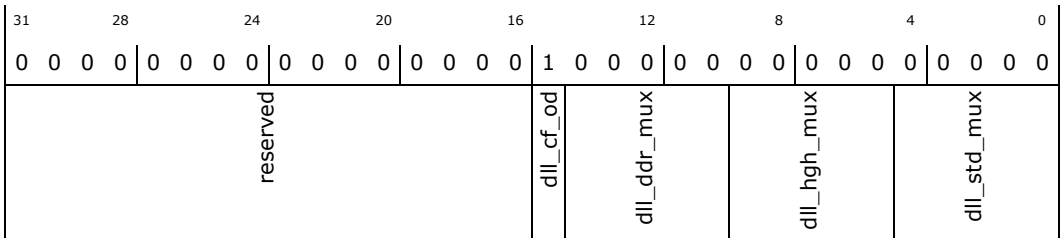
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_s3_b_PCONF1: [IOBASE + 2000h] + D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.42 Pmu Slp S3 B Pad Value (cfio_regs_pad_pmu_slp_s3_b_PAD_VAL)—Offset D8h

PADs Memory space Value register (Access via PCU Proxy)

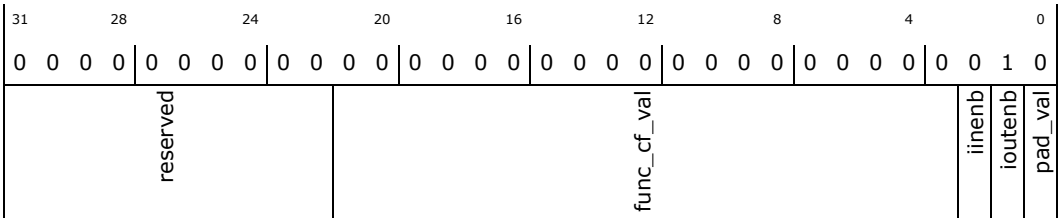
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_s3_b_PAD_VAL: [IOBASE + 2000h] + D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.43 Pmu Ac Present Pad Configuration (cfio_regs_pad_pmu_ac_present_PCONF0)—Offset E0h

PADs Memory space configuration register (Access via PCU Proxy)

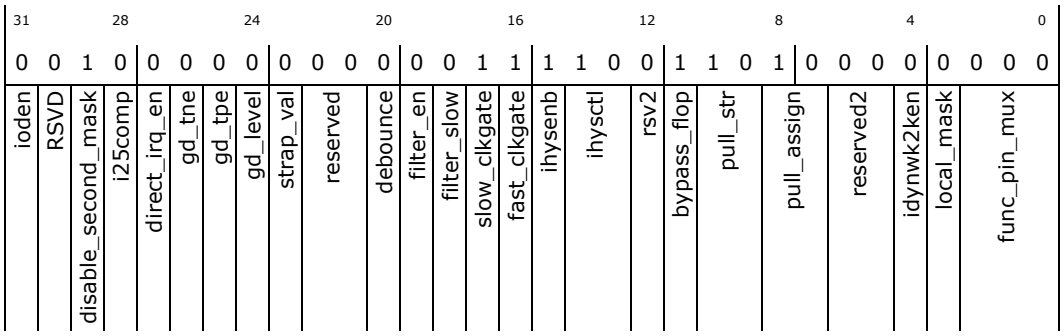
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_ac_present_PCONF0: [IOBASE + 2000h] + E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_AC_PRESENT

3.69.44 Pmu Ac Present Delay Line Multiplexer (cfio_regs_pad_pmu_ac_present_PCONF1)—Offset E4h

DLL Multiplexer

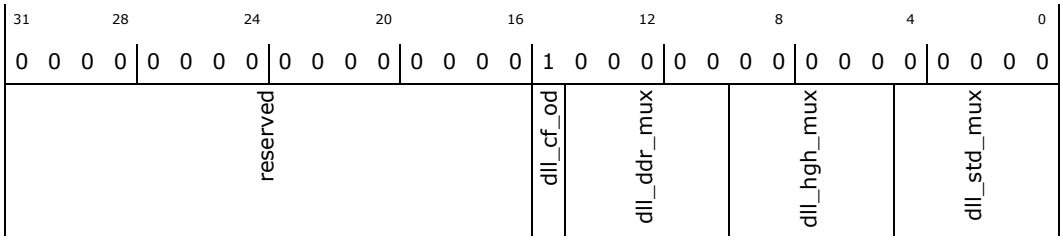
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_ac_present_PCONF1: [IOBASE + 2000h] + E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.45 Pmu Ac Present Pad Value (cfio_regs_pad_pmu_ac_present_PAD_VAL)—Offset E8h

PADs Memory space Value register (Access via PCU Proxy)

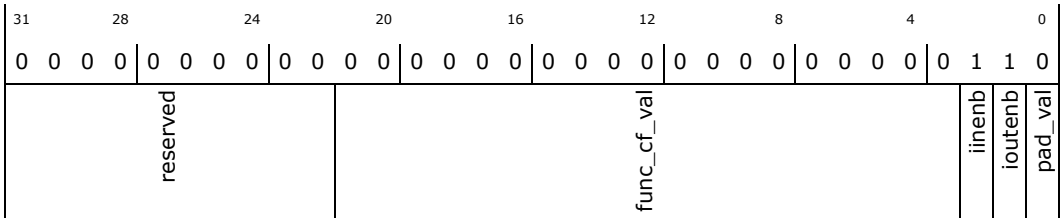
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_ac_present_PAD_VAL: [IOBASE + 2000h] + E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.46 Pmu Slp S4 B Pad Configuration (cfio_regs_pad_pmu_slp_s4_b_PCONF0)—Offset F0h

PADs Memory space configuration register (Access via PCU Proxy)

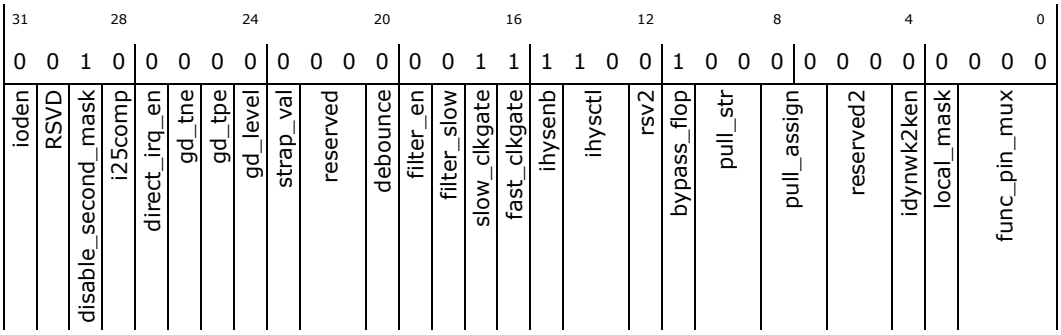
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_s4_b_PCONF0: [IOBASE + 2000h] + F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_SLP_S4_B

3.69.47 Pmu Slp S4 B Delay Line Multiplexer (cfio_regs_pad_pmu_slp_s4_b_PCONF1)—Offset F4h

DLL Multiplexer

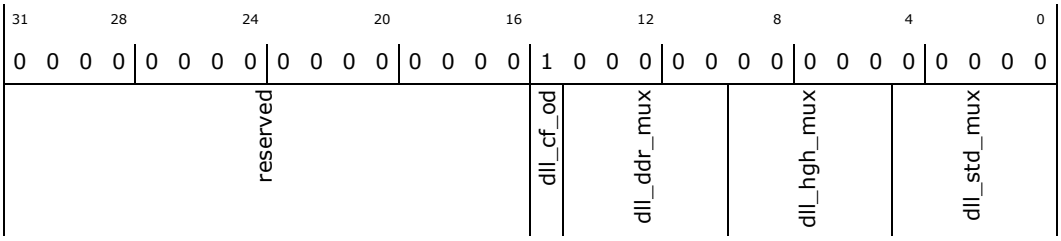
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_s4_b_PCONF1: [IOBASE + 2000h] + F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.48 Pmu Slp S4 B Pad Value (cfio_regs_pad_pmu_slp_s4_b_PAD_VAL)—Offset F8h

PADs Memory space Value register (Access via PCU Proxy)

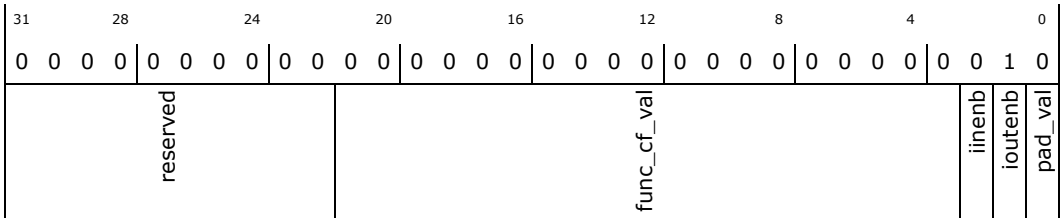
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_s4_b_PAD_VAL: [IOBASE + 2000h] + F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.49 Pmu Pltrst B Pad Configuration (cfio_regs_pad_pmu_pltrst_b_PCONF0)—Offset 100h

PADs Memory space configuration register (Access via PCU Proxy)

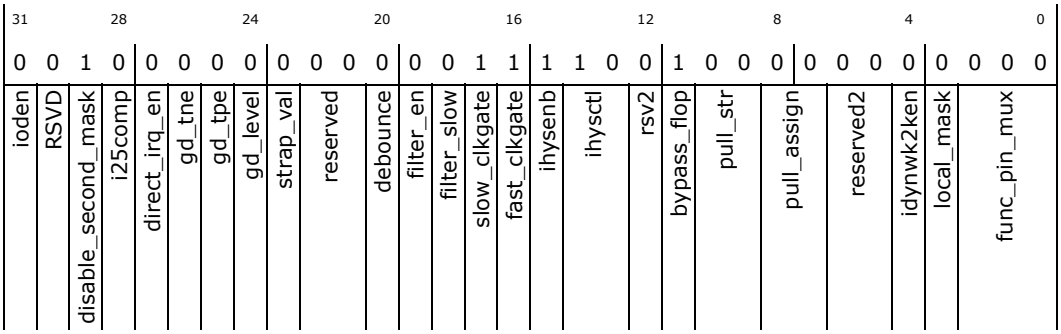
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_pltrst_b_PCONF0: [IOBASE + 2000h] + 100h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_PLTRST_B

3.69.50 Pmu Pltrst B Delay Line Multiplexer (cfio_regs_pad_pmu_pltrst_b_PCONF1)—Offset 104h

DLL Multiplexer

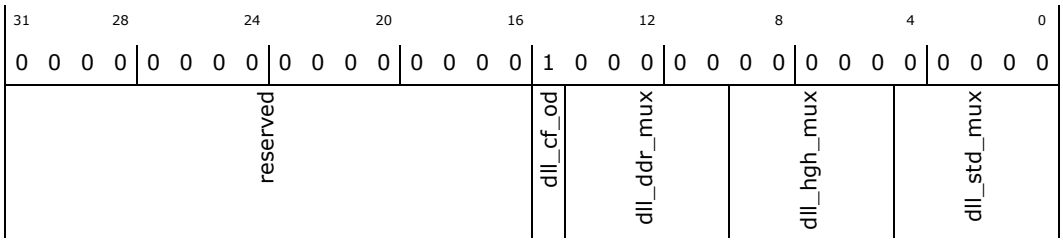
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_pltrst_b_PCONF1: [IOBASE + 2000h] + 104h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.51 Pmu Pltrst B Pad Value (cfio_regs_pad_pmu_pltrst_b_PAD_VAL)—Offset 108h

PADs Memory space Value register (Access via PCU Proxy)

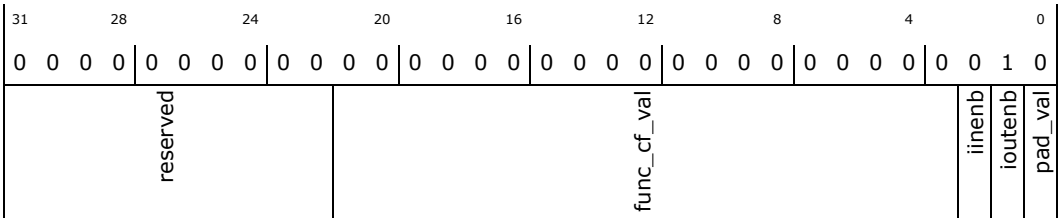
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_pltrst_b_PAD_VAL: [IOBASE + 2000h] + 108h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.52 Pmu Slp Lan B Pad Configuration (cfio_regs_pad_pmu_slp_lan_b_PCONF0)—Offset 110h

PADs Memory space configuration register (Access via PCU Proxy)

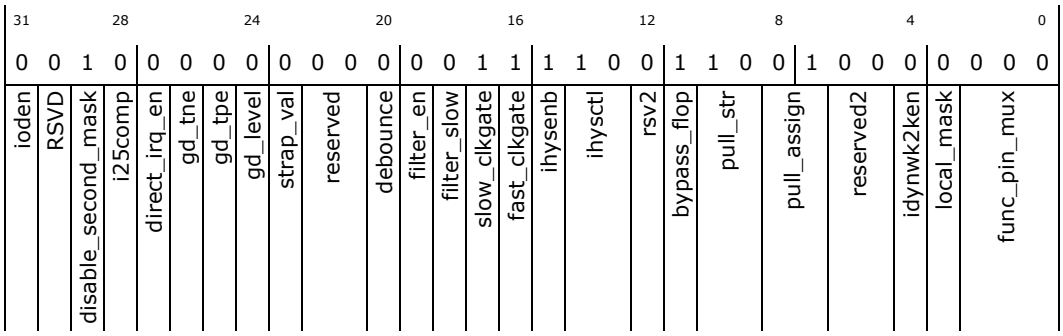
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

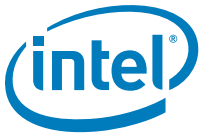
cfio_regs_pad_pmu_slp_lan_b_PCONF0: [IOBASE + 2000h] + 110h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq



Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_SLP_LAN_B function 1 is GPIOS_14 function 2 is ULPI_RESET_N

3.69.53 Pmu Slp Lan B Delay Line Multiplexer (cfio_regs_pad_pmu_slp_lan_b_PCONF1)—Offset 114h

DLL Multiplexer

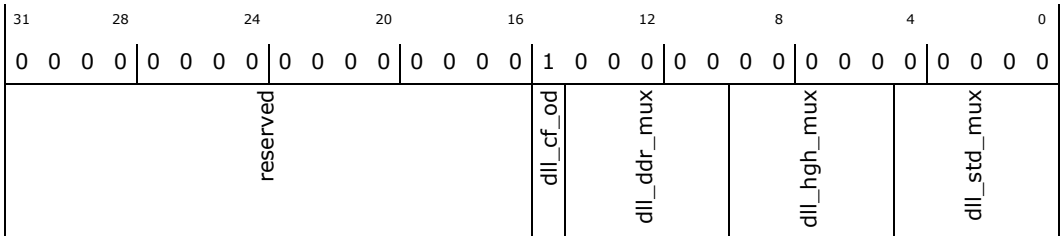
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_lan_b_PCONF1: [IOBASE + 2000h] + 114h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.54 Pmu Slp Lan B Pad Value (cfio_regs_pad_pmu_slp_lan_b_PAD_VAL)—Offset 118h

PADs Memory space Value register (Access via PCU Proxy)

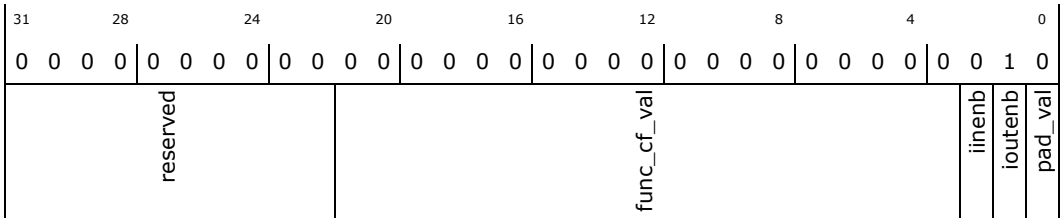
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_lan_b_PAD_VAL: [IOBASE + 2000h] + 118h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.55 Sec Gpio Sus10 Pad Configuration (cfio_regs_pad_sec_gpio_sus10_PCONF0)—Offset 120h

PADs Memory space configuration register (Access via PCU Proxy)

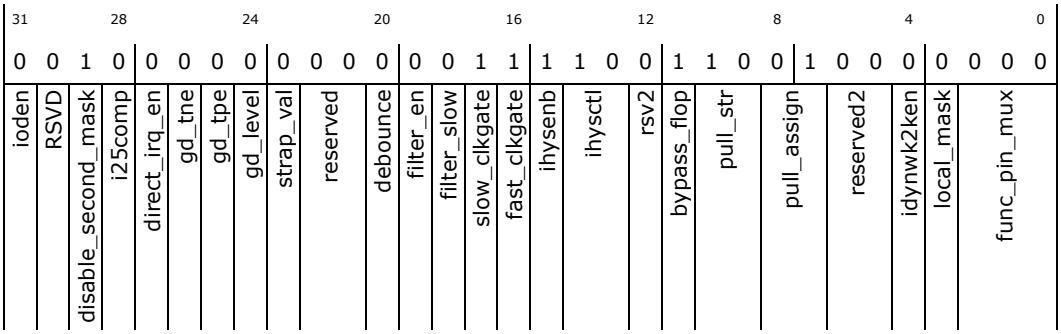
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sec_gpio_sus10_PCONF0: [IOBASE + 2000h] + 120h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is SEC_GPIO_SUS10 function 1 is Unused function 2 is USH_HBP[12] function 3 is MCSI_LPDEBUG[0] For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10 function 4 is DUN0_MISR_ECC_OUT_A function 5 is DUN1_MISR_ECC_OUT_A

3.69.56 Sec Gpio Sus10 Delay Line Multiplexer (cfio_regs_pad_sec_gpio_sus10_PCONF1)—Offset 124h

DLL Multiplexer

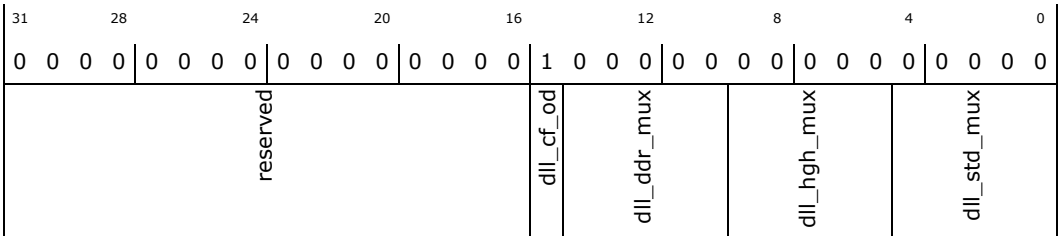
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sec_gpio_sus10_PCONF1: [IOBASE + 2000h] + 124h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux

Bit Range	Default & Access	Description
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.57 Sec Gpio Sus10 Pad Value (cfio_regs_pad_sec_gpio_sus10_PAD_VAL)—Offset 128h

PADs Memory space Value register (Access via PCU Proxy)

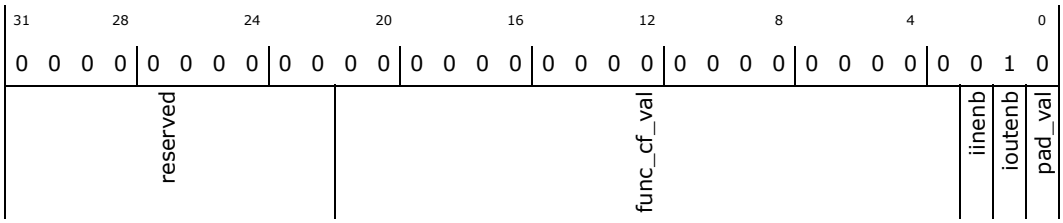
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sec_gpio_sus10_PAD_VAL: [IOBASE + 2000h] + 128h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.58 Sus Stat B Pad Configuration (cfio_regs_pad_sus_stat_b_PCONF0)—Offset 130h

PADs Memory space configuration register (Access via PCU Proxy)

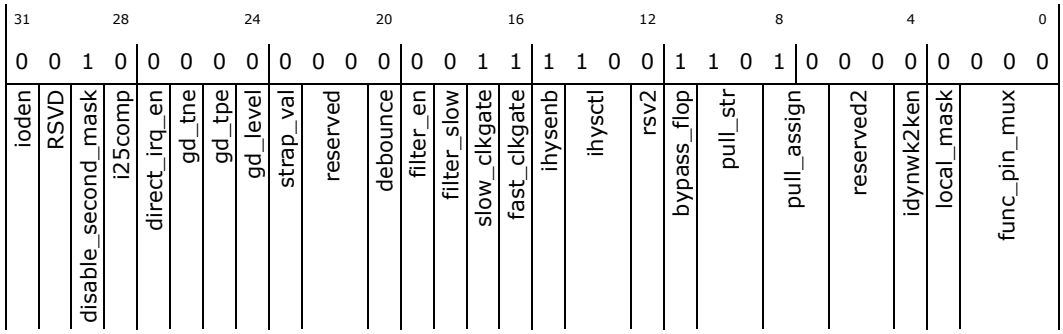
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sus_stat_b_PCONF0: [IOBASE + 2000h] + 130h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register

Bit Range	Default & Access	Description
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is SUS_STAT_B function 1 is GPIOS_18

3.69.59 Sus Stat B Delay Line Multiplexer (cfio_regs_pad_sus_stat_b_PCONF1)—Offset 134h

DLL Multiplexer

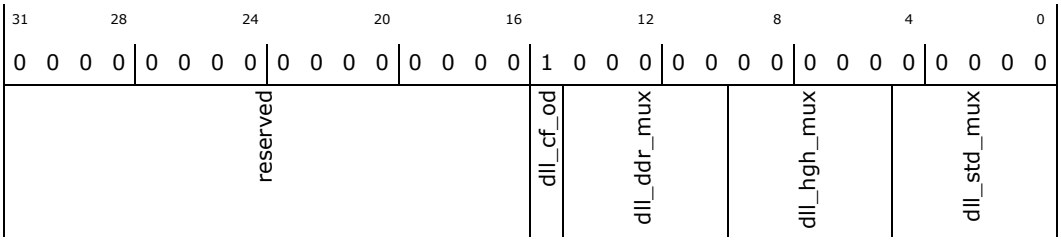
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sus_stat_b_PCONF1: [IOBASE + 2000h] + 134h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.60 Sus Stat B Pad Value (cfio_regs_pad_sus_stat_b_PAD_VAL)—Offset 138h

PADs Memory space Value register (Access via PCU Proxy)

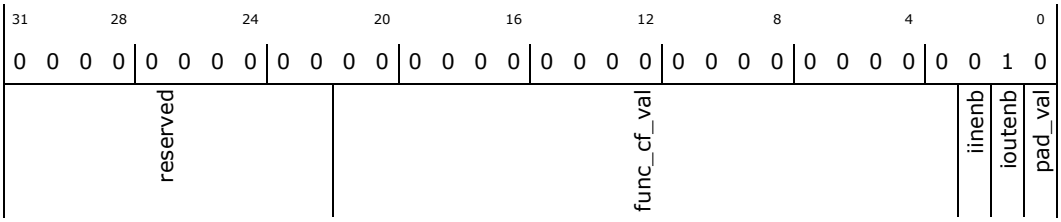
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sus_stat_b_PAD_VAL: [IOBASE + 2000h] + 138h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.61 Pmu Slp S0ix B Pad Configuration (cfio_regs_pad_pmu_slp_s0ix_b_PCONF0)—Offset 140h

PADs Memory space configuration register (Access via PCU Proxy)

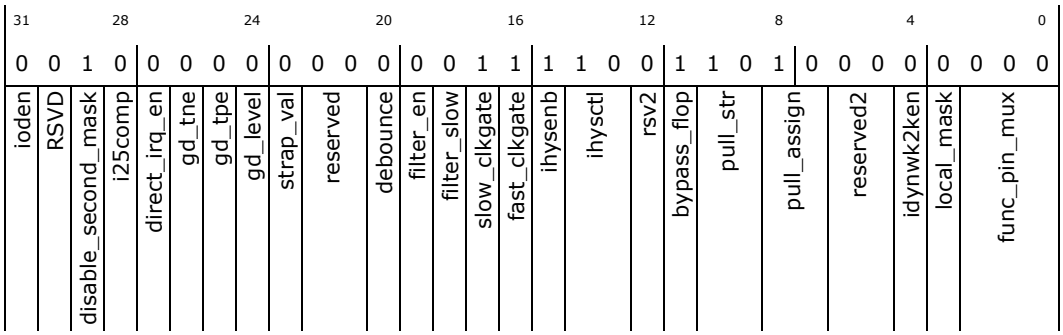
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_s0ix_b_PCONF0: [IOBASE + 2000h] + 140h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is PMU_SLP_S0IX_B function 1 is GPIOS_13

3.69.62 Pmu Slp S0ix B Delay Line Multiplexer (cfio_regs_pad_pmu_slp_s0ix_b_PCONF1)—Offset 144h

DLL Multiplexer

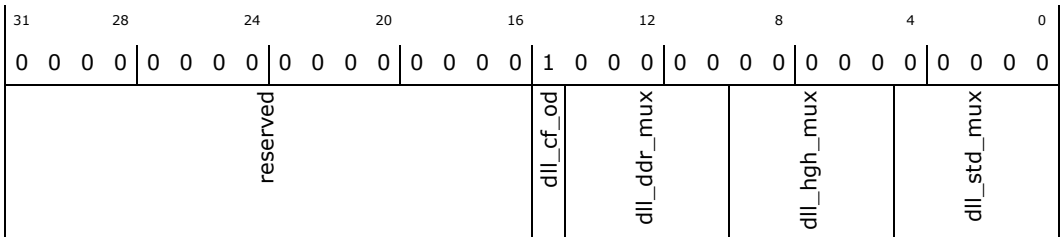
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_s0ix_b_PCONF1: [IOBASE + 2000h] + 144h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.63 Pmu Slp S0ix B Pad Value (cfio_regs_pad_pmu_slp_s0ix_b_PAD_VAL)—Offset 148h

PADs Memory space Value register (Access via PCU Proxy)

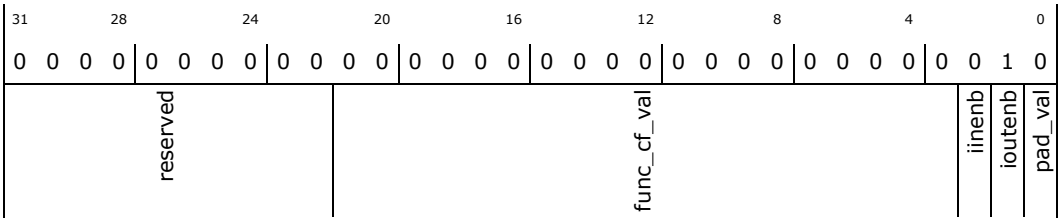
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_pmu_slp_s0ix_b_PAD_VAL: [IOBASE + 2000h] + 148h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.64 Gpio Dfx5 Pad Configuration (cfio_regs_pad_gpio_dfx5_PCONF0)—Offset 150h

PADs Memory space configuration register (Access via PCU Proxy)

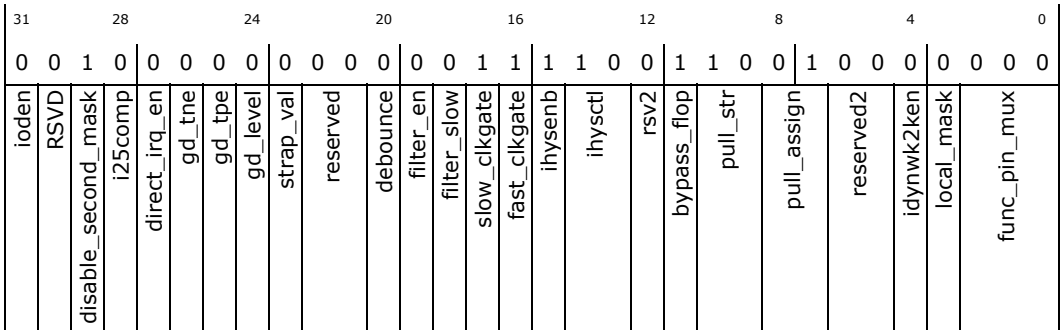
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx5_PCONF0: [IOBASE + 2000h] + 150h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_27 function 1 is SUS_OBS_4 function 2 is USH_CRC_RESET function 3 is ICLKPH1 function 4 is GCLKPH function 5 is Cx_BPM0_TX

3.69.65 Gpio Dfx5 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx5_PCONF1)—Offset 154h

DLL Multiplexer

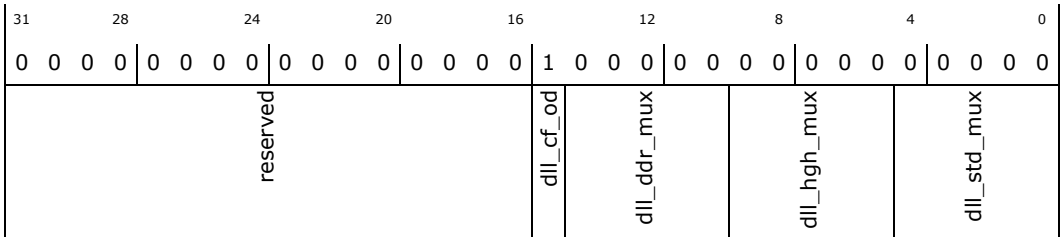
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx5_PCONF1: [IOBASE + 2000h] + 154h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.66 Gpio Dfx5 Pad Value (cfio_regs_pad_gpio_dfx5_PAD_VAL)—Offset 158h

PADs Memory space Value register (Access via PCU Proxy)

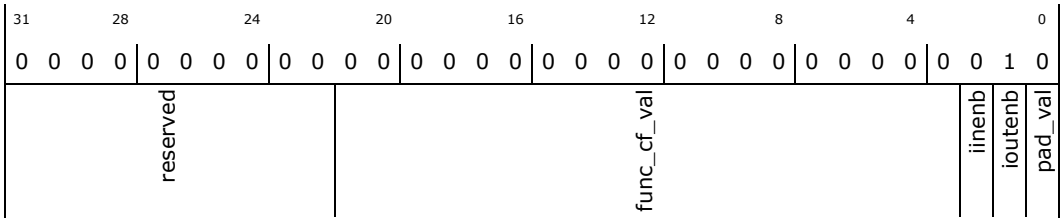
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx5_PAD_VAL: [IOBASE + 2000h] + 158h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.67 Gpio Dfx4 Pad Configuration (cfio_regs_pad_gpio_dfx4_PCONF0)—Offset 160h

PADs Memory space configuration register (Access via PCU Proxy)

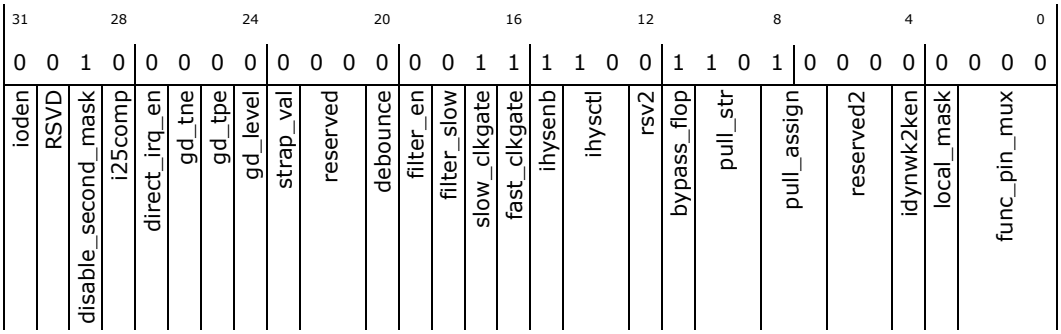
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx4_PCONF0: [IOBASE + 2000h] + 160h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_26 function 1 is SUS_OBS_3 function 2 is EXT_TRIG0 function 3 is ICLKPH0 function 4 is HCLKPH function 5 is Cx_BPM3_TX

3.69.68 Gpio Dfx4 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx4_PCONF1)—Offset 164h

DLL Multiplexer

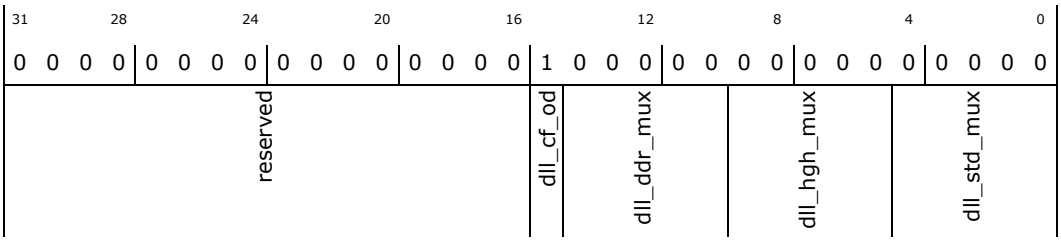
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx4_PCONF1: [IOBASE + 2000h] + 164h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.69 Gpio Dfx4 Pad Value (cfio_regs_pad_gpio_dfx4_PAD_VAL)—Offset 168h

PADs Memory space Value register (Access via PCU Proxy)

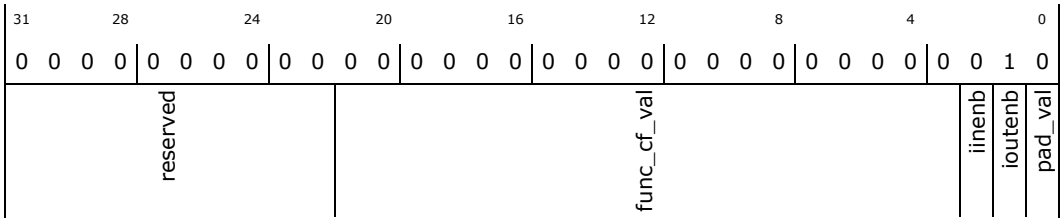
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx4_PAD_VAL: [IOBASE + 2000h] + 168h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.70 Gpio Dfx0 Pad Configuration (cfio_regs_pad_gpio_dfx0_PCONF0)—Offset 170h

PADs Memory space configuration register (Access via PCU Proxy)

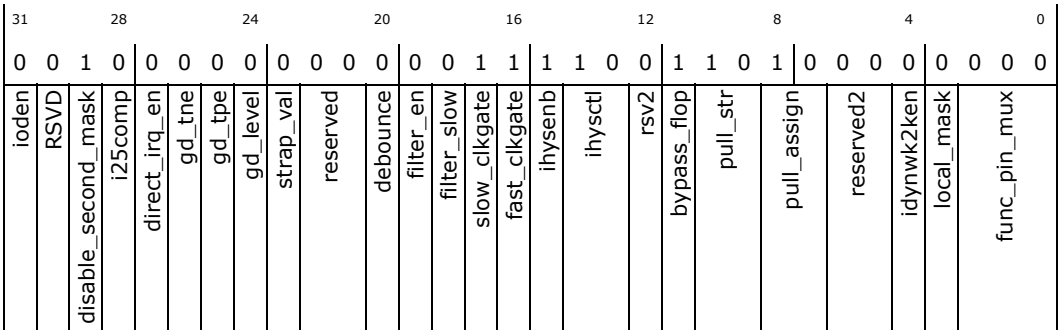
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx0_PCONF0: [IOBASE + 2000h] + 170h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_22 function 1 is SUS_VALID function 2 is Unused function 3 is CCLKPH0[0] function 4 is HFPLLN function 5 is CRTDAC_CNT

3.69.71 Gpio Dfx0 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx0_PCONF1)—Offset 174h

DLL Multiplexer

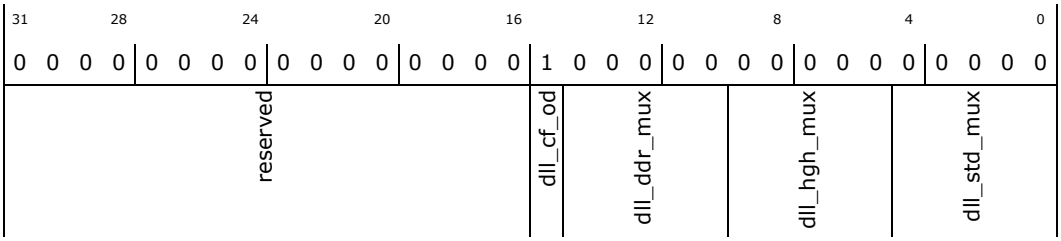
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx0_PCONF1: [IOBASE + 2000h] + 174h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.72 Gpio Dfx0 Pad Value (cfio_regs_pad_gpio_dfx0_PAD_VAL)—Offset 178h

PADs Memory space Value register (Access via PCU Proxy)

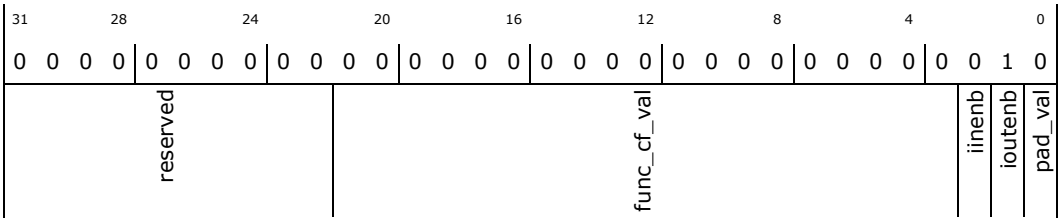
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx0_PAD_VAL: [IOBASE + 2000h] + 178h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.73 Gpio Dfx6 Pad Configuration (cfio_regs_pad_gpio_dfx6_PCONF0)—Offset 180h

PADs Memory space configuration register (Access via PCU Proxy)

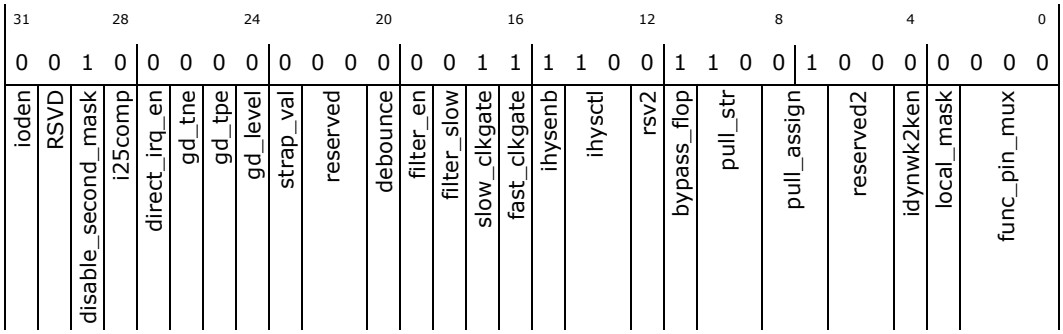
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx6_PCONF0: [IOBASE + 2000h] + 180h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_28 function 1 is SUS_OBS_5 function 2 is IERR function 3 is DCLKPH[0] function 4 is ICLKPH0 function 5 is Cx_BPM1_TX

3.69.74 Gpio Dfx6 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx6_PCONF1)—Offset 184h

DLL Multiplexer

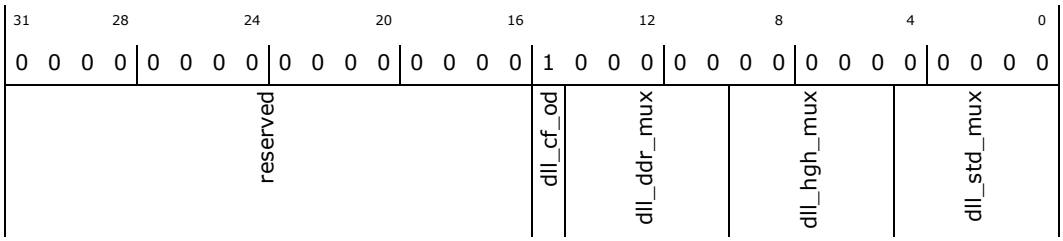
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx6_PCONF1: [IOBASE + 2000h] + 184h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.75 Gpio Dfx6 Pad Value (cfio_regs_pad_gpio_dfx6_PAD_VAL)—Offset 188h

PADs Memory space Value register (Access via PCU Proxy)

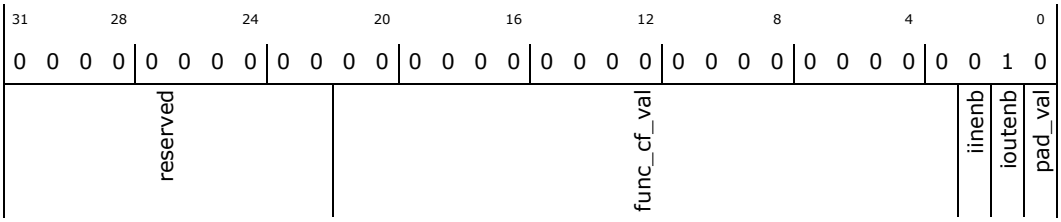
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx6_PAD_VAL: [IOBASE + 2000h] + 188h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.76 Gpio Dfx7 Pad Configuration (cfio_regs_pad_gpio_dfx7_PCONF0)—Offset 190h

PADs Memory space configuration register (Access via PCU Proxy)

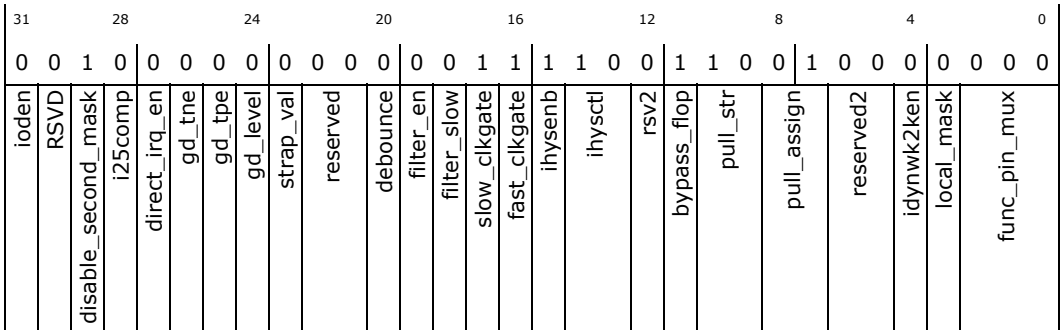
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx7_PCONF0: [IOBASE + 2000h] + 190h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_29 function 1 is SUS_OBS_6 function 2 is EXT_TRIG1 function 3 is HFPLLN function 4 is ICLKPH1 function 5 is Cx_BPM2_TX

3.69.77 Gpio Dfx7 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx7_PCONF1)—Offset 194h

DLL Multiplexer

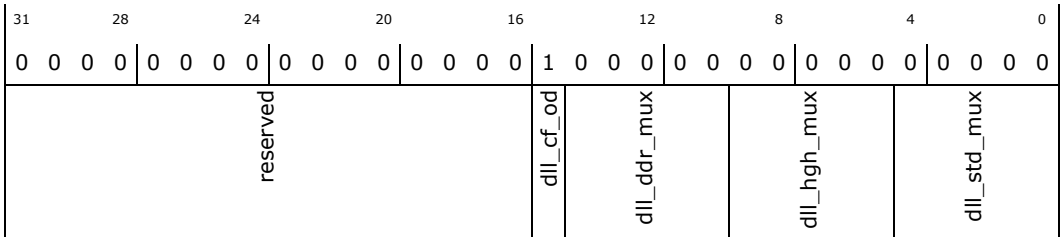
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx7_PCONF1: [IOBASE + 2000h] + 194h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.78 Gpio Dfx7 Pad Value (cfio_regs_pad_gpio_dfx7_PAD_VAL)—Offset 198h

PADs Memory space Value register (Access via PCU Proxy)

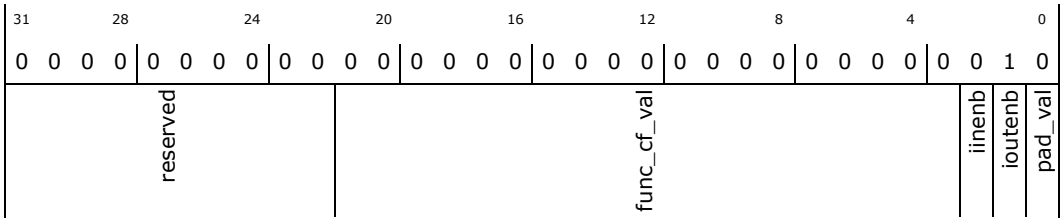
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx7_PAD_VAL: [IOBASE + 2000h] + 198h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.79 Gpio Dfx8 Pad Configuration (cfio_regs_pad_gpio_dfx8_PCONF0)—Offset 1A0h

PADs Memory space configuration register (Access via PCU Proxy)

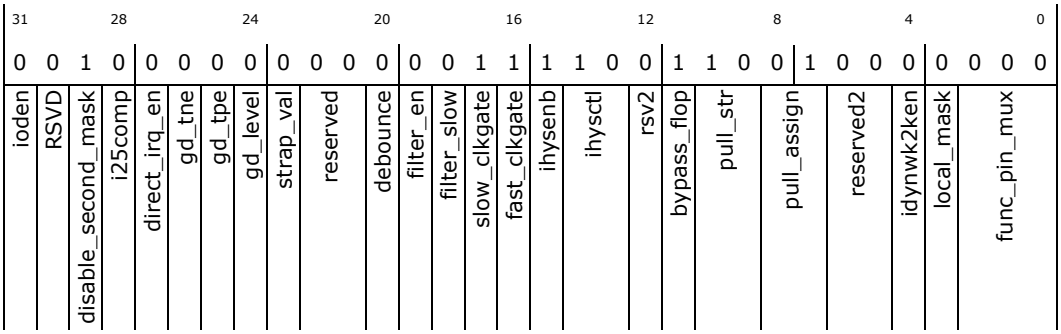
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx8_PCONF0: [IOBASE + 2000h] + 1A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_30 function 1 is SUS_OBS_7 function 2 is SECTAP_TDO function 3 is CCK_ACLKPH function 4 is DCLKPH[1] function 5 is Cx_BPM3_TX

3.69.80 Gpio Dfx8 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx8_PCONF1)—Offset 1A4h

DLL Multiplexer

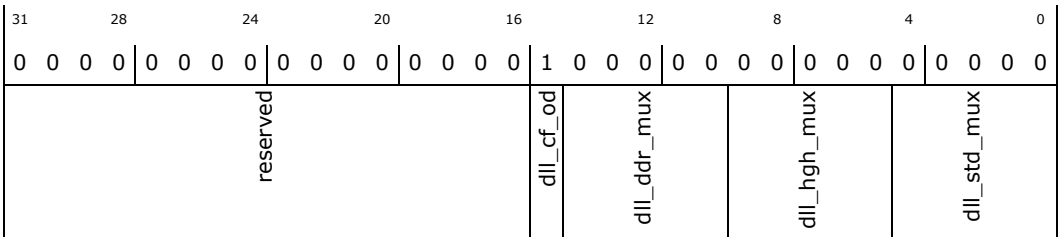
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx8_PCONF1: [IOBASE + 2000h] + 1A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.81 Gpio Dfx8 Pad Value (cfio_regs_pad_gpio_dfx8_PAD_VAL)—Offset 1A8h

PADs Memory space Value register (Access via PCU Proxy)

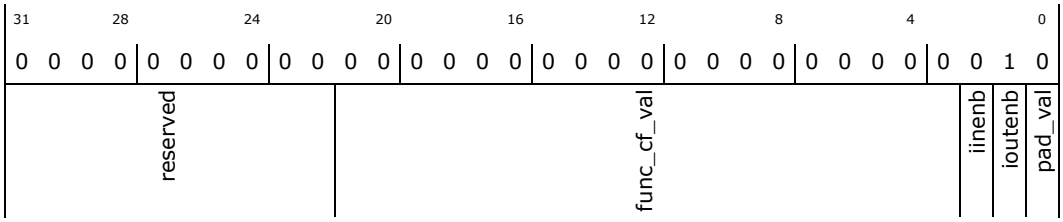
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx8_PAD_VAL: [IOBASE + 2000h] + 1A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.82 Gpio Dfx3 Pad Configuration (cfio_regs_pad_gpio_dfx3_PCONF0)—Offset 1B0h

PADs Memory space configuration register (Access via PCU Proxy)

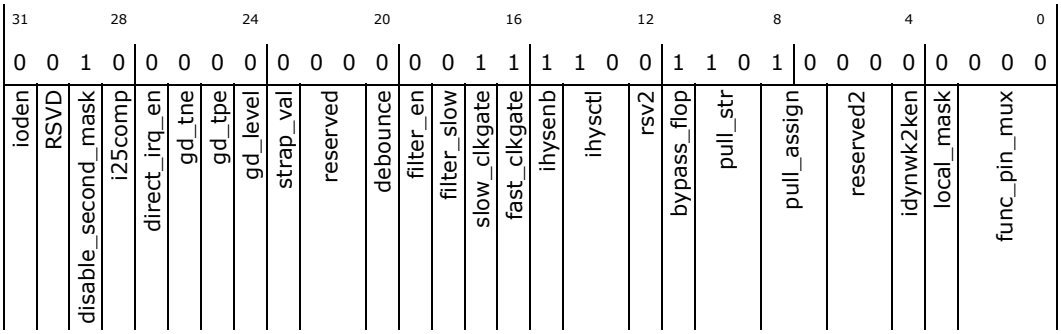
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx3_PCONF0: [IOBASE + 2000h] + 1B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_25 function 1 is SUS_OBS_2 function 2 is SECTAP_TDO function 3 is GCLKPH function 4 is CCLKPH1[1] function 5 is Cx_BPM2_TX

3.69.83 Gpio Dfx3 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx3_PCONF1)—Offset 1B4h

DLL Multiplexer

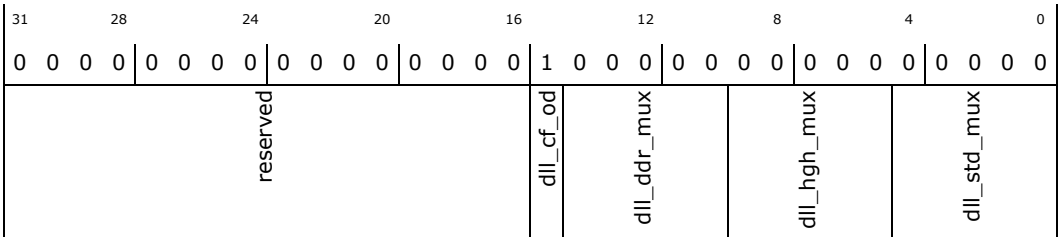
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx3_PCONF1: [IOBASE + 2000h] + 1B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.84 Gpio Dfx3 Pad Value (cfio_regs_pad_gpio_dfx3_PAD_VAL)—Offset 1B8h

PADs Memory space Value register (Access via PCU Proxy)

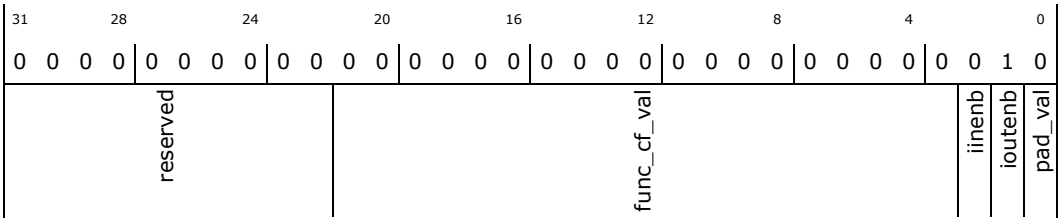
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx3_PAD_VAL: [IOBASE + 2000h] + 1B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.85 Gpio Dfx2 Pad Configuration (cfio_regs_pad_gpio_dfx2_PCONF0)—Offset 1C0h

PADs Memory space configuration register (Access via PCU Proxy)

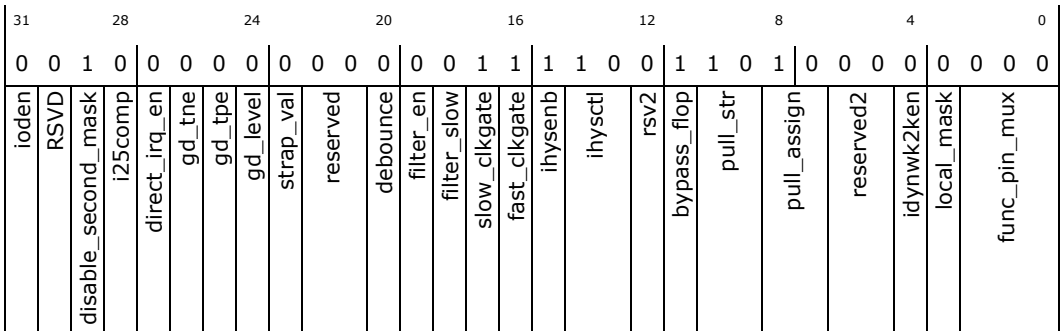
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx2_PCONF0: [IOBASE + 2000h] + 1C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_24 function 1 is SUS_OBS_1 function 2 is CRTSER_OUT function 3 is HCLKPH function 4 is CCLKPH0[1] function 5 is Cx_BPM1_TX

3.69.86 Gpio Dfx2 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx2_PCONF1)—Offset 1C4h

DLL Multiplexer

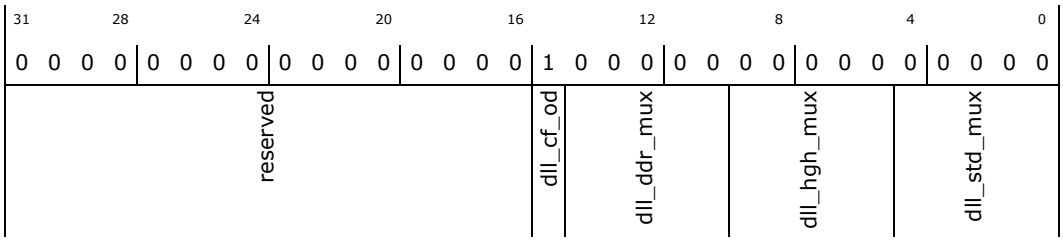
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx2_PCONF1: [IOBASE + 2000h] + 1C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.87 Gpio Dfx2 Pad Value (cfio_regs_pad_gpio_dfx2_PAD_VAL)—Offset 1C8h

PADs Memory space Value register (Access via PCU Proxy)

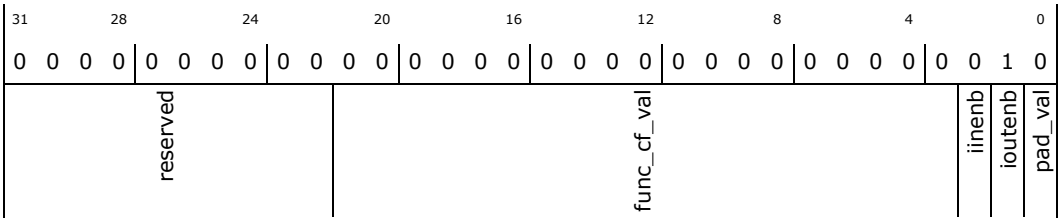
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx2_PAD_VAL: [IOBASE + 2000h] + 1C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.88 Gpio Sus0 Pad Configuration (cfio_regs_pad_gpio_sus0_PCONF0)—Offset 1D0h

PADs Memory space configuration register (Access via PCU Proxy)

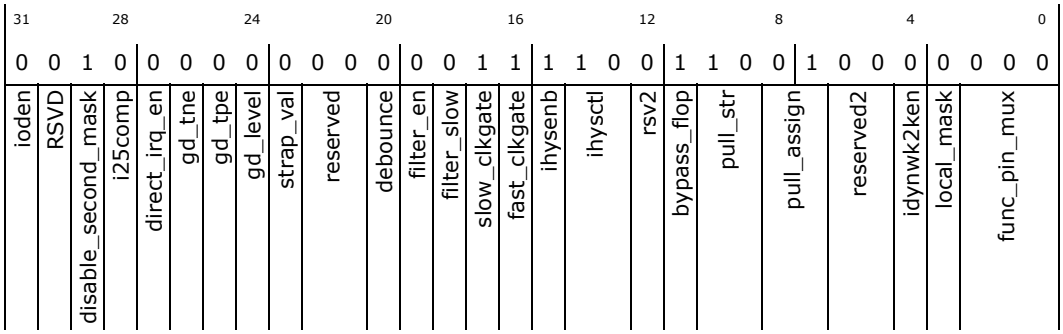
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus0_PCONF0: [IOBASE + 2000h] + 1D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIO_SUS0 function 1 is RO_BYPASS

3.69.89 Gpio Sus0 Delay Line Multiplexer (cfio_regs_pad_gpio_sus0_PCONF1)—Offset 1D4h

DLL Multiplexer

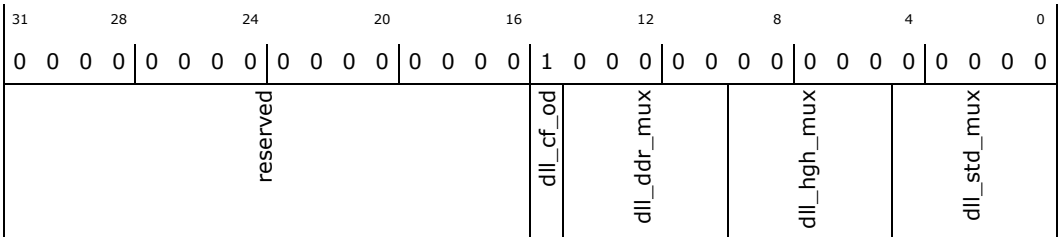
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus0_PCONF1: [IOBASE + 2000h] + 1D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.90 Gpio Sus0 Pad Value (cfio_regs_pad_gpio_sus0_PAD_VAL)—Offset 1D8h

PADs Memory space Value register (Access via PCU Proxy)

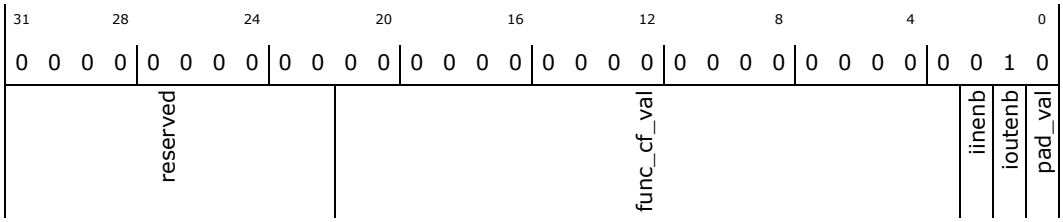
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus0_PAD_VAL: [IOBASE + 2000h] + 1D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.91 Gpio Sus2 Pad Configuration (cfio_regs_pad_gpio_sus2_PCONF0)—Offset 1E0h

PADs Memory space configuration register (Access via PCU Proxy)

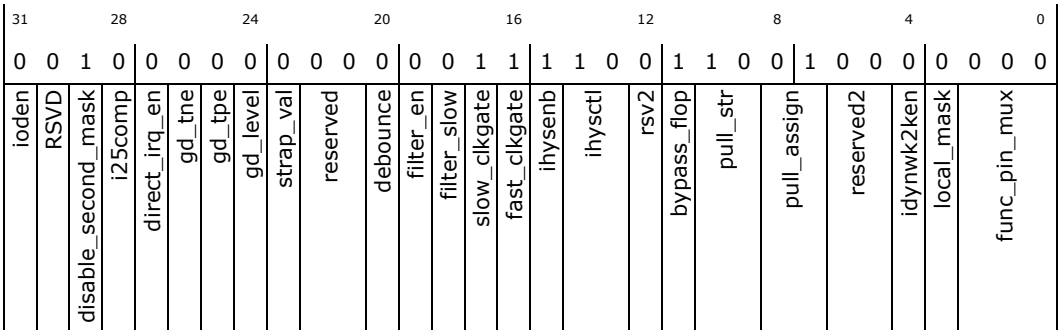
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus2_PCONF0: [IOBASE + 2000h] + 1E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIO_SUS2 function 1 is SEC_TMS function 2 is USH_HBP[19] function 3 is SSA_MISR_DATA_OUT function 4 is DUN0_MISR_CMD_OUT_B function 5 is DUN1_MISR_CMD_OUT_B function 6 is PCI_WAKE2_B function 7 is DFX_VISA_OBS0

3.69.92 Gpio Sus2 Delay Line Multiplexer (cfio_regs_pad_gpio_sus2_PCONF1)—Offset 1E4h

DLL Multiplexer

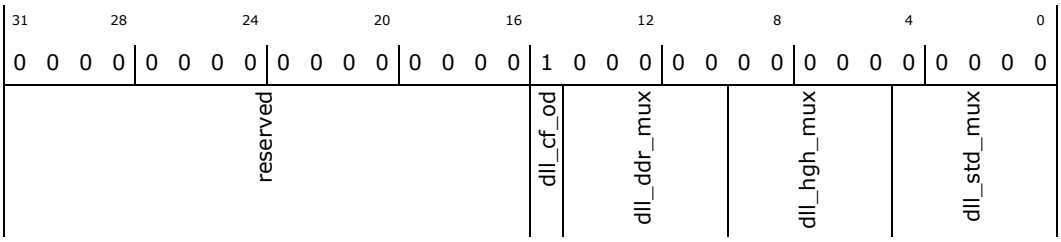
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus2_PCONF1: [IOBASE + 2000h] + 1E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.93 Gpio Sus2 Pad Value (cfio_regs_pad_gpio_sus2_PAD_VAL)—Offset 1E8h

PADs Memory space Value register (Access via PCU Proxy)

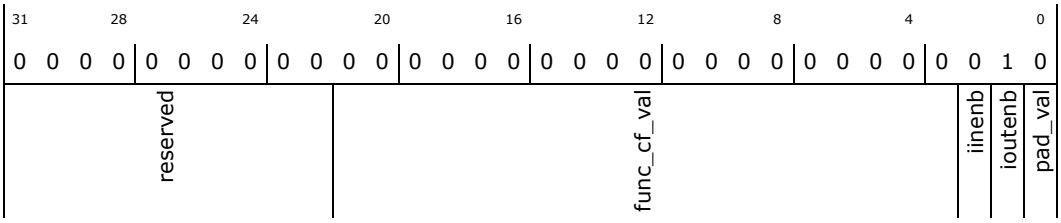
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus2_PAD_VAL: [IOBASE + 2000h] + 1E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.94 Gpio Sus3 Pad Configuration (cfio_regs_pad_gpio_sus3_PCONF0)—Offset 1F0h

PADs Memory space configuration register (Access via PCU Proxy)

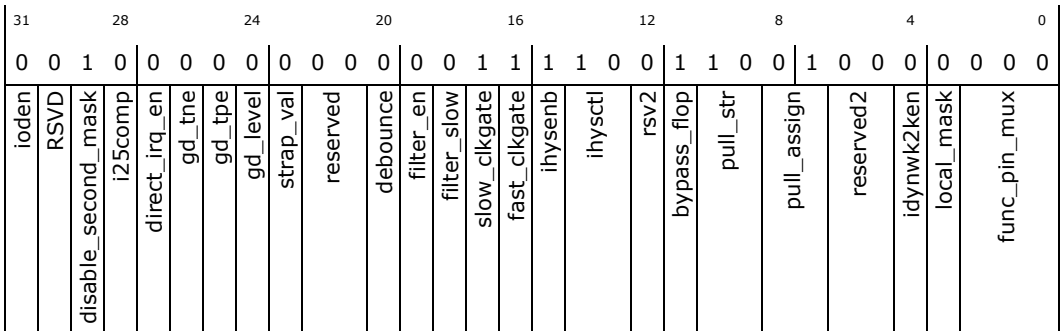
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus3_PCONF0: [IOBASE + 2000h] + 1F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIO_SUS3 function 1 is SEC_TDI function 2 is USH_HBP[18] function 3 is SSA_MISR_S2CREQ function 4 is DUN0_MISR_ECC_OUT_B function 5 is DUN1_MISR_ECC_OUT_B function 6 is PCI_WAKE3_B function 7 is DFX_VISA_OBS1

3.69.95 Gpio Sus3 Delay Line Multiplexer (cfio_regs_pad_gpio_sus3_PCONF1)—Offset 1F4h

DLL Multiplexer

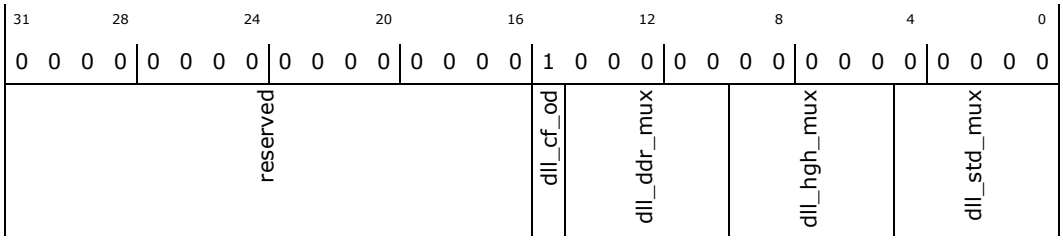
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus3_PCONF1: [IOBASE + 2000h] + 1F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux

Bit Range	Default & Access	Description
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.96 Gpio Sus3 Pad Value (cfio_regs_pad_gpio_sus3_PAD_VAL)—Offset 1F8h

PADs Memory space Value register (Access via PCU Proxy)

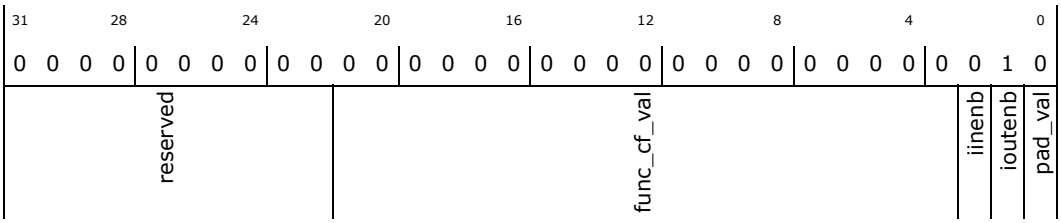
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus3_PAD_VAL: [IOBASE + 2000h] + 1F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.97 Gpio Sus4 Pad Configuration (cfio_regs_pad_gpio_sus4_PCONF0)—Offset 200h

PADs Memory space configuration register (Access via PCU Proxy)

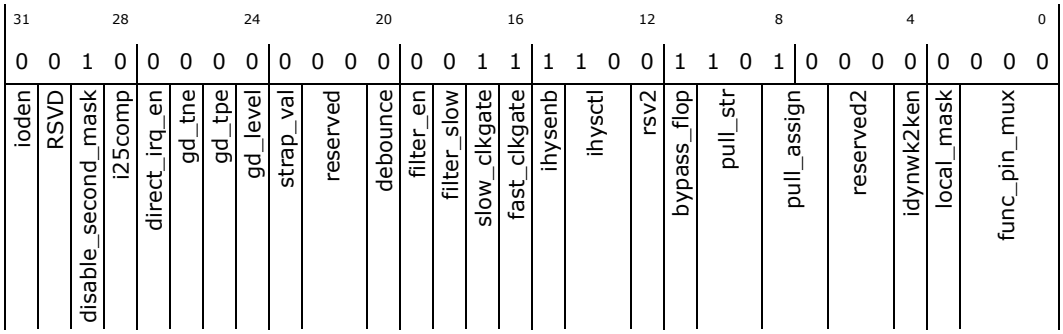
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus4_PCONF0: [IOBASE + 2000h] + 200h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register

Bit Range	Default & Access	Description
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIO_SUS4 function 1 is SEC_TDO function 2 is USH_HPB[17] function 3 is SSA_MISR_S2CDAT function 4 is Unused function 5 is Unused function 6 is Unused function 7 is DFX_VISA_OBS2

3.69.98 Gpio Sus4 Delay Line Multiplexer (cfio_regs_pad_gpio_sus4_PCONF1)—Offset 204h

DLL Multiplexer

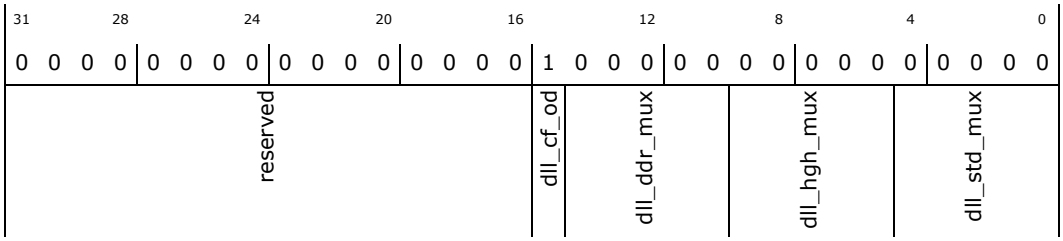
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus4_PCONF1: [IOBASE + 2000h] + 204h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.99 Gpio Sus4 Pad Value (cfio_regs_pad_gpio_sus4_PAD_VAL)—Offset 208h

PADs Memory space Value register (Access via PCU Proxy)

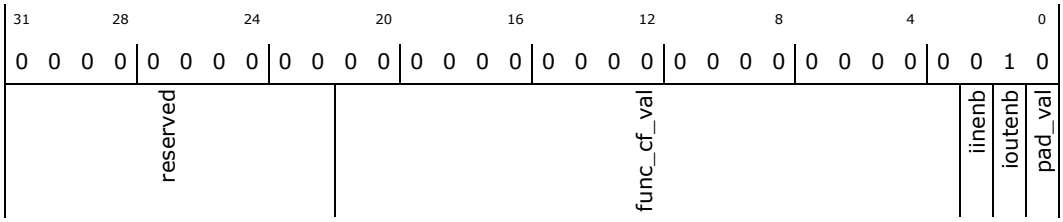
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus4_PAD_VAL: [IOBASE + 2000h] + 208h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.100 Gpio Sus1 Pad Configuration (cfio_regs_pad_gpio_sus1_PCONF0)—Offset 210h

PADs Memory space configuration register (Access via PCU Proxy)

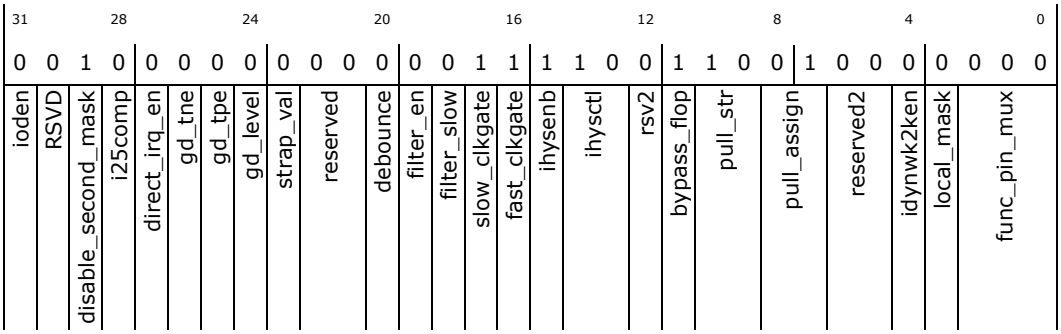
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus1_PCONF0: [IOBASE + 2000h] + 210h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIO_SUS1 function 1 is SEC_TCK For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10 function 2 is USH_CLK0 function 3 is SSA_MISR_CMD_OUT function 4 is DUN0_MISR_CMD_OUT_A function 5 is DUN1_MISR_CMD_OUT_A function 6 is PCI_WAKE1_B function 7 is DFX_VISA_VALID

3.69.101 Gpio Sus1 Delay Line Multiplexer (cfio_regs_pad_gpio_sus1_PCONF1)—Offset 214h

DLL Multiplexer

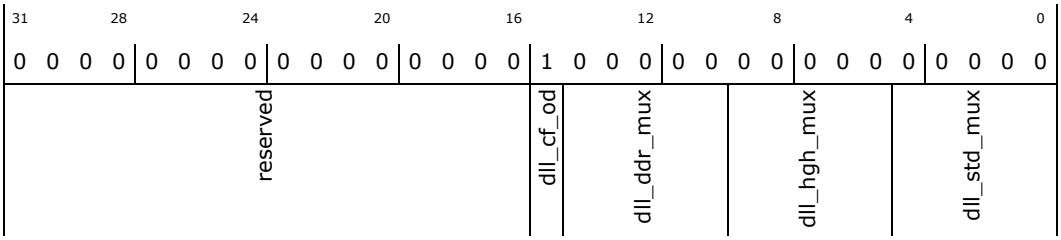
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus1_PCONF1: [IOBASE + 2000h] + 214h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.102 Gpio Sus1 Pad Value (cfio_regs_pad_gpio_sus1_PAD_VAL)—Offset 218h

PADs Memory space Value register (Access via PCU Proxy)

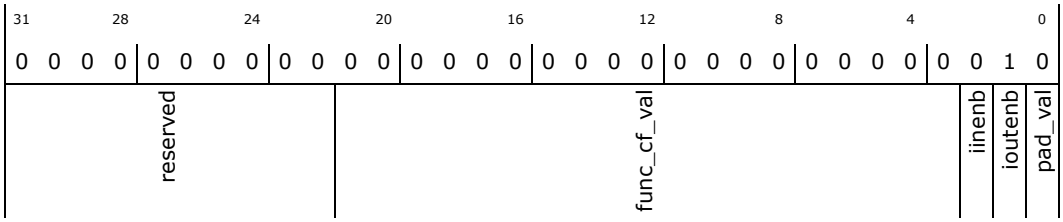
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus1_PAD_VAL: [IOBASE + 2000h] + 218h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.103 Gpio Sus5 Pad Configuration (cfio_regs_pad_gpio_sus5_PCONF0)—Offset 220h

PADs Memory space configuration register (Access via PCU Proxy)

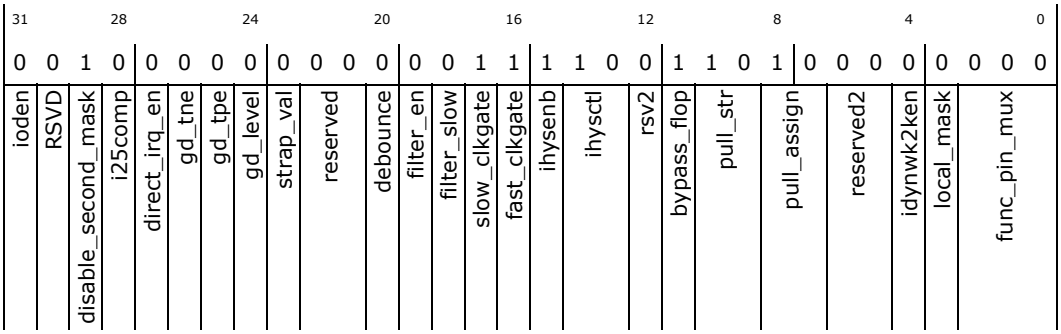
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus5_PCONF0: [IOBASE + 2000h] + 220h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIO_SUS5 function 1 is PMU_SUSCLK1 function 2 is USH_HPB[16] function 3 is SSA_MISR_RPL_OUT function 4 is Unused function 5 is Unused function 6 is Unused function 7 is DFX_VISA_OBS3

3.69.104 Gpio Sus5 Delay Line Multiplexer (cfio_regs_pad_gpio_sus5_PCONF1)—Offset 224h

DLL Multiplexer

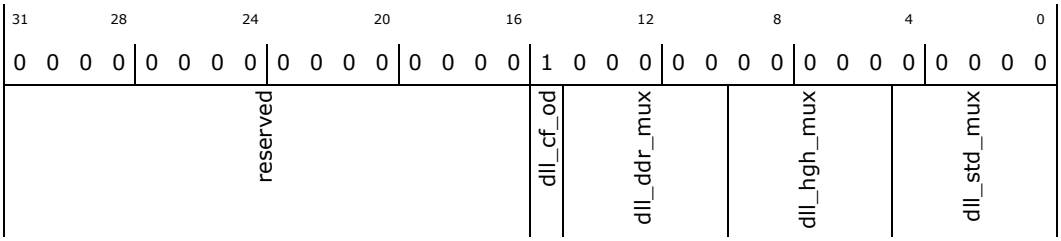
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus5_PCONF1: [IOBASE + 2000h] + 224h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.105 Gpio Sus5 Pad Value (cfio_regs_pad_gpio_sus5_PAD_VAL)—Offset 228h

PADs Memory space Value register (Access via PCU Proxy)

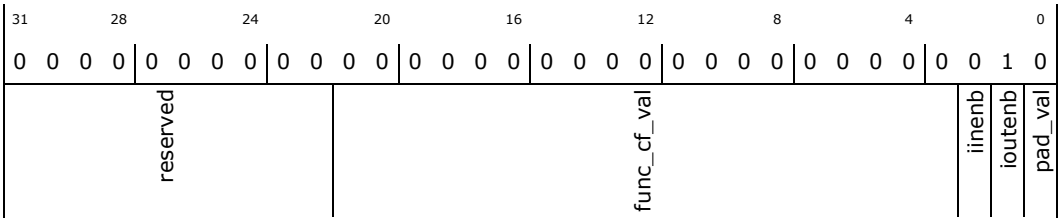
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus5_PAD_VAL: [IOBASE + 2000h] + 228h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.106 Gpio Sus7 Pad Configuration (cfio_regs_pad_gpio_sus7_PCONF0)—Offset 230h

PADs Memory space configuration register (Access via PCU Proxy)

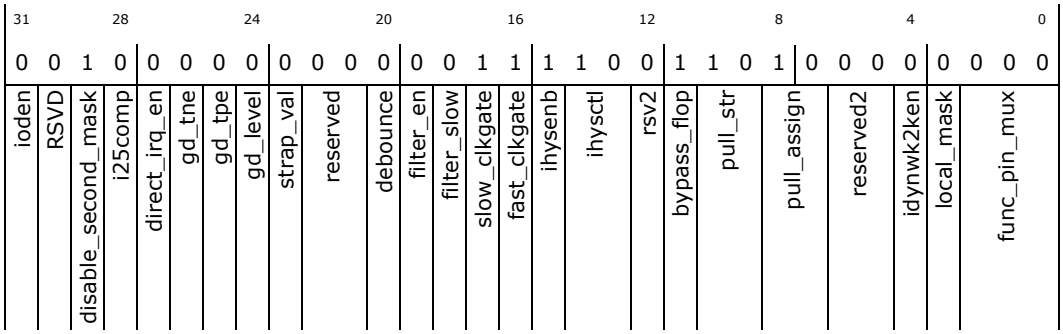
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus7_PCONF0: [IOBASE + 2000h] + 230h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIO_SUS7 function 1 is PMU_SUSCLK3 function 2 is USH_HBP[20] function 3 is SSA_MISR_C2CDAT function 4 is Unused function 5 is Unused function 6 is Unused function 7 is DFX_VISA_OBS5

3.69.107 Gpio Sus7 Delay Line Multiplexer (cfio_regs_pad_gpio_sus7_PCONF1)—Offset 234h

DLL Multiplexer

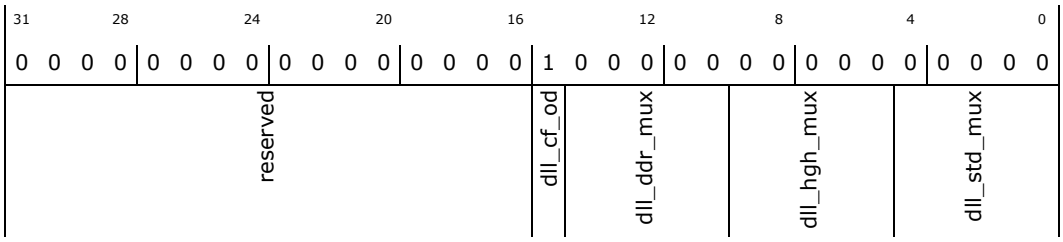
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus7_PCONF1: [IOBASE + 2000h] + 234h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.108 Gpio Sus7 Pad Value (cfio_regs_pad_gpio_sus7_PAD_VAL)—Offset 238h

PADs Memory space Value register (Access via PCU Proxy)

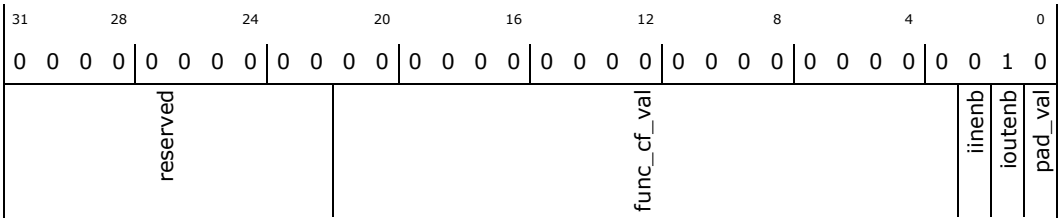
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus7_PAD_VAL: [IOBASE + 2000h] + 238h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.109 Gpio Sus6 Pad Configuration (cfio_regs_pad_gpio_sus6_PCONF0)—Offset 240h

PADs Memory space configuration register (Access via PCU Proxy)

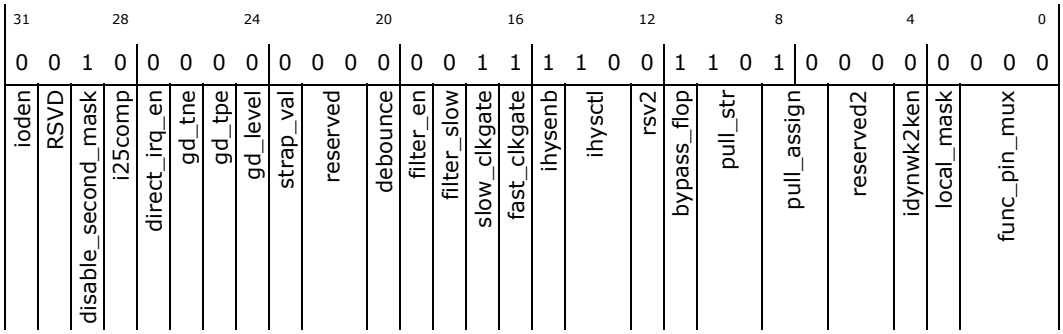
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus6_PCONF0: [IOBASE + 2000h] + 240h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIO_SUS6 function 1 is PMU_SUSCLK2 function 2 is USH_HBP[15] function 3 is SSA_MISR_C2CREQ function 4 is Unused function 5 is Unused function 6 is Unused function 7 is DFX_VISA_OBS4

3.69.110 Gpio Sus6 Delay Line Multiplexer (cfio_regs_pad_gpio_sus6_PCONF1)—Offset 244h

DLL Multiplexer

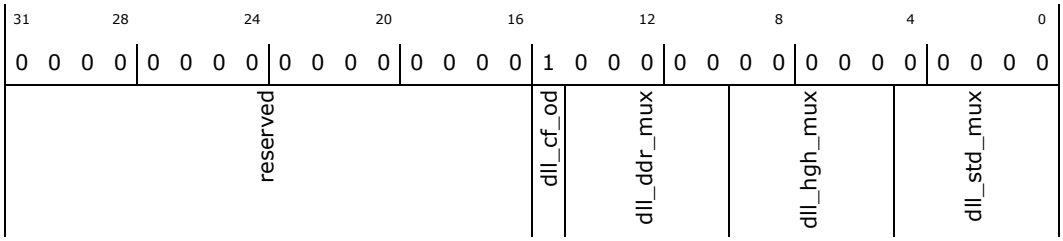
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus6_PCONF1: [IOBASE + 2000h] + 244h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.111 Gpio Sus6 Pad Value (cfio_regs_pad_gpio_sus6_PAD_VAL)—Offset 248h

PADs Memory space Value register (Access via PCU Proxy)

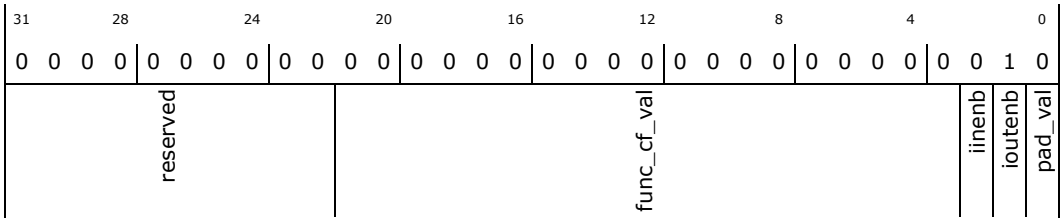
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_sus6_PAD_VAL: [IOBASE + 2000h] + 248h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.112 Sec Gpio Sus9 Pad Configuration (cfio_regs_pad_sec_gpio_sus9_PCONF0)—Offset 250h

PADs Memory space configuration register (Access via PCU Proxy)

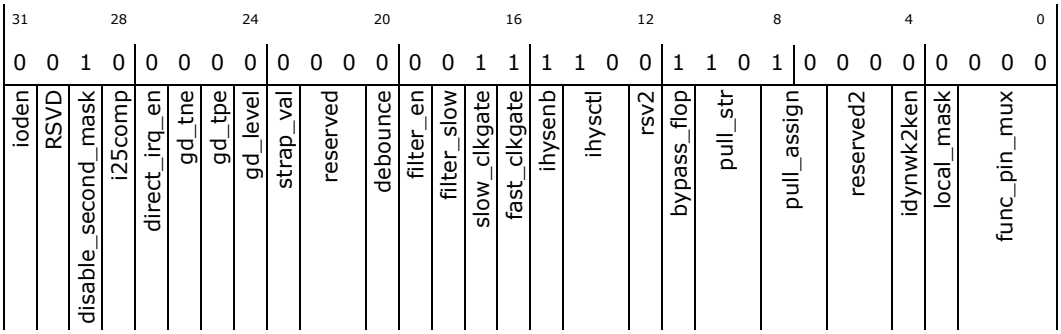
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sec_gpio_sus9_PCONF0: [IOBASE + 2000h] + 250h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is SEC_GPIO_SUS9 function 1 is Unused function 2 is USH_HBP[13] function 3 is MCSI_LPDEBUG[1] function 4 is DUN0_MISR_DATA_OUT_B function 5 is DUN1_MISR_DATA_OUT_B function 6 is Unused function 7 is DFX_VISA_OBS7

3.69.113 Sec Gpio Sus9 Delay Line Multiplexer (cfio_regs_pad_sec_gpio_sus9_PCONF1)—Offset 254h

DLL Multiplexer

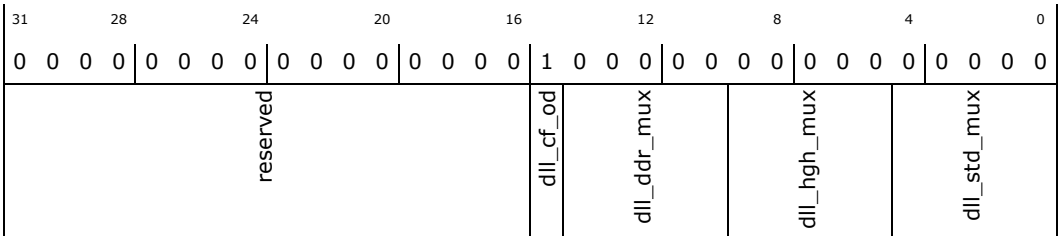
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sec_gpio_sus9_PCONF1: [IOBASE + 2000h] + 254h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.114 Sec Gpio Sus9 Pad Value (cfio_regs_pad_sec_gpio_sus9_PAD_VAL)—Offset 258h

PADs Memory space Value register (Access via PCU Proxy)

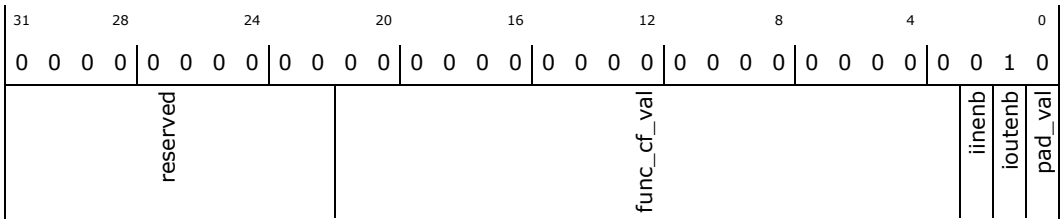
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sec_gpio_sus9_PAD_VAL: [IOBASE + 2000h] + 258h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.115 Sec Gpio Sus8 Pad Configuration (cfio_regs_pad_sec_gpio_sus8_PCONF0)—Offset 260h

PADs Memory space configuration register (Access via PCU Proxy)

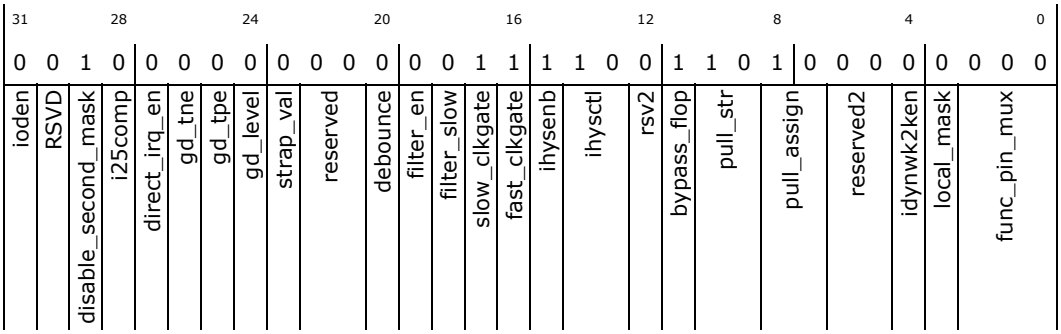
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sec_gpio_sus8_PCONF0: [IOBASE + 2000h] + 260h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is SEC_GPIO_SUS8 function 1 is Unused function 2 is USH_HBP[14] function 3 is MCSI_LPDEBUG[2] function 4 is DUN0_MISR_DATA_OUT_A function 5 is DUN1_MISR_DATA_OUT_A function 6 is Unused function 7 is DFX_VISA_OBS6

3.69.116 Sec Gpio Sus8 Delay Line Multiplexer (cfio_regs_pad_sec_gpio_sus8_PCONF1)—Offset 264h

DLL Multiplexer

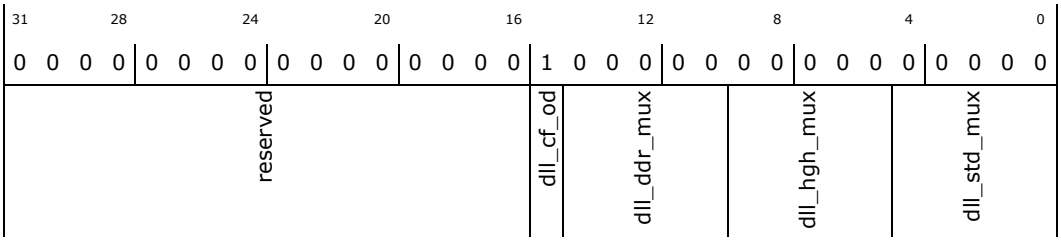
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sec_gpio_sus8_PCONF1: [IOBASE + 2000h] + 264h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.117 Sec Gpio Sus8 Pad Value (cfio_regs_pad_sec_gpio_sus8_PAD_VAL)—Offset 268h

PADs Memory space Value register (Access via PCU Proxy)

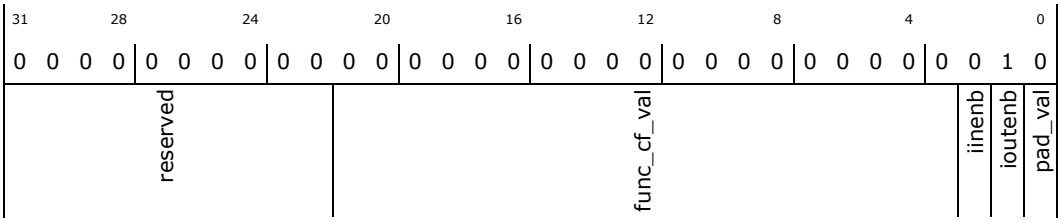
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_sec_gpio_sus8_PAD_VAL: [IOBASE + 2000h] + 268h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.118 Gpio Dfx1 Pad Configuration (cfio_regs_pad_gpio_dfx1_PCONF0)—Offset 270h

PADs Memory space configuration register (Access via PCU Proxy)

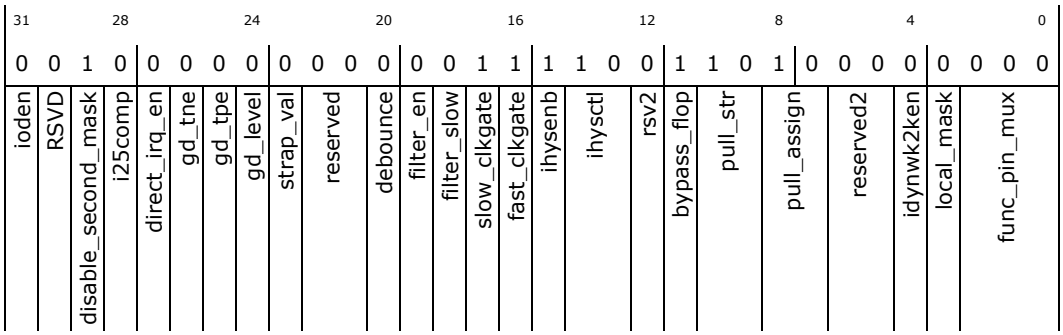
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx1_PCONF0: [IOBASE + 2000h] + 270h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_23 function 1 is SUS_OBS_0 function 2 is USH_CRC_DEBUG function 3 is CCLKPH1[0] function 4 is GCLKPH function 5 is Cx_BPM0_TX

3.69.119 Gpio Dfx1 Delay Line Multiplexer (cfio_regs_pad_gpio_dfx1_PCONF1)—Offset 274h

DLL Multiplexer

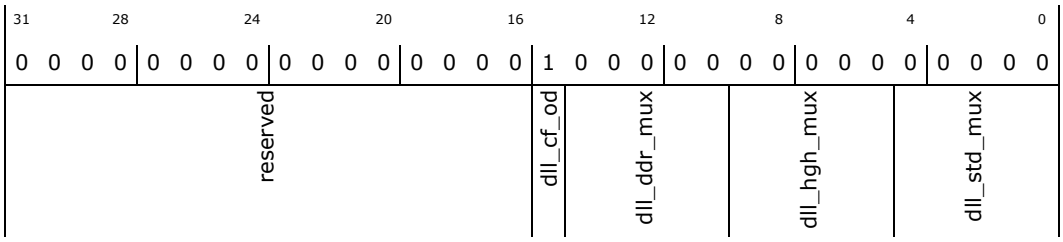
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx1_PCONF1: [IOBASE + 2000h] + 274h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.120 Gpio Dfx1 Pad Value (cfio_regs_pad_gpio_dfx1_PAD_VAL)—Offset 278h

PADs Memory space Value register (Access via PCU Proxy)

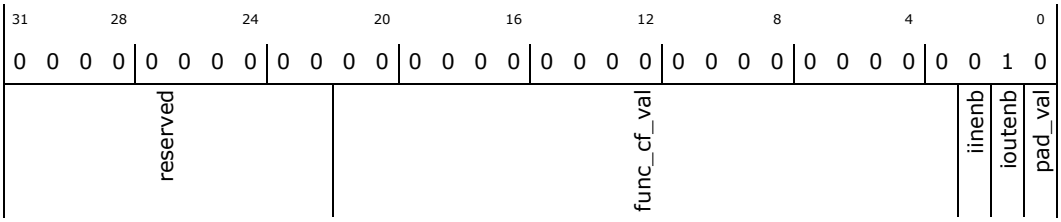
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_gpio_dfx1_PAD_VAL: [IOBASE + 2000h] + 278h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.121 Usb Ulpi 0 Refclk Pad Configuration (cfio_regs_pad_usb_ulpi_0_refclk_PCONF0)—Offset 280h

PADs Memory space configuration register (Access via PCU Proxy)

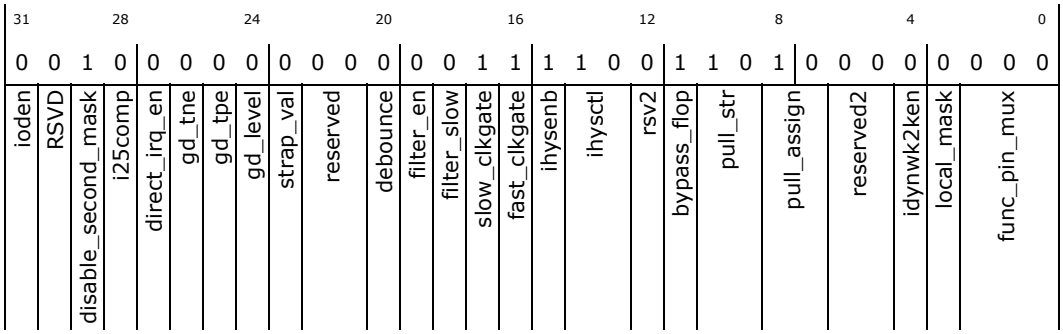
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_refclk_PCONF0: [IOBASE + 2000h] + 280h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_43 function 1 is USB_ULPI_0_REFCLK function 2 is USH_HBP[11] function 3 is MCSI_LPDEBUG[3]

3.69.122 Usb Ulpi 0 Refclk Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_refclk_PCONF1)—Offset 284h

DLL Multiplexer

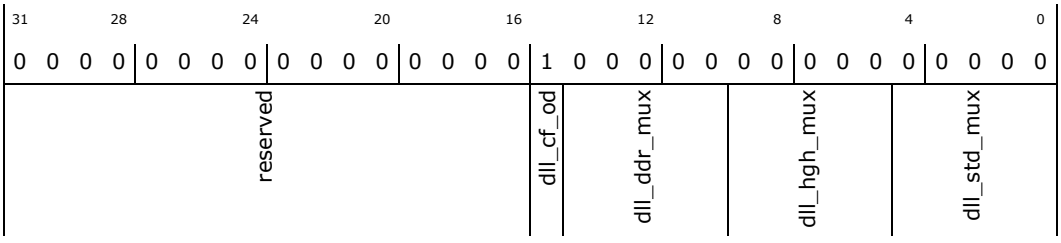
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_refclk_PCONF1: [IOBASE + 2000h] + 284h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.123 Usb Ulpi 0 Refclk Pad Value (cfio_regs_pad_usb_ulpi_0_refclk_PAD_VAL)—Offset 288h

PADs Memory space Value register (Access via PCU Proxy)

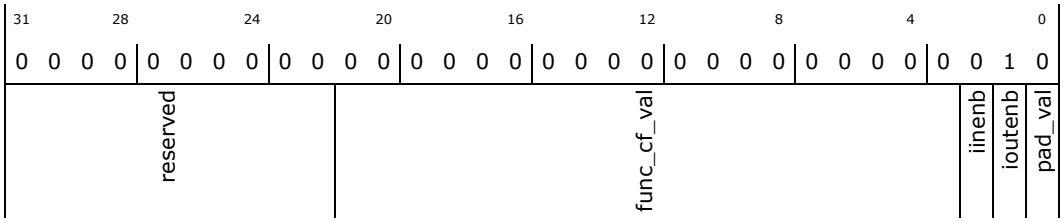
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_refclk_PAD_VAL: [IOBASE + 2000h] + 288h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low

Bit Range	Default & Access	Description
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.124 Tck Pad Configuration (cfio_regs_pad_tck_PCONF0)—Offset 290h

PADs Memory space configuration register (Access via PCU Proxy)

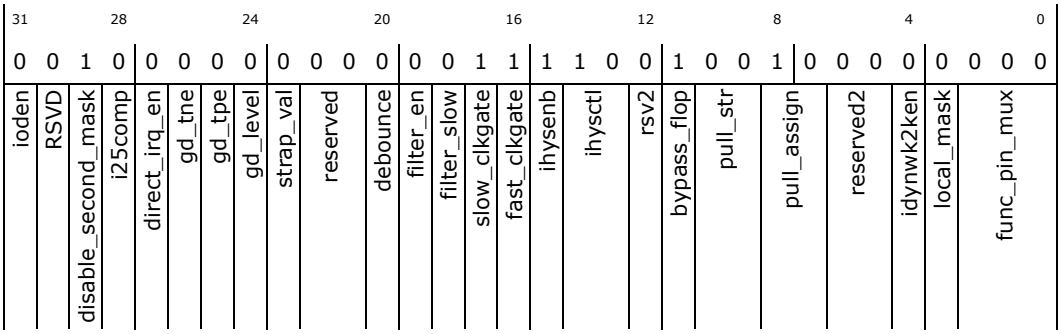
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tck_PCONF0: [IOBASE + 2000h] + 290h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C900h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Description
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is TCK

3.69.125 Tck Delay Line Multiplexer (cfio_regs_pad_tck_PCONF1)—Offset 294h

DLL Multiplexer

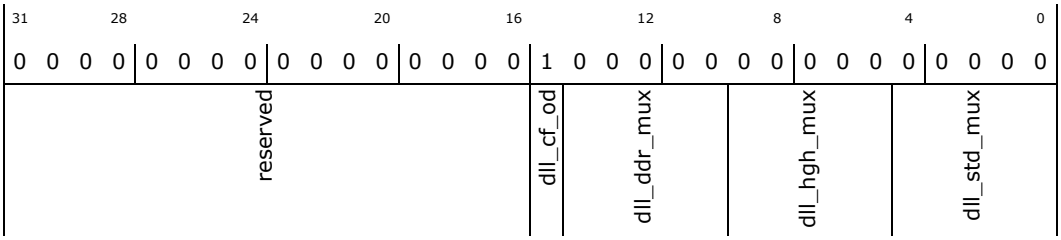
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tck_PCONF1: [IOBASE + 2000h] + 294h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.126 Tck Pad Value (cfio_regs_pad_tck_PAD_VAL)—Offset 298h

PADs Memory space Value register (Access via PCU Proxy)

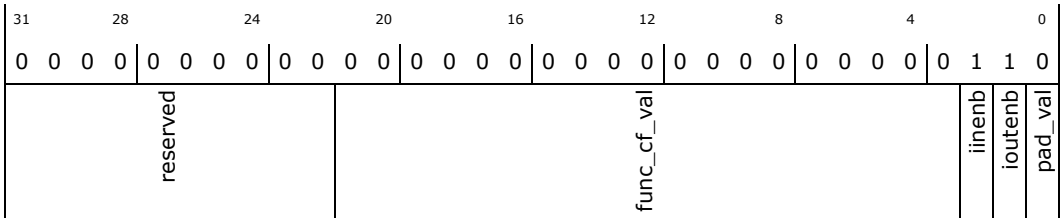
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tck_PAD_VAL: [IOBASE + 2000h] + 298h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.127 Trst B Pad Configuration (cfio_regs_pad_trst_b_PCONF0)—Offset 2A0h

PADs Memory space configuration register (Access via PCU Proxy)

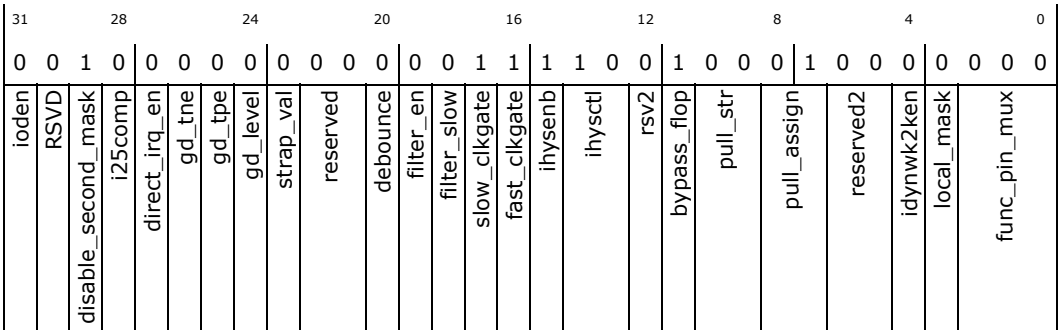
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_trst_b_PCONF0: [IOBASE + 2000h] + 2A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C880h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is TRST_B

3.69.128 Trst B Delay Line Multiplexer (cfio_regs_pad_trst_b_PCONF1)—Offset 2A4h

DLL Multiplexer

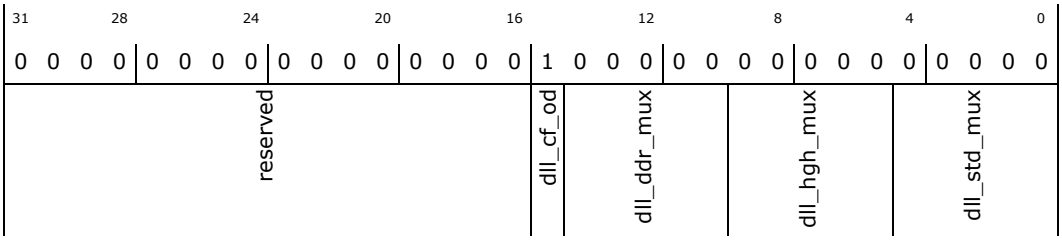
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_trst_b_PCONF1: [IOBASE + 2000h] + 2A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.129 Trst B Pad Value (cfio_regs_pad_trst_b_PAD_VAL)—Offset 2A8h

PADs Memory space Value register (Access via PCU Proxy)

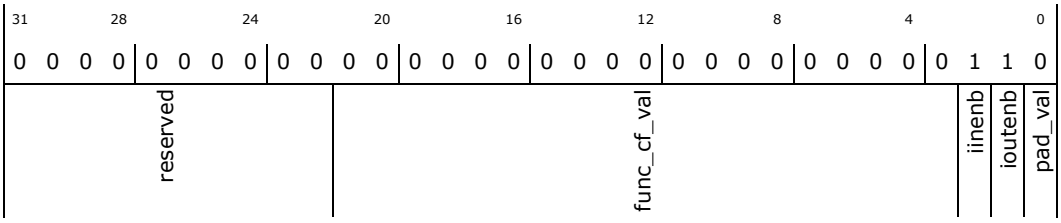
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_trst_b_PAD_VAL: [IOBASE + 2000h] + 2A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.130 Tdi Pad Configuration (cfio_regs_pad_tdi_PCONF0)—Offset 2B0h

PADs Memory space configuration register (Access via PCU Proxy)

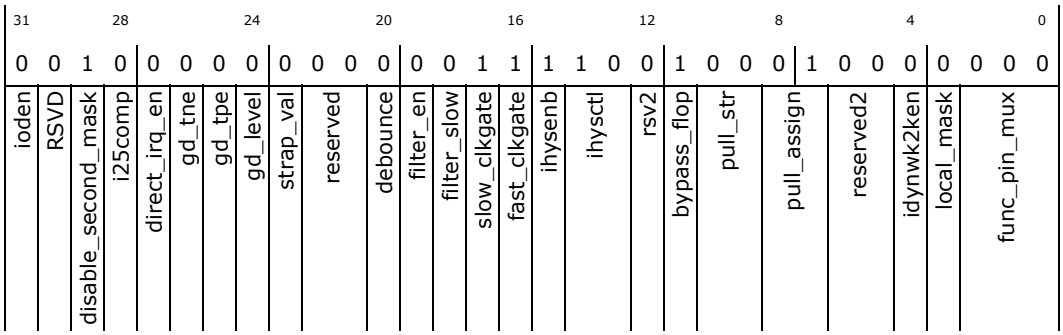
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tdi_PCONF0: [IOBASE + 2000h] + 2B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C880h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is TDI

3.69.131 Tdi Delay Line Multiplexer (cfio_regs_pad_tdi_PCONF1)—Offset 2B4h

DLL Multiplexer

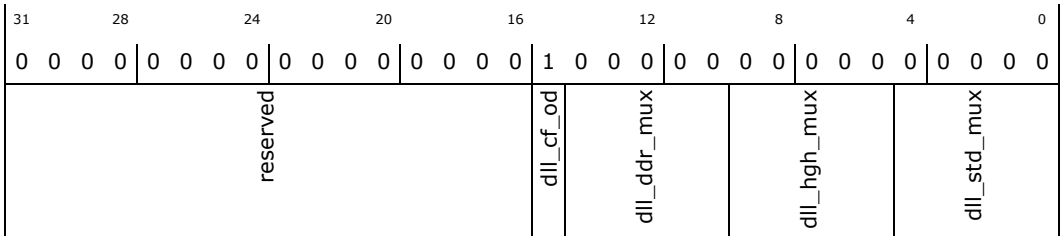
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tdi_PCONF1: [IOBASE + 2000h] + 2B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.132 Tdi Pad Value (cfio_regs_pad_tdi_PAD_VAL)—Offset 2B8h

PADs Memory space Value register (Access via PCU Proxy)

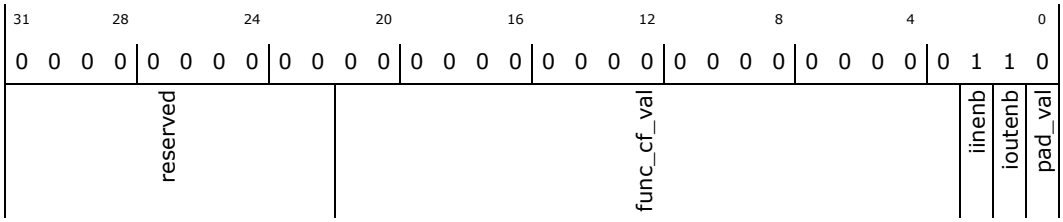
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tdi_PAD_VAL: [IOBASE + 2000h] + 2B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.133 Tms Pad Configuration (cfio_regs_pad_tms_PCONF0)—Offset 2C0h

PADs Memory space configuration register (Access via PCU Proxy)

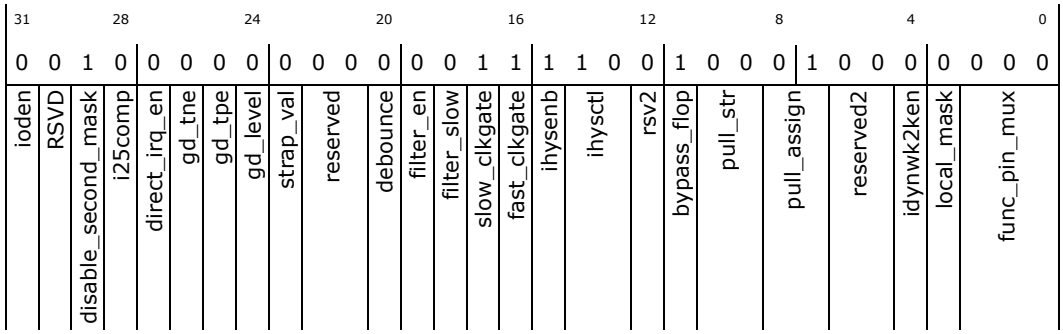
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tms_PCONF0: [IOBASE + 2000h] + 2C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C880h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is TMS

3.69.134 Tms Delay Line Multiplexer (cfio_regs_pad_tms_PCONF1)—Offset 2C4h

DLL Multiplexer

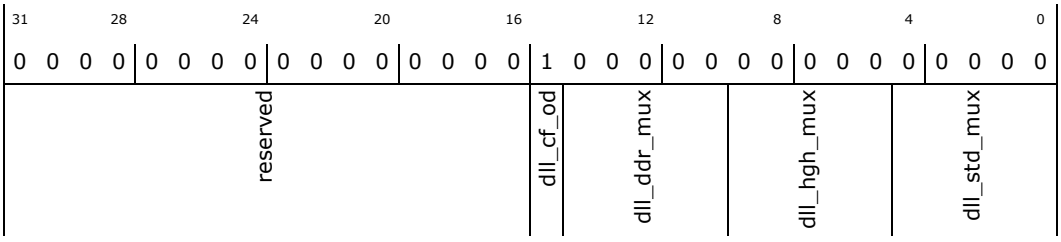
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tms_PCONF1: [IOBASE + 2000h] + 2C4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.135 Tms Pad Value (cfio_regs_pad_tms_PAD_VAL)—Offset 2C8h

PADs Memory space Value register (Access via PCU Proxy)

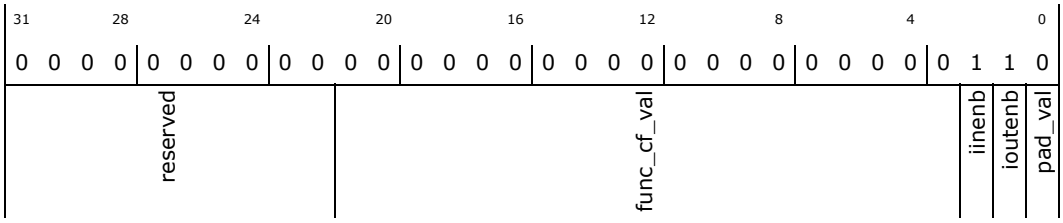
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tms_PAD_VAL: [IOBASE + 2000h] + 2C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.136 Cx Prdy B Pad Configuration (cfio_regs_pad_cx_prdy_b_PCONF0)—Offset 2D0h

PADs Memory space configuration register (Access via PCU Proxy)

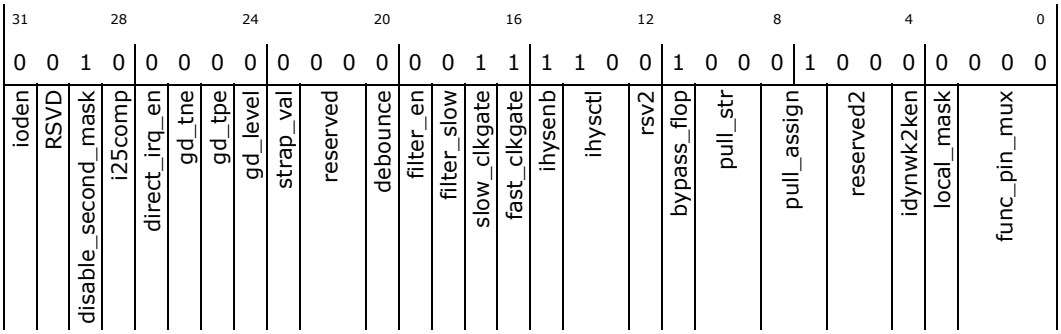
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_cx_prdy_b_PCONF0: [IOBASE + 2000h] + 2D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C880h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is CX_PRDY_B For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

3.69.137 Cx Prdy B Delay Line Multiplexer (cfio_regs_pad_cx_prdy_b_PCONF1)—Offset 2D4h

DLL Multiplexer

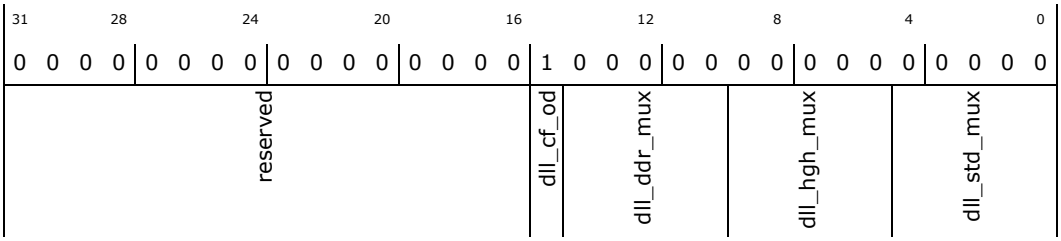
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_cx_prdy_b_PCONF1: [IOBASE + 2000h] + 2D4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.138 Cx Prdy B Pad Value (cfio_regs_pad_cx_prdy_b_PAD_VAL)—Offset 2D8h

PADs Memory space Value register (Access via PCU Proxy)

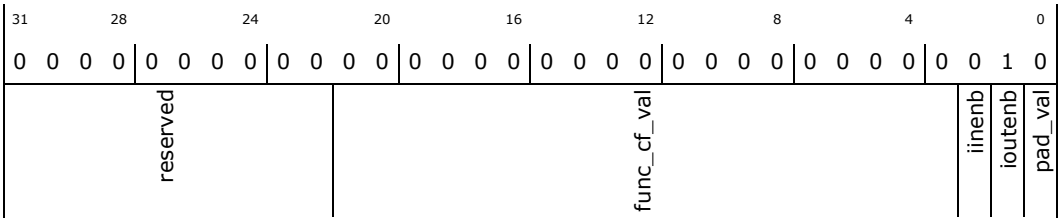
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_cx_prdy_b_PAD_VAL: [IOBASE + 2000h] + 2D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.139 Cx Preq B Pad Configuration (cfio_regs_pad_cx_preq_b_PCONF0)—Offset 2E0h

PADs Memory space configuration register (Access via PCU Proxy)

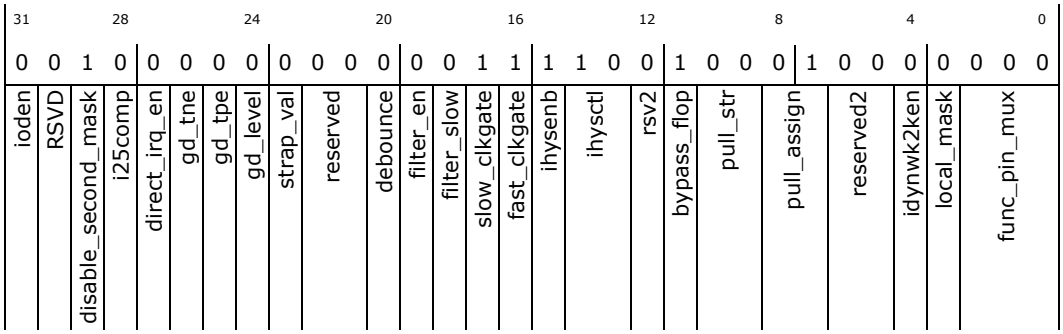
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_cx_preq_b_PCONF0: [IOBASE + 2000h] + 2E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C880h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is CX_PREQ_B

3.69.140 Cx Preq B Delay Line Multiplexer (cfio_regs_pad_cx_preq_b_PCONF1)—Offset 2E4h

DLL Multiplexer

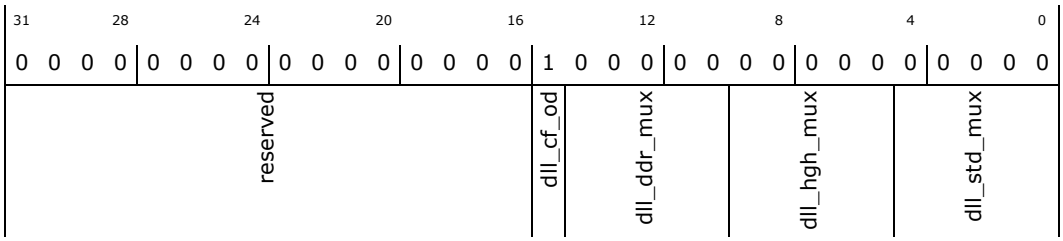
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_cx_preq_b_PCONF1: [IOBASE + 2000h] + 2E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.141 Cx Preq B Pad Value (cfio_regs_pad_cx_preq_b_PAD_VAL)—Offset 2E8h

PADs Memory space Value register (Access via PCU Proxy)

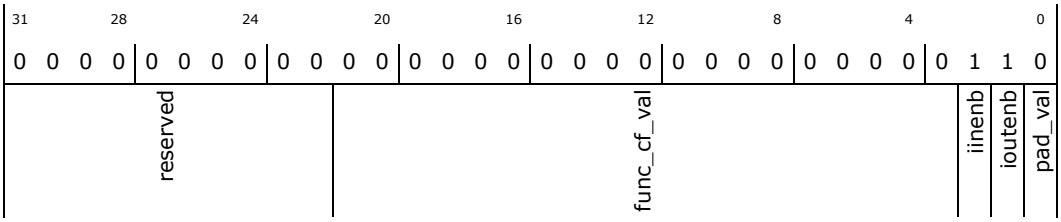
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_cx_preq_b_PAD_VAL: [IOBASE + 2000h] + 2E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	1b RO	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.142 Tdo Pad Configuration (cfio_regs_pad_tdo_PCONF0)—Offset 2F0h

PADs Memory space configuration register (Access via PCU Proxy)

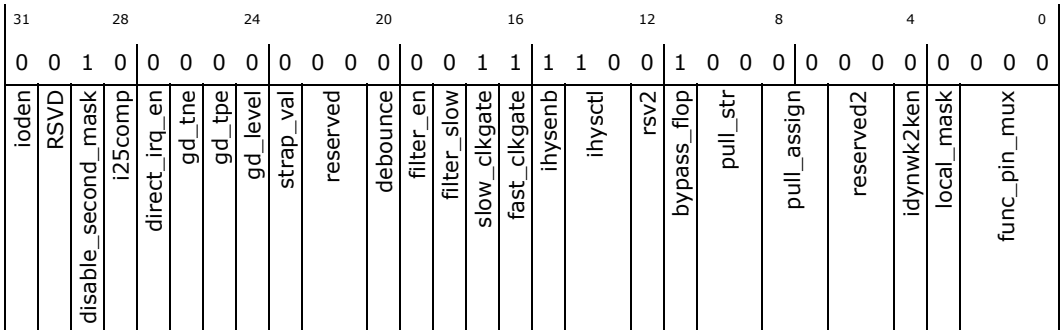
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tdo_PCONF0: [IOBASE + 2000h] + 2F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RO	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RO	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RO	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RO	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RO	**Filter En (filter_en):** Enabling the glitch filter
18	0b RO	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RO	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RO	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	00b RO	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	00b RO	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is TDO

3.69.143 Tdo Delay Line Multiplexer (cfio_regs_pad_tdo_PCONF1)—Offset 2F4h

DLL Multiplexer

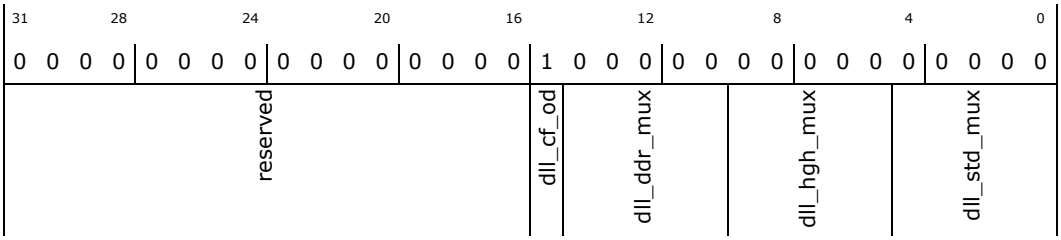
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tdo_PCONF1: [IOBASE + 2000h] + 2F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.144 Tdo Pad Value (cfio_regs_pad_tdo_PAD_VAL)—Offset 2F8h

PADs Memory space Value register (Access via PCU Proxy)

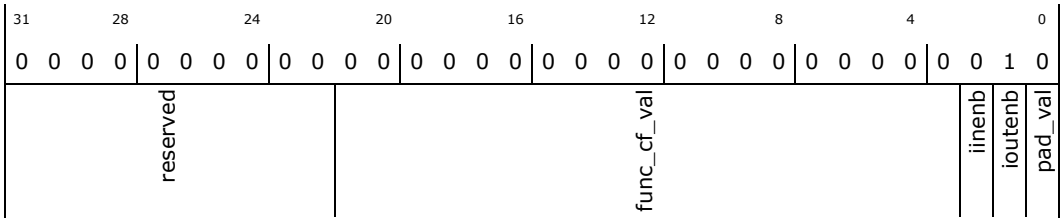
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_tdo_PAD_VAL: [IOBASE + 2000h] + 2F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RO	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.145 Usb Ulpi 0 Data4 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data4_PCONF0)—Offset 300h

PADs Memory space configuration register (Access via PCU Proxy)

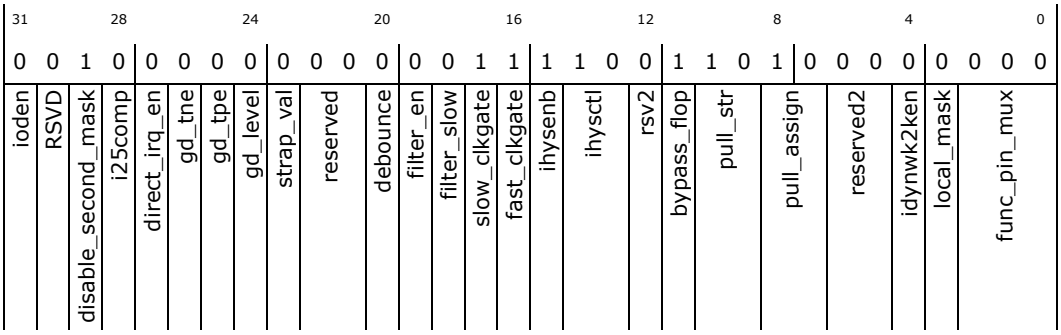
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data4_PCONF0: [IOBASE + 2000h] + 300h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq

Bit Range	Default & Access	Description
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_36 function 1 is USB_ULPI_0_DATA4 function 2 is USH_HBP[6] function 3 is MCSI_LPDEBUG[10]

3.69.146 Usb Ulpi 0 Data4 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data4_PCONF1)—Offset 304h

DLL Multiplexer

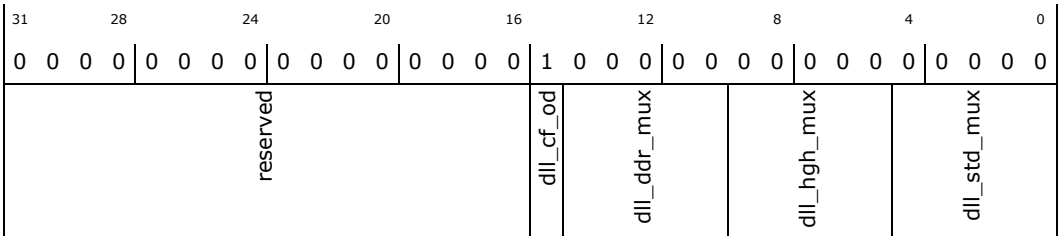
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data4_PCONF1: [IOBASE + 2000h] + 304h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.147 Usb Ulpi 0 Data4 Pad Value (cfio_regs_pad_usb_ulpi_0_data4_PAD_VAL)—Offset 308h

PADs Memory space Value register (Access via PCU Proxy)

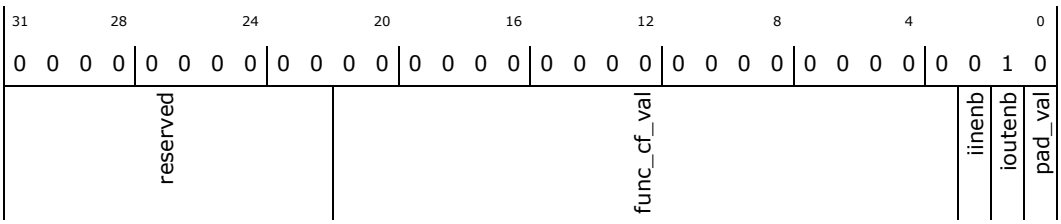
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data4_PAD_VAL: [IOBASE + 2000h] + 308h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.148 Usb Ulpi 0 Data2 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data2_PCONF0)—Offset 310h

PADs Memory space configuration register (Access via PCU Proxy)

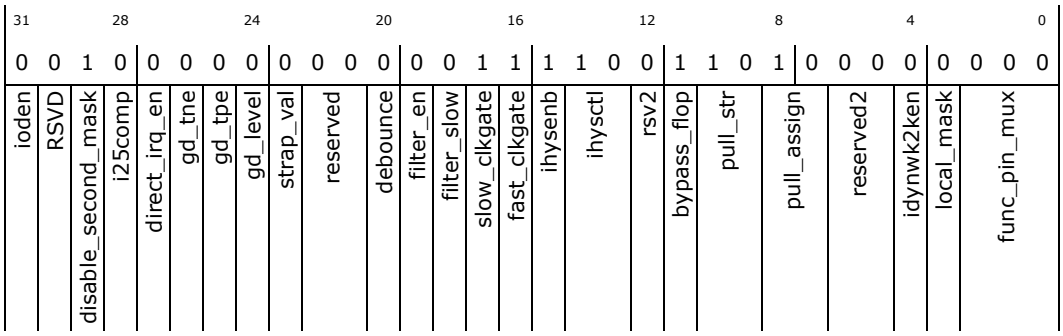
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data2_PCONF0: [IOBASE + 2000h] + 310h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Description
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_34 function 1 is USB_ULPI_0_DATA2 function 2 is USH_HBP[8] function 3 is MCSI_LPDEBUG[12]

3.69.149 Usb Ulpi 0 Data2 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data2_PCONF1)—Offset 314h

DLL Multiplexer

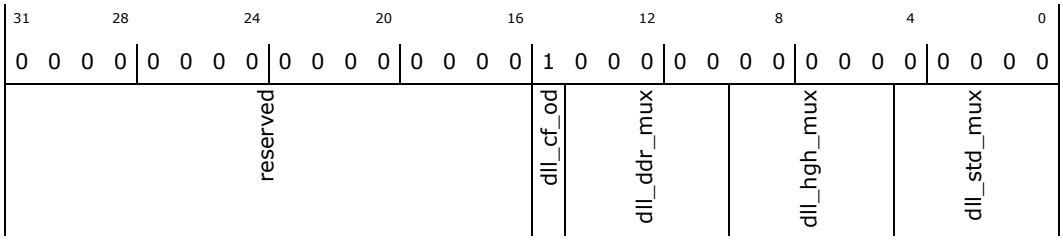
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data2_PCONF1: [IOBASE + 2000h] + 314h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.150 Usb Ulpi 0 Data2 Pad Value (cfio_regs_pad_usb_ulpi_0_data2_PAD_VAL)—Offset 318h

PADs Memory space Value register (Access via PCU Proxy)

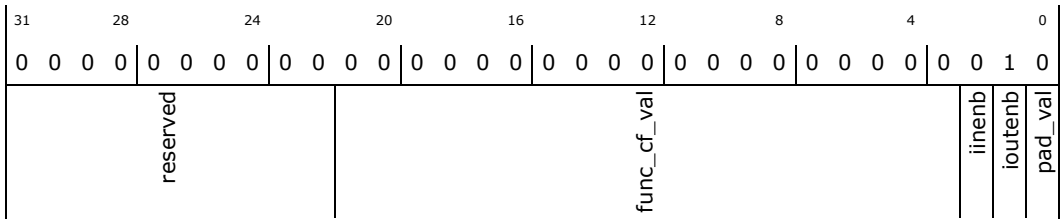
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data2_PAD_VAL: [IOBASE + 2000h] + 318h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.151 Usb Ulpi 0 Data6 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data6_PCONF0)—Offset 320h

PADs Memory space configuration register (Access via PCU Proxy)

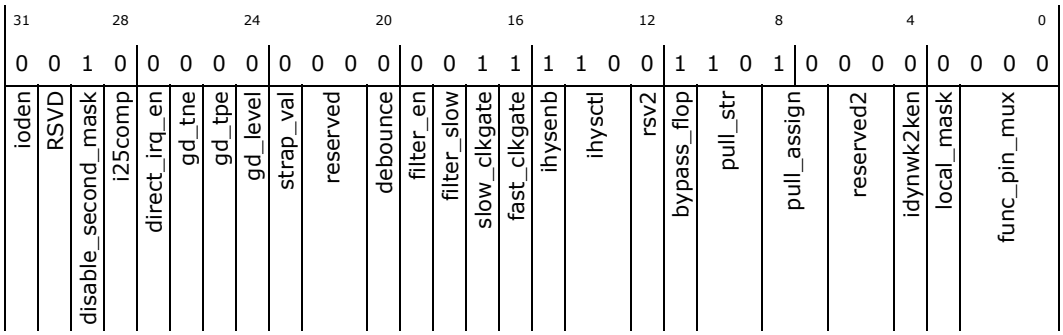
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data6_PCONF0: [IOBASE + 2000h] + 320h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad

Bit Range	Default & Access	Description
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_38 function 1 is USB_ULPI_0_DATA6 function 2 is USH_HBP[4] function 3 is MCSI_LPDEBUG[8]

3.69.152 Usb Ulpi 0 Data6 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data6_PCONF1)—Offset 324h

DLL Multiplexer

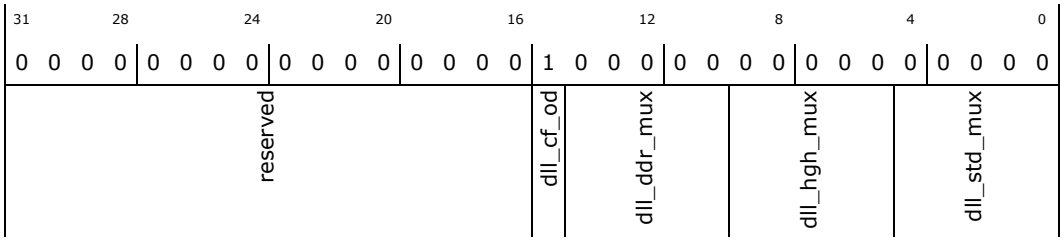
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data6_PCONF1: [IOBASE + 2000h] + 324h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.153 Usb Ulpi 0 Data6 Pad Value (cfio_regs_pad_usb_ulpi_0_data6_PAD_VAL)—Offset 328h

PADs Memory space Value register (Access via PCU Proxy)

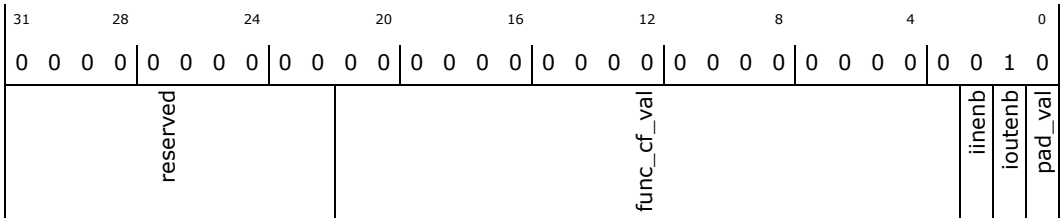
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data6_PAD_VAL: [IOBASE + 2000h] + 328h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.154 Usb Ulpi 0 Clk Pad Configuration (cfio_regs_pad_usb_ulpi_0_clk_PCONF0)—Offset 330h

PADs Memory space configuration register (Access via PCU Proxy)

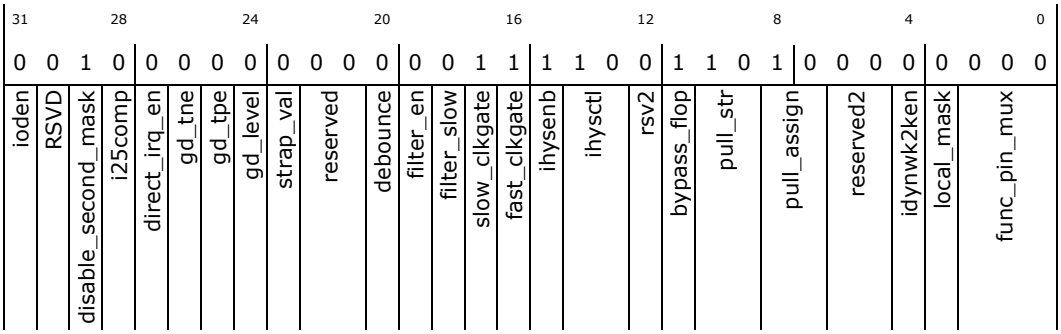
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_clk_PCONF0: [IOBASE + 2000h] + 330h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_31 function 1 is USB_ULPI_0_CLK function 2 is USH_HBP_CLK1 function 3 is MCSI_LPDEBUG[15]

3.69.155 Usb Ulpi 0 Clk Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_clk_PCONF1)—Offset 334h

DLL Multiplexer

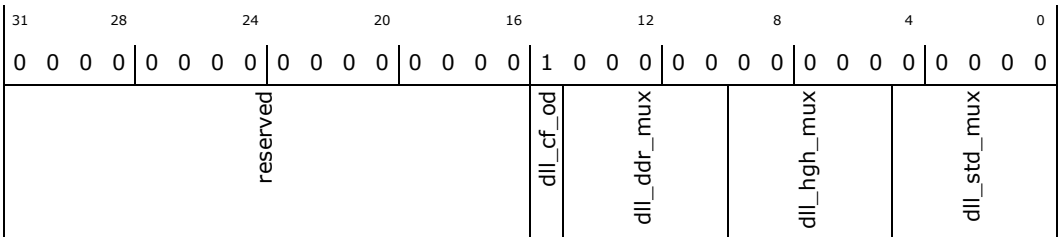
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_clk_PCONF1: [IOBASE + 2000h] + 334h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.156 Usb Ulpi 0 Clk Pad Value (cfio_regs_pad_usb_ulpi_0_clk_PAD_VAL)—Offset 338h

PADs Memory space Value register (Access via PCU Proxy)

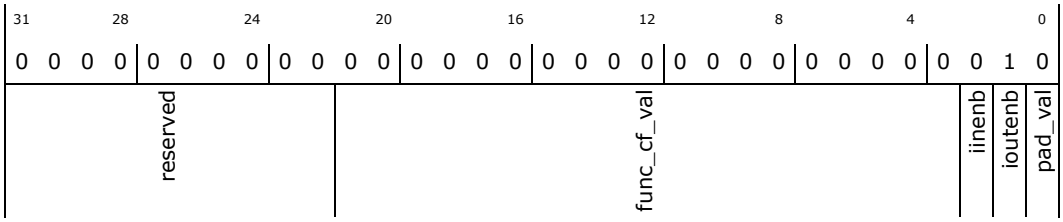
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_clk_PAD_VAL: [IOBASE + 2000h] + 338h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.157 Usb Ulpi 0 Dir Pad Configuration (cfio_regs_pad_usb_ulpi_0_dir_PCONF0)—Offset 340h

PADs Memory space configuration register (Access via PCU Proxy)

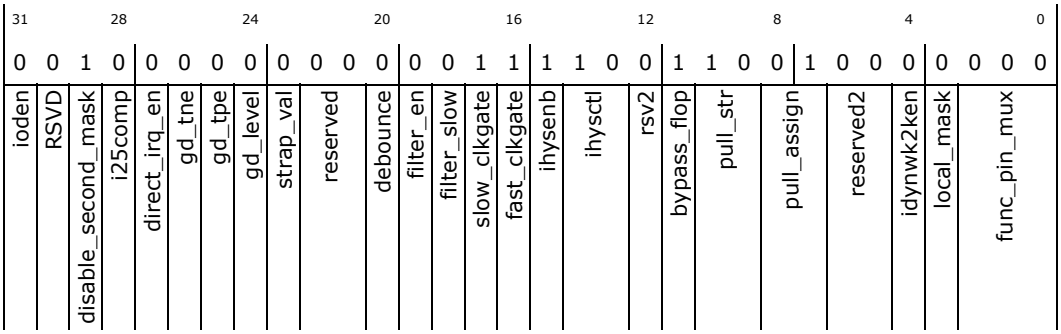
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_dir_PCONF0: [IOBASE + 2000h] + 340h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_40 function 1 is USB_ULPI_0_DIR function 2 is USH_HBP[2] function 3 is MCSI_LPDEBUG[6] For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

3.69.158 Usb Ulpi 0 Dir Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_dir_PCONF1)—Offset 344h

DLL Multiplexer

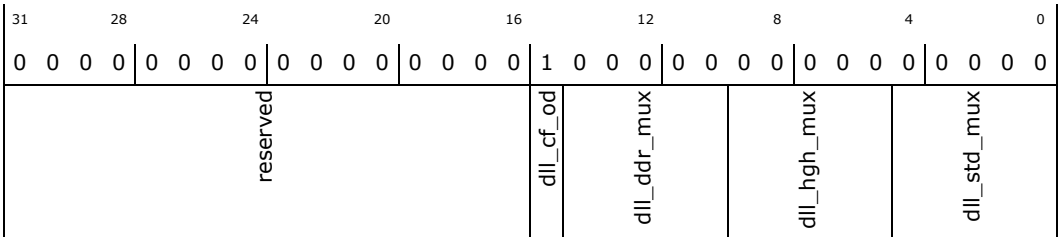
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_dir_PCONF1: [IOBASE + 2000h] + 344h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.159 Usb Ulpi 0 Dir Pad Value (cfio_regs_pad_usb_ulpi_0_dir_PAD_VAL)—Offset 348h

PADs Memory space Value register (Access via PCU Proxy)

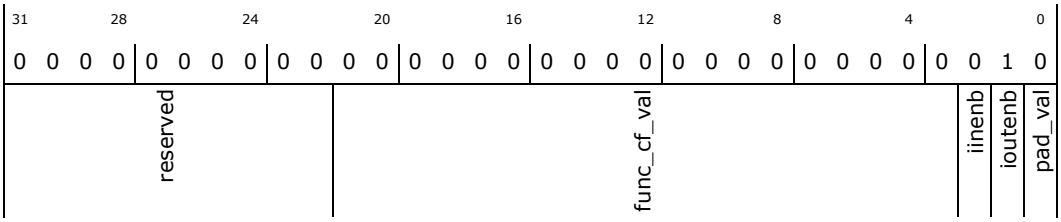
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_dir_PAD_VAL: [IOBASE + 2000h] + 348h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value

Bit Range	Default & Access	Description
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.160 Usb Ulpi 0 Nxt Pad Configuration (cfio_regs_pad_usb_ulpi_0_nxt_PCONF0)—Offset 350h

PADs Memory space configuration register (Access via PCU Proxy)

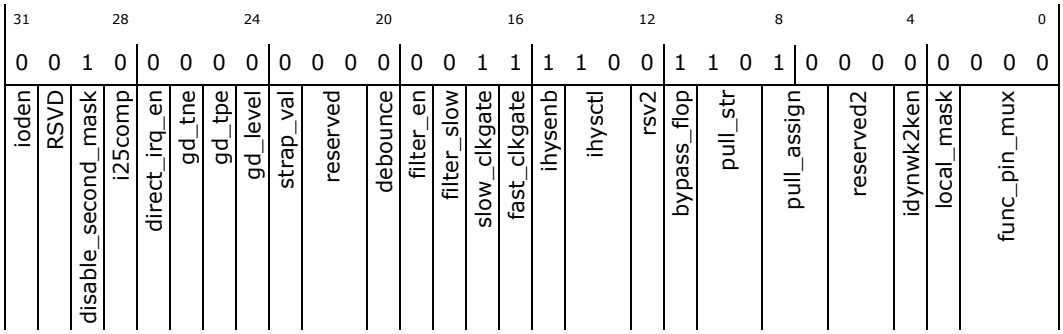
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_nxt_PCONF0: [IOBASE + 2000h] + 350h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers

Bit Range	Default & Access	Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_41 function 1 is USB_ULPI_0_NXT function 2 is USH_HBP[1] function 3 is MCSI_LPDEBUG[5]

3.69.161 Usb Ulpi 0 Nxt Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_nxt_PCONF1)—Offset 354h

DLL Multiplexer

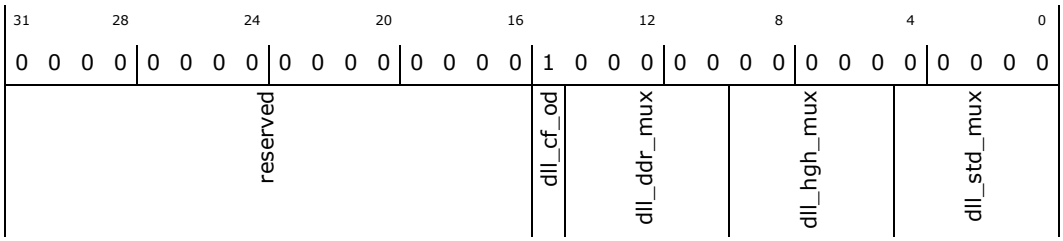
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_nxt_PCONF1: [IOBASE + 2000h] + 354h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.162 Usb Ulpi 0 Nxt Pad Value (cfio_regs_pad_usb_ulpi_0_nxt_PAD_VAL)—Offset 358h

PADs Memory space Value register (Access via PCU Proxy)

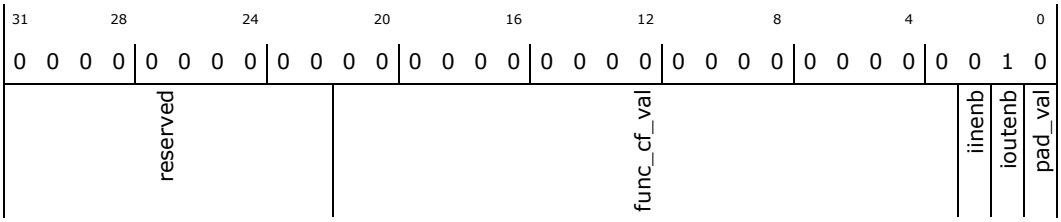
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_nxt_PAD_VAL: [IOBASE + 2000h] + 358h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.163 Usb Ulpi 0 Data1 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data1_PCONF0)—Offset 360h

PADs Memory space configuration register (Access via PCU Proxy)

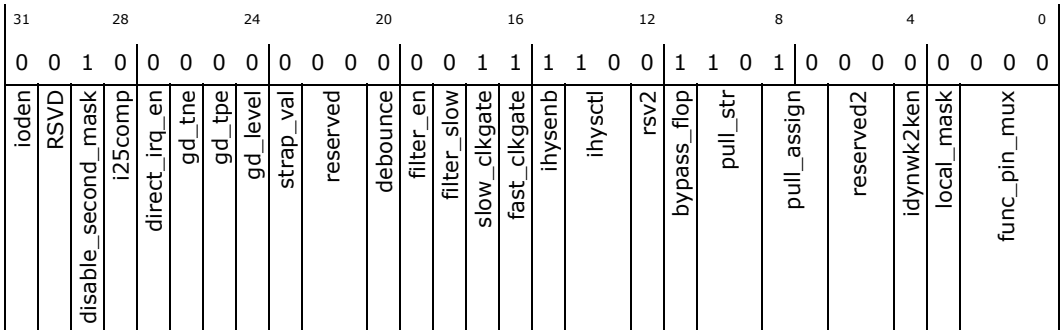
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data1_PCONF0: [IOBASE + 2000h] + 360h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_33 function 1 is USB_ULPI_0_DATA1 function 2 is USH_HBP[9] function 3 is MCSI_LPDEBUG[13]

3.69.164 Usb Ulpi 0 Data1 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data1_PCONF1)—Offset 364h

DLL Multiplexer

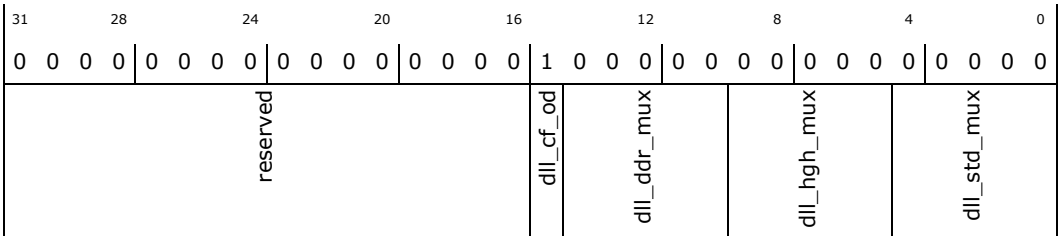
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data1_PCONF1: [IOBASE + 2000h] + 364h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.165 Usb Ulpi 0 Data1 Pad Value (cfio_regs_pad_usb_ulpi_0_data1_PAD_VAL)—Offset 368h

PADs Memory space Value register (Access via PCU Proxy)

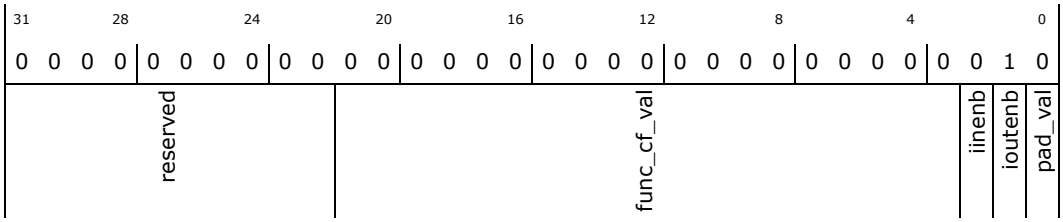
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data1_PAD_VAL: [IOBASE + 2000h] + 368h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low

Bit Range	Default & Access	Description
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.166 Usb Ulpi 0 Data3 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data3_PCONF0)—Offset 370h

PADs Memory space configuration register (Access via PCU Proxy)

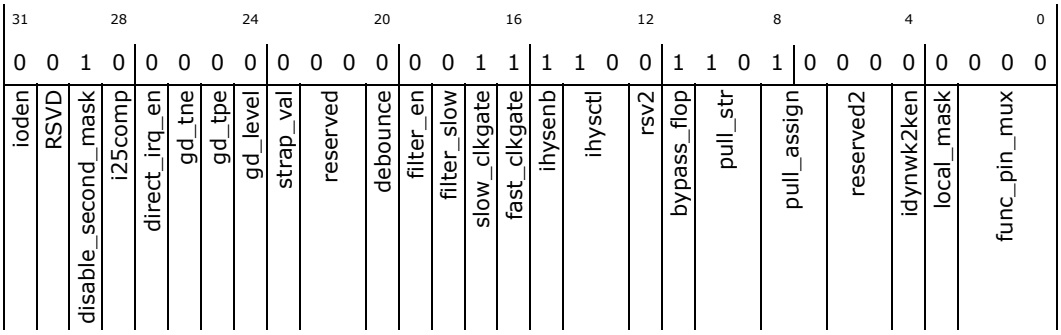
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data3_PCONF0: [IOBASE + 2000h] + 370h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_35 function 1 is USB_ULPI_0_DATA3 function 2 is USH_HPB[7] function 3 is MCSI_LPDEBUG[11]

3.69.167 Usb Ulpi 0 Data3 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data3_PCONF1)—Offset 374h

DLL Multiplexer

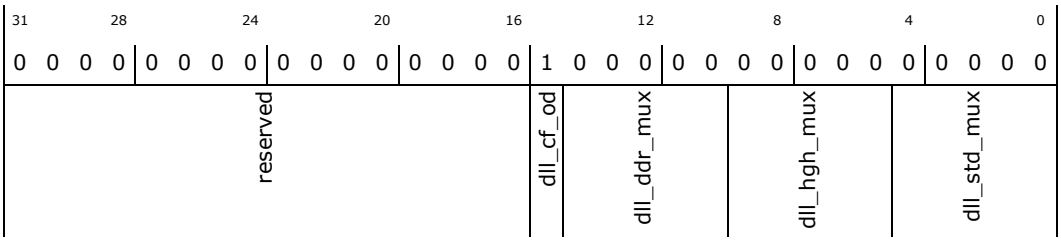
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data3_PCONF1: [IOBASE + 2000h] + 374h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.168 Usb Ulpi 0 Data3 Pad Value (cfio_regs_pad_usb_ulpi_0_data3_PAD_VAL)—Offset 378h

PADs Memory space Value register (Access via PCU Proxy)

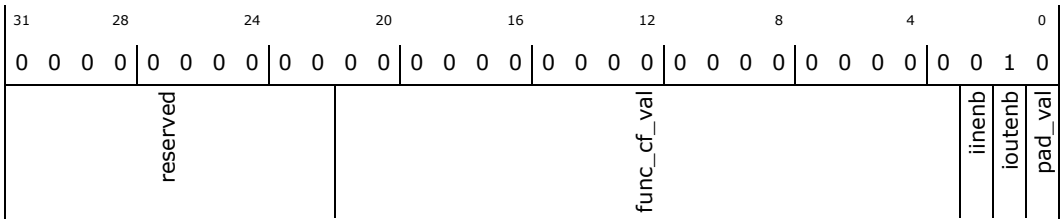
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data3_PAD_VAL: [IOBASE + 2000h] + 378h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.169 Usb Ulpi 0 Data0 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data0_PCONF0)—Offset 380h

PADs Memory space configuration register (Access via PCU Proxy)

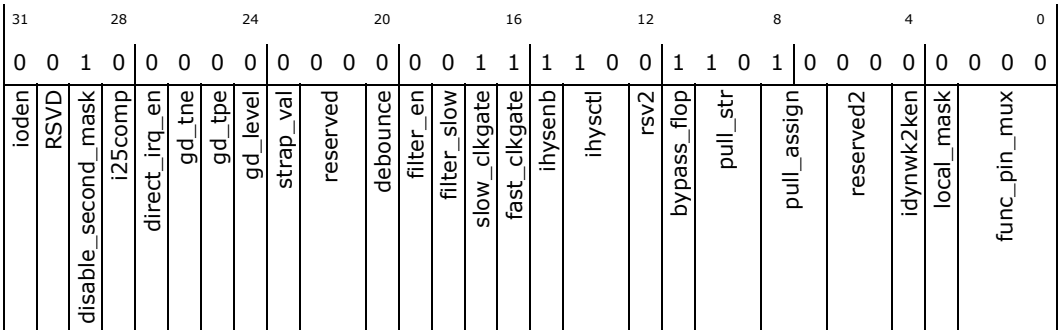
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data0_PCONF0: [IOBASE + 2000h] + 380h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_32 function 1 is USB_ULPI_0_DATA0 function 2 is USH_HBP[10] function 3 is MCSI_LPDEBUG[14]

3.69.170 Usb Ulpi 0 Data0 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data0_PCONF1)—Offset 384h

DLL Multiplexer

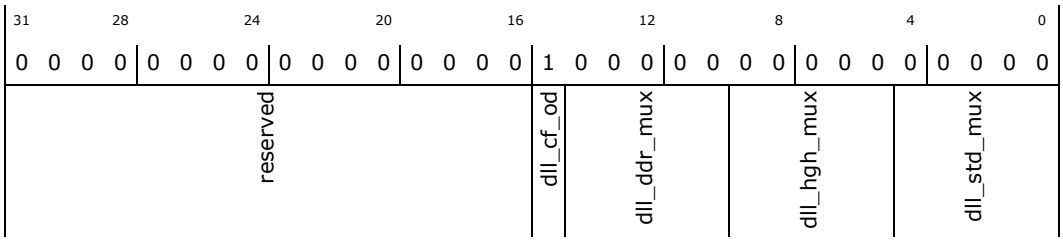
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data0_PCONF1: [IOBASE + 2000h] + 384h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.171 Usb Ulpi 0 Data0 Pad Value (cfio_regs_pad_usb_ulpi_0_data0_PAD_VAL)—Offset 388h

PADs Memory space Value register (Access via PCU Proxy)

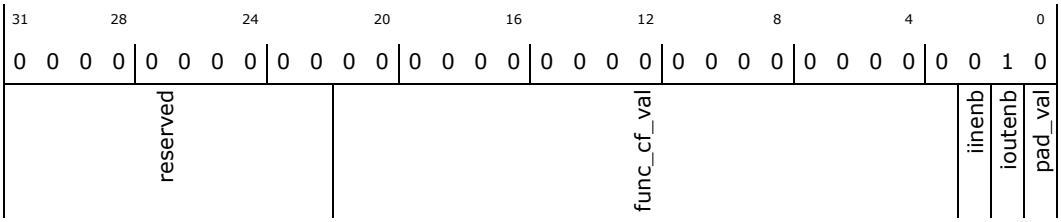
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data0_PAD_VAL: [IOBASE + 2000h] + 388h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low

Bit Range	Default & Access	Description
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.172 Usb Ulpi 0 Data5 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data5_PCONF0)—Offset 390h

PADs Memory space configuration register (Access via PCU Proxy)

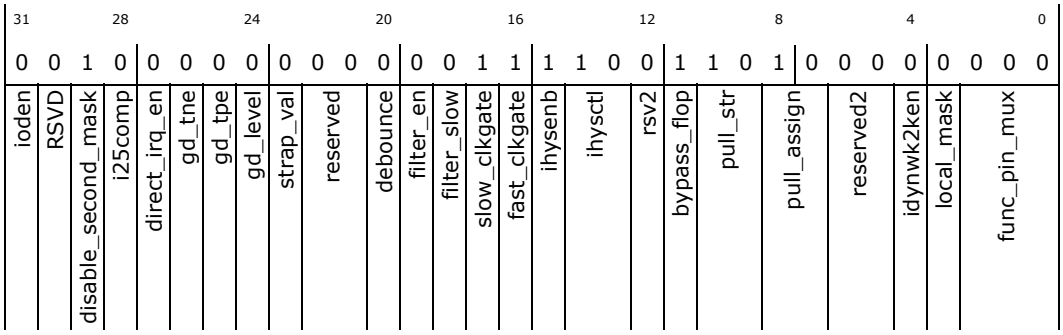
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data5_PCONF0: [IOBASE + 2000h] + 390h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_37 function 1 is USB_ULPI_0_DATA5 function 2 is USH_HBP[5] function 3 is MCSI_LPDEBUG[9]

3.69.173 Usb Ulpi 0 Data5 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data5_PCONF1)—Offset 394h

DLL Multiplexer

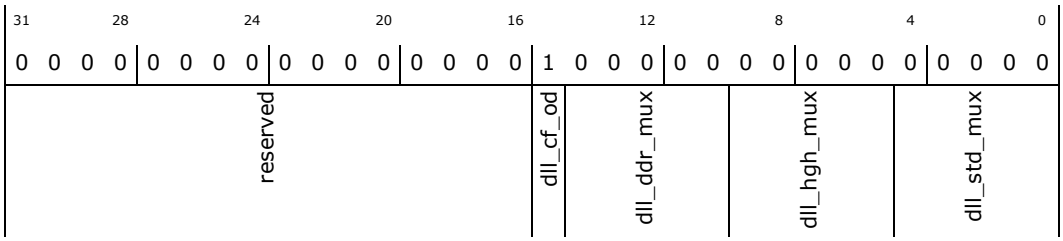
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data5_PCONF1: [IOBASE + 2000h] + 394h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.174 Usb Ulpi 0 Data5 Pad Value (cfio_regs_pad_usb_ulpi_0_data5_PAD_VAL)—Offset 398h

PADs Memory space Value register (Access via PCU Proxy)

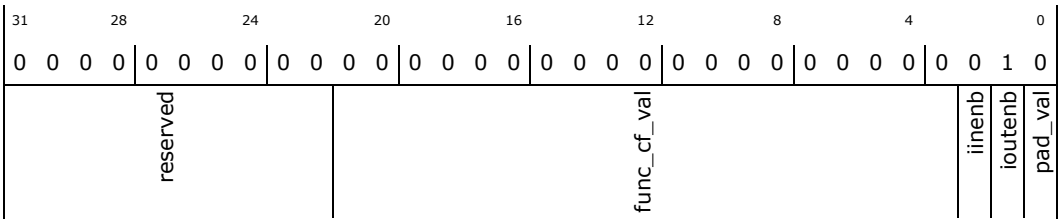
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data5_PAD_VAL: [IOBASE + 2000h] + 398h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.175 Usb Ulpi 0 Data7 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data7_PCONF0)—Offset 3A0h

PADs Memory space configuration register (Access via PCU Proxy)

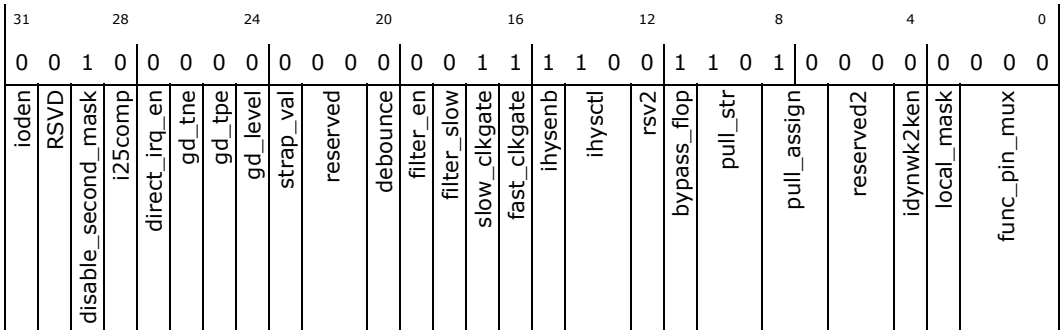
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data7_PCONF0: [IOBASE + 2000h] + 3A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock

Bit Range	Default & Access	Description
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_39 function 1 is USB_ULPI_0_DATA7 function 2 is USH_HBP[3] function 3 is MCSI_LPDEBUG[7]

3.69.176 Usb Ulpi 0 Data7 Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_data7_PCONF1)—Offset 3A4h

DLL Multiplexer

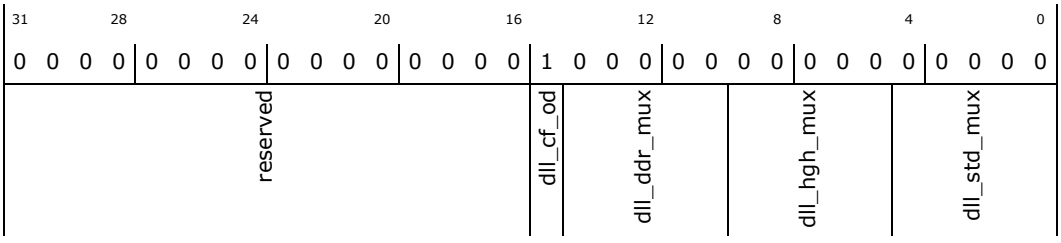
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data7_PCONF1: [IOBASE + 2000h] + 3A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.177 Usb Ulpi 0 Data7 Pad Value (cfio_regs_pad_usb_ulpi_0_data7_PAD_VAL)—Offset 3A8h

PADs Memory space Value register (Access via PCU Proxy)

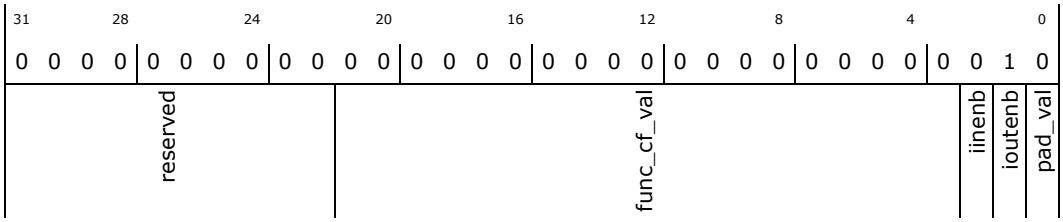
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_data7_PAD_VAL: [IOBASE + 2000h] + 3A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low

Bit Range	Default & Access	Description
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.178 Usb Ulpi 0 Stp Pad Configuration (cfio_regs_pad_usb_ulpi_0_stp_PCONF0)—Offset 3B0h

PADs Memory space configuration register (Access via PCU Proxy)

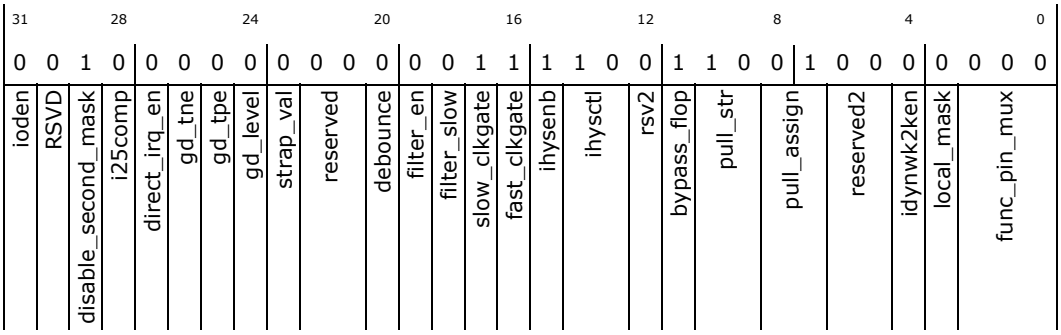
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_stp_PCONF0: [IOBASE + 2000h] + 3B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h



Bit Range	Default & Access	Description
31	0b RW	**Ioden (ioden):** Open Drain enable. Active high. Voltage domain: vcccore_1p0
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** This bit will disable second mask when PB_CONFIG all_func_mask is used. The second mask is for changing the pull and the direction of the pad in different cycles. Please refer to the GPIO HAS for details.
28	0b RO	**I25comp (i25comp):** 25 ohm compensation of hflvt buffers
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will used direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No falling edge detect. 1 - Detect rising edge. (may be overridden and inaccessible to memory region write by legacy write). For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be chosen and not edge irq
23	0b RO	**Strap Val (strap_val):** If strap pin exist, this bit will reflect its value even if overridden with DFT value
22:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debouce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter
18	0b RW	**Filter Slow (filter_slow):** Use RTC clock for unglitch filter. This bit is reserved if unglitch filter does not exist for this pad
17	1b RW	**Slow Clkgate (slow_clkgate):** 1 Enables the glitch filter slow clock
16	1b RW	**Fast Clkgate (fast_clkgate):** 1 Enables the glitch filter fast clock
15	1b RO	**Ihysenb (ihysenb):** Hysteresis enable, active low
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control
12	0b RO	**Rsv2 (rsv2):** reserved
11	1b RO	**Bypass Flop (bypass_flop):** 1 - Bypass pad controller I/O flops (if exists) 0 - Flop enabled if exists.
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - 10K 10 - 20K 11 - 40K
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment: 00 - Non pull 01 - Pull Up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved2 (reserved2):** reserved
4	0b RW	**Idynwk2ken (idynwk2ken):** reduce weak 2kohm pull contention current when other chip driving
3	0b RO	**Local Mask (local_mask):** reserved

Bit Range	Default & Access	Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. The func_pin_mux function is masked by all_func_mask bit at the PB_CONFIG register. When IO_USE_SEL is set the pad will choose the GPIO function. function 0 is GPIOS_42 function 1 is USB_ULPI_0_STP function 2 is USH_HBP[0] function 3 is MCSI_LPDEBUG[4] For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

3.69.179 Usb Ulpi 0 Stp Delay Line Multiplexer (cfio_regs_pad_usb_ulpi_0_stp_PCONF1)—Offset 3B4h

DLL Multiplexer

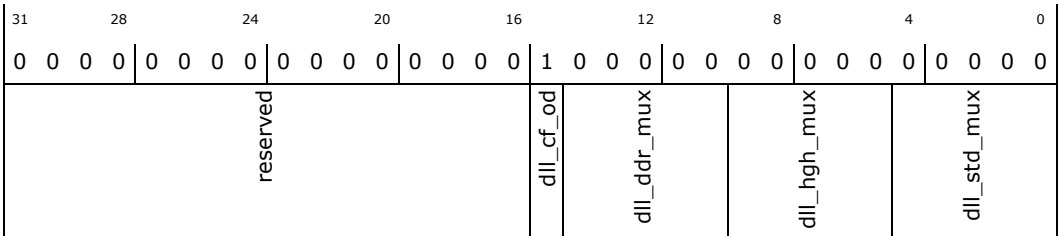
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_stp_PCONF1: [IOBASE + 2000h] + 3B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (reserved):** reserved
15	1b RO	**Dll Cf Od (dll_cf_od):** cf values, software override enable
14:10	00000b RO	**Dll Ddr Mux (dll_ddr_mux):** Delay ddr mux
9:5	00000b RO	**Dll Hgh Mux (dll_hgh_mux):** Delay high mux
4:0	00000b RO	**Dll Std Mux (dll_std_mux):** Delay standard mux

3.69.180 Usb Ulpi 0 Stp Pad Value (cfio_regs_pad_usb_ulpi_0_stp_PAD_VAL)—Offset 3B8h

PADs Memory space Value register (Access via PCU Proxy)

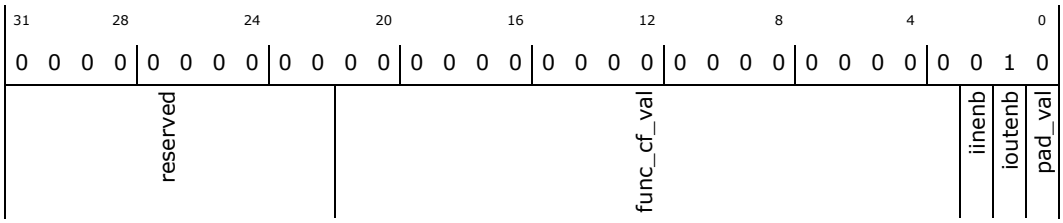
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pad_usb_ulpi_0_stp_PAD_VAL: [IOBASE + 2000h] + 3B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h



Bit Range	Default & Access	Description
31:22	0h RO	**Reserved (reserved):** reserved
21:3	0h RO	**Func Cf Val (func_cf_val):** c and f values for the function delay, first 15 bits are c value and 4 msb are the f value
2	0b RW	**Iinenb (iinenb):** input enable - active low
1	1b RW	**Ioutenb (ioutenb):** output enable - active low
0	0b WO	**Pad Val (pad_val):** These registers are implemented as dual read/write with dedicated storage each. This is the same register as GP_LVL for IO space. (may be overridden and inaccessible to memory region write by legacy write) - default value can be both high or low. When the register is read it is reading the pad value. When pad is written it writes the pad value only if it is output enable and it is a gpio function

3.69.181 C71p1cfiomvnsusdfxgpio1 Compensation Configuration (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_CFG)—Offset 610h

FAMs Memory space Value register

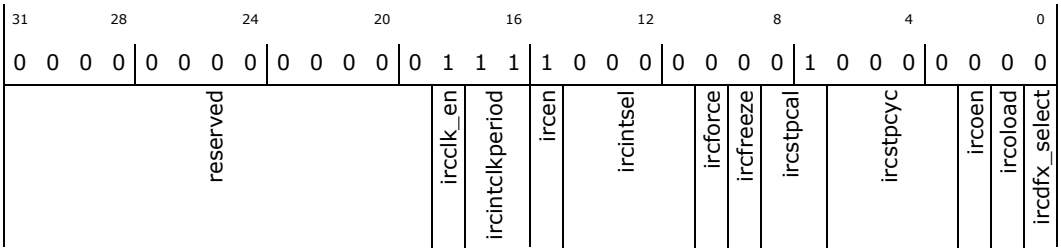
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_CFG: [IOBASE + 2000h] + 610h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078080h



Bit Range	Default & Access	Description
31:19	0000h RO	**Reserved (reserved):** reserved
18	1b RW	**Ircclk En (ircclk_en):** This is enabling the rcomp clock. When rcomp clock is gated, rcomp reset is forced too, so when it is ungated again it will compensate
17:16	11b RW	**Ircintclkperiod (ircintclkperiod):** reserved
15	1b RW	**Ircen (ircen):** Enable RCOMP state machine for periodic RCOMP mode. This has to be enabled throughout periodic mode .0 state machine disabled 1 state machine enabled (default)
14:11	0000b RW	**Ircintsel (ircintsel):** Interval select this will select the periodic RCOMP update interval. All are periodic mode except 0000 option. 0000 non-periodic mode 0.5ms - 0001 1ms 0010 2ms 0011 3ms - 0100 4ms - 0101 5ms - 0110 10ms 0111 (Default) 15ms - 1000 25ms - 1001 50ms - 1010 100ms - 1011 200ms 1100 500ms - 1101 1000ms - 1110 2000ms - 1111 (non-periodic mode RCOMP update is not automatically triggered after the initial RCOMP cycle)
10	0b RW	**Ircforce (ircforce):** Force rcomp. only valid during non-periodic mode. RCOMP SM will trigger upon this signal goes high, so need first to clear it, and then set it high
9	0b RW	**Ircfreeze (ircfreeze):** Freeze rcomp. only valid during periodic mode. Setting this bit to 1 will stop the RCOMP S/M by stopping and clearing the 1ms and 10ms counter. Clearing it (0) would enable 1ms and 10ms counter again.
8:7	01b RW	**Ircstpcal (ircstpcal):** Stop calibration option. RCOMP SM (pullup and pulldown) will finish calibrating once orcpupen/orcpdnen toggle/s. The toggling would indicate the compensation value has been reached. This options is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by ircstpcyc input). 00 single edge detect (10 or 01) 01 double edge detect (101 or 010) (default) 10 triple edge detect (1010 or 0101) 11 stop after x cycles (depending on ircompstpcyc[3:0] value -- This is meant for debug) Default is 01 (double edge detect 101 or 010)
6:3	0000b RW	**Ircstpcyc (ircstpcyc):** Number of cycles calibration would be going through before stopping.0000 0 cycle 0001 1 cycle 0010 2 cycles ..... 1110 14 cycles 1111 15 cycles (maximum allowed with this options) valid only when ircompstpcal[1:0]=2b11. This is meant for debug.
2	0b RW	**Ircoen (ircoen):** Override enable. Setting this bit would allow system to go and override RCOMP value with data from config registers (which will drive ircpuov and ircpdov)

Bit Range	Default & Access	Description
1	0b RW	**Ircoload (ircoload):** Do override now. only valid with ircoen enabled. once this bit is set, data from ircpuov and ircpdov will be loaded into each buffer
0	0b RW	**Ircdfx Select (ircdfx_select):** Bypass RCOMP calibration values and use DFX values instead. Setting this bit (1) would let ircdfx_pstr and ircdfx_nstr value loaded into all buffers.

3.69.182 C71p1cfiomvnsusdfxgpio1 Compensation Override (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_OV)—Offset 614h

FAMs Memory space Value register

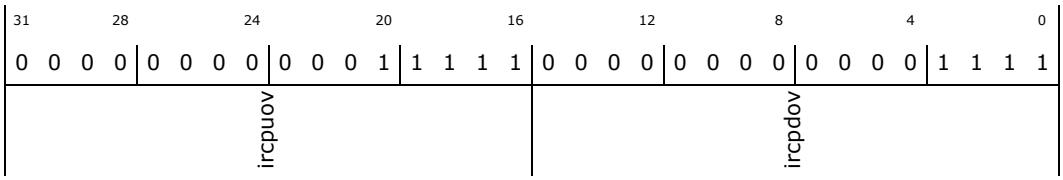
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_OV: [IOBASE + 2000h] + 614h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 001F000Fh



Bit Range	Default & Access	Description
31:16	001fh RW	**Ircpuov (ircpuov):** override RCOMP value for pullup Should be 50ohm typical corner.
15:0	000fh RW	**Ircpdov (ircpdov):** override RCOMP value for pulldown Should be 50ohm typical corner.

3.69.183 C71p1cfiomvnsusdfxgpio1 Compensation Initial Values (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_INIT)—Offset 618h

FAMs Memory space Value register

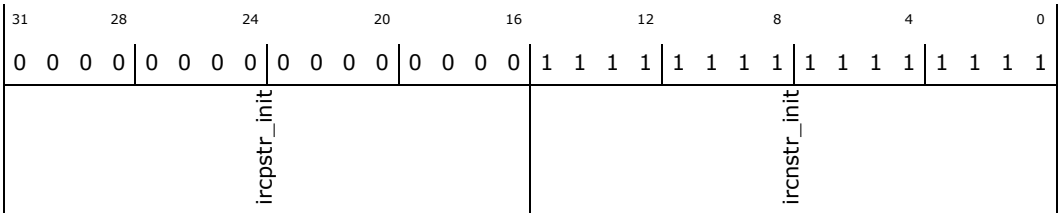
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_INIT: [IOBASE + 2000h] + 618h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0000FFFFh



Bit Range	Default & Access	Description
31:16	0000h RW	**Ircpstr Init (ircpstr_init):** Initial pleg calibration value. Should not be changed.
15:0	FFFFh RW	**Ircnstr Init (ircnstr_init):** Initial nleg calibration value. Should not be changed.

3.69.184 C71p1cfiomvnsusdfxgpio1 Compensation DFX Override (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_DFX)—Offset 61Ch

FAMs Memory space Value register

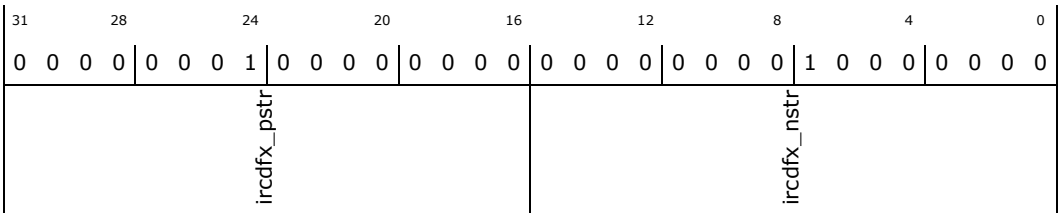
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_DFX: [IOBASE + 2000h] + 61Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01000080h



Bit Range	Default & Access	Description
31:16	0100h RW	**Ircdfx Pstr (ircdfx_pstr):** DFX compensation p-leg value. Should be 50ohm typical corner.
15:0	0080h RW	**Ircdfx Nstr (ircdfx_nstr):** DFX compensation n-leg value Should be 50ohm typical corner.

3.69.185 TS0 SSUS Interrupt Status 0 (cfio_regs_REG_TS0_SSUS_IRQ_TS_0)—Offset 800h

IRQ TS 0 status register

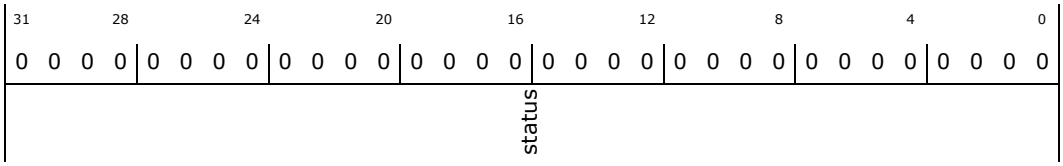
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_TS0_SSUS_IRQ_TS_0: [IOBASE + 2000h] + 800h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RWOC	**Status (status):** TS: Trigger Status: When set to a 1, the corresponding GPIO (if disabled in the GPIO_USE_SEL register) if enabled as input via , triggered an IRQ event. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. Each bit is associated with different PAD controller, see RDL. Bellow is the given list of gpio number and pads, the irq status refers to bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

3.69.186 TS1 SSUS Interrupt Status 1 (cfio_regs_REG_TS1_SSUS_IRQ_TS_1)—Offset 804h

IRQ TS 1 status register

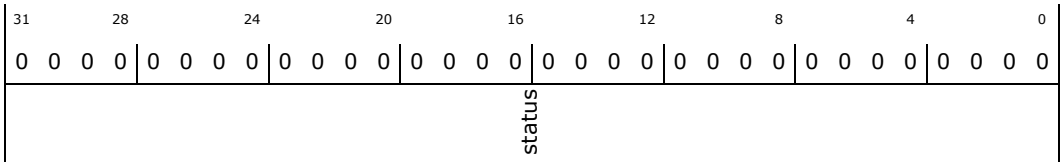
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_TS1_SSUS_IRQ_TS_1: [IOBASE + 2000h] + 804h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RWOC	**Status (status):** TS: Trigger Status: When set to a 1, the corresponding GPIO (if disabled in the GPIO_USE_SEL register) if enabled as input via , triggered an IRQ event. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. Each bit is associated with different PAD controller, see RDL. Bellow is the given list of gpio number and pads, the irq status refers to bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

3.69.187 TS2 SSUS Interrupt Status 2 (cfio_regs_REG_TS2_SSUS_IRQ_TS_2)—Offset 808h

IRQ TS 2 status register

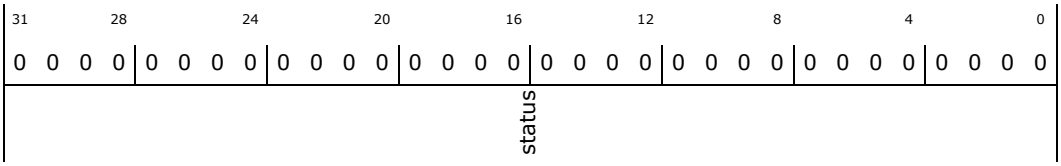
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_TS2_SSUS_IRQ_TS_2: [IOBASE + 2000h] + 808h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RWOC	**Status (status):** TS: Trigger Status: When set to a 1, the corresponding GPIO (if disabled in the GPIO_USE_SEL register) if enabled as input via , triggered an IRQ event. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. Each bit is associated with different PAD controller, see RDL. Bellow is the given list of gpio number and pads, the irq status refers to

3.69.188 TS3 SSUS Interrupt Status 3 (cfio_regs_REG_TS3_SSUS_IRQ_TS_3)—Offset 80Ch

IRQ TS 3 status register

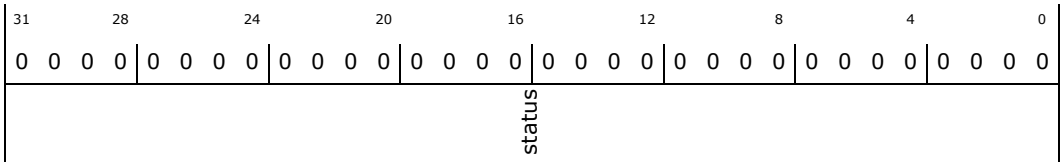
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_TS3_SSUS_IRQ_TS_3: [IOBASE + 2000h] + 80Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RWOC	**Status (status):** TS: Trigger Status: When set to a 1, the corresponding GPIO (if disabled in the GPIO_USE_SEL register) if enabled as input via , triggered an IRQ event. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. Each bit is associated with different PAD controller, see RDL. Bellow is the given list of gpio number and pads, the irq status refers to

3.69.189 Itp Strength Group (cfio_regs_itp_STRENGTH)—Offset 850h

P and N strength register

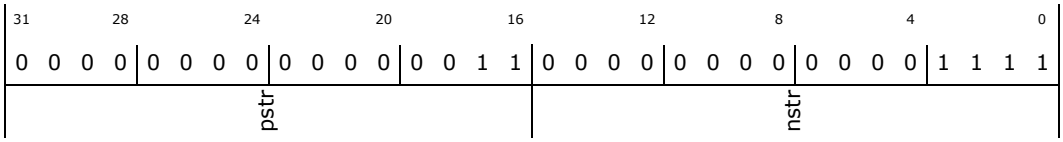
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_itp_STRENGTH: [IOBASE + 2000h] + 850h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.69.190 Sus Rcomp Strength Group (cfio_regs_sus_rcomp_STRENGTH)—Offset 854h

P and N strength register

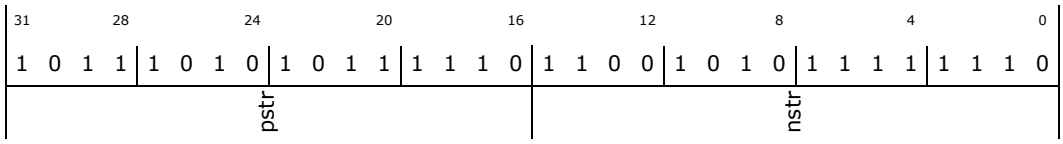
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sus_rcomp_STRENGTH: [IOBASE + 2000h] + 854h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: BABECAFEh



Bit Range	Default & Access	Description
31:16	babeh RO	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	cafeh RO	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.69.191 Sus Spi Strength Group (cfio_regs_sus_spi_STRENGTH)—Offset 858h

P and N strength register

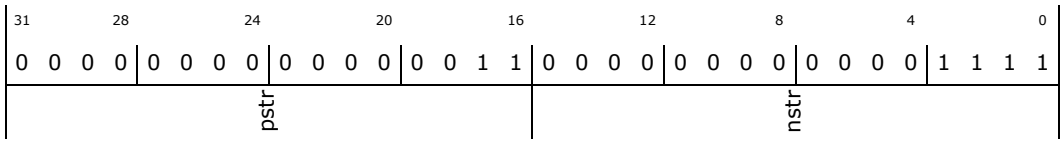
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sus_spi_STRENGTH: [IOBASE + 2000h] + 858h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.69.192 Ulpi Strength Group (cfio_regs_ulpi_STRENGTH)—Offset 85Ch

P and N strength register

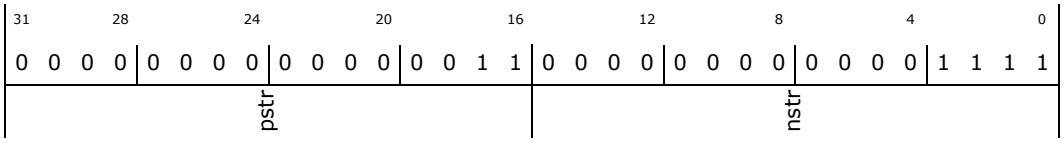
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_ulpi_STRENGTH: [IOBASE + 2000h] + 85Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh



Bit Range	Default & Access	Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negative strength - for cfiohvio buffers, only the 3 lsb bits will be used

3.69.193 Dfx Electrical Group (cfio_regs_dfx_ELECTRICAL)—Offset 860h

Electrical register includes slew and static values

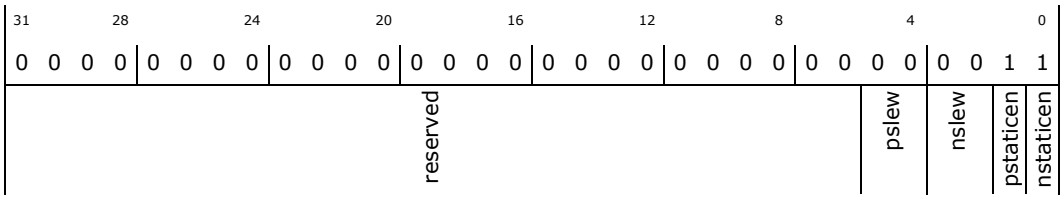
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_dfx_ELECTRICAL: [IOBASE + 2000h] + 860h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used

Bit Range	Default & Access	Description
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.194 Itp Electrical Group (cfio_regs_itp_ELECTRICAL)—Offset 864h

Electrical register includes slew and static values

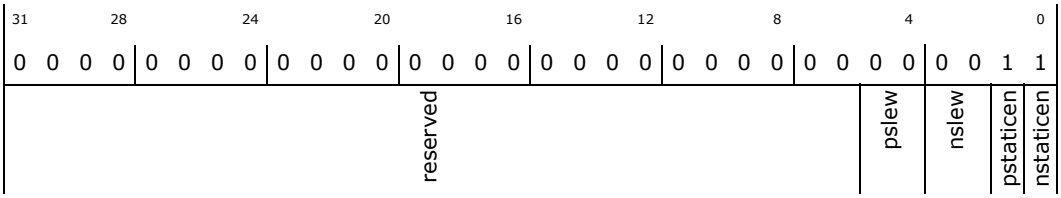
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_itp_ELECTRICAL: [IOBASE + 2000h] + 864h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.195 Pmu Electrical Group (cfio_regs_pmu_ELECTRICAL)—Offset 868h

Electrical register includes slew and static values

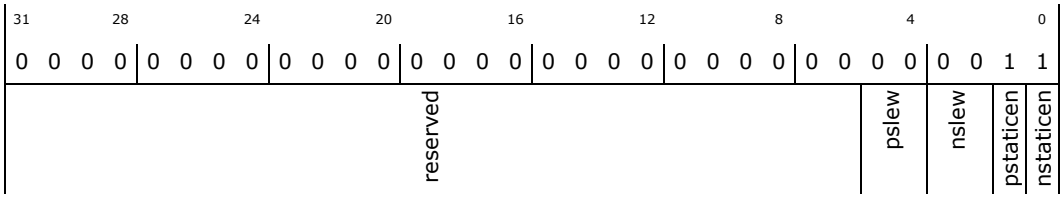
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_pmu_ELECTRICAL: [IOBASE + 2000h] + 868h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.196 Sec Electrical Group (cfio_regs_sec_ELECTRICAL)—Offset 86Ch

Electrical register includes slew and static values

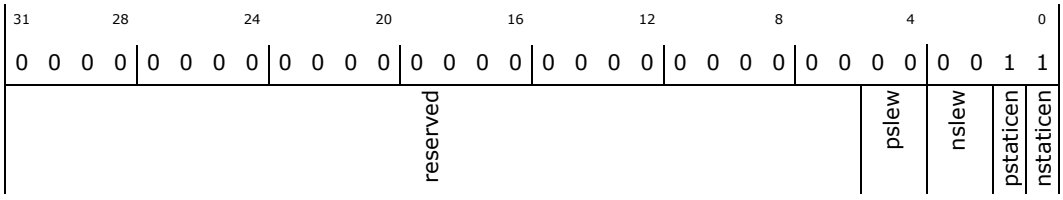
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sec_ELECTRICAL: [IOBASE + 2000h] + 86Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved

Bit Range	Default & Access	Description
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.197 Sec10 Electrical Group (cfio_regs_sec10_ELECTRICAL)—Offset 870h

Electrical register includes slew and static values

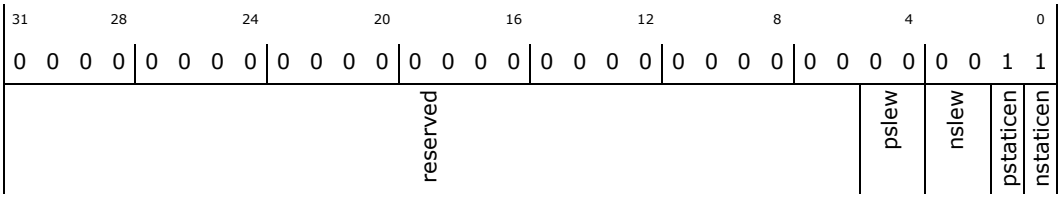
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sec10_ELECTRICAL: [IOBASE + 2000h] + 870h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.198 Sus1 Electrical Group (cfio_regs_sus1_ELECTRICAL)—Offset 874h

Electrical register includes slew and static values

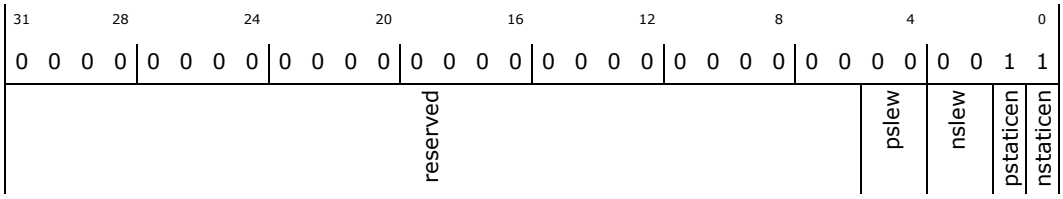
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sus1_ELECTRICAL: [IOBASE + 2000h] + 874h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.199 Sus2 Electrical Group (cfio_regs_sus2_ELECTRICAL)—Offset 878h

Electrical register includes slew and static values

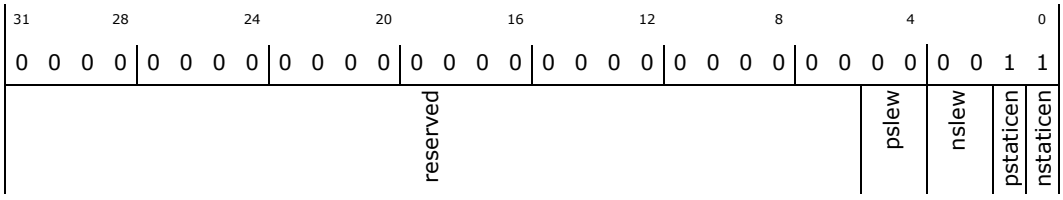
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sus2_ELECTRICAL: [IOBASE + 2000h] + 878h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.200 Sus3 Electrical Group (cfio_regs_sus3_ELECTRICAL)—Offset 87Ch

Electrical register includes slew and static values

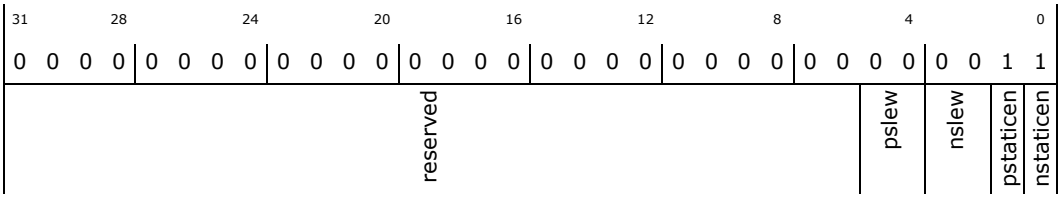
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sus3_ELECTRICAL: [IOBASE + 2000h] + 87Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.201 Sus4 Electrical Group (cfio_regs_sus4_ELECTRICAL)—Offset 880h

Electrical register includes slew and static values

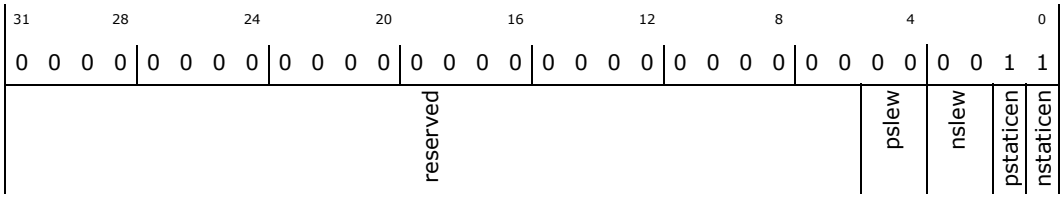
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sus4_ELECTRICAL: [IOBASE + 2000h] + 880h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.202 Sus Spi Electrical Group (cfio_regs_sus_spi_ELECTRICAL)—Offset 884h

Electrical register includes slew and static values

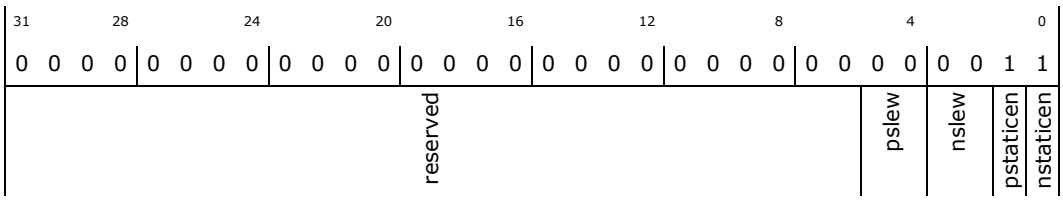
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_sus_spi_ELECTRICAL: [IOBASE + 2000h] + 884h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.203 Tap Electrical Group (cfio_regs_tap_ELECTRICAL)—Offset 888h

Electrical register includes slew and static values

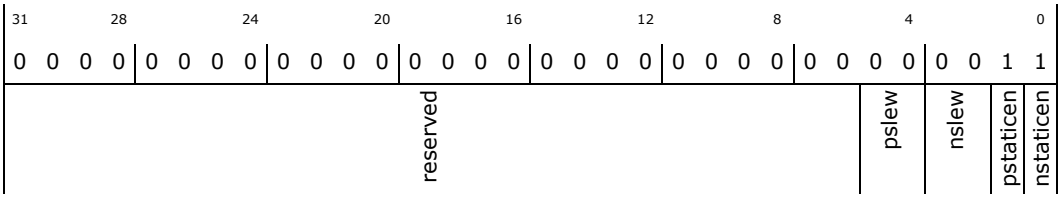
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_tap_ELECTRICAL: [IOBASE + 2000h] + 888h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.204 Ulpi Electrical Group (cfio_regs_ulpi_ELECTRICAL)—Offset 88Ch

Electrical register includes slew and static values

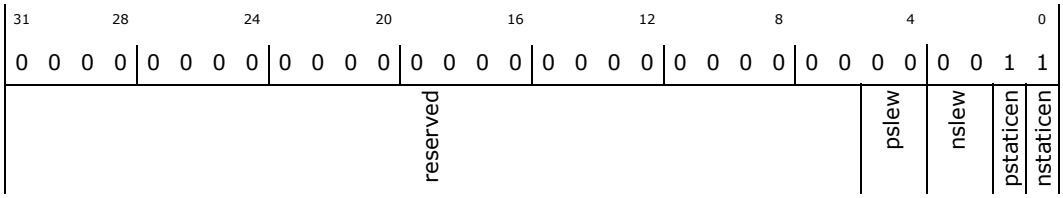
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_ulpi_ELECTRICAL: [IOBASE + 2000h] + 88Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.205 Usb Electrical Group (cfio_regs_usb_ELECTRICAL)—Offset 890h

Electrical register includes slew and static values

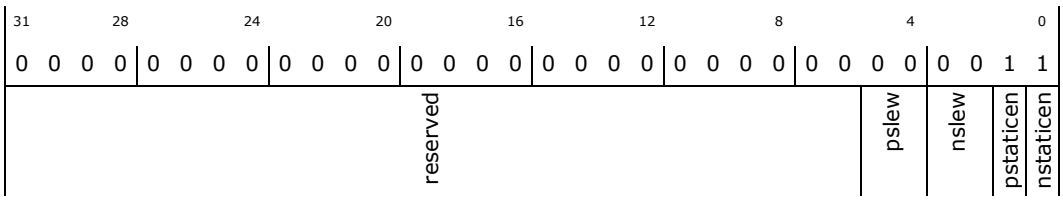
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_usb_ELECTRICAL: [IOBASE + 2000h] + 890h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:6	0000h RO	**Reserved (reserved):** reserved
5:4	00b RW	**Pslew (pslew):** positive slew rate - for cfiohvio buffers, only the lsb will be used
3:2	00b RW	**Nslew (nslew):** negative slew rate - for cfiohvio buffers, only the lsb will be used
1	1b RW	**Pstaticen (pstaticen):** enable positive static
0	1b RW	**Nstaticen (nstaticen):** enable negative static

3.69.206 CFG SSUS PSB Configuration (cfio_regs_COM_CFG_SSUS_PB_CONFIG)—Offset 900h

PSB configuration register for setup and hold times configuration.

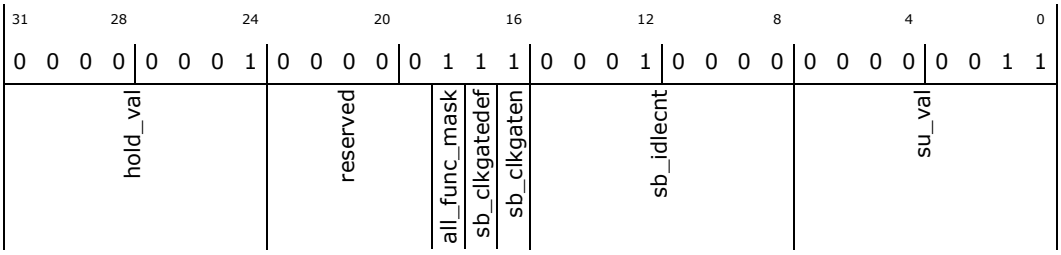
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_COM_CFG_SSUS_PB_CONFIG: [IOBASE + 2000h] + 900h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01071003h



Bit Range	Default & Access	Description
31:24	01h RW	**Hold Val (hold_val):** Hold Value - number of cycles to for hold.
23:19	00000b RO	**Reserved (reserved):** reserved
18	1b RW	**All Func Mask (all_func_mask):** all_func_mask - masking the functional function select for south cfio, reserved for north use
17	1b RW	**Sb Clkgatedef (sb_clkgatedef):** Sideband clock gate default
16	1b RW	**Sb Clkgaten (sb_clkgaten):** Sideband clock gate enable
15:8	10h RW	**Sb Idlecnt (sb_idlecnt):** Sideband idle count

Bit Range	Default & Access	Description
7:0	03h RW	**Su Val (su_val):** Setup Value - number of cycles to for setup.

3.69.207 IRQ TYPE SSUS Interrupt Type (cfio_regs_REG_IRQ_TYPE_SSUS_IRQ_TYPE)—Offset 904h

IRQ TYPE register

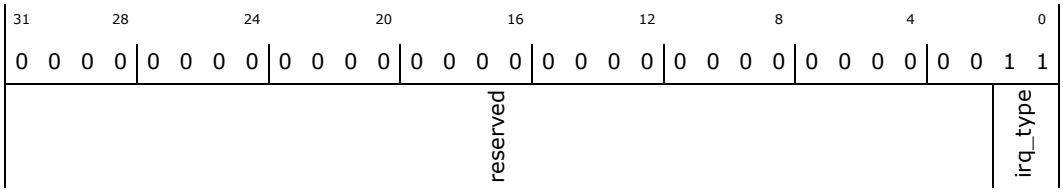
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_IRQ_TYPE_SSUS_IRQ_TYPE: [IOBASE + 2000h] + 904h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000003h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved (reserved):** reserved
1:0	11b RO	**Irq Type (irq_type):** IRQ message type. This field defines the IRQ message type that community will send to ILB 00 =) IRQ5 opcode assert = C0, deassert = C1 01 =) IRQ6 opcode assert = C2, deassert = C3 10 =) IRQ7 opcode assert = CE, deassert = CF 11 =) IRQ13 opcode assert = D2, deassert = D3 - reserved, unused in VLV2

3.69.208 WR PATH SSUS Master Delay Line Write Address (cfio_regs_DLL_WR_PATH_SSUS_MDL_WRITE_PATH_C_F_ADDR)—Offset 950h

Master delay line write path values

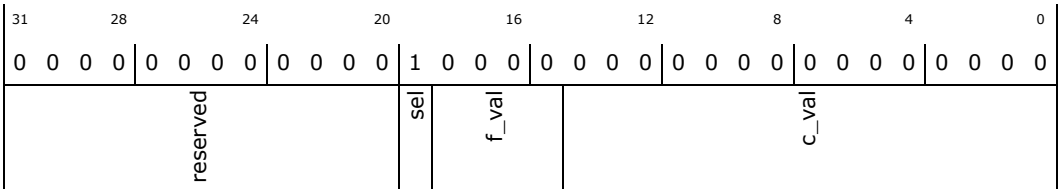
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_WR_PATH_SSUS_MDL_WRITE_PATH_C_F_ADDR: [IOBASE + 2000h] + 950h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00080000h



Bit Range	Default & Access	Description
31:20	000h RO	**Reserved (reserved):** reserved
19	1b RW	**Sel (sel):** DLL f_c select
18:15	0000b RW	**F Val (f_val):** write path f value
14:0	0h RW	**C Val (c_val):** write path c value

3.69.209 WR PATH1 MUX SSUS Delay Line Write Multiplexer 1 (cfio_regs_DLL_WR_PATH1_MUX_SSUS_DLL_WRITE_PATH1_MUX)—Offset 954h

Master delay line write path mux values

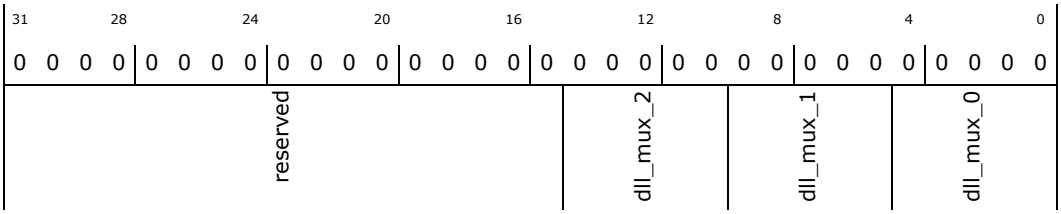
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_WR_PATH1_MUX_SSUS_DLL_WRITE_PATH1_MUX: [IOBASE + 2000h] + 954h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RO	**Reserved (reserved):** reserved
14:10	0h RW	**Dll Mux 2 (dll_mux_2):** mux select 2 for dll
9:5	0h RW	**Dll Mux 1 (dll_mux_1):** mux select 1 for dll
4:0	0h RW	**Dll Mux 0 (dll_mux_0):** mux select 0 for dll

3.69.210 WR PATH2 MUX SSUS Delay Line Write Multiplexer 2 (cfio_regs_DLL_WR_PATH2_MUX_SSUS_DLL_WRITE_PATH2_MUX)—Offset 958h

Master delay line write path mux values

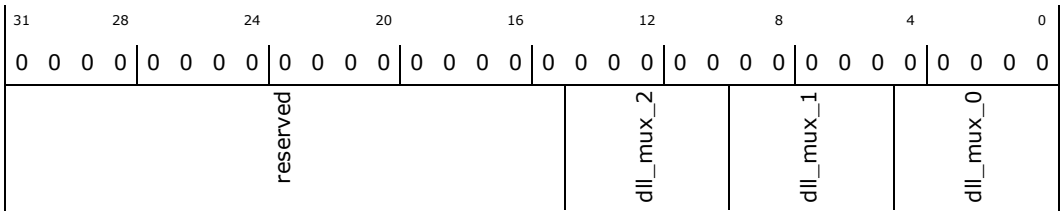
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_WR_PATH2_MUX_SSUS_DLL_WRITE_PATH2_MUX: [IOBASE + 2000h] + 958h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RO	**Reserved (reserved):** reserved
14:10	0h RW	**Dll Mux 2 (dll_mux_2):** mux select 2 for dll
9:5	0h RW	**Dll Mux 1 (dll_mux_1):** mux select 1 for dll
4:0	0h RW	**Dll Mux 0 (dll_mux_0):** mux select 0 for dll

3.69.211 WR PATH3 MUX SSUS Delay Line Write Multiplexer 3 (cfio_regs_DLL_WR_PATH3_MUX_SSUS_DLL_WRITE_PATH3_MUX)—Offset 95Ch

Master delay line write path mux values

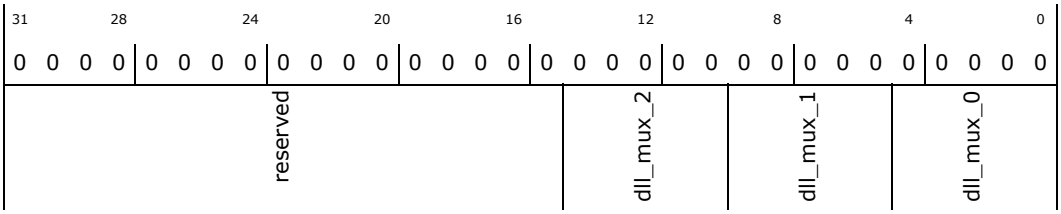
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_WR_PATH3_MUX_SSUS_DLL_WRITE_PATH3_MUX: [IOBASE + 2000h] + 95Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0h RO	**Reserved (reserved):** reserved
14:10	0h RW	**Dll Mux 2 (dll_mux_2):** mux select 2 for dll
9:5	0h RW	**Dll Mux 1 (dll_mux_1):** mux select 1 for dll
4:0	0h RW	**Dll Mux 0 (dll_mux_0):** mux select 0 for dll

3.69.212 FIFO SSUS Emmc Fifo Control (cfio_regs_EMMC_FIFO_SSUS_EMMC_FIFO)—Offset 960h

EMMC fifo controller

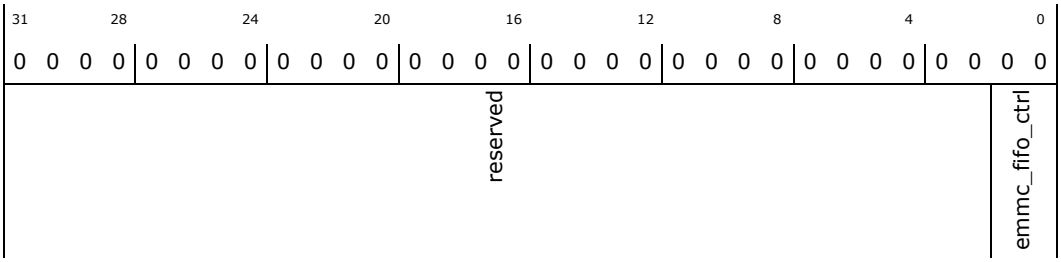
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_EMMC_FIFO_SSUS_EMMC_FIFO: [IOBASE + 2000h] + 960h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**Reserved (reserved):** reserved
1:0	00b RW	**Emmc Fifo Ctrl (emmc_fifo_ctrl):** reserved

3.69.213 INIT SSUS Master Delay Line Initial Values (cfio_regs_DLL_INIT_SSUS_MDL_CF_INIT)—Offset 964h

Master delay line c and f init values

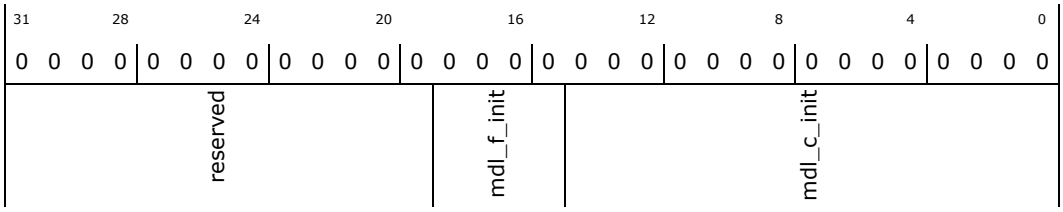
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_INIT_SSUS_MDL_CF_INIT: [IOBASE + 2000h] + 964h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0000h RO	**Reserved (reserved):** reserved
18:15	0h RW	**Mdl F Init (mdl_f_init):** Master delay f init value
14:0	0000h RW	**Mdl C Init (mdl_c_init):** Master delay c init value

3.69.214 SW MODE SSUS Master Delay Line Software Values (cfio_regs_DLL_SW_MODE_SSUS_MDL_CF_SW)—Offset 968h

Master delay line c and f software values

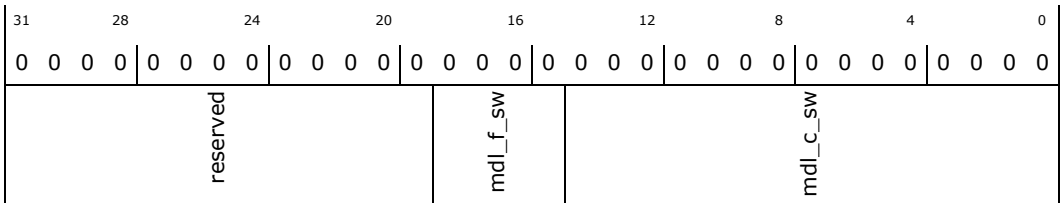
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_SW_MODE_SSUS_MDL_CF_SW: [IOBASE + 2000h] + 968h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0000h RO	**Reserved (reserved):** reserved
18:15	0h RW	**Mdl F Sw (mdl_f_sw):** Master delay f software value
14:0	0000h RW	**Mdl C Sw (mdl_c_sw):** Master delay c software value

3.69.215 VALS SSUS Master Delay Line Fsm Values (cfio_regs_DLL_VALS_SSUS_MDL_FSM_VALS)—Offset 96Ch

Master delay line fsm values

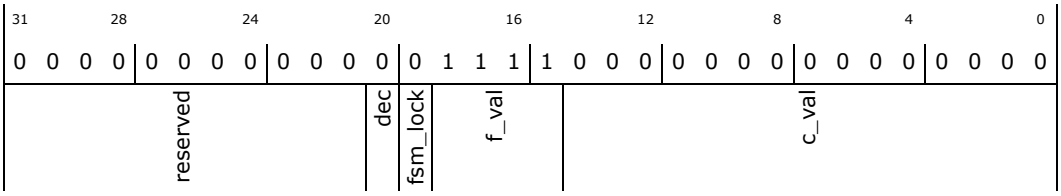
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_VALS_SSUS_MDL_FSM_VALS: [IOBASE + 2000h] + 96Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078000h



Bit Range	Default & Access	Description
31:21	0h RO	**Reserved (reserved):** reserved
20	0b RO	**Dec (dec):** fsm decrease
19	0b RO	**Fsm Lock (fsm_lock):** fsm lock
18:15	1111b RO	**F Val (f_val):** fsm f value
14:0	0h RO	**C Val (c_val):** fsm c value

3.69.216 CTRL SSUS Master Delay Line Fsm Control (cfio_regs_DLL_CTRL_SSUS_MDL_FSM_CTRL)—Offset 970h

Master delay line fsm controller

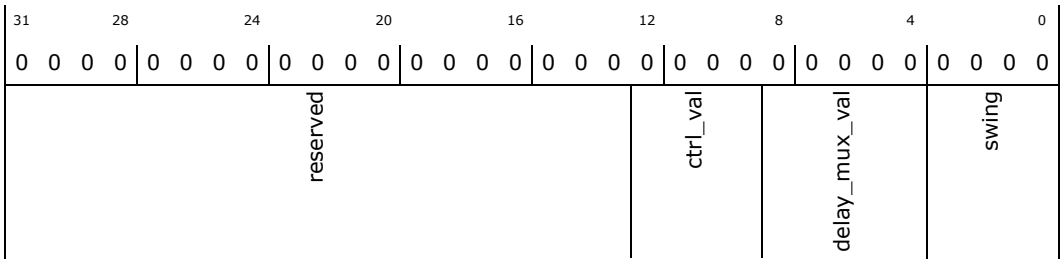
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_DLL_CTRL_SSUS_MDL_FSM_CTRL: [IOBASE + 2000h] + 970h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:13	0h RO	**Reserved (reserved):** reserved
12:9	0b RW	**Ctrl Val (ctrl_val):** fsm control value
8:4	00000b RW	**Delay Mux Val (delay_mux_val):** fsm delay mux value
3:0	0000b RW	**Swing (swing):** swing value

3.69.217 DIRECT IRQ0 SSUS Direct Interrupt Multiplexer 0 (cfio_regs_REG_DIRECT_IRQ0_SSUS_DIRECT_IRQ_0)—Offset 980h

Direct irq select register for irq 0 - 3

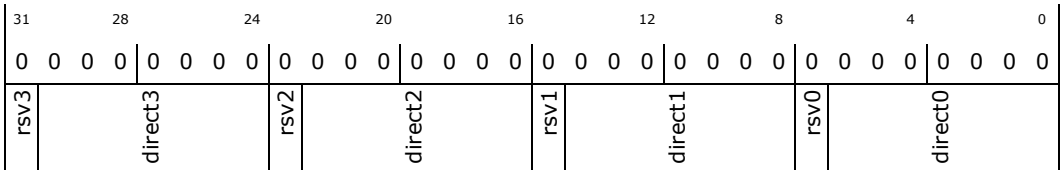
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_DIRECT_IRQ0_SSUS_DIRECT_IRQ_0: [IOBASE + 2000h] + 980h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31	0b R0	**Rsv3 (rsv3):** reserved
30:24	0000000b RW	**Direct3 (direct3):** Selects the 4th direct irq
23	0b R0	**Rsv2 (rsv2):** reserved
22:16	0000000b RW	**Direct2 (direct2):** Selects the 3th direct irq
15	0b R0	**Rsv1 (rsv1):** reserved
14:8	0000000b RW	**Direct1 (direct1):** Selects the 2nd direct irq
7	0b R0	**Rsv0 (rsv0):** reserved
6:0	0000000b RW	**Direct0 (direct0):** Selects the 1st direct irq

3.69.218 DIRECT IRQ1 SSUS Direct Interrupt Multiplexer 1 (cfio_regs_REG_DIRECT_IRQ1_SSUS_DIRECT_IRQ_1)—Offset 984h

Direct irq select register for irq 4 - 7

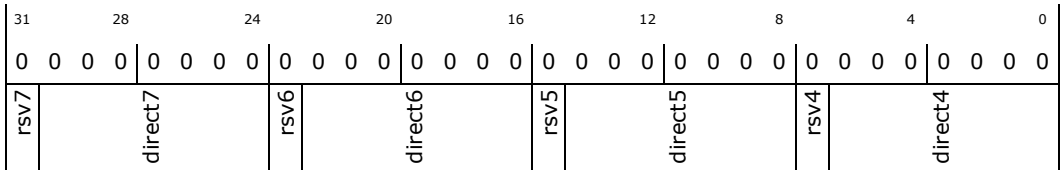
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_DIRECT_IRQ1_SSUS_DIRECT_IRQ_1:
[IOBASE + 2000h] + 984h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31	0b R0	**Rsv7 (rsv7):** reserved
30:24	0000000b RW	**Direct7 (direct7):** Selects the 8th direct irq
23	0b R0	**Rsv6 (rsv6):** reserved
22:16	0000000b RW	**Direct6 (direct6):** Selects the 7th direct irq

Bit Range	Default & Access	Description
15	0b R0	**Rsv5 (rsv5):** reserved
14:8	0000000b RW	**Direct5 (direct5):** Selects the 5th direct irq
7	0b R0	**Rsv4 (rsv4):** reserved
6:0	0000000b RW	**Direct4 (direct4):** Selects the 4th direct irq

3.69.219 DIRECT IRQ2 SSUS Direct Interrupt Multiplexer 2 (cfio_regs_REG_DIRECT_IRQ2_SSUS_DIRECT_IRQ_2)—Offset 988h

Direct irq select register for irq 8 - 11

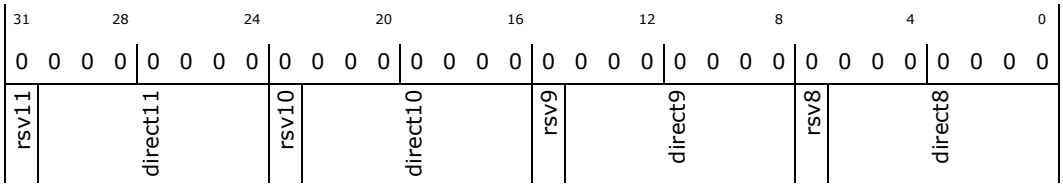
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_DIRECT_IRQ2_SSUS_DIRECT_IRQ_2: [IOBASE + 2000h] + 988h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31	0b R0	**Rsv11 (rsv11):** reserved
30:24	0000000b RW	**Direct11 (direct11):** Selects the 11th direct irq
23	0b R0	**Rsv10 (rsv10):** reserved
22:16	0000000b RW	**Direct10 (direct10):** Selects the 10th direct irq
15	0b R0	**Rsv9 (rsv9):** reserved
14:8	0000000b RW	**Direct9 (direct9):** Selects the 9th direct irq
7	0b R0	**Rsv8 (rsv8):** reserved

Bit Range	Default & Access	Description
6:0	0000000b RW	**Direct8 (direct8):** Selects the 8th direct irq

3.69.220 DIRECT IRQ3 SSUS Direct Interrupt Multiplexer 3 (cfio_regs_REG_DIRECT_IRQ3_SSUS_DIRECT_IRQ_3)—Offset 98Ch

Direct irq select register for irq 12 - 15

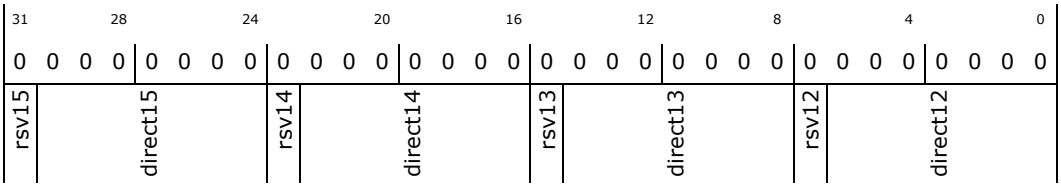
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

cfio_regs_REG_DIRECT_IRQ3_SSUS_DIRECT_IRQ_3: [IOBASE + 2000h] + 98Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31	0b R0	**Rsv15 (rsv15):** reserved
30:24	0000000b RW	**Direct15 (direct15):** Selects the 15th direct irq
23	0b R0	**Rsv14 (rsv14):** reserved
22:16	0000000b RW	**Direct14 (direct14):** Selects the 14th direct irq
15	0b R0	**Rsv13 (rsv13):** reserved
14:8	0000000b RW	**Direct13 (direct13):** Selects the 13th direct irq
7	0b R0	**Rsv12 (rsv12):** reserved
6:0	0000000b RW	**Direct12 (direct12):** Selects the 12th direct irq

3.70 PCU iLB IO APIC Memory Mapped I/O Registers

Table 78. Summary of PCU iLB I/O APIC Memory Mapped I/O Registers—

Offset	Size	Register ID—Description	Default Value
FEC00000h	1	"IDX (IOAPIC_IDX)—Offset FEC00000h" on page 4012	00h
FEC00010h	4	"WDW (IOAPIC_WDW)—Offset FEC00010h" on page 4012	00000000h
FEC00040h	4	"EOI (IOAPIC_EOI)—Offset FEC00040h" on page 4013	00000000h

3.70.1 IDX (IOAPIC_IDX)—Offset FEC00000h

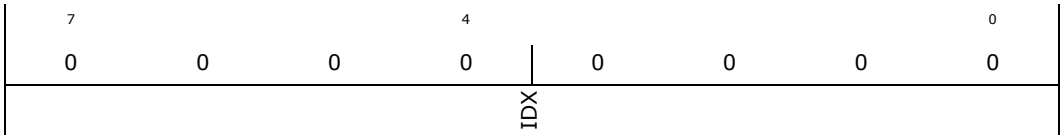
Index Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

IOAPIC_IDX: FEC00000h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RW	**IDX:** This 8-bit register selects which indirect register appears in the window register to be manipulated by software. Software will program this register to select the desired APIC internal register.

3.70.2 WDW (IOAPIC_WDW)—Offset FEC00010h

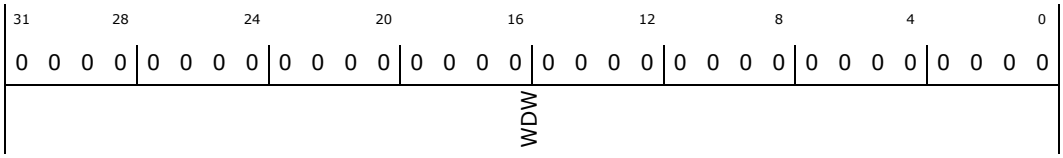
Window Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IOAPIC_WDW: FEC00010h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**WDW:** This 32-bit register specifies the data to be read or written to the register pointed to by the IDX register. This register can be accessed only in DW quantities.

3.70.3 EOI (IOAPIC_EOI)—Offset FEC00040h

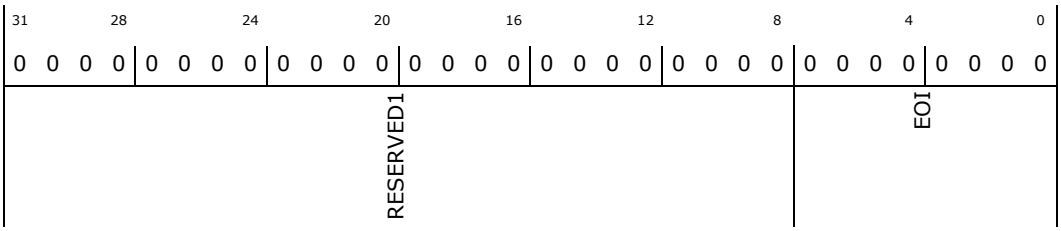
EOI Register

Access Method

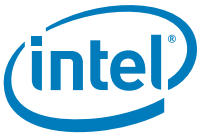
Type: Memory Mapped I/O Register (Size: 32 bits)

IOAPIC_EOI: FEC00040h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b WO	**RESERVED (RESERVED1):** Reserved.
7:0	0h WO	**EOI:** When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared.



3.71 PCU iLB 8259 Interrupt Controller (PIC) I/O Registers

Table 79. Summary of PCU iLB 8259 Interrupt Controller (PIC) I/O Registers—

Offset	Size	Register ID—Description	Default Value
20h	1	"MICW1—Offset 20h" on page 4014	00h
21h	1	"MICW2—Offset 21h" on page 4015	00h
24h	1	"MOCW2—Offset 24h" on page 4016	20h
25h	1	"MICW3—Offset 25h" on page 4017	00h
28h	1	"MOCW3—Offset 28h" on page 4017	22h
29h	1	"MICW4—Offset 29h" on page 4018	01h
2Dh	1	"MOCW1—Offset 2Dh" on page 4019	00h
A0h	1	"SICW1—Offset A0h" on page 4019	00h
A1h	1	"SICW2—Offset A1h" on page 4020	00h
A4h	1	"SOCW2—Offset A4h" on page 4021	20h
A5h	1	"SICW3—Offset A5h" on page 4022	00h
A8h	1	"SOCW3—Offset A8h" on page 4022	22h
A9h	1	"SICW4—Offset A9h" on page 4023	01h
ADh	1	"SOCW1—Offset ADh" on page 4024	00h
4D0h	1	"ELCR1—Offset 4D0h" on page 4024	00h
4D1h	1	"ELCR2—Offset 4D1h" on page 4025	00h

3.71.1 MICW1—Offset 20h

Master Initialization Command Word 1.A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs: * The Interrupt Mask register is cleared. * IRQ7 input is assigned priority 7. * The slave mode address is set to 7. * Special Mask Mode is cleared and Status Read is set to IRR. Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: I/O Register (Size: 8 bits)

MICW1: 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MCS85			ICWOCWSEL	LTIM	ADI	SNGL	IC4

Bit Range	Default & Access	Description
7:5	X WO	**MCS85:** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	X WO	**ICWOCWSEL:** ICW/OCW select: This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	X WO	**LTIM:** Edge/Level Bank Select (LTIM): Disabled. Replaced by ELCR1 and ELCR2.
2	X WO	**ADI:** ADI. Ignored for VLV. Should be programmed to 0.
1	X WO	**SNGL:** Single or Cascade (SNGL): Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	X WO	**IC4:** wICW4 Write Required (IC4): This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

3.71.2 MICW2—Offset 21h

Master ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: I/O Register
(Size: 8 bits)

MICW2: 21h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
IVBA					IRL		

Bit Range	Default & Access	Description
7:3	X WO	**IVBA:** Interrupt Vector Base Address: Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.

Bit Range	Default & Access	Description
2:0	X WO	**IRL:** Interrupt Request Level: When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

3.71.3 MOCW2—Offset 24h

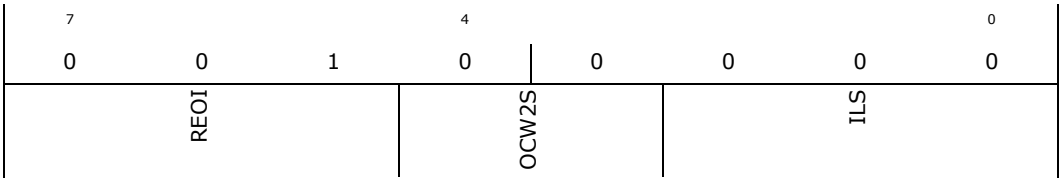
Master Operational Control Word 2 (Interrupt Mask).Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: I/O Register
(Size: 8 bits)

MOCW2: 24h

Default: 20h



Bit Range	Default & Access	Description
7:5	001b WO	**REOI:** Rotate and EOI Codes: R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 - Rotate in Auto EOI Mode (Clear) 001 - Non-specific EOI command 010 - No Operation 011 - *Specific EOI Command 100 - Rotate in Auto EOI Mode (Set) 101 - Rotate on Non-Specific EOI Command 110 - *Set Priority Command 111 - *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	X WO	**OCW2S:** OCW2 Select: When selecting OCW2, bits 4:3 = 00
2:0	X WO	**ILS:** Interrupt Level Select (L2, L1, L0): L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. Bits Interrupt Level Bits Interrupt Level 000 IRQ0/8 100 IRQ4/12 001 IRQ1/9 101 IRQ5/13 010 IRQ2/10 110 IRQ6/14 011 IRQ3/11 111 IRQ7/15

3.71.4 MICW3—Offset 25h

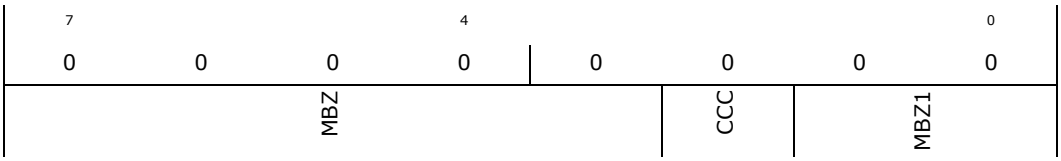
Master Initialization Command Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

MICW3: 25h

Default: 00h



Bit Range	Default & Access	Description
7:3	X WO	**MBZ:** These bits must be programmed to zero.
2	X WO	**CCC:** Cascaded Controller Connection (CCC): This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 15 is cascaded on IRQ2.
1:0	X WO	**MBZ (MBZ1):** These bits must be programmed to zero.

3.71.5 MOCW3—Offset 28h

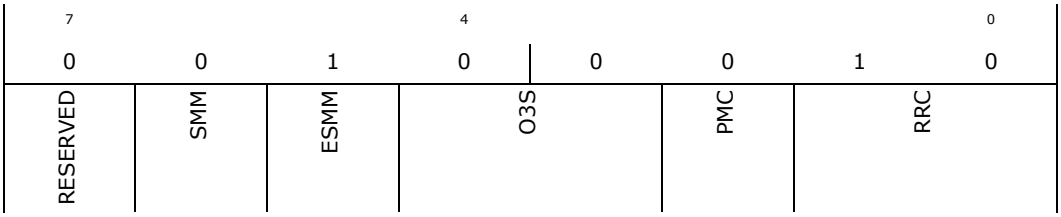
Master Operational Control Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

MOCW3: 28h

Default: 22h



Bit Range	Default & Access	Description
7	0b RO	**RESERVED:** Reserved. Must be 0.
6	0b WO	**SMM:** Special Mask Mode (SMM): If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.

Bit Range	Default & Access	Description
5	1b WO	**ESMM:** Enable Special Mask Mode (ESMM): When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a don't care.
4:3	X WO	**O3S:** OCW3 Select (O3S): When selecting OCW3, bits 4:3 = 01
2	X WO	**PMC:** Poll Mode Command (PMC): When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	10b WO	**RRC:** Register Read Command (RRC): These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be read IRR. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

3.71.6 MICW4—Offset 29h

Master Initialization Command Word 4

Access Method

Type: I/O Register
(Size: 8 bits)

MICW4: 29h

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
MBZ			SFNM	BUF	MSBM	AEOI	MM

Bit Range	Default & Access	Description
7:5	X WO	**MBZ:** These bits must be programmed to zero.
4	0b WO	**SFNM:** Special Fully Nested Mode (SFNM): Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0b WO	**BUF:** Buffered Mode (BUF): Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0b WO	**MSBM:** Master/Slave in Buffered Mode (MSBM): Not used. Should always be programmed to 0.
1	0b WO	**AEOI:** Automatic End of Interrupt (AEOI): This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.

Bit Range	Default & Access	Description
0	1b WO	**MM:** Microprocessor Mode (MM): This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.

3.71.7 MOCW1—Offset 2Dh

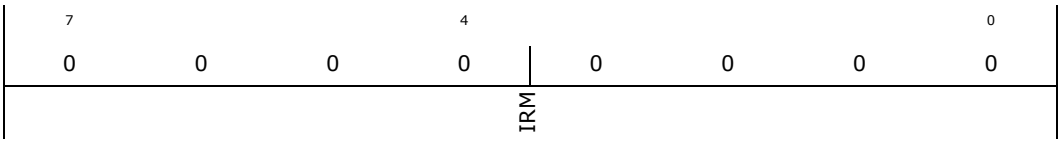
Master Operational Control Word 1 (Interrupt Mask)

Access Method

Type: I/O Register (Size: 8 bits)

MOCW1: 2Dh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**IRM:** Interrupt Request Mask (IRM): When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

3.71.8 SICW1—Offset A0h

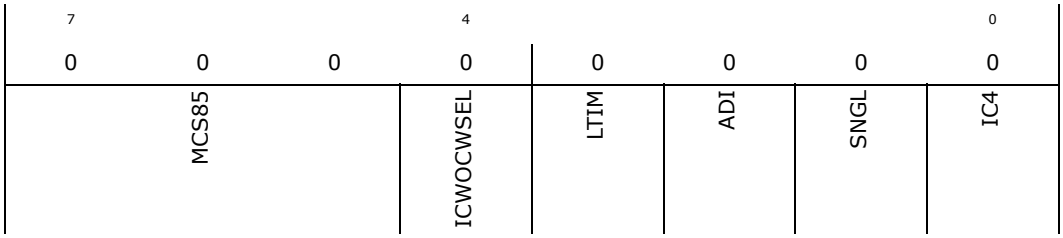
Slave Initialization Command Word 1.A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs: * The Interrupt Mask register is cleared. * IRQ7 input is assigned priority 7. * The slave mode address is set to 7. * Special Mask Mode is cleared and Status Read is set to IRR. Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: I/O Register (Size: 8 bits)

SICW1: A0h

Default: 00h



7			4				0
0	0	0	0	0	0	0	0
MCS85			ICWOCWSEL	LTIM	ADI	SNGL	IC4

Bit Range	Default & Access	Description
7:5	X WO	**MCS85:** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	X WO	**ICWOCWSEL:** ICW/OCW select: This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	X WO	**LTIM:** Edge/Level Bank Select (LTIM): Disabled. Replaced by ELCR1 and ELCR2.
2	X WO	**ADI:** ADI. Ignored for VLV. Should be programmed to 0.
1	X WO	**SNGL:** Single or Cascade (SNGL): Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	X WO	**IC4:** wICW4 Write Required (IC4): This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

3.71.9 SICW2—Offset A1h

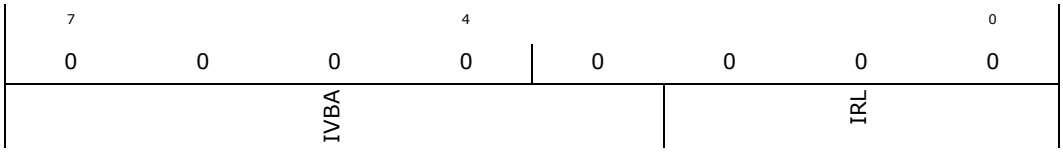
Slave ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: I/O Register
(Size: 8 bits)

SICW2: A1h

Default: 00h



7			4				0
0	0	0	0	0	0	0	0
IVBA					IRL		

Bit Range	Default & Access	Description
7:3	X WO	**IVBA:** Interrupt Vector Base Address: Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.

Bit Range	Default & Access	Description
2:0	X WO	**IRL:** Interrupt Request Level: When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

3.71.10 SOCW2—Offset A4h

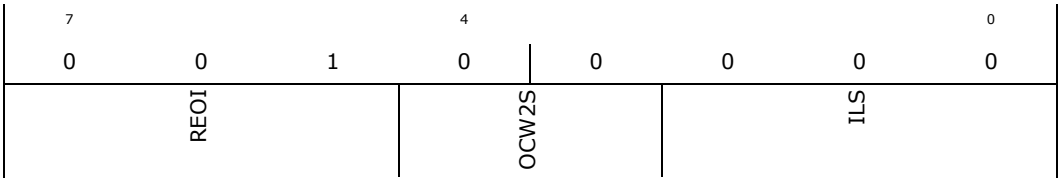
Slave Operational Control Word 2 (Interrupt Mask).Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: I/O Register
(Size: 8 bits)

SOCW2: A4h

Default: 20h



Bit Range	Default & Access	Description
7:5	001b WO	**REOI:** Rotate and EOI Codes: R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 - Rotate in Auto EOI Mode (Clear) 001 - Non-specific EOI command 010 - No Operation 011 - *Specific EOI Command 100 - Rotate in Auto EOI Mode (Set) 101 - Rotate on Non-Specific EOI Command 110 - *Set Priority Command 111 - *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	X WO	**OCW2S:** OCW2 Select: When selecting OCW2, bits 4:3 = 00
2:0	X WO	**ILS:** Interrupt Level Select (L2, L1, L0): L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. Bits Interrupt Level Bits Interrupt Level 000 IRQ0/8 100 IRQ4/12 001 IRQ1/9 101 IRQ5/13 010 IRQ2/10 110 IRQ6/14 011 IRQ3/11 111 IRQ7/15

3.71.11 SICW3—Offset A5h

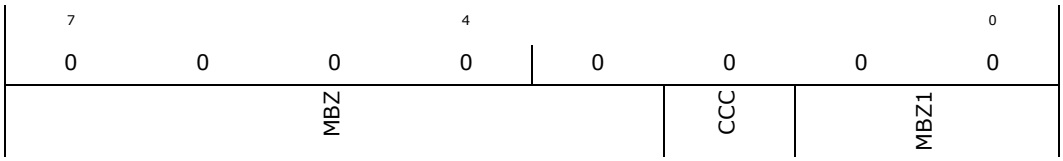
Slave Initialization Command Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

SICW3: A5h

Default: 00h



Bit Range	Default & Access	Description
7:3	X WO	**MBZ:** These bits must be programmed to zero.
2	X WO	**CCC:** Cascaded Controller Connection (CCC): This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 15 is cascaded on IRQ2.
1:0	X WO	**MBZ (MBZ1):** These bits must be programmed to zero.

3.71.12 SOCW3—Offset A8h

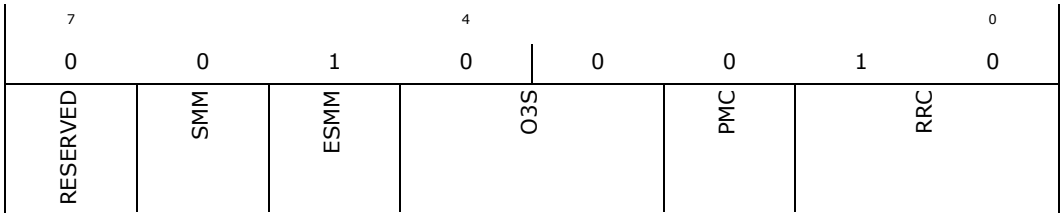
Slave Operational Control Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

SOCW3: A8h

Default: 22h



Bit Range	Default & Access	Description
7	0b RO	**RESERVED:** Reserved. Must be 0.
6	0b WO	**SMM:** Special Mask Mode (SMM): If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.

Bit Range	Default & Access	Description
5	1b WO	**ESMM:** Enable Special Mask Mode (ESMM): When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a don't care.
4:3	X WO	**O3S:** OCW3 Select (O3S): When selecting OCW3, bits 4:3 = 01
2	X WO	**PMC:** Poll Mode Command (PMC): When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	10b WO	**RRC:** Register Read Command (RRC): These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be read IRR. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

3.71.13 SICW4—Offset A9h

Slave Initialization Command Word 4

Access Method

Type: I/O Register
(Size: 8 bits)

SICW4: A9h

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
MBZ			SFNM	BUF	MSBM	AEOI	MM

Bit Range	Default & Access	Description
7:5	X WO	**MBZ:** These bits must be programmed to zero.
4	0b WO	**SFNM:** Special Fully Nested Mode (SFNM): Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0b WO	**BUF:** Buffered Mode (BUF): Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0b WO	**MSBM:** Master/Slave in Buffered Mode (MSBM): Not used. Should always be programmed to 0.
1	0b WO	**AEOI:** Automatic End of Interrupt (AEOI): This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.

Bit Range	Default & Access	Description
0	1b WO	**MM:** Microprocessor Mode (MM): This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.

3.71.14 SOCW1—Offset ADh

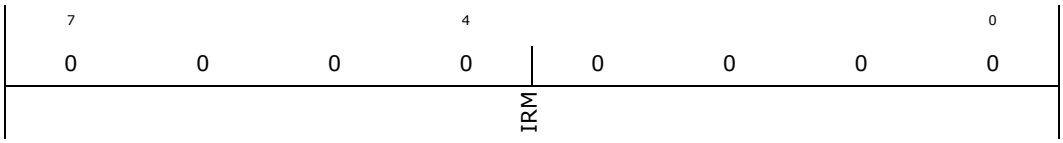
Slave Operational Control Word 1 (Interrupt Mask)

Access Method

Type: I/O Register
(Size: 8 bits)

SOCW1: ADh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**IRM:** Interrupt Request Mask (IRM): When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

3.71.15 ELCR1—Offset 4D0h

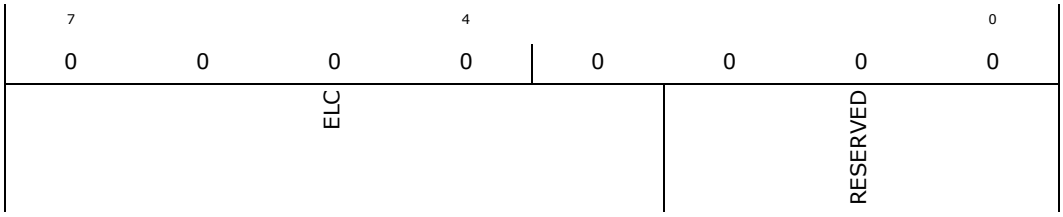
Master Edge/Level Control

Access Method

Type: I/O Register
(Size: 8 bits)

ELCR1: 4D0h

Default: 00h



Bit Range	Default & Access	Description
7:3	X RW	**ELC:** Edge Level Control (ECL[7:3]): In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	0b RO	**RESERVED:** Reserved.

3.71.16 ELCR2—Offset 4D1h

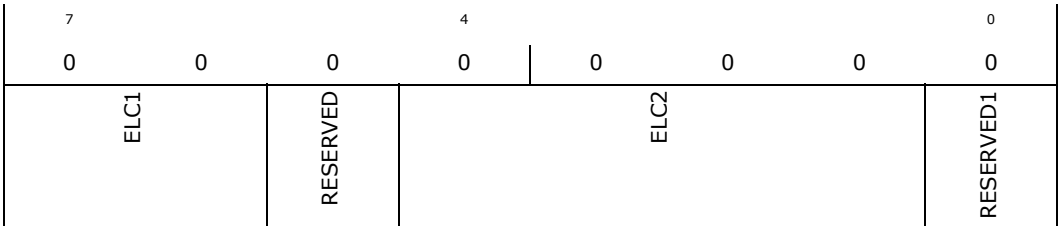
Slave Edge/Level Control

Access Method

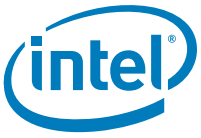
Type: I/O Register
(Size: 8 bits)

ELCR2: 4D1h

Default: 00h



Bit Range	Default & Access	Description
7:6	X RW	**ELC1:** Edge Level Control (ECL[15:14]): In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0b RO	**RESERVED:** Reserved.
4:1	X RW	**ELC2:** Edge Level Control (ECL[12:9]: In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	0b RO	**RESERVED (RESERVED1):** Reserved.



3.72 USB 3.0 Device PCI Configuration Registers

Table 80. Summary of USB 3.0 Device PCI Configuration Registers—0/22/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 4026	00000000h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 4027	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 4028	00000000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 4028	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 4029	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 4030	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 4030	00000000h
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4031	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 4032	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 4032	00000100h
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 4033	48030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 4033	00000008h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 4034	00000000h

3.72.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

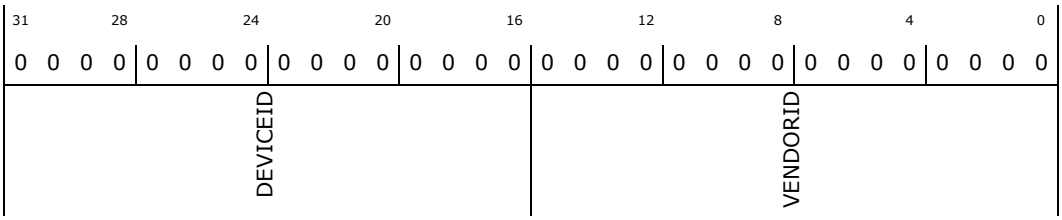
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:22, F:0] + 0h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**DEVICEID:** Reserved.

Bit Range	Default & Access	Description
15:0	0000h RO	**VENDORID:** Reserved.

3.72.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

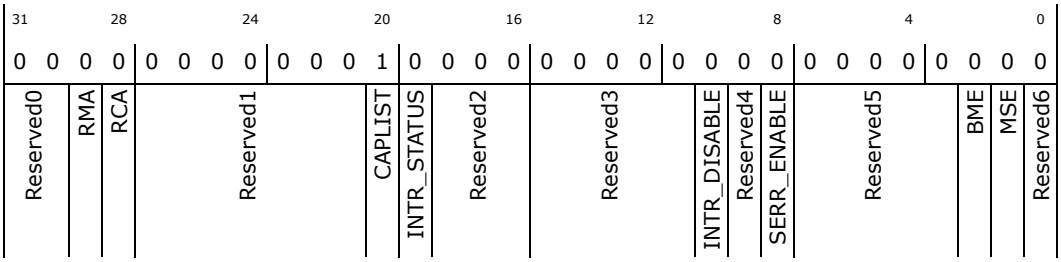
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

STATUSCOMMAND: [B:0, D:22, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** Reserved.
29	0h RW/1C	**RMA:** Reserved.
28	0h RW/1C	**RCA:** Reserved.
27:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**CAPLIST:** Reserved.
19	0h RO	**INTR_STATUS:** Reserved.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**INTR_DISABLE:** Reserved.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR_ENABLE:** Reserved.

Bit Range	Default & Access	Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**BME:** Reserved.
1	0h RW	**MSE:** Reserved.
0	0h RO	**Reserved6:** Reserved.

3.72.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

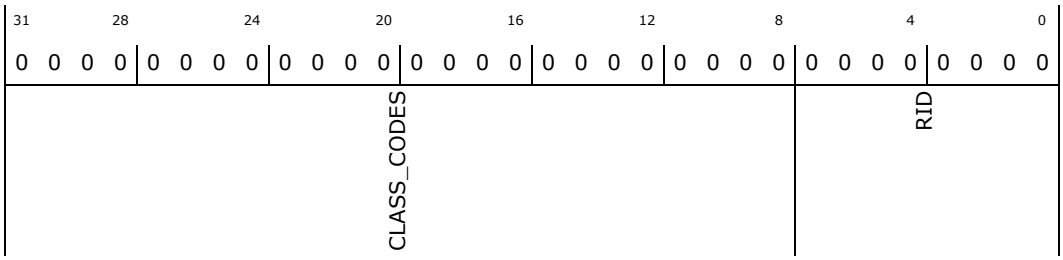
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:22, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**CLASS_CODES:** Reserved.
7:0	00h RO	**RID:** Reserved.

3.72.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

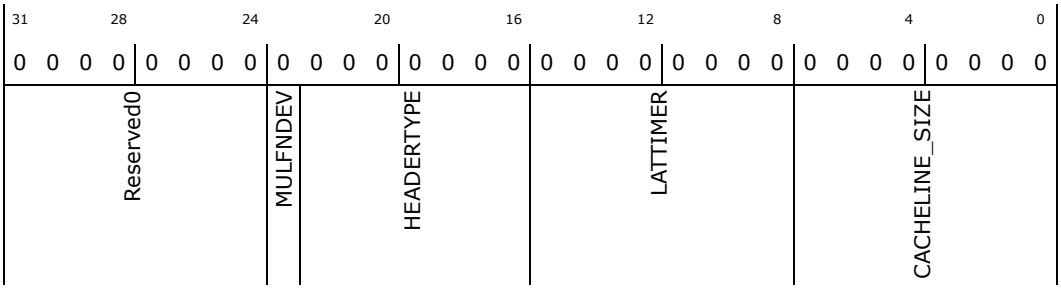
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:22, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	0h RO	**MULFNDEV:** Reserved.
22:16	00h RO	**HEADERTYPE:** Reserved.
15:8	00h RO	**LATTIMER:** Reserved.
7:0	00h RW	**CACHELINE_SIZE:** Reserved.

3.72.5 reg_BAR_type (BAR)—Offset 10h

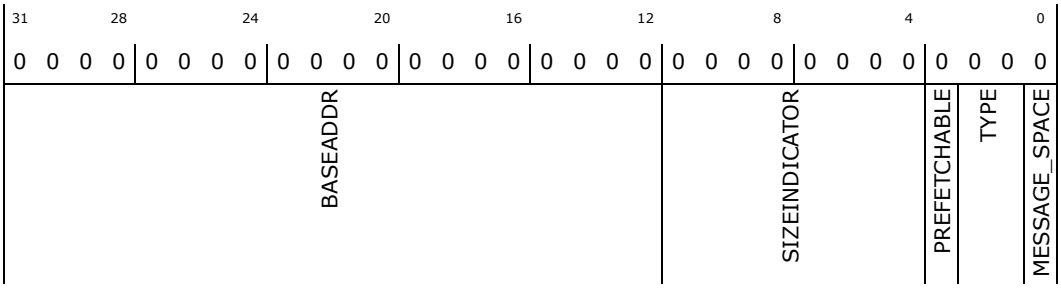
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Reserved.
11:4	00h RO	**SIZEINDICATOR:** Reserved.

Bit Range	Default & Access	Description
3	0h RO	**PREFETCHABLE:** Reserved.
2:1	0h RO	**TYPE:** Reserved.
0	0h RO	**MESSAGE_SPACE:** Reserved.

3.72.6 reg_BAR1_type (BAR1)—Offset 14h

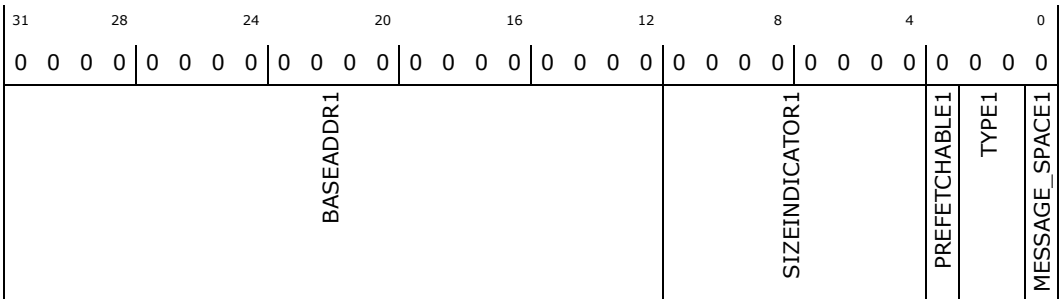
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:22, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** Reserved.
11:4	00h RO	**SIZEINDICATOR1:** Reserved.
3	0h RO	**PREFETCHABLE1:** Reserved.
2:1	0h RO	**TYPE1:** Reserved.
0	0h RO	**MESSAGE_SPACE1:** Reserved.

3.72.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

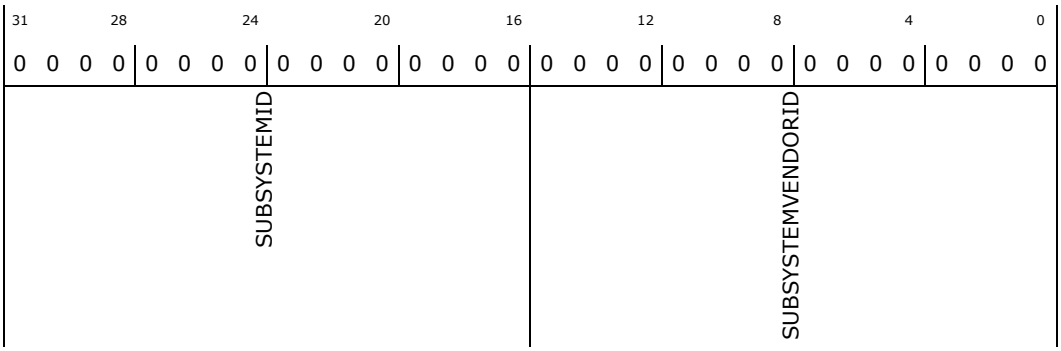
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:22, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Reserved.
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Reserved.

3.72.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

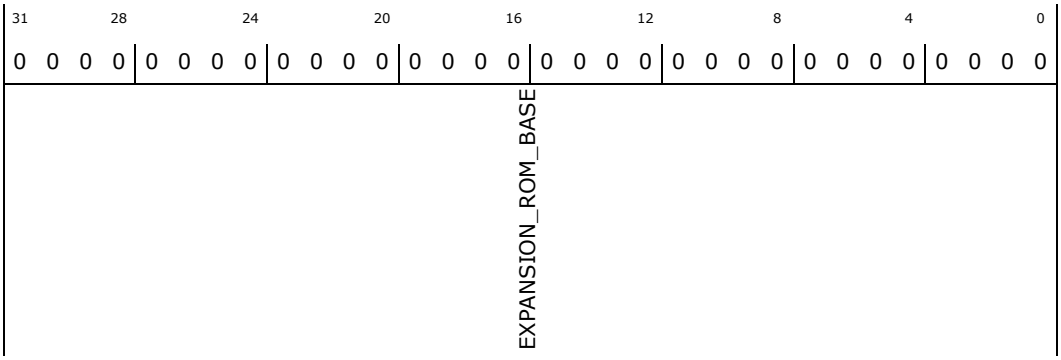
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:22, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

3.72.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

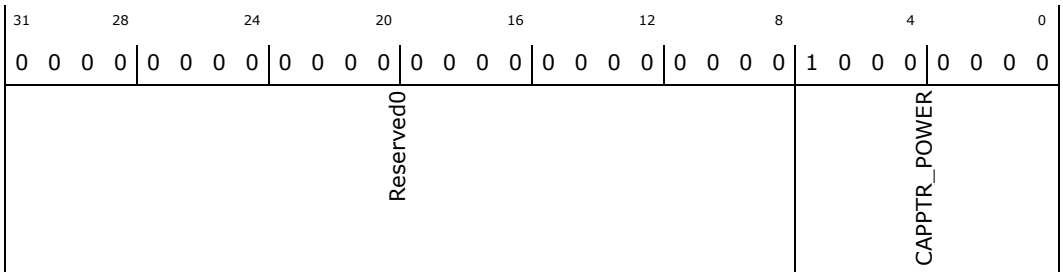
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:22, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	80h RO	**CAPPTR_POWER:** Reserved.

3.72.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

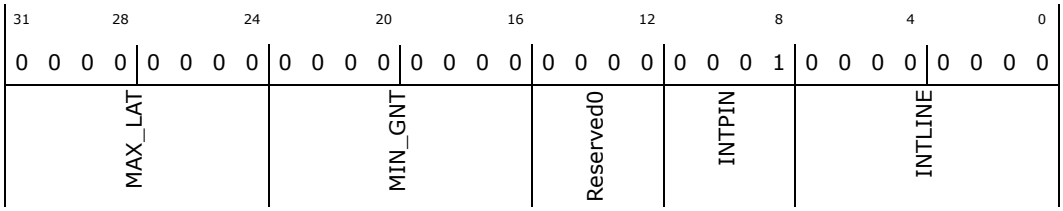
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:22, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Reserved.
23:16	00h RO	**MIN_GNT:** Reserved.
15:12	0h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Description
11:8	1h RO	**INTPIN:** Reserved.
7:0	00h RW	**INTLINE:** Reserved.

3.72.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

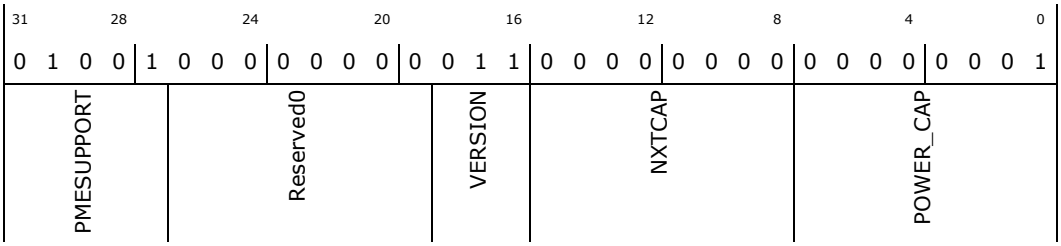
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:22, F:0] + 80h

Default: 48030001h



Bit Range	Default & Access	Description
31:27	09h RO	**PMESUPPORT:** Reserved.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**VERSION:** Reserved.
15:8	00h RO	**NXTCAP:** Reserved.
7:0	01h RO	**POWER_CAP:** Reserved.

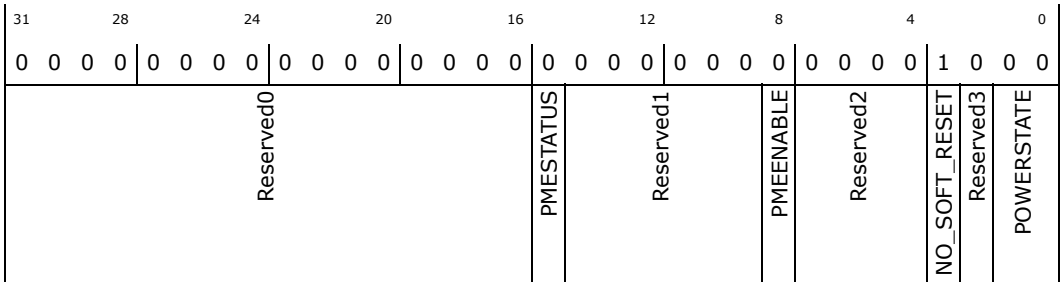
3.72.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:22, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PMESTATUS:** Reserved.
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PMEENABLE:** Reserved.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**NO_SOFT_RESET:** Reserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**POWERSTATE:** Reserved.

3.72.13 reg_MANID_type (MANID)—Offset F8h

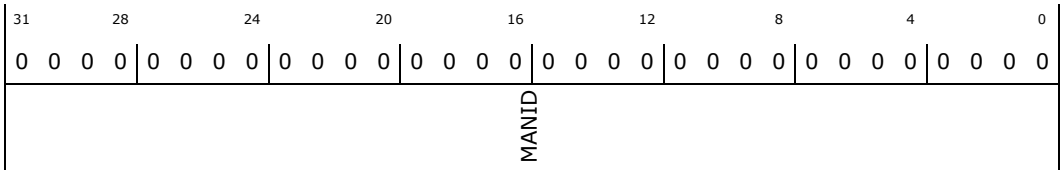
Manufacturers ID

Access Method

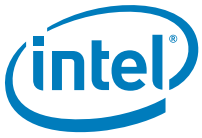
Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:22, F:0] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**MANID:** Reserved.



3.73 USB 3.0 Device Memory Mapped I/O Registers

Table 81. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
8h	2	"APBFC_ILDOA0—Offset 8h" on page 4035	0000h
Ch	2	"APBFC_ILDOACLK0—Offset Ch" on page 4036	0000h
10h	2	"APBFC_ILDOS0—Offset 10h" on page 4037	0000h
14h	2	"APBFC_IPMA0—Offset 14h" on page 4038	0000h
18h	2	"APBFC_IPMA1—Offset 18h" on page 4040	0000h
1Ch	2	"APBFC_OPMA0—Offset 1Ch" on page 4041	0000h
20h	2	"APBFC_IPIPE0—Offset 20h" on page 4042	0000h
24h	2	"APBFC_IPIPE1A—Offset 24h" on page 4043	0000h
28h	2	"APBFC_IPIPE1B—Offset 28h" on page 4044	0000h
2Ch	2	"APBFC_IPIPE1C—Offset 2Ch" on page 4044	0000h
30h	2	"APBFC_IPIPE2—Offset 30h" on page 4045	0000h
34h	2	"APBFC_IPIPE3—Offset 34h" on page 4046	0000h
38h	2	"APBFC_OPIPE0—Offset 38h" on page 4047	0000h
3Ch	2	"APBFC_OPIPE1A—Offset 3Ch" on page 4048	0000h
40h	2	"APBFC_OPIPE1B—Offset 40h" on page 4049	0000h
44h	2	"APBFC_OPIPE1C—Offset 44h" on page 4049	0000h
48h	2	"APBFC_OPIPE2—Offset 48h" on page 4050	0000h
4Ch	2	"APBFC_OTG3_MISC0—Offset 4Ch" on page 4051	000Bh
50h	2	"APBFC_OTG3_MISC1—Offset 50h" on page 4052	0000h
54h	2	"APBFC_OTG3_MISC2—Offset 54h" on page 4052	1100h
58h	2	"APBFC_OTG3_MISC3—Offset 58h" on page 4053	7008h
5Ch	2	"APBFC_U3PMU_CFG0_REG—Offset 5Ch" on page 4054	0000h
60h	2	"APBFC_U3PMU_CFG1_REG—Offset 60h" on page 4054	0000h

3.73.1 APBFC_ILDOA0—Offset 8h

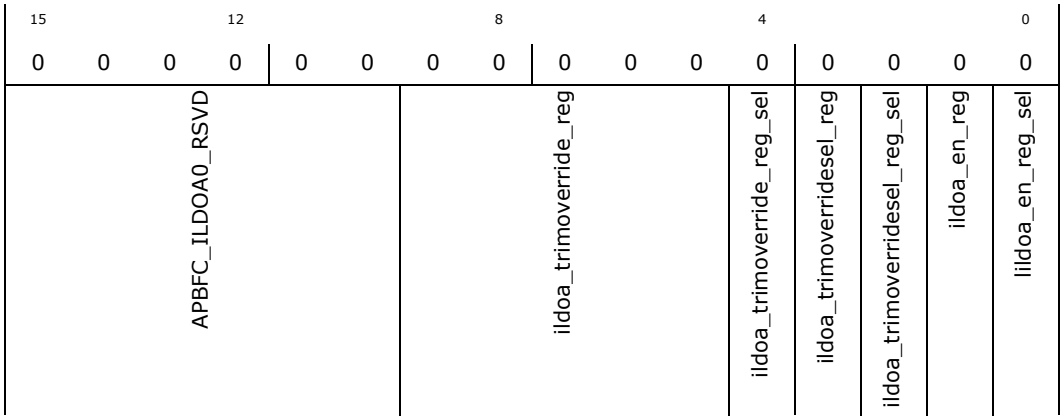
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_ILDOA0: [BAR + 10F800h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:10	0h RW	**APBFC_ILDOA0_RSVD:** Reserved.
9:5	0h RW	**ildoa_trimoverride_reg:** Reserved.
4	0b RW	**ildoa_trimoverride_reg_sel:** Reserved.
3	0b RW	**ildoa_en_reg (ildoa_trimoverridesel_reg):** Reserved.
2	0b RW	**ildoa_trimoverridesel_reg_sel:** Reserved.
1	0b RW	**ildoa_en_reg:** Reserved.
0	0b RW	**lildoa_en_reg_sel:** Reserved.

3.73.2 APBFC_ILDOACLK0—Offset Ch

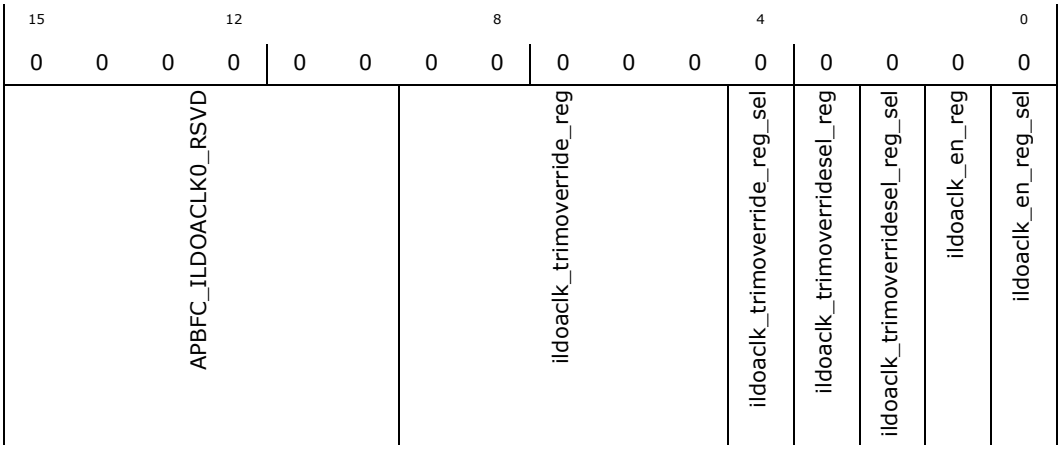
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_ILDOACLK0: [BAR + 10F800h] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:10	0h RW	**APBFC_ILDOACLK0_RSVD:** Reserved.
9:5	0h RW	**ildoaclk_trimoverride_reg:** Reserved.
4	0b RW	**ildoaclk_trimoverride_reg_sel:** Reserved.
3	0b RW	**ildoaclk_trimoverridesel_reg:** Reserved.
2	0b RW	**ildoaclk_trimoverridesel_reg_sel:** Reserved.
1	0b RW	**ildoaclk_en_reg:** Reserved.
0	0b RW	**ildoaclk_en_reg_sel:** Reserved.

3.73.3 APBFC_ILDOS0—Offset 10h

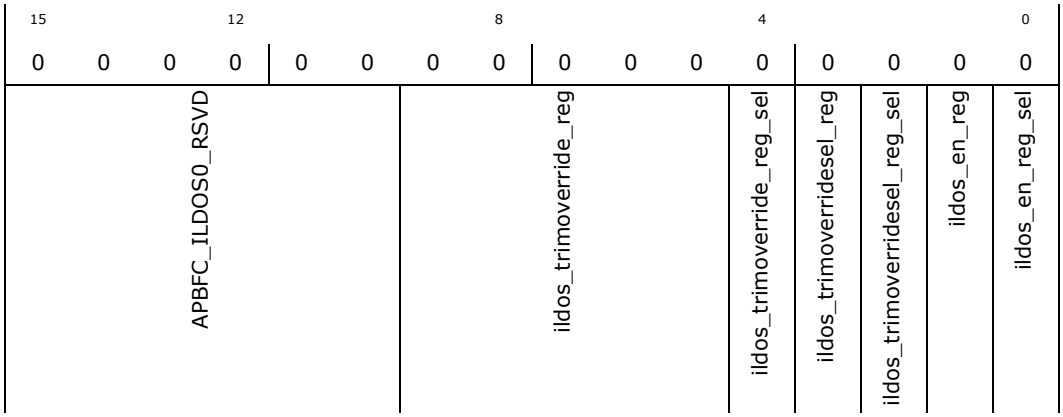
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_ILDOS0: [BAR + 10F800h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:10	0h RW	**APBFC_ILDOS0_RSVD:** Reserved.
9:5	0h RW	**ildos_trimoverride_reg:** Reserved.
4	0b RW	**ildos_trimoverride_reg_sel:** Reserved.
3	0b RW	**ildos_trimoverridesel_reg:** Reserved.
2	0b RW	**ildos_trimoverridesel_reg_sel:** Reserved.
1	0b RW	**ildos_en_reg:** Reserved.
0	0b RW	**ildos_en_reg_sel:** Reserved.

3.73.4 APBFC_IPMA0—Offset 14h

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_IPMA0: [BAR + 10F800h] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IPMA_CMN_REFCLK_RCV_EN_REG	IPMA_CMN_REFCLK_RCV_EN_REG_SEL	IPMA_CMN_REFCLK_INT_SEL_REG	IPMA_CMN_REFCLK_INT_SEL_REG_SEL	IPMA_CMN_REFCLK_INT_B_REG	IPMA_CMN_REFCLK_INT_B_REG_SEL	IPMA_CMN_REFCLK_INT_REG	IPMA_CMN_REFCLK_INT_REG_SEL	IPMA_CMN_REFCLK_DISABLE_REG	IPMA_CMN_REFCLK_DISABLE_REG_SEL	IPMA_CMN_REFCLK_ALL_SEL_REG	IPMA_CMN_REFCLK_ALL_SEL_REG_SEL	IPMA_CMN_MACRO_EN_REG	IPMA_CMN_MACRO_EN_REG_SEL	IPMA_CMN_ANA_DISABLE_REG	IPMA_CMN_ANA_DISABLE_REG_SEL

Bit Range	Default & Access	Description
15	0b RW	**IPMA_CMN_REFCLK_RCV_EN_REG:** Reserved.
14	0b RW	**IPMA_CMN_REFCLK_RCV_EN_REG_SEL:** Reserved.
13	0b RW	**IPMA_CMN_REFCLK_INT_SEL_REG:** Reserved.
12	0b RW	**IPMA_CMN_REFCLK_INT_SEL_REG_SEL:** Reserved.
11	0b RW	**IPMA_CMN_REFCLK_INT_B_REG:** Reserved.
10	0b RW	**IPMA_CMN_REFCLK_INT_B_REG_SEL:** Reserved.
9	0b RW	**IPMA_CMN_REFCLK_INT_REG:** Reserved.
8	0b RW	**IPMA_CMN_REFCLK_INT_REG_SEL:** Reserved.
7	0b RW	**IPMA_CMN_REFCLK_DISABLE_REG:** Reserved.
6	0b RW	**IPMA_CMN_REFCLK_DISABLE_REG_SEL:** Reserved.
5	0b RW	**IPMA_CMN_REFCLK_ALL_SEL_REG:** Reserved.
4	0b RW	**IPMA_CMN_REFCLK_ALL_SEL_REG_SEL:** Reserved.
3	0b RW	**IPMA_CMN_MACRO_EN_REG:** Reserved.
2	0b RW	**IPMA_CMN_MACRO_EN_REG_SEL:** Reserved.

Bit Range	Default & Access	Description
1	0b RW	**IPMA_CMN_ANA_DISABLE_REG:** Reserved.
0	0b RW	**IPMA_CMN_ANA_DISABLE_REG_SEL:** Reserved.

3.73.5 APBFC_IPMA1—Offset 18h

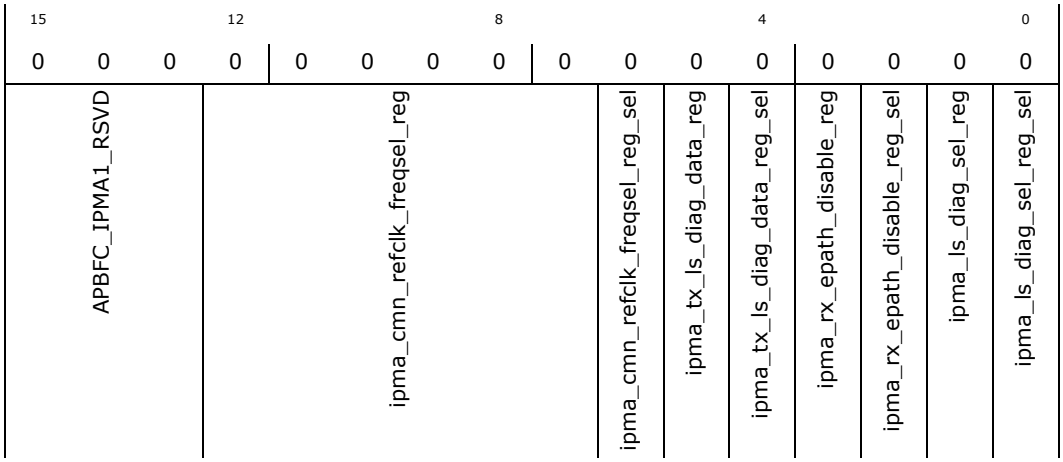
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_IPMA1: [BAR + 10F800h] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:13	0h RO	**APBFC_IPMA1_RSVD:** Reserved.
12:7	0h RW	**ipma_cmn_refclk_freqsel_reg:** Reserved.
6	0b RW	**ipma_cmn_refclk_freqsel_reg_sel:** Reserved.
5	0b RW	**ipma_tx_ls_diag_data_reg:** Reserved.
4	0b RW	**ipma_tx_ls_diag_data_reg_sel:** Reserved.
3	0b RW	**ipma_rx_epath_disable_reg:** Reserved.
2	0b RW	**ipma_rx_epath_disable_reg_sel:** Reserved.

Bit Range	Default & Access	Description
1	0b RW	**ipma_ls_diag_sel_reg:** Reserved.
0	0b RW	**ipma_ls_diag_sel_reg_sel:** Reserved.

3.73.6 APBFC_OPMA0—Offset 1Ch

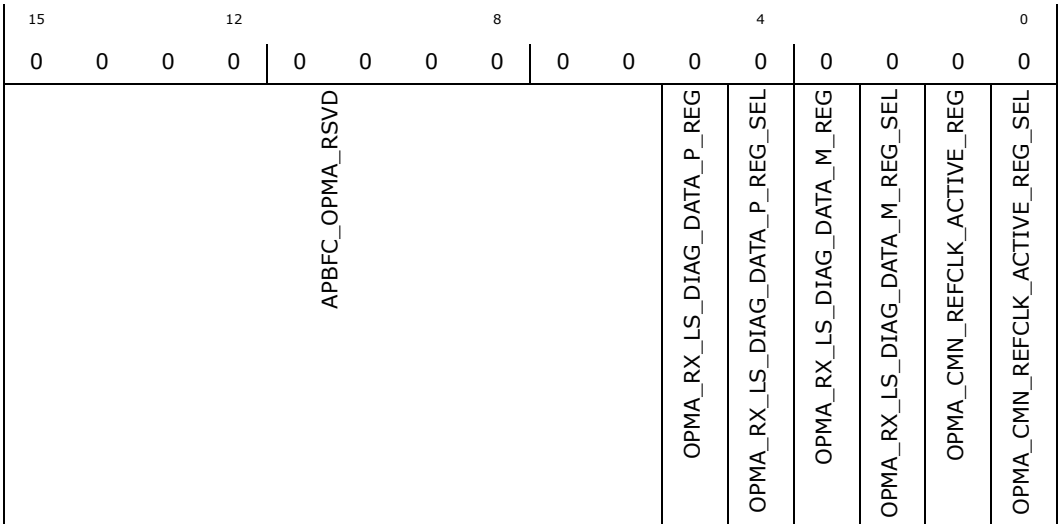
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_OPMA0: [BAR + 10F800h] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:6	0h RW	**APBFC_OPMA_RSVD:** Reserved.
5	0b RW	**OPMA_RX_LS_DIAG_DATA_P_REG:** Reserved.
4	0b RW	**OPMA_RX_LS_DIAG_DATA_P_REG_SEL:** Reserved.
3	0b RW	**OPMA_RX_LS_DIAG_DATA_M_REG:** Reserved.
2	0b RW	**OPMA_RX_LS_DIAG_DATA_M_REG_SEL:** Reserved.
1	0b RW	**OPMA_CMN_REFCLK_ACTIVE_REG:** Reserved.

Bit Range	Default & Access	Description
0	0b RW	**OPMA_CMN_REFCLK_ACTIVE_REG_SEL:** Reserved.

3.73.7 APBFC_IPIPE0—Offset 20h

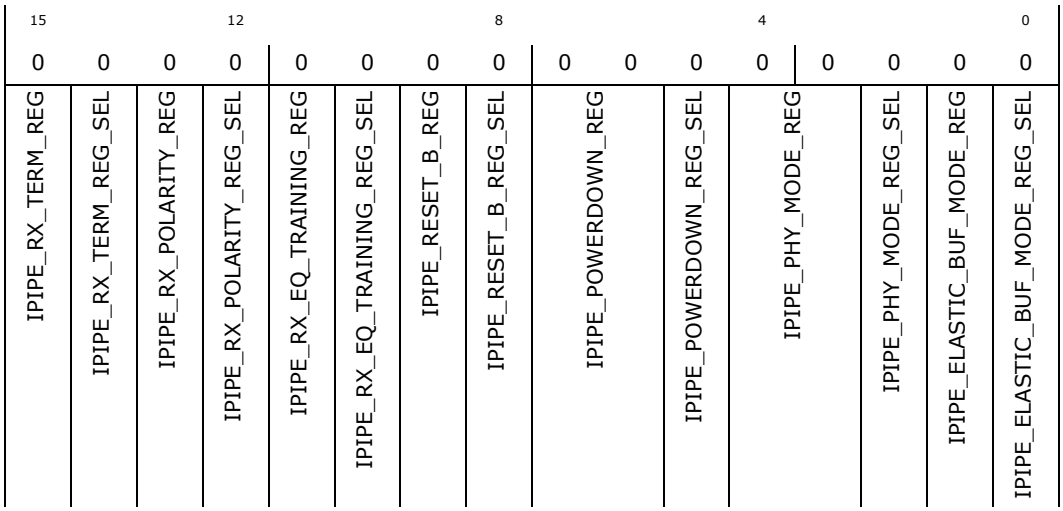
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_IPIPE0: [BAR + 10F800h] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**IPIPE_RX_TERM_REG:** Reserved.
14	0b RW	**IPIPE_RX_TERM_REG_SEL:** Reserved.
13	0b RW	**IPIPE_RX_POLARITY_REG:** Reserved.
12	0b RW	**IPIPE_RX_POLARITY_REG_SEL:** Reserved.
11	0b RW	**IPIPE_RX_EQ_TRAINING_REG:** Reserved.
10	0b RW	**IPIPE_RX_EQ_TRAINING_REG_SEL:** Reserved.
9	0b RW	**IPIPE_RESET_B_REG:** Reserved.

Bit Range	Default & Access	Description
8	0b RW	**IPIPE_RESET_B_REG_SEL:** Reserved.
7:6	0h RW	**IPIPE_POWERDOWN_REG:** Reserved.
5	0b RW	**IPIPE_POWERDOWN_REG_SEL:** Reserved.
4:3	0h RW	**IPIPE_PHY_MODE_REG:** Reserved.
2	0b RW	**IPIPE_PHY_MODE_REG_SEL:** Reserved.
1	0b RW	**IPIPE_ELASTIC_BUF_MODE_REG:** Reserved.
0	0b RW	**IPIPE_ELASTIC_BUF_MODE_REG_SEL:** Reserved.

3.73.8 APBFC_IPIPE1A—Offset 24h

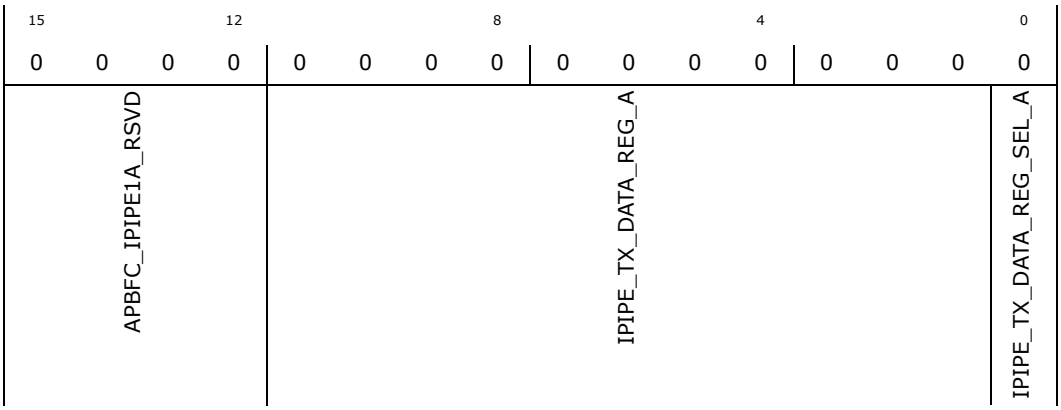
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_IPIPE1A: [BAR + 10F800h] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0h RO	**APBFC_IPIPE1A_RSVD:** Reserved.
11:1	0h RW	**IPIPE_TX_DATA_REG_A:** Reserved.
0	0b RW	**IPIPE_TX_DATA_REG_SEL_A:** Reserved.

3.73.9 APBFC_IPIPE1B—Offset 28h

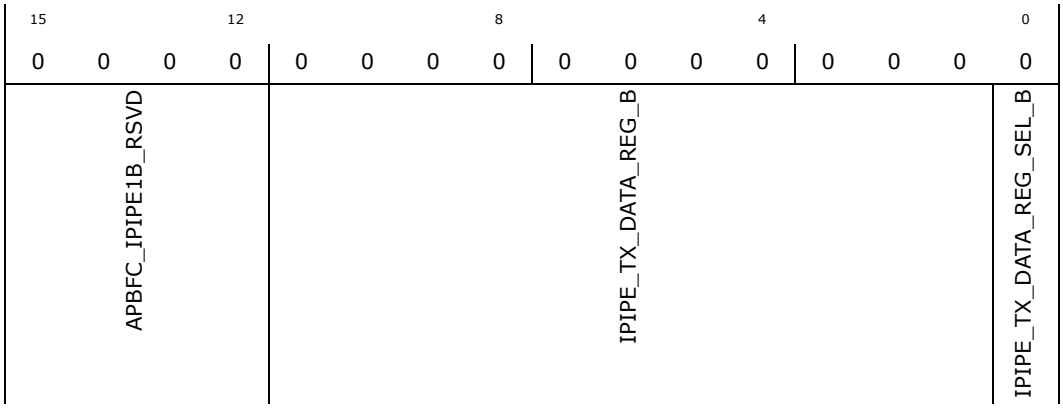
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_IPIPE1B: [BAR + 10F800h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0h RO	**APBFC_IPIPE1B_RSVD:** Reserved.
11:1	0h RW	**IPIPE_TX_DATA_REG_B:** Reserved.
0	0b RW	**IPIPE_TX_DATA_REG_SEL_B:** Reserved.

3.73.10 APBFC_IPIPE1C—Offset 2Ch

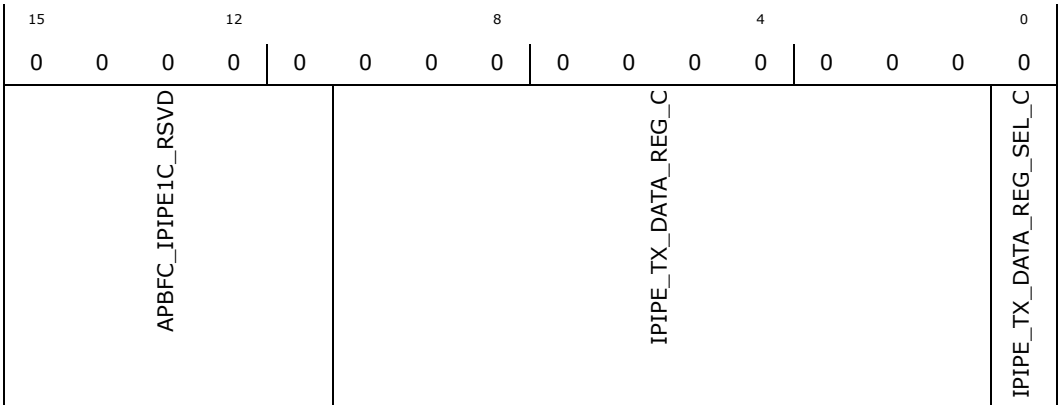
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_IPIPE1C: [BAR + 10F800h] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:11	0h RO	**APBFC_IPIPE1C_RSVD:** Reserved.
10:1	0h RW	**IPIPE_TX_DATA_REG_C:** Reserved.
0	0b RW	**IPIPE_TX_DATA_REG_SEL_C:** Reserved.

3.73.11 APBFC_IPIPE2—Offset 30h

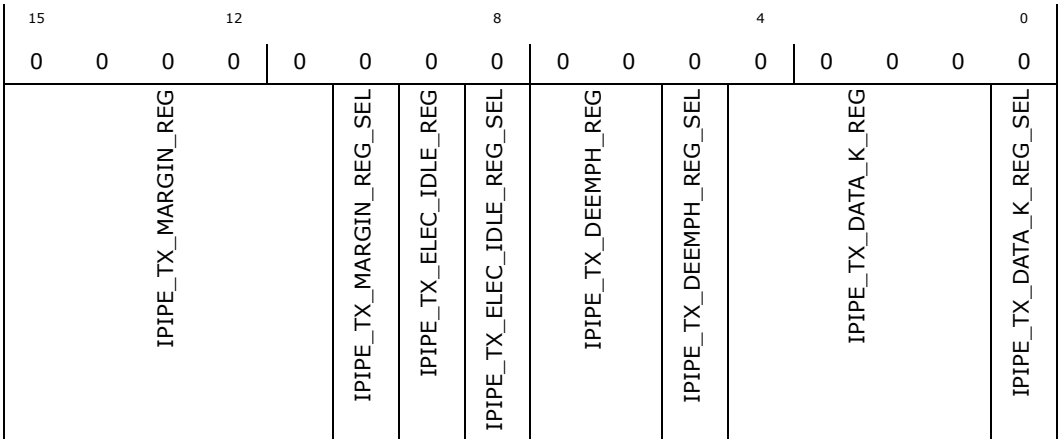
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_IPIPE2: [BAR + 10F800h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:11	0h RW	**IPIPE_TX_MARGIN_REG:** Reserved.
10	0b RW	**IPIPE_TX_MARGIN_REG_SEL:** Reserved.
9	0b RW	**IPIPE_TX_ELEC_IDLE_REG:** Reserved.
8	0b RW	**IPIPE_TX_ELEC_IDLE_REG_SEL:** Reserved.
7:6	0h RW	**IPIPE_TX_DEEMPH_REG:** Reserved.
5	0b RW	**IPIPE_TX_DEEMPH_REG_SEL:** Reserved.
4:1	0h RW	**IPIPE_TX_DATA_K_REG:** Reserved.
0	0b RW	**IPIPE_TX_DATA_K_REG_SEL:** Reserved.

3.73.12 APBFC_IPIPE3—Offset 34h

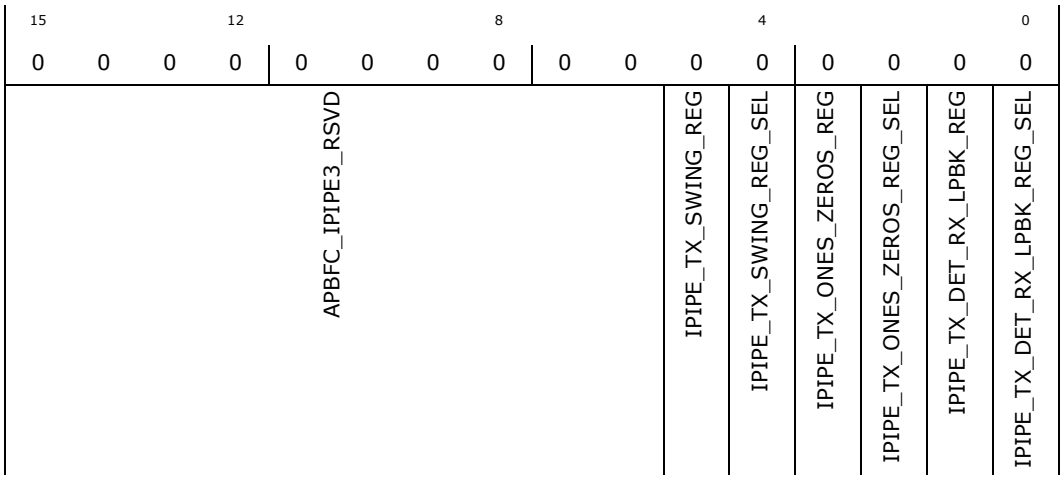
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_IPIPE3: [BAR + 10F800h] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:6	0h RO	**APBFC_IPIPE3_RSVD:** Reserved.

Bit Range	Default & Access	Description
5	0b RW	**IPIPE_TX_SWING_REG:** Reserved.
4	0b RW	**IPIPE_TX_SWING_REG_SEL:** Reserved.
3	0b RW	**IPIPE_TX_ONES_ZEROS_REG:** Reserved.
2	0b RW	**IPIPE_TX_ONES_ZEROS_REG_SEL:** Reserved.
1	0b RW	**IPIPE_TX_DET_RX_LPBK_REG:** Reserved.
0	0b RW	**IPIPE_TX_DET_RX_LPBK_REG_SEL:** Reserved.

3.73.13 APBFC_OPIPE0—Offset 38h

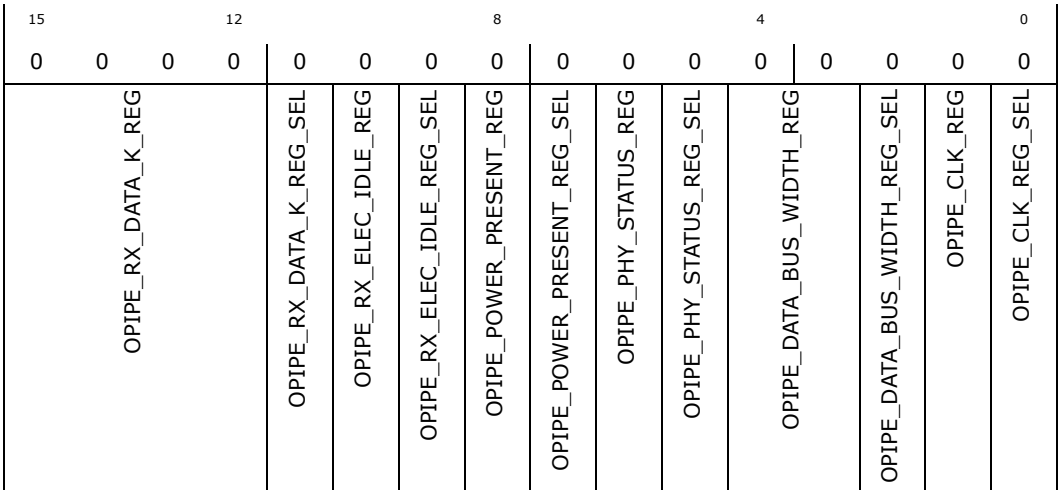
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_OPIPE0: [BAR + 10F800h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0h RW	**OPIPE_RX_DATA_K_REG:** Reserved.
11	0b RW	**OPIPE_RX_DATA_K_REG_SEL:** Reserved.
10	0b RW	**OPIPE_RX_ELEC_IDLE_REG:** Reserved.

Bit Range	Default & Access	Description
9	0b RW	**OPIPE_RX_ELEC_IDLE_REG_SEL:** Reserved.
8	0b RW	**OPIPE_POWER_PRESENT_REG:** Reserved.
7	0b RW	**OPIPE_POWER_PRESENT_REG_SEL:** Reserved.
6	0b RW	**OPIPE_PHY_STATUS_REG:** Reserved.
5	0b RW	**OPIPE_PHY_STATUS_REG_SEL:** Reserved.
4:3	0h RW	**OPIPE_DATA_BUS_WIDTH_REG:** Reserved.
2	0b RW	**OPIPE_DATA_BUS_WIDTH_REG_SEL:** Reserved.
1	0b RW	**OPIPE_CLK_REG:** Reserved.
0	0b RW	**OPIPE_CLK_REG_SEL:** Reserved.

3.73.14 APBFC_OPIPE1A—Offset 3Ch

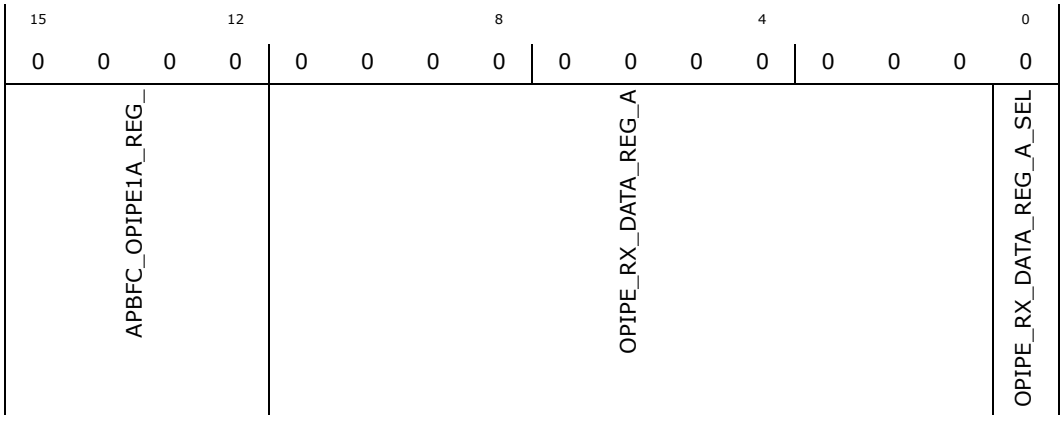
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_OPIPE1A: [BAR + 10F800h] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0h RW	**APBFC_OPIPE1A_REG_:** Reserved.

Bit Range	Default & Access	Description
11:1	0h RW	**OPIPE_RX_DATA_REG_A:** Reserved.
0	0b RW	**OPIPE_RX_DATA_REG_A_SEL:** Reserved.

3.73.15 APBFC_OPIPE1B—Offset 40h

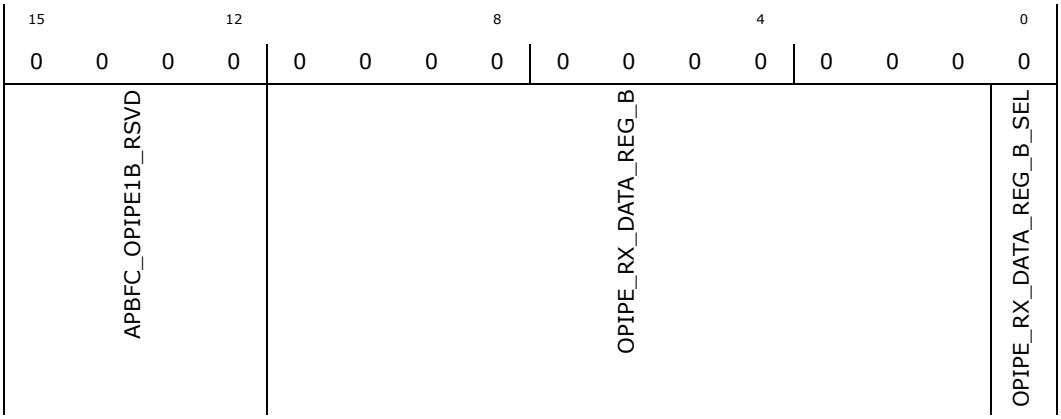
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_OPIPE1B: [BAR + 10F800h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:12	0h RO	**APBFC_OPIPE1B_RSVD:** Reserved.
11:1	0h RW	**OPIPE_RX_DATA_REG_B:** Reserved.
0	0b RW	**OPIPE_RX_DATA_REG_B_SEL:** Reserved.

3.73.16 APBFC_OPIPE1C—Offset 44h

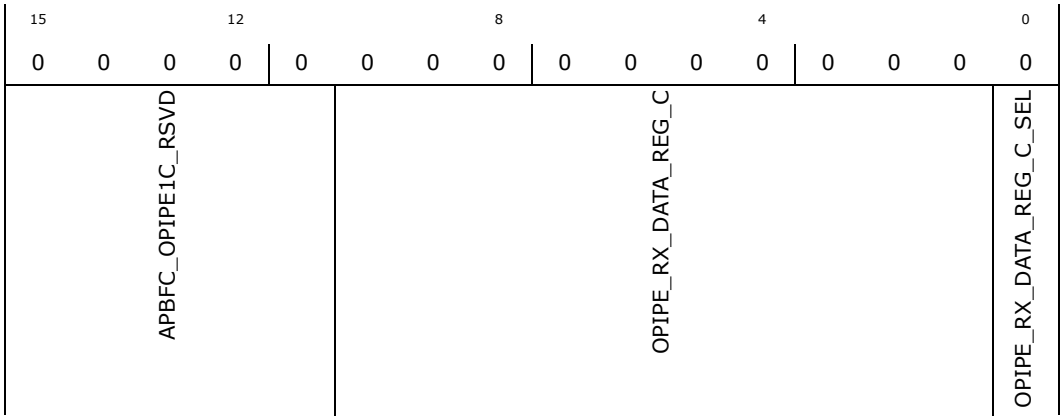
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_OPIPE1C: [BAR + 10F800h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:11	0h RO	**APBFC_OPIPE1C_RSVD:** Reserved.
10:1	0h RW	**OPIPE_RX_DATA_REG_C:** Reserved.
0	0b RW	**OPIPE_RX_DATA_REG_C_SEL:** Reserved.

3.73.17 APBFC_OPIPE2—Offset 48h

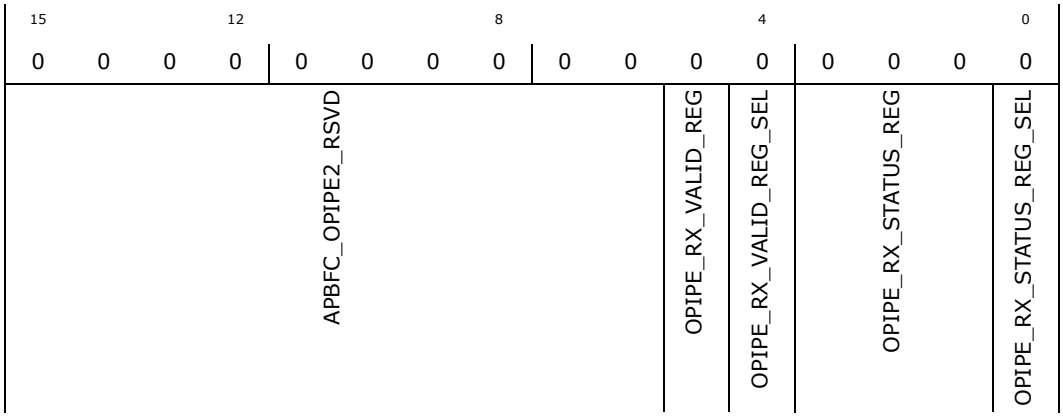
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_OPIPE2: [BAR + 10F800h] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:6	0h RO	**APBFC_OPIPE2_RSVD:** Reserved.
5	0b RW	**OPIPE_RX_VALID_REG:** Reserved.
4	0b RW	**OPIPE_RX_VALID_REG_SEL:** Reserved.
3:1	0h RW	**OPIPE_RX_STATUS_REG:** Reserved.
0	0b RW	**OPIPE_RX_STATUS_REG_SEL:** Reserved.

3.73.18 APBFC_OTG3_MISC0—Offset 4Ch

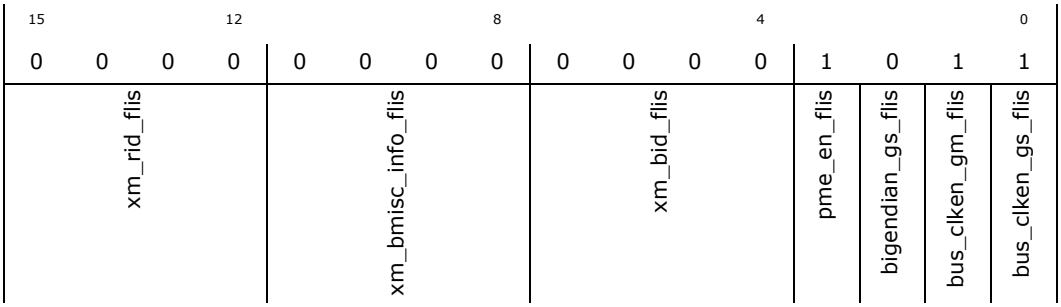
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_OTG3_MISC0: [BAR + 10F800h] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 000Bh



Bit Range	Default & Access	Description
15:12	0b RW	**xm_rid_flis:** Reserved.
11:8	0b RW	**xm_bmisc_info_flis:** Reserved.
7:4	0b RW	**xm_bid_flis:** Reserved.
3	1b RW	**pme_en_flis:** Reserved.
2	0b RW	**bigendian_gs_flis:** Reserved.
1	1b RW	**bus_clken_gm_flis:** Reserved.
0	1b RW	**bus_clken_gs_flis:** Reserved.

3.73.19 APBFC_OTG3_MISC1—Offset 50h

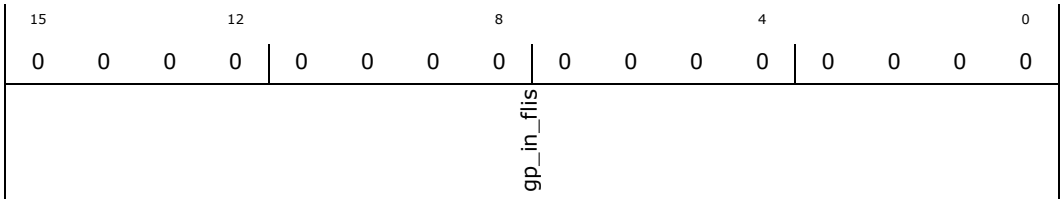
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_OTG3_MISC1: [BAR + 10F800h] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	0b RW	**gp_in_flis:** Reserved.

3.73.20 APBFC_OTG3_MISC2—Offset 54h

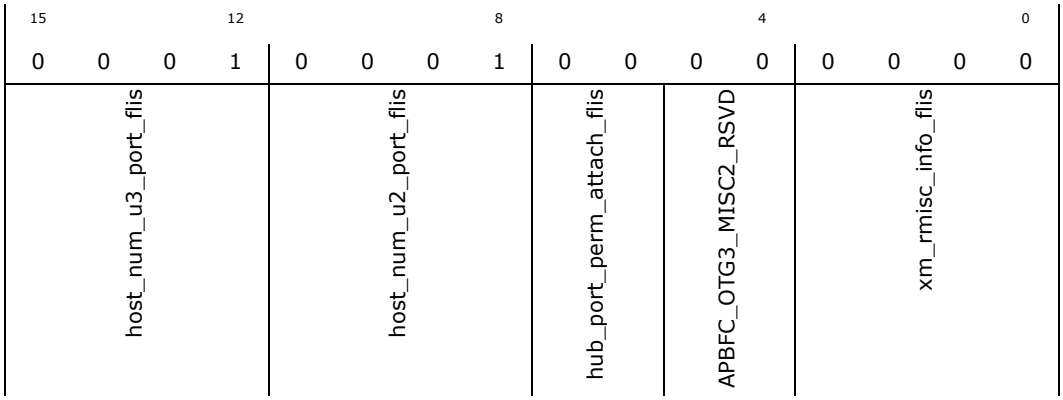
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_OTG3_MISC2: [BAR + 10F800h] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 1100h



Bit Range	Default & Access	Description
15:12	0001b RW	**host_num_u3_port_flis:** Reserved.
11:8	0001b RW	**host_num_u2_port_flis:** Reserved.

Bit Range	Default & Access	Description
7:6	0b RW	**hub_port_perm_attach_flis:** Reserved.
5:4	00b RO	**APBFC_OTG3_MISC2_RSVD:** Reserved.
3:0	0b RW	**xm_rmisc_info_flis:** Reserved.

3.73.21 APBFC_OTG3_MISC3—Offset 58h

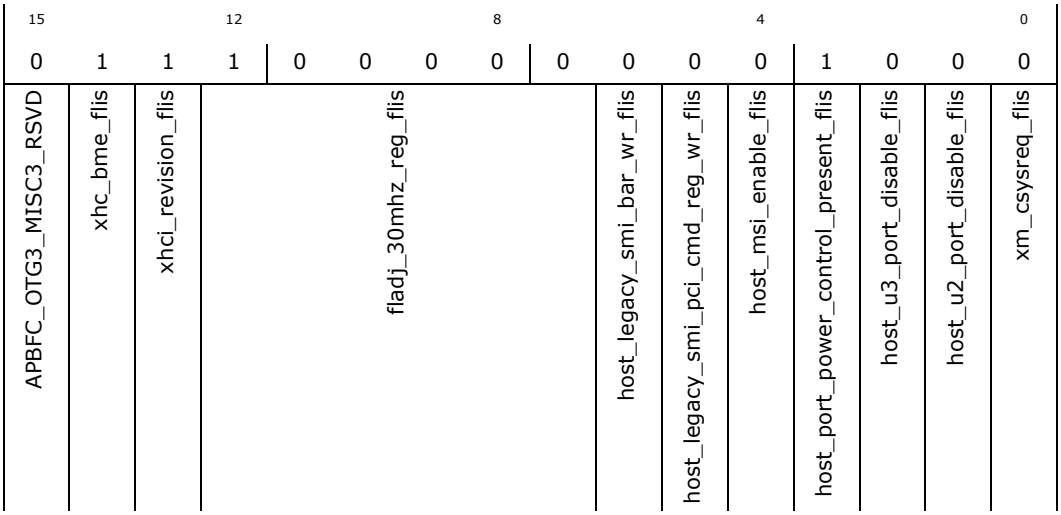
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_OTG3_MISC3: [BAR + 10F800h] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 7008h



Bit Range	Default & Access	Description
15	0b RO	**APBFC_OTG3_MISC3_RSVD:** Reserved.
14	1b RW	**xhc_bme_flis:** Reserved.
13	1b RW	**xhci_revision_flis:** Reserved.
12:7	100000b RW	**fladj_30mhz_reg_flis:** Reserved.
6	0b RW	**host_legacy_smi_bar_wr_flis:** Reserved.

Bit Range	Default & Access	Description
5	0b RW	**host_legacy_smi_pci_cmd_reg_wr_flis:** Reserved.
4	0b RW	**host_msi_enable_flis:** Reserved.
3	1b RW	**host_port_power_control_present_flis:** Reserved.
2	0b RW	**host_u3_port_disable_flis:** Reserved.
1	0b RW	**host_u2_port_disable_flis:** Reserved.
0	0b RW	**xm_csysreq_flis:** Reserved.

3.73.22 APBFC_U3PMU_CFG0_REG—Offset 5Ch

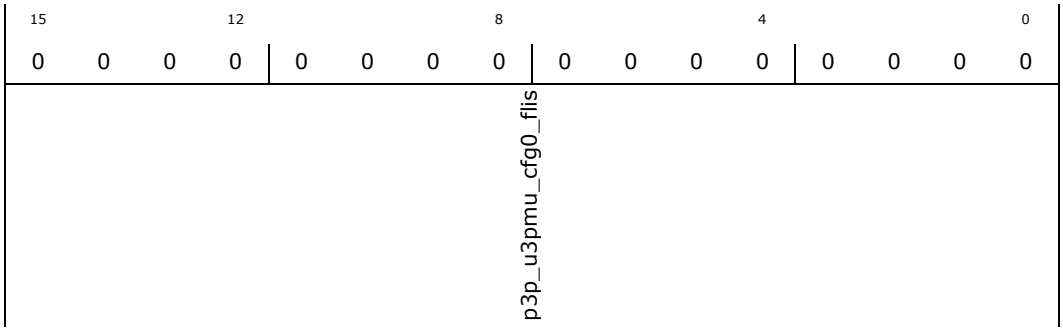
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_U3PMU_CFG0_REG: [BAR + 10F800h] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	0h RW	**p3p_u3pmu_cfg0_flis:** Reserved.

3.73.23 APBFC_U3PMU_CFG1_REG—Offset 60h

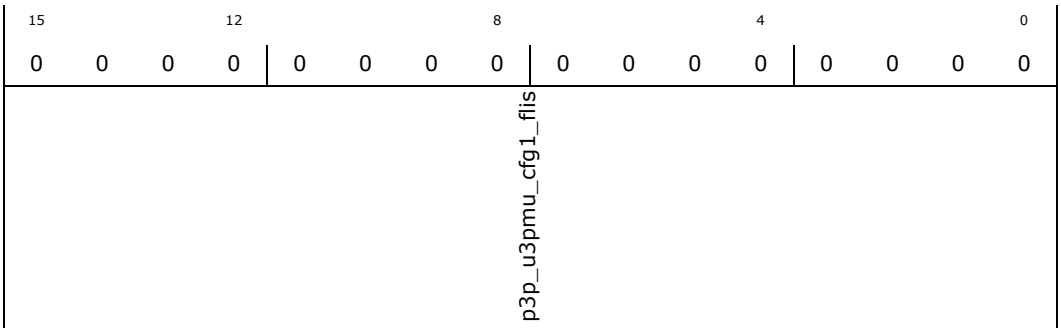
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

APBFC_U3PMU_CFG1_REG: [BAR + 10F800h] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	0h RW	**p3p_u3pmu_cfg1_flis:** Reserved.

3.74 USB 3.0 Device Memory Mapped I/O Registers

Table 82. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"CAPLENGTH—Offset 0h" on page 4063	00960020h
4h	4	"HCSPARAMS1—Offset 4h" on page 4064	0200017Fh
8h	4	"HCSPARAMS2—Offset 8h" on page 4065	140000F1h
Ch	4	"HCSPARAMS3—Offset Ch" on page 4066	07FF000Ah
10h	4	"HCCPARAMS—Offset 10h" on page 4067	0220F04Ch
14h	4	"DBOFF—Offset 14h" on page 4068	00000480h
18h	4	"RTSOFF—Offset 18h" on page 4069	00000440h
1Ch	4	"Rsvd_HC—Offset 1Ch" on page 4070	00000000h
20h	4	"USBCMD—Offset 20h" on page 4070	00000000h
24h	4	"USBSTS—Offset 24h" on page 4072	00000001h
28h	4	"PAGESIZE—Offset 28h" on page 4074	00000001h
34h	4	"DNCTRL—Offset 34h" on page 4074	00000000h
38h	4	"CRCR_LO—Offset 38h" on page 4075	00000000h
3Ch	4	"CRCR_HI—Offset 3Ch" on page 4076	00000000h
50h	4	"DCBAAP_LO—Offset 50h" on page 4077	00000000h
54h	4	"DCBAAP_HI—Offset 54h" on page 4077	00000000h
58h	4	"CONFIG—Offset 58h" on page 4078	00000000h
420h	4	"PORTSC1—Offset 420h" on page 4079	000002A0h
424h	4	"PORTPMSC1—Offset 424h" on page 4082	00000000h
428h	4	"PORTLI—Offset 428h" on page 4083	00000000h
42Ch	4	"PORTHLPMC—Offset 42Ch" on page 4084	00000000h
430h	4	"PORTSC2—Offset 430h" on page 4085	000002A0h
434h	4	"PORTPMSC2—Offset 434h" on page 4088	00000000h
440h	4	"MFINDEX—Offset 440h" on page 4089	00000000h
444h	4	"RsvdZ—Offset 444h" on page 4090	00000000h
460h	4	"IMAN—Offset 460h" on page 4090	00000000h
464h	4	"IMOD—Offset 464h" on page 4091	00000FA0h
468h	4	"ERSTSZ—Offset 468h" on page 4092	00000000h
46Ch	4	"RsvdP—Offset 46Ch" on page 4092	00000000h
470h	4	"ERSTBA_LO—Offset 470h" on page 4093	00000000h
474h	4	"ERSTBA_HI—Offset 474h" on page 4093	00000000h
478h	4	"ERDP_LO—Offset 478h" on page 4094	00000000h
47Ch	4	"ERDP_HI—Offset 47Ch" on page 4095	00000000h

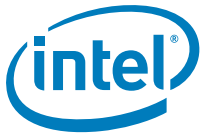


Table 82. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
480h	4	"DB_0—Offset 480h" on page 4095	00000000h
484h	4	"DB_1—Offset 484h" on page 4096	00000000h
488h	4	"DB_2—Offset 488h" on page 4098	00000000h
48Ch	4	"DB_3—Offset 48Ch" on page 4099	00000000h
490h	4	"DB_4—Offset 490h" on page 4100	00000000h
494h	4	"DB_5—Offset 494h" on page 4101	00000000h
498h	4	"DB_6—Offset 498h" on page 4103	00000000h
49Ch	4	"DB_7—Offset 49Ch" on page 4104	00000000h
4A0h	4	"DB_8—Offset 4A0h" on page 4105	00000000h
4A4h	4	"DB_9—Offset 4A4h" on page 4106	00000000h
4A8h	4	"DB_10—Offset 4A8h" on page 4108	00000000h
4ACh	4	"DB_11—Offset 4ACh" on page 4109	00000000h
4B0h	4	"DB_12—Offset 4B0h" on page 4110	00000000h
4B4h	4	"DB_13—Offset 4B4h" on page 4111	00000000h
4B8h	4	"DB_14—Offset 4B8h" on page 4113	00000000h
4BCh	4	"DB_15—Offset 4BCh" on page 4114	00000000h
4C0h	4	"DB_16—Offset 4C0h" on page 4115	00000000h
880h	4	"USBLEGSUP—Offset 880h" on page 4116	00000401h
884h	4	"USBLEGCTLSTS—Offset 884h" on page 4117	00000000h
890h	4	"SUPTPRT2_DW0—Offset 890h" on page 4118	02000002h
894h	4	"SUPTPRT2_DW1—Offset 894h" on page 4119	02000110h
898h	4	"SUPTPRT2_DW2—Offset 898h" on page 4120	00080001h
8A0h	4	"SUPTPRT3_DW0—Offset 8A0h" on page 4121	03000002h
8A4h	4	"SUPTPRT3_DW1—Offset 8A4h" on page 4121	00000000h
8A8h	4	"SUPTPRT3_DW2—Offset 8A8h" on page 4122	00000000h
8B0h	4	"DCID—Offset 8B0h" on page 4123	00960020h
8B4h	4	"DCDB—Offset 8B4h" on page 4123	02000110h
8B8h	4	"DCERSTSZ—Offset 8B8h" on page 4124	0C0000F1h
8BCh	4	"DCERSTBA_LO—Offset 8BCh" on page 4125	07FF000Ah
8C0h	4	"DCERSTBA_HI—Offset 8C0h" on page 4125	0220F04Ch
8C4h	4	"DCERDP_LO—Offset 8C4h" on page 4126	00000480h
8C8h	4	"DCERDP_HI—Offset 8C8h" on page 4127	00000440h
8CCh	4	"DCCTRL—Offset 8CCh" on page 4127	00000000h
8D0h	4	"DCSTAT—Offset 8D0h" on page 4128	00000000h
8D4h	4	"DCPORTSC—Offset 8D4h" on page 4129	00000001h
8D8h	4	"DCECP_LO—Offset 8D8h" on page 4130	00000001h

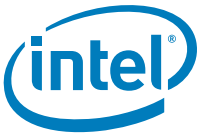


Table 82. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
8DCh	4	"DCECP_HI—Offset 8DCh" on page 4130	00000000h
8E0h	4	"DCDDI1—Offset 8E0h" on page 4131	00000000h
8E4h	4	"DCDDI2—Offset 8E4h" on page 4132	00000000h
C100h	4	"GSBUSCFG0—Offset C100h" on page 4132	00000006h
C104h	4	"GSBUSCFG1—Offset C104h" on page 4134	00000F00h
C108h	4	"GTXTHRCFG—Offset C108h" on page 4134	230A0000h
C10Ch	4	"GRXTHRCFG—Offset C10Ch" on page 4135	22800000h
C110h	4	"GCTL—Offset C110h" on page 4136	45803000h
C118h	4	"GSTS—Offset C118h" on page 4138	3E800002h
C120h	4	"GSNPSID—Offset C120h" on page 4139	5533192Ah
C124h	4	"GGPIO—Offset C124h" on page 4140	00000000h
C128h	4	"GUID—Offset C128h" on page 4140	12345678h
C12Ch	4	"GUCTL—Offset C12Ch" on page 4140	7FC0C600h
C130h	4	"GBUSERRADDRLO—Offset C130h" on page 4142	00000000h
C134h	4	"GBUSERRADDRHI—Offset C134h" on page 4142	00000000h
C138h	4	"GPRTBIMAPLO—Offset C138h" on page 4143	00000000h
C13Ch	4	"GPRTBIMAPHI—Offset C13Ch" on page 4144	00000000h
C140h	4	"GHWPARAMS0—Offset C140h" on page 4145	2020400Ah
C144h	4	"GHWPARAMS1—Offset C144h" on page 4145	0260C93Bh
C148h	4	"GHWPARAMS2—Offset C148h" on page 4147	008086A0h
C14Ch	4	"GHWPARAMS3—Offset C14Ch" on page 4147	10420089h
C150h	4	"GHWPARAMS4—Offset C150h" on page 4148	48822004h
C154h	4	"GHWPARAMS5—Offset C154h" on page 4149	04202088h
C158h	4	"GHWPARAMS6—Offset C158h" on page 4150	0C00AC20h
C15Ch	4	"GHWPARAMS7—Offset C15Ch" on page 4152	038807E6h
C160h	4	"GDBGFIFOSPACE—Offset C160h" on page 4152	00420000h
C164h	4	"GDBGLTSSM—Offset C164h" on page 4153	01010440h
C180h	4	"GPRTBIMAP_HSLO—Offset C180h" on page 4154	00000000h
C184h	4	"GPRTBIMAP_HSHI—Offset C184h" on page 4155	00000000h
C188h	4	"GPRTBIMAP_FSLO—Offset C188h" on page 4156	00000000h
C18Ch	4	"GPRTBIMAP_FSHI—Offset C18Ch" on page 4157	00000000h
C200h	4	"GUSB2PHYCFG—Offset C200h" on page 4157	0000A410h
C240h	4	"GUSB2I2CCTL—Offset C240h" on page 4159	00000000h
C280h	4	"GUSB2PHYACC—Offset C280h" on page 4160	00000000h
C2C0h	4	"GUSB3PIPECTL—Offset C2C0h" on page 4161	02044002h
C300h	4	"GTXFIFOSIZ0—Offset C300h" on page 4163	00000042h

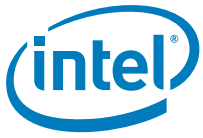


Table 82. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
C304h	4	"GTXFIFOSIZ1—Offset C304h" on page 4163	00420184h
C308h	4	"GTXFIFOSIZ2—Offset C308h" on page 4164	01C60184h
C30Ch	4	"GTXFIFOSIZ3—Offset C30Ch" on page 4164	034A0184h
C310h	4	"GTXFIFOSIZ4—Offset C310h" on page 4165	04CE0082h
C314h	4	"GTXFIFOSIZ5—Offset C314h" on page 4166	05500082h
C318h	4	"GTXFIFOSIZ6—Offset C318h" on page 4166	05D20082h
C31Ch	4	"GTXFIFOSIZ7—Offset C31Ch" on page 4167	06540082h
C320h	4	"GTXFIFOSIZ8—Offset C320h" on page 4167	06D60022h
C324h	4	"GTXFIFOSIZ9—Offset C324h" on page 4168	06F80022h
C328h	4	"GTXFIFOSIZ10—Offset C328h" on page 4168	071A0022h
C32Ch	4	"GTXFIFOSIZ11—Offset C32Ch" on page 4169	073C0022h
C330h	4	"GTXFIFOSIZ12—Offset C330h" on page 4170	075E0022h
C334h	4	"GTXFIFOSIZ13—Offset C334h" on page 4170	07800022h
C338h	4	"GTXFIFOSIZ14—Offset C338h" on page 4171	07A20022h
C33Ch	4	"GTXFIFOSIZ15—Offset C33Ch" on page 4171	07C40022h
C380h	4	"GRXFIFOSIZ0—Offset C380h" on page 4172	00000385h
C384h	4	"GRXFIFOSIZ1—Offset C384h" on page 4172	03850000h
C388h	4	"GRXFIFOSIZ2—Offset C388h" on page 4173	03850000h
C400h	4	"GEVNTADRLO—Offset C400h" on page 4174	00000000h
C404h	4	"GEVNTADRHI—Offset C404h" on page 4174	00000000h
C408h	4	"GEVNTSIZ—Offset C408h" on page 4174	00000000h
C40Ch	4	"GEVNTCOUNT—Offset C40Ch" on page 4175	00000000h
C600h	4	"GHWPARAMS8—Offset C600h" on page 4176	00002000h
C700h	4	"DCFG—Offset C700h" on page 4176	00080800h
C704h	4	"DCTL—Offset C704h" on page 4177	00000000h
C708h	4	"DEVTEN—Offset C708h" on page 4178	00000000h
C70Ch	4	"DSTS—Offset C70Ch" on page 4179	00120004h
C710h	4	"DGCMDPAR—Offset C710h" on page 4181	00000000h
C714h	4	"DGCMDPAR—Offset C710h" on page 4181	00000000h
C720h	4	"DALEPENA—Offset C720h" on page 4182	00000000h
C800h	4	"DEPCMDPAR2_0—Offset C800h" on page 4182	00000000h
C804h	4	"DEPCMDPAR1_0—Offset C804h" on page 4183	00000000h
C808h	4	"DEPCMDPAR0_0—Offset C808h" on page 4183	00000000h
C80Ch	4	"DEPCMD_0—Offset C80Ch" on page 4184	00000000h
C810h	4	"DEPCMDPAR2_1—Offset C810h" on page 4185	00000000h
C814h	4	"DEPCMDPAR1_1—Offset C814h" on page 4185	00000000h

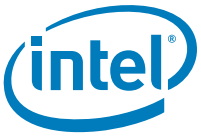


Table 82. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
C818h	4	"DEPCMDPAR0_1—Offset C818h" on page 4186	00000000h
C81Ch	4	"DEPCMD_1—Offset C81Ch" on page 4186	00000000h
C820h	4	"DEPCMDPAR2_2—Offset C820h" on page 4187	00000000h
C824h	4	"DEPCMDPAR1_2—Offset C824h" on page 4188	00000000h
C828h	4	"DEPCMDPAR0_2—Offset C828h" on page 4188	00000000h
C82Ch	4	"DEPCMD_2—Offset C82Ch" on page 4189	00000000h
C830h	4	"DEPCMDPAR2_3—Offset C830h" on page 4189	00000000h
C834h	4	"DEPCMDPAR1_3—Offset C834h" on page 4190	00000000h
C838h	4	"DEPCMDPAR0_3—Offset C838h" on page 4190	00000000h
C83Ch	4	"DEPCMD_3—Offset C83Ch" on page 4191	00000000h
C840h	4	"DEPCMDPAR2_4—Offset C840h" on page 4192	00000000h
C844h	4	"DEPCMDPAR1_4—Offset C844h" on page 4192	00000000h
C848h	4	"DEPCMDPAR0_4—Offset C848h" on page 4193	00000000h
C84Ch	4	"DEPCMD_4—Offset C84Ch" on page 4193	00000000h
C850h	4	"DEPCMDPAR2_5—Offset C850h" on page 4194	00000000h
C854h	4	"DEPCMDPAR1_5—Offset C854h" on page 4195	00000000h
C858h	4	"DEPCMDPAR0_5—Offset C858h" on page 4195	00000000h
C85Ch	4	"DEPCMD_5—Offset C85Ch" on page 4196	00000000h
C860h	4	"DEPCMDPAR2_6—Offset C860h" on page 4196	00000000h
C864h	4	"DEPCMDPAR1_6—Offset C864h" on page 4197	00000000h
C868h	4	"DEPCMDPAR0_6—Offset C868h" on page 4197	00000000h
C86Ch	4	"DEPCMD_6—Offset C86Ch" on page 4198	00000000h
C870h	4	"DEPCMDPAR2_7—Offset C870h" on page 4199	00000000h
C874h	4	"DEPCMDPAR1_7—Offset C874h" on page 4199	00000000h
C878h	4	"DEPCMDPAR0_7—Offset C878h" on page 4200	00000000h
C87Ch	4	"DEPCMD_7—Offset C87Ch" on page 4200	00000000h
C880h	4	"DEPCMDPAR2_8—Offset C880h" on page 4201	00000000h
C884h	4	"DEPCMDPAR1_8—Offset C884h" on page 4202	00000000h
C888h	4	"DEPCMDPAR0_8—Offset C888h" on page 4202	00000000h
C88Ch	4	"DEPCMD_8—Offset C88Ch" on page 4203	00000000h
C890h	4	"DEPCMDPAR2_9—Offset C890h" on page 4203	00000000h
C894h	4	"DEPCMDPAR1_9—Offset C894h" on page 4204	00000000h
C898h	4	"DEPCMDPAR0_9—Offset C898h" on page 4204	00000000h
C89Ch	4	"DEPCMD_9—Offset C89Ch" on page 4205	00000000h
C8A0h	4	"DEPCMDPAR2_10—Offset C8A0h" on page 4206	00000000h
C8A4h	4	"DEPCMDPAR1_10—Offset C8A4h" on page 4206	00000000h

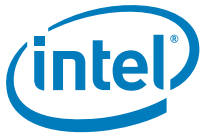


Table 82. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
C8A8h	4	"DEPCMDPAR0_10—Offset C8A8h" on page 4207	00000000h
C8ACh	4	"DEPCMD_10—Offset C8ACh" on page 4207	00000000h
C8B0h	4	"DEPCMDPAR2_11—Offset C8B0h" on page 4208	00000000h
C8B4h	4	"DEPCMDPAR1_11—Offset C8B4h" on page 4209	00000000h
C8B8h	4	"DEPCMDPAR0_11—Offset C8B8h" on page 4209	00000000h
C8BCh	4	"DEPCMD_11—Offset C8BCh" on page 4210	00000000h
C8C0h	4	"DEPCMDPAR2_12—Offset C8C0h" on page 4210	00000000h
C8C4h	4	"DEPCMDPAR1_12—Offset C8C4h" on page 4211	00000000h
C8C8h	4	"DEPCMDPAR0_12—Offset C8C8h" on page 4211	00000000h
C8CCh	4	"DEPCMD_12—Offset C8CCh" on page 4212	00000000h
C8D0h	4	"DEPCMDPAR2_13—Offset C8D0h" on page 4213	00000000h
C8D4h	4	"DEPCMDPAR1_13—Offset C8D4h" on page 4213	00000000h
C8D8h	4	"DEPCMDPAR0_13—Offset C8D8h" on page 4214	00000000h
C8DCh	4	"DEPCMD_13—Offset C8DCh" on page 4214	00000000h
C8E0h	4	"DEPCMDPAR2_14—Offset C8E0h" on page 4215	00000000h
C8E4h	4	"DEPCMDPAR1_14—Offset C8E4h" on page 4216	00000000h
C8E8h	4	"DEPCMDPAR0_14—Offset C8E8h" on page 4216	00000000h
C8ECh	4	"DEPCMD_14—Offset C8ECh" on page 4217	00000000h
C8F0h	4	"DEPCMDPAR2_15—Offset C8F0h" on page 4217	00000000h
C8F4h	4	"DEPCMDPAR1_15—Offset C8F4h" on page 4218	00000000h
C8F8h	4	"DEPCMDPAR0_15—Offset C8F8h" on page 4218	00000000h
C8FCh	4	"DEPCMD_15—Offset C8FCh" on page 4219	00000000h
C900h	4	"DEPCMDPAR2_16—Offset C900h" on page 4220	00000000h
C904h	4	"DEPCMDPAR1_16—Offset C904h" on page 4220	00000000h
C908h	4	"DEPCMDPAR0_16—Offset C908h" on page 4221	00000000h
C90Ch	4	"DEPCMD_16—Offset C90Ch" on page 4221	00000000h
C910h	4	"DEPCMDPAR2_17—Offset C910h" on page 4222	00000000h
C914h	4	"DEPCMDPAR1_17—Offset C914h" on page 4223	00000000h
C918h	4	"DEPCMDPAR0_17—Offset C918h" on page 4223	00000000h
C91Ch	4	"DEPCMD_17—Offset C91Ch" on page 4224	00000000h
C920h	4	"DEPCMDPAR2_18—Offset C920h" on page 4224	00000000h
C924h	4	"DEPCMDPAR1_18—Offset C924h" on page 4225	00000000h
C928h	4	"DEPCMDPAR0_18—Offset C928h" on page 4225	00000000h
C92Ch	4	"DEPCMD_18—Offset C92Ch" on page 4226	00000000h
C930h	4	"DEPCMDPAR2_19—Offset C930h" on page 4227	00000000h
C934h	4	"DEPCMDPAR1_19—Offset C934h" on page 4227	00000000h

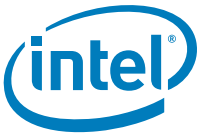


Table 82. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
C938h	4	"DEPCMDPAR0_19—Offset C938h" on page 4228	00000000h
C93Ch	4	"DEPCMD_19—Offset C93Ch" on page 4228	00000000h
C940h	4	"DEPCMDPAR2_20—Offset C940h" on page 4229	00000000h
C944h	4	"DEPCMDPAR1_20—Offset C944h" on page 4230	00000000h
C948h	4	"DEPCMDPAR0_20—Offset C948h" on page 4230	00000000h
C94Ch	4	"DEPCMD_20—Offset C94Ch" on page 4231	00000000h
C950h	4	"DEPCMDPAR2_21—Offset C950h" on page 4231	00000000h
C954h	4	"DEPCMDPAR1_21—Offset C954h" on page 4232	00000000h
C958h	4	"DEPCMDPAR0_21—Offset C958h" on page 4232	00000000h
C95Ch	4	"DEPCMD_21—Offset C95Ch" on page 4233	00000000h
C960h	4	"DEPCMDPAR2_22—Offset C960h" on page 4234	00000000h
C964h	4	"DEPCMDPAR1_22—Offset C964h" on page 4234	00000000h
C968h	4	"DEPCMDPAR0_22—Offset C968h" on page 4235	00000000h
C96Ch	4	"DEPCMD_22—Offset C96Ch" on page 4235	00000000h
C970h	4	"DEPCMDPAR2_23—Offset C970h" on page 4236	00000000h
C974h	4	"DEPCMDPAR1_23—Offset C974h" on page 4237	00000000h
C978h	4	"DEPCMDPAR0_23—Offset C978h" on page 4237	00000000h
C97Ch	4	"DEPCMD_23—Offset C97Ch" on page 4238	00000000h
C980h	4	"DEPCMDPAR2_24—Offset C980h" on page 4238	00000000h
C984h	4	"DEPCMDPAR1_24—Offset C984h" on page 4239	00000000h
C988h	4	"DEPCMDPAR0_24—Offset C988h" on page 4239	00000000h
C98Ch	4	"DEPCMD_24—Offset C98Ch" on page 4240	00000000h
C990h	4	"DEPCMDPAR2_25—Offset C990h" on page 4241	00000000h
C994h	4	"DEPCMDPAR1_25—Offset C994h" on page 4241	00000000h
C998h	4	"DEPCMDPAR0_25—Offset C998h" on page 4242	00000000h
C99Ch	4	"DEPCMD_25—Offset C99Ch" on page 4242	00000000h
C9A0h	4	"DEPCMDPAR2_26—Offset C9A0h" on page 4243	00000000h
C9A4h	4	"DEPCMDPAR1_26—Offset C9A4h" on page 4244	00000000h
C9A8h	4	"DEPCMDPAR0_26—Offset C9A8h" on page 4244	00000000h
C9ACh	4	"DEPCMD_26—Offset C9ACh" on page 4245	00000000h
C9B0h	4	"DEPCMDPAR2_27—Offset C9B0h" on page 4245	00000000h
C9B4h	4	"DEPCMDPAR1_27—Offset C9B4h" on page 4246	00000000h
C9B8h	4	"DEPCMDPAR0_27—Offset C9B8h" on page 4246	00000000h
C9BCh	4	"DEPCMD_27—Offset C9BCh" on page 4247	00000000h
C9C0h	4	"DEPCMDPAR2_28—Offset C9C0h" on page 4248	00000000h
C9C4h	4	"DEPCMDPAR1_28—Offset C9C4h" on page 4248	00000000h

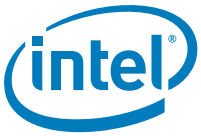


Table 82. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
C9C8h	4	"DEPCMDPAR0_28—Offset C9C8h" on page 4249	00000000h
C9CCh	4	"DEPCMD_28—Offset C9CCh" on page 4249	00000000h
C9D0h	4	"DEPCMDPAR2_29—Offset C9D0h" on page 4250	00000000h
C9D4h	4	"DEPCMDPAR1_29—Offset C9D4h" on page 4251	00000000h
C9D8h	4	"DEPCMDPAR0_29—Offset C9D8h" on page 4251	00000000h
C9DCh	4	"DEPCMD_29—Offset C9DCh" on page 4252	00000000h
C9E0h	4	"DEPCMDPAR2_30—Offset C9E0h" on page 4252	00000000h
C9E4h	4	"DEPCMDPAR1_30—Offset C9E4h" on page 4253	00000000h
C9E8h	4	"DEPCMDPAR0_30—Offset C9E8h" on page 4253	00000000h
C9ECh	4	"DEPCMD_30—Offset C9ECh" on page 4254	00000000h
C9F0h	4	"DEPCMDPAR2_31—Offset C9F0h" on page 4255	00000000h
C9F4h	4	"DEPCMDPAR1_31—Offset C9F4h" on page 4255	00000000h
C9F8h	4	"DEPCMDPAR0_31—Offset C9F8h" on page 4256	00000000h
C9FCh	4	"DEPCMD_31—Offset C9FCh" on page 4256	00000000h
CC00h	4	"OCFG—Offset CC00h" on page 4257	00000000h
CC04h	4	"OCTL—Offset CC04h" on page 4258	00000040h
CC08h	4	"OEVT—Offset CC08h" on page 4259	80000000h
CC0Ch	4	"OEVTEN—Offset CC0Ch" on page 4261	00000000h
CC10h	4	"OSTS—Offset CC10h" on page 4263	00000019h
CC20h	4	"ADPCFG—Offset CC20h" on page 4264	00000000h
CC24h	4	"ADPCTL—Offset CC24h" on page 4265	00000000h
CC28h	4	"ADPEVT—Offset CC28h" on page 4265	00000000h
CC2Ch	4	"ADPEVTEN—Offset CC2Ch" on page 4266	00000000h
CC30h	4	"BCFG—Offset CC30h" on page 4267	00000000h
CC38h	4	"BCEVT—Offset CC38h" on page 4268	00000000h
CC3Ch	4	"BCEVTEN—Offset CC3Ch" on page 4268	00000000h

3.74.1 CAPLENGTH—Offset 0h

This register is used as an offset to add to register base to find the beginning of the Operational Register Space.

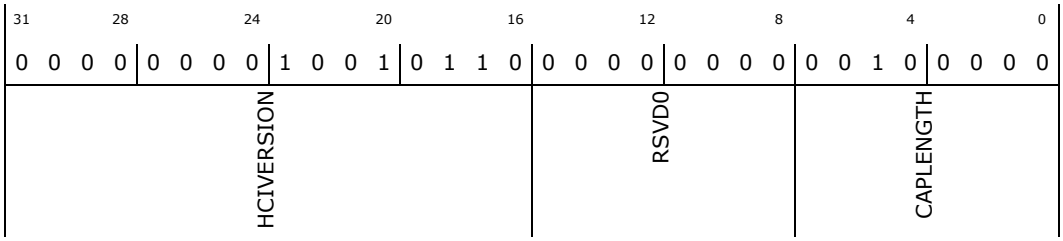
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPLENGTH: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00960020h



Bit Range	Default & Access	Description
31:16	096h RO	**HCIVERSION:** This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. e.g. 0100h corresponds to xHCI version 1.0.xs
15:8	0h RO	**RSVD0:** Reserved.
7:0	20h RO	**CAPLENGTH:** This register is used as an offset to add to register base to find the beginning of the Operational Register Space.

3.74.2 HCSPARAMS1—Offset 4h

number of ports implemented is 2 because there is 1 DWC_USB2_HOST_NUM_U2_ROOT_PORTS and 1 DWC_USB3_HOST_NUM_U3_ROOT_PORT

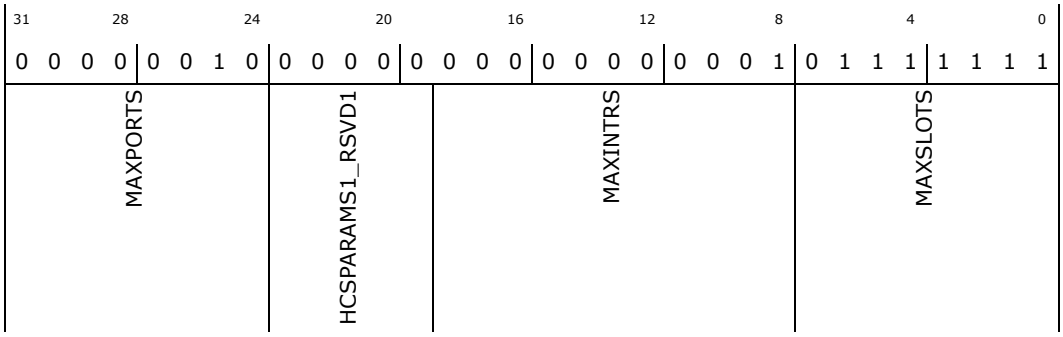
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HCSPARAMS1: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0200017Fh



Bit Range	Default & Access	Description
31:24	02h RO	**MAXPORTS:** Number of Ports (MaxPorts). This field specifies the maximum Port Number value, i.e. the highest numbered Port Register Set that are addressable in the Operational Register Space (refer to Table 29). Valid values are in the range of 1h to FFh. The value in this field shall reflect the maximum Port Number value assigned by an xHCI Supported Protocol Capability, described in section 7.2. Software shall refer to these capabilities to identify whether a specific Port Number is valid, and the protocol supported by the associated Port Register Set.
23:19	0h RO	**HCSPARAMS1_RSVD1:** reserved
18:8	1h RO	**MAXINTRS:** Number of Interrupters (MaxIntrs). This field specifies the number of Interrupters implemented on this host controller. Each Interrupter may be allocated to a MSI or MSI-X vector and controls its generation and moderation. The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space (refer to section 5.5). Valid values are in the range of 1h to 400h. A 0 in this field is undefined.
7:0	7fh RO	**MAXSLOTS:** Number of Device Slots (MaxSlots). This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255. The value of 0 is reserved.

3.74.3 HCSPARAMS2—Offset 8h

Host Controller Structural Parameters 2

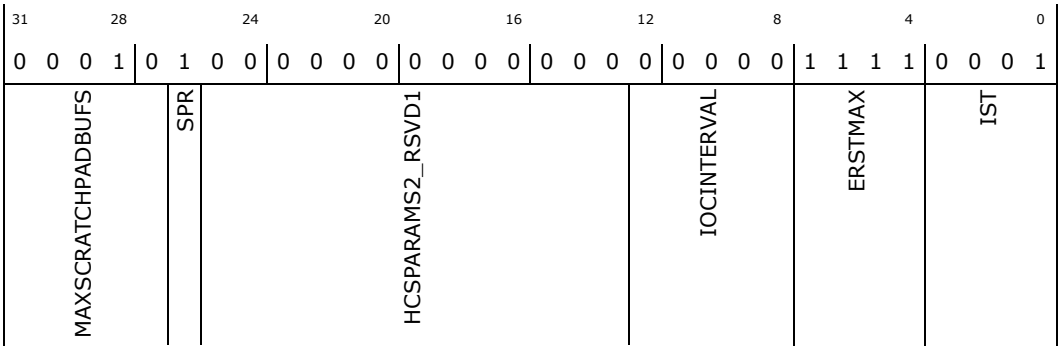
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HCSPARAMS2: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 140000F1h



Bit Range	Default & Access	Description
31:27	02h RO	**MAXSCRATCHPADBUFS:** For xHCI 0.96,this field is Max Scratchpad Bufs / For xHCI 1.0, this field is Max Scratchpad Bufs Lo
26	1h RO	**SPR:** Scratchpad Restore (SPR)
25:13	0h RO	**HCSPARAMS2_RSVD1:** reserved
12:8	0h RO	**IOCINTERVAL:** This field is valid only for xHCI 0.96. For xHCI 1.0, this field is Reserved.
7:4	fh RO	**ERSTMAX:** Event Ring Segment Table Max (ERST Max)
3:0	1h RO	**IST:** Isochronous Scheduling Threshold (IST)

3.74.4 HCSPARAMS3—Offset Ch

Structural Parameters 3 Register

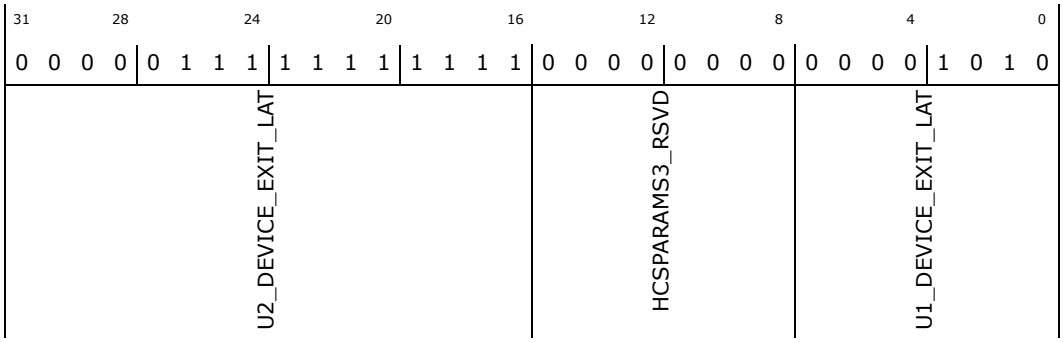
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HCSPARAMS3: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 07FF000Ah



Bit Range	Default & Access	Description
31:16	07ffh RO	**U2_DEVICE_EXIT_LAT:** Reserved.
15:8	0h RO	**HCSPARAMS3_RSVD:** Reserved.
7:0	0ah RO	**U1_DEVICE_EXIT_LAT:** Reserved.

3.74.5 HCCPARAMS—Offset 10h

Capability Parameters Register

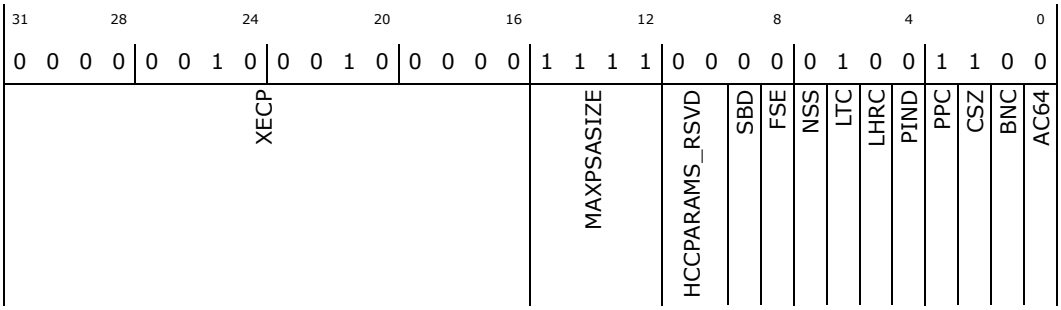
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HCCPARAMS: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0220F04Ch



Bit Range	Default & Access	Description
31:16	220h RO	**XECP:** Based on configuration, core automatically updates it
15:12	fh RO	**MAXPSASIZE:** Maximum Primary Stream Array Size
11:10	0h RO	**HCCPARAMS_RSVD:** Reserved
9	0h RO	**SBD:** Secondary Bandwidth Domain Reporting (SBD)
8	0h RO	**FSE:** For xHCI 0.96, this field is Force Stopped Event (FSE) / For xHCI 1.0, this field is Parse All Event Data (PAE)
7	0h RO	**NSS:** No Secondary SID Support (NSS). This flag indicates whether the host controller implementation supports Secondary Stream IDs. A 1 in this bit indicates that Secondary Stream ID decoding is not supported. A 0 in this bit indicates that Secondary Stream ID decoding is supported. (refer to Sections 4.12.2 and 6.2.3).
6	1h RO	**LTC:** Latency Tolerance Messaging Capability (LTC). This flag indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A 1 in this bit indicates that LTM is supported. A 0 in this bit indicates that LTM is not supported. Refer to section 4.13.1 for more information on LTM.
5	0h RO	**LHRC:** Light HC Reset Capability (LHRC). This flag indicates whether the host controller implementation supports a Light Host Controller Reset. A 1 in this bit indicates that Light Host Controller Reset is supported. A 0 in this bit indicates that Light Host Controller Reset is not supported. The value of this flag affects the functionality of the Light Host Controller Reset (LHCRST) flag in the USBCMD register (refer to Section 5.4.1).

Bit Range	Default & Access	Description
4	0h RO	**PIND:** Port Indicators (PIND). This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a 1, the port status and control registers include a read/writeable field for controlling the state of the port indicator. Refer to Section 5.4.8 for definition of the Port Indicator Control field.
3	1h RO	**PPC:** Port Power Control (PPC). This flag indicates whether the host controller implementation includes port power control. A 1 in this bit indicates the ports have port power switches. A 0 in this bit indicates the port do not have port power switches. The value of this flag affects the functionality of the PP flag in each port status and control register (refer to Section 5.4.8).
2	1h RO	**CSZ:** Context Size (CSZ). If this bit is set to 1, then the xHC uses 64 byte Context data structures. If this bit is cleared to 0, then the xHC uses 32 byte Context data structures. Note: This flag does not apply to Stream Contexts.
1	0h RO	**BNC:** BW Negotiation Capability (BNC). This flag identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this flag have the following interpretation: for Value 0 Description BW Negotiation not implemented. for Value 1 DescriptionBW Negotiation implemented. Refer to section 4.16 of XHCI specification for more information on Bandwidth Negotiation.
0	0h RO	**AC64:** 64-bit Addressing Capability (AC64). This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the high order 32 bits of 64 bit register and data structure pointer fields. Values for this flag have the following interpretation: for Value 0 Description 32-bit address memory pointers implemented. for Value 1 description 64-bit address memory pointers implemented. If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers.

3.74.6 DBOFF—Offset 14h

Doorbell Offset Register

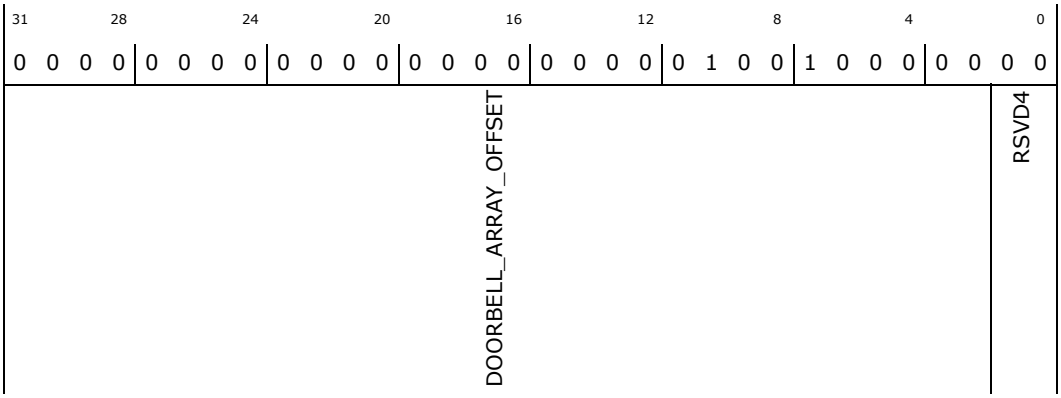
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DBOFF: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000480h



Bit Range	Default & Access	Description
31:2	120h RO	**DOORBELL_ARRAY_OFFSET:** Based on configuration, core automatically updates it
1:0	0h RO	**RSVD4:** Reserved

3.74.7 RTSOFF—Offset 18h

Runtime Register Space Offset Register

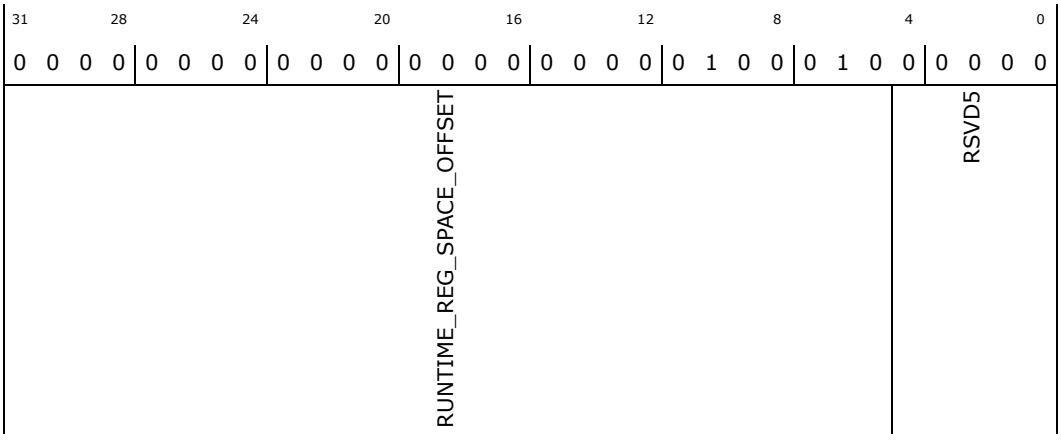
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RTSOFF: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000440h



Bit Range	Default & Access	Description
31:5	22h RO	**RUNTIME_REG_SPACE_OFFSET:** Based on configuration, core automatically updates it
4:0	0h RO	**RSVD5:** Reserved

3.74.8 Rsvd_HC—Offset 1Ch

reserved

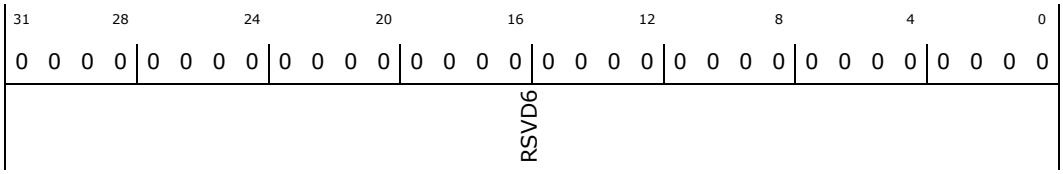
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Rsvd_HC: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**RSVD6:** Reserved.

3.74.9 USBCMD—Offset 20h

USB Command Register Bit Definitions

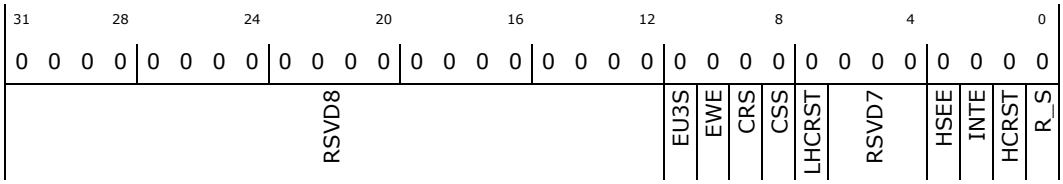
Access Method

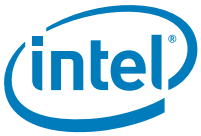
Type: Memory Mapped I/O Register (Size: 32 bits)

USBCMD: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h





Bit Range	Default & Access	Description
31:12	0h RO	**RSVD8:** reserved
11	0h RW	**EU3S:** Enable U3 MFINDEX Stop (EU3S) - RW. Default = 0. When set to 1, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to 0 the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, Training, or Powered-off state. Refer to section 4.14.2 for more information.
10	0h RW	**EWE:** Enable Wrap Event (EWE) - RW. Default = 0. When set to 1, the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to 0 no MFINDEX Wrap Events are generated. Refer to section 4.14.2 for more information. When this register is exposed by a Virtual Function (VF), the generation of MFINDEX Wrap Events to VFs shall be emulated by the VMM.
9	0h RW	**CRS:** Controller Restore State: This command is similar to the USBCMD. CRS bit in host mode and initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'.
8	0h RW	**CSS:** Controller Save State: This command is similar to the USBCMD. CSS bit in host mode and initiates the save process. When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'.
7	0h RW	**LHCRST:** Light Host Controller Reset (LHCRST) RO or RW. Optional normative. Default = 0. If the Light HC Reset Capability (LHRC) bit in the HCCPARAMS register is 1, then this flag allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as 0 indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a 1 indicates the Light Host Controller Reset has not yet completed. If not implemented, a read of this flag shall always return a 0. All registers in the Aux Power well shall maintain the values that had been asserted prior to the Light Host Controller Reset. Refer to section 4.23.1 for more information. When this register is exposed by a Virtual Function (VF), this bit only generates a Light Reset to the xHC instance presented by the selected VF, e.g. Disable the VFs device slots and set the associated VF Run bit to Stopped. Refer to section 8 for more information.
6:4	0h RO	**RSVD7:** Reserved
3	0h RW	**HSEE:** Host System Error Enable (HSEE) RW. Default = 0. When this bit is a 1, and the HSE bit in the USBSTS register is a 1, the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit. Refer to section 4.10.2.6 for more information. When this register is exposed by a Virtual Function (VF), the effect of the assertion of this bit on the Physical Function (PF0) is determined by the VMM. Refer to section 8 for more information.

Bit Range	Default & Access	Description
2	0h RW	**INTE:** Interrupter Enable (INTE) RW. Default = 0. This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is a 1, then Interrupter host system interrupt generation is allowed, e.g. the xHC shall issue an interrupt at the next interrupt threshold if the host system interrupt mechanism (e.g. MSI, MSI-X, etc.) is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism. When this register is exposed by a Virtual Function (VF), this bit only enables the set of Interrupters assigned to the selected VF. Refer to section 7.7.2 for more information.
1	0h RW	**HCRST:** Host Controller Reset (HCRST) RW. Default = 0. This control bit is used by software to reset the host controller. The effects of this bit on the xHC and the Root Hub registers are similar to a Chip Hardware Reset. When software writes a 1 to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on the USB is immediately terminated. A USB reset shall not be driven on USB2 downstream ports, however a Hot or Warm Reset shall be initiated on USB3 Root Hub downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Software shall re initialize the host controller as described in Section 4.1 in order to return the host controller to an operational state. This bit is cleared to 0 by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this bit and shall not write any xHC Operational or Runtime registers until while HCRST is 1. Note, the completion of the xHC reset process is not gated by the Root Hub port reset process. Software shall not set this bit to 1 when the HCHalted (HCH) bit in the USBSTS register is a 0. Attempting to reset an actively running host controller may result in undefined behavior. When this register is exposed by a Virtual Function (VF), this bit only resets the xHC instance presented by the selected VF. Refer to section 8 for more information.
0	0h RW	**R_S:** Run/Stop (R/S) RW. Default = 0. 1 = Run. 0 = Stop. When set to a 1, the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a 1. When this bit is cleared to 0, the xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halts. Refer to section 5.4.1.1 for more information on how R/S shall be managed. The xHC shall halt within 16 ms. after software clears the Run/Stop bit if the above conditions have been met. The HCHalted (HCH) bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a 1 to this flag unless the xHC is in the Halted state (i.e. HCH in the USBSTS register is 1). Doing so may yield undefined results. Writing a 0 to this flag when the xHC is in the Running state (i.e. HCH = 0) and any Event Rings are in the Event Ring Full state (refer to section 4.9.4) may result in lost events. When this register is exposed by a Virtual Function (VF), this bit only controls the run state of the xHC instance presented by the selected VF. Refer to section 8 for more information.

3.74.10 USBSTS—Offset 24h

USB Command Register Bit Definitions

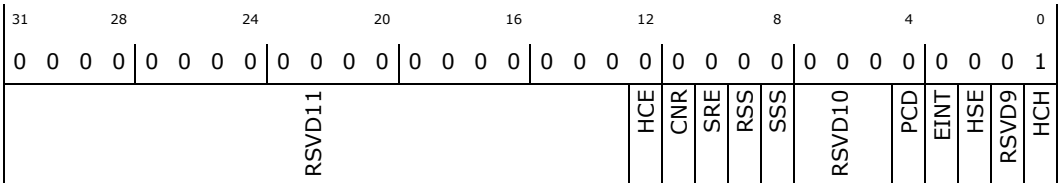
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

USBSTS: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:13	0h RO	**RSVD11:** reserved
12	0h RO	**HCE:** Host Controller Error (HCE) - RO. Default = 0. 0' = No internal xHC error conditions exist '1' = Internal xHC error condition. This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and reinitialize the xHC. Refer to section 4.24.1 of xhci specification for more information.
11	0h RO	**CNR:** Controller Not Ready (CNR) - RO. Default = '1'. '0' = Ready '1' = Not Ready. Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = '0'. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared ('0') until the next Chip Hardware Reset.
10	0h RO	**SRE:** Save/Restore Error (SRE) -RW1C. Default = '0'. If an error occurs during a Save or Restore operation this bit shall be set to '1'. This bit shall be cleared to '0' when a Save or Restore operation is initiated or when written with '1'. Refer to section 4.23.2 of xhci specification for more information.
9	0h RO	**RSS:** Restore State Status: This bit is similar to the USBSTS.RSS in host mode. When the controller has finished the save process, it will complete the command by setting DSTS.RSS to '0'.
8	0h RO	**SSS:** Save State Status: This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it will complete the command by setting DSTS.SSS to '0'
7:5	0h RO	**RSVD10:** reserved
4	0h RW	**PCD:** Reserved.
3	0h RO	**EINT:** Reserved.
2	0h RO	**HSE:** Reg field HSE
1	0h RO	**RSVD9:** reserved
0	1h RO	**HCH:** Reg field HCH

3.74.11 PAGESIZE—Offset 28h

Page Size Register Bit Definitions. This register is used by software to enable or disable the reporting of the reception of specific USB Device Notification Transaction Packets. A Notification Enable (Nx, where x = 0 to 15) flag is defined for each of the 16 possible device notification types. If a flag is set for a specific notification type, a Device Notification Event shall be generated when the respective notification packet is received. After reset all notifications are disabled. Refer to section 6.4.2.7. This register shall be written as a Dword. Byte writes produce undefined results.

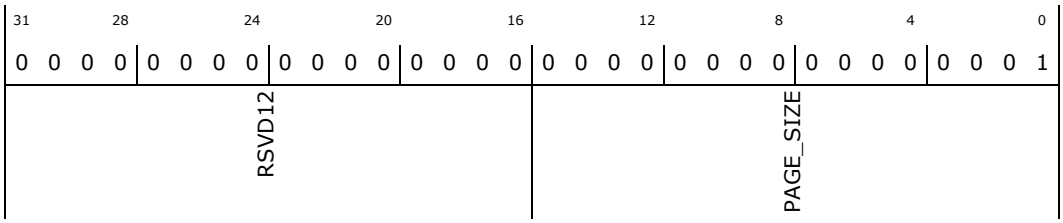
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PAGESIZE: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD12:** reserved
15:0	1h RO	**PAGE_SIZE:** Reg field PAGE_SIZE

3.74.12 DNCTRL—Offset 34h

Device Notification Register Bit Definitions.

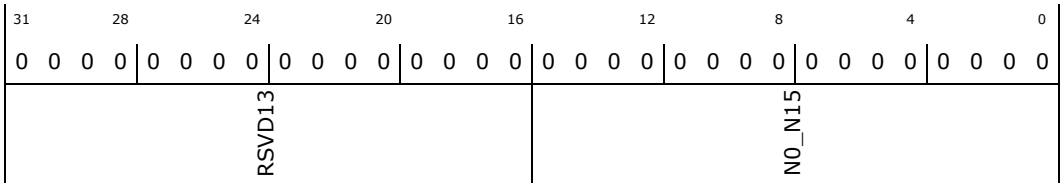
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DNCTRL: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD13:** reserved
15:0	0h RW	**N0_N15:** Reg field N0_N15

3.74.13 CRCR_LO—Offset 38h

Register CRCR_LO

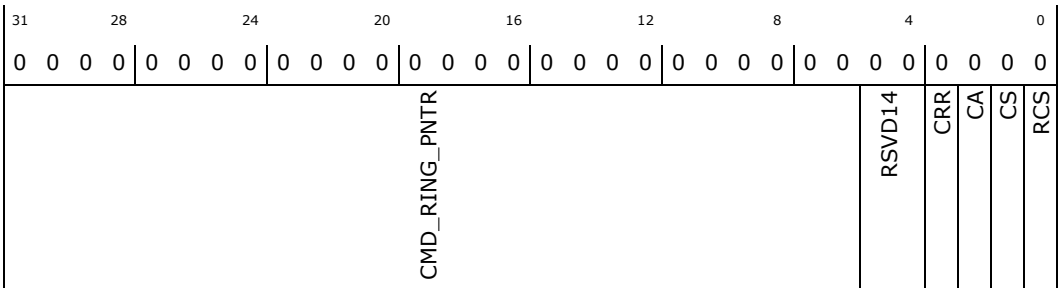
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCR_LO: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**CMD_RING_PNTR:** Command Ring Pointer - RW. Default = 0. This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when Command Ring Running (CRR) = 1. If the CRCR is written while the Command Ring is stopped (CCR = 0), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CCR = 0) then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns 0.
5:4	0h RO	**RSVD14:** reserved
3	0h RW	**CRR:** Command Ring Running (CRR) - RO. Default = 0. This flag is set to 1 if the Run/Stop (R/S) bit is 1 and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to 0 when the Command Ring is stopped after writing a 1 to the Command Stop (CS) or Command Abort (CA) flags, or if the R/S bit is cleared to 0.

Bit Range	Default & Access	Description
2	0h RW	**CA:** Command Abort (CA) - RW1S. Default = 0. Writing a 1 to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped. Refer to section 4.6.1.2 for more information on aborting a command. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0. Reading this bit always returns 0.
1	0h RW	**CS:** Command Stop (CS) - RW1S. Default = 0. Writing a 1 to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. Refer to section 4.6.1.1 for more information on stopping a command. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0. Reading this bit shall always return 0.
0	0h RW	**RCS:** Ring Cycle State (RCS) - RW. This bit identifies the value of the xHC Consumer Cycle State (CCS) flag for the TRB referenced by the Command Ring Pointer. Refer to section 4.9.3 for more information. Writes to this flag are ignored if Command Ring Running (CRR) is 1. If the CRCR is written while the Command Ring is stopped (CRR = 0), then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CRR = 0), then the Command Ring shall begin fetching Command TRBs using the current value of the internal Command Ring CCS flag. Reading this flag always returns 0.

3.74.14 CRCR_HI—Offset 3Ch

Register CRCR_HI

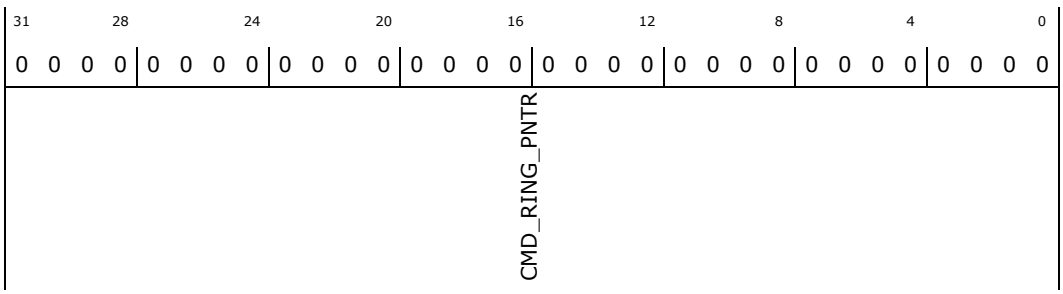
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRCR_HI: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**CMD_RING_PNTR:** Reg field CMD_RING_PNTR

3.74.15 DCBAAP_LO—Offset 50h

Register DCBAAP_LO

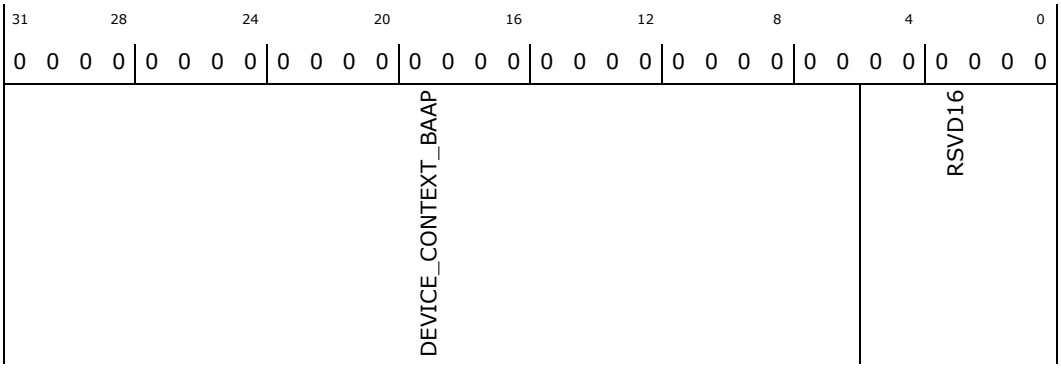
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCBAAP_LO: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**DEVICE_CONTEXT_BAAP:** Reg field DEVICE_CONTEXT_BAAP
5:0	0h RO	**RSVD16:** reserved

3.74.16 DCBAAP_HI—Offset 54h

Register DCBAAP_HI

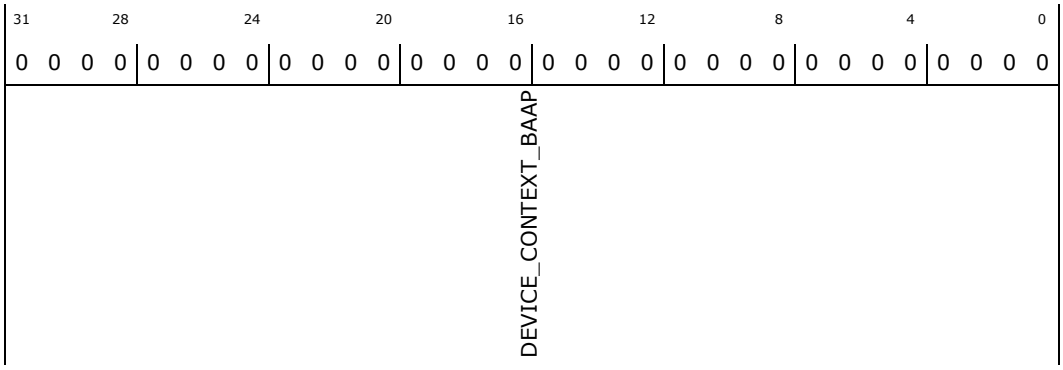
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCBAAP_HI: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DEVICE_CONTEXT_BAAP:** Reg field DEVICE_CONTEXT_BAAP

3.74.17 CONFIG—Offset 58h

Configure Register Bit Definitions. This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST). The initial conditions of a port are described in section 4.19 of xhci specification .

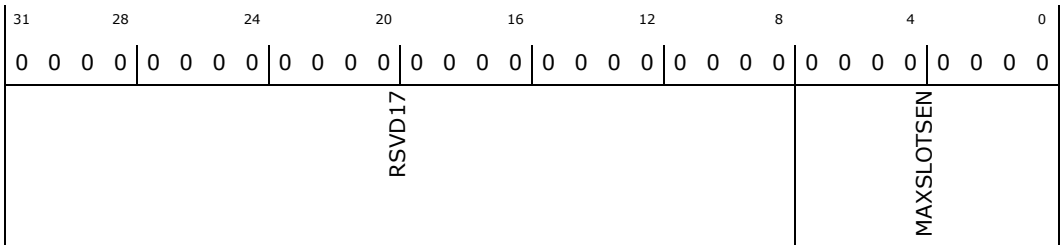
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CONFIG: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RSVD17:** reserved
7:0	0h RW	**MAXSLOTSEN:** Reg field MAXSLOTSEN

3.74.18 PORTSC1—Offset 420h

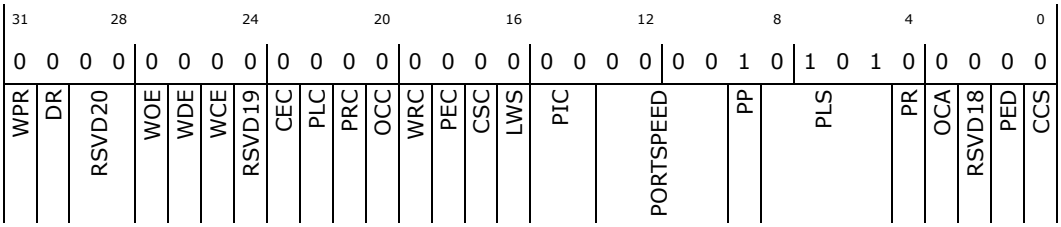
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

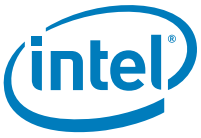
PORTSC1: [BAR] + 420h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

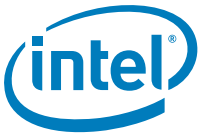
Default: 000002A0h



Bit Range	Default & Access	Description
31	0h RW	**WPR:** Warm Port Reset (WPR) RW1S/RsvdZ. Default = 0. When software writes a 1 to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to 1. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return 0 when read. Refer to section 4.19.5.1. of XHCI specification. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
30	0h RW	**DR:** Device Removable (DR) - RO. This flag indicates if this port has a removable device attached. 1 = Device is non-removable. 0 = Device is removable.
29:28	0h RO	**RSVD20:** reserved
27	0h RW	**WOE:** Wake on Over-current Enable (WOE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to over-current conditions as system wake-up events. Refer to section 4.15 for operational model.
26	0h RW	**WDE:** Wake on Disconnect Enable (WDE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to device disconnects as system wake-up eventsn. Refer to section 4.15 for operational model.
25	0h RW	**WCE:** Wake on Connect Enable (WCE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to device connects as system wake-up events . Refer to section 4.15 for operational model.
24	0h RO	**RSVD19:** reserved
23	0h RW	**CEC:** Port Config Error Change (CEC) RW1CS/RsvdZ. Default = 0. This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage. Note: This flag is valid only for USB3 protocol ports. For USB2 protocol ports this bit shall be RsvdZ.
22	0h RW	**PLC:** Port Link State Change (PLC) RW1CS. Default = 0. This flag is set to 1 due to the following PLS transitions mentioned in the XHCI specification



Bit Range	Default & Access	Description
21	0h RW	**PRC:** Port Reset Change (PRC) RW1CS. Default = 0. This flag is set to 1 due to a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to 1 if the reset processing was forced to terminate due to software clearing PP or PED to '0'. 0 = No change. 1 = Reset complete. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5. Refer to section 4.19.2 for more information on change bit usage.
20	0h RW	**OCC:** Over-current Change (OCC) RW1CS. Default = 0. This bit shall be set to a 1 when there is a 0 to 1 or 1 to 0 transition of Over-current Active (OCA). Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage.
19	0h RW	**WRC:** Warm Port Reset Change (WRC) RW1CS/RsvdZ. Default = 0. This bit is set when Warm Reset processing on this port completes. 0 = No change. 1 = Warm Reset complete. Note that this flag shall not be set to 1 if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5.1. Refer to section 4.19.2 for more information on change bit usage. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
18	0h RW	**PEC:** Port Enabled/Disabled Change (PEC) RW1CS. Default = 0. 1 = change in PED. 0 = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to 0. Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage. For a USB2 protocol port, this bit shall be set to 1 only when the port is disabled due to the appropriate conditions existing at the EOF2 point (refer to section 11.8.1 of the USB2 Specification for the definition of a Port Error). For a USB3 protocol port, this bit shall never be set to 1.
17	0h RW	**CSC:** Connect Status Change (CSC) RW1CS. Default = 0. 1 = Change in CCS. 0 = No change. This flag indicates a change has occurred in the ports Current Connect Status (CCS) or Cold Attach Status (CAS) bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to 0, or the CAS transition was due to software setting WPR to 1. The xHC sets this bit to 1 for all changes to the port device connect status , even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be setting an already-set bit (i.e., the bit will remain 1). Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage.
16	0h RW	**LWS:** Port Link State Write Strobe (LWS) RW. Default = 0. When this bit is set to 1 on a write reference to this register, this flag enables writes to the PLS field. When 0, write data in PLS field is ignored. Reads to this bit return 0.
15:14	0h RW	**PIC:** Port Indicator Control (PIC) RWS. Default = 0. Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a 0.
13:10	0h RW	**PORTSPEED:** Port Speed (Port Speed) ROS. Default = 0. This field identifies the speed of the connected USB Device. This field is only relevant if a device is connected (CCS = 1) in all other cases this field shall indicate Undefined Speed. (more information in the XHCI specification)



Bit Range	Default & Access	Description
9	1h RW	**PP:** Port Power (PP) RWS. Default = 1. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = 0 if PPC = 0. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again , undefined behavior may occur if this procedure is not followed. 0 = This port is in the Powered-off state. 1 = This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' = on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a 1 to 0 (removing power from the port). Note: If this is an SSIC Port, then the DSP Disconnect process is initiated by '1' to '0' transition of PP. Refer to section 5.1.2 in the SSIC Spec for more information. Refer to section 4.19.4 for more information.
8:5	5h RW	**PLS:** Port Link State (PLS) RWS. Default = RxDetect (5). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port.
4	0h RW	**PR:** Port Reset (PR) RW1S. Default = 0. 1 = Port Reset signaling is asserted. 0 = Port is not in Reset. When software writes a 1 to this bit generating a 0 to 1 transition, the bus reset sequence is initiated ; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a 1 to this flag to transition a USB2 port from the Polling state to the Enabled state. Refer to sections 4.15.2.3 and 4.19.1.1. This flag is 0 if PP is 0.
3	0h RW	**OCA:** Over-current Active (OCA) RO. Default = 0. 1 = This port currently has an over-current condition. 0 = This port does not have an over-current condition. This bit shall automatically transition from a 1 to a 0 when the over-current condition is removed.
2	0h RO	**RSVD18:** reserved

Bit Range	Default & Access	Description
1	0h RW	**PED:** Port Enabled/Disabled (PED) RW1CS. Default = 0. 1 = Enabled. 0 = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a 1 to this flag. A port may be disabled by software writing a 1 to this flag. This flag shall automatically be cleared to 0 by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = 0) downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = 1) to transition PED to 1 and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to 1 upon the completion of successful link training. When the port is in the Disabled state, software shall write a 5 (RxDetect) to the PLS field to transition the port to the Disconnected state. Refer to section 4.19.1.2. PED shall automatically be cleared to 0 when PR is set to 1, and set to 1 when PR transitions from 1 to 0 after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a 1, it shall also write a 0 to the PR bit . This flag is 0 if PP is 0.
0	0h RW	**CCS:** Current Connect Status (CCS) ROS. Default = 0. 1 = A device is connected to the port. 0 = A device is not connected. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to 1. Refer to sections 4.19.3 and 4.19.4 for more details on the Connect Status Change (CSC) assertion conditions. This flag is 0 if PP is 0.

3.74.19 PORTPMSC1—Offset 424h

TBD

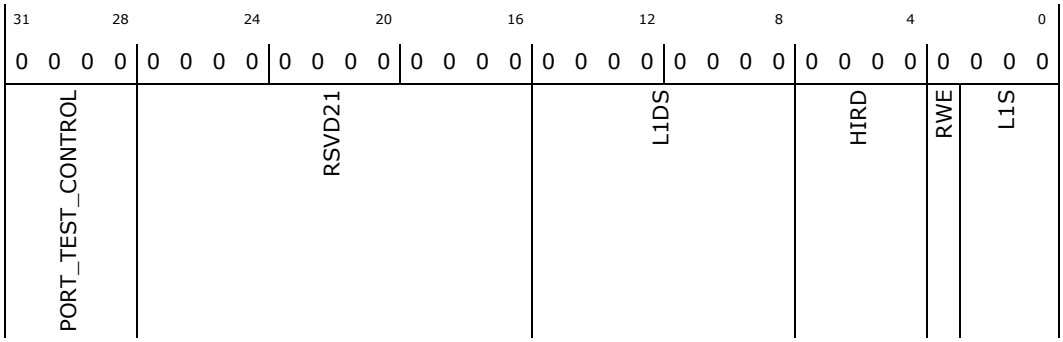
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PORTPMSC1: [BAR] + 424h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**PORT_TEST_CONTROL:** TBD
27:16	0h RO	**RSVD21:** reserved
15:8	0h RW	**L1DS:** Reg field L1DSLOT
7:4	0h RW	**HIRD:** Host Initiated Resume Duration (HIRD) - RW. Default = '0'. System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1. The HIRD value is encoded as follows: Value Description 0h 50 s. (default) 1h 125 s. 2h 200 s. Fh 1.175 ms. The value of 0000b is interpreted as 50 s. Each incrementing value up adds 75 s. to the previous value. For example, 0001b is 125 s, 0010b is 200s and so on. Based on this rule, the maximum value resume drive time is at encoding value 1111b which represents 1.2ms. Note that the HIRD field is used by both software and hardware controlled LPM. Refer to section 4.23.5.1.1 of xhci specification for more information on HIRD use. Refer to Section 4.1 of the USB2 LPM spec for more information on the use of the HIRD field.
3	0h RW	**RWE:** Port Test Control
2:0	0h RO	**L1S:** L1 Status (L1S) - RO. Default = 0. This field is used by software to determine whether an L1based suspend request (LMP transaction) was successful, specifically: Value Meaning 0 Invalid - This field shall be ignored by software. 1 Success - Port successfully transitioned to L1 (ACK) 2 Not Yet - Device is unable to enter L1 at this time (NYET) 3 Not Supported -Device does not support L1 transitions (STALL) 4 Timeout/Error -Device failed to respond to the LPM Transaction or an error occurred 5-7 Reserved The value of this field is only valid when the port resides in the L0 or L1 state (PLS = '0' or '2'). Refer to section 4.23.5.1.1 for more information.

3.74.20 PORTLI—Offset 428h

Port Link Info Register

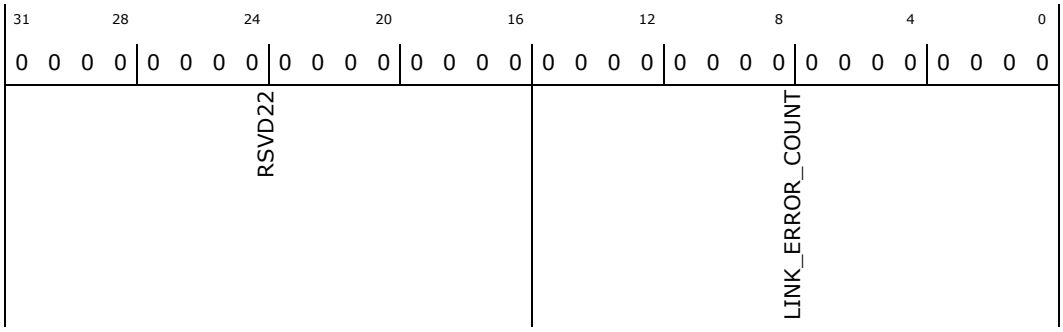
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PORTLI: [BAR] + 428h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD22:** reserved
15:0	0h RO	**LINK_ERROR_COUNT:** Reg field LINK_ERROR_COUNT

3.74.21 PORTHLPMC—Offset 42Ch

The definition of the fields in the PORTHLPMC register depend on the USB protocol supported by the port. This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST).

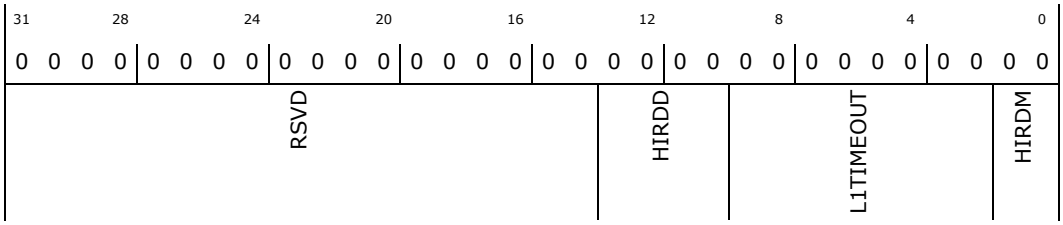
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PORTHLPMC: [BAR] + 42Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RO	**RSVD:** reserved
13:10	0h RW	**HIRDD:** Best Effort Service Latency Deep (BESLD) - RWS. Default = 0. System software sets this field to indicate to the recipient device how long the xHC will drive resume on an exit from U2. Refer to section 4.23.5.1.1.1 for more information on BESLD use. The BESLD value encoding is defined in Table 13. Refer to section 5.2.6 for information on how DBESLD may be used to establish an initial value for BESLD

Bit Range	Default & Access	Description
9:2	0h RW	**L1TIMEOUT:** L1 Timeout RWS. Default = 00h. Timeout value for the L1 inactivity timer (LPM Timer). This field shall be set to 00h by the assertion of PR to 1. Refer to section 4.23.5.1.1.1 for more information on L1 Timeout operation. The following are permissible values: for 00h 128 s. (default). for 01h 256 s. for 02h 512 s. for 03h 768 s. . . . for FFh 65,280 s.
1:0	0h RW	**HIRDM:** Host Initiated Resume Duration Mode (HIRDM) - RWS. Default = 0h. Indicates which HIRD value should be used. The following are permissible values: for 0 Initiate L1 using BESL only on timeout. (default). for 1 Initiate L1 using BESLD on timeout. If rejected by device, initiate L1 using BESL. for 3-2 Reserved.

3.74.22 PORTSC2—Offset 430h

A host controller shall implement one or more port registers. The number of port registers implemented by a particular instantiation of a host controller is documented in the HCSPARAMS1 register (Section 5.3.3). Software uses this information as an input parameter to determine how many ports need to be serviced

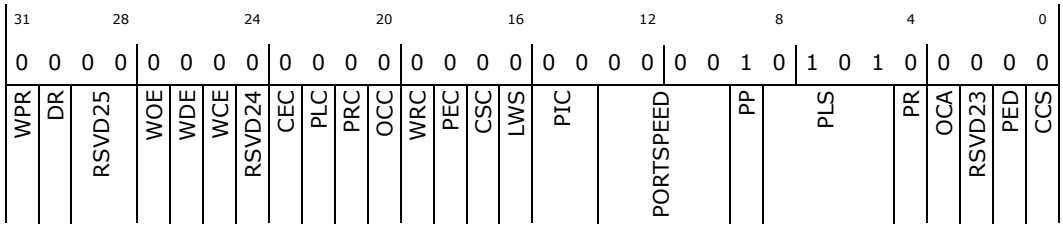
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

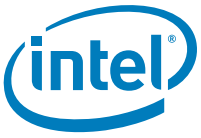
PORTSC2: [BAR] + 430h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

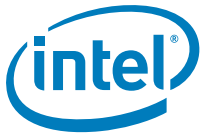
Default: 000002A0h



Bit Range	Default & Access	Description
31	0h RW	**WPR:** Warm Port Reset (WPR) RW1S/RsvdZ. Default = 0. When software writes a 1 to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to 1. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return 0 when read. Refer to section 4.19.5.1. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
30	0h RW	**DR:** Device Removable (DR) - RO. This flag indicates if this port has a removable device attached. 1 = Device is non-removable. 0 = Device is removable.
29:28	0h RO	**RSVD25:** reserved



Bit Range	Default & Access	Description
27	0h RW	**WOE:** Wake on Over-current Enable (WOE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to over-current conditions as system wake-up eventsn. Refer to section 4.15 for operational model.
26	0h RW	**WDE:** Wake on Disconnect Enable (WDE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to device disconnects as system wake-up eventsn. Refer to section 4.15 for operational model.
25	0h RW	**WCE:** Wake on Connect Enable (WCE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to device connects as system wake-up events . Refer to section 4.15 for operational model.
24	0h RO	**RSVD24:** reserved
23	0h RW	**CEC:** Port Config Error Change (CEC) RW1CS/RsvdZ. Default = 0. This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 of XHCI specification for more information on change bit usage. Note: This flag is valid only for USB3 protocol ports. For USB2 protocol ports this bit shall be RsvdZ.
22	0h RW	**PLC:** Port Link State Change (PLC) RW1CS. Default = 0. This flag is set to 1 due to the PLS transitions in the XHCI specification
21	0h RW	**PRC:** Port Reset Change (PRC) RW1CS. Default = 0. This flag is set to 1 due to a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to 1 if the reset processing was forced to terminate due to software clearing PP or PED to '0'. 0 = No change. 1 = Reset complete. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5.of XHCI specification. Refer to section 4.19.2 of XHCI specification. for more information on change bit usage.
20	0h RW	**OCC:** Over-current Change (OCC) RW1CS. Default = 0. This bit shall be set to a 1 when there is a 0 to 1 or 1 to 0 transition of Over-current Active (OCA). Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage.
19	0h RW	**WRC:** Warm Port Reset Change (WRC) RW1CS/RsvdZ. Default = 0. This bit is set when Warm Reset processing on this port completes. 0 = No change. 1 = Warm Reset complete. Note that this flag shall not be set to 1 if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5.1. Refer to section 4.19.2 for more information on change bit usage. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
18	0h RW	**PEC:** Port Enabled/Disabled Change (PEC) RW1CS. Default = 0. 1 = change in PED. 0 = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to 0. Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage. For a USB2 protocol port, this bit shall be set to 1 only when the port is disabled due to the appropriate conditions existing at the EOF2 point (refer to section 11.8.1 of the USB2 Specification for the definition of a Port Error). For a USB3 protocol port, this bit shall never be set to 1.



Bit Range	Default & Access	Description
17	0h RW	**CSC:** Connect Status Change (CSC) RW1CS. Default = 0. 1 = Change in CCS. 0 = No change. This flag indicates a change has occurred in the ports Current Connect Status (CCS) or Cold Attach Status (CAS) bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to 0, or the CAS transition was due to software setting WPR to 1. The xHC sets this bit to 1 for all changes to the port device connect status , even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be setting an already-set bit (i.e., the bit will remain 1). Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage.
16	0h RW	**LWS:** Port Link State Write Strobe (LWS) RW. Default = 0. When this bit is set to 1 on a write reference to this register, this flag enables writes to the PLS field. When 0, write data in PLS field is ignored. Reads to this bit return 0.
15:14	0h RW	**PIC:** Port Indicator Control (PIC) RWS. Default = 0. Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a 0
13:10	0h RW	**PORTSPEED:** Port Speed (Port Speed) ROS. Default = 0. This field identifies the speed of the connected USB Device. This field is only relevant if a device is connected (CCS = 1) in all other cases this field shall indicate Undefined Speed.
9	1h RW	**PP:** Port Power (PP) RWS. Default = 1. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = 0 if PPC = 0. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again , undefined behavior may occur if this procedure is not followed. 0 = This port is in the Powered-off state. 1 = This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' = on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a 1 to 0 (removing power from the port). Note: If this is an SSIC Port, then the DSP Disconnect process is initiated by '1' to '0' transition of PP. Refer to section 5.1.2 in the SSIC Spec for more information. Refer to section 4.19.4 for more information.
8:5	5h RW	**PLS:** Port Link State (PLS) RWS. Default = RxDetect (5). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port.

Bit Range	Default & Access	Description
4	0h RW	**PR:** Port Reset (PR) RW1S. Default = 0. 1 = Port Reset signaling is asserted. 0 = Port is not in Reset. When software writes a 1 to this bit generating a 0 to 1 transition, the bus reset sequence is initiated ; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a 1 to this flag to transition a USB2 port from the Polling state to the Enabled state. Refer to sections 4.15.2.3 and 4.19.1.1. of XHCI specification. This flag is 0 if PP is 0.
3	0h RW	**OCA:** Over-current Active (OCA) RO. Default = 0. 1 = This port currently has an over-current condition. 0 = This port does not have an over-current condition. This bit shall automatically transition from a 1 to a 0 when the over-current condition is removed.
2	0h RO	**RSVD23:** reserved
1	0h RW	**PED:** Port Enabled/Disabled (PED) RW1CS. Default = 0. 1 = Enabled. 0 = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a 1 to this flag. A port may be disabled by software writing a 1 to this flag. This flag shall automatically be cleared to 0 by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = 0) downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = 1) to transition PED to 1 and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to 1 upon the completion of successful link training. When the port is in the Disabled state, software shall write a 5 (RxDetect) to the PLS field to transition the port to the Disconnected state. Refer to section 4.19.1.2. of xhci specification. PED shall automatically be cleared to 0 when PR is set to 1, and set to 1 when PR transitions from 1 to 0 after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a 1, it shall also write a 0 to the PR bit. This flag is 0 if PP is 0.
0	0h RW	**CCS:** Current Connect Status (CCS) ROS. Default = 0. 1 = A device is connected to the port. 0 = A device is not connected. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to 1. Refer to sections 4.19.3 and 4.19.4 for more details on the Connect Status Change (CSC) assertion conditions. This flag is 0 if PP is 0.

3.74.23 PORTPMSC2—Offset 434h

TBD

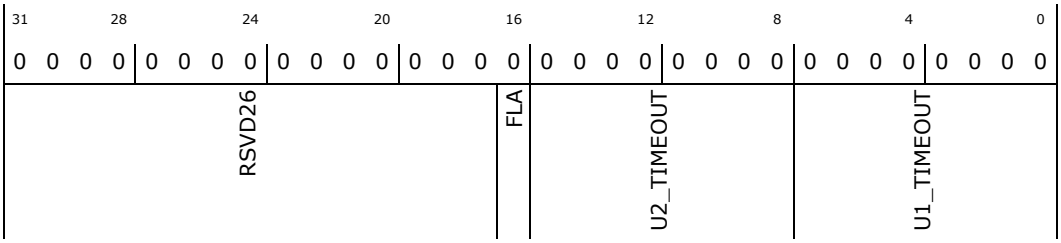
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PORTPMSC2: [BAR] + 434h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:17	0h RO	**RSVD26:** reserved
16	0h RW	**FLA:** Reg field FLA
15:8	0h RW	**U2_TIMEOUT:** Reg field U2_TIMEOUT
7:0	0h RW	**U1_TIMEOUT:** Reg field U1_TIMEOUT

3.74.24 MFINDEX—Offset 440h

Microframe Index Register Bit Definitions.

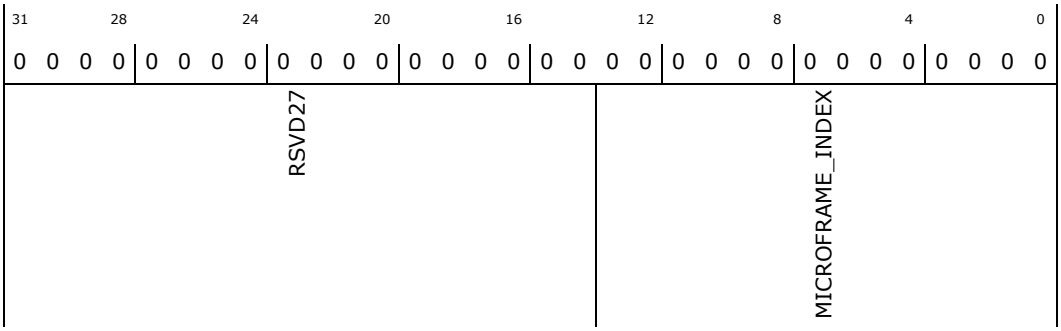
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MFINDEX: [BAR] + 440h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RO	**RSVD27:** reserved
13:0	0h RO	**MICROFRAME_INDEX:** Reg field MICROFRAME_INDEX

3.74.25 RsvdZ—Offset 444h

reserved

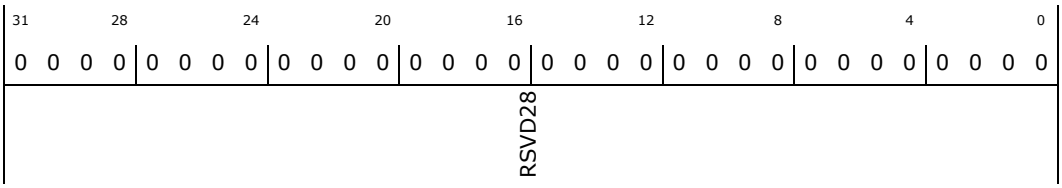
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RsvdZ: [BAR] + 444h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**RSVD28:** reserved

3.74.26 IMAN—Offset 460h

Interrupter Management Register Bit Definitions.

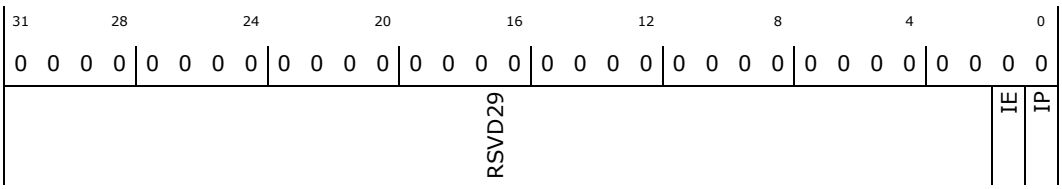
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IMAN: [BAR] + 460h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**RSVD29:** reserved
1	0h RW	**IE:** Interrupt Enable (IE) RW. Default = 0. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set (1), the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is 0, then the Interrupter is prohibited from generating interrupts.
0	0h RW	**IP:** Interrupt Pending (IP) - RW1C. Default = 0. This flag represents the current state of the Interrupter. If IP = 1, an interrupt is pending for this Interrupter. A 0 value indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.5 of XHCI specification for the conditions that modify the state of this flag.

3.74.27 IMOD—Offset 464h

Interrupter Moderation Register. Software may use this register to pace (or even out) the delivery of interrupts to the host CPU. This register provides a guaranteed inter-interrupt delay between interrupts asserted by the xHC, regardless of USB traffic conditions. To independently validate configuration settings, software may use the following algorithm to convert the inter-interrupt Interval value to the common 'interrupts/sec' performance metric:

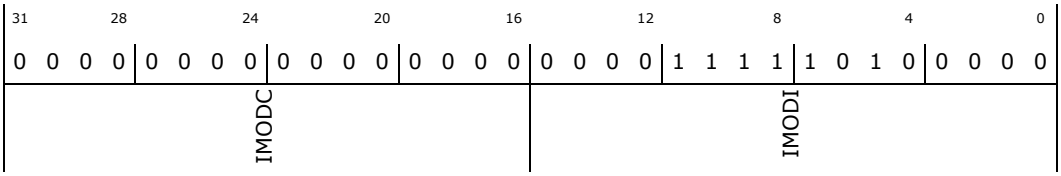
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IMOD: [BAR] + 464h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000FA0h



Bit Range	Default & Access	Description
31:16	0h RW	**IMODC:** Interrupt Moderation Counter (IMODC) - RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate.
15:0	fa0h RW	**IMODI:** Interrupt Moderation Interval (IMODI) - RW. Default = '4000' (~1ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty.

3.74.28 ERSTSZ—Offset 468h

Event Ring Segment Table Size Register Bit Definitions.

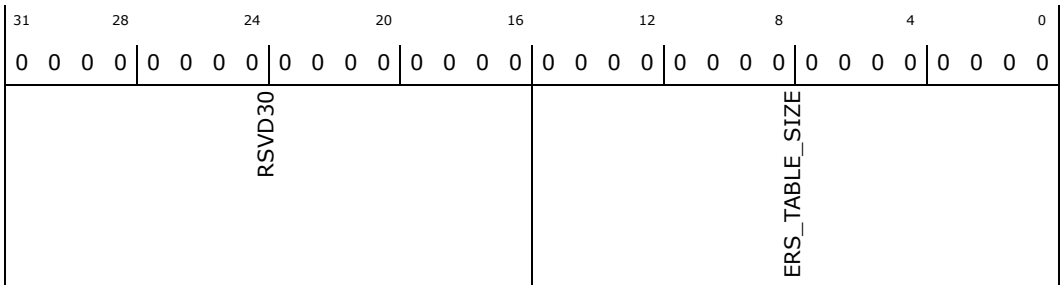
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTSZ: [BAR] + 468h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD30:** reserved
15:0	0h RW	**ERS_TABLE_SIZE:** Event Ring Segment Table Size RW. Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register (5.3.4). For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled.

3.74.29 RsvdP—Offset 46Ch

reserved

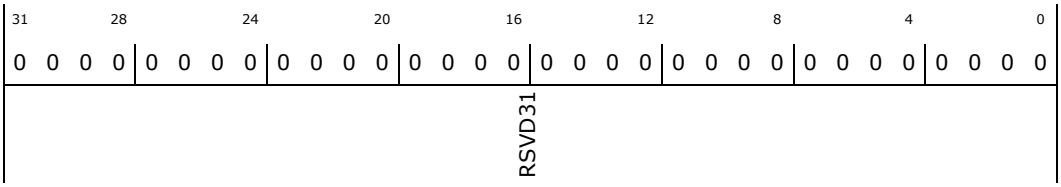
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RsvdP: [BAR] + 46Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**RSVD31:** reserved

3.74.30 ERSTBA_LO—Offset 470h

Register ERSTBA_LO

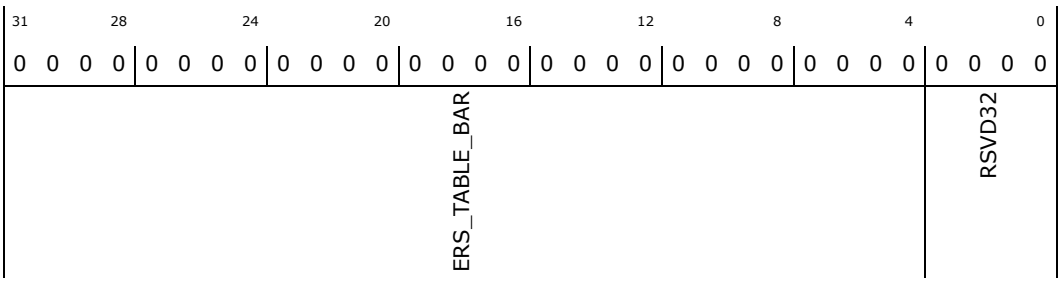
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_LO: [BAR] + 470h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**ERS_TABLE_BAR:** Reg field ERS_TABLE_BAR
3:0	0h RO	**RSVD32:** reserved

3.74.31 ERSTBA_HI—Offset 474h

Register ERSTBA_HI

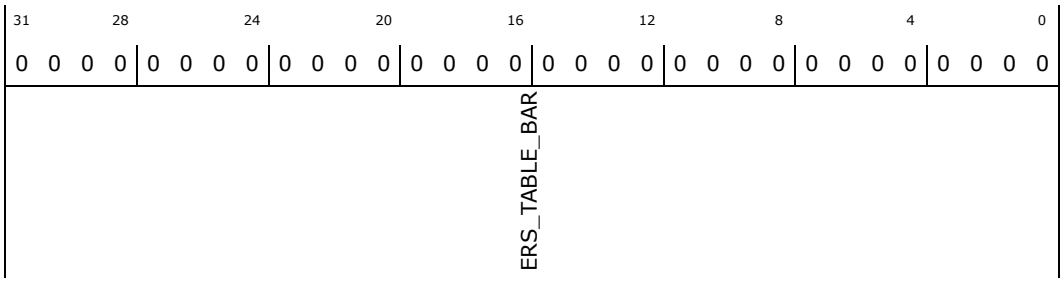
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_HI: [BAR] + 474h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**ERS_TABLE_BAR:** Reg field ERS_TABLE_BAR

3.74.32 ERDP_LO—Offset 478h

Register ERDP_LO

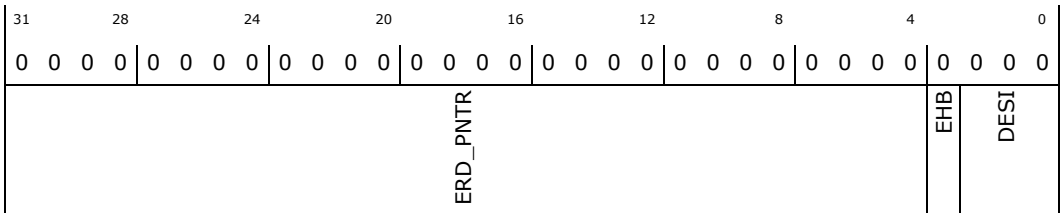
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_LO: [BAR] + 478h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**ERD_PNTR:** Reg field ERD_PNTR
3	0h RW	**EHB:** HC OS Owned Semaphore HC BIOS Owned Semaphore USB SMI Enable SMI on Host System Error Enable SMI on OS Ownership Enable SMI on PCI Command Enable SMI on BAR Enable SMI on Event Interrupt SMI on Host System Error SMI on OS Ownership Change SMI on PCI Command SMI on BAR Compatible Port Count HC OS Owned Semaphore HC BIOS Owned Semaphore USB SMI Enable SMI on Host System Error Enable SMI on OS Ownership Enable SMI on PCI Command Enable SMI on BAR Enable SMI on Event Interrupt SMI on Host System Error SMI on OS Ownership Change SMI on PCI Command SMI on BAR Compatible Port Count

Bit Range	Default & Access	Description
2:0	0h RW	**DESI:** Dequeue ERST Segment Index (DESI) RW. Default = 0. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in.

3.74.33 ERDP_HI—Offset 47Ch

Register ERDP_HI

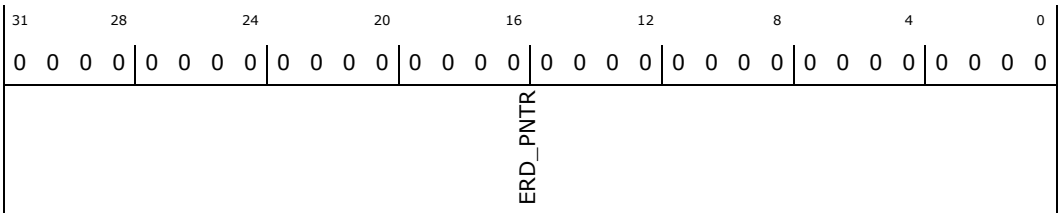
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_HI: [BAR] + 47Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**ERD_PNTR:** Reg field ERD_PNTR

3.74.34 DB_0—Offset 480h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

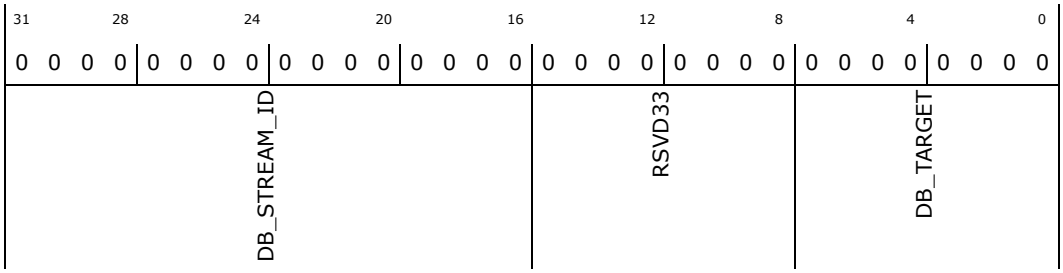
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_0: [BAR] + 480h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.35 DB_1—Offset 484h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

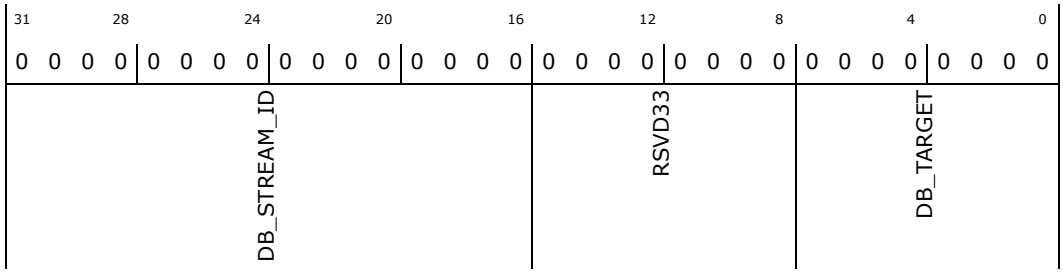
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_1: [BAR] + 484h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.36 DB_2—Offset 488h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

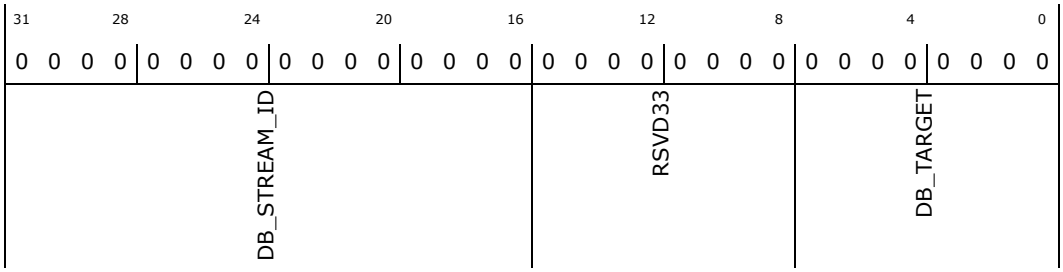
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_2: [BAR] + 488h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.37 DB_3—Offset 48Ch

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

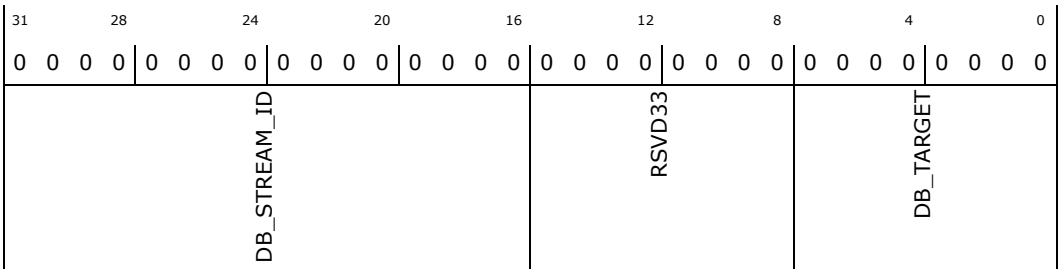
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_3: [BAR] + 48Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.38 DB_4—Offset 490h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

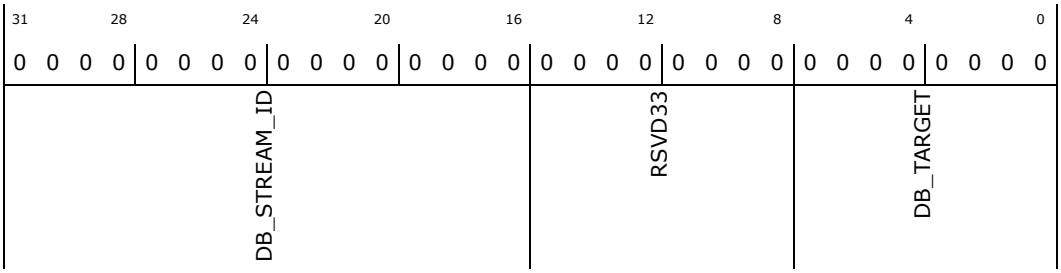
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_4: [BAR] + 490h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.39 DB_5—Offset 494h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

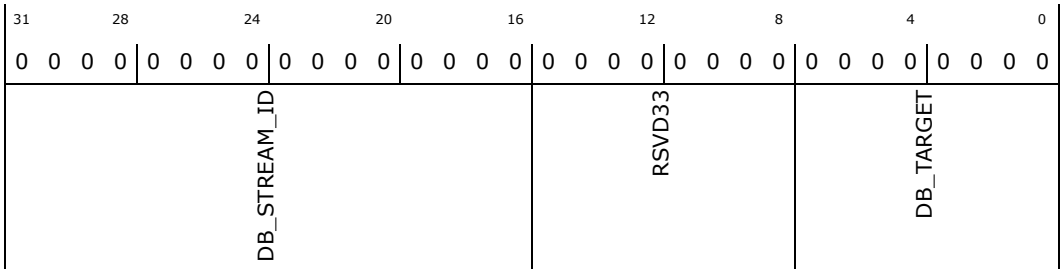
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_5: [BAR] + 494h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.40 DB_6—Offset 498h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

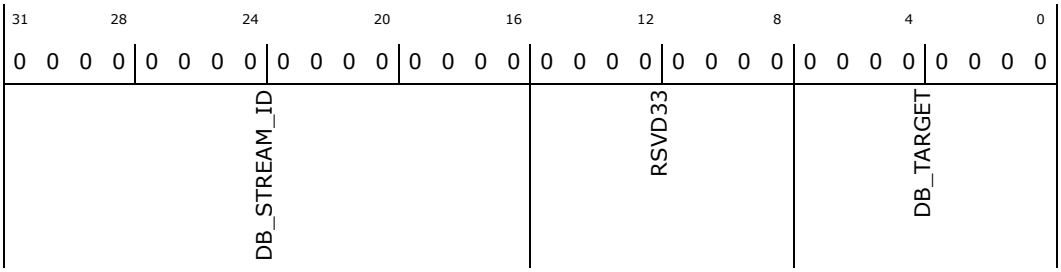
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_6: [BAR] + 498h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.41 DB_7—Offset 49Ch

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

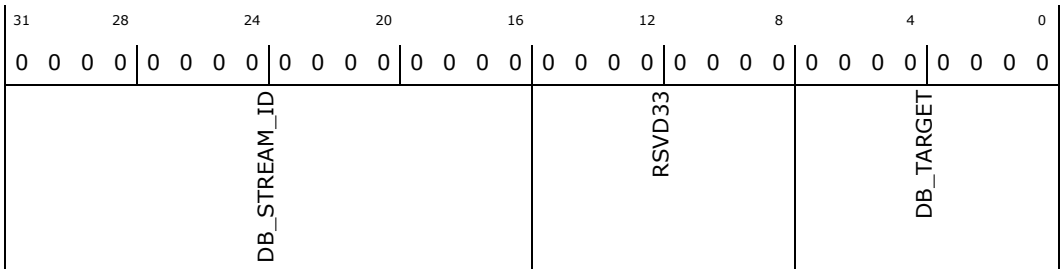
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_7: [BAR] + 49Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.42 DB_8—Offset 4A0h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

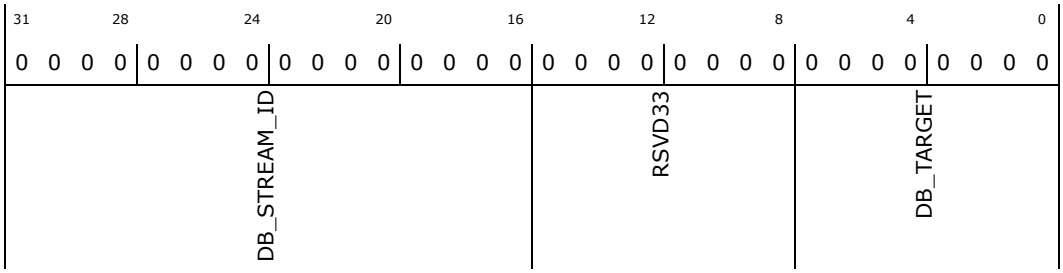
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_8: [BAR] + 4A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.43 DB_9—Offset 4A4h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

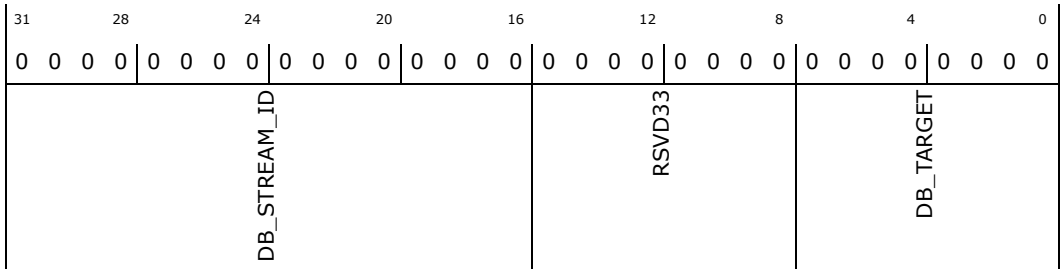
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_9: [BAR] + 4A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.44 DB_10—Offset 4A8h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

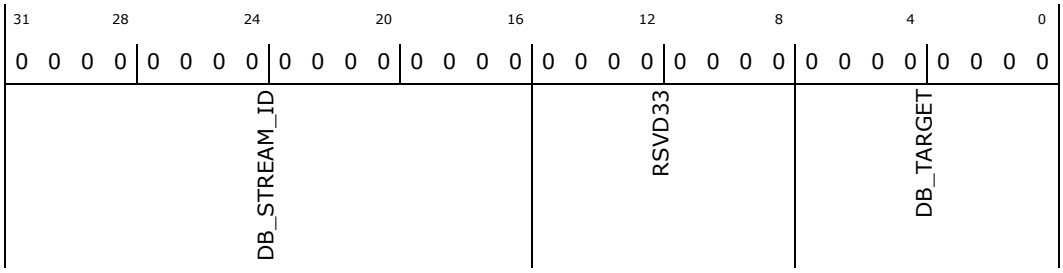
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_10: [BAR] + 4A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.45 DB_11—Offset 4ACh

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

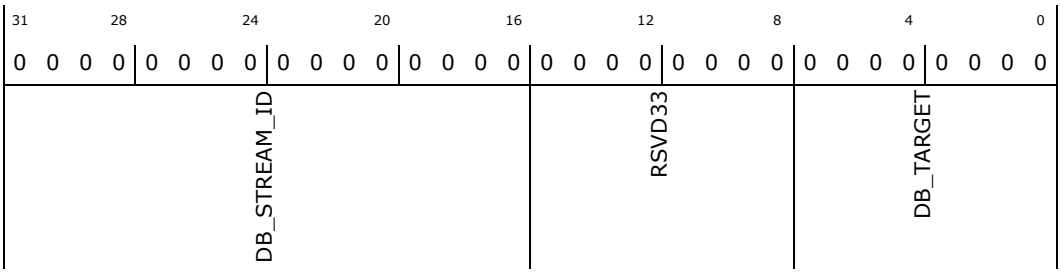
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_11: [BAR] + 4ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.46 DB_12—Offset 4B0h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

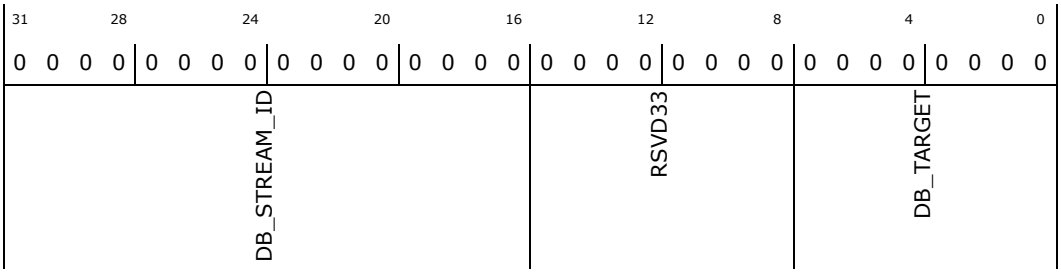
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_12: [BAR] + 4B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.47 DB_13—Offset 4B4h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

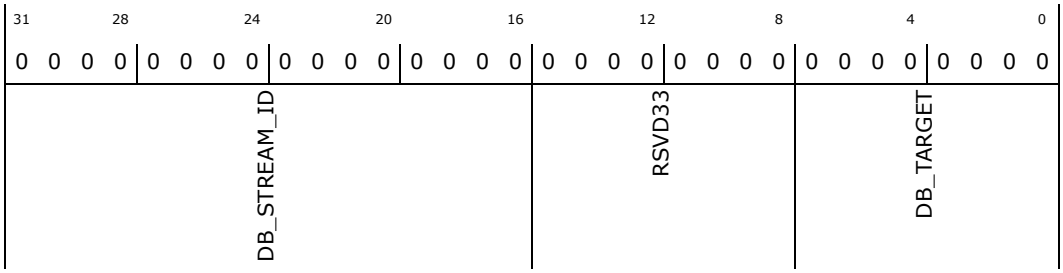
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_13: [BAR] + 4B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.48 DB_14—Offset 4B8h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

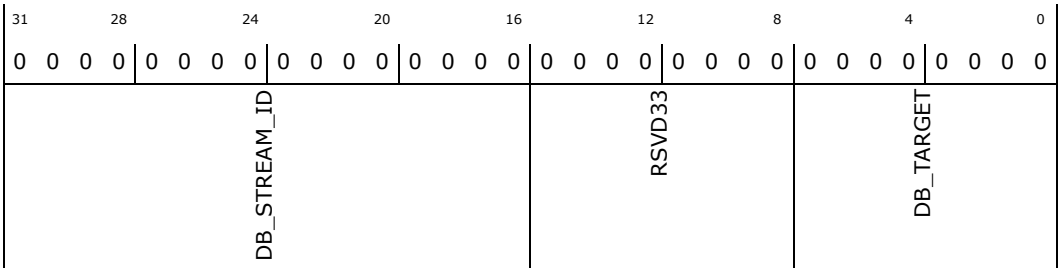
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_14: [BAR] + 4B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.49 DB_15—Offset 4BCh

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

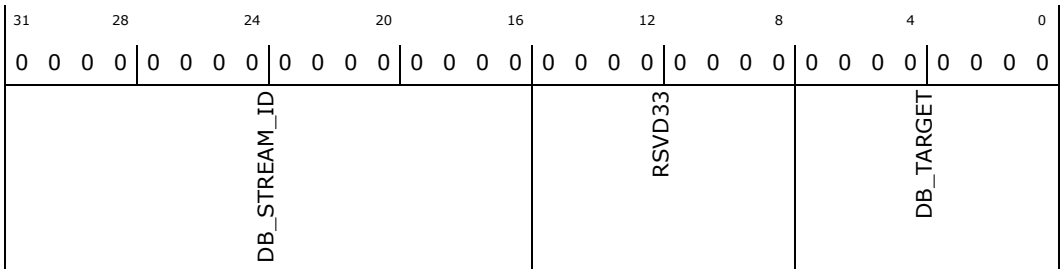
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_15: [BAR] + 4BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.50 DB_16—Offset 4C0h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

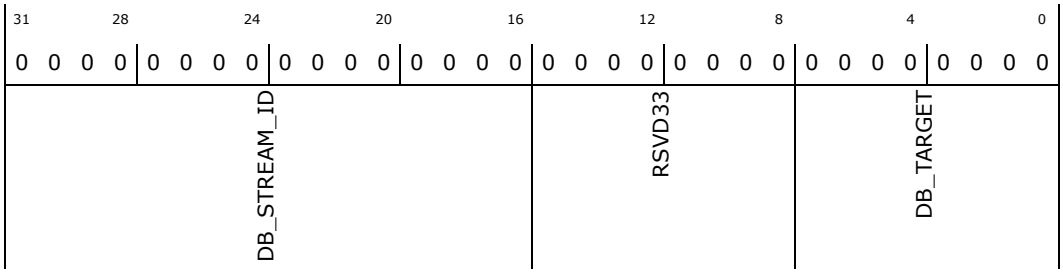
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_16: [BAR] + 4C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

3.74.51 USBLEGSUP—Offset 880h

The USBLEGSUP capability requires support for Byte accesses for Semaphore address, refer to section 7.1.of xhci specification. usb legacy support capability DW

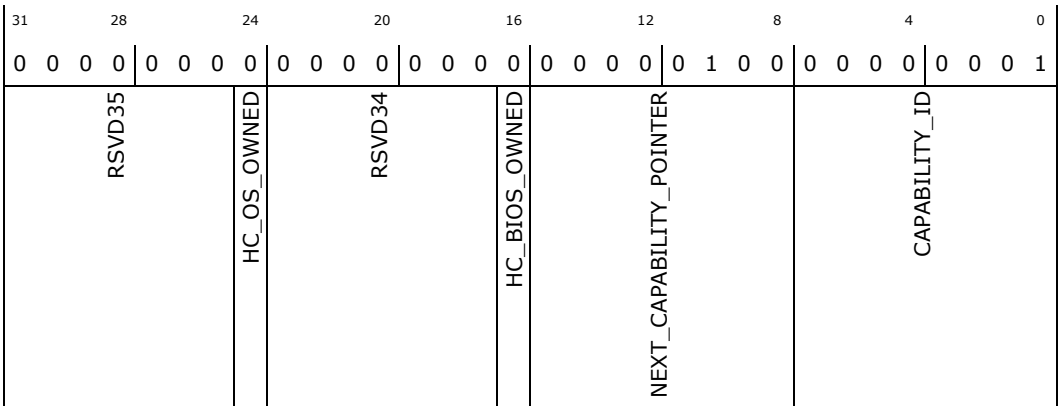
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

USBLEGSUP: [BAR] + 880h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000401h



Bit Range	Default & Access	Description
31:25	0h RO	**RSVD35:** reserved
24	0h RW	**HC_OS_OWNED:** Reg field HC_OS_OWNED SEMAPHORE
23:17	0h RO	**RSVD34:** reserved
16	0h RW	**HC_BIOS_OWNED:** Reg field HC_BIOS_OWNED SEMAPHORE
15:8	04h RO	**NEXT_CAPABILITY_POINTER:** Reg field NEXT_CAPABILITY_POINTER
7:0	01h RO	**CAPABILITY_ID:** Reg field CAPABILITY_ID

3.74.52 USBLEGCTLSTS—Offset 884h

usb legacy support capability DW

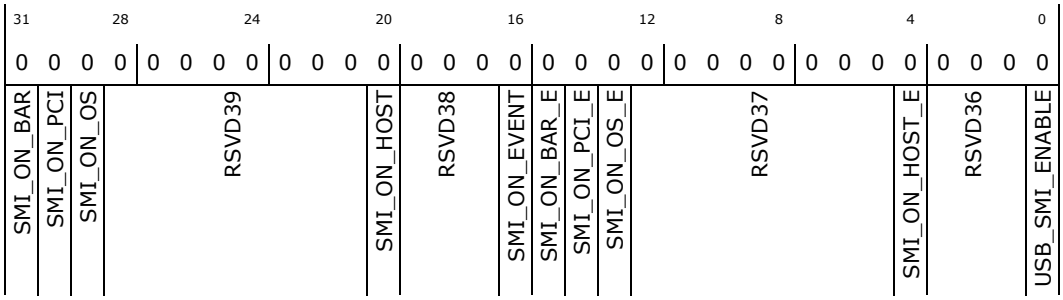
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

USBLEGCTLSTS: [BAR] + 884h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RO	**SMI_ON_BAR:** Reg field SMI_ON_BAR
30	0h RO	**SMI_ON_PCI:** Reg field SMI_ON_PCI COMMAND
29	0h RO	**SMI_ON_OS:** Reg field SMI_ON_OS OWNERSHIP CHANGE
28:21	0h RO	**RSVD39:** reserved
20	0h RO	**SMI_ON_HOST:** Reg field SMI_ON_HOST SYSTEM ERROR
19:17	0h RO	**RSVD38:** reserved
16	0h RO	**SMI_ON_EVENT:** Reg field SMI_ON_EVENT INTERRUPT
15	0h RW	**SMI_ON_BAR_E:** Reg field SMI_ON_BAR ENABLE
14	0h RW	**SMI_ON_PCI_E:** Reg field SMI_ON_PCI COMMAND ENABLE
13	0h RW	**SMI_ON_OS_E:** Reg field SMI_ON_OS OWNERSHIP ENABLE
12:5	0h RO	**RSVD37:** Reserved
4	0h RW	**SMI_ON_HOST_E:** Reg field SMI_ON_HOST SYSTEM ERROR ENABLE
3:1	0h RO	**RSVD36:** Reserved
0	0h RW	**USB_SMI_ENABLE:** Reg field USB_SMI_ENABLE

3.74.53 SUPTPRT2_DW0—Offset 890h

usb legacy support capability DW

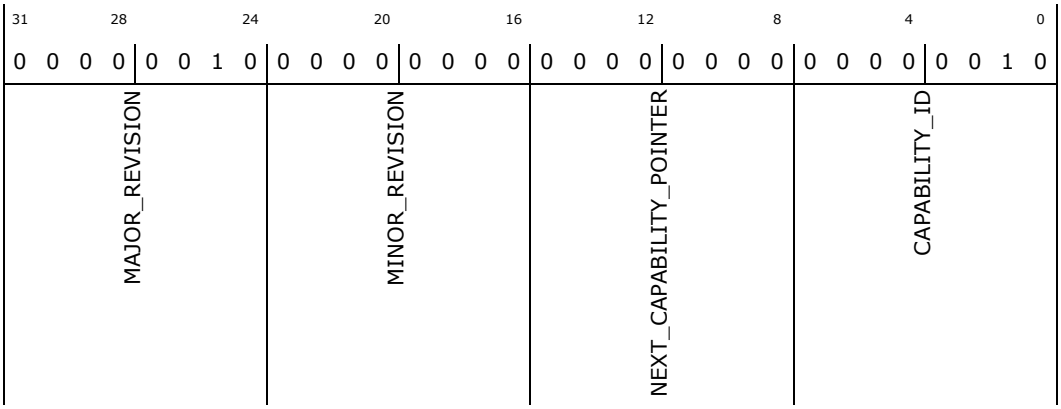
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SUPTPRT2_DW0: [BAR] + 890h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 02000002h



Bit Range	Default & Access	Description
31:24	02h RW	**MAJOR_REVISION:** Reg field MAJOR_REVISION
23:16	0h RW	**MINOR_REVISION:** Reg field MINOR_REVISION
15:8	0h RW	**NEXT_CAPABILITY_POINTER:** Reg field NEXT_CAPABILITY_POINTER
7:0	02h RW	**CAPABILITY_ID:** reg field CAPABILITY_ID

3.74.54 SUPTPRT2_DW1—Offset 894h

Register SUPTPRT2_DW1

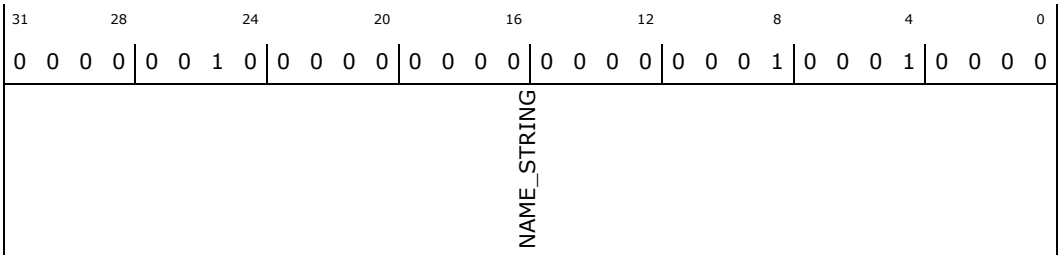
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SUPTPRT2_DW1: [BAR] + 894h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 02000110h



Bit Range	Default & Access	Description
31:0	02000110h RW	**NAME_STRING:** Reg field NAME_STRING

3.74.55 SUPTPRT2_DW2—Offset 898h

flag Value After Reset: 0x0 Register SUPTPRT2_DW2

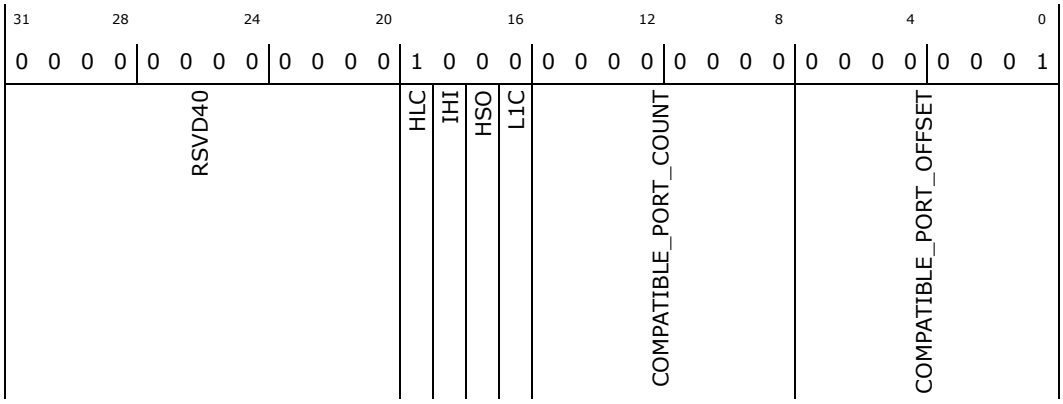
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SUPTPRT2_DW2: [BAR] + 898h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00080001h



Bit Range	Default & Access	Description
31:20	0000h RO	**RSVD40:** reserved
19	1h RO	**HLC:** Hardware LMP capability (HLC) RO.when XHCI 100 - Default = 1'b1. when XHCI 096 - Default = 1'b0 . If this bit is set to 1, the ports described by this xHCI supported Protocol Capability support hardware controlled USB2 Link Power Management. Refer to section 4.23.5.1.1.1.
18	0h RO	**IHI:** Integrated Hub Implementation (IHI) RO. Default = 1'b0. If this bit is cleared to 0, the Root Hub to External xHC port mapping adheres to the default mapping described in section 4.24.2.1. if this bit is set to 1, the Root Hub to External xHc port mapping does not adhere to the default mapping described in section 4.24.2.1, and an ACPI or other mechanism is required to define the mapping
17	0h RO	**HSO:** High-speed Only (HSO) RO. Default = 1'b0. If this bit is cleared to 0 the USB2 ports described by this capability are Low-, Full-, and high speed capable. If this bit is set to 1, the USB2 ports described by this capability are High-speed only, e.g. the ports do not support Low- or Full-Speed operation. High-speed only implementations may introduce a Tier mismatch, refer to section 4.24.2 for more information.

Bit Range	Default & Access	Description
16	0h RW	**L1C:** Reserved
15:8	0h RW	**COMPATIBLE_PORT_COUNT:** Reg field COMPATIBLE_PORT_COUNT
7:0	01h RW	**COMPATIBLE_PORT_OFFSET:** Reg field COMPATIBLE_PORT_OFFSET

3.74.56 SUPTPRT3_DW0—Offset 8A0h

flag Value After Reset: 0x0 Register SUPTPRT3_DW0

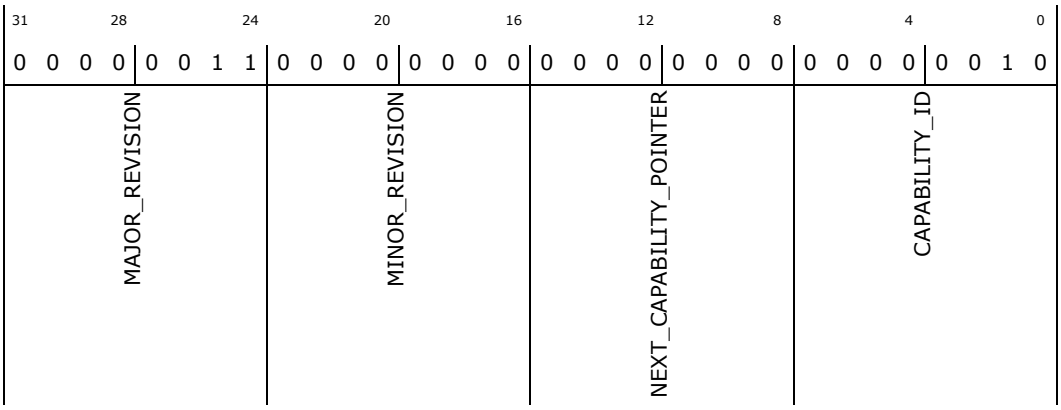
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SUPTPRT3_DW0: [BAR] + 8A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 03000002h



Bit Range	Default & Access	Description
31:24	0x03 RW	**MAJOR_REVISION:** 0x0 Reg field MAJOR_REVISION
23:16	00h RW	**MINOR_REVISION:** flag Value After Reset: 0x0 Reg field MINOR_REVISION
15:8	0h RW	**NEXT_CAPABILITY_POINTER:** Reg field NEXT_CAPABILITY_POINTER
7:0	02h RW	**CAPABILITY_ID:** Reg field CAPABILITY_ID

3.74.57 SUPTPRT3_DW1—Offset 8A4h

Register SUPTPRT3_DW1

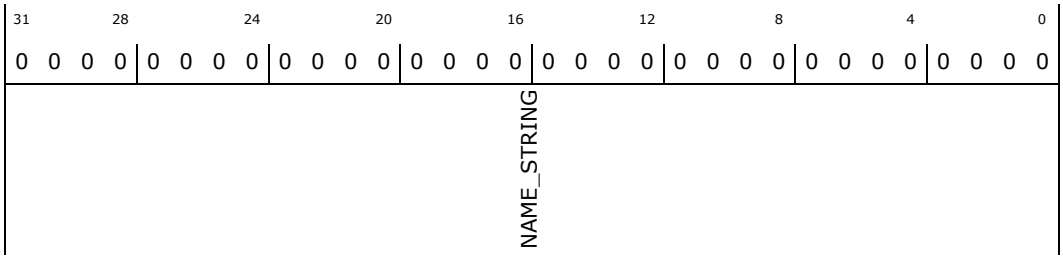
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SUPTPRT3_DW1: [BAR] + 8A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**NAME_STRING:** field NAME_STRING

3.74.58 SUPTPRT3_DW2—Offset 8A8h

0x0 Register SUPTPRT3_DW2

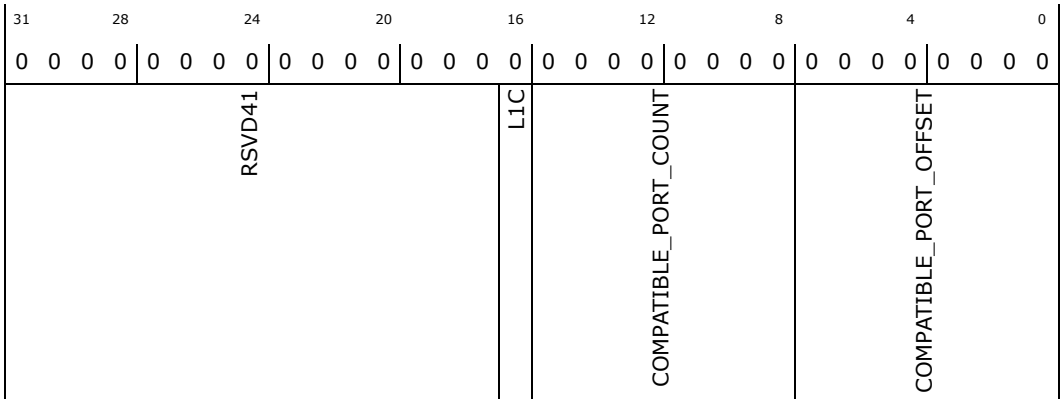
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SUPTPRT3_DW2: [BAR] + 8A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:17	0h RO	**RSVD41:** reserved

Bit Range	Default & Access	Description
16	0h RW	**L1C:** TBD
15:8	0h RW	**COMPATIBLE_PORT_COUNT:** Reg field COMPATIBLE_PORT_COUNT
7:0	0h RW	**COMPATIBLE_PORT_OFFSET:** 0x0 Reg field COMPATIBLE_PORT_OFFSET

3.74.59 DCID—Offset 8B0h

Debug capability is not supported

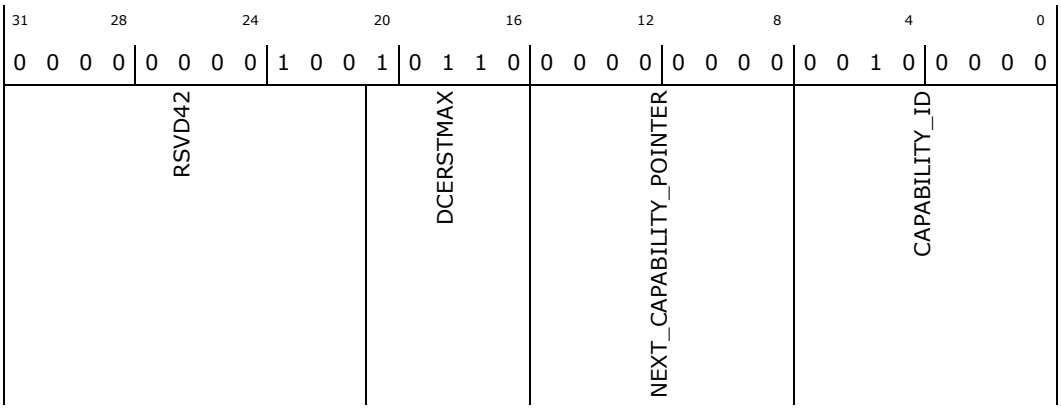
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCID: [BAR] + 8B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00960020h



Bit Range	Default & Access	Description
31:21	4h RO	**RSVD42:** reserved
20:16	16h RW	**DCERSTMAX:** TBD
15:8	0h RW	**NEXT_CAPABILITY_POINTER:** Reg field NEXT_CAPABILITY_POINTER
7:0	20h RW	**CAPABILITY_ID:** Reg field CAPABILITY_ID

3.74.60 DCDB—Offset 8B4h

Debug capability is not supported

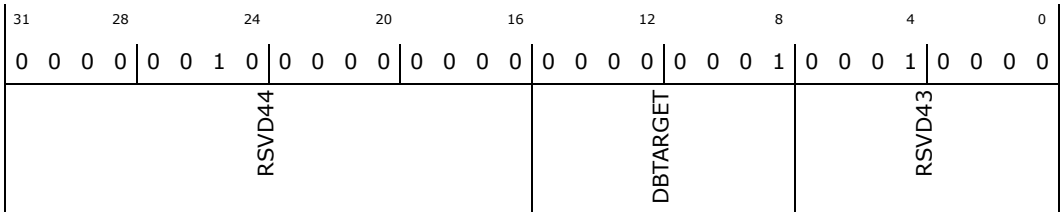
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCDB: [BAR] + 8B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 02000110h



Bit Range	Default & Access	Description
31:16	0200h RO	**RSVD44:** TBD
15:8	01h RW	**DBTARGET:** TBD
7:0	10h RO	**RSVD43:** reserved

3.74.61 DCERSTSZ—Offset 8B8h

Debug capability is not supported

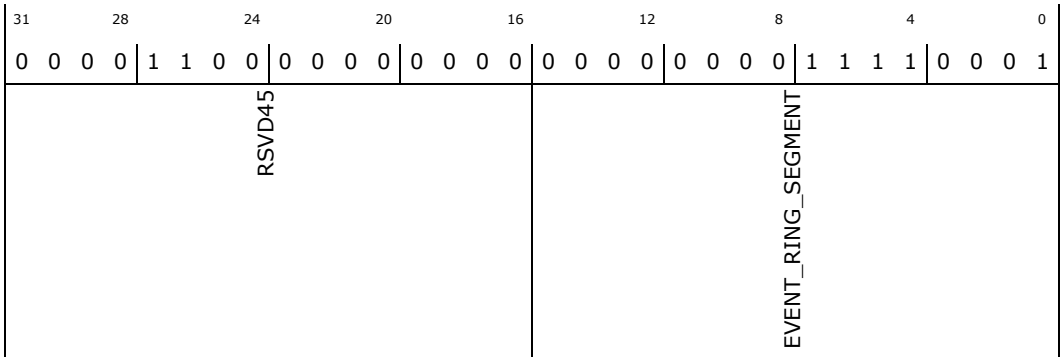
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCERSTSZ: [BAR] + 8B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0C0000F1h



Bit Range	Default & Access	Description
31:16	0c00h RO	**RSVD45:** TBD
15:0	00f1h RW	**EVENT_RING_SEGMENT:** TBD

3.74.62 DCERSTBA_LO—Offset 8BCh

Debug capability is not supported

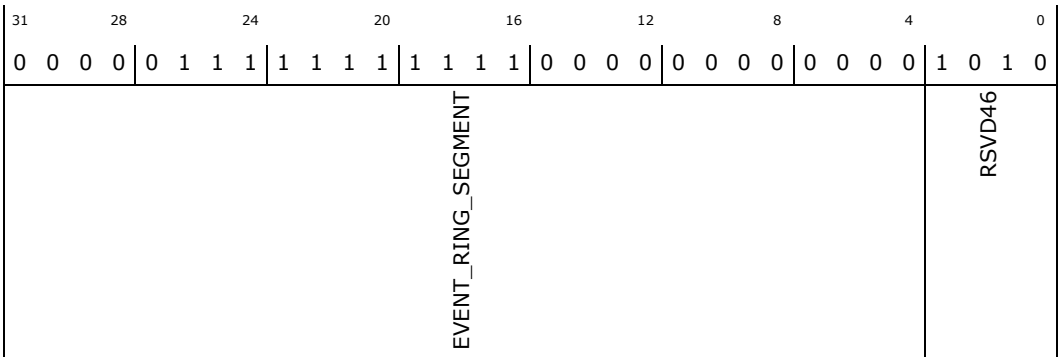
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCERSTBA_LO: [BAR] + 8BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 07FF000Ah



Bit Range	Default & Access	Description
31:4	07ff000h RW	**EVENT_RING_SEGMENT:** TBD
3:0	ah RO	**RSVD46:** TBD

3.74.63 DCERSTBA_HI—Offset 8C0h

Debug capability is not supported

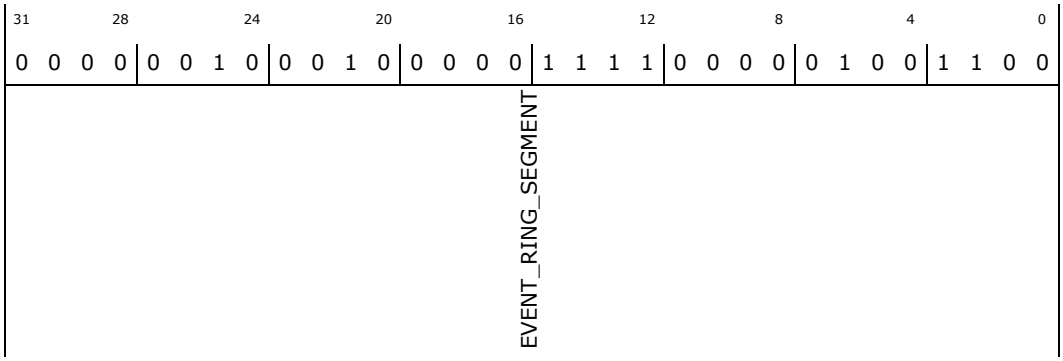
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCERSTBA_HI: [BAR] + 8C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0220F04Ch



Bit Range	Default & Access	Description
31:0	0220f04ch RW	**EVENT_RING_SEGMENT:** TBD

3.74.64 DCERDP_LO—Offset 8C4h

Debug capability is not supported

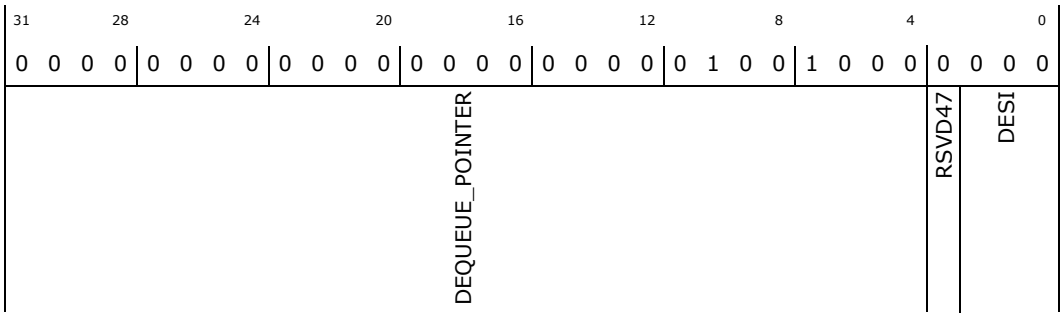
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCERDP_LO: [BAR] + 8C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000480h



Bit Range	Default & Access	Description
31:4	48h RW	**DEQUEUE_POINTER:** Reserved.
3	0h RO	**RSVD47:** TBD
2:0	0h RW	**DESI:** TBD

3.74.65 DCERDP_HI—Offset 8C8h

Debug capability is not supported

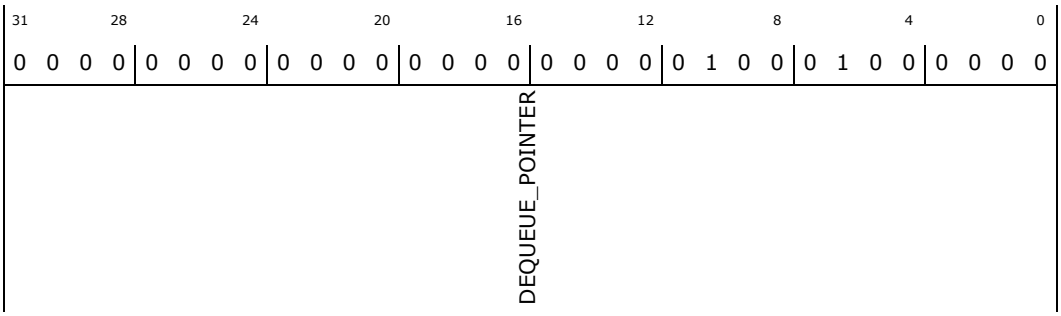
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCERDP_HI: [BAR] + 8C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000440h



Bit Range	Default & Access	Description
31:0	440h RW	**DEQUEUE_POINTER:** TBD

3.74.66 DCCTRL—Offset 8CCh

Debug capability is not supported

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCCTRL: [BAR] + 8CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bit Range	Default & Access	Description
31	0h RW	**DCE:** TBD
30:24	0h RW	**DEVICE_ADDRESS:** TBD
23:16	0h RW	**DEBUG_PROTOCOL:** TBD
15:4	0h RO	**RSVD48:** TBD
3	0h RW	**HIT:** TBD
2	0h RW	**HOT:** TBD
1	0h RW	**LSE:** TBD
0	0h RW	**DCR:** TBD

3.74.67 DCSTAT—Offset 8D0h

Debug capability is not supported

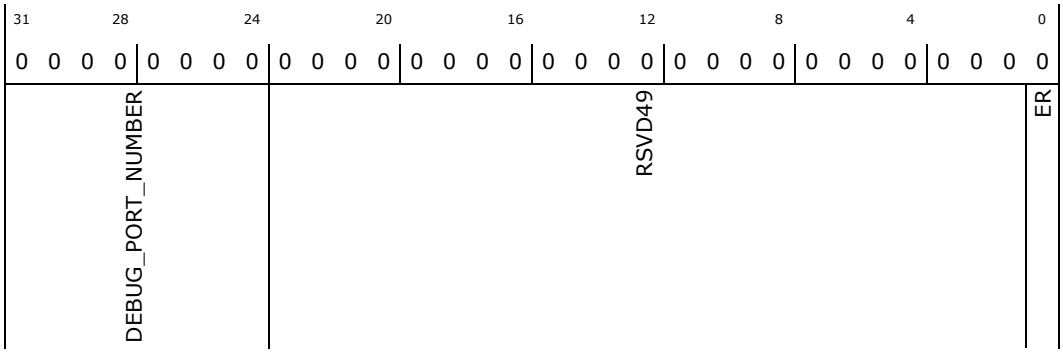
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCSTAT: [BAR] + 8D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**DEBUG_PORT_NUMBER:** TBD
23:1	0h RO	**RSVD49:** TBD

Bit Range	Default & Access	Description
0	0h RW	**ER:** TBD

3.74.68 DCPORTSC—Offset 8D4h

Debug capability is not supported

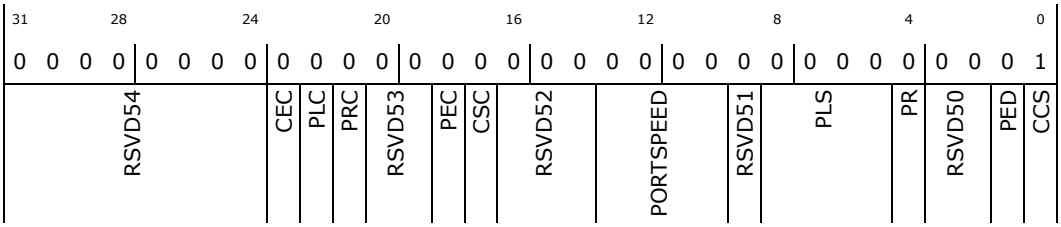
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCPORTSC: [BAR] + 8D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:24	0h RO	**RSVD54:** TBD
23	0h RW	**CEC:** Reg field CEC
22	0h RW	**PLC:** Reg field PLC
21	0h RW	**PRC:** 0x0 Reg field PRC
20:19	0h RO	**RSVD53:** TBD
18	0h RW	**PEC:** Reg field PEC
17	0h RW	**CSC:** Reg field CSC
16:14	0h RO	**RSVD52:** TBD
13:10	0h RW	**PORTSPEED:** 0x0 Reg field PORTSPEED
9	0h RO	**RSVD51:** TBD
8:5	0h RW	**PLS:** flag Value After Reset: 0x5 Reg field PLS

Bit Range	Default & Access	Description
4	0h RW	**PR:** TBD
3:2	0h RO	**RSVD50:** TBD
1	0h RW	**PED:** Reg field PED
0	1h RW	**CCS:** flag Value After Reset: 0x0 Reg field CCS

3.74.69 DCECP_LO—Offset 8D8h

Debug capability is not supported

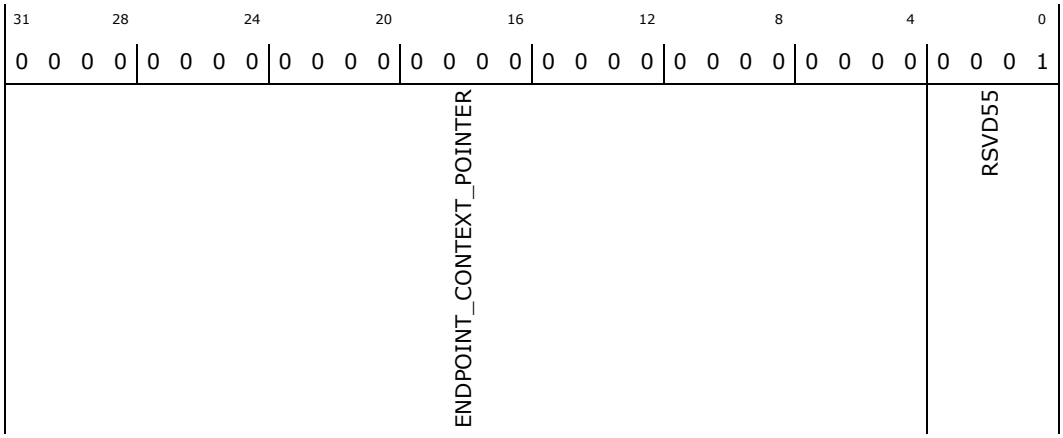
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCECP_LO: [BAR] + 8D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:4	0h RW	**ENDPOINT_CONTEXT_POINTER:** TBD
3:0	1h RO	**RSVD55:** TBD

3.74.70 DCECP_HI—Offset 8DCh

Debug capability is not supported

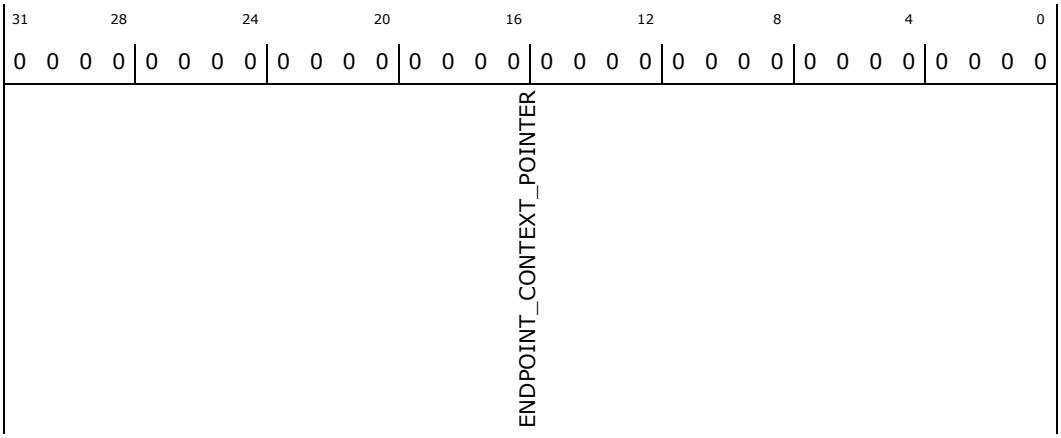
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCECP_HI: [BAR] + 8DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**ENDPOINT_CONTEXT_POINTER:** TBD

3.74.71 DCDDI1—Offset 8E0h

Debug capability is not supported

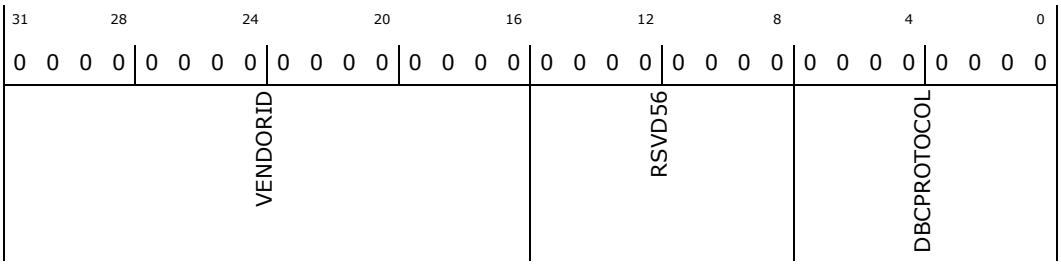
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCDDI1: [BAR] + 8E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**VENDORID:** TBD

Bit Range	Default & Access	Description
15:8	0h RO	**RSVD56:** TBD
7:0	0h RO	**DBCPROTOCOL:** TBD

3.74.72 DCDDI2—Offset 8E4h

Debug capability is not supported

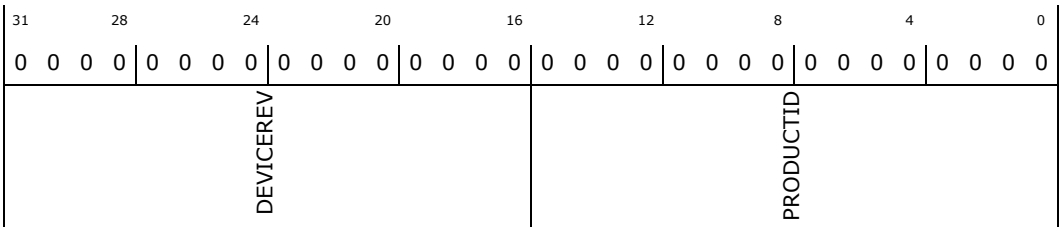
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCDDI2: [BAR] + 8E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**DEVICEREV:** TBD
15:0	0h RO	**PRODUCTID:** TBD

3.74.73 GSBUSCFG0—Offset C100h

Global SoC Bus Configuration Register 0

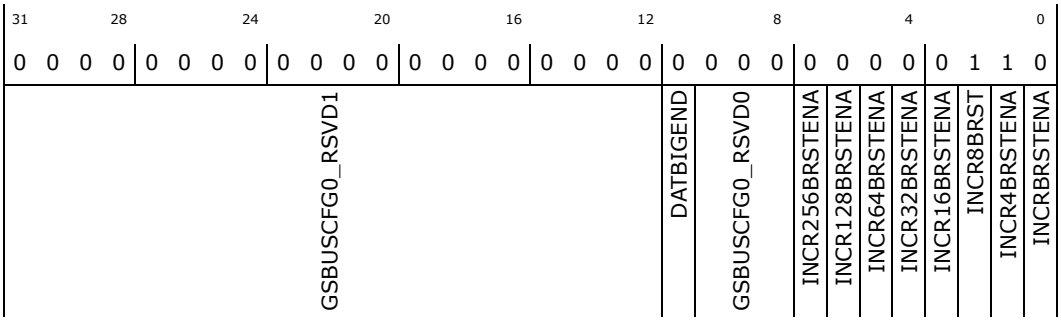
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GSBUSCFG0: [BAR] + C100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000006h



Bit Range	Default & Access	Description
31:12	0h RO	**GSBUSCFG0_RSVD1:** Reserved
11	0h RW	**DATBIGEND:** Data Access is Big-Endian (DatBigEnd). This bit controls the endian mode for data accesses. 0: Little-endian (default) 1: Big-endian In big-endian mode, DMA access (both read and write) for packet data will utilize a Byte Invariant Big-Endian mode (see Section Little-Endian and Big-Endian in the DWC SuperSpeed USB 3.0 Controller User Guide). Note: Since AXI requires byteinvariant endianness, setting DescBigend and DatBigEnd to one causes an address invariant transform to be applied, which is not appropriate.See section 9.3 and 9.4 of the AMBA AXI Specification. Hence for an AXI master (DWC_USB3_MBUS_TYPE=1), this bit must be set to zero.
10:8	0h RO	**GSBUSCFG0_RSVD0:** TBD
7	0h RW	**INCR256BRSTENA:** INCR256 Burst Type Enable
6	0h RW	**INCR128BRSTENA:** INCR128 Burst Type Enable
5	0h RW	**INCR64BRSTENA:** INCR64 Burst Type Enable
4	0h RW	**INCR32BRSTENA:** INCR32 Burst Type Enable
3	0h RW	**INCR16BRSTENA:** INCR16 Burst Type Enable
2	1h RW	**INCR8BRST:** INCR8 Burst Type Enable
1	1h RW	**INCR4BRSTENA:** INCR4 Burst Type Enable
0	0h RW	**INCRBRSTENA:** Undefined Length INCR Burst Type Enable (INCRBrstEna). Input to BUS-GM When enabled, this has higher priority than other burst types. For the AHB configuration. if this bit is set to 1, AHB master tries to do only one INCR burst for each transfer unless it has to break it at a 1Kbyte boundary. If this bit is set to 0, the AHB master may still use INCR burst type at the beginning and end bursts of transfers to align the address. The middle bursts are INCR4/8/16, depending when the type is enabled.

3.74.74 GSBUSCFG1—Offset C104h

Global SoC Bus Configuration Register 1

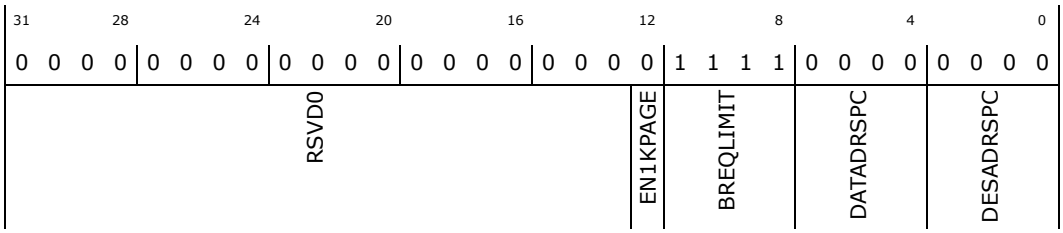
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GSBUSCFG1: [BAR] + C104h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000F00h



Bit Range	Default & Access	Description
31:13	0h RO	**RSVD0:** reserved
12	0h RW	**EN1KPAGE:** 1k Page Boundary Enable: By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data) breaks transfers at the 1k page boundary.
11:8	fh RW	**BREQLIMIT:** AXI Pipelined Transfers Burst Request Limit (PipeTransLimit) The field controls the number of outstanding pipelined transfers requests the AXI master will push to the AXI slave. Once the AXI master reaches this limit, it will not make more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete.This field is encoded as follows: h0: 1 request h1: 2 requests h2: 3 requests h3: 4 requests hF: 16 requests
7:4	0h RW	**DATADRSPC:** Reserved
3:0	0h RW	**DESADRSPC:** Reserved

3.74.75 GTXTHRCFG—Offset C108h

Global Tx Threshold Control Register

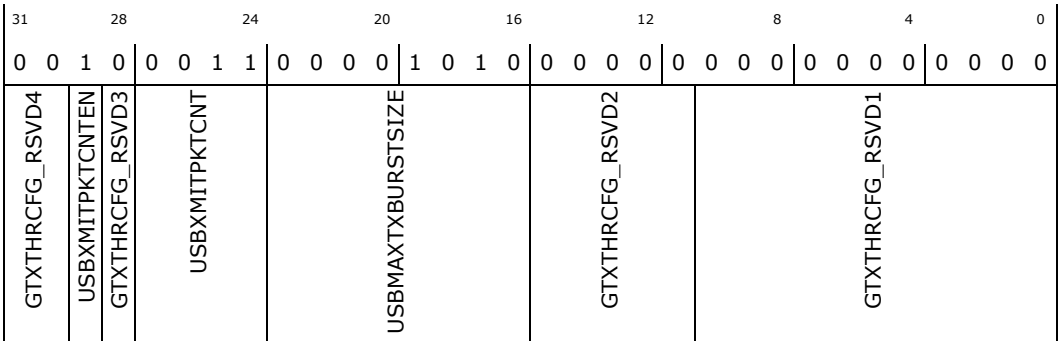
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXTHRCFG: [BAR] + C108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 230A0000h



Bit Range	Default & Access	Description
31:30	0h RW	**GTXTHRCFG_RSVD4:** Reserved
29	1h RW	**USBXMITPKTCNTEN:** USB Transmit Packet Count Enable (USBTxPktCntSel). This field enables/disables the USB transmission multi-packet thresholding: 0: USB transmission multi-packet thresholding is disabled, the core can only start transmission on the USB after the entire packet has been fetched into the corresponding TXFIFO. 1: USB transmission multi-packet thresholding is enabled. The core can only start transmission on the USB after USB Transmit Packet Count amount of packets for the USB transaction (burst) are already in the corresponding TXFIFO This mode is only valid in the host mode. It is only used for SuperSpeed.
28	0h RO	**GTXTHRCFG_RSVD3:** Reserved
27:24	3h RO	**USBXMITPKTCNT:** USB Transmit Packet Count (USBTxPktCnt) This field specifies the number of packets that must be in the TXFIFO before the core can start transmission for the corresponding USB transaction (burst). This field is only valid when the USB Transmit Packet Count Enable field is set to one. Valid values are from 1 to 15.
23:16	0Ah RW	**USBMAXTXBURSTSIZE:** USB Maximum TX Burst Size: When USBTxPktCntSel is one, this field specifies the Maximum Bulk OUT burst the core should do. When the system bus is slower than the USB, TX FIFO can underrun during a long burst. User can program a smaller value to this field to limit the TX burst size that the core can do. It only applies to SS Bulk, Isochronous, and Interrupt OUT endpoints in the host mode. Valid values are from 1 to 16.
15:11	0h RO	**GTXTHRCFG_RSVD2:** Reserved
10:0	0h RW	**GTXTHRCFG_RSVD1:** Reserved

3.74.76 GRXTHRCFG—Offset C10Ch

Global Rx Threshold Control Register

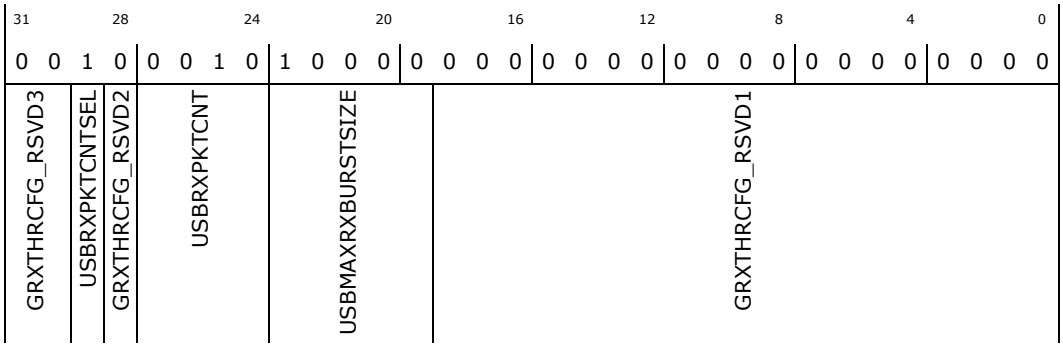
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GRXTHRCFG: [BAR] + C10Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 22800000h



Bit Range	Default & Access	Description
31:30	0h RO	**GRXTHRCFG_RSVD3:** Reserved
29	1h RW	**USBRXPKTCNTSEL:** USB ReceivePacket Count Enable: This field enables/ disables the USB reception multi-packet thresholding: n 0: The core can only start reception on the USB when the RX FIFO has space for at least one packet. n 1: The core can only start reception on the USB when the RX FIFO has space for at least USBRxPktCnt amount of packets. This mode is only valid in the host mode. It is only used for SuperSpeed.
28	0h RO	**GRXTHRCFG_RSVD2:** Reserved
27:24	2h RW	**USBRXPKTCNT:** USB Receive Packet Count: This field specifies space (in number of packets) that must be available in the RX FIFO before the core can start the corresponding USB RX transaction (burst). This field is only valid when the USB Receive Packet Count Enable field is set to one. The valid values are from 1 to 15.
23:19	10h RW	**USBMAXRXBURSTSIZE:** USB Maximum Receive Burst Size: This field is only valid when USBRxPktCntSel is one. This field specifies the Maximum Bulk IN burst the core should do. When the system bus is slower than the USB, RX FIFO can overrun during a long burst. User can program a smaller value to this field to limit the RX burst size that the core can do. It only applies to SS Bulk, Isochronous, and Interrupt IN endpoints in the host mode. Valid values are from 1 to 16.
18:0	0h RO	**GRXTHRCFG_RSVD1:** Reserved

3.74.77 GCTL—Offset C110h

Global Common Register

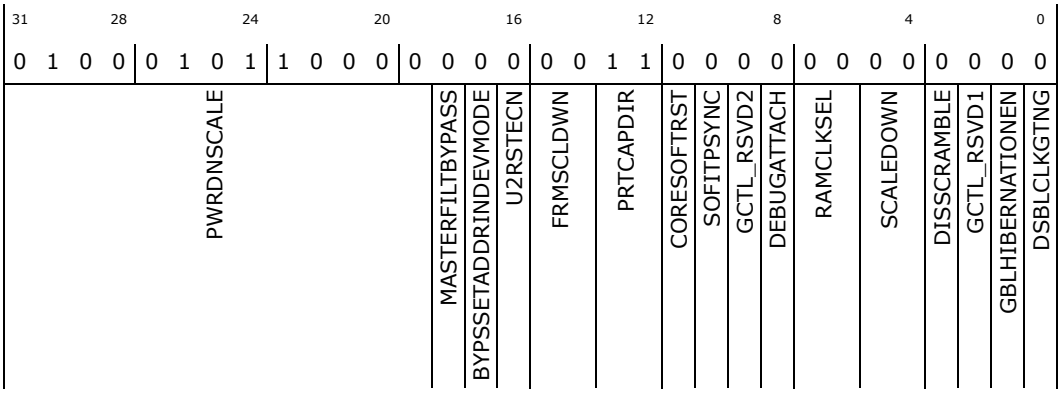
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GCTL: [BAR] + C110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 45803000h



Bit Range	Default & Access	Description
31:19	08b0h RW	**PWRDNSCALE:** Reg field PWRDNSCALE
18	0h RW	**MASTERFILTBYPASS:** Master Filter Bypass: When this bit is set to 1'b1, irrespective of the parameter DWC_USB3_EN_BUS_FILTERS chosen, all the filters in the DWC_usb3_filter module will be bypassed. The double synchronizers to mac_clk preceding the filters will also be bypassed. For enabling the filters, this bit should be 1'b0.
17	0h RW	**BYPSSETADDRINDEVMODE:** TBD
16	0h RW	**U2RSTECN:** If the super speed connection fails during POLL or LMP exchange, the device connects at non-SS mode. If this bit is set, then device attempts three more times to connect at SS, even if it previously failed to operate in SS mode.
15:14	0h RW	**FRMSCLDWN:** This field scales down device view of a SOF/USOF/ITP duration. For SS/HS mode: Value of 2'h3 implements interval to be 15. 625 us Value of 2'h2 implements interval to be 31.25 us Value of 2'h1 implements interval to be 62.5 us Value of 2'h0 implements interval to be125us For FS mode, the scale-down value is multiplied by 8.
13:12	3h RW	**PRTCAPDIR:** Reg field PRTCAPDIR
11	0h RW	**CORESOFTRST:** Core Soft Reset (CoreSoftReset) 1b0 - No soft reset 1b1 - Soft reset to core When you reset PHYs (using GUBS3PHYCFG or GUSB3PIPECTL registers), you must keep the core in reset state until PHY clocks are stable. This controls the bus, ram, and mac domain resets.
10	0h RW	**SOFITPSYNC:** Sync ITP to reference clock
9	0h RO	**GCTL_RSVD2:** Disable U1/U2 timer Scaledown (U1U2TimerScale) If set to '1' along with GCTL[5:4] (ScaleDown) = 2'bX1 disables the scale down of U1/U2 inactive timer values. This is for simulation mode only.

Bit Range	Default & Access	Description
8	0h RW	**DEBUGATTACH:** Debug Attach
7:6	0h RW	**RAMCLKSEL:** Reg field RAMCLKSEL
5:4	0h RW	**SCALEDOWN:** reg field SCALEDOWN
3	0h RW	**DISSCRAMBLE:** Disable Scrambling
2	0h RO	**GCTL_RSVD1:** Reserved
1	0h RW	**GBLHIBERNATIONEN:** This bit enables hibernation at the global level. If hibernation is not enabled via this bit, the PMU immediately accepts the D0-)D3 and D3-)D0 power state change requests, but does not save or restore any core state. In addition, the PMUs will never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	0h RW	**DSBLCLKGTNG:** Disable Clock Gating

3.74.78 GSTS—Offset C118h

Global Status Register

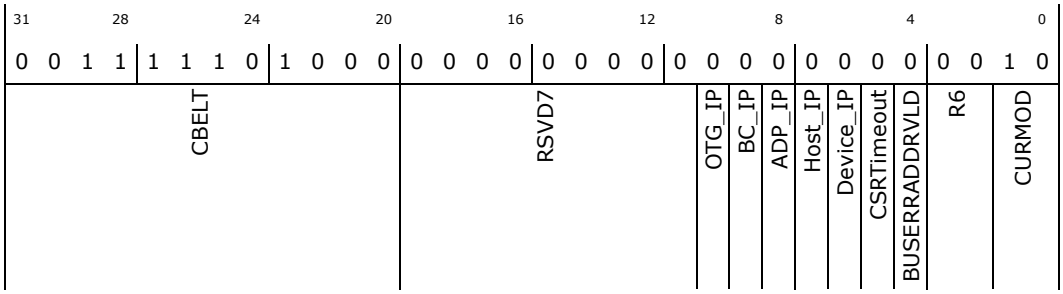
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GSTS: [BAR] + C118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 3E800002h



Bit Range	Default & Access	Description
31:20	3e8h RO	**CBELT:** Current BELT Value: In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command.
19:11	0h RO	**RSVD7:** reserved

Bit Range	Default & Access	Description
10	0h RO	**OTG_IP:** OTG Interrupt Pending: This field indicates that there is a pending interrupt pertaining to OTG in OEVT register.
9	0h RO	**BC_IP:** Battery Charger Interrupt Pending: This field indicates that there is a pending interrupt pertaining to BC in BCEVT register.
8	0h RO	**ADP_IP:** ADP Interrupt Pending: This field indicates that there is a pending interrupt pertaining to ADP in ADPEVT register.
7	0h RO	**Host_IP:** Host Interrupt Pending: This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue.
6	0h RO	**Device_IP:** Device Interrupt Pending: This field indicates that there is a pending interrupt pertaining to peripheral (device) operation in the Device event queue.
5	0h RO	**CSRTimeout:** CSR Timeout: When this bit is 1'b1, it indicates that software performed a write or read to a core register that could not be completed within DWC_USB3_CSR_ACCESS_TIMEOUT bus clock cycles (default: 65535).
4	0h RO	**BUSERRADDRVLD:** Bus Error Address Valid
3:2	0h RO	**R6:** Reg field R6
1:0	2h RO	**CURMOD:** Reg field CURMOD

3.74.79 GSNPSID—Offset C120h

flag Value After Reset: 0x5533210a Global Synopsys ID Register

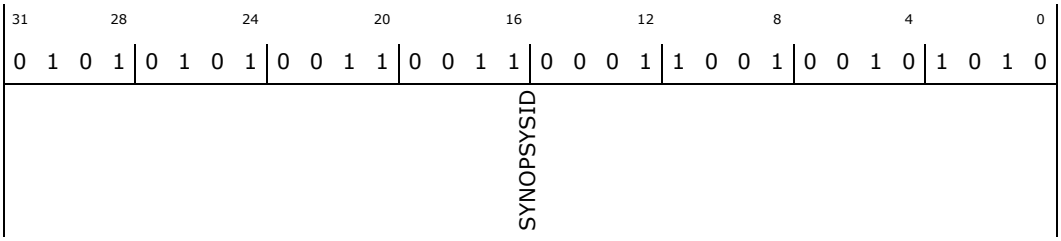
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GSNPSID: [BAR] + C120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 5533192Ah



Bit Range	Default & Access	Description
31:0	5533192ah RO	**SYNOPSYSID:** flag Value After Reset: 0x5533210a Reg field SYNOPSYSID

3.74.80 GGPIO—Offset C124h

Global General Purpose Input/Output Register

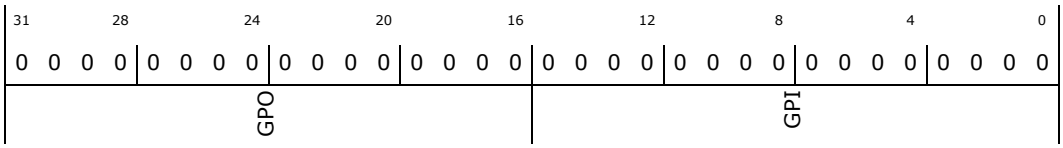
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GGPIO: [BAR] + C124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**GPO:** General Purpose Output: This field's value is driven out on the gp_o[15:0] core output port.
15:0	0h RO	**GPI:** General Purpose Input: This field's read value reflects the gp_i[15:0] core input value.

3.74.81 GUID—Offset C128h

flag Value After Reset: 0x8086a0 Global User ID Register

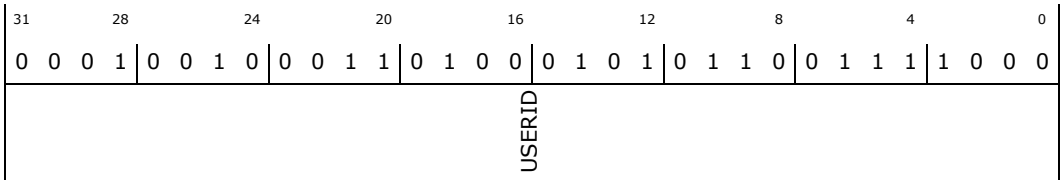
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GUID: [BAR] + C128h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 12345678h



Bit Range	Default & Access	Description
31:0	12345678h RW	**USERID:** flag Value After Reset: 0x8086a0 Reg field USERID

3.74.82 GUCTL—Offset C12Ch

flag Value After Reset: 0x200ce00 Global User Control Register

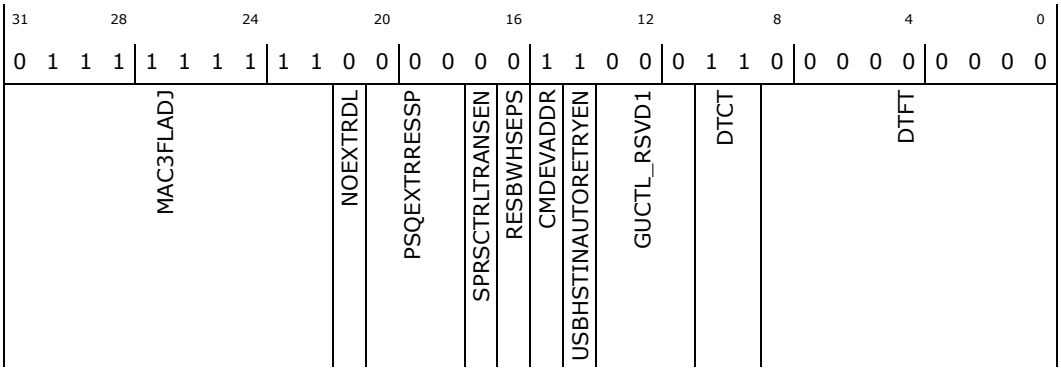
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GUCTL: [BAR] + C12Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 7FC0C600h



Bit Range	Default & Access	Description
31:22	1ffh RW	**MAC3FLADJ:** TBD
21	0h RW	**NOEXTRDL:** TBD
20:18	0h RW	**PSQEXTRRESSP:** TBD
17	0h RW	**SPRSCTRLTRANSEN:** Sparse Control Transaction Enable: Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/frame can cause these devices to misbehave. If this bit is set to 1'b1, the host controller schedules transactions for a Control transfer in different microframes/frames.
16	0h RW	**RESBWHSEPS:** Reserving 85% Bandwidth for HS Periodic EPs
15	1h RW	**CMDEVADDR:** Compliance Mode for Device Address: When this bit is 1'b1, Slot ID may have different value than Device Address if max_slot_enabled (128. n 1'b1: Increment Device Address on each Address Device command. n 1'b0: Device Address is equal to Slot ID. The xHCI compliance requires this bit to be set to 1'. The 0' mode is for debug purpose only. This all ows you to easily identify a device connected to a port in the Lecroy or Eliisys trace during hardware debug. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
14	1h RW	**USBHSTINAUTORETRYEN:** Host IN Auto Retry: When set, this field enables the Auto Retry feature. For IN transfers (non-isochronous) that encounter data packets with CRC errors or internal overrun scenarios, the auto retry feature causes the Host core to reply to the device with a non-terminating retry ACK (that is, an ACK transaction packet with Retry = 1 and NumP != 0). If the Auto Retry feature is disabled (default), the core will respond with a terminating retry ACK (that is, an ACK transaction packet with Retry = 1 and NumP = 0). n 1'b0: Auto Retry Disabled n 1'b1: Auto Retry Enabled In device mode this bit should be 0

Bit Range	Default & Access	Description
13:11	0h RO	**GUCTL_RSVD1:** TBD
10:9	3h RW	**DTCT:** Device Timeout Coarse Tuning: This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. The core first checks the DTCT value. If it is 0, then the timeout value is defined by the DTFT. If it is non-zero, then it uses the following timeout values: n 2'b00: 0 usec -) use DTFT value instead n 2'b01: 500 usec n 2'b10: 1.5 msec n 2'b11: 6.5 msec
8:0	0h RW	**DTFT:** Device Timeout Fine Tuning: This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. For DTFT field to take effect, DTCT must be set to 2'b00. The DTFT value is the number of 125 MHz clocks * 256 to count before considering a device timeout. For the 125 MHz clk (8 ns period), this is calculated as follows: (DTFT value) * 256 * (8 ns) Quick Reference: n if DTFT = 0x2, 2*256*8 = 4usec timeout n if DTFT = 0x5, 5*256*8 = 10usec timeout n if DTFT = 0xA, 10*256*8 = 20usec timeout n if DTFT = 0x10, 16*256*8 = 32usec timeout n if DTFT = 0x19, 25*256*8 = 51usec timeout n if DTFT = 0x31, 49*256*8 = 100usec timeout n if DTFT = 0x62, 98*256*8 = 200usec timeout

3.74.83 GBUSERRADDRLO—Offset C130h

Register GBUSERRADDRLO

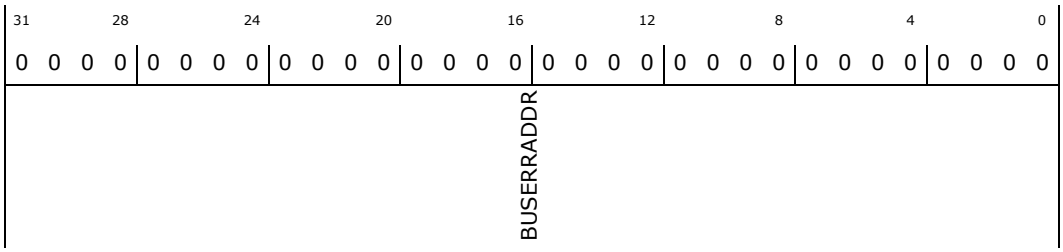
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GBUSERRADDRLO: [BAR] + C130h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**BUSERRADDR:** Reg field BUSERRADDR

3.74.84 GBUSERRADDRHI—Offset C134h

Register GBUSERRADDRHI

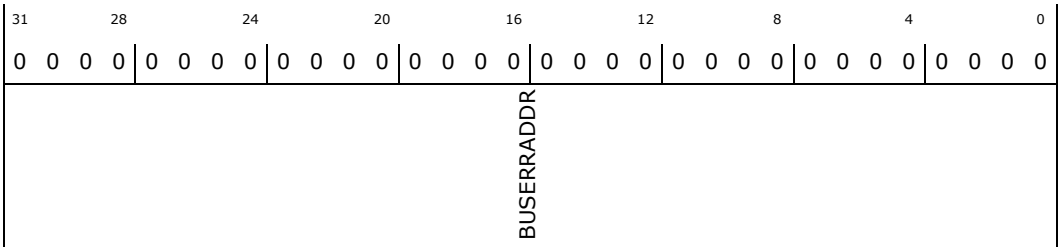
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GBUSERRADDRHI: [BAR] + C134h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**BUSERRADDR:** Reg field BUSERRADDR

3.74.85 GPRTBIMAPLO—Offset C138h

0x0 Register R

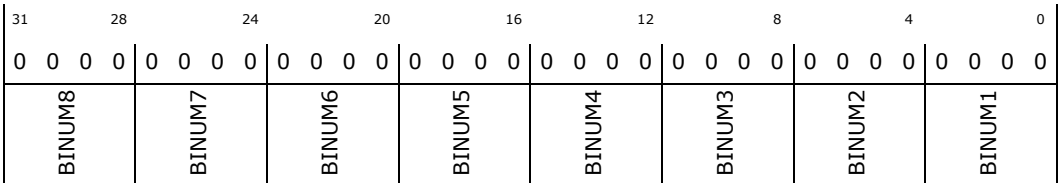
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPRTBIMAPLO: [BAR] + C138h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RO	**BINUM8:** Reg field BINUM8
27:24	0h RO	**BINUM7:** Reg field BINUM7
23:20	0h RO	**BINUM6:** Reg field BINUM6
19:16	0h RO	**BINUM5:** Reg field BINUM5

Bit Range	Default & Access	Description
15:12	0h RO	**BINUM4:** Reg field BINUM4
11:8	0h RO	**BINUM3:** Reg field BINUM3
7:4	0h RO	**BINUM2:** Reg field BINUM2
3:0	0h RW	**BINUM1:** flag Value After Reset: 0x1 Reg field BINUM1

3.74.86 GPRTBIMAPHI—Offset C13Ch

Register R

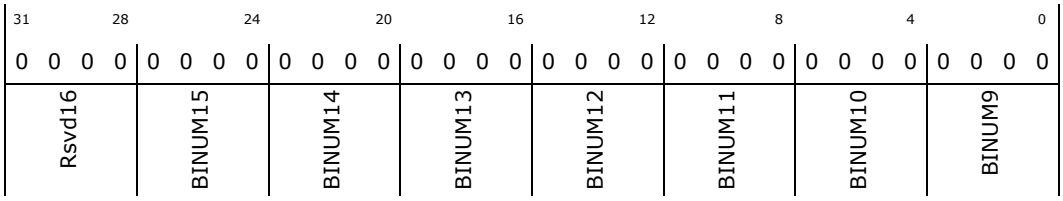
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPRTBIMAPHI: [BAR] + C13Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RO	**Rsvd16:** reserved
27:24	0h RO	**BINUM15:** Reg field BINUM15
23:20	0h RO	**BINUM14:** Reg field BINUM14
19:16	0h RO	**BINUM13:** Reg field BINUM13
15:12	0h RO	**BINUM12:** Reg field BINUM12
11:8	0h RO	**BINUM11:** Reg field BINUM11
7:4	0h RO	**BINUM10:** Reg field BINUM10
3:0	0h RO	**BINUM9:** Reg field BINUM9

3.74.87 GHWPARAMS0—Offset C140h

Global Hardware Parameters Register 0

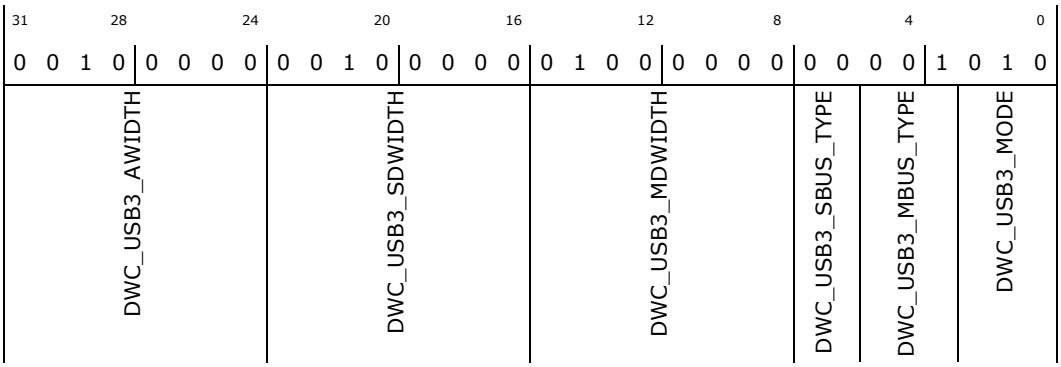
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHWPARAMS0: [BAR] + C140h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 2020400Ah



Bit Range	Default & Access	Description
31:24	20h RO	**DWC_USB3_AWIDTH:** TBD
23:16	20h RO	**DWC_USB3_SDWIDTH:** TBD
15:8	40h RO	**DWC_USB3_MDWIDTH:** TBD
7:6	0h RO	**DWC_USB3_SBUS_TYPE:** TBD
5:3	1h RO	**DWC_USB3_MBUS_TYPE:** TBD
2:0	2h RO	**DWC_USB3_MODE:** TBD

3.74.88 GHWPARAMS1—Offset C144h

Global Hardware Parameters Register 1

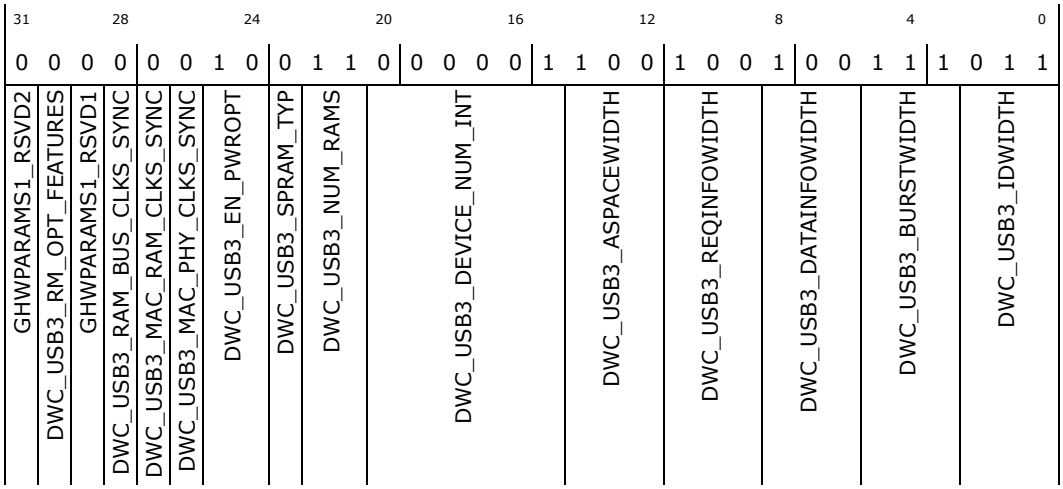
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHWPARAMS1: [BAR] + C144h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0260C93Bh



Bit Range	Default & Access	Description
31	0h RO	**GHWPARAMS1_RSVD2:** TBD
30	0h RO	**DWC_USB3_RM_OPT_FEATURES:** TBD
29	0h RO	**GHWPARAMS1_RSVD1:** TBD
28	0h RO	**DWC_USB3_RAM_BUS_CLKS_SYNC:** Reserved.
27	0h RO	**DWC_USB3_MAC_RAM_CLKS_SYNC:** Reserved.
26	0h RO	**DWC_USB3_MAC_PHY_CLKS_SYNC:** TBD
25:24	2h RO	**DWC_USB3_EN_PWROPT:** TBD
23	0h RO	**DWC_USB3_SPRAM_TYP:** TBD
22:21	3h RO	**DWC_USB3_NUM_RAMS:** TBD
20:15	01h RO	**DWC_USB3_DEVICE_NUM_INT:** TBD
14:12	4h RO	**DWC_USB3_ASPACEWIDTH:** Reserved.
11:9	4h RO	**DWC_USB3_REQINFOWIDTH:** TBD
8:6	4h RO	**DWC_USB3_DATAINFOWIDTH:** TBD
5:3	7h RO	**DWC_USB3_BURSTWIDTH:** TBD
2:0	3h RO	**DWC_USB3_IDWIDTH:** TBD

3.74.89 GHWPARAMS2—Offset C148h

Global Hardware Parameters Register 2

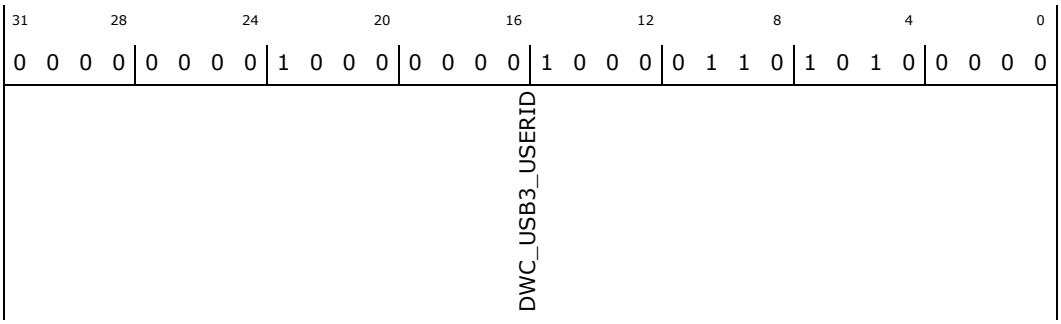
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHWPARAMS2: [BAR] + C148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 008086A0h



Bit Range	Default & Access	Description
31:0	008086a0h RO	**DWC_USB3_USERID:** TBD

3.74.90 GHWPARAMS3—Offset C14Ch

Global Hardware Parameters Register 3

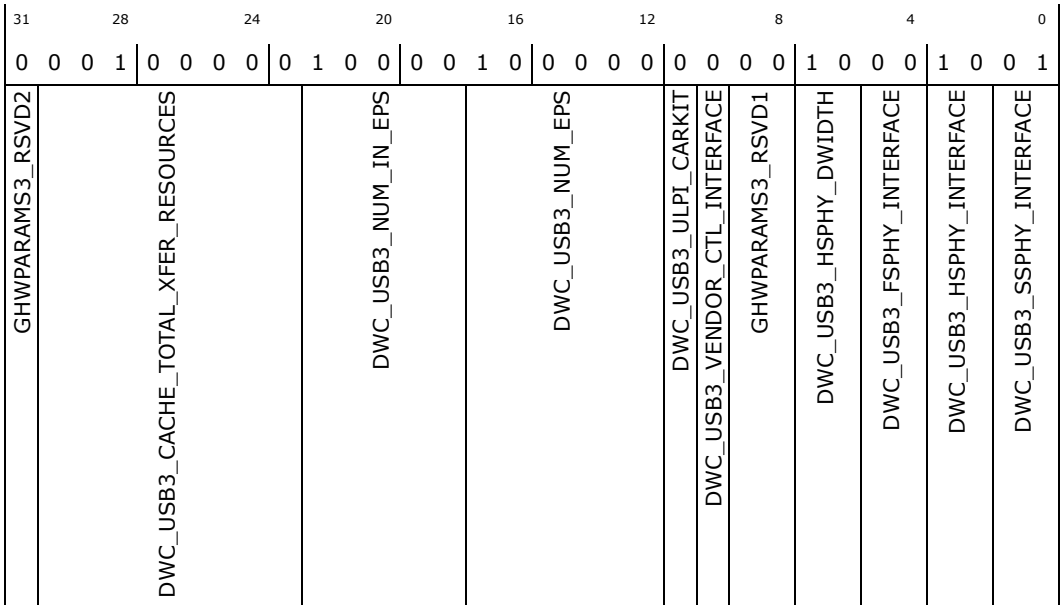
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHWPARAMS3: [BAR] + C14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 10420089h



Bit Range	Default & Access	Description
31	0h RO	**GHWPARAMS3_RSVD2:** TBD
30:23	20h RO	**DWC_USB3_CACHE_TOTAL_XFER_RESOURCES:** TBD
22:18	10h RO	**DWC_USB3_NUM_IN_EPS:** TBD
17:12	20h RO	**DWC_USB3_NUM_EPS:** TBD
11	0h RO	**DWC_USB3_ULPI_CARKIT:** TBD
10	0h RO	**DWC_USB3_VENDOR_CTL_INTERFACE:** TBD
9:8	0h RO	**GHWPARAMS3_RSVD1:** TBD
7:6	2h RO	**DWC_USB3_HSPHY_DWIDTH:** TBD
5:4	0h RO	**DWC_USB3_FSPHY_INTERFACE:** TBD
3:2	2h RO	**DWC_USB3_HSPHY_INTERFACE:** TBD
1:0	1h RO	**DWC_USB3_SSPHY_INTERFACE:** TBD

3.74.91 GHWPARAMS4—Offset C150h

falg Value After Reset: 0x48a22004 Global Hardware Parameters Register 4

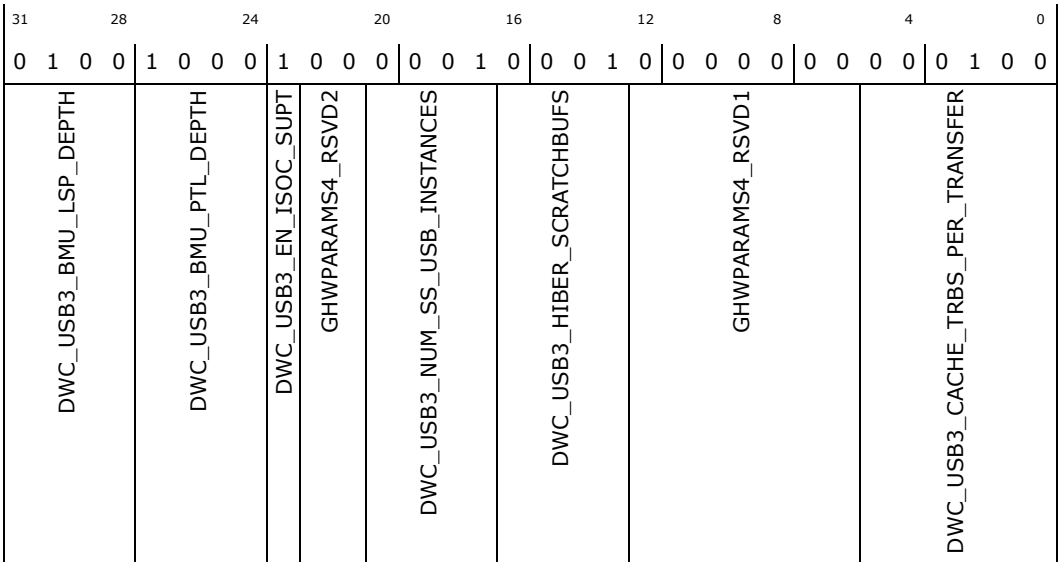
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHWPARAMS4: [BAR] + C150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 48822004h



Bit Range	Default & Access	Description
31:28	4h RO	**DWC_USB3_BMU_LSP_DEPTH:** TBD
27:24	8h RO	**DWC_USB3_BMU_PTL_DEPTH:** TBD
23	1h RO	**DWC_USB3_EN_ISOC_SUPT:** TBD
22:21	0h RO	**GHWPARAMS4_RSVD2:** TBD
20:17	1h RO	**DWC_USB3_NUM_SS_USB_INSTANCES:** TBD
16:13	1h RO	**DWC_USB3_HIBER_SCRATCHBUFS:** TBD
12:6	0h RO	**GHWPARAMS4_RSVD1:** TBD
5:0	04h RO	**DWC_USB3_CACHE_TRBS_PER_TRANSFER:** TBD

3.74.92 GHWPARAMS5—Offset C154h

Global Hardware Parameters Register 5

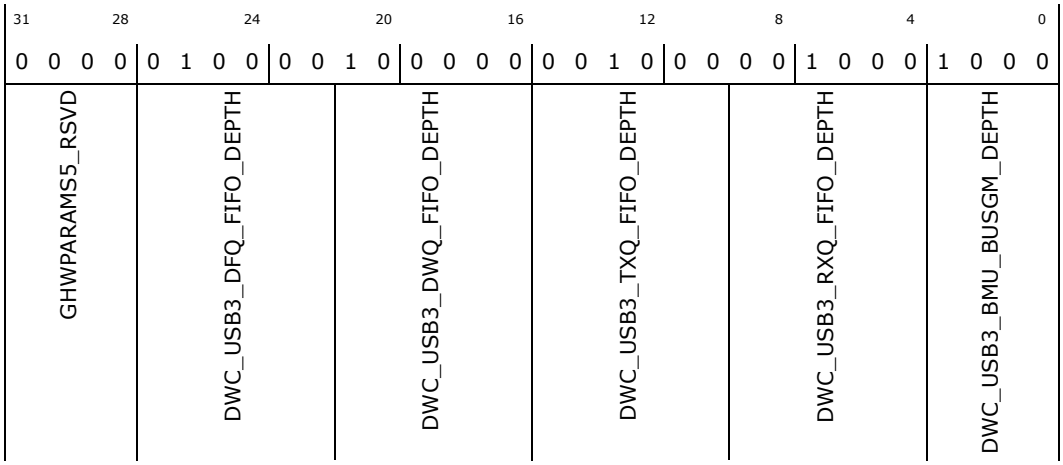
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHWPARAMS5: [BAR] + C154h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 04202088h



Bit Range	Default & Access	Description
31:28	0h RO	**GHWPARAMS5_RSVD:** TBD
27:22	10h RO	**DWC_USB3_DFQ_FIFO_DEPTH:** TBD
21:16	20h RO	**DWC_USB3_DWQ_FIFO_DEPTH:** TBD
15:10	08h RO	**DWC_USB3_TXQ_FIFO_DEPTH:** TBD
9:4	08h RO	**DWC_USB3_RXQ_FIFO_DEPTH:** TBD
3:0	8h RO	**DWC_USB3_BMU_BUSGM_DEPTH:** TBD

3.74.93 GHWPARAMS6—Offset C158h

Global Hardware Parameters Register 6

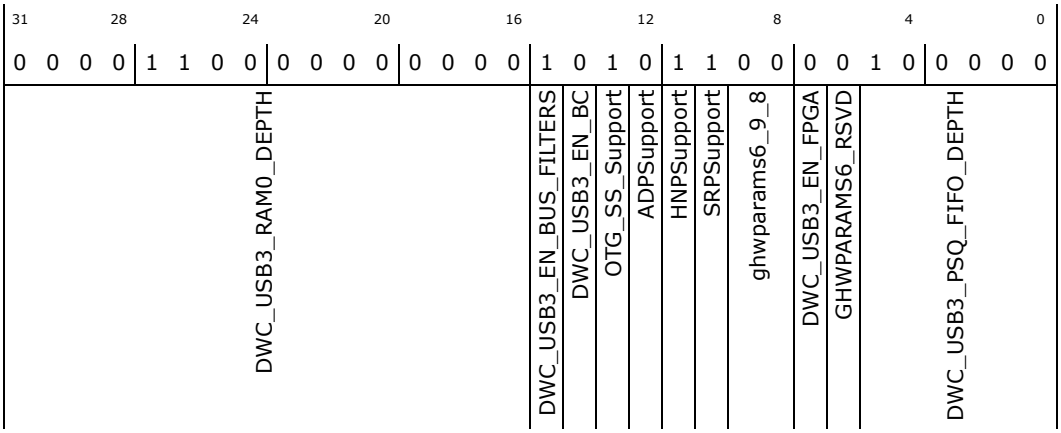
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHWPARAMS6: [BAR] + C158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0C00AC20h



Bit Range	Default & Access	Description
31:16	0c00h RO	**DWC_USB3_RAM0_DEPTH:** TBD
15	1h RO	**DWC_USB3_EN_BUS_FILTERS:** TBD
14	0h RO	**DWC_USB3_EN_BC:** TBD
13	1h RO	**OTG_SS_Support:** Reg field CORECONSULTANT
12	0h RO	**ADPSupport:** DWC_USB3_EN_ADP:
11	1h RO	**HNPSupport:** RSP/HNP Support Enabled: The application uses this bit to determine the DWC_usb3 core's RSP/HNP support. If DWC_USB3_EN_OTG=2, n 1'b0: RSP and HNP support is not enabled. The only exception for this rule is for SSPC-OTG devices where RSP support is not enabled, but HNP support is enabled. (Refer OCFG.SSPC-OTG bit) n 1'b1: RSP and HNP support is enabled If DWC_USB3_EN_OTG=1, n 1'b0: HNP support is not enabled n 1'b1: HNP support is enabled This bit is enabled only if HNP mode was specified for HNP Mode of Operation in coreConsultant (parameter DWC_USB3_EN_OTG is not 0, and DWC_USB3_MODE is DRD). Other wise, it reads 0.
10	1h RO	**SRPSupport:** SRP Support Enabled: The application uses this bit to determine the DWC_usb3 core's SRP support. n1'b0: SRP support is not enabled n 1'b1: SRP support is enabled This bit is 1'b1 when the parameter DWC_USB3_EN_OTG is not 0.
9:8	0h RO	**ghwparams6_9_8:** Reg field CORECONSULTANT
7	0h RO	**DWC_USB3_EN_FPGA:** TBD
6	0h RO	**GHWPARAMS6_RSVD:** TBD
5:0	20h RO	**DWC_USB3_PSQ_FIFO_DEPTH:** TBD

3.74.94 GHWPARAMS7—Offset C15Ch

Global Hardware Parameters Register 7

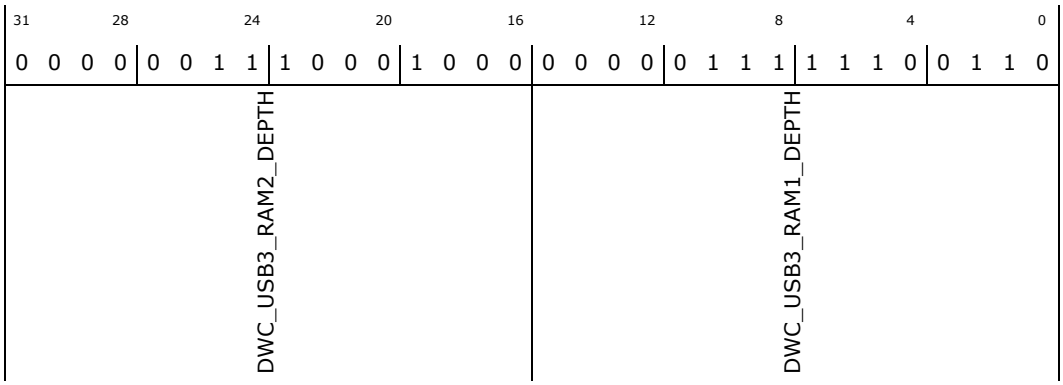
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHWPARAMS7: [BAR] + C15Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 038807E6h



Bit Range	Default & Access	Description
31:16	0388h RO	**DWC_USB3_RAM2_DEPTH:** TBD
15:0	07e6h RO	**DWC_USB3_RAM1_DEPTH:** TBD

3.74.95 GDBGFIFOSPACE—Offset C160h

flag Value After Reset: 0x820000 Global Debug Queue/FIFO Space Available Register

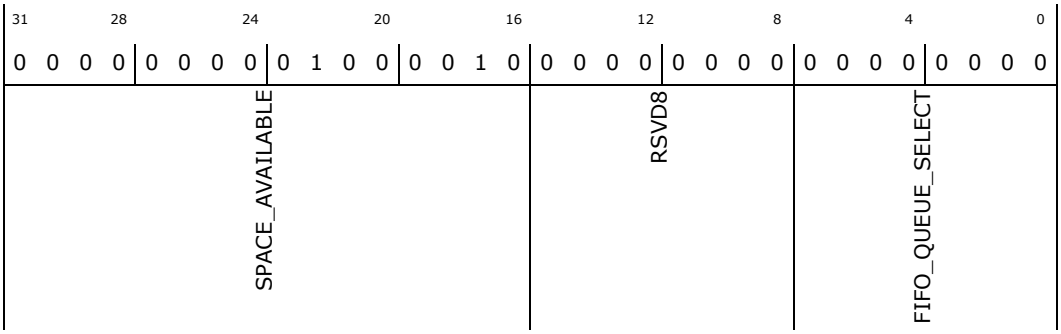
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GDBGFIFOSPACE: [BAR] + C160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00420000h



Bit Range	Default & Access	Description
31:16	42h RO	**SPACE_AVAILABLE:** Reg field SPACE_AVAILABLE
15:8	0h RO	**RSVD8:** reserved
7:0	0h RW	**FIFO_QUEUE_SELECT:** Reg field FIFO_QUEUE_SELECT

3.74.96 GDBGLTSSM—Offset C164h

Global Debug LTSSM Register

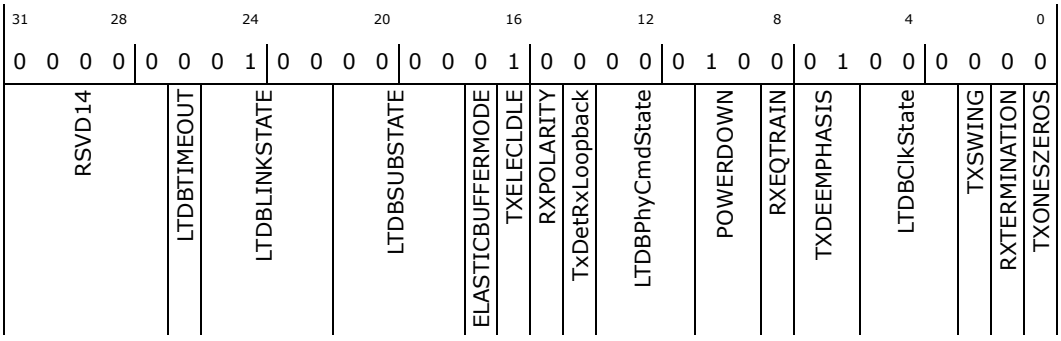
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GDBGLTSSM: [BAR] + C164h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 01010440h



Bit Range	Default & Access	Description
31:27	0h RO	**RSVD14:** reserved
26	0h RO	**LTDBTIMEOUT:** LTDB Timeout

Bit Range	Default & Access	Description
25:22	4h RO	**LTDBLINKSTATE:** flag Value After Reset: 0x0 LTDB Link State
21:18	0h RO	**LTDBSUBSTATE:** LTDB Sub-State
17	0h RO	**ELASTICBUFFERMODE:** Elastic Buffer Mode
16	1h RO	**TXELECLDLE:** Tx Elec Idle
15	0h RO	**RXPOLARITY:** Rx Polarity
14	0h RO	**TxDetRxLoopback:** Tx Detect Rx/Loopback:
13:11	0h RO	**LTDBPhyCmdState:** LTSSM PHY command State: n 000: PHY_IDLE (PHY command state is in IDLE. No PHY request pending) n 001: PHY_DET (Request to start Receiver detection) n 010: PHY_DET_3 (Wait for Phy_Status (Receiver detection)) n 011: PHY_PWR_DLY (Delay Pipe3_PowerDown P0 -) P1/P2/P3 request) n 100: PHY_PWR_A (Delay for internal logic) n 101: PHY_PWR_B (Wait for Phy_Status(Power state change request))
10:9	2h RO	**POWERDOWN:** flag Value After Reset: 0x0 Reg field POWERDOWN
8	0h RO	**RXEQTRAIN:** RxEq Train
7:6	1h RO	**TXDEEMPHASIS:** flag Value After Reset: 0x0 Reg field TXDEEMPHASIS
5:3	0h RO	**LTDBClkState:** LTSSM Clock State: n 000: CLK_NORM (PHY is in non-P3 state and PCLK is running) n 001: CLK_TO_P3 (P3 entry request to PHY) n 010: CLK_WAIT1 (Wait for Phy_Status (P3 request)) n 011: CLK_P3 (PHY is in P3 and PCLK is not running) n 100: CLK_TO_P0 (P3 exit request to PHY) n 101: CLK_WAIT2 (Wait for Phy_Status (P3 exit request))
2	0h RO	**TXSWING:** Tx Swing
1	0h RO	**RXTERMINATION:** Rx Termination
0	0h RO	**TXONESZEROS:** Tx Ones/Zeros

3.74.97 GPRTBIMAP_HSLO—Offset C180h

High Speed port to bus instance mapping

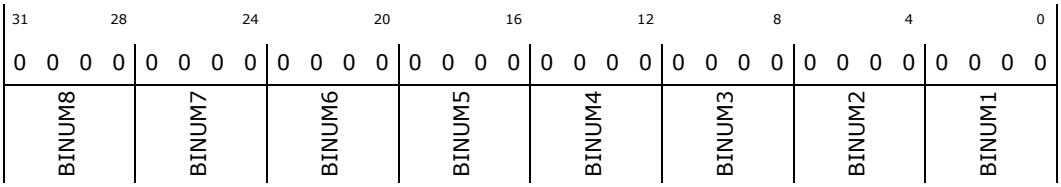
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPRTBIMAP_HSLO: [BAR] + C180h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RO	**BINUM8:** Reg field BINUM8
27:24	0h RO	**BINUM7:** Reg field BINUM7
23:20	0h RO	**BINUM6:** Reg field BINUM6
19:16	0h RO	**BINUM5:** Reg field BINUM5
15:12	0h RO	**BINUM4:** Reg field BINUM4
11:8	0h RO	**BINUM3:** Reg field BINUM3
7:4	0h RO	**BINUM2:** Reg field BINUM2
3:0	0h RW	**BINUM1:** flag Value After Reset: 0x1 Reg field BINUM1

3.74.98 GPRTBIMAP_HSHI—Offset C184h

High Speed port to bus instance mapping

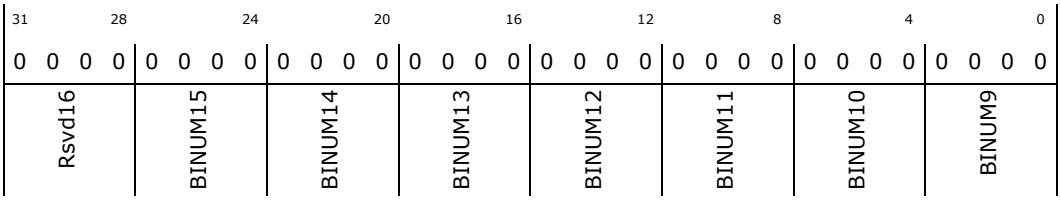
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPRTBIMAP_HSHI: [BAR] + C184h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RO	**Rsvd16:** reserved

Bit Range	Default & Access	Description
27:24	0h RO	**BINUM15:** Reg field BINUM15
23:20	0h RO	**BINUM14:** Reg field BINUM14
19:16	0h RO	**BINUM13:** Reg field BINUM13
15:12	0h RO	**BINUM12:** Reg field BINUM12
11:8	0h RO	**BINUM11:** Reg field BINUM11
7:4	0h RO	**BINUM10:** Reg field BINUM10
3:0	0h RO	**BINUM9:** Reg field BINUM9

3.74.99 GPRTBIMAP_FSLO—Offset C188h

Register Full Speed port to bus instance mapping

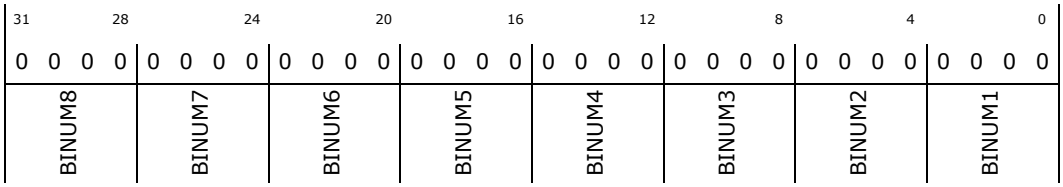
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPRTBIMAP_FSLO: [BAR] + C188h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RO	**BINUM8:** Reg field BINUM8
27:24	0h RO	**BINUM7:** Reg field BINUM7
23:20	0h RO	**BINUM6:** Reg field BINUM6
19:16	0h RO	**BINUM5:** Reg field BINUM5
15:12	0h RO	**BINUM4:** Reg field BINUM4
11:8	0h RO	**BINUM3:** Reg field BINUM3

Bit Range	Default & Access	Description
7:4	0h RO	**BINUM2:** Reg field BINUM2
3:0	0h RW	**BINUM1:** flag Value After Reset: 0x1 Reg field BINUM1

3.74.100 GPRTBIMAP_FSHI—Offset C18Ch

Register Full Speed port to bus instance mapping

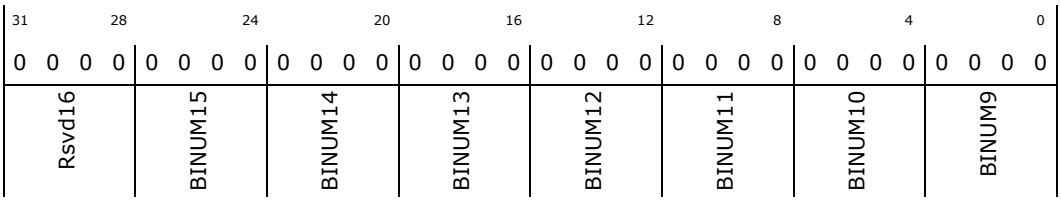
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPRTBIMAP_FSHI: [BAR] + C18Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RO	**Rsvd16:** reserved
27:24	0h RO	**BINUM15:** Reg field BINUM15
23:20	0h RO	**BINUM14:** Reg field BINUM14
19:16	0h RO	**BINUM13:** Reg field BINUM13
15:12	0h RO	**BINUM12:** Reg field BINUM12
11:8	0h RO	**BINUM11:** Reg field BINUM11
7:4	0h RO	**BINUM10:** Reg field BINUM10
3:0	0h RO	**BINUM9:** Reg field BINUM9

3.74.101 GUSB2PHYCFG—Offset C200h

Register Rs

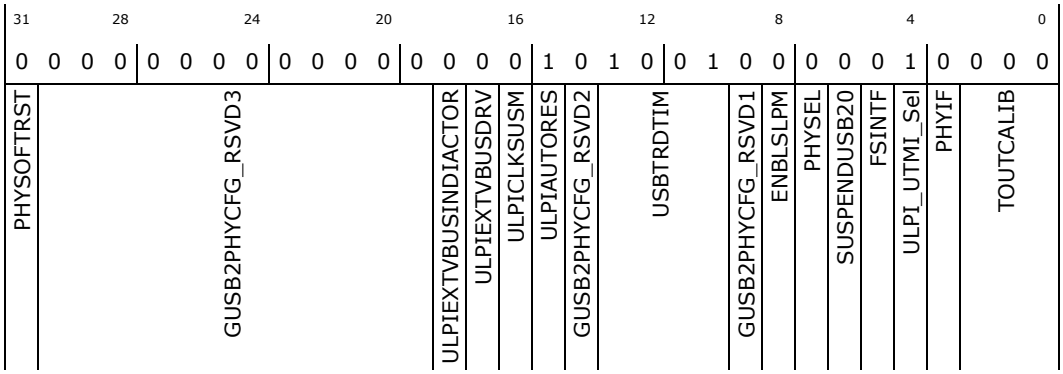
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GUSB2PHYCFG: [BAR] + C200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000A410h



Bit Range	Default & Access	Description
31	0h RW	**PHYSOFTRST:** Reg field PHYSOFTRST
30:19	0h RO	**GUSB2PHYCFG_RSVD3:** TBD
18	0h RW	**ULPIEXTVBUSINDIACTOR:** Reg field ULPIEXTVBUSINDIACTOR
17	0h RW	**ULPIEXTVBUSDRV:** Reg field ULPIEXTVBUSDRV
16	0h RW	**ULPICLKSUSM:** Reg field ULPICLKSUSM
15	1h RW	**ULPIAUTORES:** flag Value After Reset: 0x0 Reg field ULPIAUTORES
14	0h RO	**GUSB2PHYCFG_RSVD2:** TBD
13:10	9h RW	**USBTRDTIM:** Reg field USBTRDTIM
9	0h RO	**GUSB2PHYCFG_RSVD1:** TBD
8	0h RW	**ENBLSLPM:** Reg field ENBLSLPM
7	0h WO	**PHYSEL:** Reg field PHYSEL
6	0h RW	**SUSPENDUSB20:** SUSPENDUSB20
5	0h RO	**FSINTF:** Reg field FSINTF

Bit Range	Default & Access	Description
4	1h RO	**ULPI_UTMI_Sel:** flag Value After Reset: 0x0 ULPI or UTMI+ Select: The application uses this bit to select a UTMI+ or ULPI Interface. n 1'b0: UTMI+ Interface n 1'b1: ULPI Interface This bit is writable only if UTMI+ and ULPI is specified for High-Speed PHY Interface(s) in coreConsultant configuration (DWC_USB3_HSPHY_INTERFACE = 3). Otherwise, this bit is Read Only and the value depends on the interface selected through DWC_USB3_HSPHY_INTERFACE.
3	0h RW	**PHYIF:** Reg field PHYIF
2:0	0h RW	**TOUTCALIB:** TBD

3.74.102 GUSB2I2CCTL—Offset C240h

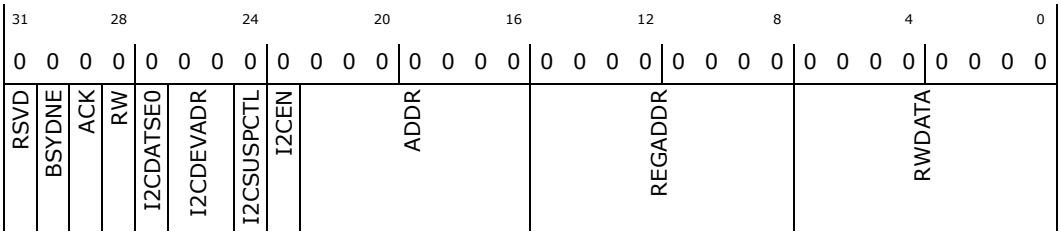
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GUSB2I2CCTL: [BAR] + C240h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**RSVD:** TBD
30	0h RW	**BSYDNE:** Reg field BSYDNE
29	0h RO	**ACK:** TBD
28	0h RW	**RW:** TBD
27	0h RW	**I2CDATSE0:** Reg field I2CDATSE0
26:25	0h RW	**I2CDEVADR:** Reg field I2CDEVADR
24	0h RW	**I2CSUSPCTL:** Reg field I2CSUSPCTL
23	0h RW	**I2CEN:** Reg field I2CEN

Bit Range	Default & Access	Description
22:16	0h RW	**ADDR:** Reg field ADDR
15:8	0h RW	**REGADDR:** Reg field REGADDR
7:0	0h RW	**RWDATA:** Reg field RWDATA

3.74.103 GUSB2PHYACC—Offset C280h

TBD

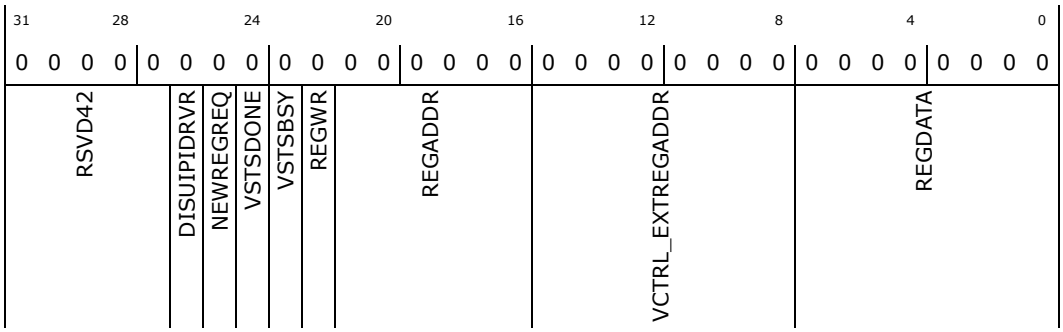
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GUSB2PHYACC: [BAR] + C280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:27	0h RO	**RSVD42:** reserved
26	0h RO	**DISUIPIDRVR:** Reg field DISUIPIDRVR
25	0h RO	**NEWREGREQ:** Reg field NEWREGREQ
24	0h RO	**VSTSDONE:** Reg field VSTSDONE
23	0h RO	**VSTSBSY:** Reg field VSTSBSY
22	0h RO	**REGWR:** Reg field REGWR
21:16	0h RO	**REGADDR:** Reg field REGADDR

Bit Range	Default & Access	Description
15:8	0h RO	**VCTRL_EXTREGADDR:** TDB
7:0	0h RO	**REGDATA:** Reg field REGDATA

3.74.104 GUSB3PIPECTL—Offset C2C0h

flag Value After Reset: 0x2020002

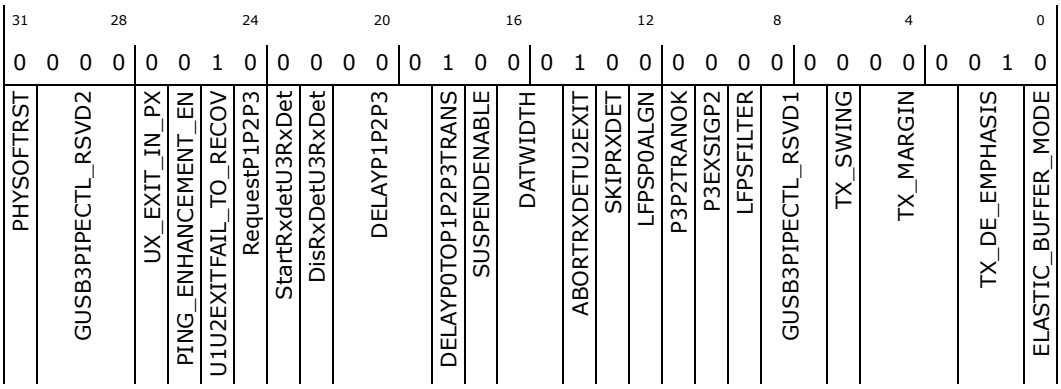
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

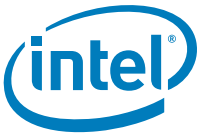
GUSB3PIPECTL: [BAR] + C2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 02044002h



Bit Range	Default & Access	Description
31	0h RW	**PHYSOFTRST:** Reg field PHYSOFTRST
30:28	0h RO	**GUSB3PIPECTL_RSVD2:**
27	0h RW	**UX_EXIT_IN_PX:** Ux Exit in Px: n 0: The core does U1/U2/U3 exit in PHY power state P0 (default behavior) n 1: The core does U1/U2/U3 exit in PHY power state P1/P2/P3 respectively This bit is added for SS PHY workaround where SS PHY injects a glitch on pipe3_RxElecIdle while receiving Ux exit LFPS, and pipe3_PowerDown change is in progress. Note: This bit is used by third-party SS PHY. It should be set to '0' for Synopsys PHY.
26	0h RW	**PING_ENHANCEMENT_EN:** Ping Enhancement Enable: When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns (one mac3_clk). This field is valid for Downstream port only. Note: This bit is used by third-party SS PHY. It should be set to '0' for Synopsys PHY.



Bit Range	Default & Access	Description
25	1h RW	**U1U2EXITFAIL_TO_RECOV:** Reg field u1u2exitfail_to_recov
24	0h RW	**REQUESTp1p2p3 (RequestP1P2P3):** TBD
23	0h RW	**STARTRXDETU3RXDET (StartRxdetU3RxDet):** Reg field StartRxDetU3RxDet
22	0h RW	**DISRXDETU3RXDET (DisRxDetU3RxDet):** Disable Receiver Detection in U3/Rx.Det: When set, the core does not do receiver detection in U3 or Rx.Detect state. DWC_USB3_GUSB3PIPECTL_INIT[23] should be used to start receiver detection manually. This bit is valid for Downstream ports only. Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until (DWC_USB3_GUSB3PIPECTL_INIT[21:19]*8) 8B10B error occurs, or Pipe3_RxValid drops to 0. DWC_USB3_GUSB3PIPECTL_INIT[18] must be 1 to enable this functionality. Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively. n 1'b1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIlde is 1 and pipe3_RxValid is 0 n 1'b0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIlde and pipe3_RxValid. Note: This bit should be set to '1' for Synopsys PHY. It is also used by third-party SS PHY.
21:19	0h RW	**DELAYP1P2P3:** Reg field DelayP1P2P3
18	1h RW	**DELAYP0TOP1P2P3TRANS:** TBD
17	0h RW	**SUSPENDENABLE:** Reg field SUSPENDENABLE
16:15	0h RO	**DATWIDTH:** Reg field DATWIDTH
14	1h RW	**ABORTRXDETU2EXIT:** TBD
13	0h RW	**SKIPRXDET:** Skip Rx Detect: When set, the core skips Rx Detection if pipe3_RxElecIdle is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation.
12	0h RW	**LFPSP0ALGN:** LFPS P0 Align: When set, n The core deasserts LFPS transmission on the clock edge that it requests Phy power state 0 when exiting U1, U2, or U3 low power states. Otherwise, LFPS transmission is asserted one clock earlier. n The core requests symbol transmission two pipe3_rx_pclks periods after the PHY asserts PhyStatus as a result of the PHY switching from P1 or P2 state to P0 state. Currently, this bit is only used in USB 3.0 HUB with Synopsys PHY. For other USB 3.0 Host, Device, and DRD cores, this is not required.
11	0h RW	**P3P2TRANOK:** Reg field P3P2TranOK
10	0h RW	**P3EXSIGP2:** Reg field P3ExSigP2
9	0h RW	**LFPSFILTER:** Reg field LFPSFILTER
8:7	0h RO	**GUSB3PIPECTL_RSVD1:** TBD

Bit Range	Default & Access	Description
6	0h RW	**TX_SWING:** Reg field TX_SWING
5:3	0h RW	**TX_MARGIN:** Reg field TX_MARGIN
2:1	1h RW	**TX_DE_EMPHASIS:** TBD
0	0h RW	**ELASTIC_BUFFER_MODE:** Reg field ELASTIC_BUFFER_MODE

3.74.105 GTXFIFOSIZ0—Offset C300h

TBD

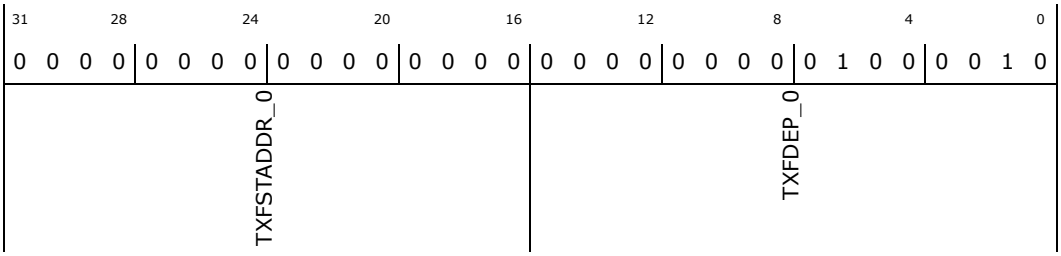
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ0: [BAR] + C300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000042h



Bit Range	Default & Access	Description
31:16	0h RW	**TXFSTADDR_0:** Reserved.
15:0	0042h RW	**TXFDEP_0:**

3.74.106 GTXFIFOSIZ1—Offset C304h

TBD

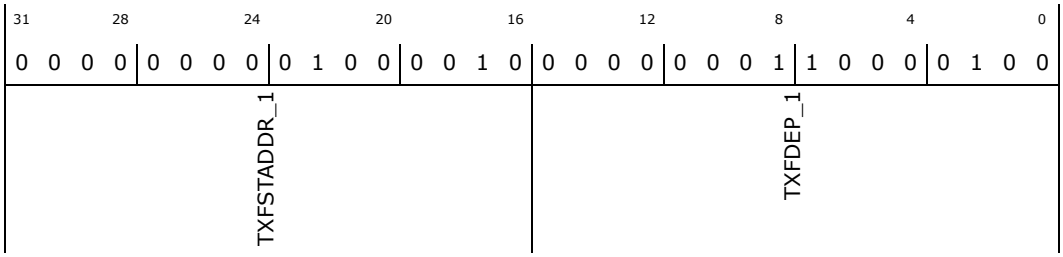
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ1: [BAR] + C304h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00420184h



Bit Range	Default & Access	Description
31:16	0042h RW	**TXFSTADDR_1:** TBD
15:0	0184h RW	**TXFDEP_1:** TBD

3.74.107 GTXFIFOSIZ2—Offset C308h

TBD

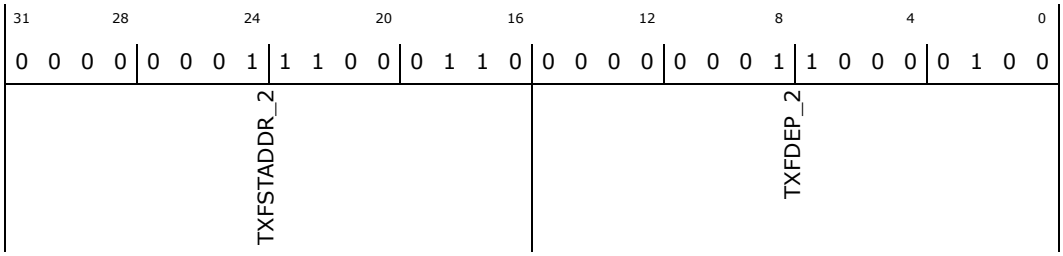
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ2: [BAR] + C308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 01C60184h



Bit Range	Default & Access	Description
31:16	01c6h RW	**TXFSTADDR_2:** TBD
15:0	0184h RW	**TXFDEP_2:** Reserved.

3.74.108 GTXFIFOSIZ3—Offset C30Ch

TBD

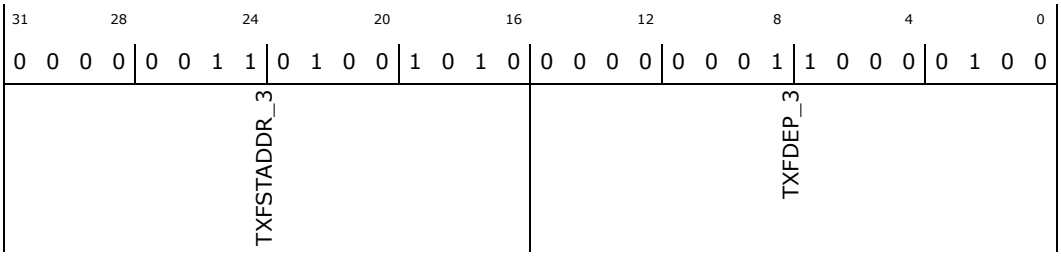
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ3: [BAR] + C30Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 034A0184h



Bit Range	Default & Access	Description
31:16	034ah RW	**TXFSTADDR_3:** TBD
15:0	0184h RW	**TXFDEP_3:** TBD

3.74.109 GTXFIFOSIZ4—Offset C310h

TBD

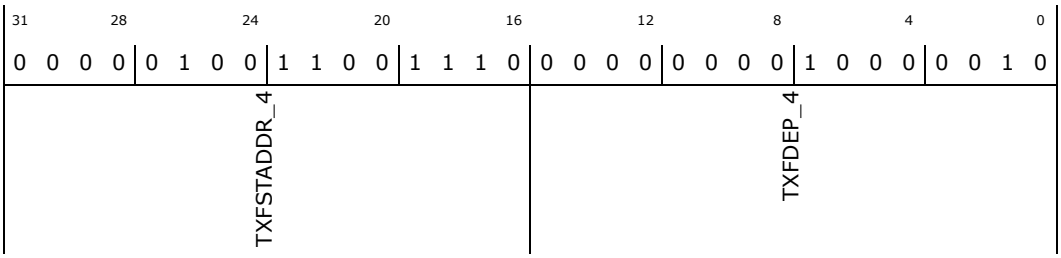
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ4: [BAR] + C310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 04CE0082h



Bit Range	Default & Access	Description
31:16	04ceh RW	**TXFSTADDR_4:** TBD
15:0	0082h RW	**TXFDEP_4:** TBD

3.74.110 GTXFIFOSIZ5—Offset C314h

TBD

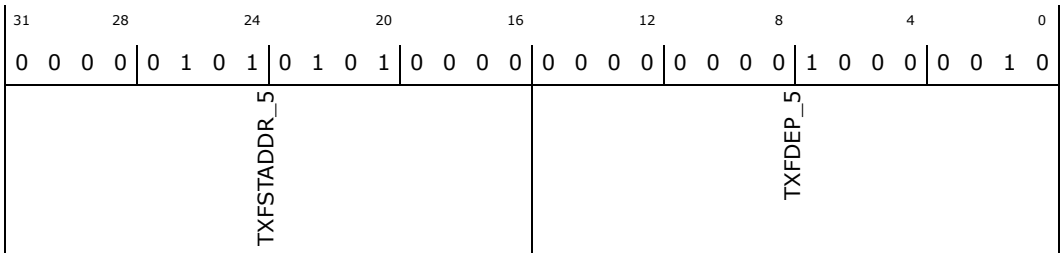
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ5: [BAR] + C314h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 05500082h



Bit Range	Default & Access	Description
31:16	0550h RW	**TXFSTADDR_5:** TBD
15:0	0082h RW	**TXFDEP_5:** TBD

3.74.111 GTXFIFOSIZ6—Offset C318h

TBD

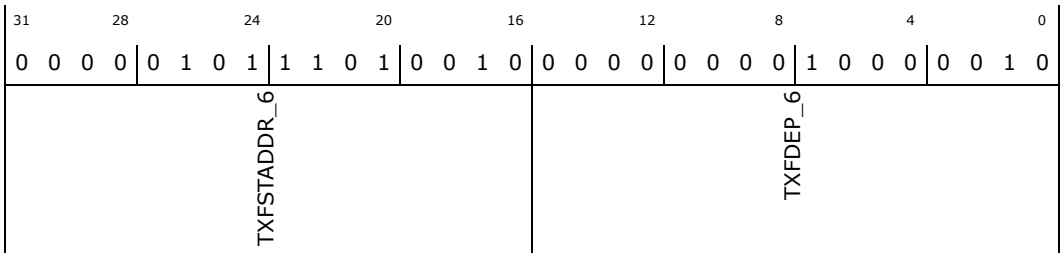
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ6: [BAR] + C318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 05D20082h



Bit Range	Default & Access	Description
31:16	05d2h RW	**TXFSTADDR_6:** TBD
15:0	0082h RW	**TXFDEP_6:** TBD

3.74.112 GTXFIFOSIZ7—Offset C31Ch

TBD

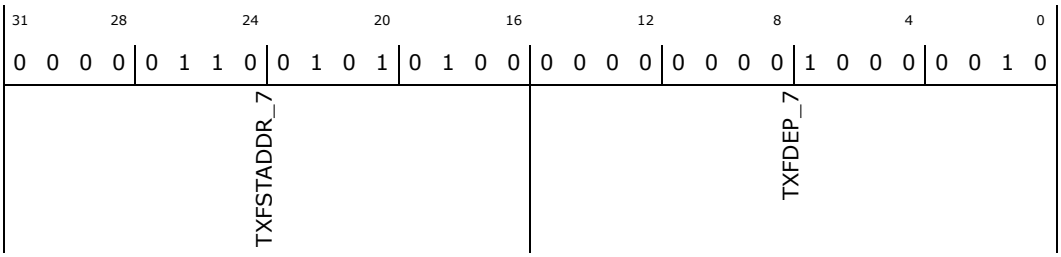
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ7: [BAR] + C31Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 06540082h



Bit Range	Default & Access	Description
31:16	0654h RW	**TXFSTADDR_7:** TBD
15:0	0082h RW	**TXFDEP_7:** TBD

3.74.113 GTXFIFOSIZ8—Offset C320h

TBD

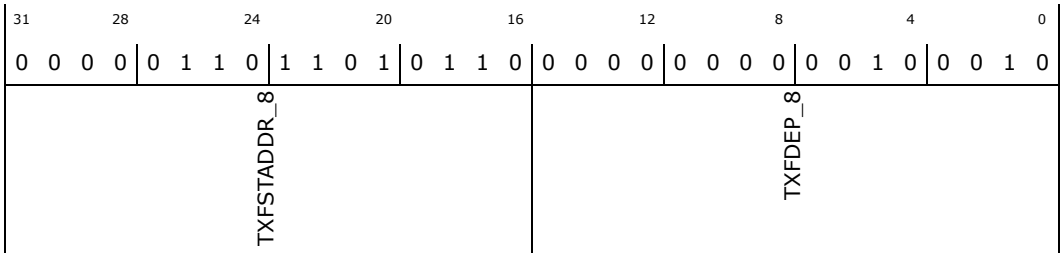
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ8: [BAR] + C320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 06D60022h



Bit Range	Default & Access	Description
31:16	06d6h RW	**TXFSTADDR_8:** TBD
15:0	0022h RW	**TXFDEP_8:** TBD

3.74.114 GTXFIFOSIZ9—Offset C324h

TBD

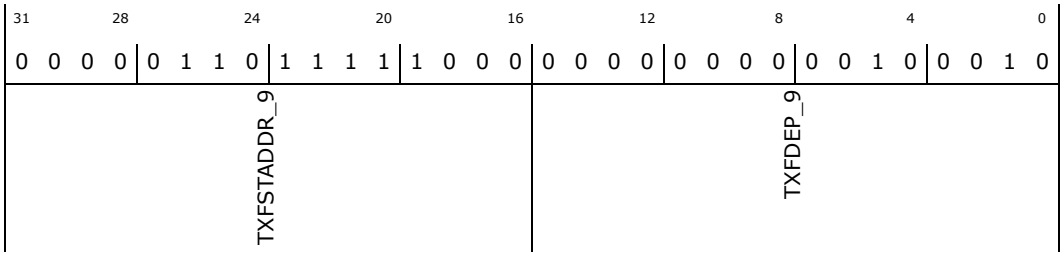
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ9: [BAR] + C324h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 06F80022h



Bit Range	Default & Access	Description
31:16	06f8h RW	**TXFSTADDR_9:** TBD
15:0	0022h RW	**TXFDEP_9:** TBD

3.74.115 GTXFIFOSIZ10—Offset C328h

TBD

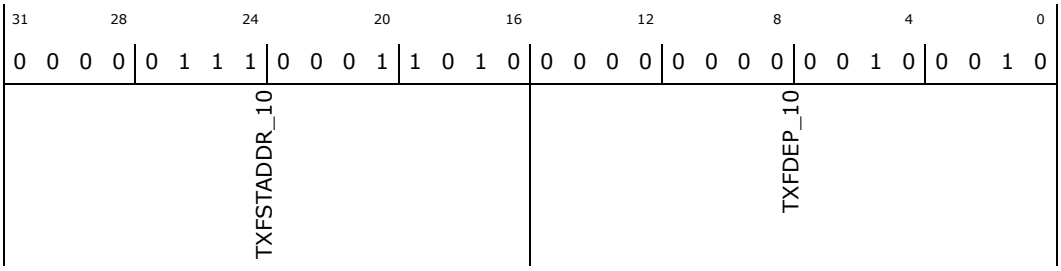
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ10: [BAR] + C328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 071A0022h



Bit Range	Default & Access	Description
31:16	071ah RW	**TXFSTADDR_10:** TBD
15:0	0022h RW	**TXFDEP_10:** TBD

3.74.116 GTXFIFOSIZ11—Offset C32Ch

TBD

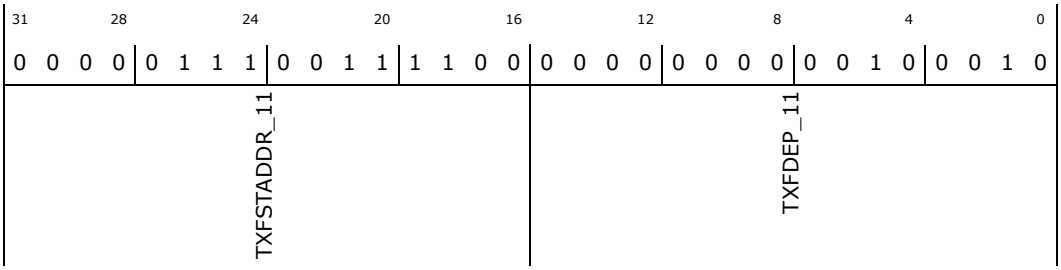
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ11: [BAR] + C32Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 073C0022h



Bit Range	Default & Access	Description
31:16	073ch RW	**TXFSTADDR_11:** TBD
15:0	0022h RW	**TXFDEP_11:** TBD

3.74.117 GTXFIFOSIZ12—Offset C330h

TBD

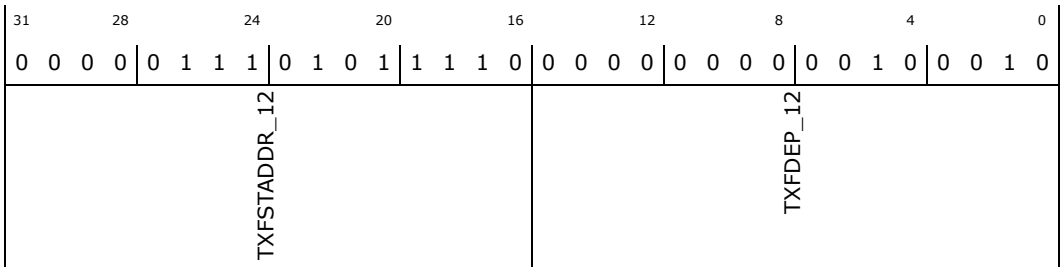
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ12: [BAR] + C330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 075E0022h



Bit Range	Default & Access	Description
31:16	075eh RW	**TXFSTADDR_12:** TBD
15:0	0022h RW	**TXFDEP_12:** TBD

3.74.118 GTXFIFOSIZ13—Offset C334h

TBD

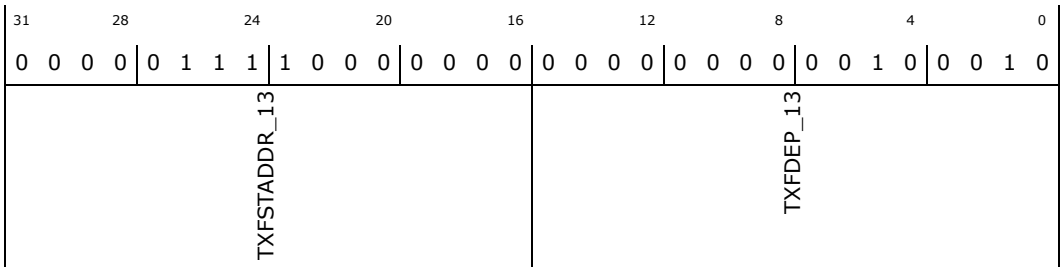
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ13: [BAR] + C334h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 07800022h



Bit Range	Default & Access	Description
31:16	0780h RW	**TXFSTADDR_13:** TBD
15:0	0022h RW	**TXFDEP_13:** TBD

3.74.119 GTXFIFOSIZ14—Offset C338h

TBD

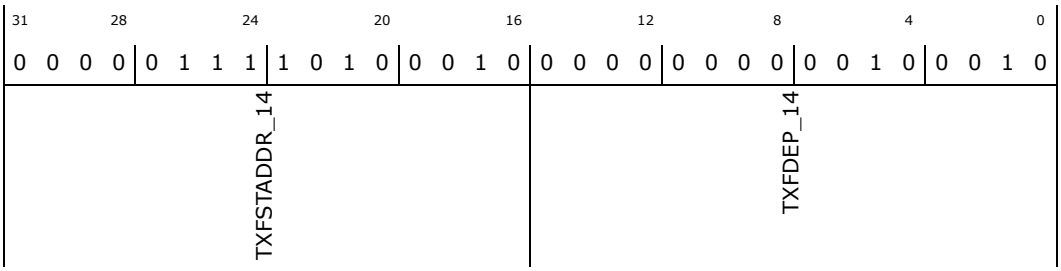
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ14: [BAR] + C338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 07A20022h



Bit Range	Default & Access	Description
31:16	07a2h RW	**TXFSTADDR_14:** TBD
15:0	0022h RW	**TXFDEP_14:** TBD

3.74.120 GTXFIFOSIZ15—Offset C33Ch

TBD

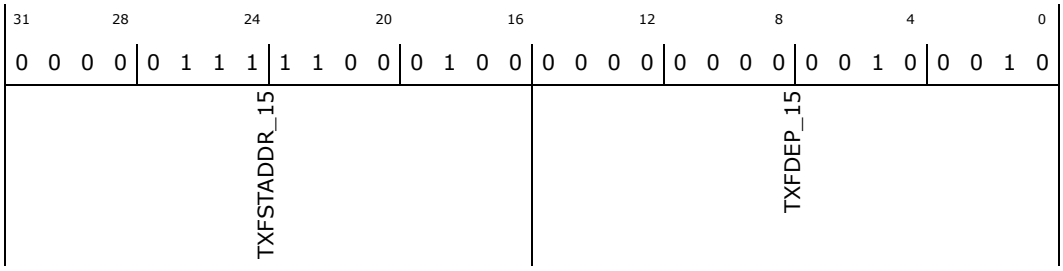
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GTXFIFOSIZ15: [BAR] + C33Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 07C40022h



Bit Range	Default & Access	Description
31:16	07c4h RW	**TXFSTADDR_15:** TBD
15:0	0022h RW	**TXFDEP_15:** TBD

3.74.121 GRXFIFOSIZ0—Offset C380h

TBD

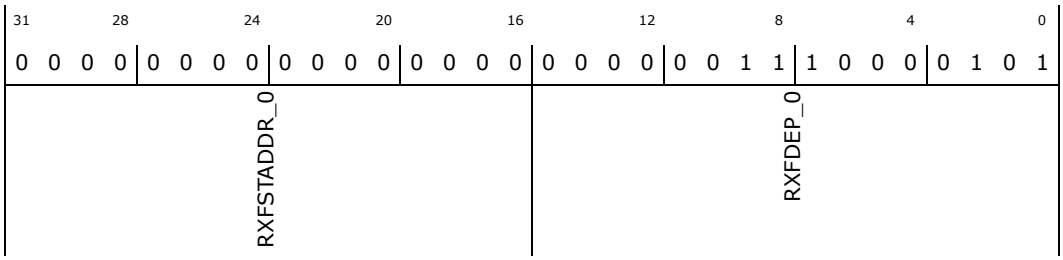
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GRXFIFOSIZ0: [BAR] + C380h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000385h



Bit Range	Default & Access	Description
31:16	0h RW	**RXFSTADDR_0:** TBD
15:0	0385h RW	**RXFDEP_0:** TBD

3.74.122 GRXFIFOSIZ1—Offset C384h

TBD

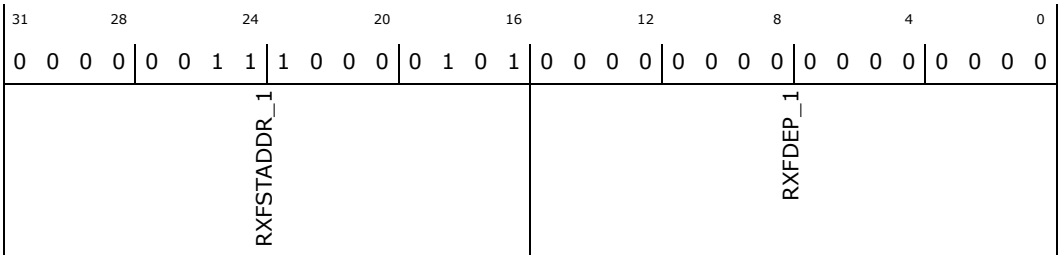
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GRXFIFOSIZ1: [BAR] + C384h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 03850000h



Bit Range	Default & Access	Description
31:16	0385h RW	**RXFSTADDR_1:** TBD
15:0	0000h RW	**RXFDEP_1:** TBD

3.74.123 GRXFIFOSIZ2—Offset C388h

TBD

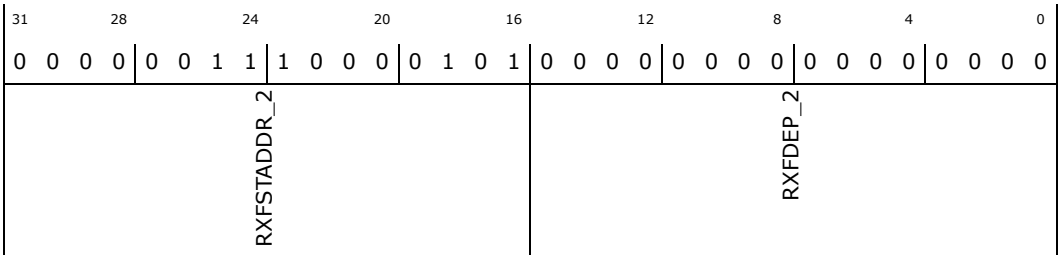
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GRXFIFOSIZ2: [BAR] + C388h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 03850000h



Bit Range	Default & Access	Description
31:16	0385h RW	**RXFSTADDR_2:** TBD
15:0	0h RW	**RXFDEP_2:** TBD

3.74.124 GEVNTADRLO—Offset C400h

TBD

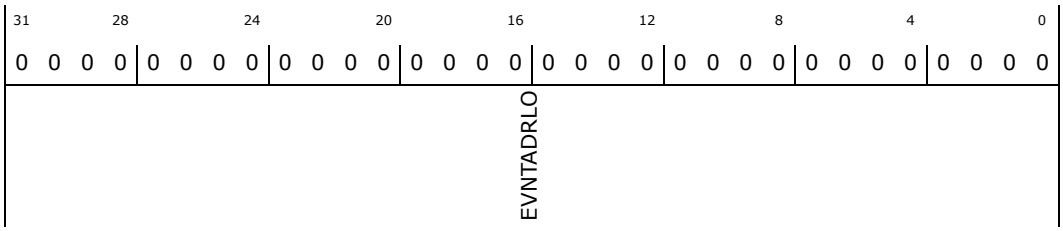
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GEVNTADRLO: [BAR] + C400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**EVNTADRLO:** field EVNTADRLO

3.74.125 GEVNTADRHI—Offset C404h

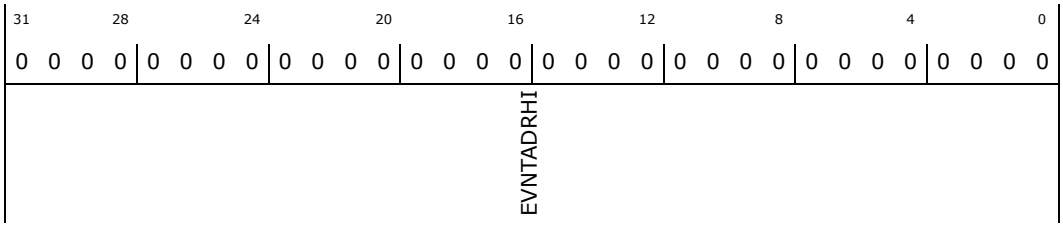
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GEVNTADRHI: [BAR] + C404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**EVNTADRHI:** Reg field EVNTADRHI

3.74.126 GEVNTSIZ—Offset C408h

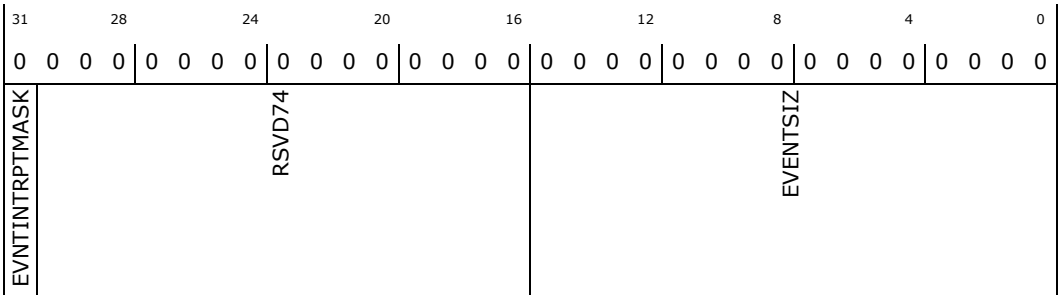
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GEVNTSIZ: [BAR] + C408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**EVNTINTRPTMASK:** Reg field EVNTINTRPTMASK
30:16	0h RO	**RSVD74:** reserved
15:0	0h RW	**EVENTSIZ:** Reg field EVENTSIZ

3.74.127 GEVNTCOUNT—Offset C40Ch

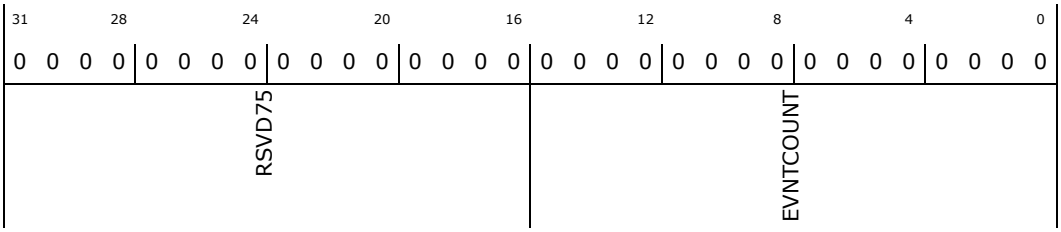
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GEVNTCOUNT: [BAR] + C40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD75:** reserved
15:0	0h RO	**EVNTCOUNT:** Reg field EVNTCOUNT

3.74.128 GHWPARAMS8—Offset C600h

flag Value After Reset: 0xc00 Global Hardware Parameters Register 8

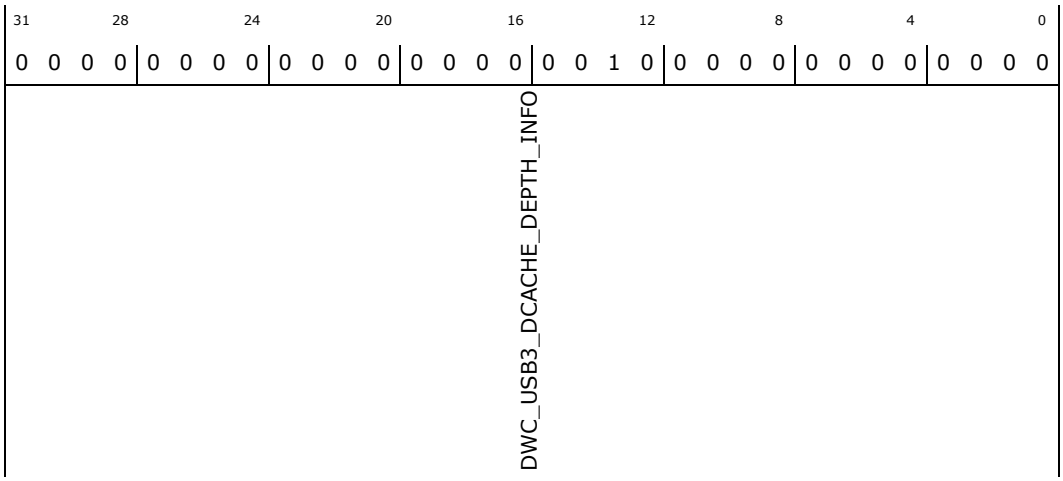
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHWPARAMS8: [BAR] + C600h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00002000h



Bit Range	Default & Access	Description
31:0	2000h RO	**DWC_USB3_DCACHE_DEPTH_INFO:** TBD

3.74.129 DCFG—Offset C700h

flag Value After Reset: 0x80804 Device Configuration Register

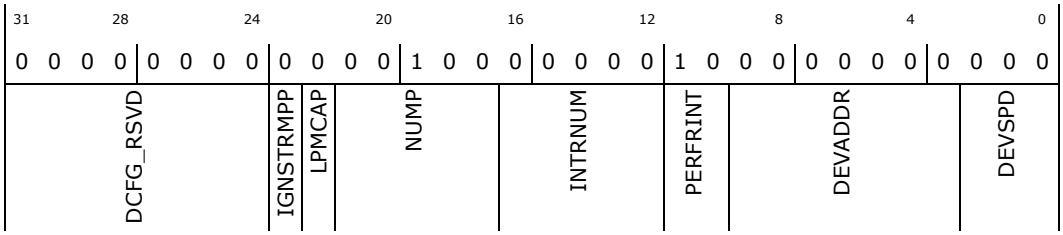
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCFG: [BAR] + C700h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00080800h



Bit Range	Default & Access	Description
31:24	0h RO	**DCFG_RSVD:** TBD
23	0h RW	**IGNSTRMPP:** Reserved
22	0h RW	**LPMCAP:** LPM Capable
21:17	04h RW	**NUMP:** Reg field NUMP
16:12	0h RW	**INTRNUM:** Reg field INTRNUM
11:10	2h RW	**PERFRINT:** Reg field PERFRINT
9:3	0h RW	**DEVADDR:** Reg field DEVADDR
2:0	0h RW	**DEVSPD:** flag Value After Reset: 0x4 Reg field DEVSPD

3.74.130 DCTL—Offset C704h

Device Control Register

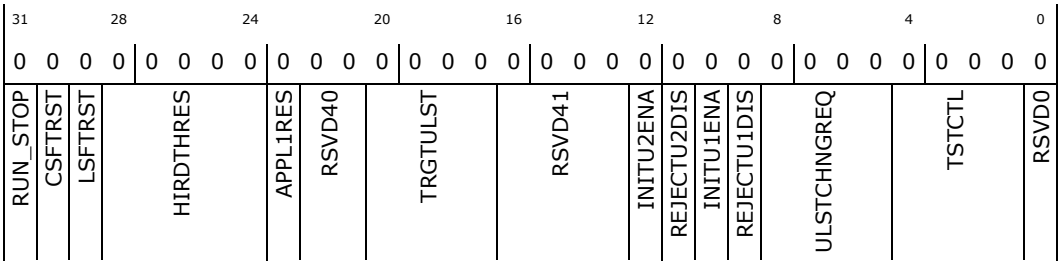
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DCTL: [BAR] + C704h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**RUN_STOP:** Run/Stop
30	0h RW	**CSFTRST:** Core Soft Reset
29	0h RW	**LSFTRST:** Light Soft Reset

Bit Range	Default & Access	Description
28:24	0h RW	**HIRDTHRES:** Reg field HIRDTHRES
23	0h RW	**APPL1RES:** LPM Response Programmed by Application
22:21	0h RO	**RSVD40:** reserved
20:17	0h RW	**TRGTULST:** TBD
16:13	0h RO	**RSVD41:** reserved
12	0h RW	**INITU2ENA:** Initiate U2 Enable
11	0h RW	**REJECTU2DIS:** TBD
10	0h RW	**INITU1ENA:** Compliance
9	0h RW	**REJECTU1DIS:** TBD
8:5	0h RW	**ULSTCHNGREQ:** Reg field ULSTCHNGREQ
4:1	0h RW	**TSTCTL:** Reg field TSTCTL
0	0h RO	**RSVD0:** reserved

3.74.131 DEVTEN—Offset C708h

Device Event Enable Register

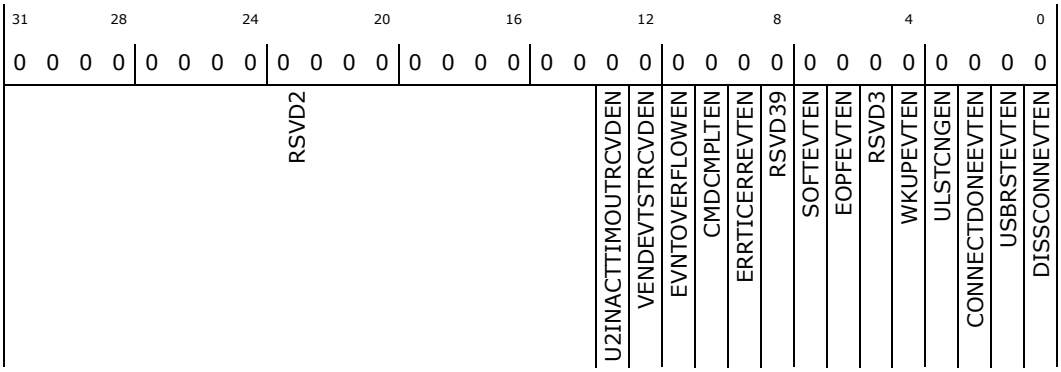
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEVTEN: [BAR] + C708h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RO	**RSVD2:** reserved
13	0h RW	**U2INACTTIMOUTRCVDEN:** U2 Inactivity Timeout LMP Received Event Enable
12	0h RW	**VENDEVTSTRCVDEN:** Vendor Device Test LMP Received Event
11	0h RW	**EVNTOVERFLOWEN:** Event Buffer Overflow Event Enable
10	0h RW	**CMDCMPLTEN:** Generic Command Complete Event Enable
9	0h RW	**ERRTICERREVTEN:** Erratic Error Event Enable
8	0h RW	**RSVD39:** reserved
7	0h RW	**SOFTEVTEN:** Start of
6	0h RW	**EOPFEVTEN:** End of Periodic Frame Event Enable
5	0h RW	**RSVD3:** reserved
4	0h RW	**WKUPEVTEN:** Resume/Remote Wakeup Detected Event Enable
3	0h RW	**ULSTCNGEN:** USB/Link State Change Event Enable
2	0h RW	**CONNECTDONEEVTEN:** Connection Done Enable
1	0h RW	**USBRSTEVTEN:** USB Reset Enable
0	0h RW	**DISSCONNEVTEN:** Disconnect Detected Event Enable

3.74.132 DSTS—Offset C70Ch

flag Value After Reset: 0x20820004 Device Status Register

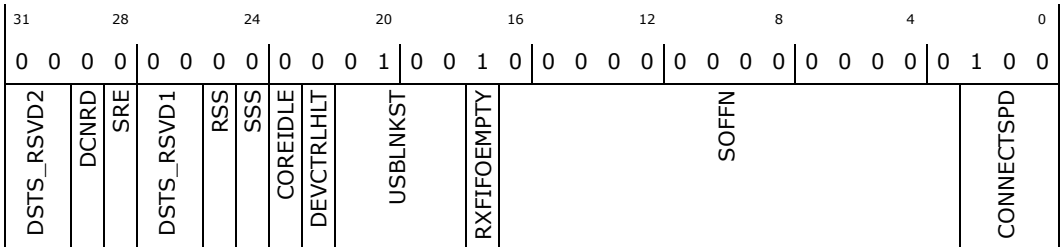
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTS: [BAR] + C70Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00120004h



Bit Range	Default & Access	Description
31:30	0h RO	**DSTS_RSVD2:** TBD
29	0h RO	**DCNRD:** Value After Reset: 0x1 Device Controller Not Ready: The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. Software must wait for this bit to be de-asserted to zero before processing DS TS.USBLnk
28	0h RW	**SRE:** Save/Restore Error (SRE) -RW1C. Default = '0'. If an error occurs during a Save or Restore operation this bit shall be set to '1'. This bit shall be cleared to '0' when a Save or Restore operation is initiated or when written with '1'. Refer to section 4.23.2 for more information. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the Save/Restore completion status for the selected VF. Refer to section 8 for more information.x
27:26	0h RO	**DSTS_RSVD1:** TBD
25	0h RO	**RSS:** Restore State Status: This bit is similar to the USBSTS.RSS in host mode. When the controller has finished the save process, it will complete the command by setting DSTS.RSS to '0'
24	0h RO	**SSS:** Save State Status: This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it will complete the command by setting DSTS.SSS to '0'.
23	0h RO	**COREIDLE:** flag Value After Reset: 0x1 Core Idle
22	0h RO	**DEVCTRLHLT:** Device Controller Halted
21:18	4h RO	**USBLNKST:** flag Value After Reset: 0x0 Reg field USBLNKST
17	1h RO	**RXFIFOEMPTY:** RxFIFO Empty
16:3	0h RO	**SOFFN:** Frame/Microframe Number of the Received SOF: When the core is operating at high-speed, this field contains a microframe number. When the core is operating at full- or low-speed, this field contains a frame number.

Bit Range	Default & Access	Description
2:0	4h RO	**CONNECTSPD:** Reg field CONNECTSPD

3.74.133 DGCMDPAR—Offset C710h

Device Generic Command Parameter Register

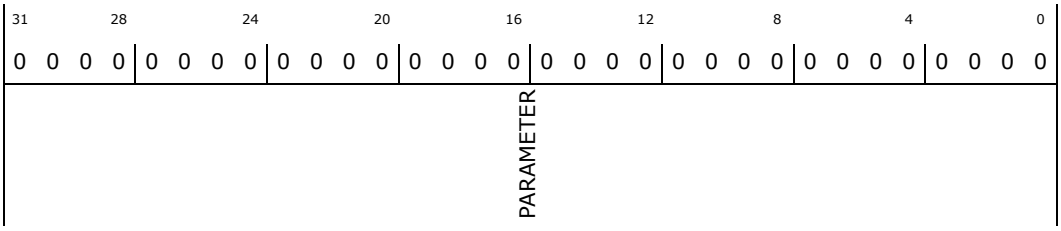
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DGCMDPAR: [BAR] + C710h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reserved.

3.74.134 DGCMD—Offset C714h

Device Generic Command Register

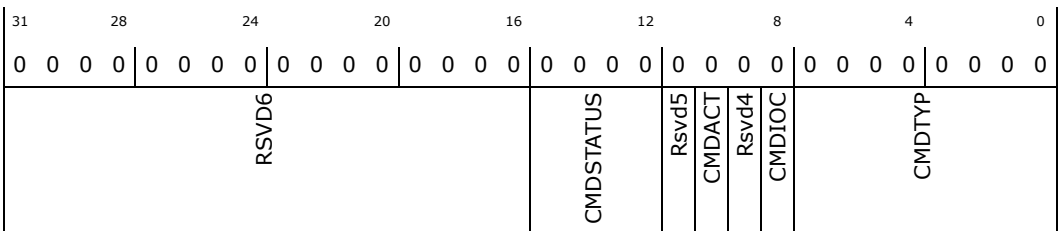
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DGCMD: [BAR] + C714h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RO	**RSVD6:** reserved
15:12	0h RO	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RO	**Rsvd5:** reserved
10	0h WO	**CMDACT:** Command Active
9	0h RO	**Rsvd4:** reserved
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.135 DALEPENA—Offset C720h

Device Active USB Endpoint Enable Register

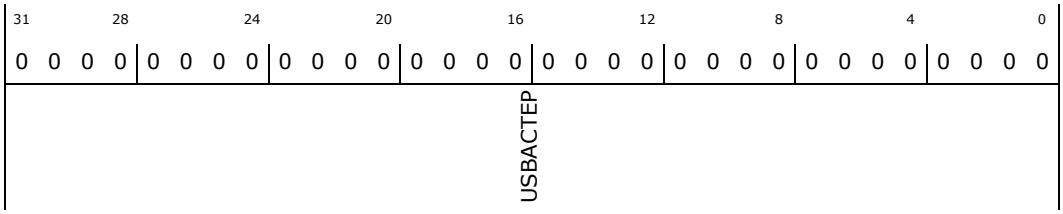
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DALEPENA: [BAR] + C720h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**USBACTEP:** Reg field USBACTEP

3.74.136 DEPCMDPAR2_0—Offset C800h

Reg field PARAMETER

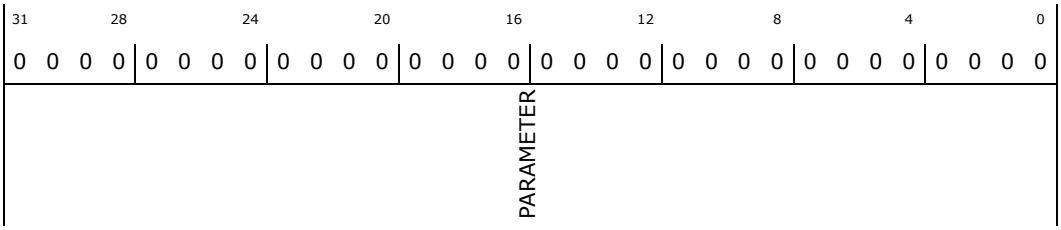
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_0: [BAR] + C800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.137 DEPCMDPAR1_0—Offset C804h

TBD

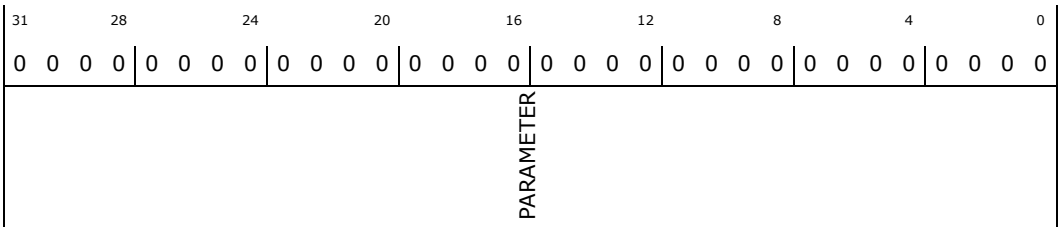
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_0: [BAR] + C804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.138 DEPCMDPAR0_0—Offset C808h

TBD

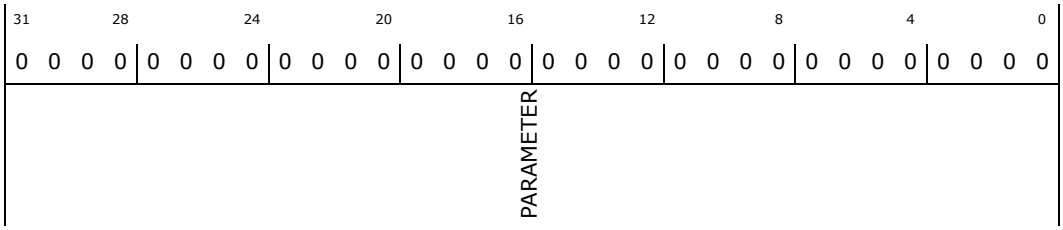
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_0: [BAR] + C808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.139 DEPCMD_0—Offset C80Ch

TBD

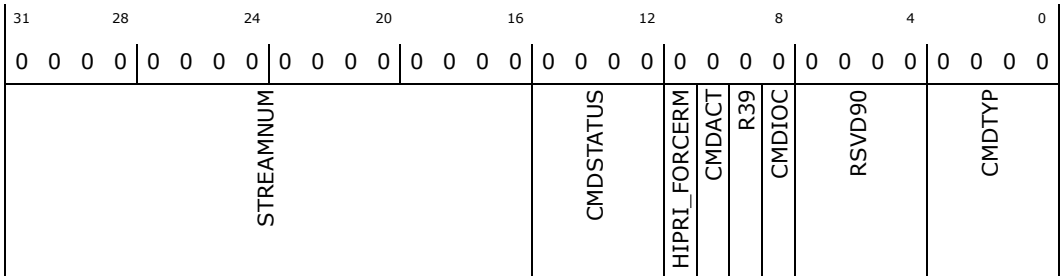
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_0: [BAR] + C80Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.140 DEPCMDPAR2_1—Offset C810h

TBD

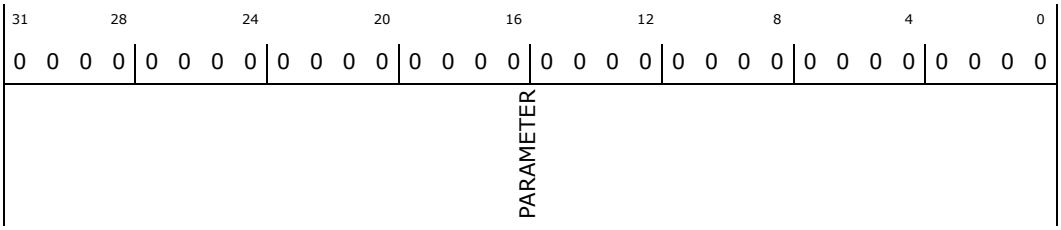
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_1: [BAR] + C810h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.141 DEPCMDPAR1_1—Offset C814h

TBD

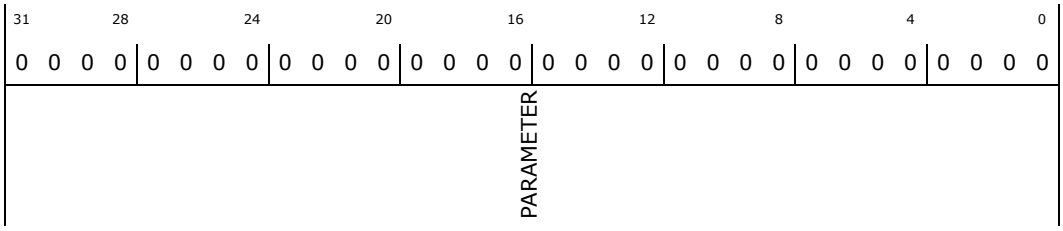
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_1: [BAR] + C814h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.142 DEPCMDPAR0_1—Offset C818h

TBD

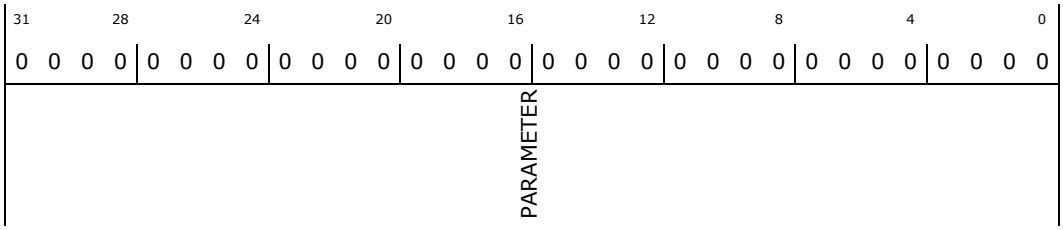
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_1: [BAR] + C818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.143 DEPCMD_1—Offset C81Ch

TBD

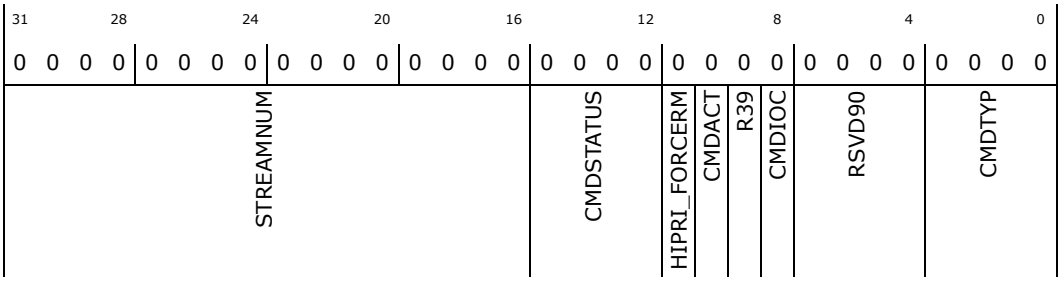
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_1: [BAR] + C81Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.144 DEPCMDPAR2_2—Offset C820h

TBD

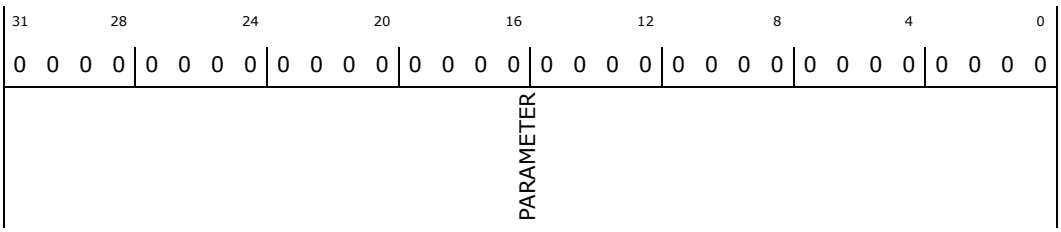
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_2: [BAR] + C820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.145 DEPCMDPAR1_2—Offset C824h

TBD

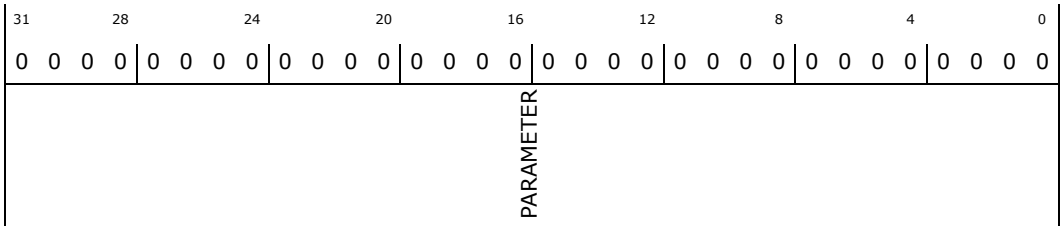
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_2: [BAR] + C824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.146 DEPCMDPAR0_2—Offset C828h

TBD

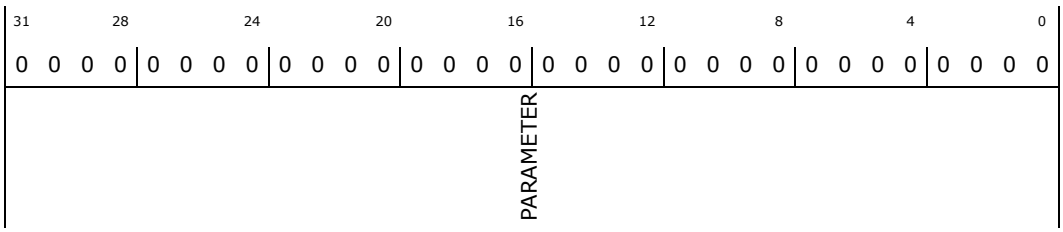
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_2: [BAR] + C828h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.147 DEPCMD_2—Offset C82Ch

TBD

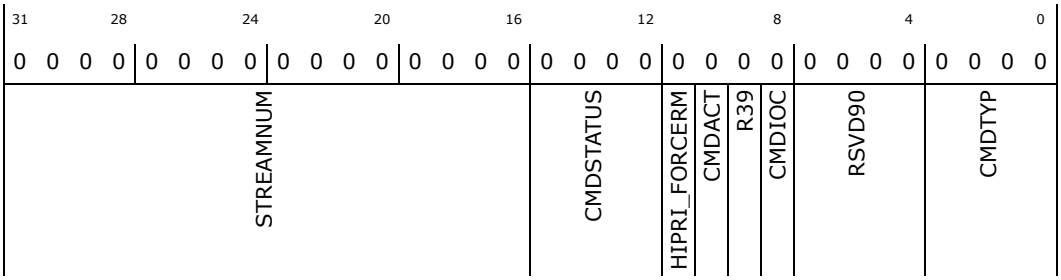
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_2: [BAR] + C82Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.148 DEPCMDPAR2_3—Offset C830h

TBD

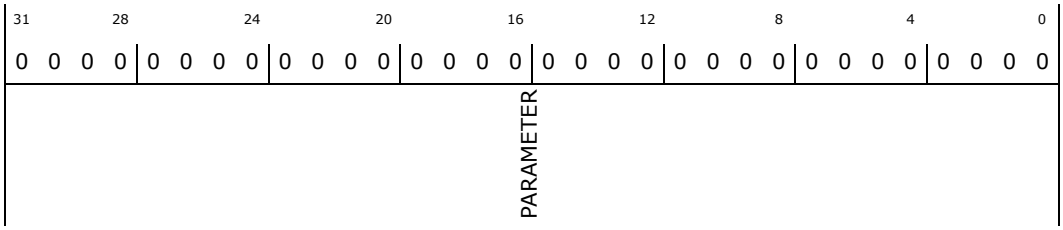
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_3: [BAR] + C830h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.149 DEPCMDPAR1_3—Offset C834h

TBD

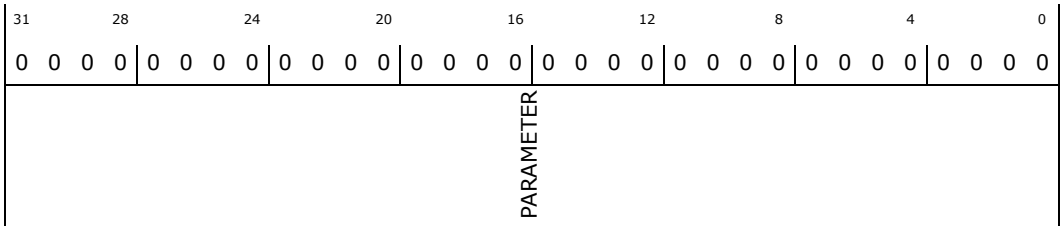
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_3: [BAR] + C834h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.150 DEPCMDPAR0_3—Offset C838h

TBD

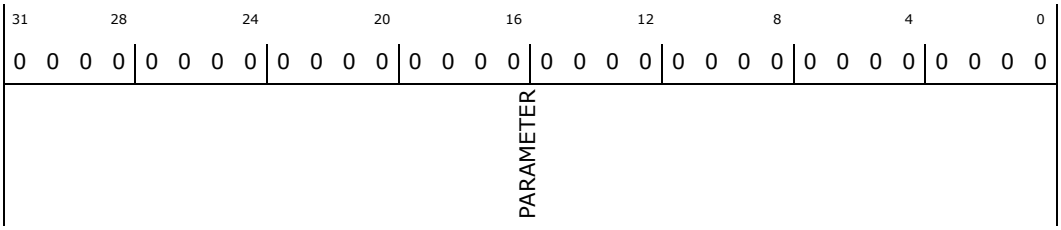
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_3: [BAR] + C838h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.151 DEPCMD_3—Offset C83Ch

TBD

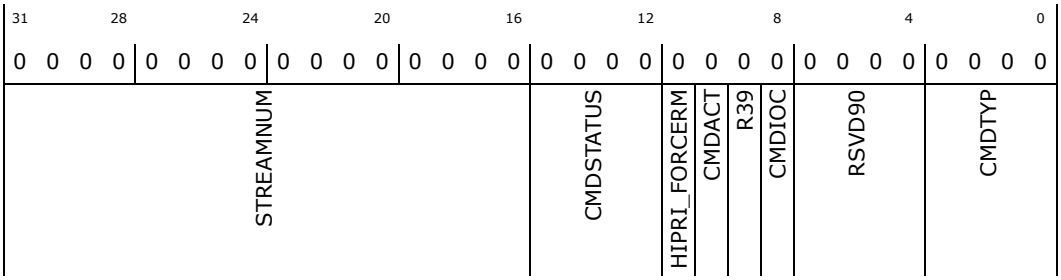
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_3: [BAR] + C83Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.152 DEPCMDPAR2_4—Offset C840h

TBD

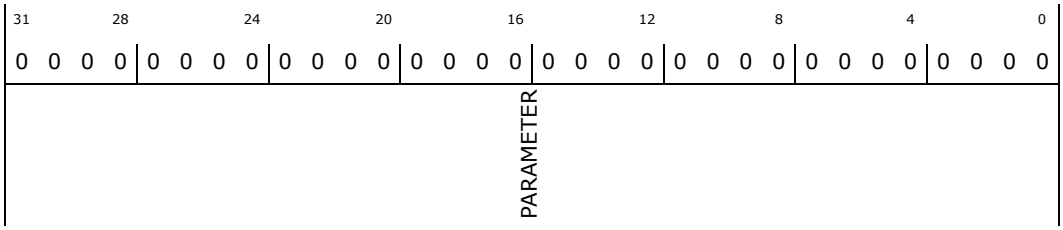
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_4: [BAR] + C840h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.153 DEPCMDPAR1_4—Offset C844h

TBD

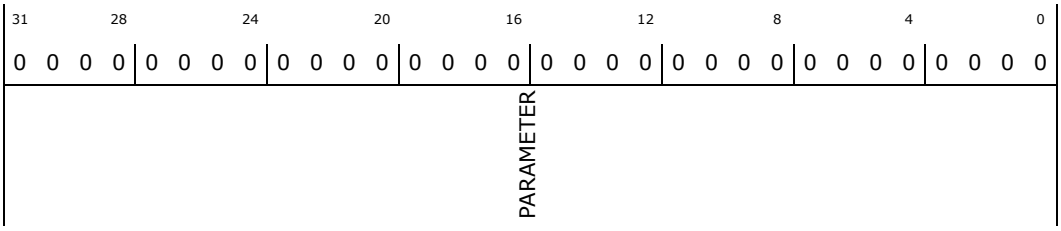
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_4: [BAR] + C844h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.154 DEPCMDPAR0_4—Offset C848h

TBD

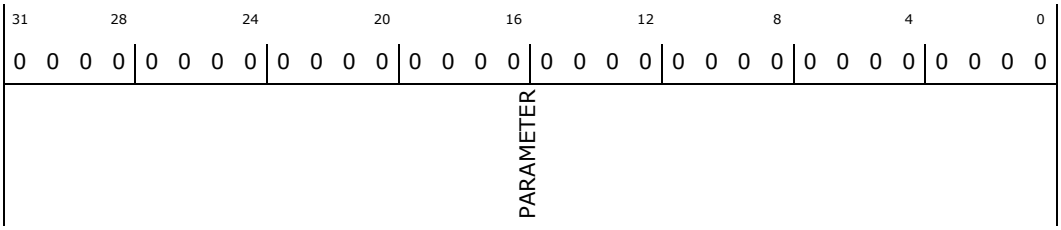
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_4: [BAR] + C848h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.155 DEPCMD_4—Offset C84Ch

TBD

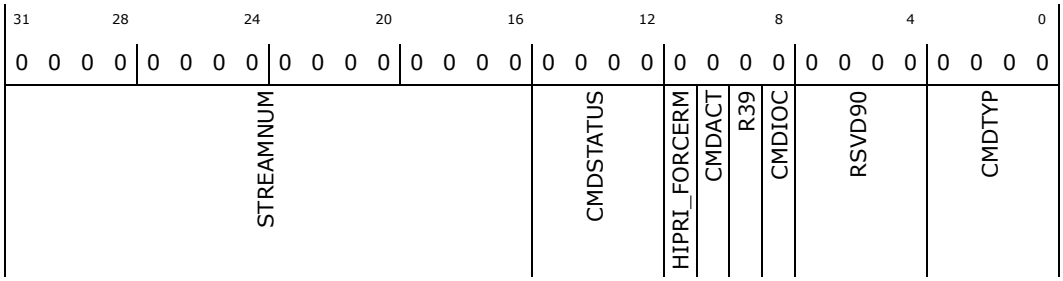
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_4: [BAR] + C84Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.156 DEPCMDPAR2_5—Offset C850h

TBD

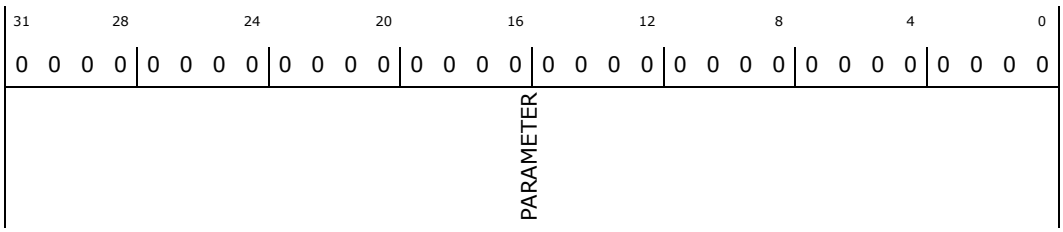
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_5: [BAR] + C850h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reserved.

3.74.157 DEPCMDPAR1_5—Offset C854h

TBD

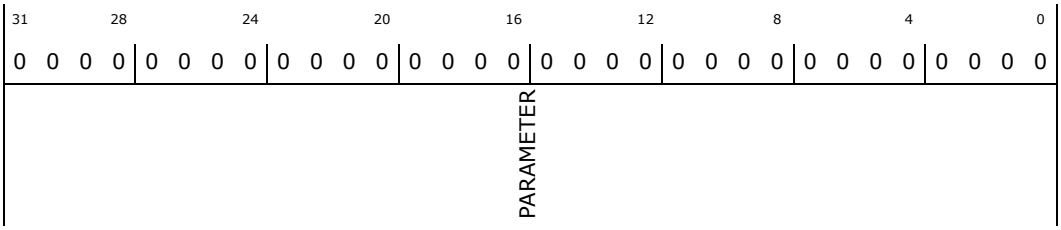
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_5: [BAR] + C854h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reserved.

3.74.158 DEPCMDPAR0_5—Offset C858h

TBD

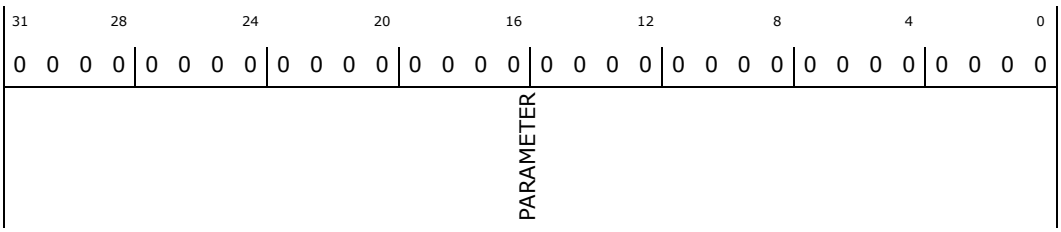
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_5: [BAR] + C858h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.159 DEPCMD_5—Offset C85Ch

TBD

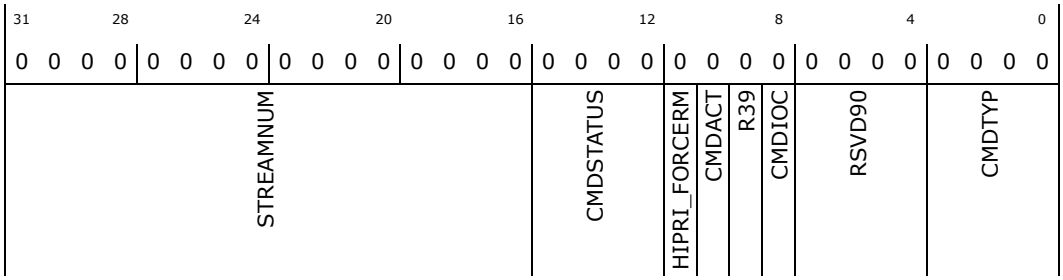
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_5: [BAR] + C85Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.160 DEPCMDPAR2_6—Offset C860h

TBD

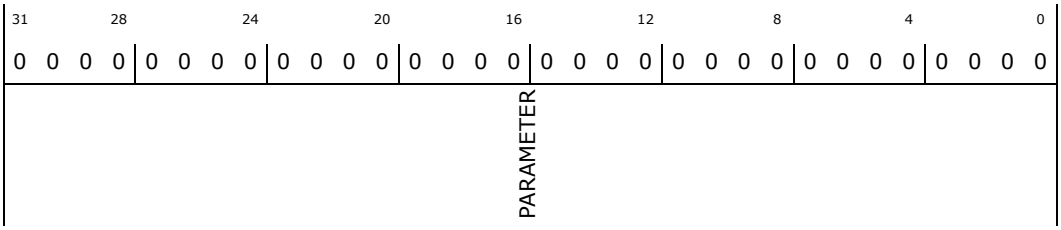
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_6: [BAR] + C860h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.161 DEPCMDPAR1_6—Offset C864h

TBD

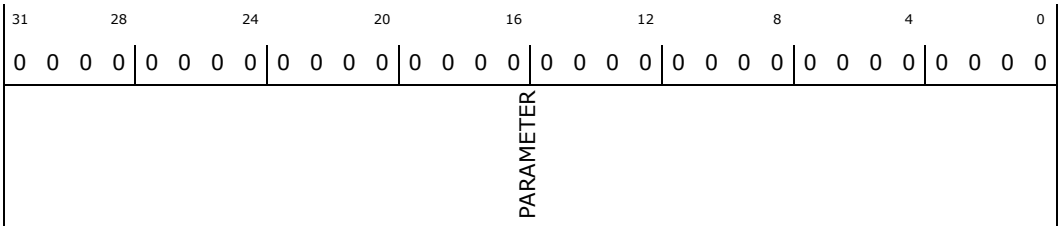
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_6: [BAR] + C864h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.162 DEPCMDPAR0_6—Offset C868h

TBD

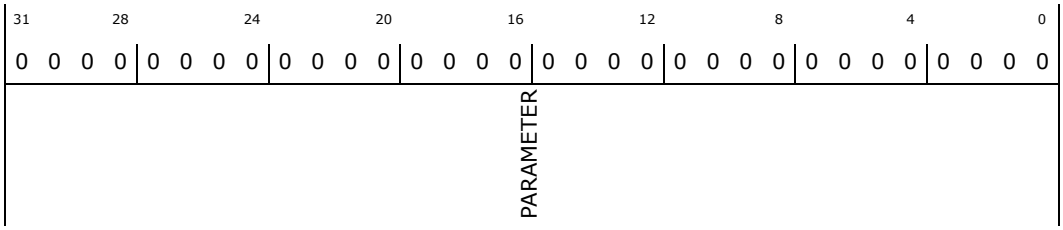
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_6: [BAR] + C868h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.163 DEPCMD_6—Offset C86Ch

TBD

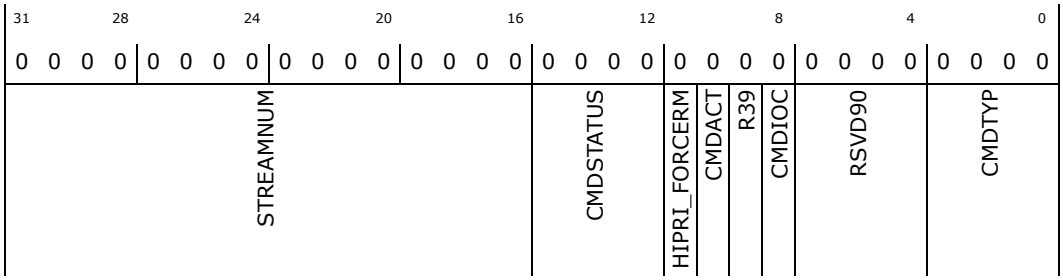
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_6: [BAR] + C86Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.164 DEPCMDPAR2_7—Offset C870h

TBD

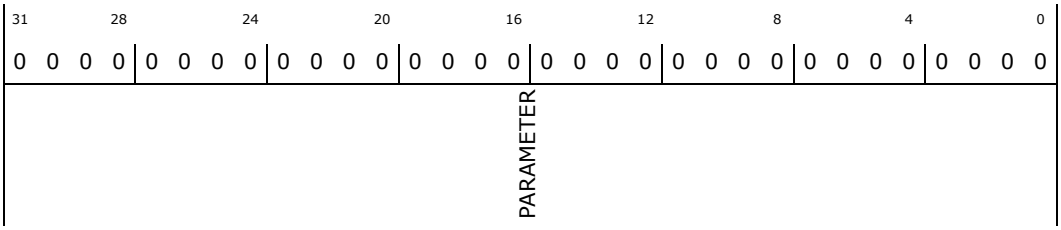
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_7: [BAR] + C870h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.165 DEPCMDPAR1_7—Offset C874h

TBD

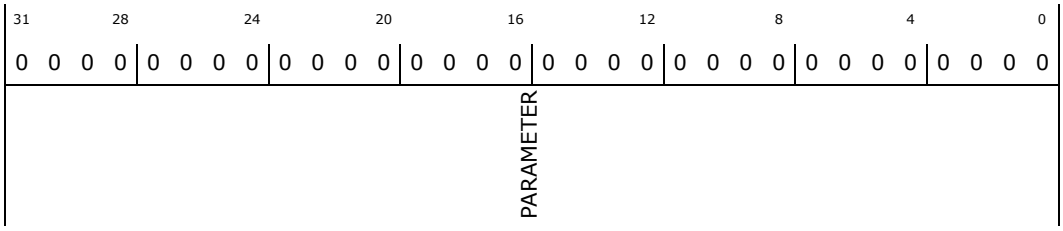
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_7: [BAR] + C874h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.166 DEPCMDPAR0_7—Offset C878h

TBD

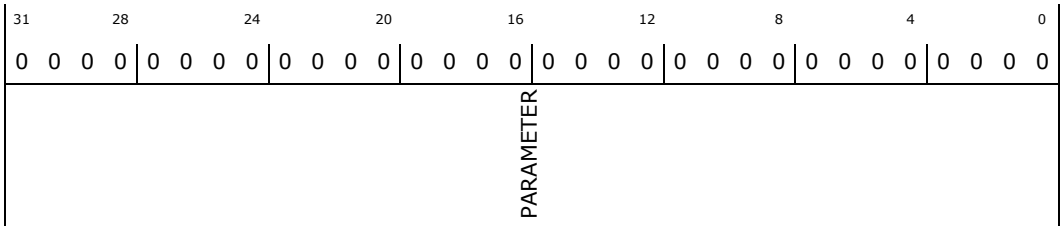
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_7: [BAR] + C878h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.167 DEPCMD_7—Offset C87Ch

TBD

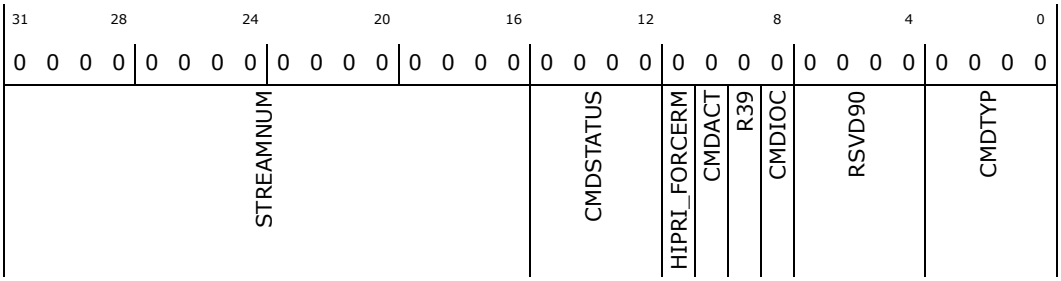
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_7: [BAR] + C87Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.168 DEPCMDPAR2_8—Offset C880h

TBD

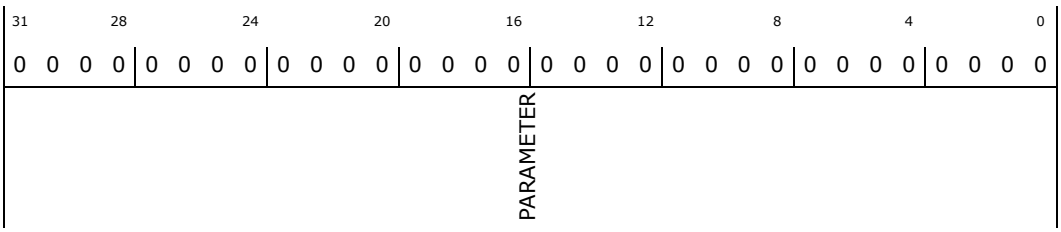
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_8: [BAR] + C880h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.169 DEPCMDPAR1_8—Offset C884h

TBD

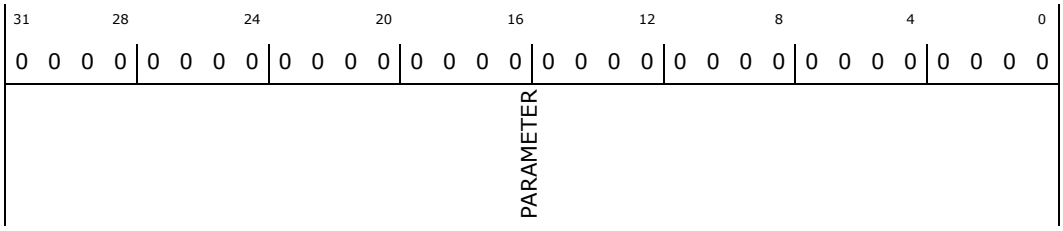
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_8: [BAR] + C884h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.170 DEPCMDPAR0_8—Offset C888h

TBD

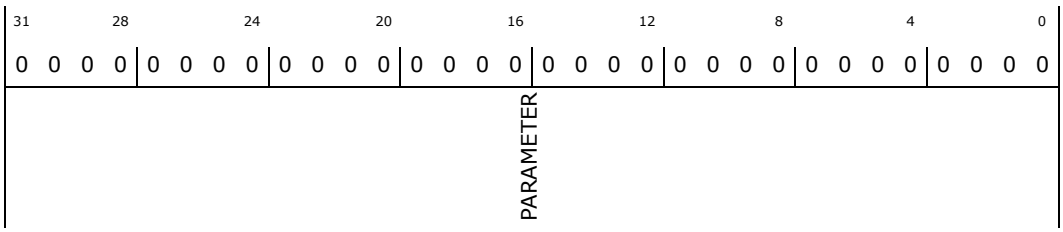
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_8: [BAR] + C888h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.171 DEPCMD_8—Offset C88Ch

TBD

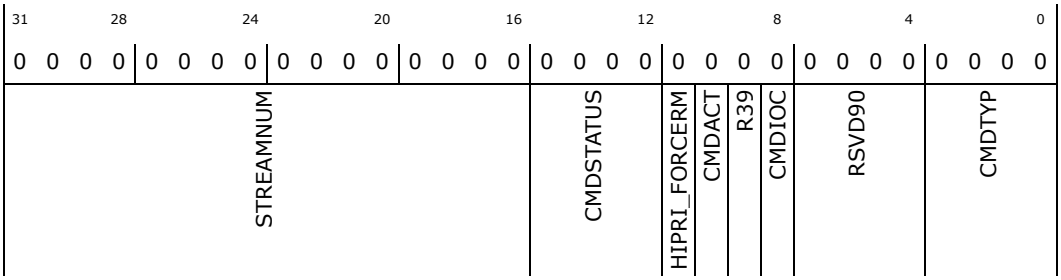
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_8: [BAR] + C88Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.172 DEPCMDPAR2_9—Offset C890h

TBD

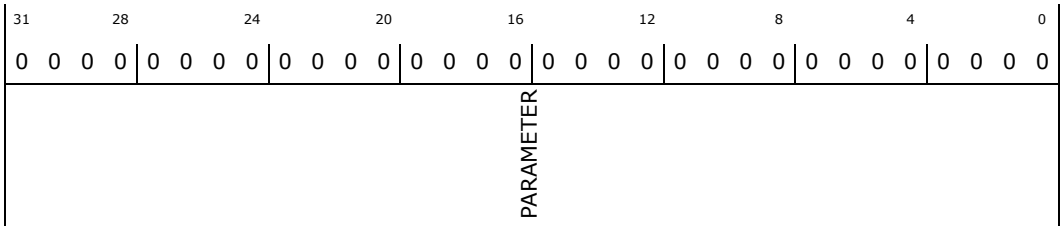
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_9: [BAR] + C890h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.173 DEPCMDPAR1_9—Offset C894h

TBD

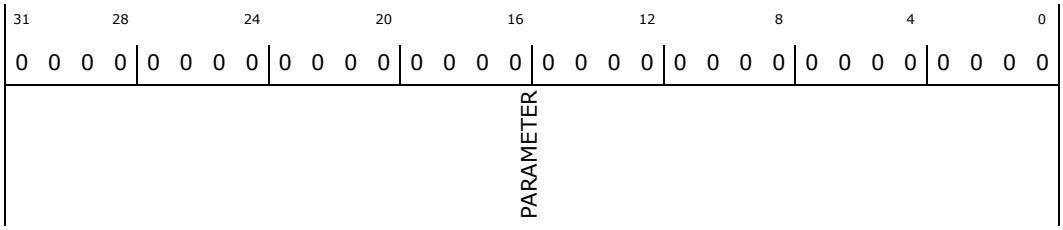
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_9: [BAR] + C894h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.174 DEPCMDPAR0_9—Offset C898h

TBD

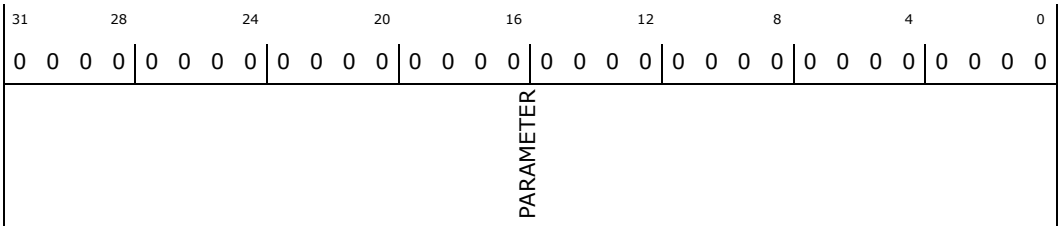
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_9: [BAR] + C898h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.175 DEPCMD_9—Offset C89Ch

TBD

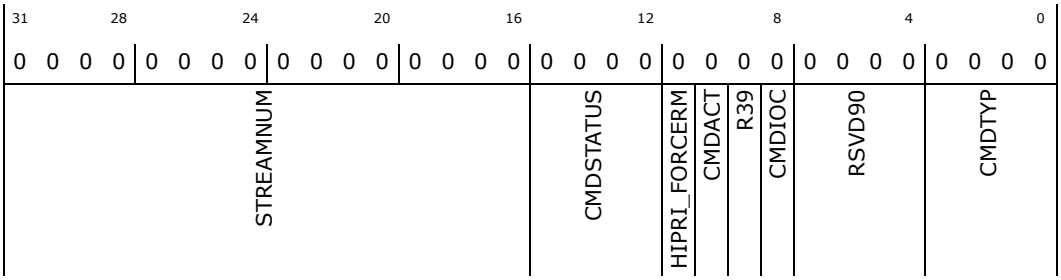
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_9: [BAR] + C89Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.176 DEPCMDPAR2_10—Offset C8A0h

TBD

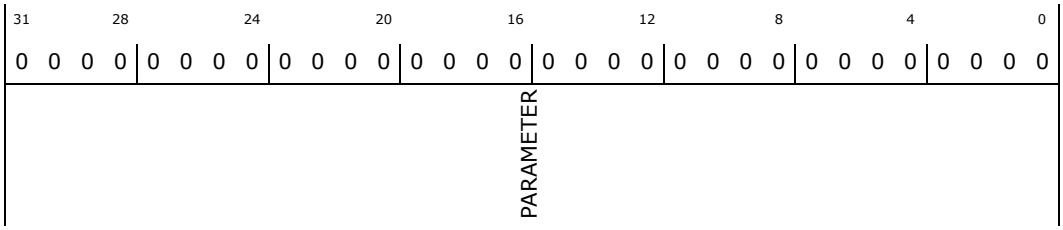
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_10: [BAR] + C8A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.177 DEPCMDPAR1_10—Offset C8A4h

TBD

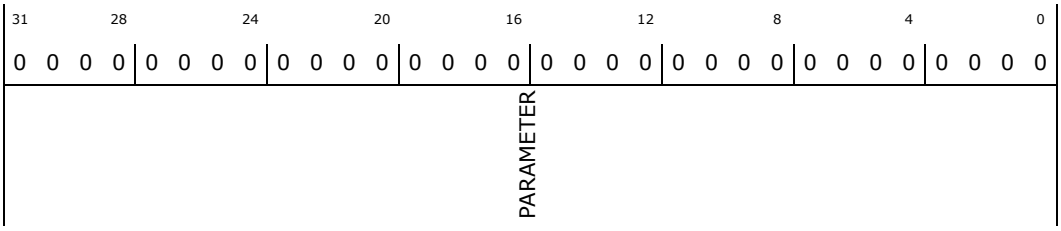
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_10: [BAR] + C8A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.178 DEPCMDPAR0_10—Offset C8A8h

TBD

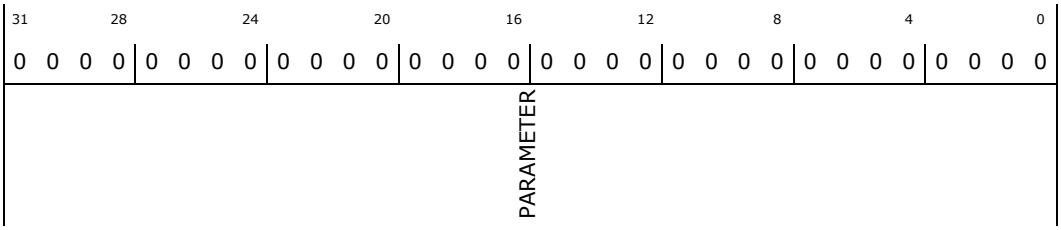
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_10: [BAR] + C8A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.179 DEPCMD_10—Offset C8ACh

TBD

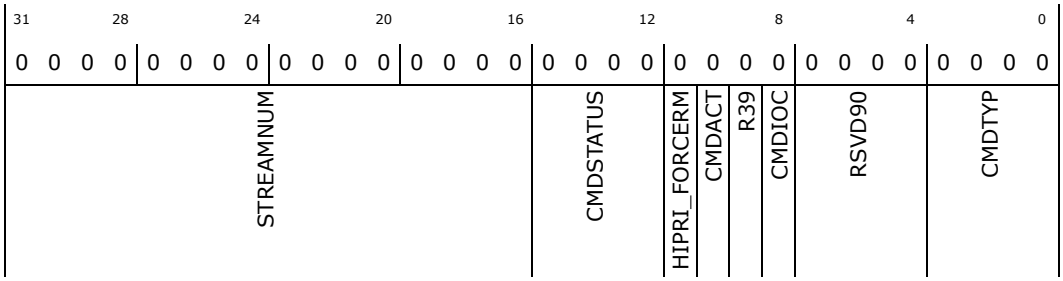
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_10: [BAR] + C8ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.180 DEPCMDPAR2_11—Offset C8B0h

TBD

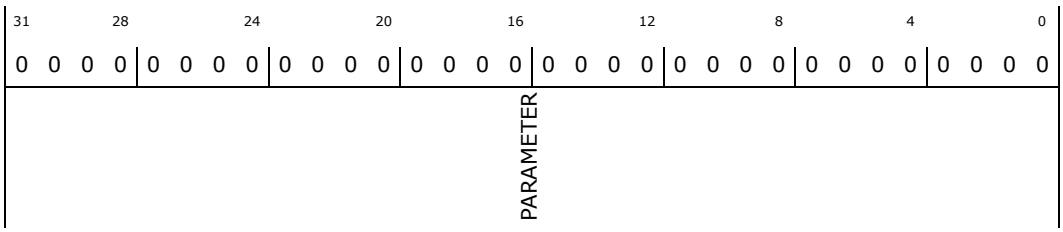
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_11: [BAR] + C8B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.181 DEPCMDPAR1_11—Offset C8B4h

TBD

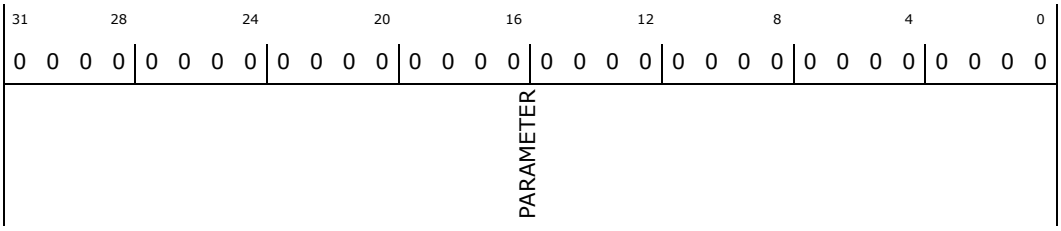
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_11: [BAR] + C8B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.182 DEPCMDPAR0_11—Offset C8B8h

TBD

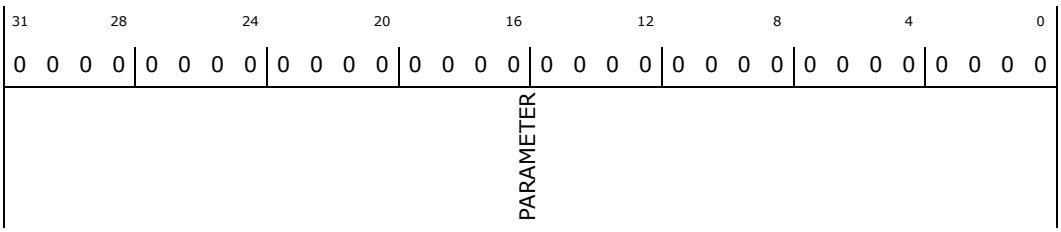
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_11: [BAR] + C8B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.183 DEPCMD_11—Offset C8BCh

TBD

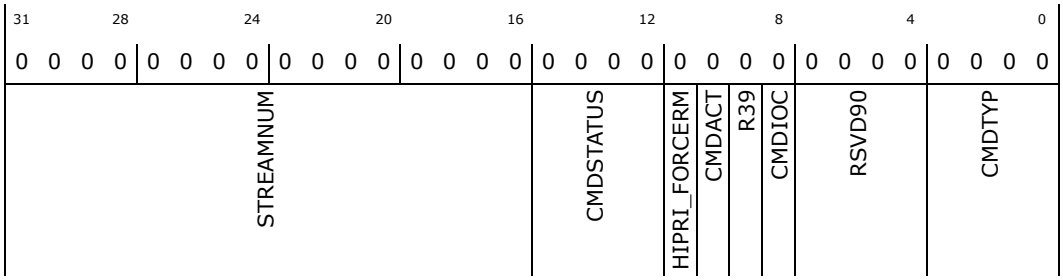
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_11: [BAR] + C8BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.184 DEPCMDPAR2_12—Offset C8C0h

TBD

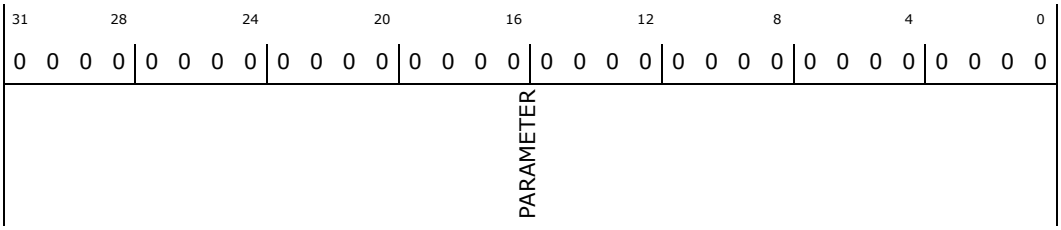
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_12: [BAR] + C8C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.185 DEPCMDPAR1_12—Offset C8C4h

TBD

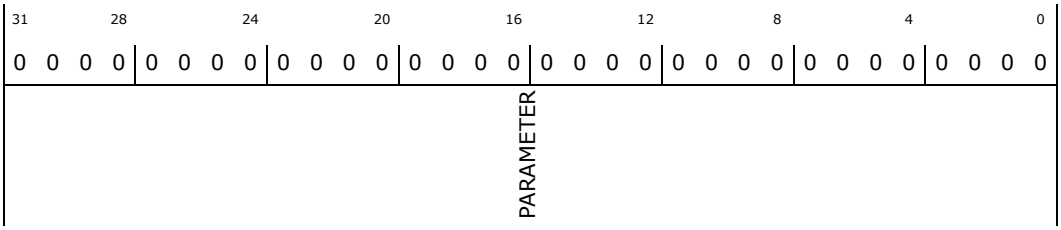
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_12: [BAR] + C8C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.186 DEPCMDPAR0_12—Offset C8C8h

TBD

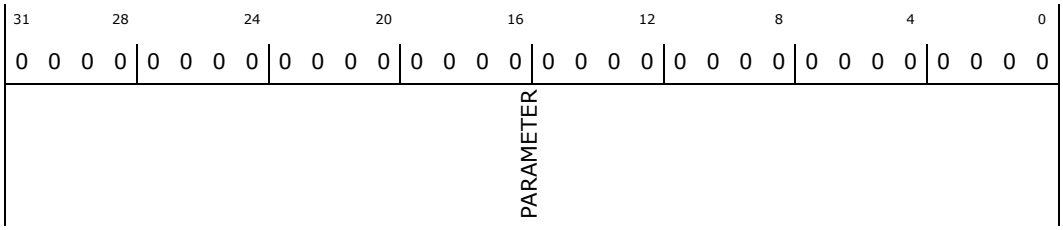
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_12: [BAR] + C8C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.187 DEPCMD_12—Offset C8CCh

TBD

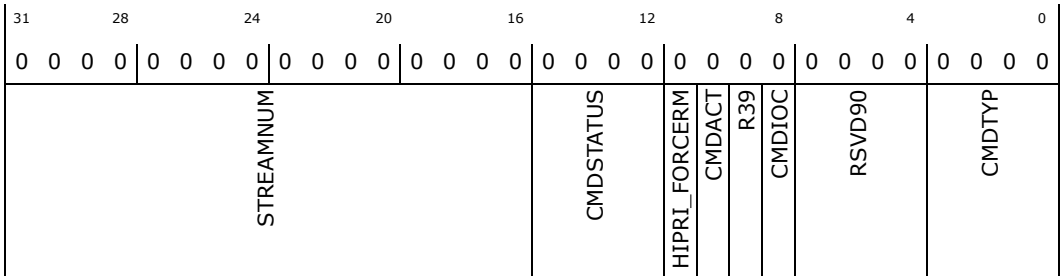
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_12: [BAR] + C8CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.188 DEPCMDPAR2_13—Offset C8D0h

TBD

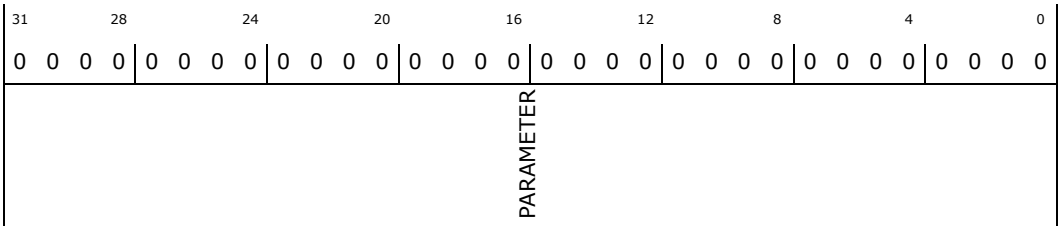
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_13: [BAR] + C8D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.189 DEPCMDPAR1_13—Offset C8D4h

TBD

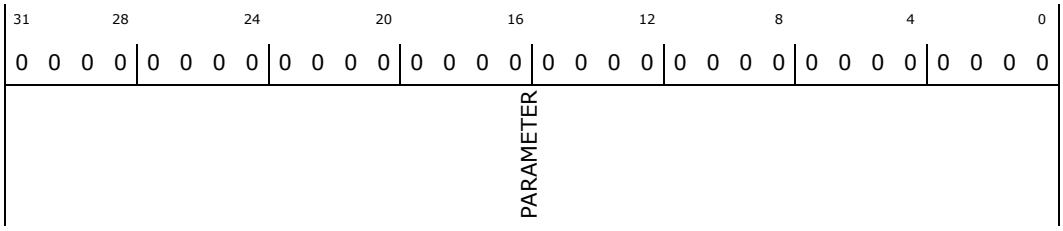
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_13: [BAR] + C8D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.190 DEPCMDPAR0_13—Offset C8D8h

TBD

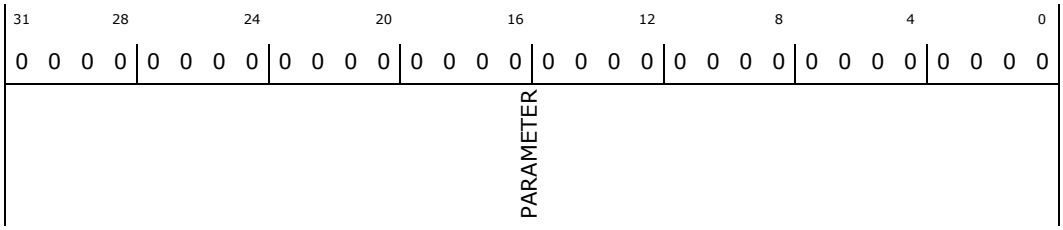
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_13: [BAR] + C8D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.191 DEPCMD_13—Offset C8DCh

TBD

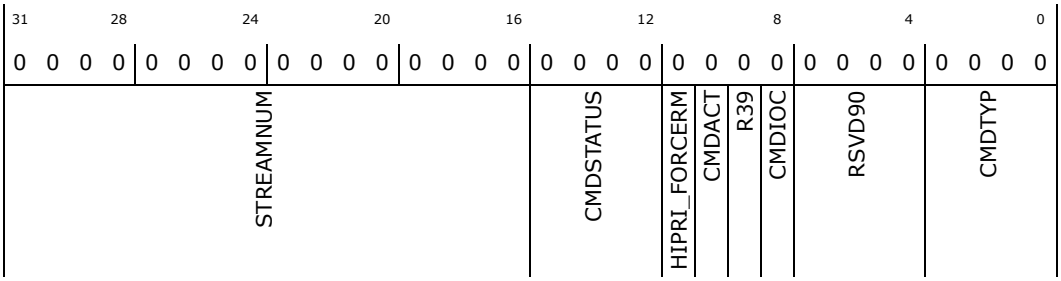
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_13: [BAR] + C8DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.192 DEPCMDPAR2_14—Offset C8E0h

TBD

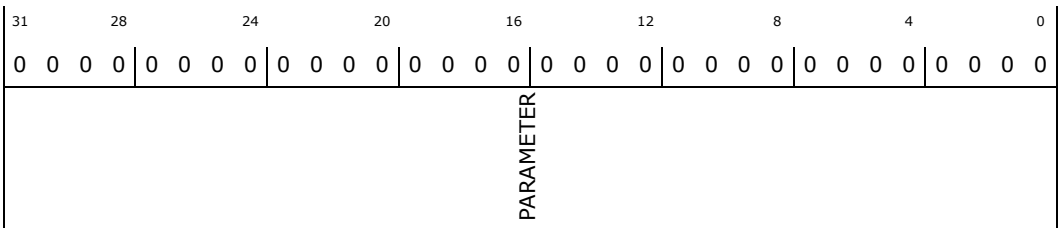
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_14: [BAR] + C8E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.193 DEPCMDPAR1_14—Offset C8E4h

TBD

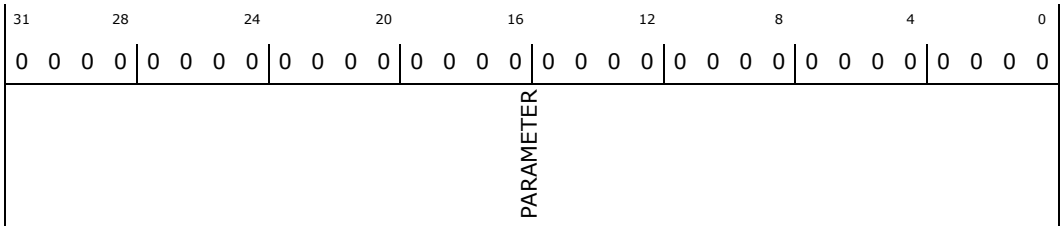
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_14: [BAR] + C8E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.194 DEPCMDPAR0_14—Offset C8E8h

TBD

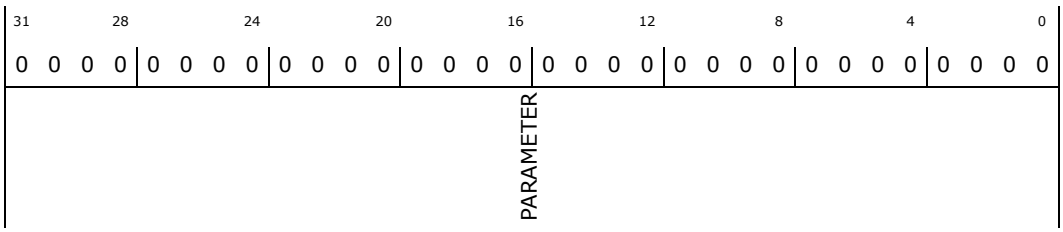
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_14: [BAR] + C8E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.195 DEPCMD_14—Offset C8ECh

TBD

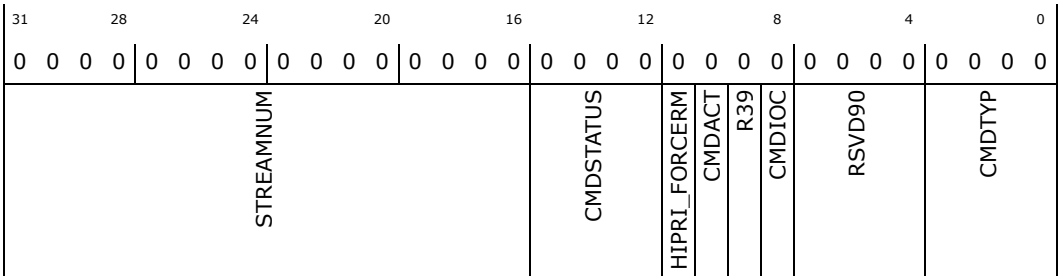
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_14: [BAR] + C8ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.196 DEPCMDPAR2_15—Offset C8F0h

TBD

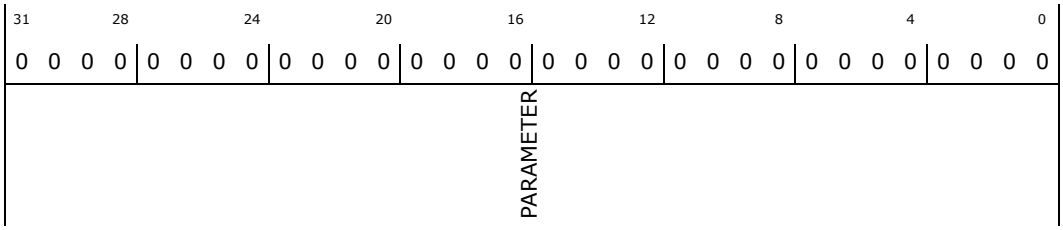
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_15: [BAR] + C8F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.197 DEPCMDPAR1_15—Offset C8F4h

TBD

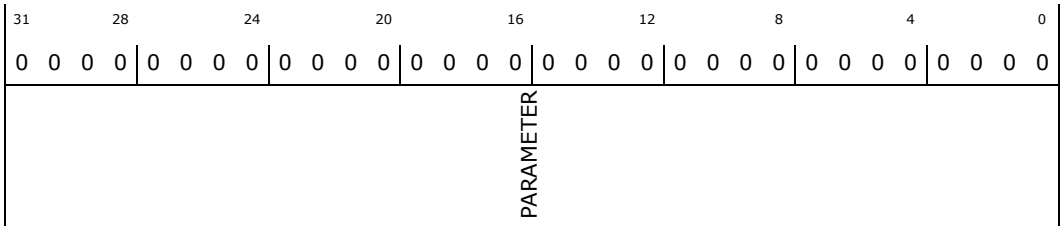
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_15: [BAR] + C8F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.198 DEPCMDPAR0_15—Offset C8F8h

TBD

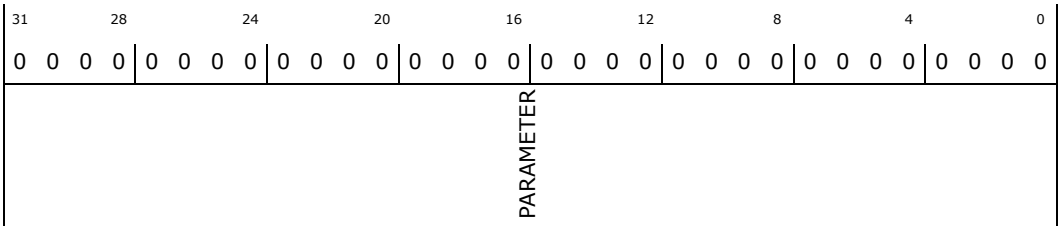
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_15: [BAR] + C8F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.199 DEPCMD_15—Offset C8FCh

TBD

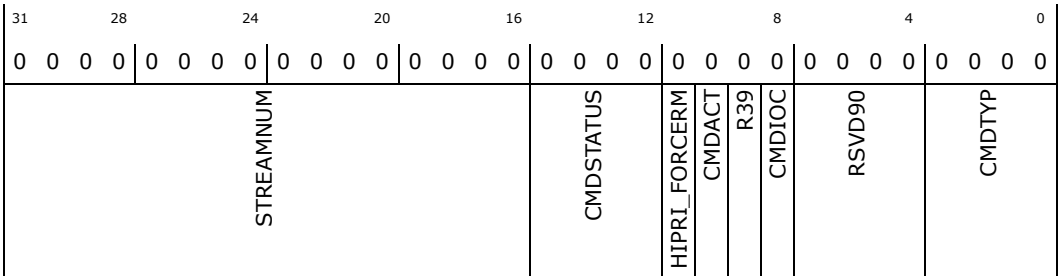
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_15: [BAR] + C8FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.200 DEPCMDPAR2_16—Offset C900h

TBD

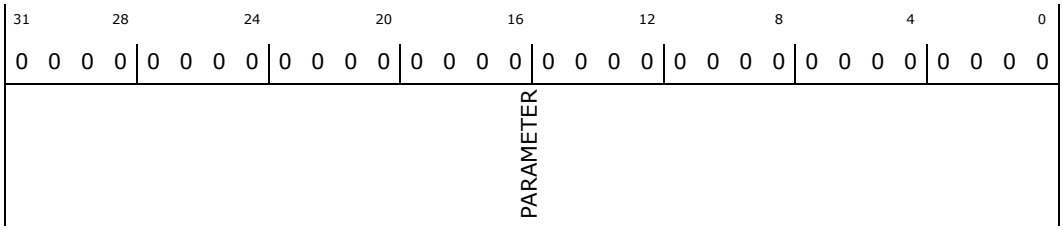
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_16: [BAR] + C900h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.201 DEPCMDPAR1_16—Offset C904h

TBD

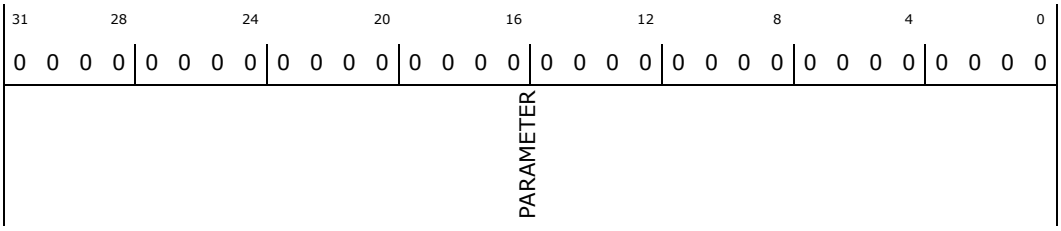
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_16: [BAR] + C904h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.202 DEPCMDPAR0_16—Offset C908h

TBD

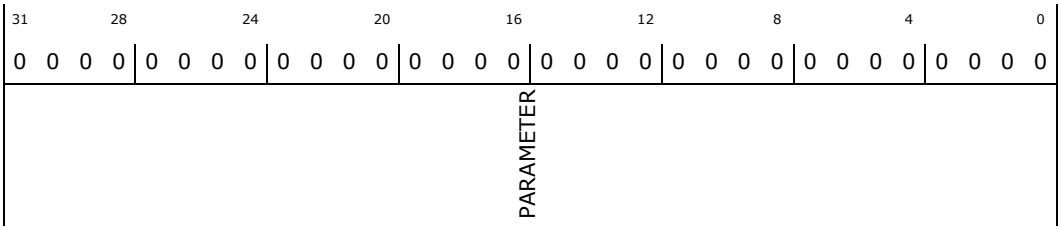
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_16: [BAR] + C908h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.203 DEPCMD_16—Offset C90Ch

TBD

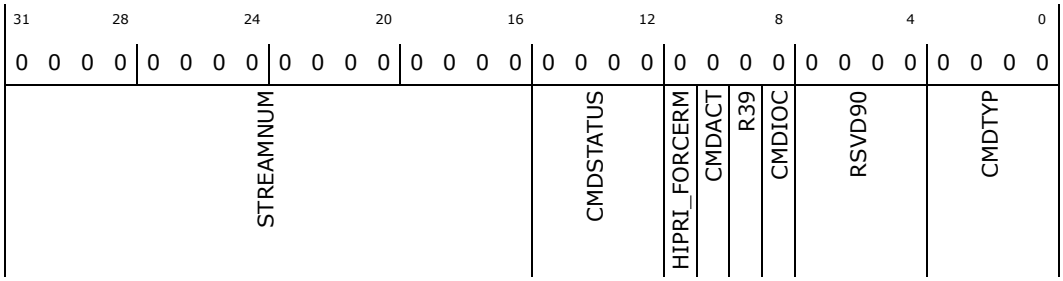
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_16: [BAR] + C90Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDACT
11	0h RW	**HIPRI_FORCERM:** Reg field CMDACT
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.204 DEPCMDPAR2_17—Offset C910h

TBD

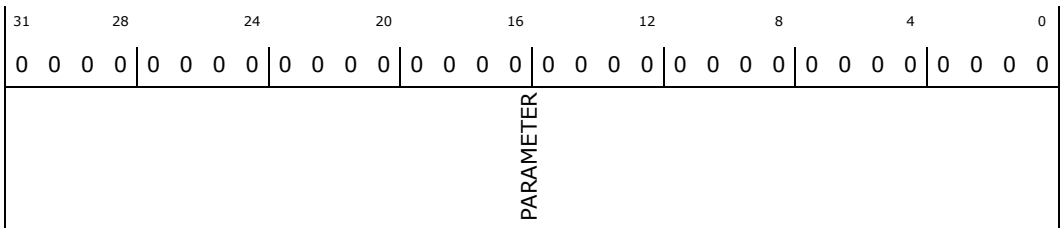
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_17: [BAR] + C910h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.205 DEPCMDPAR1_17—Offset C914h

TBD

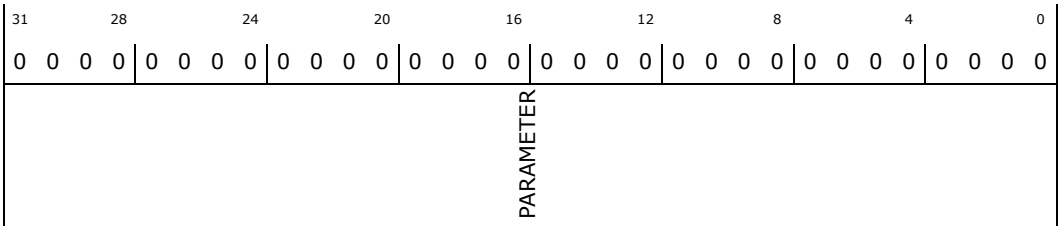
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_17: [BAR] + C914h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.206 DEPCMDPAR0_17—Offset C918h

TBD

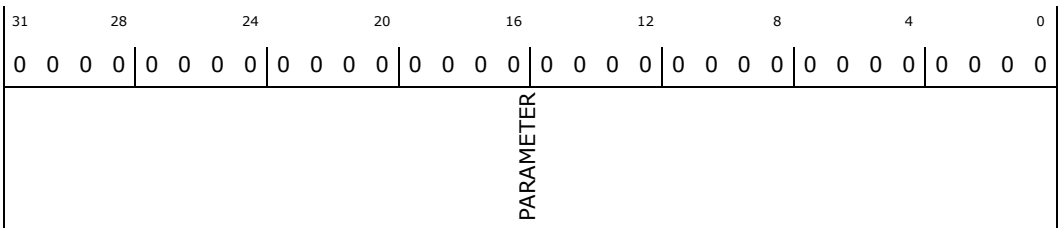
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_17: [BAR] + C918h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.207 DEPCMD_17—Offset C91Ch

TBD

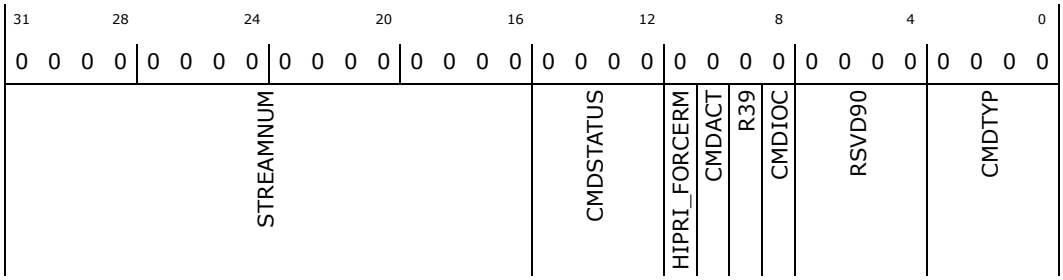
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_17: [BAR] + C91Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.208 DEPCMDPAR2_18—Offset C920h

TBD

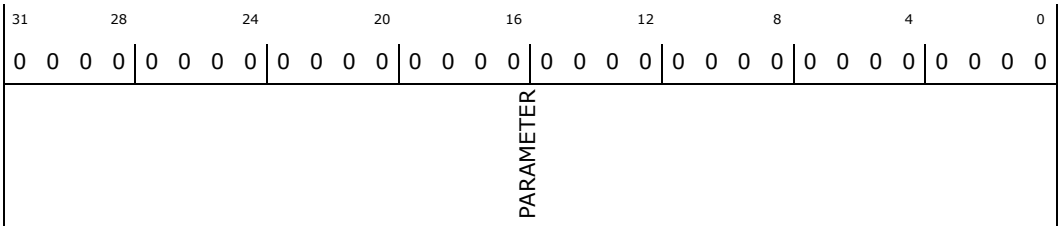
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_18: [BAR] + C920h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.209 DEPCMDPAR1_18—Offset C924h

TBD

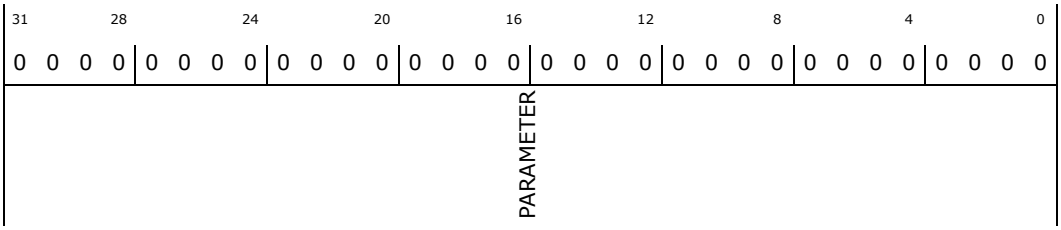
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_18: [BAR] + C924h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.210 DEPCMDPAR0_18—Offset C928h

TBD

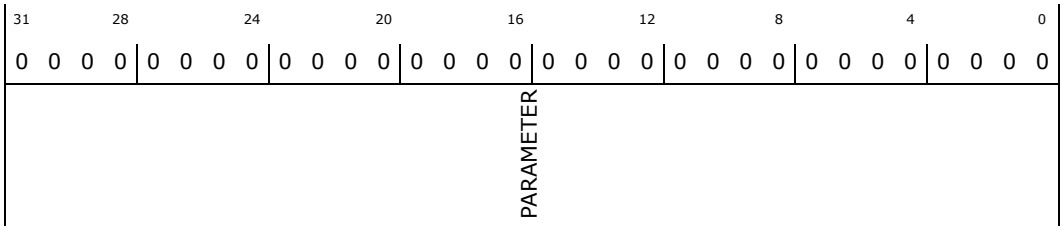
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_18: [BAR] + C928h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.211 DEPCMD_18—Offset C92Ch

TBD

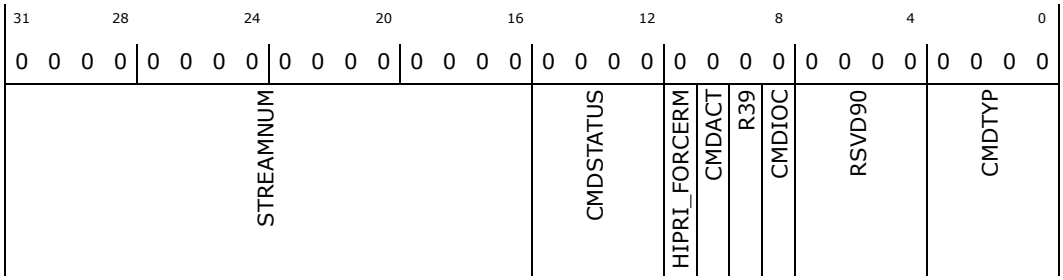
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_18: [BAR] + C92Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.212 DEPCMDPAR2_19—Offset C930h

TBD

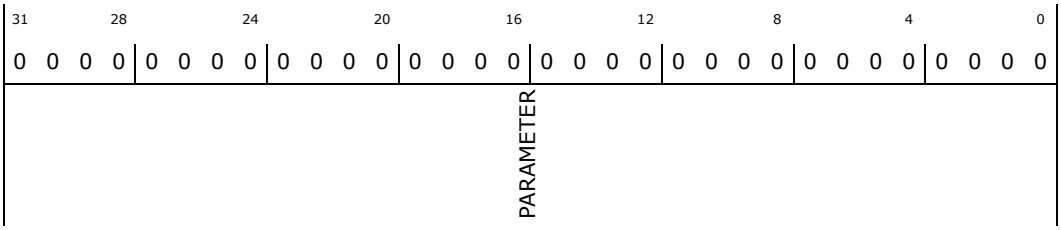
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_19: [BAR] + C930h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.213 DEPCMDPAR1_19—Offset C934h

TBD

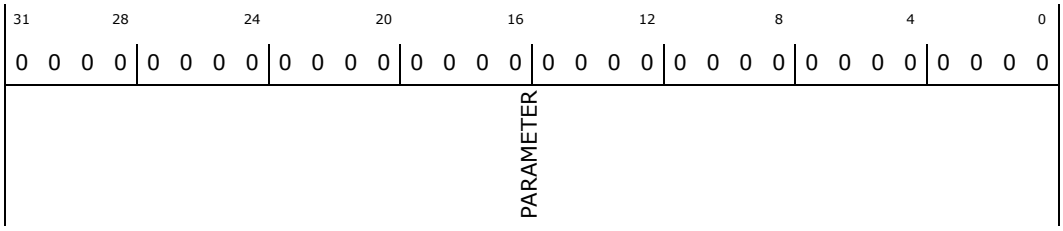
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_19: [BAR] + C934h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.214 DEPCMDPAR0_19—Offset C938h

TBD

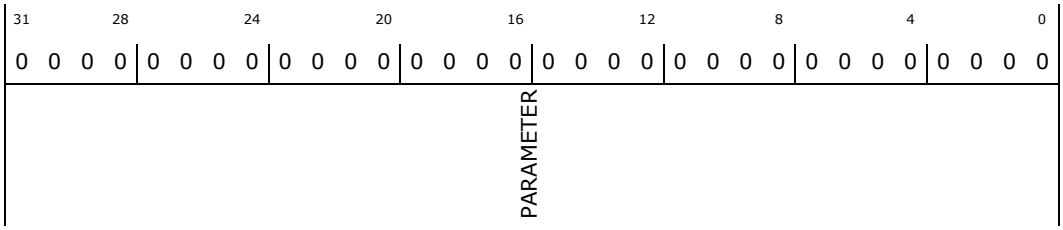
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_19: [BAR] + C938h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.215 DEPCMD_19—Offset C93Ch

TBD

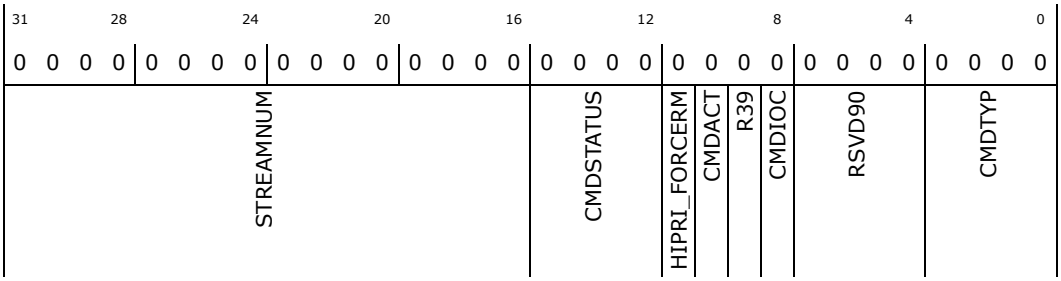
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_19: [BAR] + C93Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.216 DEPCMDPAR2_20—Offset C940h

TBD

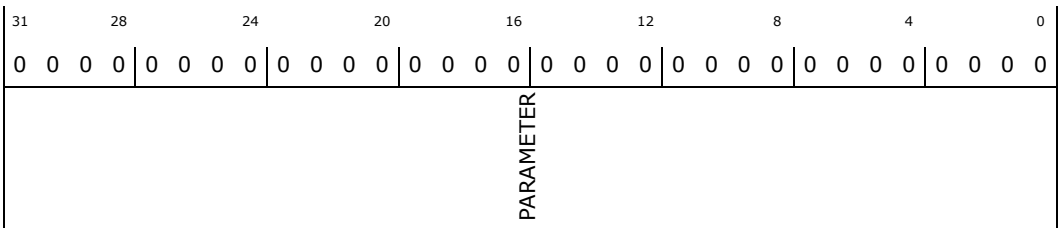
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_20: [BAR] + C940h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reserved.

3.74.217 DEPCMDPAR1_20—Offset C944h

TBD

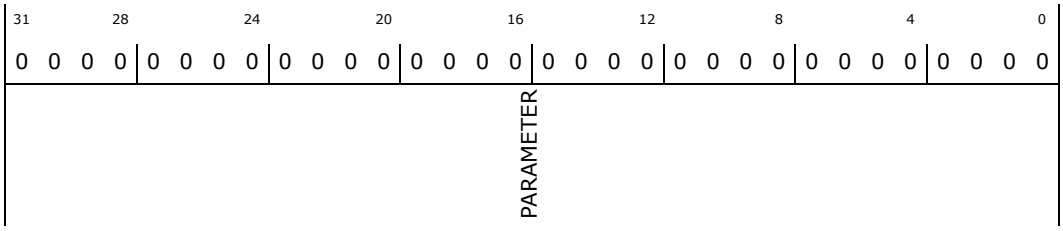
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_20: [BAR] + C944h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.218 DEPCMDPAR0_20—Offset C948h

TBD

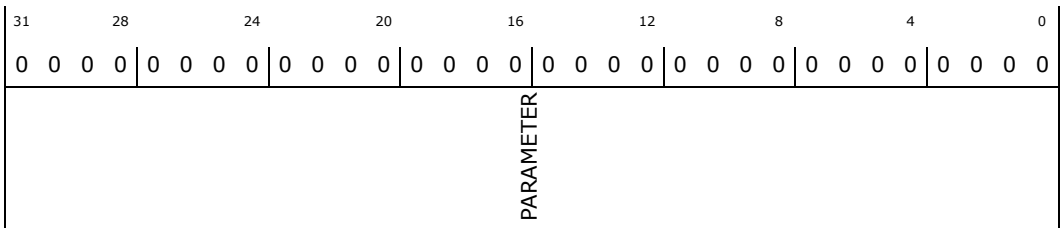
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_20: [BAR] + C948h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.219 DEPCMD_20—Offset C94Ch

TBD

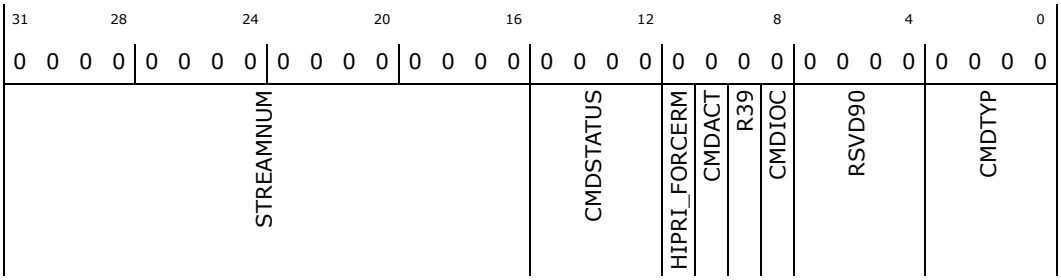
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_20: [BAR] + C94Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reserved.
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.220 DEPCMDPAR2_21—Offset C950h

TBD

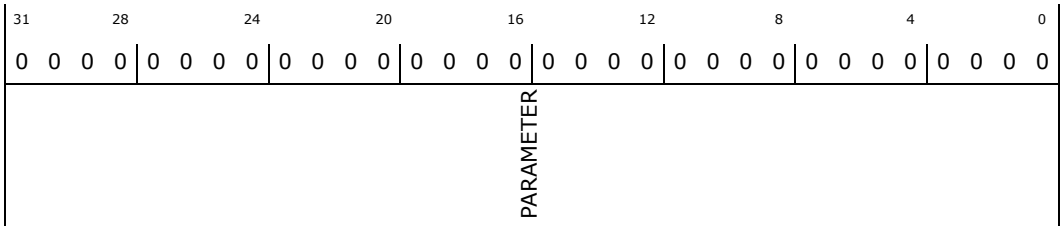
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_21: [BAR] + C950h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.221 DEPCMDPAR1_21—Offset C954h

TBD

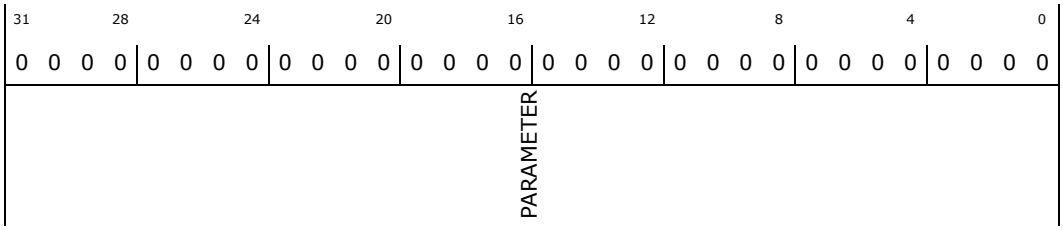
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_21: [BAR] + C954h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.222 DEPCMDPAR0_21—Offset C958h

TBD

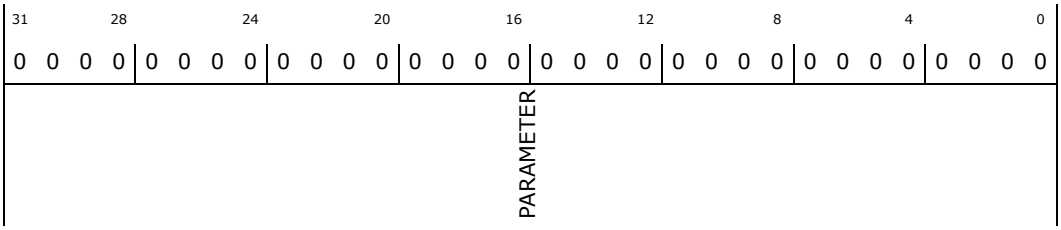
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_21: [BAR] + C958h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.223 DEPCMD_21—Offset C95Ch

TBD

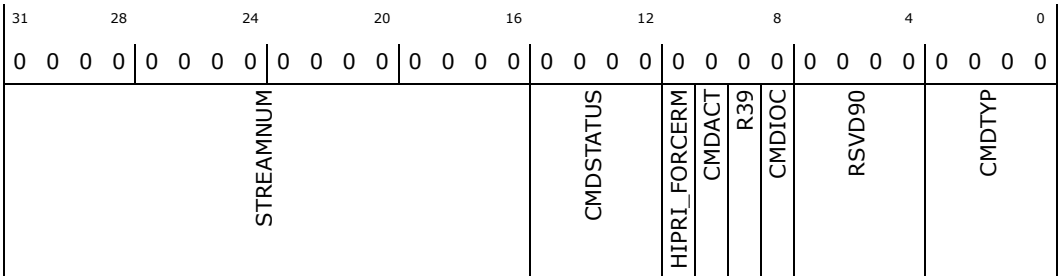
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_21: [BAR] + C95Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.224 DEPCMDPAR2_22—Offset C960h

TBD

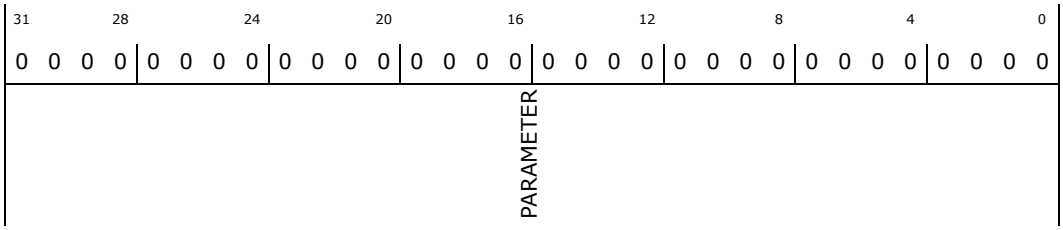
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_22: [BAR] + C960h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.225 DEPCMDPAR1_22—Offset C964h

TBD

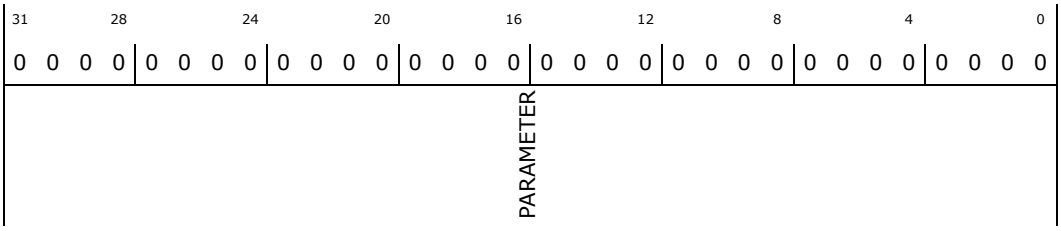
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_22: [BAR] + C964h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.226 DEPCMDPAR0_22—Offset C968h

TBD

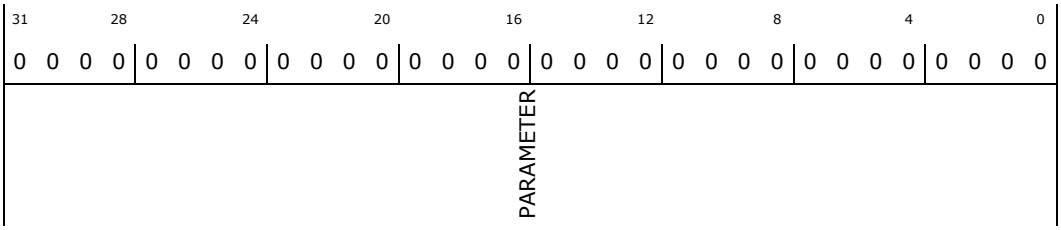
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_22: [BAR] + C968h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.227 DEPCMD_22—Offset C96Ch

TBD

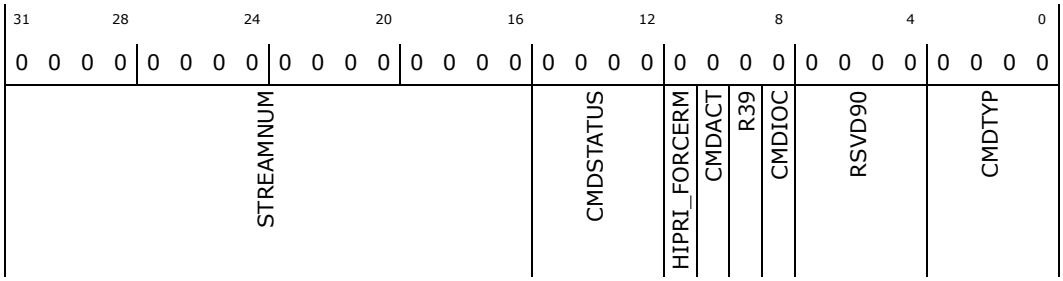
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_22: [BAR] + C96Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.228 DEPCMDPAR2_23—Offset C970h

TBD

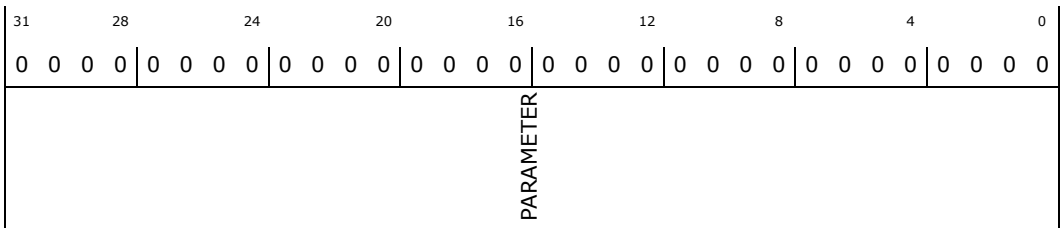
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_23: [BAR] + C970h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.229 DEPCMDPAR1_23—Offset C974h

TBD

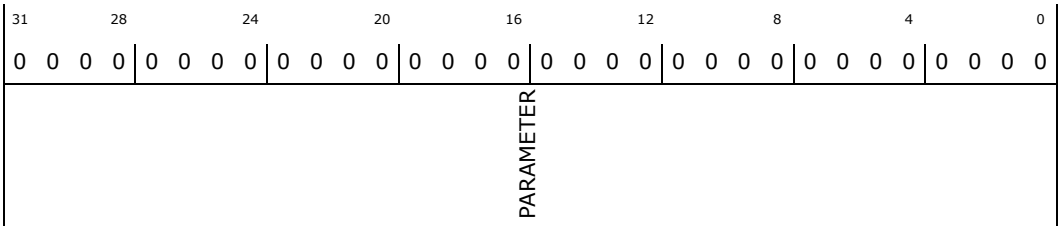
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_23: [BAR] + C974h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.230 DEPCMDPAR0_23—Offset C978h

TBD

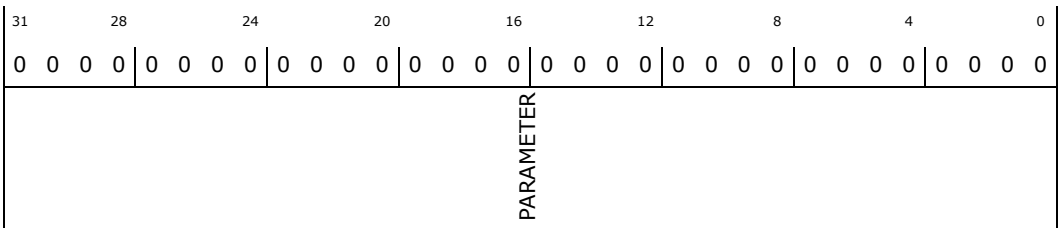
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_23: [BAR] + C978h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.231 DEPCMD_23—Offset C97Ch

TBD

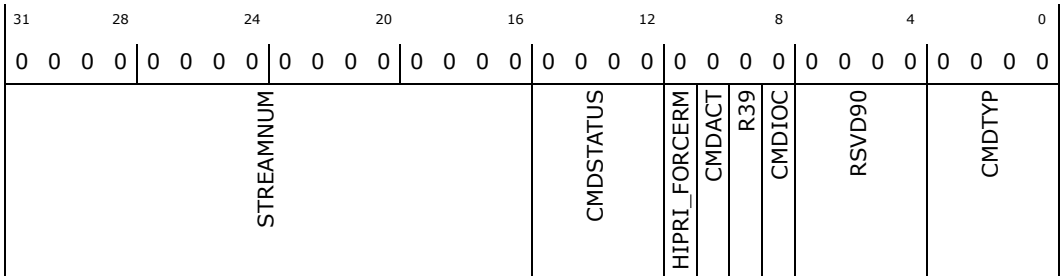
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_23: [BAR] + C97Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.232 DEPCMDPAR2_24—Offset C980h

TBD

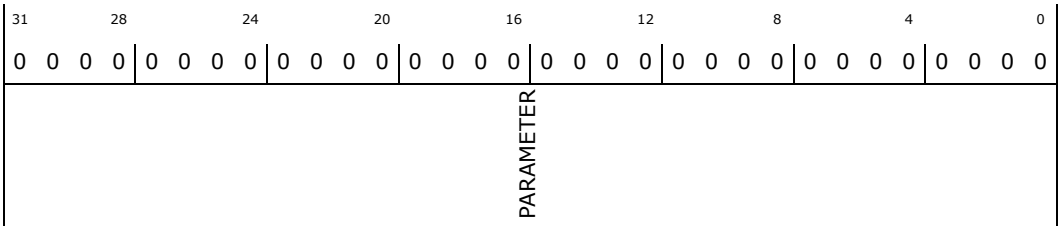
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_24: [BAR] + C980h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.233 DEPCMDPAR1_24—Offset C984h

TBD

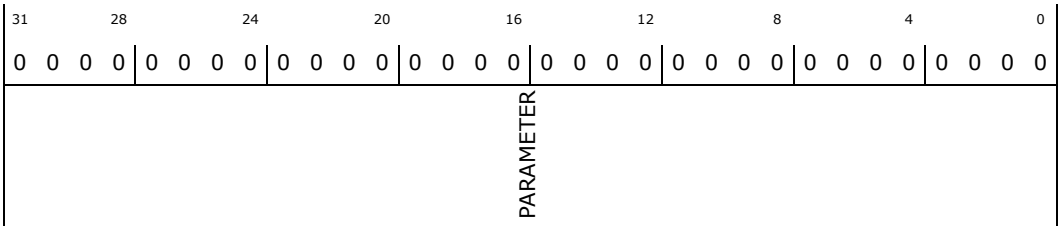
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_24: [BAR] + C984h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.234 DEPCMDPAR0_24—Offset C988h

TBD

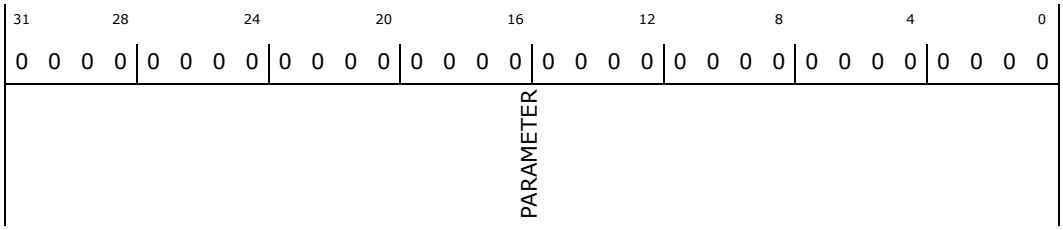
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_24: [BAR] + C988h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.235 DEPCMD_24—Offset C98Ch

TBD

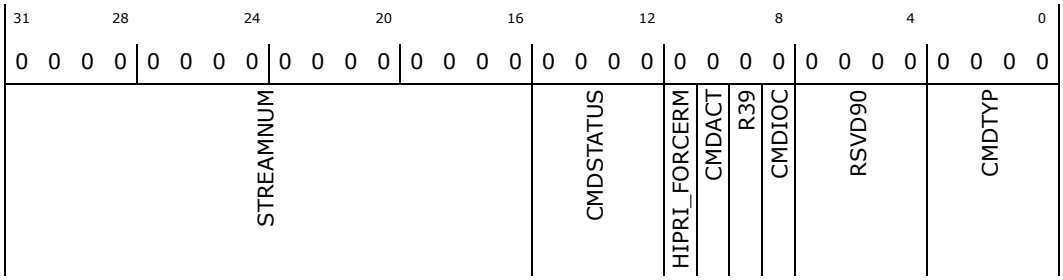
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_24: [BAR] + C98Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.236 DEPCMDPAR2_25—Offset C990h

TBD

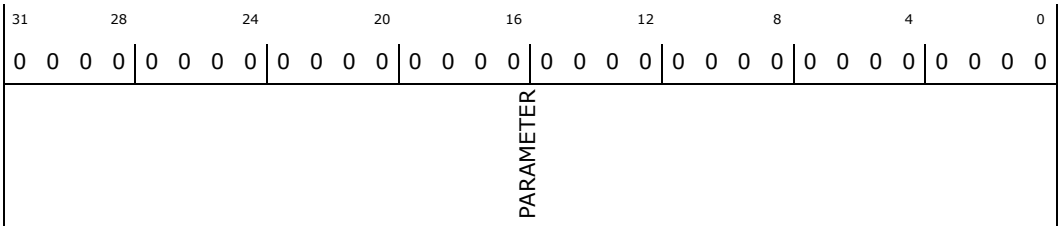
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_25: [BAR] + C990h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.237 DEPCMDPAR1_25—Offset C994h

TBD

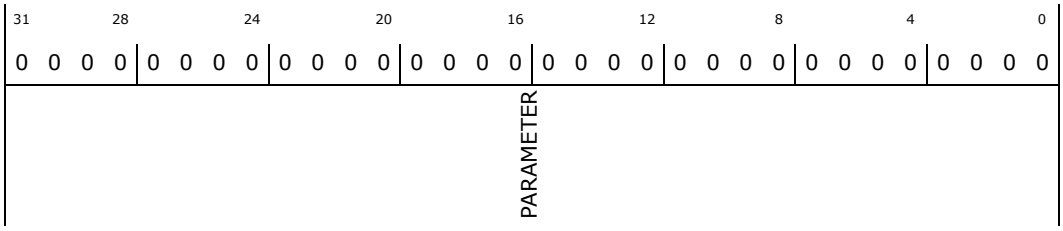
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_25: [BAR] + C994h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.238 DEPCMDPAR0_25—Offset C998h

TBD

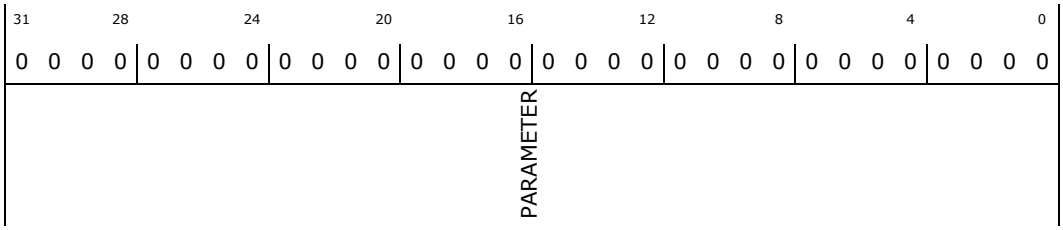
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_25: [BAR] + C998h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.239 DEPCMD_25—Offset C99Ch

TBD

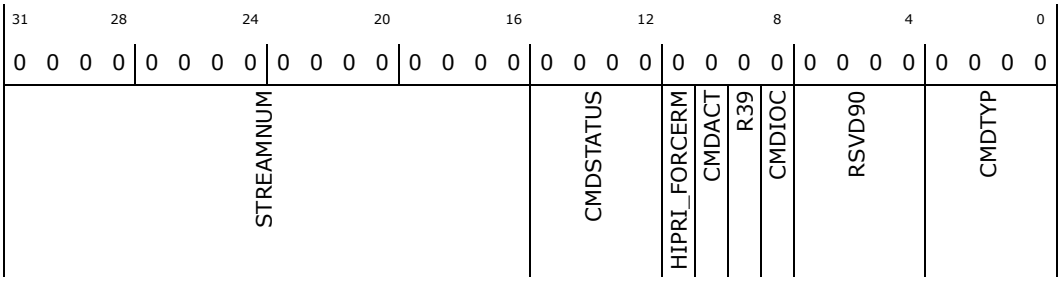
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_25: [BAR] + C99Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.240 DEPCMDPAR2_26—Offset C9A0h

TBD

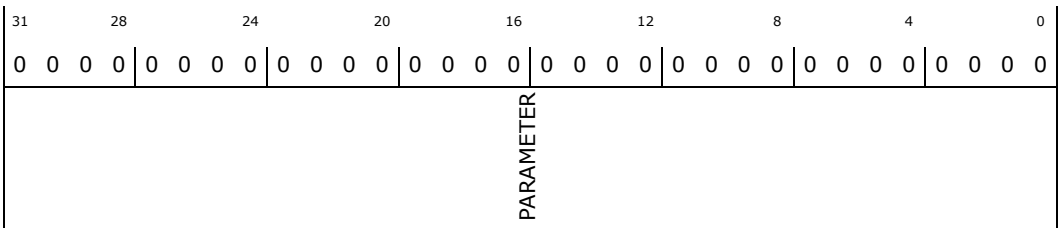
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_26: [BAR] + C9A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.241 DEPCMDPAR1_26—Offset C9A4h

TBD

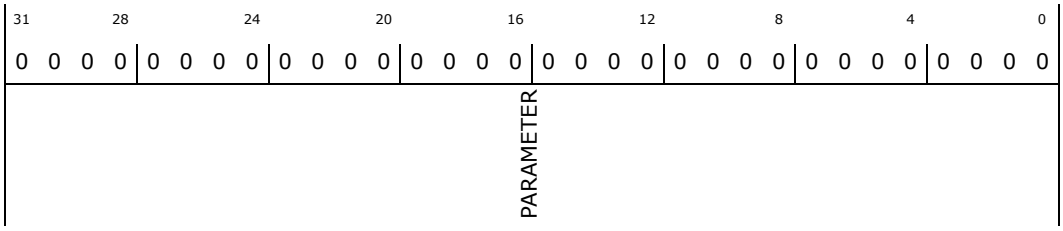
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_26: [BAR] + C9A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.242 DEPCMDPAR0_26—Offset C9A8h

TBD

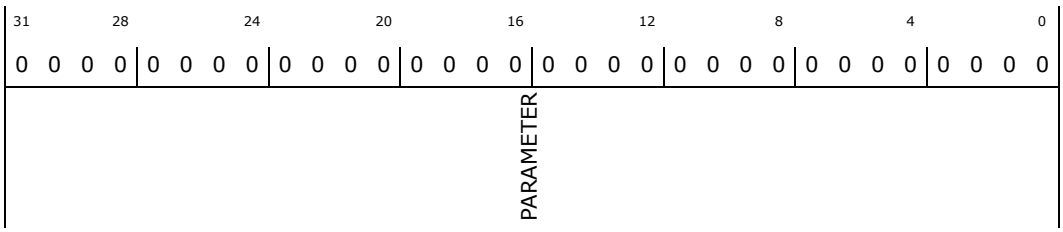
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_26: [BAR] + C9A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.243 DEPCMD_26—Offset C9ACh

TBD

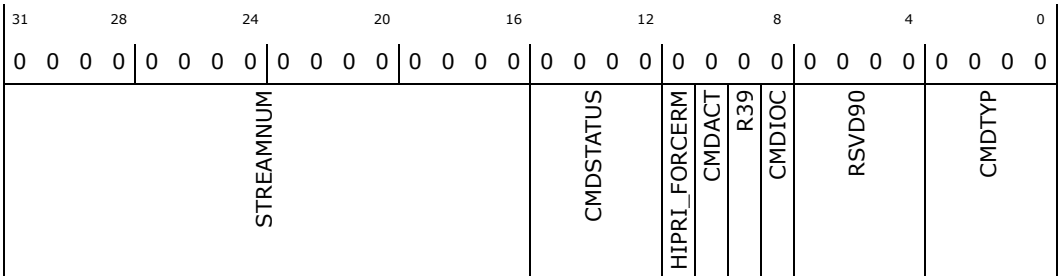
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_26: [BAR] + C9ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.244 DEPCMDPAR2_27—Offset C9B0h

TBD

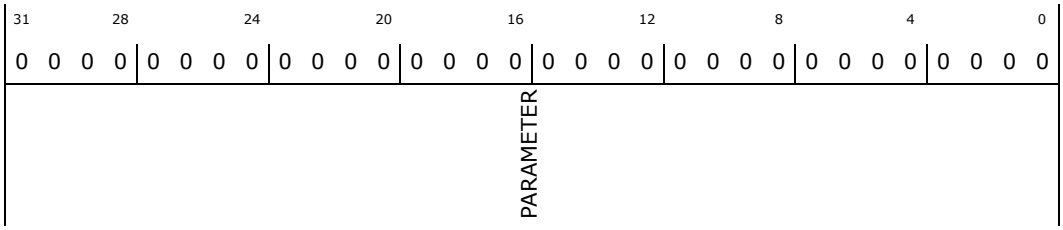
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_27: [BAR] + C9B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.245 DEPCMDPAR1_27—Offset C9B4h

TBD

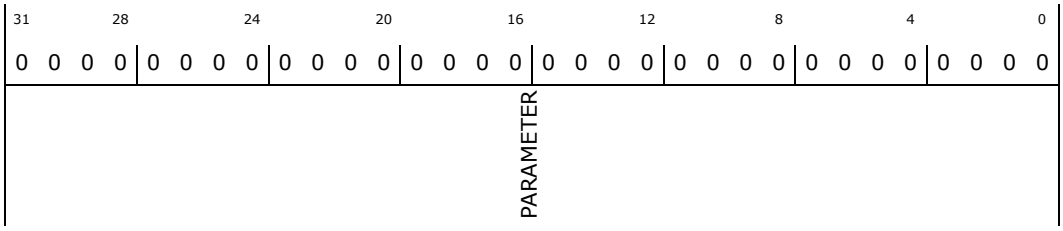
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_27: [BAR] + C9B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.246 DEPCMDPAR0_27—Offset C9B8h

TBD

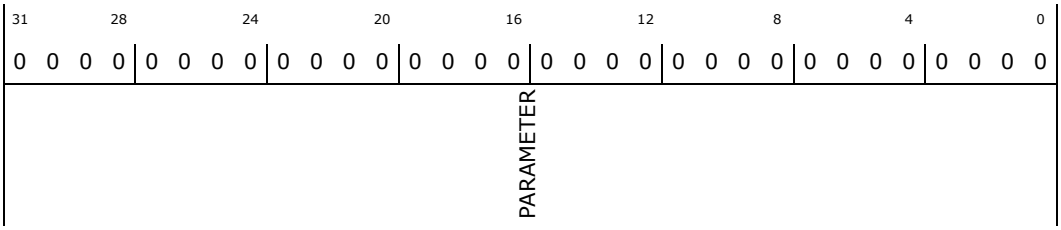
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_27: [BAR] + C9B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.247 DEPCMD_27—Offset C9BCh

TBD

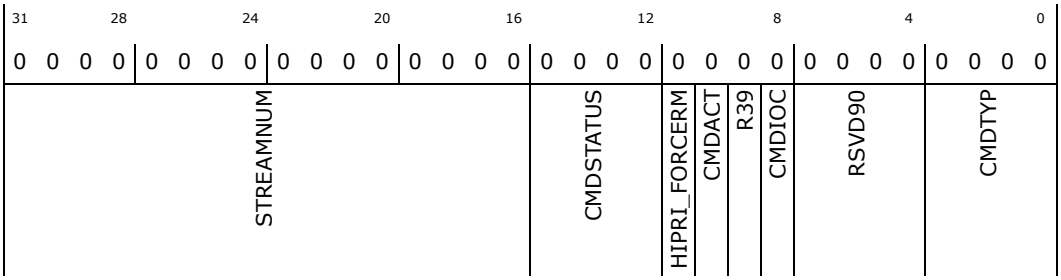
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_27: [BAR] + C9BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.248 DEPCMDPAR2_28—Offset C9C0h

TBD

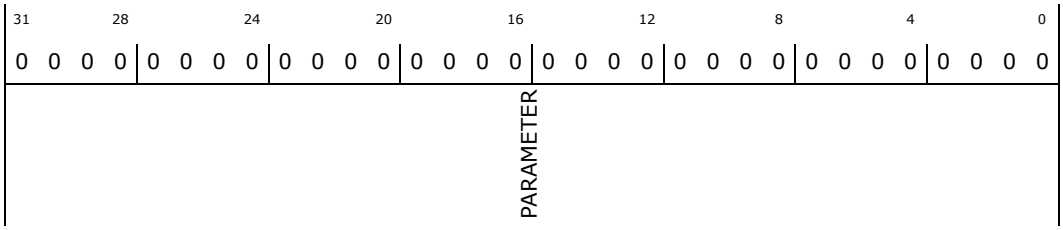
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_28: [BAR] + C9C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.249 DEPCMDPAR1_28—Offset C9C4h

TBD

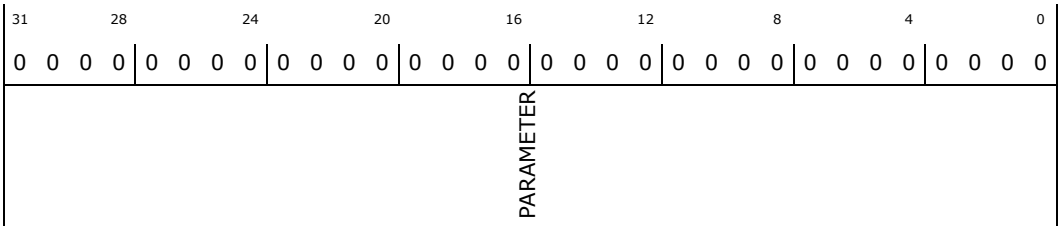
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_28: [BAR] + C9C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.250 DEPCMDPAR0_28—Offset C9C8h

TBD

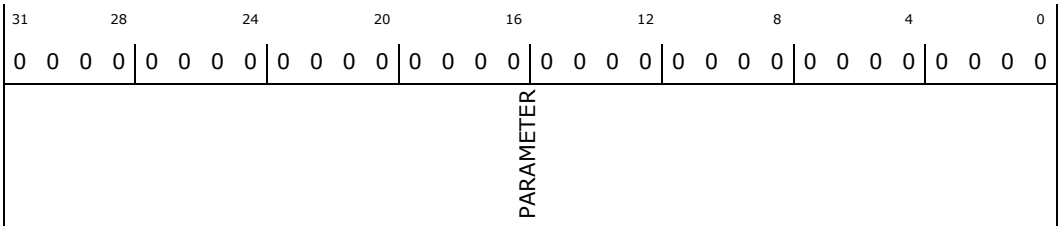
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_28: [BAR] + C9C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.251 DEPCMD_28—Offset C9CCh

TBD

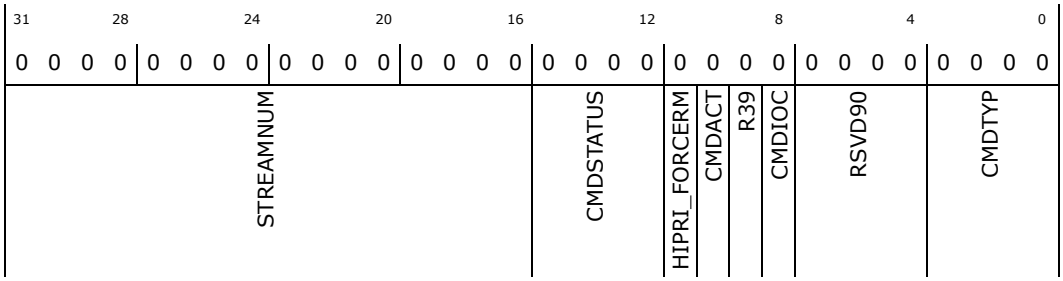
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_28: [BAR] + C9CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reserved.
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.252 DEPCMDPAR2_29—Offset C9D0h

TBD

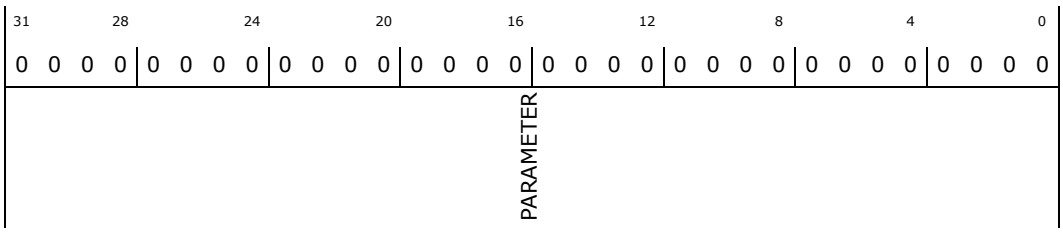
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_29: [BAR] + C9D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.253 DEPCMDPAR1_29—Offset C9D4h

TBD

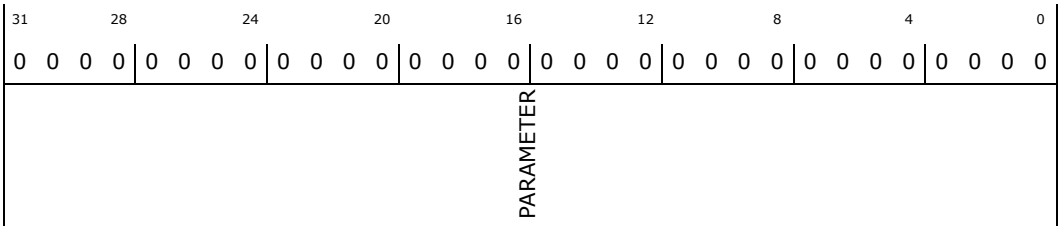
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_29: [BAR] + C9D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.254 DEPCMDPAR0_29—Offset C9D8h

TBD

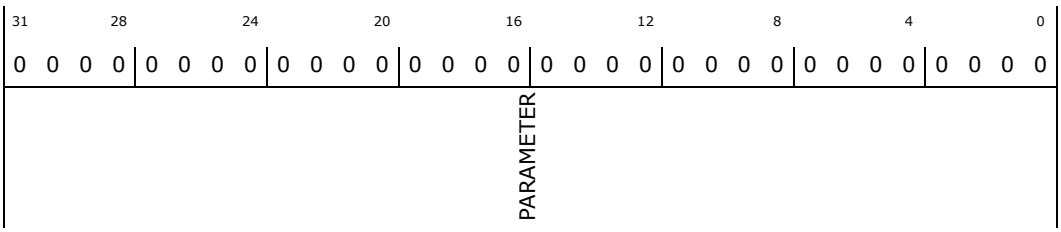
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_29: [BAR] + C9D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.255 DEPCMD_29—Offset C9DCh

TBD

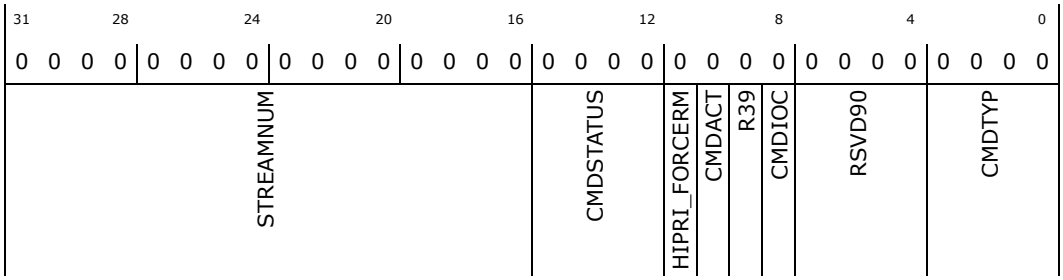
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_29: [BAR] + C9DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.256 DEPCMDPAR2_30—Offset C9E0h

TBD

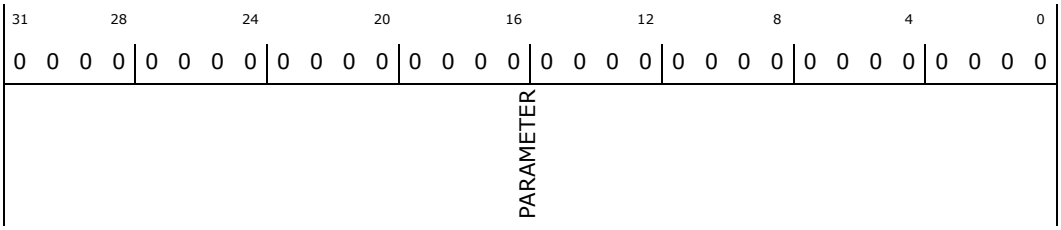
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_30: [BAR] + C9E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.257 DEPCMDPAR1_30—Offset C9E4h

TBD

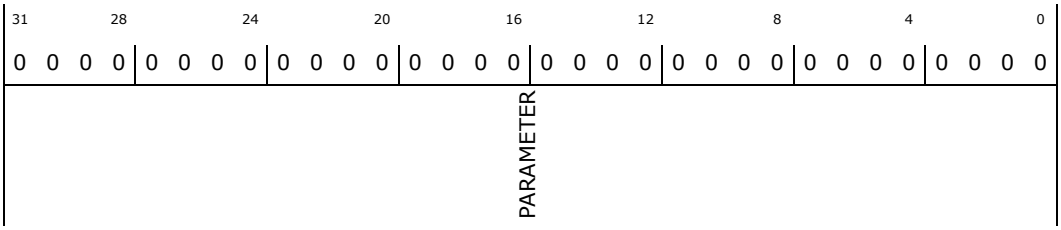
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_30: [BAR] + C9E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.258 DEPCMDPAR0_30—Offset C9E8h

TBD

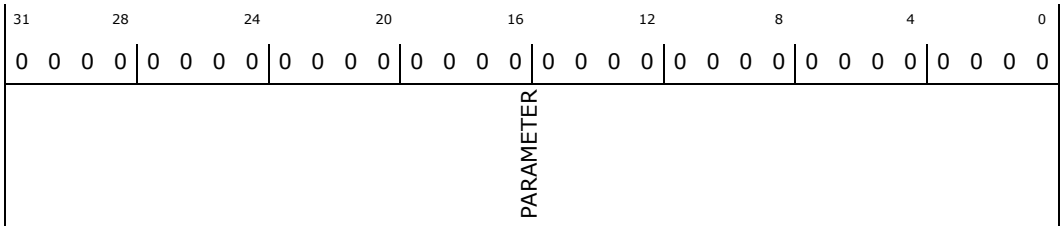
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_30: [BAR] + C9E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.259 DEPCMD_30—Offset C9ECh

TBD

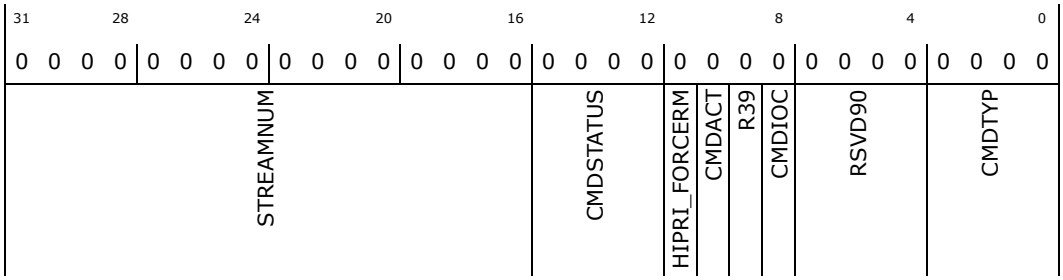
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_30: [BAR] + C9ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT

Bit Range	Default & Access	Description
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.260 DEPCMDPAR2_31—Offset C9F0h

TBD

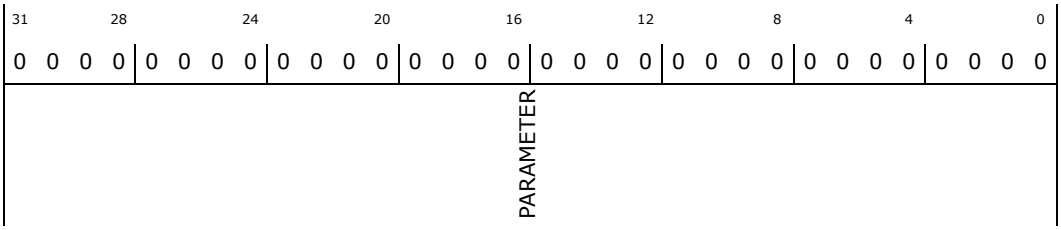
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_31: [BAR] + C9F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.261 DEPCMDPAR1_31—Offset C9F4h

TBD

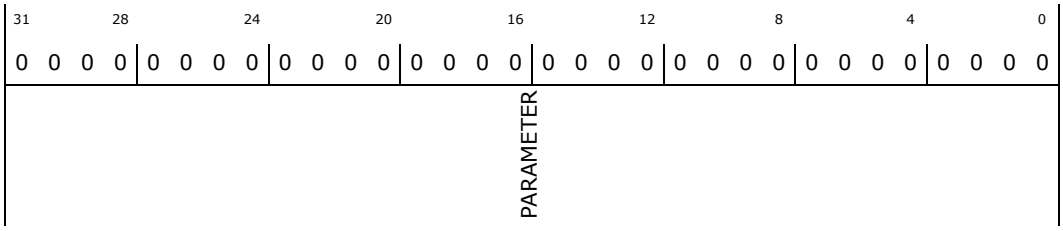
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_31: [BAR] + C9F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.262 DEPCMDPAR0_31—Offset C9F8h

TBD

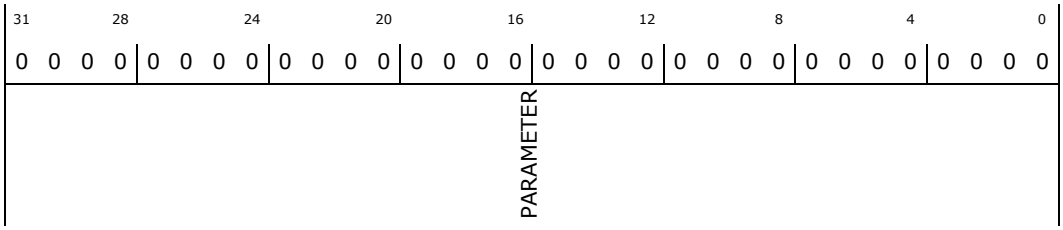
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_31: [BAR] + C9F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

3.74.263 DEPCMD_31—Offset C9FCh

TBD

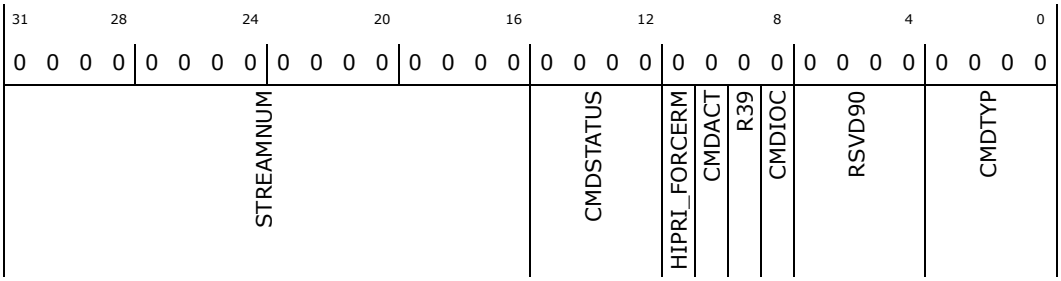
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_31: [BAR] + C9FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:** TBD
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

3.74.264 OCFG—Offset CC00h

OTG Configuration Register

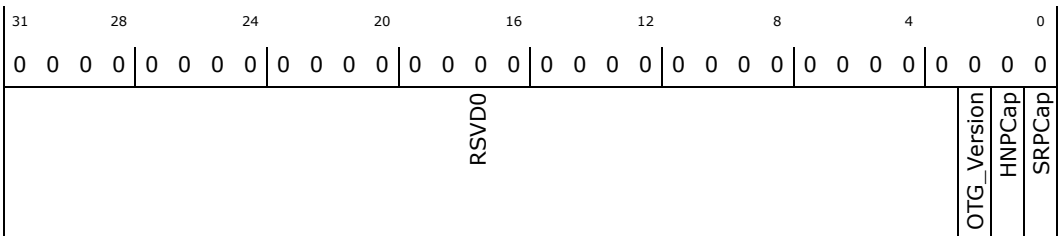
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OCFG: [BAR] + CC00h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0h RO	**RSVD0:** reserved
2	0h RW	**OTG_Version:** TBD
1	0h RW	**HNPCap:** RSP/HNP Capability: The terminology RSP is used when the core is operating in SS mode, and HNP is used when the core is operating in non-SS mode. The application uses this bit to control the DWC_usb3 core's RSP/HNP capabilities. n 1'b0: RSP/HNP capability is not enabled. n 1'b1: RSP/HNP capability is enabled. Note: This bit is writable only if RSP/HNP mode is specified for Mode of Operation in coreConsultant, that is when DWC_USB3_EN_OTG != 0 and DWC_USB3_MODE = DRD. If RSP/HNP mode is not specified, this bit is Read Only, and is set to 1'b0.
0	0h RW	**SRPCap:** SRP Capability: The application uses this bit to control the DWC_usb3 core's SRP capabilities. n 1'b0: SRP capability is not enabled. n 1'b1: SRP capability is enabled. If this bit is not set for B-device, it cannot request the connected A-device (host) to activate Vbus and start a session. If this bit is not set for A-device, it cannot detect the SRP from B-device (device) to activate Vbus and start a session. Note: This bit is writable only if OTG is enabled in coreConsultant (DWC_USB3_EN_OTG !=0). If OTG is not enabled, then this bit is Read Only and is set to 1'b0.

3.74.265 OCTL—Offset CC04h

OTG Control Register

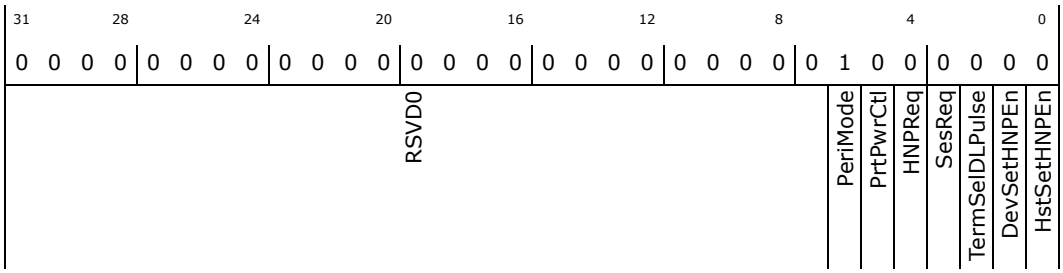
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OCTL: [BAR] + CC04h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000040h



Bit Range	Default & Access	Description
31:7	0h RO	**RSVD0:** reserved
6	1h RW	**PeriMode:** Peripheral Mode: Application uses this bit to program the core to work as a peripheral or as a host. n 1'b0: The OTG device acts as a host n 1'b1: The OTG device acts as a peripheral

Bit Range	Default & Access	Description
5	0h RW	**PrtPwrCtl:** Port Power Control: Application sets this bit to initiate Vbus drive when it is an A-device. The application should clear this bit only if it wants to switch off the Vbus to B-device. The core clears this bit in the following conditions: n Transition from any state to A-IDLE state defined in OTG2.0 state machine. n When AIDL_BDIS_TOUT occurs in A_SUSPEND n When A_WAIT_BCON_TOUT occurs in A_WAIT_BCON n Transition to any B- state defined in OTG2.0 state machine
4	0h RW	**HNPReq:** HNP Request: n 1'b0: No HNP request n 1'b1: HNP request The application sets this bit to initiate a HNP request to the connected USB host. The application clears this bit by writing a 1'b0 when either of the following is detected: n OEVT.OTGBDevBHostEndEvnt n OEVT.OTGBDevVBusChngEvnt
3	0h RW	**SesReq:** Session Request: n 1'b0: No session request n 1'b1: Session request The application sets this bit to initiate a session request on the USB. Writing 1'b1 to this field will trigger the core to send SRP (data line pulsing) on PHY interface. In the absence of OEVT.OTGBDevSessVldDetEvnt after a session request, the application must wait for at least TB_SRP_FAIL time (6 secs) before initiating another session request. This field returns 1'b0 when read.
2	0h RW	**TermSelDLPulse:** TermSel DLine Pulsing Selection: This bit selects utmi_termselect to drive data line pulse during SRP. n 1'b0: Data line pulsing using utmi_txvalid (default). n 1'b1: Data line pulsing using utmi_termsel.
1	0h RW	**DevSetHNPEn:** Device Set RSP/HNP Enable: n 1'b0: RSP/HNP is not enabled in the application n 1'b1: RSP/HNP is enabled in the application The application sets this bit in the following scenario: n In HS/FS mode, when it successfully receives a SetFeature.SetHNPEnable command from the connected USB host. n In SS mode, when it has sent a b3_ntf_hst_rel to the A-device, or the A-device has sent an a3_ntf_host_req. Note: The terminology RSP is used when the core is operating in SS mode, and HNP is used when the core is operating in non-SS mode.
0	0h RW	**HstSetHNPEn:** Host Set RSP/HNP Enable: n 1'b0: Host Set RSP/HNP is not enabled n 1'b1: Host Set RSP/HNP is enabled The application sets this bit in the following scenario: n In HS/FS mode, when it has successfully enabled HNP (using the SetFeature.SetHNPEnable command) from the connected device. n In SS mode, when it has successfully enabled b3_rsp_enable feature in RSP-capable Device using SetFeature command while operating as an A-Host, or when it has received a b3_ntf_hst_rel through SetFeature command while operating as A-peripheral. Note: The terminology RSP is used when the core is operating in SS mode, and HNP is used when the core is operating in non-SS mode.

3.74.266 OEVT—Offset CC08h

Value After Reset: 0x0 OTG Events Register

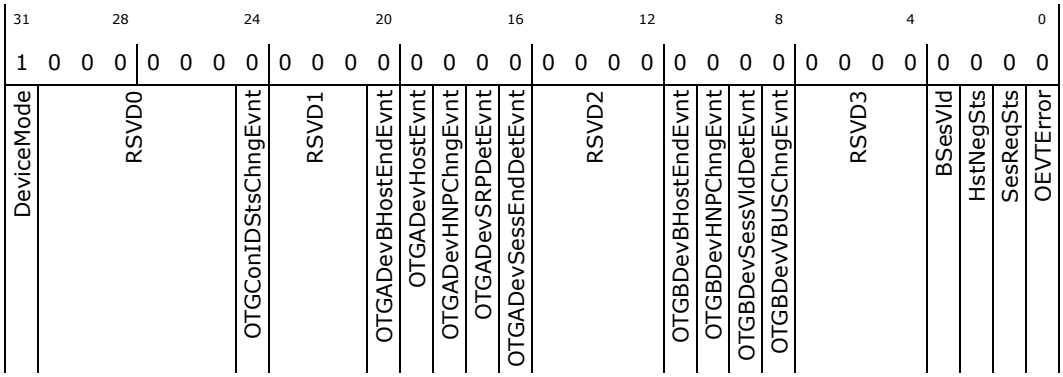
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

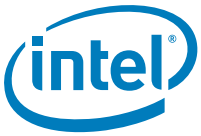
OEVT: [BAR] + CC08h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 80000000h



Bit Range	Default & Access	Description
31	1h RO	**DeviceMode:** Device Mode: Indicates whether the device is in A-device or B-device mode based on utmiotg_iddig n 1'b0: A-Device mode n1'b1: B-Device mode The rest of the OTG Event Information bits (OTGxxxxEvtInfo) in OEVT register will be based on the contents of this field.
30:25	0h RO	**RSVD0:** reserved
24	0h RO	**OTGConIDStsChngEvnt:** Write Behavior: oneToClear Connector ID Status Change Event: Set in both A-Dev/B-Dev Mode. This event is generated when there is a change in connector ID status.
23:21	0h RO	**RSVD1:** reserved
20	0h RO	**OTGADevBHostEndEvnt:** Write Behavior: oneToClear A-device B-Host End Event: Set in A-device Mode Only. The event is generated when B-device has completed its host role. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
19	0h RO	**OTGADevHostEvnt:** Write Behavior: oneToClear A-device host event: Set in A-device Mode Only. This event is generated when A-device enters host role. In HS/FS mode, it occurs after the initial connect to a B-device as A-host as well as when there is a role change from A-peripheral to A-host. Note: This bit is applicable only for OTG 2.0 mode of operation.
18	0h RO	**OTGADevHNPChngEvnt:** Write Behavior: oneToClear A-Dev HNP Change Event: Set in A-device Mode Only. The event is generated when there is an HNP attempt. Note: This bit is applicable only for OTG 2.0 mode of operation.
17	0h RO	**OTGADevSRPDetEvnt:** Write Behavior: oneToClear SRP Detect Event: Set in A-device Mode Only. This event is asserted when a session request from the B-device is detected via SRP. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
16	0h RO	**OTGADevSessEndDetEvnt:** Write Behavior: oneToClear Session End Detected Event: Set in A-device Mode Only. This event is asserted when the utmisrp_avalid signal goes low indicating the end of a session. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation
15:12	0h RO	**RSVD2:** Reserved



Bit Range	Default & Access	Description
11	0h RO	**OTGBDevBHostEndEvnt:** Write Behavior: oneToClear B-Device B-Host End Event: Set in B-device Mode Only. This event is generated when B-device has completed its host role. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
10	0h RO	**OTGBDevHNPChngEvnt:** Write Behavior: oneToClear B-Dev HNP Change Event: Set in B-Device Mode only. This event is generated when there is a Success or Failure of an HNP attempt. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
9	0h RO	**OTGBDevSessVldDetEvnt:** Write Behavior: oneToClear Session Valid Detected Event: Set in B-device Mode Only. This event is asserted when there is a valid Vbus from A-device and B-device succeeds in starting a session. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
8	0h RO	**OTGBDevVBUSChngEvnt:** Write Behavior: oneToClear Vbus Change Event: Set in B-device Mode Only. This event is asserted when the utmisrp_bvalid signal goes low (indicating the end of a session), or goes high. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
7:4	0h RO	**RSVD3:** reserved
3	0h RO	**BSesVld:** Indicates the Device mode transceiver status. Indicates the Device mode transceiver status. The core updates this bit when OEVTEN.OTGBDevVBUSChngEvnt is set. 1b0: B-session is not valid 1b1: B-session is valid Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
2	0h RO	**HstNegSts:** Host Negotiation Status: The core updates this bit when any of the following bits is set: n OEVTEN.OTGADevHNPChngEvnt n OEVTEN.OTGBDevHNPChngEvnt This bit indicates Host Negotiation Success or Failure. n 1'b0: Host negotiation failure. In A-device, for HS/FS, this indicates an imminent end of session indication from the core. In B-device, for HS/LS, it indicates that the timer used to wait for an A-device to signal a connection (b_ase0_brst_tmout in OTG 2.0) timed out resulting in B-device staying as B-peripheral. n 1'b1: Host negotiation success. This indicates that the host negotiation was successful. Note: This bit is applicable only for OTG 2.0 mode of operation.
1	0h RO	**SesReqSts:** Session Request Status: The core updates this bit when OEVTEN.OTGBDevSessVldDetEvnt is set. o 1'b0: Session request due to Vbus. This indicates that the session started due to Vbus without SRP detection by A-host. o 1'b1: Session request due to SRP. This indicates that the session started as a result of successful SRP detection by A-host. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
0	0h RO	**OEVTError:** Write Behavior: oneToClear OTG Event Error: There are no errors currently defined.

3.74.267 OEVTEN—Offset CC0Ch

OTG Events Enable Register

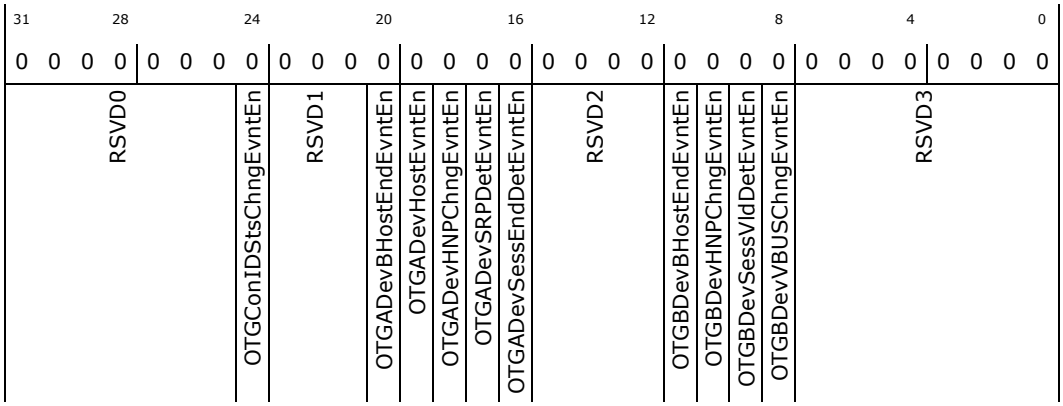
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OEVTEN: [BAR] + CC0Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RO	**RSVD0:** reserved
24	0h RW	**OTGConIDStsChngEvntEn:** Connector ID Status Change Event (OTGConIDStsChngEvnt) Set in both A-Dev/B-Dev Mode: This Event is generated when there is a change in connector ID status
23:21	0h RO	**RSVD1:** reserved
20	0h RW	**OTGADevBHostEndEvntEn:** A-device B-Host End Event Enable (OTGADevBHostEndEvntEn) When this bit is set, OEVT.OTGADevBHostEndEvnt is enabled. Else the event is disabled.
19	0h RW	**OTGADevHostEvntEn:** A-device host event: When this bit is set, OEVT.OTGADevHostEvnt is enabled. If not, the event is disabled
18	0h RW	**OTGADevHNPChngEvntEn:** A-Dev HNP Change EventEn: When this bit is set, OEVT.OTGADevHNPChngEvnt is enabled. If not, the event is disabled
17	0h RW	**OTGADevSRPDetEvntEn:** SRP Detect Event Enable: When this bit is set, OEVT.OTGADevSRPDetEvnt is enabled. If not, the event is disabled
16	0h RW	**OTGADevSessEndDetEvntEn:** Session End Detected Event Enable (OTGADevSessEndDetEvntEn) When this bit is set, OEVT.OTGADevSessEndEvnt is enabled. Else the event is disabled
15:12	0h RO	**RSVD2:** reserved
11	0h RW	**OTGBDevBHostEndEvntEn:** B-device B-Host End Event Enable: When this bit is set, OEVT.OTGBDevHostEndEvnt is enabled. If not, the event is disabled
10	0h RW	**OTGBDevHNPChngEvntEn:** B-Dev HNP Change Event Enable: When this bit is set, OEVT.OTGBDevHNPChngEvnt is enabled. If not, the event is disabled

Bit Range	Default & Access	Description
9	0h RW	**OTGBDevSessVldDetEvntEn:** Session Valid Detected Event Enable (OTGBDevSessVldDetEvntEn) Set in B-device Mode Only: This Event is asserted when there is a valid VBUS from A-device and B-device succeeds in starting a session.
8	0h RW	**OTGBDevVBUSChngEvntEn:** Vbus Change Event Enable: When this bit is set, OEVT.OTGBDevVBUSChngEvnt is enabled. If not, the event is disabled
7:0	0h RO	**RSVD3:** reserved

3.74.268 OSTS—Offset CC10h

flag Value After Reset: 0x819 OTG Status Register

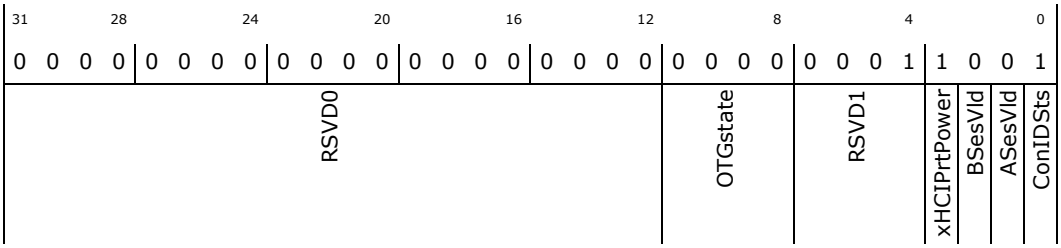
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSTS: [BAR] + CC10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000019h



Bit Range	Default & Access	Description
31:12	0h RO	**RSVD0:** reserved
11:8	0h RO	**OTGstate:** This is a debug field indicating the current state of the OTG state machine. Value Encoding 4'b0000 A_IDLE 4'b0001 A_WAIT_VRISE 4'b0010 A_WAIT_BCON 4'b0011 A_WAIT_VFALL 4'b0100 A_VBUS_ERR 4'b0101 A_HOST 4'b0110 A_SUSPEND 4'b1111 A_PERIPHERAL 4'b0111 A_WAIT_PPWR 4'b1000 B_IDLE 4'b1001 B_SRP_INIT 4'b1010 B_PERIPHERAL 4'b1011 B_WAIT_ACON 4'b1100 B_HOST 4'b1101 A_WAIT_SWITCH 4'b1110 B_WAIT _SWITCH
7:4	1h RO	**RSVD1:** reserved
3	1h RO	**xHCIPrtPower:** This bit reflects the PORTSC.PP bit in the xHCI register.

Bit Range	Default & Access	Description
2	0h RO	**BSesVld:** Indicates the Device mode transceiver status. Indicates the Device mode transceiver status. The core updates this bit when OEVTEN.OTGBDevVBUSChngEvnt is set. 1b0: B-session is not valid 1b1: B-session is valid Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
1	0h RO	**ASesVld:** Indicates the Host mode transceiver status. 1b0: A-session is not valid 1b1: A-session is valid
0	1h RO	**ConIDSts:** Connector ID Status: Indicates the connector ID status n 1'b0: The DWC_usb3 core is in A-device mode n 1'b1: The DWC_usb3 core is in B-device mode Note: The reset value of this field depends on the power-on value of the IDDIG signal from the PHY.

3.74.269 ADPCFG—Offset CC20h

ADP Configuration Register

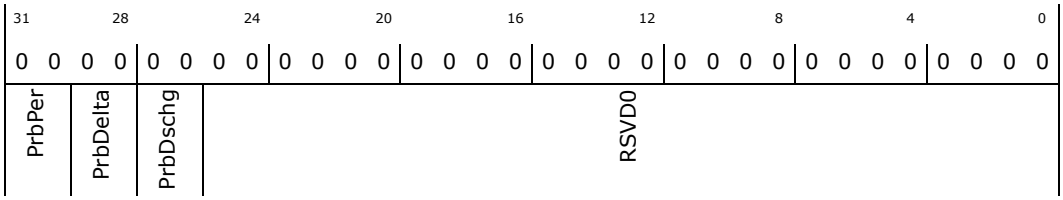
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ADPCFG: [BAR] + CC20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**PrbPer:** Probe Period: These bits set the T_ADP_PRB as follows: n 2'b00: 0.775 sec n 2'b01: 1.55 sec n 2'b10: 2.275 sec n 2'b11: Reserved The scaledown values for PrbPer are: n 2'b00: 12.5ms n 2'b01: 18.75ms n 2'b10: 25 ms n 2'b11: 31.25 ms
29:28	0h RW	**PrbDelta:** Probe Delta: These bits set the resolution for RTIM value. They are defined in units of 32 kHz clock cycles as follows: n2'b00: 1 cycles n 2'b01: 2 cycles n 2'b10: 3 cycles n 2'b11: 4 cycles For example, if this value is chosen to be 2'b01, it means that RTIM increments for every two 32 kHz clock cycles.
27:26	0h RW	**PrbDschg:** Probe Discharge: These bits set the time for TADP_DSCHG. They are defined as follows: n 2'b00: 4 msec n 2'b01: 8 msec n 2'b10: 16 msec n 2'b11: 32 msec The scaledown values for the PrbDschg are as follows: n 2'b00: 62.5 us n 2'b01: 125 us n 2'b10: 250 us n 2'b11: 500 us
25:0	0h RO	**RSVD0:** reserved

3.74.270 ADPCTL—Offset CC24h

ADP Control Register

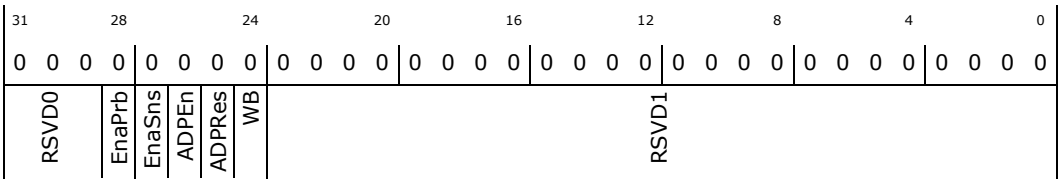
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ADPCTL: [BAR] + CC24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD0:** reserved
28	0h RW	**EnaPrb:** Enable Probe: When set to 1'b1 along with ADPEn, the core performs a probe operation.
27	0h RW	**EnaSns:** ADP Enable: When set to 1'b1, the core performs either ADP probing or sensing based on EnaPrb and EnaSns. ADPEn = 1'b0 gates the suspend clock for major portion of ADP related logic.
26	0h RW	**ADPEn:** ADP Enable: When set to 1'b1, the core performs either ADP probing or sensing based on EnaPrb and EnaSns. ADPEn = 1'b0 gates the suspend clock for major portion of ADP related logic.
25	0h RW	**ADPRes:** ADP Reset: When set to 1'b1, the ADP controller is reset. This bit is auto-cleared after the reset procedure is complete in the ADP controller.
24	0b RO	**WB:** Write Busy: n 1'b0: Write Completed n 1'b1: Write in Progress The application can read or write ADPCFG and ADPCTL registers only if this field is cleared. Hardware sets this bit when the write is in progress in the Suspend clock domain.
23:0	0h RO	**RSVD1:** reserved

3.74.271 ADPEVT—Offset CC28h

ADP Event Register

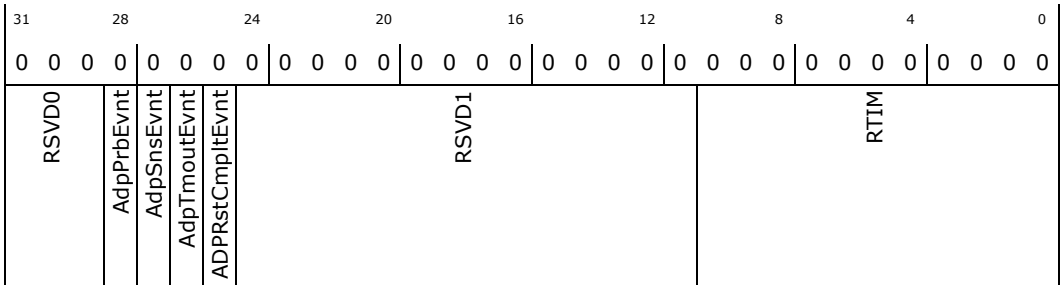
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ADPEVT: [BAR] + CC28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD0:** Reserved
28	0h RO	**AdpPrbEvnt:** Write Behavior: oneToClear ADP Probe Event: When this event is set, it means that the Vbus voltage is greater than VadpPrb or VadpPrb is reached.
27	0h RO	**AdpSnsEvnt:** Write Behavior: oneToClear ADP Sense Event: When this event is set, it means that the Vbus voltage is greater than VadpSns or VadpSns is reached.
26	0h RO	**AdpTmoutEvnt:** Write Behavior: oneToClear ADP Timeout Event: This event is relevant when ADP probe command is executed. When this event is set, it means that the ramp time is completed (GADPCTL.RTIM has reached its terminal value of 0x7FF). This is a debug feature that allows software to read the ramp time after each cycle.
25	0h RO	**ADPRstCmpltEvnt:** Write Behavior: oneToClear This event, when set, indicates that the ADP Reset command is successful
24:11	0h RO	**RSVD1:** reserved
10:0	0h RO	**RTIM:** RAMP TIME: These bits capture the latest time it took for Vbus to ramp from VADP_SINK to VADP_PRB. The bits are defined in units of 32 kHz clock cycles as follows: n 0x000: 1 cycles n 0x001: 2 cycles n 0x002: 3 cycles and so on till, n 0x7FF: 2048 cycles A time of 1024 cycles at 32 kHz corresponds to a time of 32 msec. Note for scaledown ramp_timeout, n PrbDelta = 2'b00 =) 6250 us n PrbDelta = 2'b01 =) 3125 us n PrbDelta = 2'b10 =) 1562.5 us n PrbDelta = 2'b11 =) 781.25 us

3.74.272 ADPEVTEN—Offset CC2Ch

ADP Event Enable Register

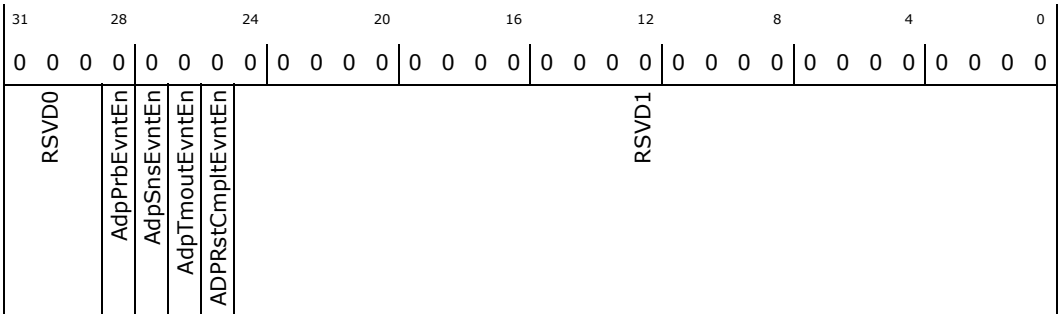
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ADPEVTEN: [BAR] + CC2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RSVD0:** Reserved
28	0h RW	**AdpPrbEvntEn:** ADP Probe Event Enable: When this bit is set, ADPPrbEvnt in ADPEVT register is enabled.
27	0h RW	**AdpSnsEvntEn:** ADP Sense Event Enable: When this bit is set, AdpSnsEvntEn in ADPEVT register is enabled.
26	0h RW	**AdpTmoutEvntEn:** ADP Timeout Event Enable: When this bit is set, AdpTmoutEvntEn in ADPEVT register is enabled.
25	0h RW	**ADPRstCmpltEvntEn:** ADP Reset complete Event Enable: When this bit is set, ADPRstCmpltEvnt in ADPEVT register is enabled.
24:0	0h RO	**RSVD1:** Reserved

3.74.273 BCFG—Offset CC30h

BC Configuration Register

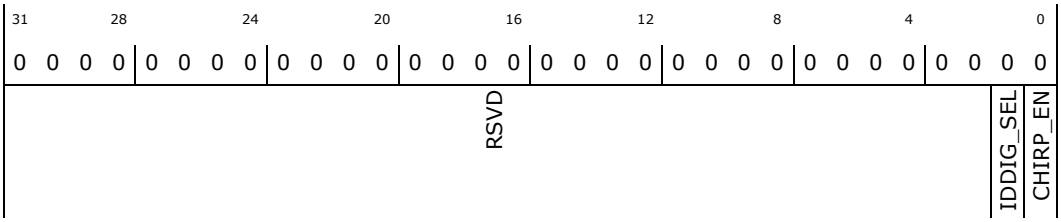
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BCFG: [BAR] + CC30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RO	**RSVD:** TBD

Bit Range	Default & Access	Description
1	0h RW	**IDDIG_SEL:** TBD
0	0h RW	**CHIRP_EN:** TBD

3.74.274 BCEVT—Offset CC38h

BC Event Register

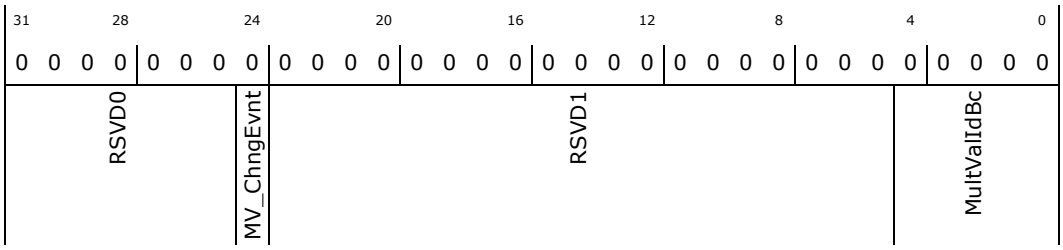
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BCEVT: [BAR] + CC38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RO	**RSVD0:** reserved
24	0h RO	**MV_ChngEvnt:**
23:5	0h RO	**RSVD1:** TBD
4:0	0h RO	**MultValIdBc:**

3.74.275 BCEVTEN—Offset CC3Ch

BC Event Enable Register

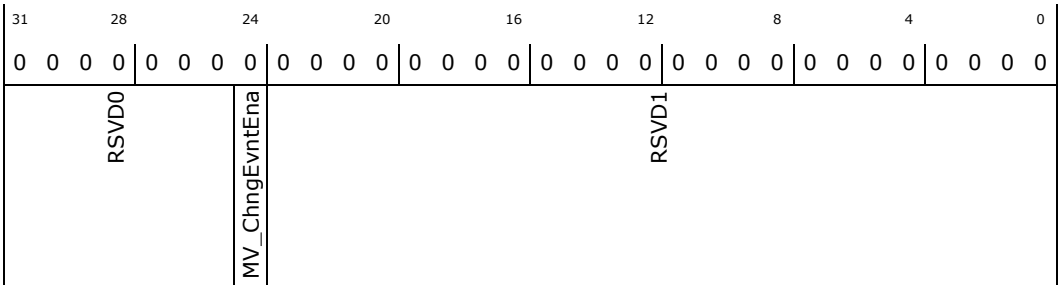
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BCEVTEN: [BAR] + CC3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RO	**RSVD0:** reserved
24	0h RW	**MV_ChngEvntEna:** TBD
23:0	0h RO	**RSVD1:** reserved

3.75 USB 3.0 Device PCI Configuration Registers

Table 83. Summary of USB 3.0 Device PCI Configuration Registers—0/22/0

Offset	Size	Register ID—Description	Default Value
A0h	4	"reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h" on page 4270	00000000h
A4h	4	"reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h" on page 4272	00000000h
A8h	4	"reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h" on page 4272	00000000h
ACh	4	"reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh" on page 4272	00000000h
C0h	4	"reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h" on page 4273	00000000h

3.75.1 reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h

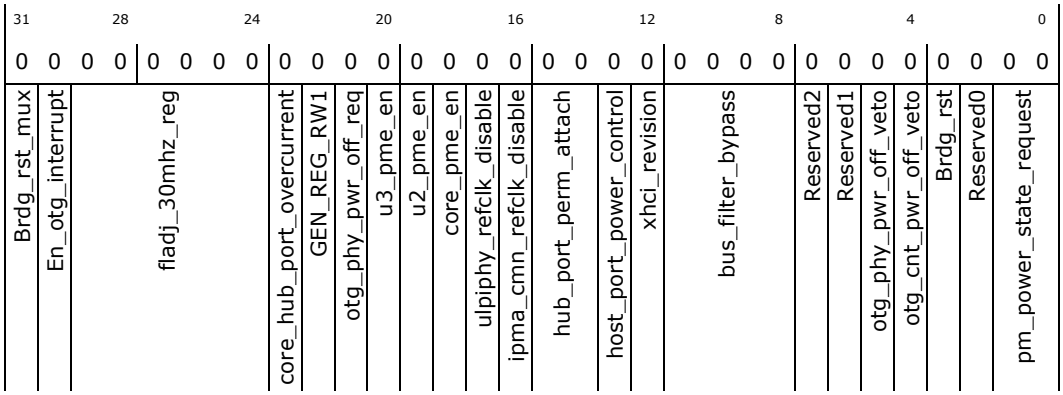
General Purpose Read Write Register1

Access Method

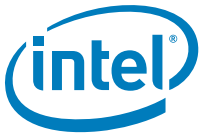
Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW1: [B:0, D:22, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**Brdg_rst_mux:** This is a mux the core reset between the normal reset or reset and with bdg_reset regRW1[3]
30	0b RW	**En_otg_interrupt:** enable the OTG interrupt
29:24	000000b RW	**fladj_30mhz_reg:** HS jitter adjusment
23	0b RW	**core_hub_port_overcurrent:** This is a generic register provided for product specific behavior
22	0b RW	**GEN_REG_RW1:** This is a generic register provided for product specific behavior



Bit Range	Default & Access	Description
21	0b RW	**otg_phy_pwr_off_req:** Indicates that the PHY power (both core and suspend well) can be turned off. Valid for D0 and RTD3hot
20	0b RW	**u3_pme_en:** Determines whether USB3 flis PME events are allowed to trigger PME events to brige/GPIO
19	0b RW	**u2_pme_en:** Determines whether ULPI flis PME events are allowed to trigger PME events to brige/GPIO
18	0b RW	**core_pme_en:** Determines whether core PME events are allowed to trigger PME events to brige/GPIO
17	0b RW	**ulpiphy_refclk_disable:** Feeds logic that generates the 19.2MHz clkreq signal
16	0b RW	**ipma_cmn_refclk_disable:** Feeds through PIMA PHY into 25MHz clkreq signal
15:14	00b RW	**hub_port_perm_attach:** Indicates if the device attached to a downstream port is permanently attached or not
13	0b RW	**host_port_power_control:** This port defines the bit [3] of Capability Parameters (HCCPARAMS). Change the PPC value through the pin Port Power Control (PPC). This indicates whether the host controller implementation includes port power control. ? 0 - Indicates that the port does not have port power switches. ? 1 - Indicates that the port has port power switches.
12	0b RW	**xhci_revision:** This signal is used to select the xHCI revision that the host controller complies with
11:8	0000b RW	**bus_filter_bypass:** Bus Filter Bypass. Disables the internal bus filters that are enabled by DWC_USB3_EN_BUS_FILTERS coreConsultant parameter. This static signal is present only when DWC_USB3_EN_BUS_FILTERS is 1. It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core.
7	0b RW	**Reserved2:** reserved
6	0b RW	**Reserved1:** reserved
5	0b RW	**otg_phy_pwr_off_veto:** Indicates that PHY suspend power should not power off even on RTD3hot (Note that the PHY core power is turned off during RTD3hot in line with the OTG core, as a function of otg_cnt_pwr_off_veto)
4	0b RW	**otg_cnt_pwr_off_veto:** Indicates that controller power should not power off even on RTD3hot.Also a veto signal to keep LPPLL on. Note: Currently LPPLL results in a veto for S0iX flows
3	0b RW	**Brdg_rst:** reset the core see also regRW1[31]
2	0b RW	**Reserved0:** reserved
1:0	00b RW	**pm_power_state_request:** This port defines the PCI power management state requested by the software. When the core is configured with two power rail support (DWC_USB3_EN_PWROPT=2), the valid states are: ? 00: D0 ? 11: D3 Active State

3.75.2 reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h

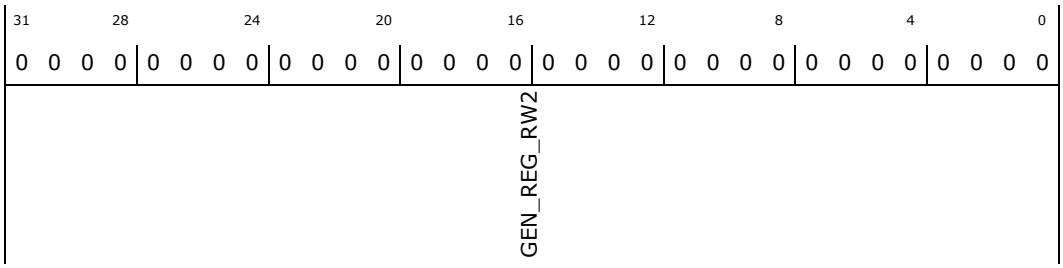
General Purpose Read Write Register2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW2: [B:0, D:22, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW2:** Reserved.

3.75.3 reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h

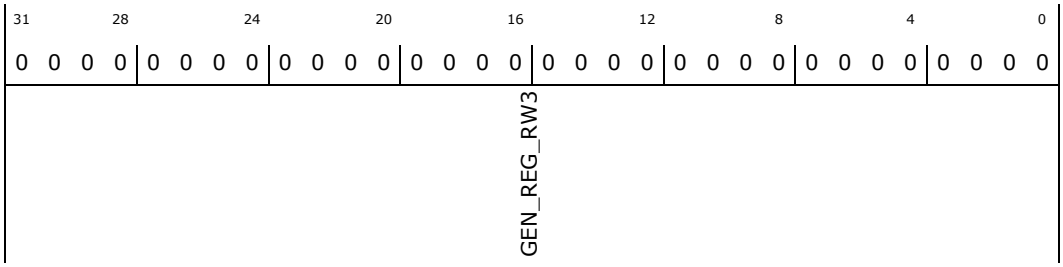
General Purpose Read Write Register3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW3: [B:0, D:22, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW3:** Reserved.

3.75.4 reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh

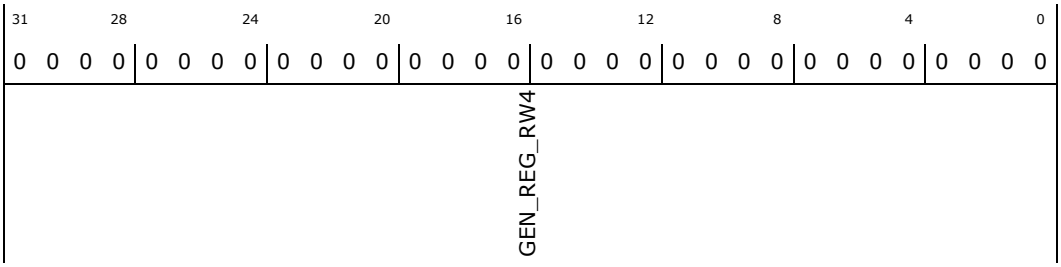
General Purpose Read Write Register4

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_REGRW4: [B:0, D:22, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**GEN_REG_RW4:** Reserved.

3.75.5 reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h

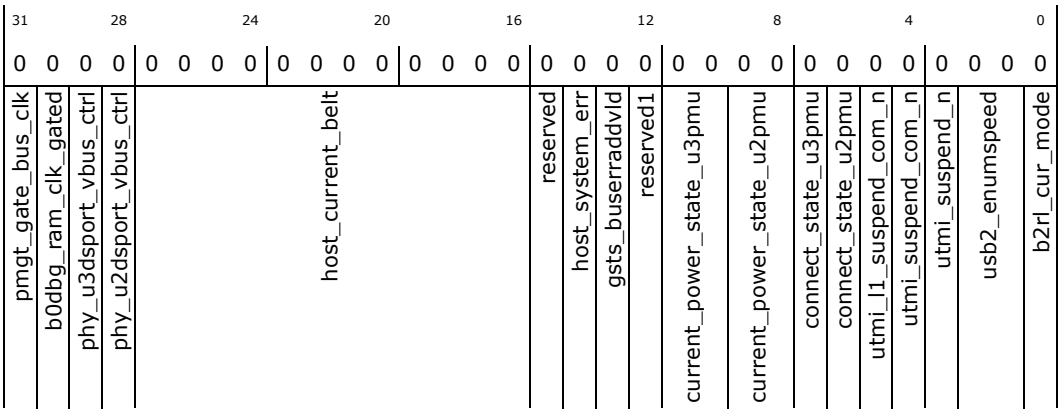
General Purpose Input Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GEN_INPUT_REGRW: [B:0, D:22, F:0] + C0h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**pmgt_gate_bus_clk:** Indicates that the conditions are appropriate for some internal modules to receive a gated bus_clk. This signal is used by the test environment to verify low power operation.

Bit Range	Default & Access	Description
30	0b RO	**b0dbg_ram_clk_gated:** Indicates that the internal ram_clk is being gated. It indicates whether ram_clk_gated is turned on or off. This signal is used by the test environment to verify low power
29	0b RO	**phy_u3dsport_vbus_ctrl:** When the PMU is in the D0 state, this PHY-side output is fed directly from the core without any intervening logic. The core-side input is called core_u3dsport_vbus_ctrl
28	0b RO	**phy_u2dsport_vbus_ctrl:** When the PMU is in the D0 state, this PHY-side output is fed directly from the core without any intervening logic. The core-side input is called core_u2dsport_vbus_ctrl
27:16	000h RO	**host_current_belt:** Current BELT Value. This signal indicates the minimum value of all received BELT values and the BELT that is set by the Set LTV command. This signal is valid only in Host mode.
15	0b RO	**reserved:** Reserved.
14	0b RO	**host_system_err:** Host System Error. Indicates that a Host System Error has occurred as reflected in the USBSTS.HSE field.
13	0b RO	**gsts_buserraddvld:** Bus error
12	0b RO	**reserved1:** Reserved.
11:10	00b RO	**current_power_state_u3pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
9:8	00b RO	**current_power_state_u2pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
7	0b RO	**connect_state_u3pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in U3). When '0', indicates the PMU has no connection to the host or any device.
6	0b RO	**connect_state_u2pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in L1, L2). When '0', indicates the PMU has no connection to the host or any device
5	0b RO	**utmi_l1_suspend_com_n:** Common L1 suspend
4	0b RO	**utmi_suspend_com_n:** Common suspend
3	0b RO	**utmi_suspend_n:** USB 2.0 Port Suspend
2:1	00b RO	**usb2_enumspeed:** Device Enumerated Speed
0	0b RO	**b2rl_cur_mode:** Current Mode. Current Mode 1'b0 Host ,1'b1 Device